

SNx4AHCT32 Quadruple 2-Input Positive-OR Gates

1 Features

- Inputs are TTL-voltage compatible
- Latch-up performance exceeds 250 mA per JESD 17
- ESD protection exceeds JESD 22
 - 2000-V Human-Body Model
 - 200-V Machine Model
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters

2 Applications

- [Electronic points-of-sale](#)
- [Telecom infrastructure](#)
- [Network switches](#)
- [Test and measurement](#)

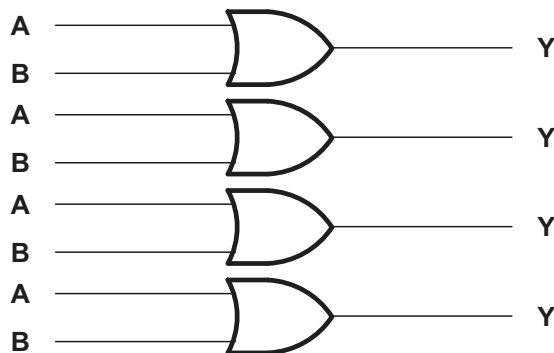
3 Description

The SNx4AHCT32 devices are quadruple 2-input positive-OR gates. These devices perform the Boolean function $Y = \overline{A} \times \overline{B}$ or $Y = A + B$ in positive logic.

Package Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------------|--------------------|
| SN54AHCT32 | J (CDIP, 14) | 19.56 mm × 6.67 mm |
| | W (CFP, 14) | 13.09 mm × 6.92 mm |
| | FK (LCCC, 20) | 8.89 mm × 8.89 mm |
| SN74AHCT32 | N (PDIP, 14) | 19.3 mm × 6.35 mm |
| | D (SOIC, 14) | 8.65 mm × 3.91 mm |
| | NS (SOP, 14) | 10.30 mm × 5.30 mm |
| | DB (SSOP, 14) | 6.20 mm × 5.30 mm |
| | PW (TSSOP, 14) | 5.00 mm × 4.40 mm |
| | DGV (TVSOP, 14) | 3.60 mm × 4.40 mm |
| | RGY (VQFN, 14) | 3.50 mm × 3.50 mm |
| | BQA (WQFN, 14) | 3.00 mm × 2.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision N (May 2023) to Revision O (July 2023) | Page |
|--|-------------|
| <ul style="list-style-type: none"> Updated thermal values for RθJA: PW = 125.1 to 147.7, RθJC(top) = 53.7 to 77.4, RθJB = 66.9 to 90.9, ΨJT = 7.6 to 27.2, ΨJB = 66.3 to 90.2, all values in °C/W.” | 5 |

| Changes from Revision M (October 2014) to Revision N (May 2023) | Page |
|---|-------------|
| <ul style="list-style-type: none"> Updated the numbering format for tables, figures, and cross-references throughout the document..... Updated the <i>Package Information</i> table..... Added the <i>BQA</i> package to the data sheet..... | 1 |

5 Pin Configuration and Functions



Figure 5-1. SN54AHCT32 J or W Package, 14-Pin (Top View)
SN74AHCT32 D, DB, DGV, N, NS, or PW Package, 14-Pin (Top View)

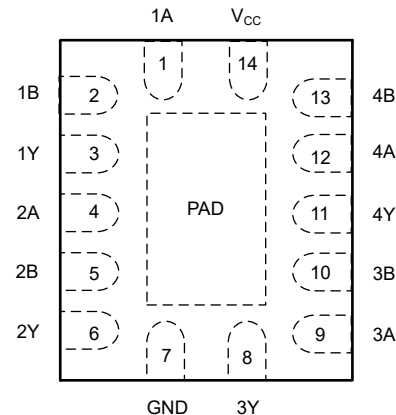


Figure 5-2. SN74AHCT32 RGY or BQA Package, 14-Pin (Top View)

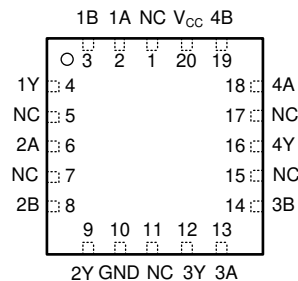


Figure 5-3. SN54AHCT32 FK Package, 20-Pin (Top View)

Table 5-1. Pin Functions

| NAME | PIN | | | | TYPE ⁽¹⁾ | DESCRIPTION |
|-----------------|-----------------------|----------|------------|---------------------|---------------------|---------------|
| | SN74AHCT32 | | SN54AHCT32 | | | |
| | D, DB, DGV, N, NS, PW | RGY, BQA | J, W | FK | | |
| 1A | 1 | 1 | 1 | 2 | I | 1A Input |
| 1B | 2 | 2 | 2 | 3 | I | 1B Input |
| 1Y | 3 | 3 | 3 | 4 | O | 1Y Output |
| 2A | 4 | 4 | 4 | 6 | I | 2A Input |
| 2B | 5 | 5 | 5 | 8 | I | 2B Input |
| 2Y | 6 | 6 | 6 | 9 | O | 2Y Output |
| 3Y | 8 | 8 | 8 | 12 | O | 3Y Output |
| 3A | 9 | 9 | 9 | 13 | I | 3A Input |
| 3B | 10 | 10 | 10 | 14 | I | 3B Input |
| 4Y | 11 | 11 | 11 | 16 | O | 4Y Output |
| 4A | 12 | 12 | 12 | 18 | I | 4A Input |
| 4B | 13 | 13 | 13 | 19 | I | 4B Input |
| GND | 7 | 7 | 7 | 10 | — | Ground Pin |
| NC | — | — | — | 1, 5, 7, 11, 15, 17 | — | No Connection |
| V _{CC} | 14 | 14 | 14 | 20 | I | Power Pin |
| Thermal Pad | — | PAD | — | — | — | Thermal Pad |

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|---|--|-----------------------|------|
| V _{CC} | Supply voltage range | -0.5 | 7 | V |
| V _I | Input voltage range ⁽²⁾ | -0.5 | 7 | V |
| V _O | Output voltage range ⁽²⁾ | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < 0 | -20 | mA |
| I _{OK} | Output clamp current | V _O < 0 or V _O > V _{CC} | ±20 | mA |
| I _O | Continuous output current | V _O = 0 to V _{CC} | ±25 | mA |
| | Continuous current through V _{CC} or GND | | ±50 | mA |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|----------------------------|-------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM) | ±1000 |
| | | Charged device model (CDM) | ±750 |

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | | SN54AHCT32 | | SN74AHCT32 | | UNIT |
|-----------------|------------------------------------|------------|-----------------|------------|-----------------|------|
| | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V _{IH} | High-level input voltage | 2 | | 2 | | V |
| V _{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V _I | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| V _O | Output voltage | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | | -8 | | -8 | mA |
| I _{OL} | Low-level output current | | 8 | | 8 | mA |
| Δt/Δv | Input transition rise or fall rate | | 20 | | 20 | ns/V |
| T _A | Operating free-air temperature | -55 | 125 | -40 | 125 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs (SCBA004)*.

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | SN74AHCT32 | | | | | | | | UNIT |
|-------------------------------|--|------------|-------|-------|------|------|-------|------|------|------|
| | | D | DB | DGV | N | NS | PW | RGY | BQA | |
| | | 14 PINS | | | | | | | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 97.5 | 109.5 | 133.3 | 59.7 | 92.2 | 147.7 | 59.0 | 88.3 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 58.7 | 62.1 | 55.6 | 47.3 | 49.8 | 77.4 | 72.5 | 90.9 | |
| R _{θJB} | Junction-to-board thermal resistance | 51.8 | 56.9 | 66.3 | 39.5 | 51.0 | 90.9 | 35.0 | 56.8 | |
| Ψ _{JT} | Junction-to-top characterization parameter | 22.6 | 22.6 | 7.8 | 32.4 | 15.7 | 27.2 | 3.9 | 9.9 | |
| Ψ _{JB} | Junction-to-board characterization parameter | 51.6 | 56.3 | 56.6 | 39.4 | 50.6 | 90.2 | 35.1 | 56.7 | |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | — | — | — | — | — | — | 15.4 | 33.4 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54AHCT32 | | SN74AHCT32 | | -40°C to 125°C SN74AHCT32 | | UNIT |
|---------------------------------|---|-----------------|-----------------------|-----|------|------------|-------------------|------------|------|------------------------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = -50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | 4.4 | V | |
| | I _{OH} = -8 mA | | 3.94 | | | 3.8 | | 3.8 | | 3.8 | | |
| V _{OL} | I _{OL} = 50 μA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | | V | |
| | I _{OL} = 8 mA | | | | 0.36 | | 0.44 | | 0.44 | | | 0.44 |
| I _I | V _I = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1 ⁽¹⁾ | | ±1 | | ±1 | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 2 | | 20 | | 20 | | 20 | μA |
| ΔI _{CC} ⁽²⁾ | One input at 3.4 V, Other inputs at V _{CC} or GND | 5.5 V | | | 1.35 | | 1.5 | | 1.5 | | 1.5 | mA |
| C _i | V _I = V _{CC} or GND | 5 V | | | 2 | | 10 | | 10 | | 10 | pF |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

6.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see [Figure 7-1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | SN54AHCT32 | | SN74AHCT32 | | -40°C to 125°C SN74AHCT32 | | UNIT |
|------------------|--------------|-------------|------------------------|-----------------------|--------------------|------------------|------------------|------------|-----|------------------------------|-----|------|
| | | | | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | A or B | Y | C _L = 15 pF | 5 ⁽¹⁾ | 6.9 ⁽¹⁾ | 1 ⁽¹⁾ | 8 ⁽¹⁾ | 1 | 8 | 1 | 9 | ns |
| t _{PHL} | | | | 5 ⁽¹⁾ | 6.9 ⁽¹⁾ | 1 ⁽¹⁾ | 8 ⁽¹⁾ | 1 | 8 | 1 | 9 | |
| t _{PLH} | A or B | Y | C _L = 50 pF | 5.5 | 7.9 | 1 | 9 | 1 | 9 | 1 | 10 | ns |
| t _{PHL} | | | | 5.5 | 7.9 | 1 | 9 | 1 | 9 | 1 | 10 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.7 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

| PARAMETER | | SN74AHCT32 | | | UNIT |
|-------------|--|------------|------|------|------|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic V_{OL} | | 0.4 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic V_{OL} | | -0.4 | -0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic V_{OH} | | 4.5 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

(1) Characteristics are for surface-mount packages only.

6.8 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|-----------|-----------------------------|------|------|
| C_{pd} | No load, $f = 1\text{ MHz}$ | 11.5 | pF |

6.9 Typical Characteristics

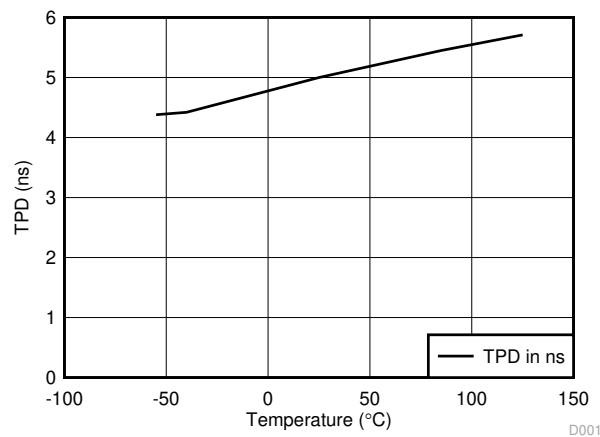
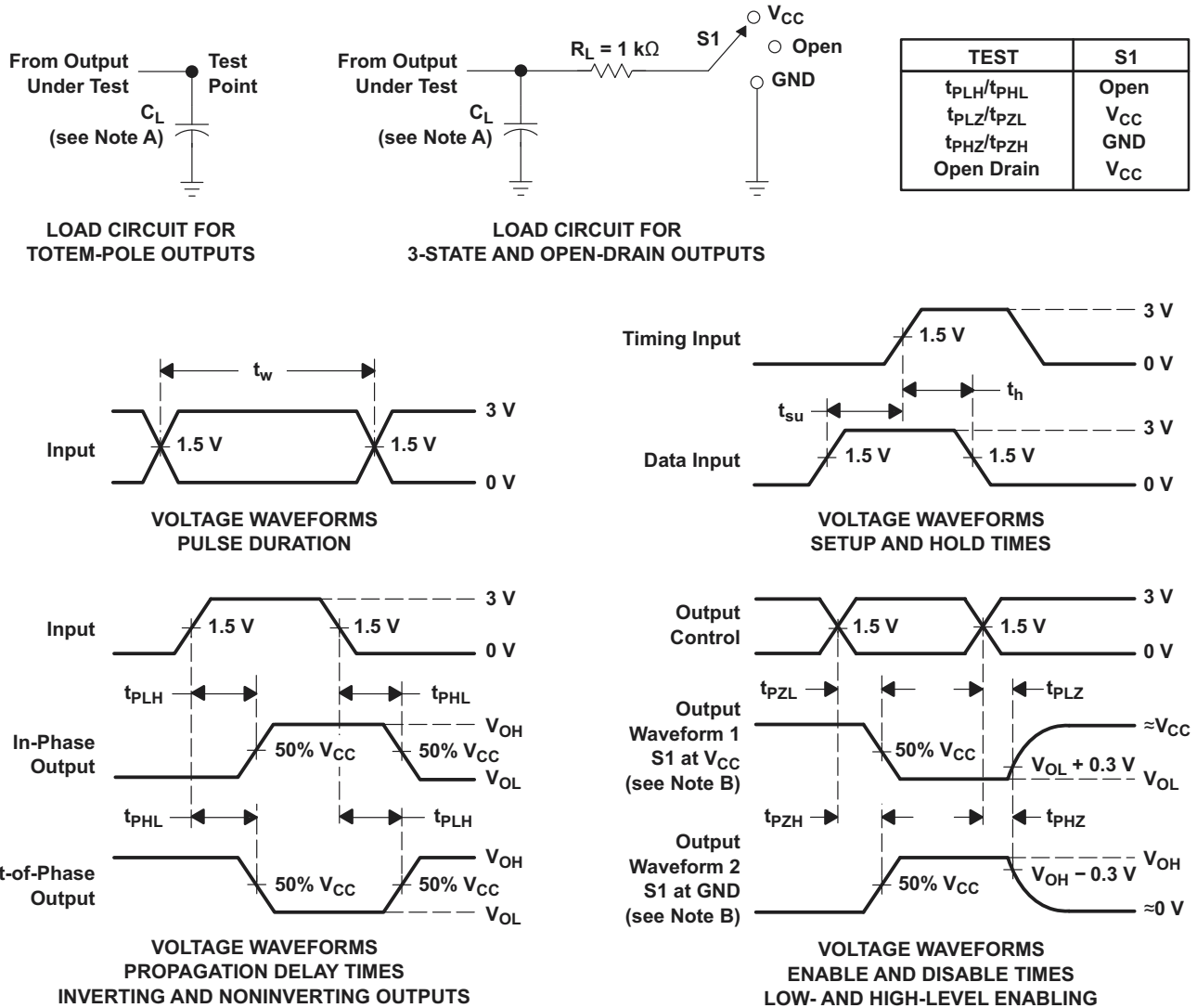


Figure 6-1. TPD vs Temperature

7 Parameter Measurement Information



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

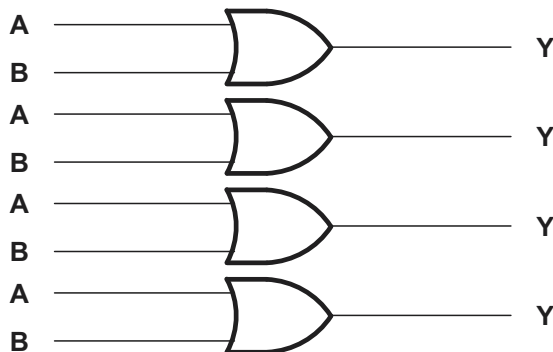
Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SNx4AHCT32 is a quadruple 2-input positive-OR gate with low drive that will produce slow rise and fall times. This slow transition reduces ringing on the output signal. The device has TTL inputs that allow up translation from 3.3 V to 5 V. The inputs are high impedance when $V_{CC} = 0$ V.

8.2 Functional Block Diagram



8.3 Feature Description

- Slow rise and fall time on outputs allows for low-noise outputs
- TTL inputs allow up translation from 3.3 V to 5 V

8.4 Device Functional Modes

**Table 8-1. Function Table
(Each Gate)**

| INPUTS | | OUTPUT Y |
|--------|---|-------------|
| A | B | |
| H | X | H |
| X | H | H |
| L | L | L |

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SNx4AHCT32 is a low-drive CMOS device that can be used for a multitude of bus-interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The TTL inputs can accept voltages down to 3.3 V and can translate up to 5 V.

9.2 Typical Application

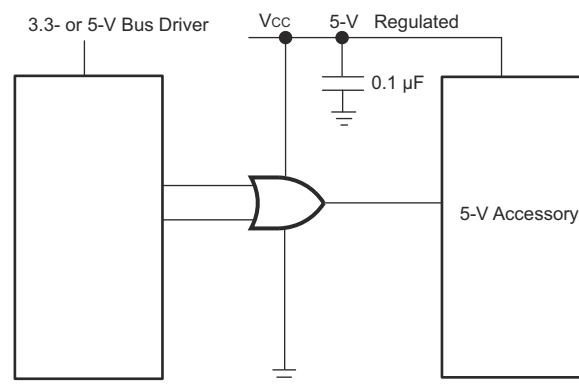


Figure 9-1. Typical Application Diagram for a Single Gate

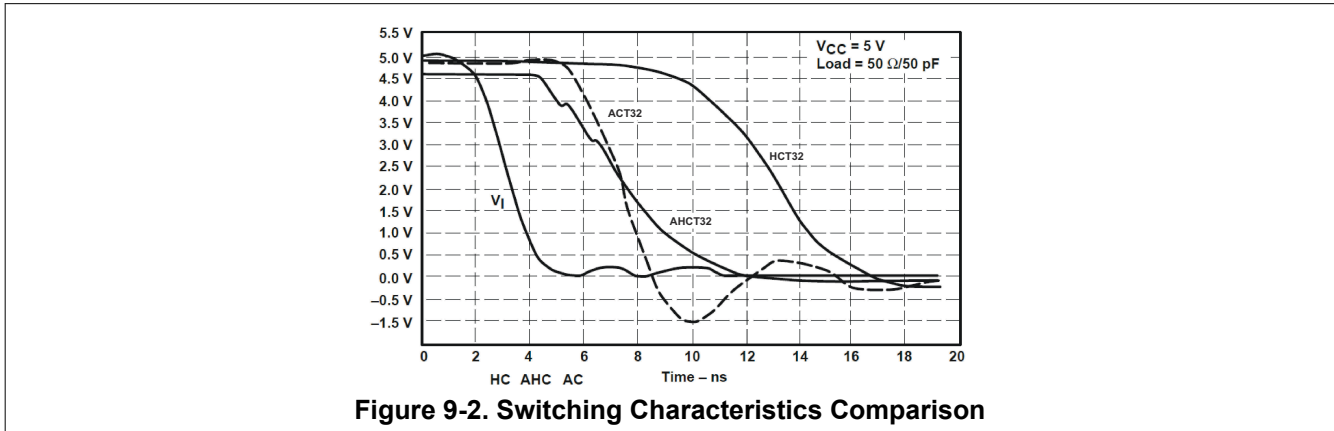
9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

- Recommended input conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the [Recommended Operating Conditions](#) table.
 - For specified high and low levels, see V_{IH} and V_{IL} in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
- Recommend output conditions:
 - Load currents should not exceed 25 mA per output and 50 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

9.2.3 Application Curves



9.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply-voltage rating located in [Recommended Operating Conditions](#).

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins then a 0.01 μF or a 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and a 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 9-3](#) shows the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

9.4.2 Layout Example

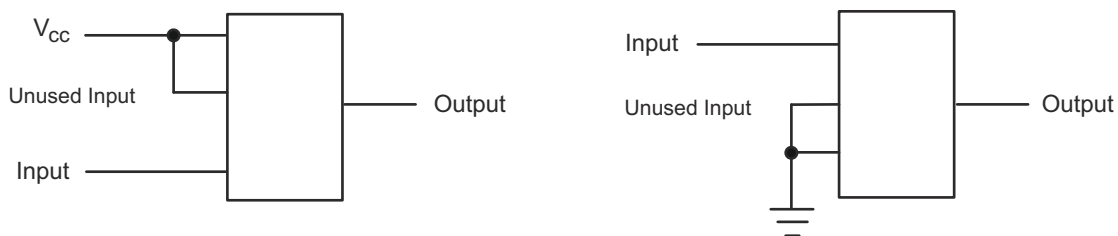


Figure 9-3. Layout Diagram

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|----------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|--|
| 5962-9682601Q2A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 9682601Q2A SNJ54AHCT 32FK |
| 5962-9682601QCA | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9682601QC A SNJ54AHCT32J |
| 5962-9682601QDA | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9682601QD A SNJ54AHCT32W |
| SN74AHCT32BQAR | Active | Production | WQFN (BQA) 14 | 3000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | AHCT32 |
| SN74AHCT32BQAR.A | Active | Production | WQFN (BQA) 14 | 3000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | AHCT32 |
| SN74AHCT32D | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | -40 to 85 | AHCT32 |
| SN74AHCT32DBR | Active | Production | SSOP (DB) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB32 |
| SN74AHCT32DBR.A | Active | Production | SSOP (DB) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB32 |
| SN74AHCT32DGVR | Active | Production | TVSOP (DGV) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB32 |
| SN74AHCT32DGVR.A | Active | Production | TVSOP (DGV) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB32 |
| SN74AHCT32DR | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT32 |
| SN74AHCT32DR.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT32 |
| SN74AHCT32N | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 125 | SN74AHCT32N |
| SN74AHCT32N.A | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 125 | SN74AHCT32N |
| SN74AHCT32NSR | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT32 |
| SN74AHCT32NSR.A | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT32 |
| SN74AHCT32PW | Obsolete | Production | TSSOP (PW) 14 | - | - | Call TI | Call TI | -40 to 125 | HB32 |
| SN74AHCT32PWR | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | HB32 |
| SN74AHCT32PWR.A | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB32 |
| SN74AHCT32RGYR | Active | Production | VQFN (RGY) 14 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HB32 |
| SN74AHCT32RGYR.A | Active | Production | VQFN (RGY) 14 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HB32 |
| SNJ54AHCT32FK | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 9682601Q2A SNJ54AHCT 32FK |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|--|
| SNJ54AHCT32FK.A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 9682601Q2A SNJ54AHCT 32FK |
| SNJ54AHCT32J | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9682601QC A SNJ54AHCT32J |
| SNJ54AHCT32J.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9682601QC A SNJ54AHCT32J |
| SNJ54AHCT32W | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9682601QD A SNJ54AHCT32W |
| SNJ54AHCT32W.A | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9682601QD A SNJ54AHCT32W |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHCT32, SN74AHCT32 :

- Catalog : [SN74AHCT32](#)

- Automotive : [SN74AHCT32-Q1](#), [SN74AHCT32-Q1](#)

- Enhanced Product : [SN74AHCT32-EP](#), [SN74AHCT32-EP](#)

- Military : [SN54AHCT32](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHCT32BQAR | WQFN | BQA | 14 | 3000 | 180.0 | 12.4 | 2.8 | 3.3 | 1.1 | 4.0 | 12.0 | Q1 |
| SN74AHCT32DBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74AHCT32DGVR | TVSOP | DGV | 14 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHCT32DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74AHCT32NSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AHCT32PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHCT32RGR | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHCT32BQAR | WQFN | BQA | 14 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74AHCT32DBR | SSOP | DB | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHCT32DGVR | TVSOP | DGV | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHCT32DR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74AHCT32NSR | SOP | NS | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHCT32PWR | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHCT32RGYR | VQFN | RGY | 14 | 3000 | 353.0 | 353.0 | 32.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9682601Q2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-9682601QDA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74AHCT32N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AHCT32N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AHCT32N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AHCT32N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54AHCT32FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54AHCT32FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54AHCT32W | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54AHCT32W.A | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

BQA 14

WQFN - 0.8 mm max height

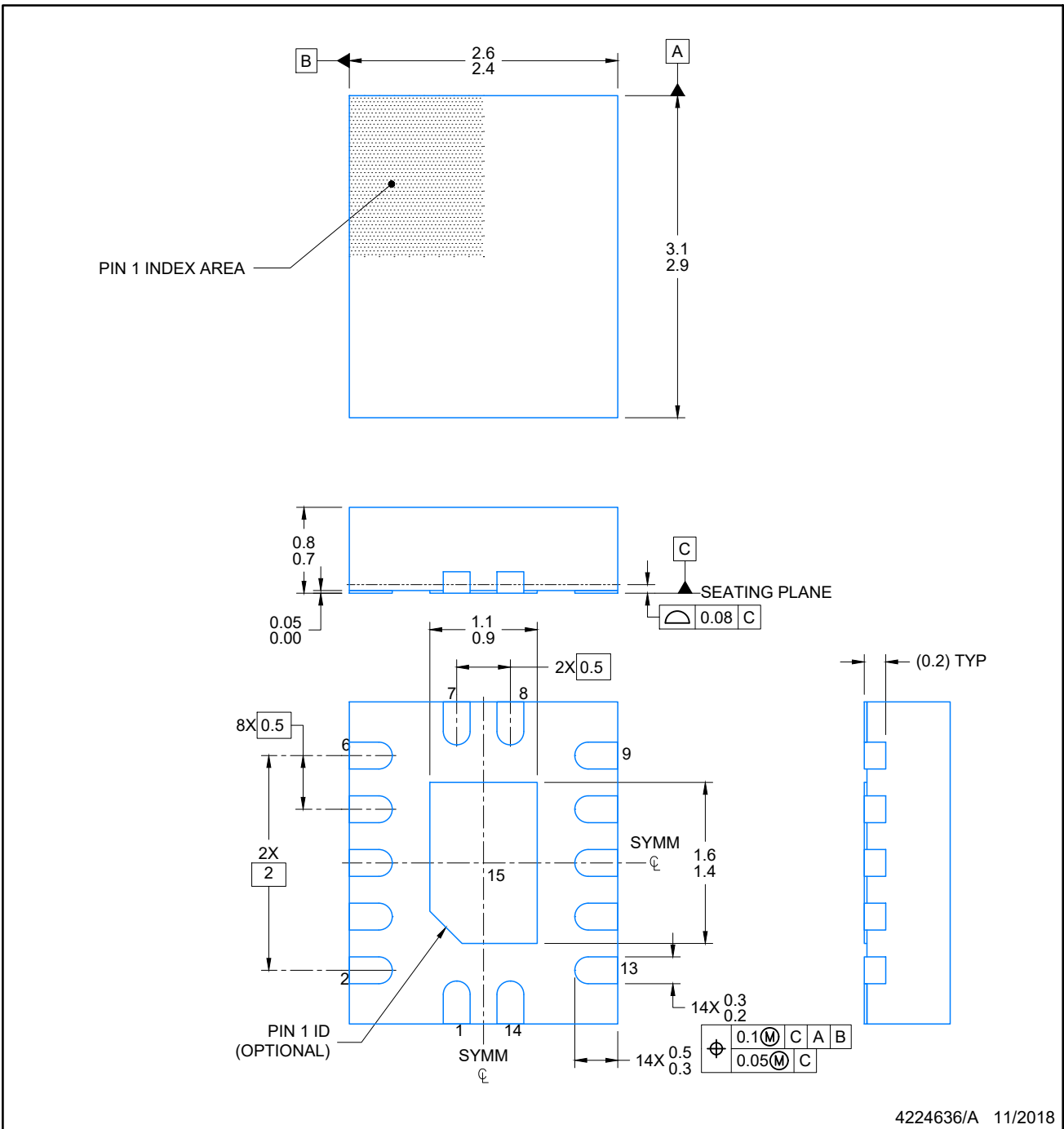
2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227145/A



4224636/A 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 88% PRINTED COVERAGE BY AREA
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G



J0014A

PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

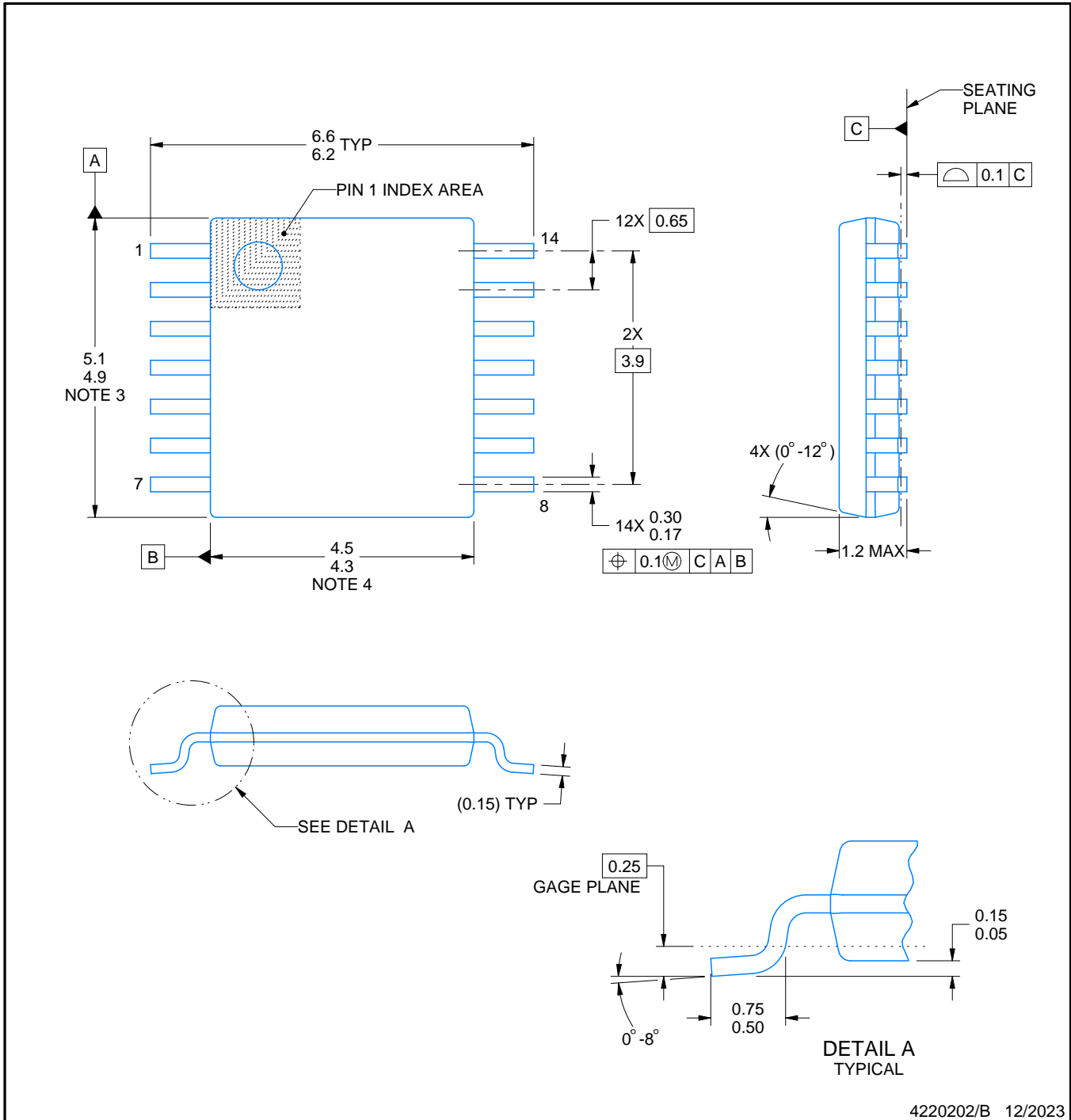
PW0014A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

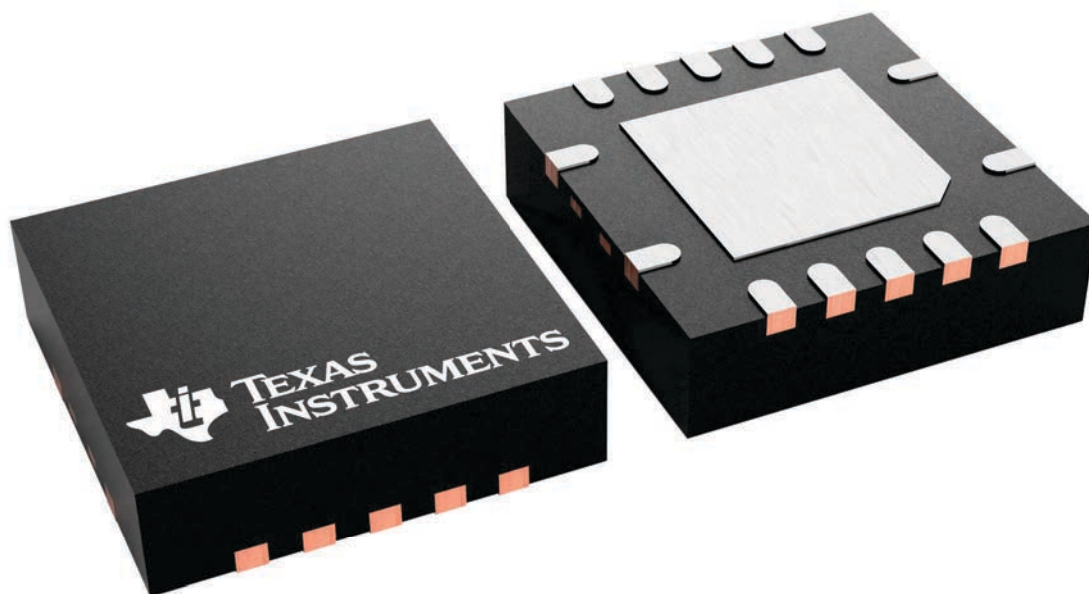
RGY 14

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

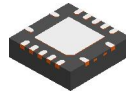
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231541/A

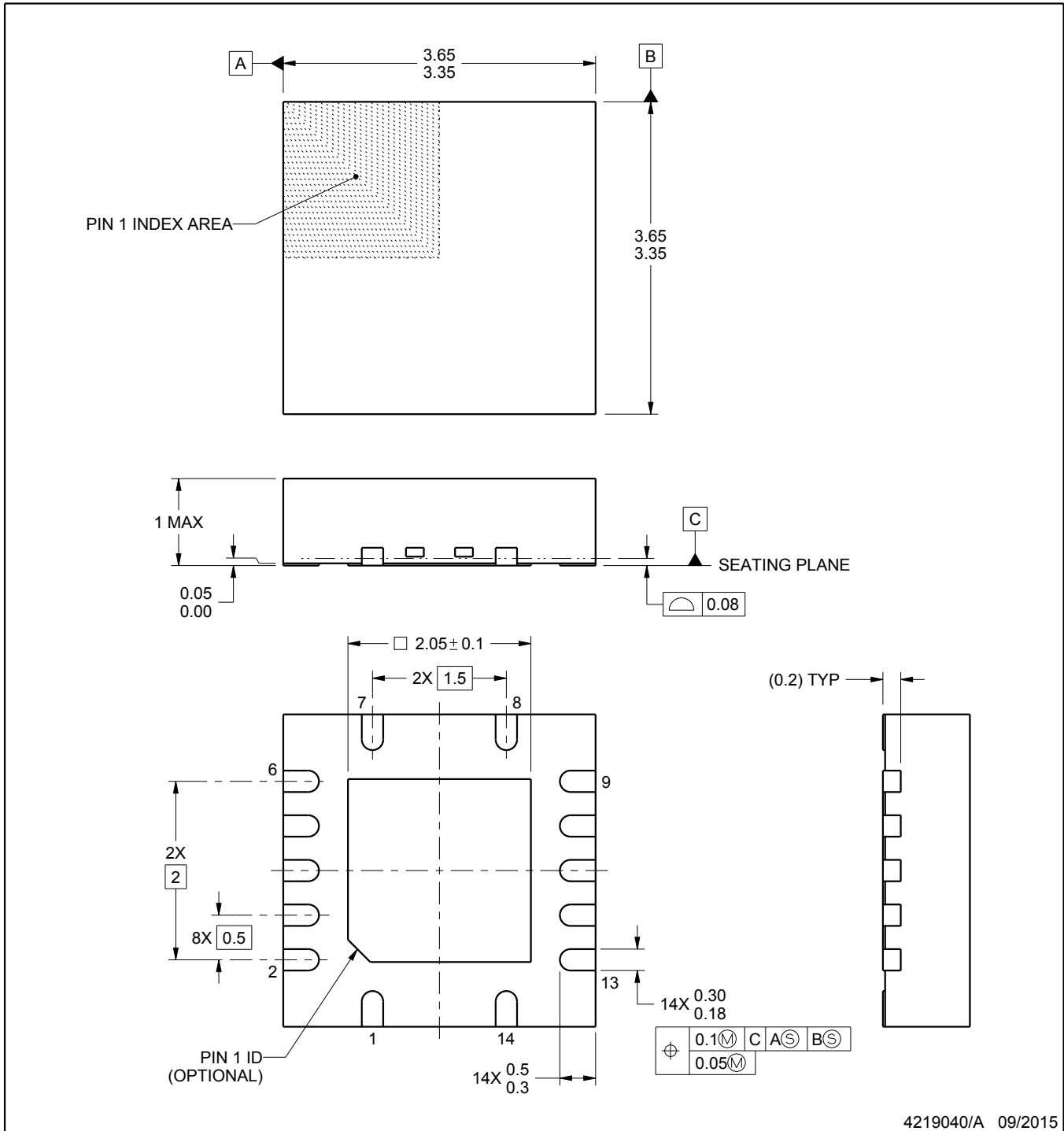
RGY0014A



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219040/A 09/2015

NOTES:

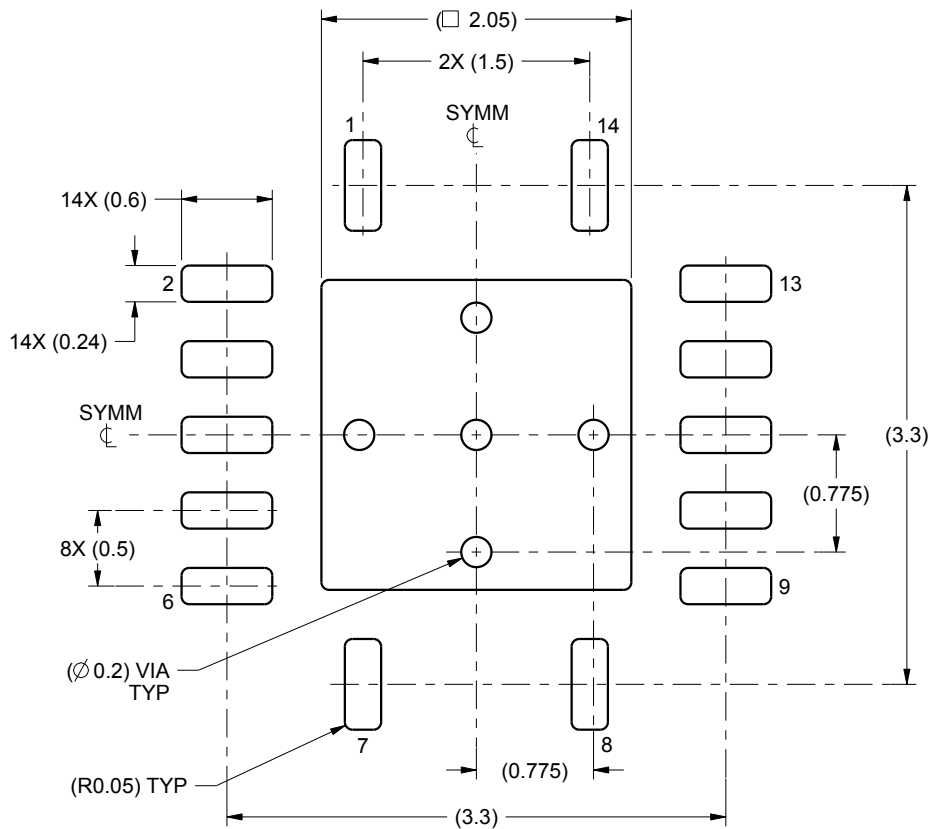
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

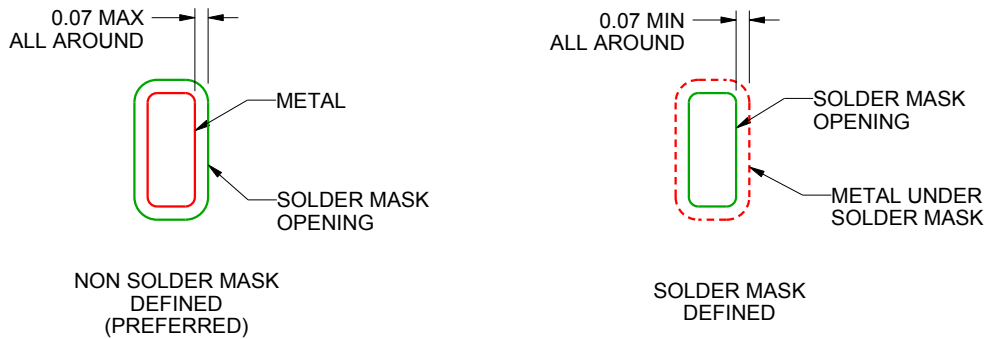
RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

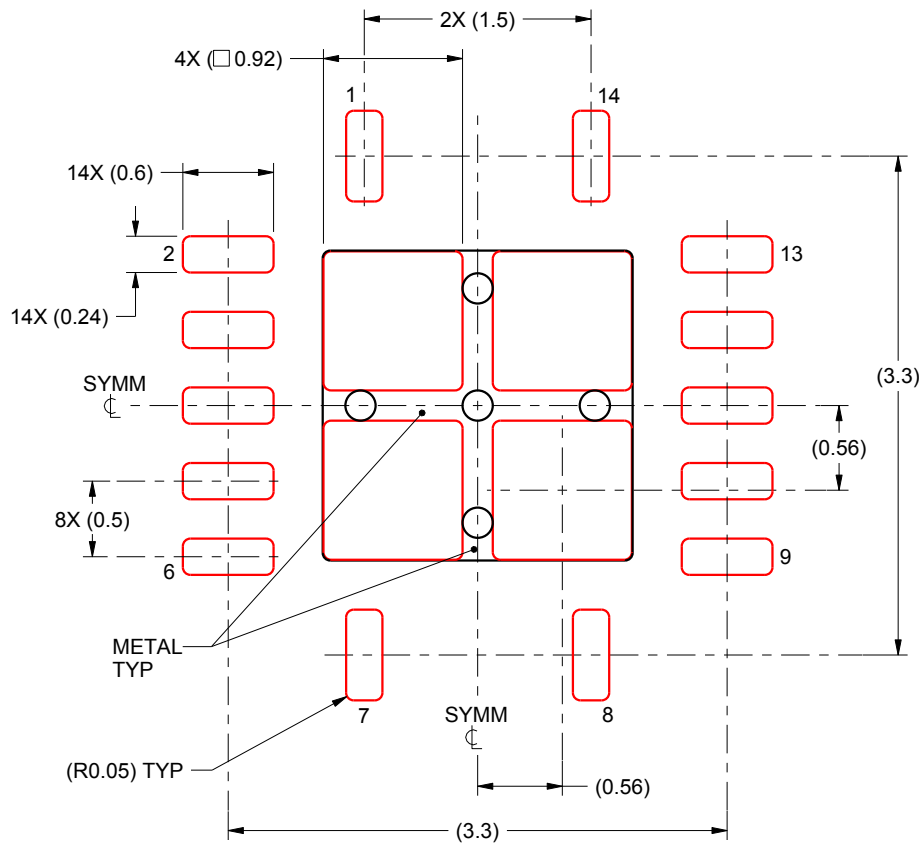
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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