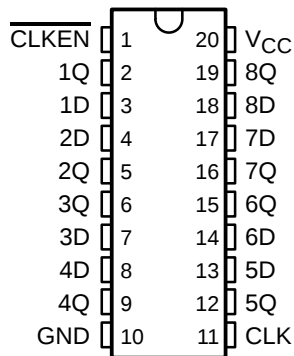


SN54HCT377, SN74HCT377 OCTAL D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

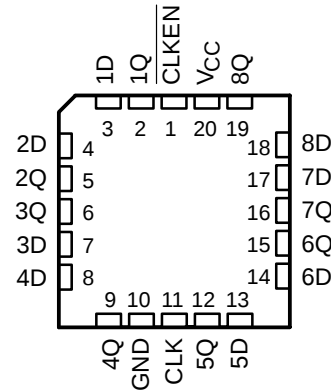
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- Operating Voltage Range of 4.5 V to 5.5 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 12$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Inputs Are TTL-Voltage Compatible
- Contain Eight Flip-Flops With Single-Rail Outputs
- Clock Enable Latched to Avoid False Clocking
- Applications Include:
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators

SN54HCT377 . . . J OR W PACKAGE
SN74HCT377 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT377 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These devices are positive-edge-triggered D-type flip-flops. The 'HCT377 devices are similar to the 'HCT273 devices, but feature a latched clock-enable (CLKEN) input instead of a common clear.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse if CLKEN is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output. These devices are designed to prevent false clocking by transitions at CLKEN.

ORDERING INFORMATION

T _A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74HCT377N	HCT377
	SOIC – DW	Tube	SN74HCT377DW	
		Tape and reel	SN74HCT377DWR	
–55°C to 125°C	CDIP – J	Tube	SNJ54HCT377J	SNJ54HCT377J
	CFP – W	Tube	SNJ54HCT377W	SNJ54HCT377W
	LCCC – FK	Tube	SNJ54HCT377FK	SNJ54HCT377FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
INSTRUMENTS**

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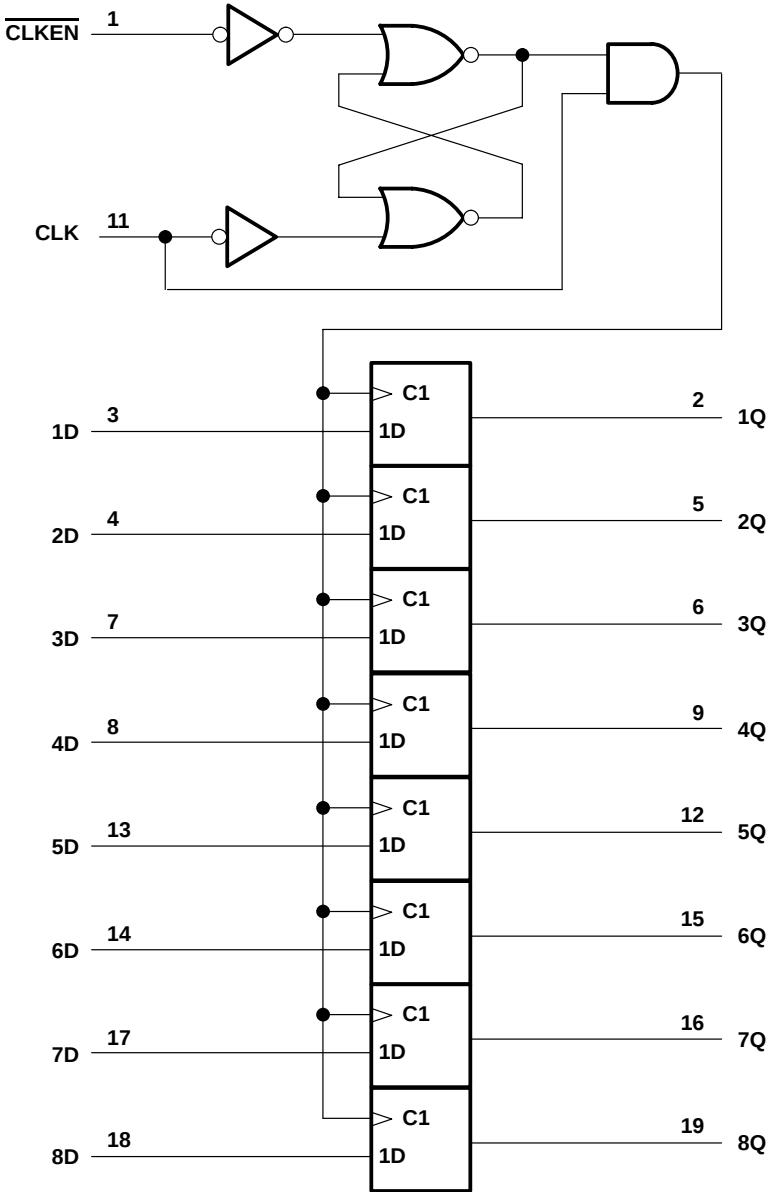
SN54HCT377, SN74HCT377 OCTAL D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

SCLS067D – NOVEMBER 1988 – REVISED MARCH 2003

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT Q
CLKEN	CLK	D	
H	X	X	Q ₀
L	↑	H	H
L	↑	L	L
X	L	X	Q ₀

logic diagram (positive logic)



SN54HCT377, SN74HCT377 OCTAL D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package	58°C/W
N package	69°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54HCT377			SN74HCT377			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	$V_{CC} = 4.5$ V to 5.5 V			0.8			0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times				500			500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT377		SN74HCT377		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20\ \mu\text{A}$	4.5 V	4.4	4.499	4.4		4.4		V
		$I_{OH} = -4\ \text{mA}$	4.5 V	3.98	4.30	3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20\ \mu\text{A}$	4.5 V		0.001	0.1		0.1		V
		$I_{OL} = 4\ \text{mA}$	4.5 V		0.17	0.26		0.4	0.33	
I_I	$V_I = V_{CC}$ or 0		5.5 V	±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$		5.5 V		8		160		80	μA
$\Delta I_{CC}^\ddagger$	One input at 0.5 V or 2.4 V, Other inputs at GND or V_{CC}		5.5 V		1.4	2.4		3	2.9	mA
C_i		4.5 V to 5.5 V			3	10		10*	10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC} .

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SN54HCT377, SN74HCT377 OCTAL D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V _{CC}	T _A = 25°C		SN54HCT377		SN74HCT377		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		4.5 V	25		17		20		MHz
			5.5 V	30		19		22		
t _w	Pulse duration	CLK high or low	4.5 V	20		30		25		ns
			5.5 V	18		28		23		
t _{su}	Setup time before CLK↑	Data	4.5 V	12		18		15		ns
			5.5 V	10		17		14		
		CLKEN high or low	4.5 V	12		18		15		
			5.5 V	10		17		14		
t _h	Hold time data after CLK↑	Data	4.5 V	3		3		3		ns
			5.5 V	3		3		3		
		CLKEN inactive or active	4.5 V	5		5		5		
			5.5 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN54HCT377				UNIT	
				T _A = 25°C			MIN		MAX
				MIN	TYP	MAX			
f _{max}			4.5 V	25	31	17		MHz	
			5.5 V	30	37	19			
t _{pd}	CLK	Any	4.5 V	15		30	45	ns	
			5.5 V	12		28	40		
t _t		Any	4.5 V	8		15	22	ns	
			5.5 V	6		14	21		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN74HCT377				UNIT	
				T _A = 25°C			MIN		MAX
				MIN	TYP	MAX			
f _{max}			4.5 V	25	31	20	MHz		
			5.5 V	30	37	22			
t _{pd}	CLK	Any	4.5 V	15	30	38	ns		
			5.5 V	12	28	35			
t _t		Any	4.5 V	8	15	19	ns		
			5.5 V	6	14	17			

operating characteristics, T_A = 25°C

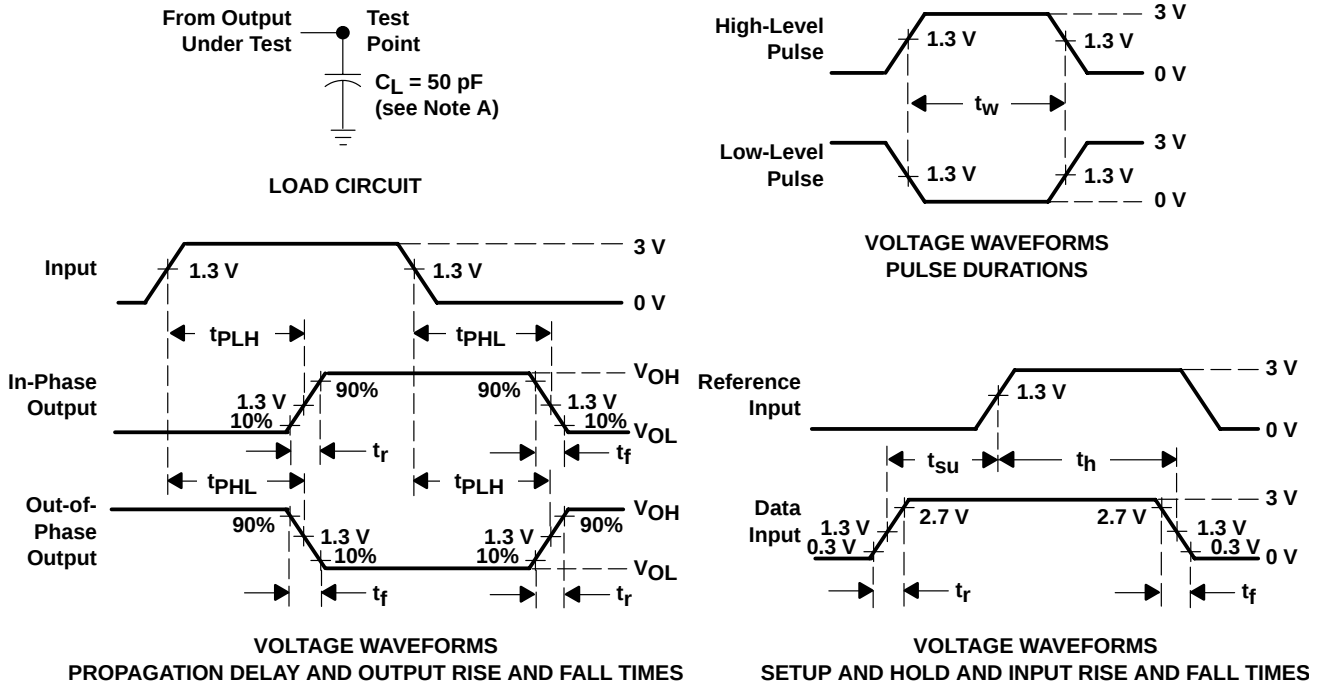
PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load	30	pF

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. The outputs are measured one at a time with one input transition per measurement.
 - D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HCT377DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 85	HCT377
SN74HCT377DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT377
SN74HCT377DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT377
SN74HCT377N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT377N
SN74HCT377N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT377N

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

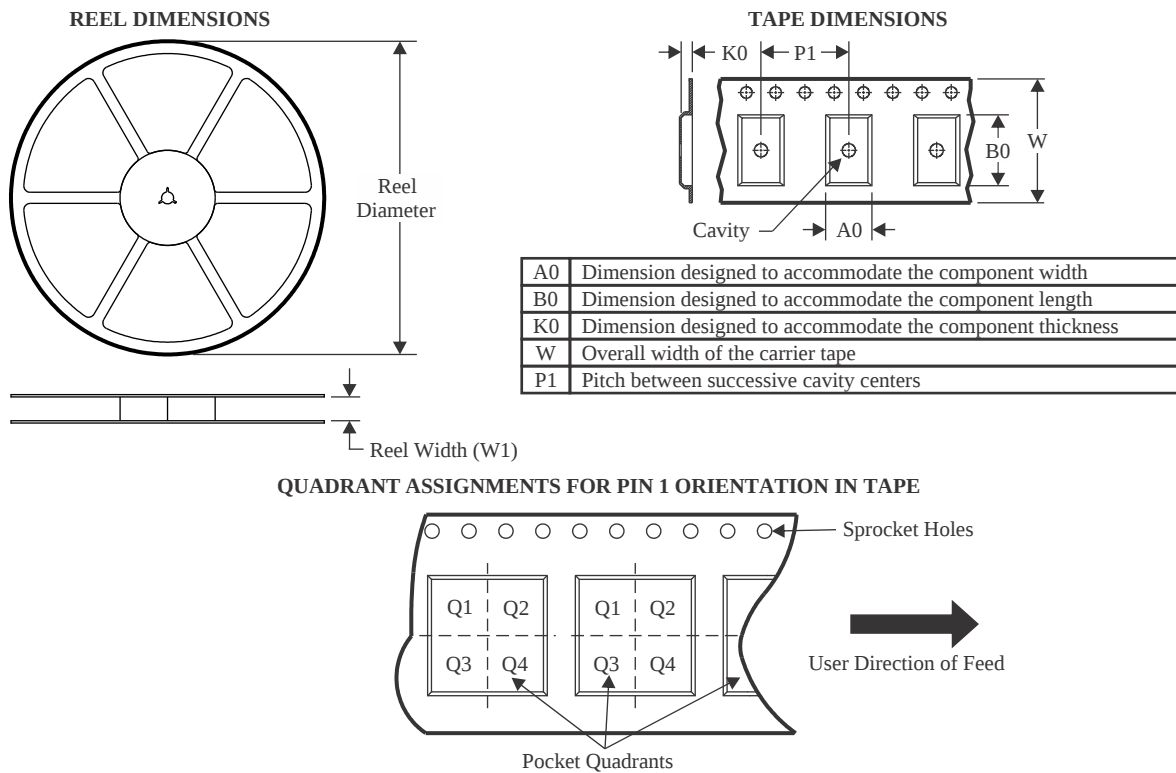
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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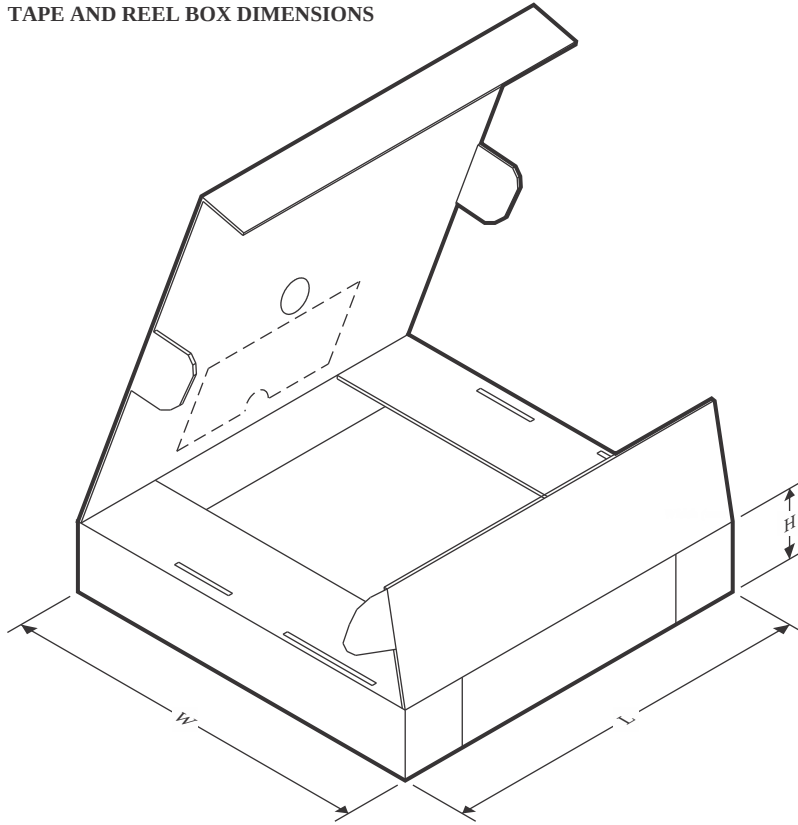
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT377DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

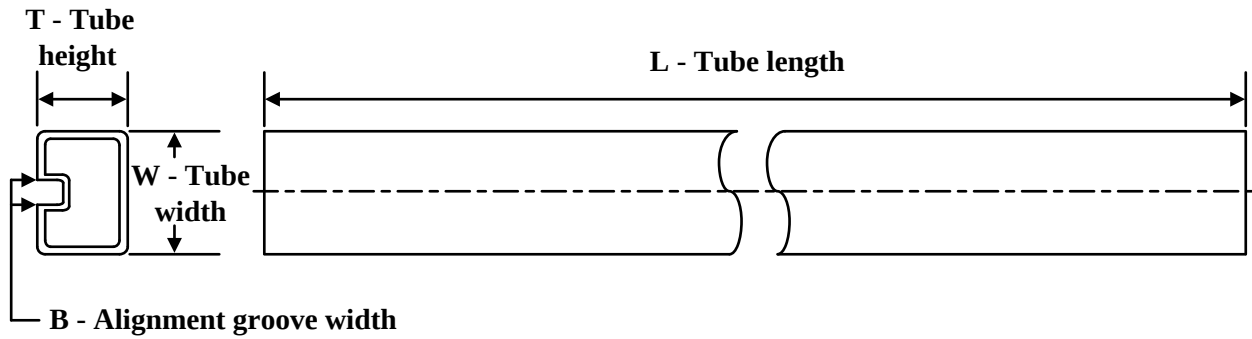
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT377DWR	SOIC	DW	20	2000	356.0	356.0	45.0

TUBE



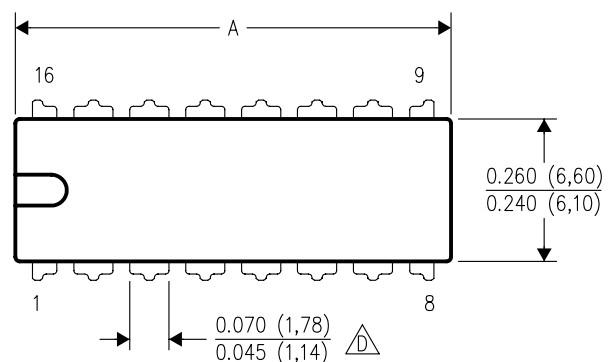
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74HCT377N	N	PDIP	20	20	506	13.97	11230	4.32
SN74HCT377N.A	N	PDIP	20	20	506	13.97	11230	4.32

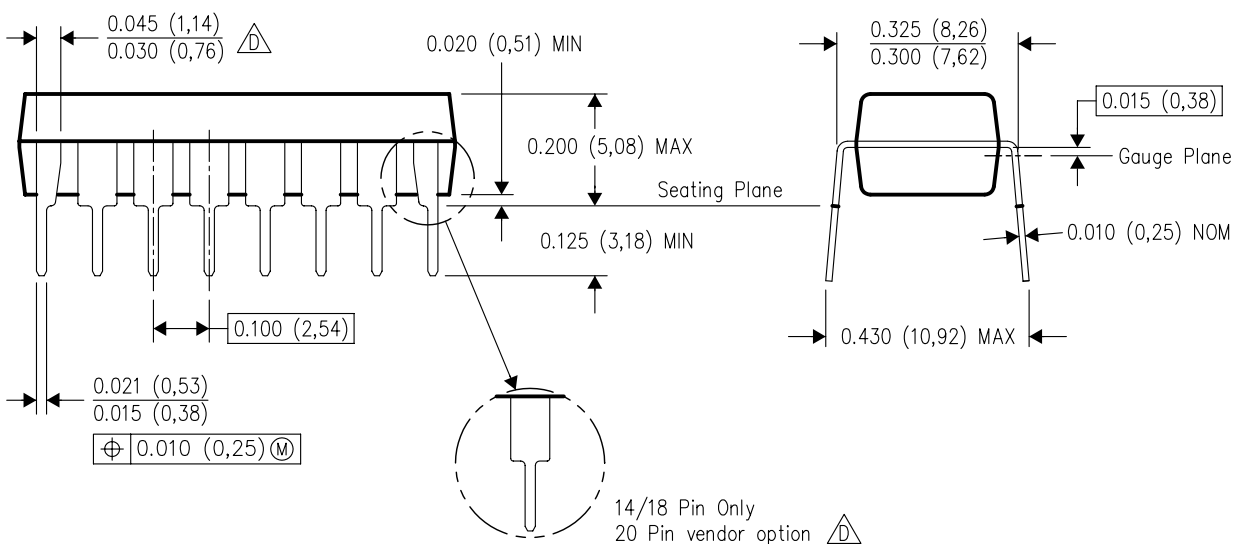
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



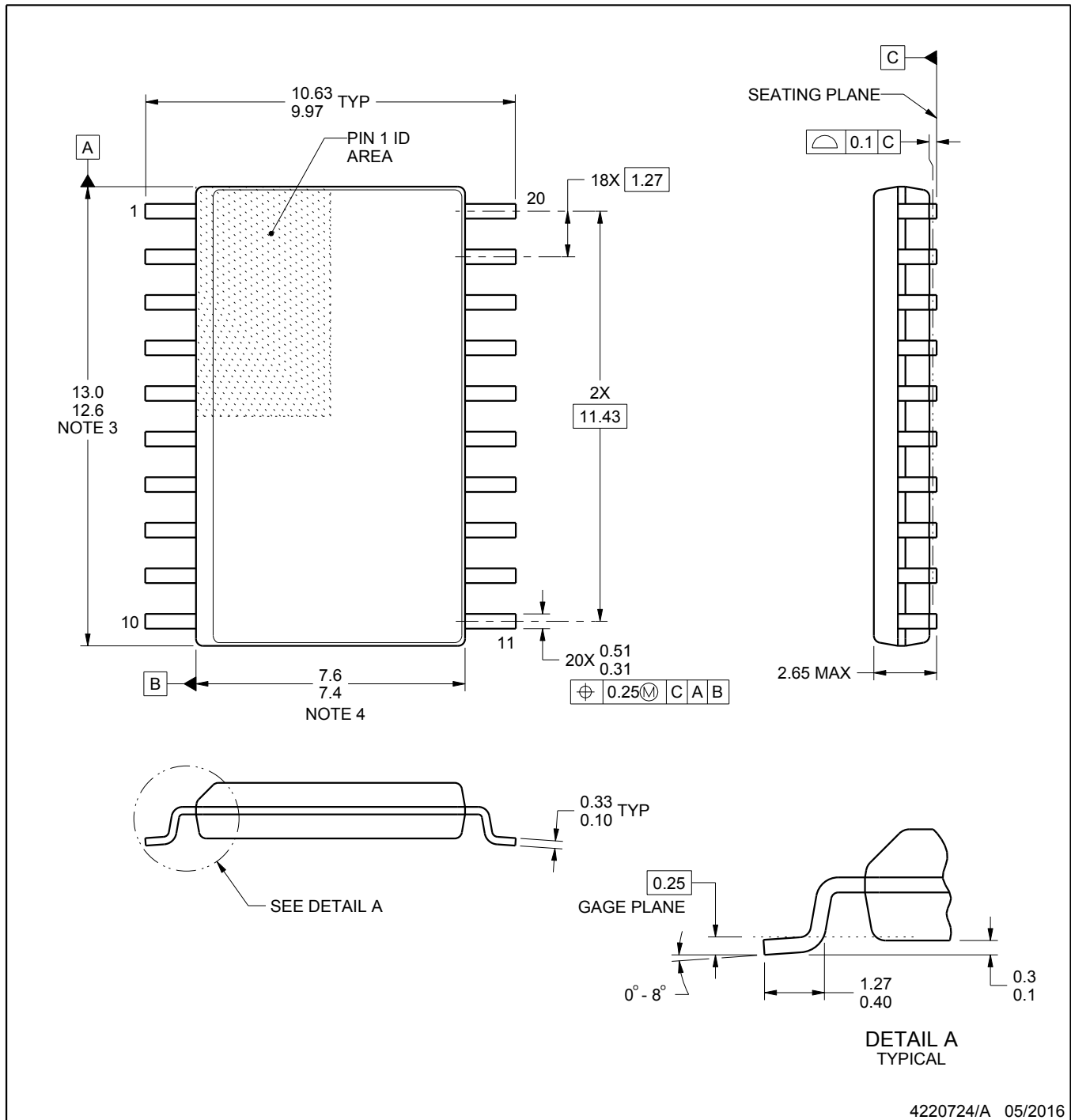
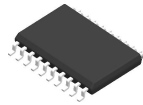
PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220724/A 05/2016

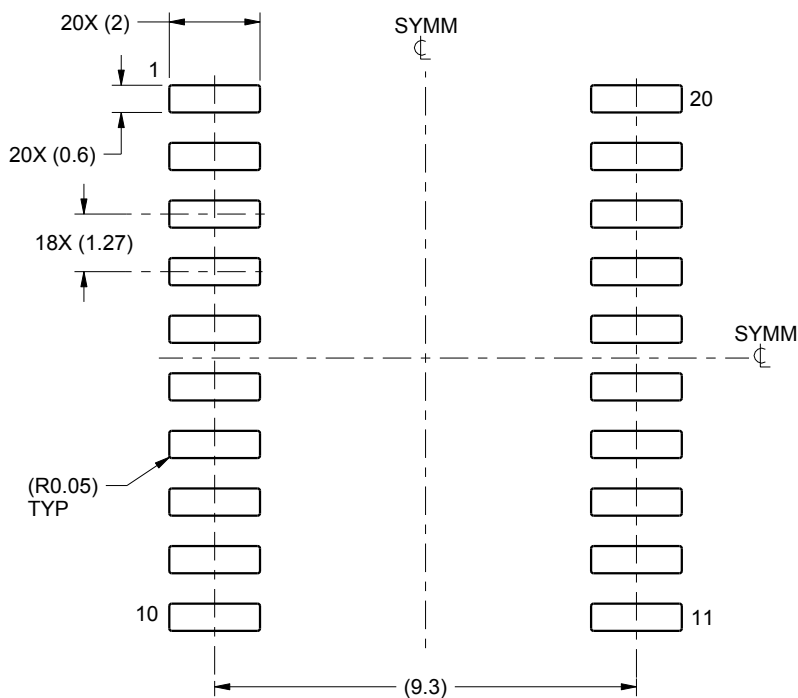
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

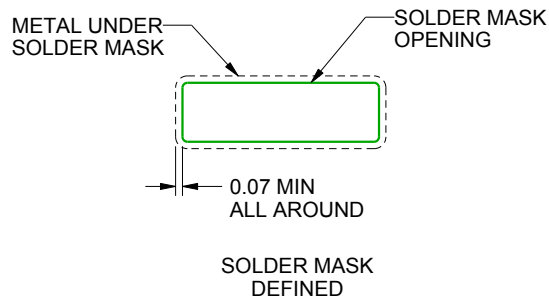
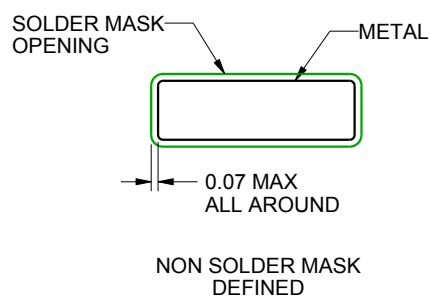
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

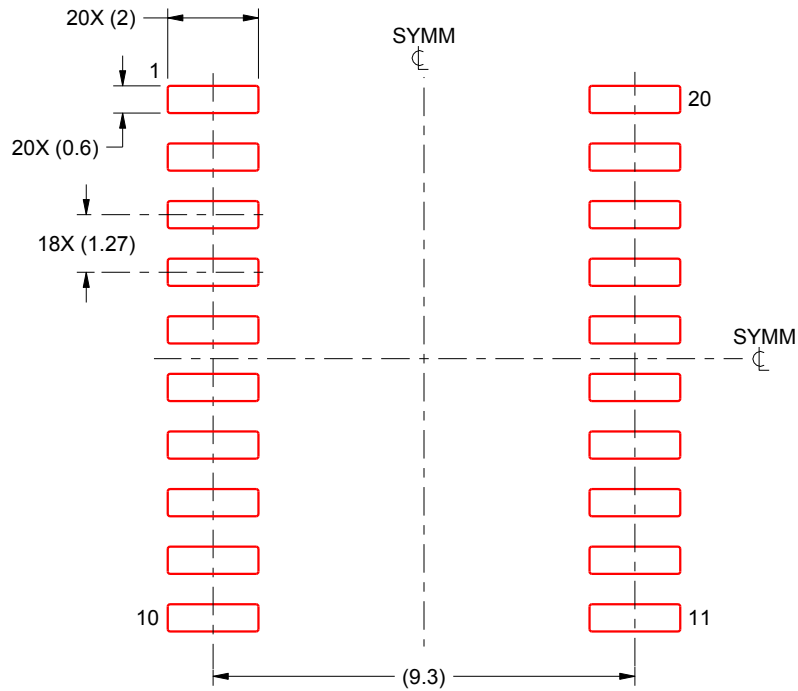
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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