TDEL1G522 Single Filtering Delay Element

1 Features

- 1% typical, 10% maximum delay variation
- Pre-configured digital timing - no external timing components required
- Wide operating range from 1.65V to 5.5V
- I/O clamp diodes protect from over- and under-voltage transients
- Schmitt-trigger architecture on all inputs

2 Applications

- Deglitch a signal
- Delay a signal
- Debounce both edges of a signal

3 Description

The TDEL1G522 devices are fixed-time signal delay elements. The delay amount can be selected by setting pins S0 and S1. Pulses shorter than the selected delay amount are filtered out.

The TDEL1G522 features two interchangable inputs (A, B). When one input (A or B) is used for the input signal, the other input (B or A) selects non-inverted (low) or inverted (high) operation.

The TDEL1G522 features a non-inverted (Y) and inverted ($\overline{Y}$) output.

Package Information

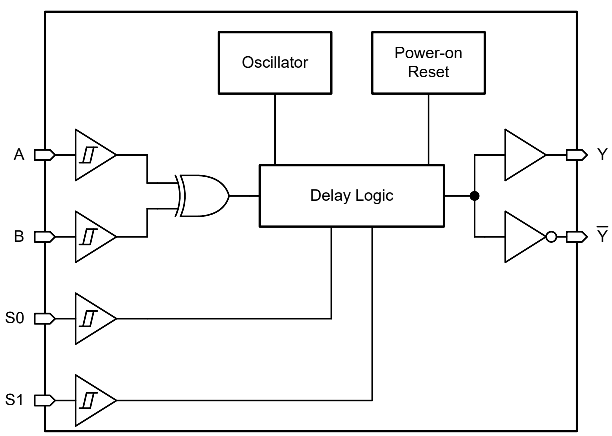
PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
TDEL1G522	DRL (SOT-5X3, 8)	2.1mm × 1.6mm	2.1mm × 1.6mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.

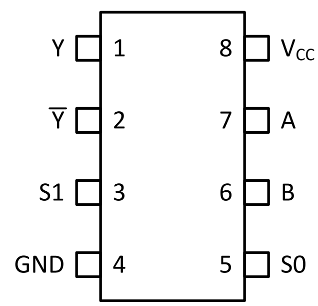
Device Information

PART NUMBER	DELAY TIME(1)			
	T1	T2	T3	T4
TDEL1G522**00**	30µs	100µs	1ms	10ms

(1) Approximate values shown; see *Typical Characteristics* for details



Functional Block Diagram



Pinout Diagram

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4 Pin Configuration and Functions

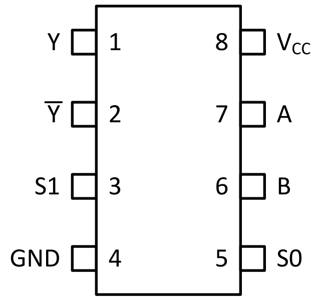


Figure 4-1. TDEL1G522 DRL Package (Top View)

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	DRL NO.		
Y	1	O	Non-inverted output
$\overline{Y}$	2	O	Inverted output
S1	3	I	Configuration input 1
GND	4	G	Ground
S0	5	I	Configuration input 0
B	6	I	Input B
A	7	I	Input A
V_{CC}	8	P	Positive supply

(1) Signal Types: I = Input, O = Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Digital input voltage range[2]		–0.5	V_{CC} + 0.5	V
V_O	Digital output voltage range[2]		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp diode current, continuous	V_I < -0.5V or V_I > V_{CC} + 0.5		±20	mA
	Input clamp diode current, pulsed 1µs	V_I < -0.5V or V_I > V_{CC} + 0.5		±200	mA
I_{OK}	Output clamp diode current, continuous	V_I < -0.5V or V_I > V_{CC} + 0.5		±20	mA
	Output clamp diode current, pulsed 1µs	V_I < -0.5V or V_I > V_{CC} + 0.5		±200	mA
I_O	Digital output current, continuous	V_O = 0 to V_{CC}		±20	mA
	Digital output current, pulsed 1µs	V_O = 0 to V_{CC}		±100	mA
	Continuous current through V_{CC} or GND			±60	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The voltage ratings may be exceeded if the associated clamp current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
V_I	Input Voltage[1]		0	V_{CC}	V
V_O	Output Voltage		0	V_{CC}	V
I_{OH} [2]	High-level output current	V_{CC} = 1.65V to 2.2V		–6	mA
		V_{CC} = 2.3V to 5.5V		–20	mA
I_{OL} [2]	Low-level output current	V_{CC} = 1.65V to 5.5V		20	mA
C_L	Digital output load capacitance	V_{CC} = 1.65V to 5.5V		50	pF
V_{POR}	Power-on reset ramp voltage	$\Delta t/\Delta V_{CC} \geq 20\mu s/V$	0.3	1.5	V
$\Delta t/\Delta V_{CC}$	Power-on ramp rate	V_{CC} = 0.3V to 1.5V	20		µs/V
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.65V to 5.5V		100	ms/V

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.
(2) Recommended maximum output current for continuous operation; see *Electrical Characteristics* for test current values to maintain V_{OH} and V_{OL} specifications. Operating with average output current greater than 12mA may impact device reliability and shorten the device lifetime.

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC[1]						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DRL (SOT-5X3)	8	118.4	77.1	26.5	3.9	25.9	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

Over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive switching threshold		1.65V	0.84	1.02	1.21	V
			1.8V	0.91	1.11	1.31	
			2.5V	1.24	1.48	1.72	
			3.3V	1.59	1.85	2.13	
			5V	2.29	2.65	3.03	
			5.5V	2.5	2.88	3.3	
V_{T-}	Negative switching threshold		1.65V	0.51	0.67	0.85	V
			1.8V	0.58	0.74	0.93	
			2.5V	0.88	1.07	1.29	
			3.3V	1.19	1.42	1.68	
			5V	1.8	2.11	2.47	
			5.5V	1.99	2.32	2.71	
ΔV_T	Hysteresis (V_{T+} - V_{T-})		1.65V	0.23	0.36	0.49	V
			1.8V	0.24	0.37	0.5	
			2.5V	0.29	0.40	0.54	
			3.3V	0.34	0.44	0.55	
			5V	0.43	0.53	0.63	
			5.5V	0.44	0.57	0.66	
V_{OH}	High-level output voltage	I_{OH} = -50µA	1.65V - 5.5V	V_{CC} – 0.1	V_{CC} – 0.01		V
		I_{OH} = -1mA	1.65V	1.5	1.6		
		I_{OH} = -2mA	2.3V	2.1	2.2		
		I_{OH} = -8mA	3V	2.3	2.6		
		I_{OH} = -12mA	4.5V	3.6	4		
		I_{OH} = -12mA	5.5V	4.7	5		

5.5 Electrical Characteristics (continued)

Over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	I_{OL} = 50μA	1.65V - 5.5V		0.01	0.1	V
		I_{OL} = 1mA	1.65V		0.01	0.1	
		I_{OL} = 2mA	2.3V		0.02	0.1	
		I_{OL} = 8mA	3V		0.05	0.3	
		I_{OL} = 12mA	4.5V		0.06	0.3	
		I_{OL} = 12mA	5.5V		0.06	0.3	
I_I	Input leakage current	V_I = 5.5V or GND	5.5V			±200	nA
I_{CC}	Supply current	Standby state, V_I = V_{CC} or GND, I_O = 0	5.5V		1	5	μA
I_{CC}	Supply current	Active state using high speed oscillator(1), V_I = V_{CC} or GND, I_O = 0	1.65V		57	59	μA
			2.3V		61	62	
			3V		65	66	
			4.5V		79	97	
			5.5V		93	123	
ΔI_{CC}	Supply-current change	One input, 0 < V_i < V_{CC}, all other inputs at V_{CC} or GND, I_O = 0	1.65V - 5.5V			1.6	mA
C_I		V_I = 5.5V or GND	5.5V		3		pF

(1) See *Typical Characteristics* for a table of which devices use each oscillator.

5.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	MIN	MAX	UNIT
t_{wi} (1)	Pulse width	Any input	1.8V ± 0.15V	10		ns
			2.5V ± 0.2V	10		
			3.3V ± 0.3V	10		
			5V ± 0.5V	10		
$t_{startup}$ (2)	Startup time		1.65V - 5.5V		265	μs

(1) Minimum input pulse width to activate the timing circuitry inside the TDEL family device. Active state operation increases power consumption but may not change the output state. See *Detailed Description* section for operation details.
(2) Outputs are in the high-impedance state until startup time expires.

5.7 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_t		Any output	C_L = 15pF	1.65V		12	18	ns
				2.3V		9	14	
				3V		8	11	
				4.5V		6	9	
				5.5V		6	9	
			C_L = 50pF	1.65V		22	33	
				2.3V		16	24	
				3V		14	20	
				4.5V		11	16	
				5.5V		10	15	
Δt_{delay} (1)		Any output	C_L = 50pF	1.65V to 5.5V		±1	±10	%
C_{pd}	Any Input1	Any Output	T = V_{CC}, $\overline{T}$ = GND, f_I = 1MHz, C_L = 50pF	1.65V		30		pF
				2.3V		21		pF
				3V		14		pF
				4.5V		9		pF
				5.5V		8		pF

(1) Variation in delay time from nominal.

5.8 Typical Characteristics

Table 5-1. Delay time for each device and configuration

T_A = 25°C (unless otherwise noted)

Device	Oscillator	Parameter	Timing Value(1)			
			T1 S1 = L, S0 = L	T2 S1 = L, S0 = H	T3 S1 = H, S0 = L	T4 S1 = H, S0 = H
TDEL1G52200DRLR	High speed	t_{delay}	30μs	100μs	1ms	10ms
		t_{osc}	1μs	1μs	12μs	64μs

(1) The delay time (t_{delay}) can additionally vary by up to –t_{osc}.

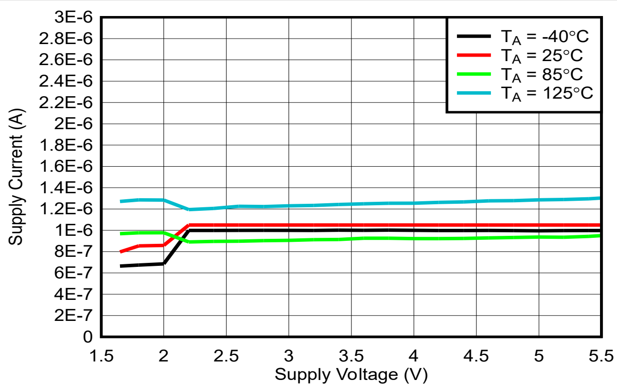


Figure 5-1. Supply Current vs Supply Voltage

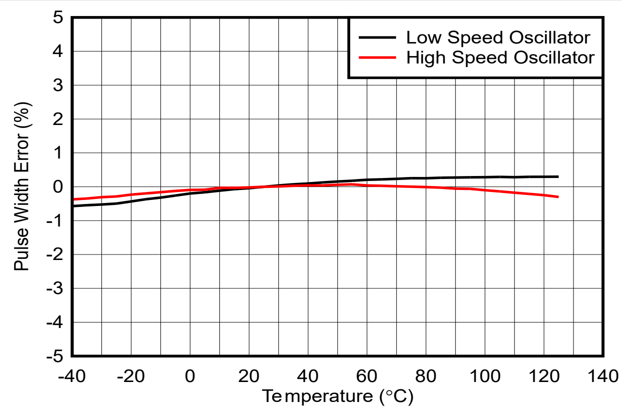


Figure 5-2. Pulse Width Error vs Temperature

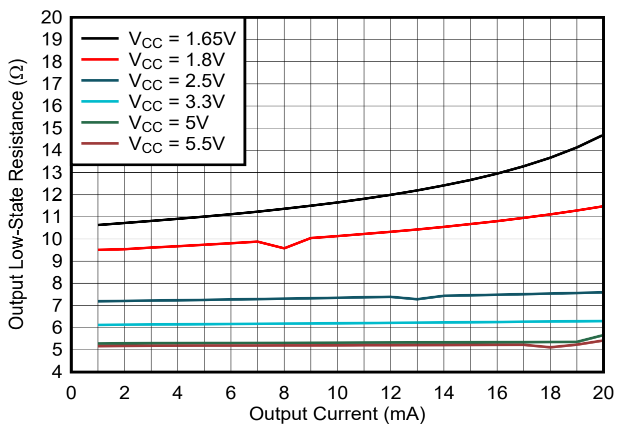


Figure 5-3. Output Low-State Resistance vs Output Current

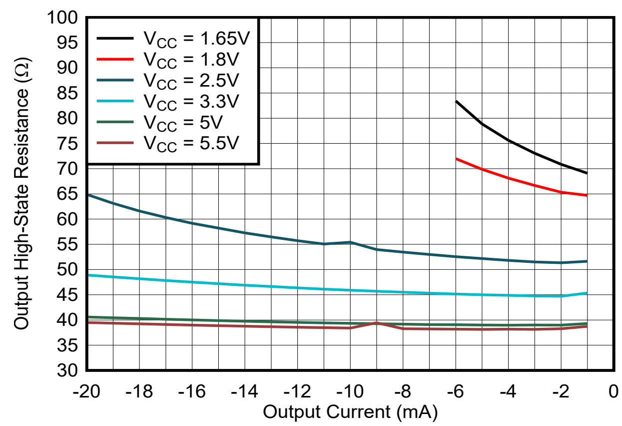


Figure 5-4. Output High-State Resistance vs Output Current

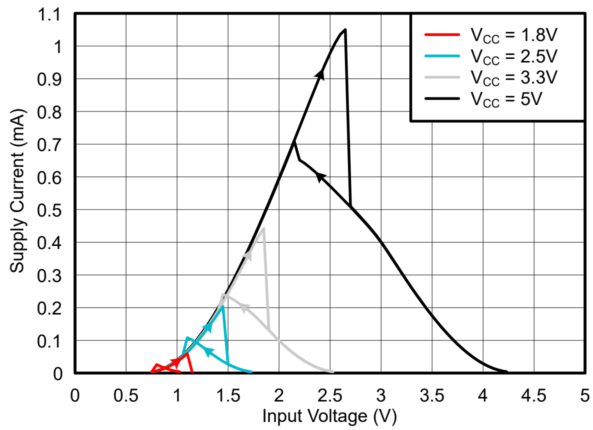
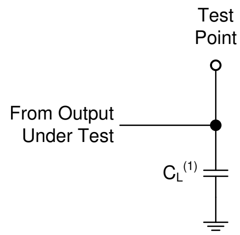


Figure 5-5. Input Voltage vs Supply Current

6 Parameter Measurement Information

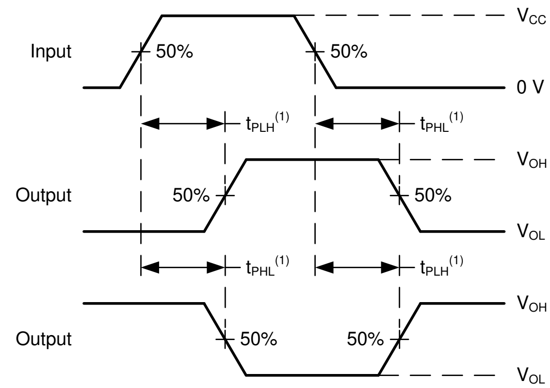
Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5ns.

The outputs are measured individually with one input transition per measurement.



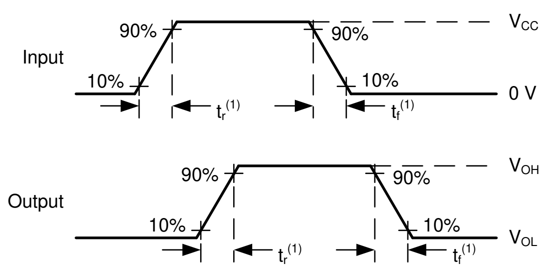
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-3. Voltage Waveforms, Input and Output Transition Times

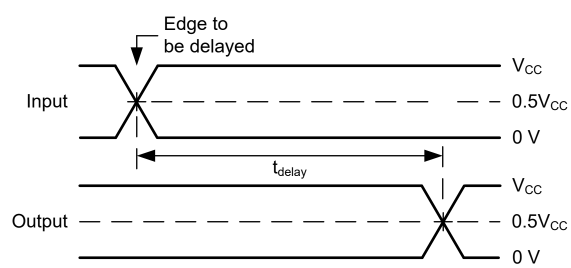


Figure 6-4. Voltage Waveforms, Edge Delay Time

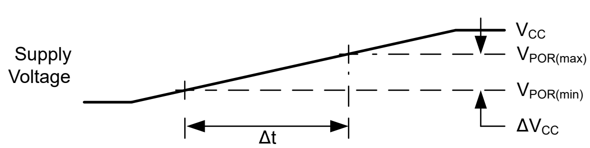


Figure 6-5. Voltage Waveforms, Supply Ramp

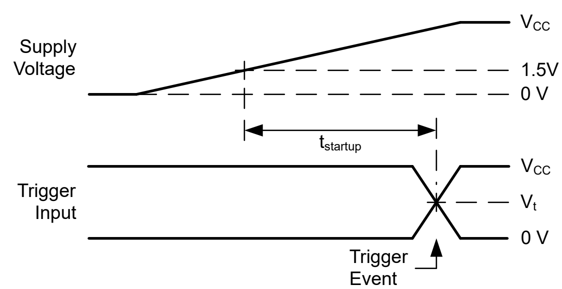


Figure 6-6. Voltage Waveforms, Startup Time

7 Detailed Description

7.1 Overview

The TDEL1G522 device is a fixed-time signal delay element with selectable delay values and maximum flexibility for input/output signal polarity. Each orderable device offers four configurable delay times. The delay amount can be selected by setting pins S0 and S1.

When the input transitions, the internal timer starts. When the timer reaches the selected delay value, the output transitions accordingly and the timer is disabled. If the input transitions back before the delay time expires, the timer is reset and disabled, awaiting the next delay operation.

The delay feature provides inherent filtering behavior, preventing pulses shorter than the selected delay amount from propagating to the output. The output state is maintained when input pulses do not remain in the triggered state longer than the programmed delay time.

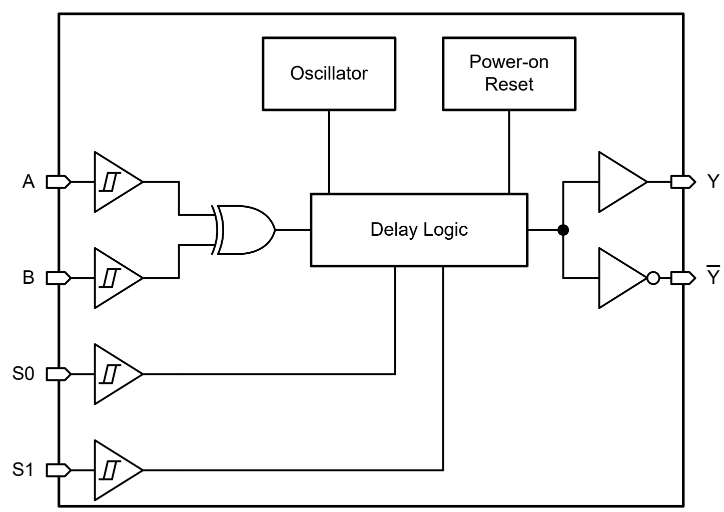
The TDEL1G522 features two interchangeable inputs (A, B). When one input (A or B) is used for the input signal, the other input (B or A) selects the operating mode: non-inverted operation (when held low) or inverted operation (when held high). The behavior can be described by the Boolean equation $X = A \oplus B$, where X is the input signal to the edge delay element.

The device provides both non-inverted (Y) and inverted ($\overline{Y}$) outputs, allowing simultaneous access to both polarities of the delayed signal.

The internal oscillator turns off when not in use. When a delay is being measured, the oscillator is turned on to provide precise timing control.

During the power-up ramp, the outputs remain in a high-impedance state until the internal power-on reset circuit enables normal device operation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Naming Convention

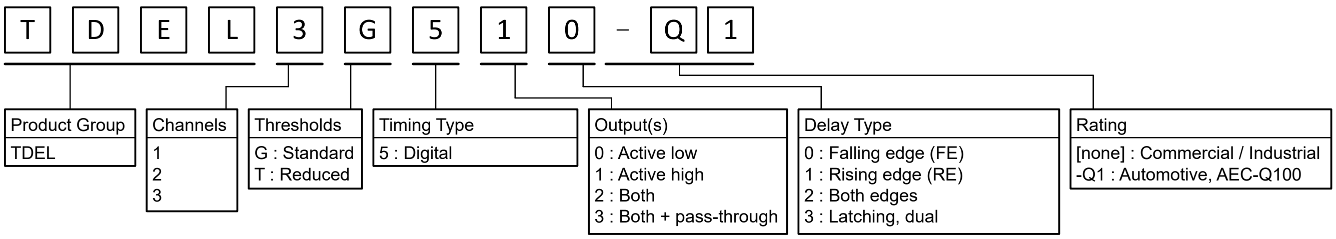


Figure 7-1. Device name meaning

7.3.2 Timing Mechanism and Accuracy

The output delay (t_{delay}) is generated by a factory-trimmed internal oscillator and binary counter. When an edge transition is detected, the oscillator activates and drives the counter until the pre-configured count is reached, at which point the output responds according to the delay type.

The maximum delay error is provided as Δt_{delay} in the *Switching Characteristics* section and includes variations due to voltage, design, manufacturing, and temperature. This variation is given as a percentage of the typical delay provided in the *Typical Characteristics* section.

7.3.3 CMOS Push-Pull Outputs

This device includes CMOS push-pull outputs. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.4 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device with the maximum value per input defined as ΔI_{CC} in the *Electrical Characteristics* table. For additional information regarding Schmitt-trigger inputs, please see *Understanding Schmitt Triggers*.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at a valid high or low voltage level. If a system is not actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10kΩ resistor is recommended and will typically meet all requirements.

7.3.5 Latching Logic with Known Power-Up State

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory. In typical logic devices, the output state of each latching circuit is unknown after power is initially applied; however, this device includes an added Power On Reset (POR) circuit which sets the states of all included latching circuits during the power-up ramp prior to the device starting normal functionality.

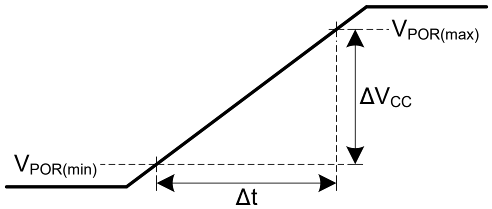


Figure 7-2. Supply (V_{CC}) Ramp Characteristics for Known Power-Up State

Figure 7-2 shows a correct supply voltage turn-on ramp and defines values used in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

Prior to starting the power-on ramp, the supply must be completely off ($V_{CC} \leq V_{POR(min)}$).

The supply voltage must ramp at a rate within the range provided in the *Recommended Operating Conditions* table.

The output state of each latching logic circuit only remains stable as long as power is applied to the device ($V_{CC} \geq V_{POR(max)}$).

Variation from these recommendations will result in the device having an unknown power-up state.

7.3.6 Clamp Diode Structure

As shown in Figure 7-3, the inputs and outputs to this device have both positive and negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.

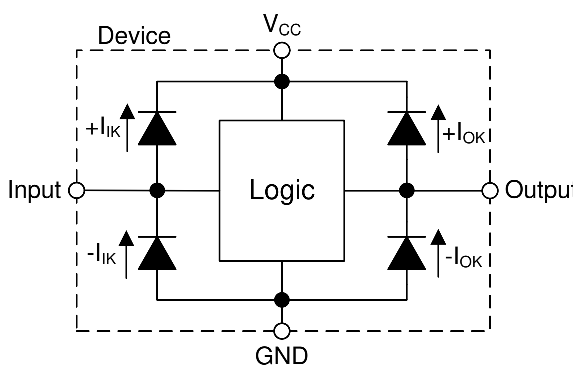


Figure 7-3. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

7.4.1 Startup Operation

The TDEL1G522 includes an internal power-on reset (POR) circuit that prevents erroneous triggers from occurring during startup. There are details on the supply ramp requirements provided in *Latching Logic with Known Power-Up State*. Normal operation can be started after the startup time ($t_{startup}$) has expired per the *Timing Requirements* table. While active, the POR circuit holds all outputs of the TDEL1G522 in the high-impedance state.

7.4.2 On-State Operation

The tables below list the on-state functional modes for the TDEL1G522.

Table 7-1. Timing Configuration Table

INPUTS		CONFIGURED TIMING(1)
S1	S0	
L	L	T1
L	H	T2
H	L	T3
H	H	T4

(1) See the *Typical Characteristics* section for device specific timings.

Table 7-2. Function Table

INPUTS(1)		OUTPUTS(2) (3)	
A	B	Y	$\overline{Y}$
L	L	L	H
L	H	H	L
H	L	H	L
H	H	L	H

(1) H = high voltage level, L = low voltage level
(2) L = driving low, H = driving high
(3) The outputs change to the shown state after the input is held in the described condition for the pre-configured delay time.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TDEL1G522 is used to add a fixed-time falling-edge and rising-edge delay to a digital input signal. The three most common use cases are: signal delay, deglitch, debounce. All three applications are the same logic function with the only difference being the input signal.

8.2 Typical Application

In this application, the TDEL1G522 is used to delay both edges on an input signal. The circuit configuration is shown in Figure 8-1.

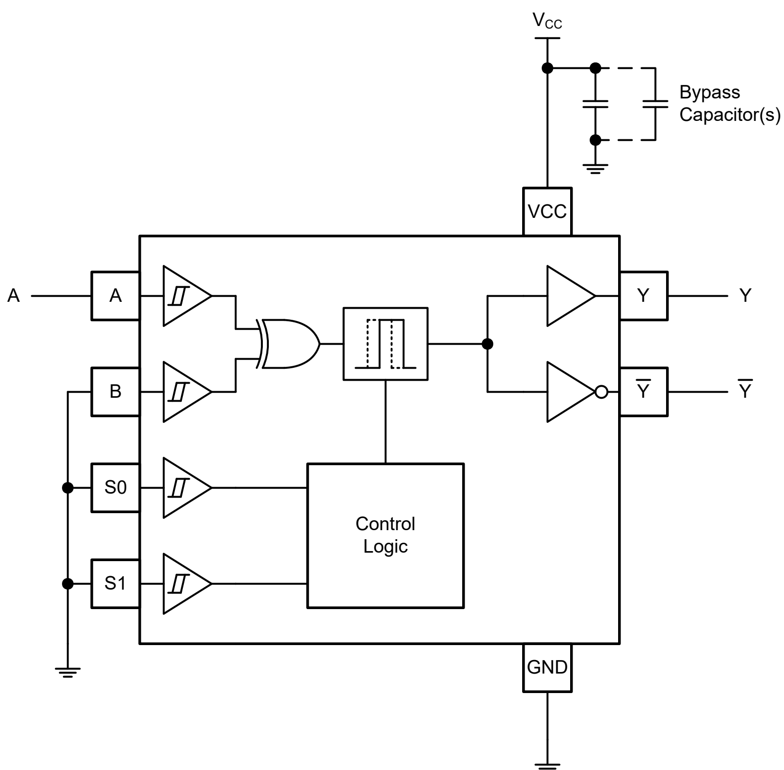


Figure 8-1. Delay Schematic Using the TDEL1G522

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Verify that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the TDEL1G522 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Verify that the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the TDEL1G522 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into the ground connection. Verify that the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The TDEL1G522 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied; however, do not exceed 50pF.

The TDEL1G522 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the TDEL1G522 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The TDEL1G522 supports very slow input signal transition rates because it has Schmitt-Trigger inputs. See *Recommended Operating Conditions*.

Another benefit to having Schmitt-Trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics* table. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-Trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics* section.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. Low load capacitance can be accomplished by providing short, appropriately sized traces from the TDEL1G522 to the receiving device.
3. Verify that the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Never violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; however, the power consumption and thermal increase can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation* application note.

8.2.3 Application Curves

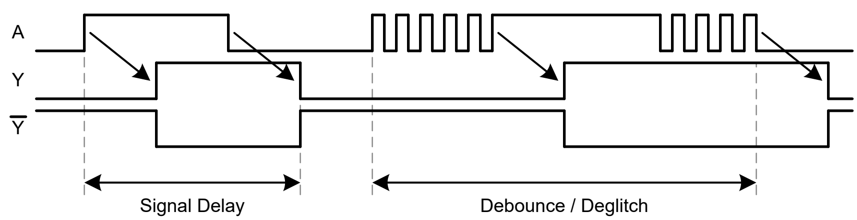


Figure 8-2. Output Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

During startup, the power supply should ramp within the provided power-up ramp rate range in the *Recommended Operating Conditions* table.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For normal operation of the TDEL1G522, a 0.1µF bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness

- For traces longer than 12cm
  - Use impedance controlled traces
  - Source-terminate using a series damping resistor near the output
  - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

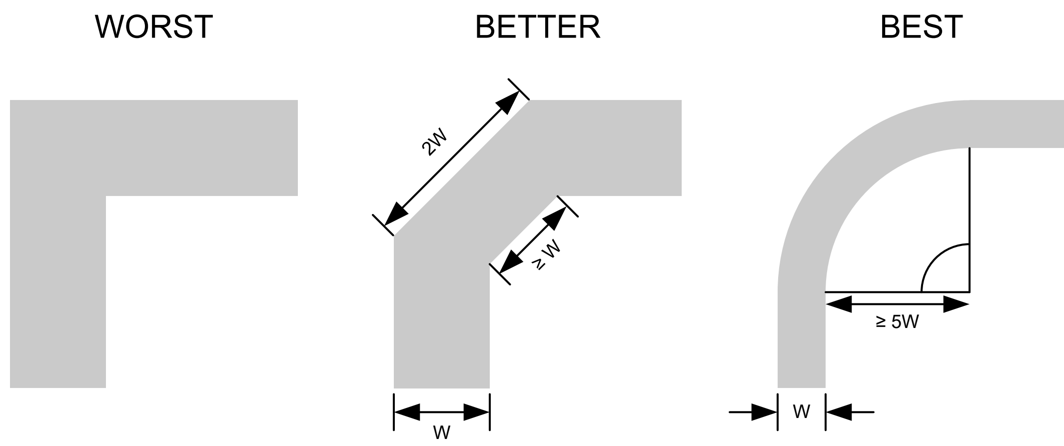


Figure 8-3. Example Trace Corners for Improved Signal Integrity

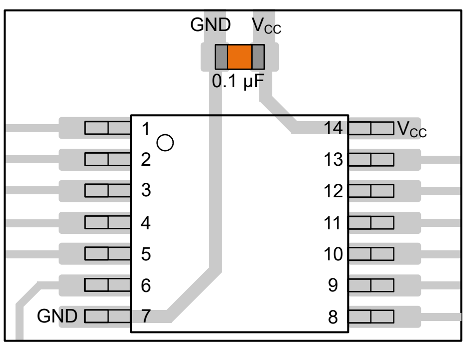


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

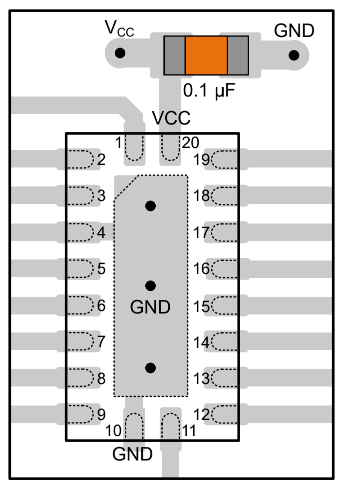


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

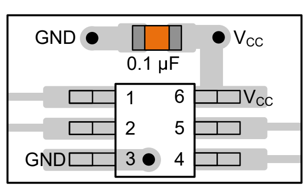


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

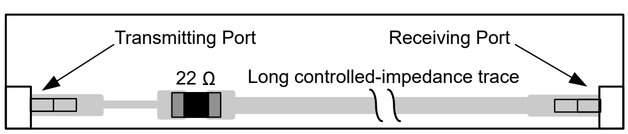


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Support

9.1.1 Device Nomenclature

Table 9-1. Device Nomenclature

PRODUCT[(1)]	DESCRIPTION
TDEL1G522 **xx yyy z**	**xx** is the timing variant. See page 1 for a table of timing options. **yyy** is the package designator. **z** indicates the package quantity. R is for large reel (3000 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TDEL1G52200DRLR	Active	Production	SOT-5X3 (DRL) | 8	3000 | LARGE T&R	-	Call TI	Level-1-260C-UNLIM	-	TDB00

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TDEL1G522 :

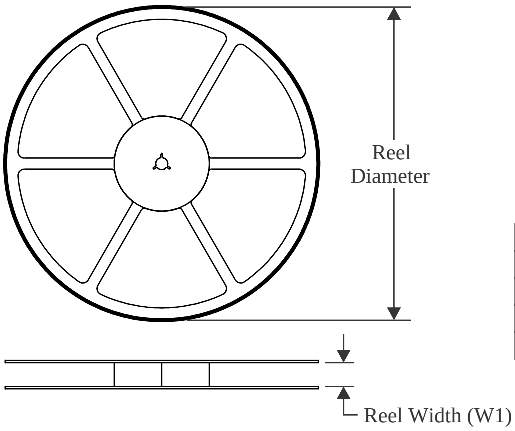
- Automotive : TDEL1G522-Q1

NOTE: Qualified Version Definitions:

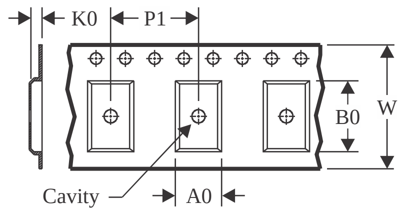
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

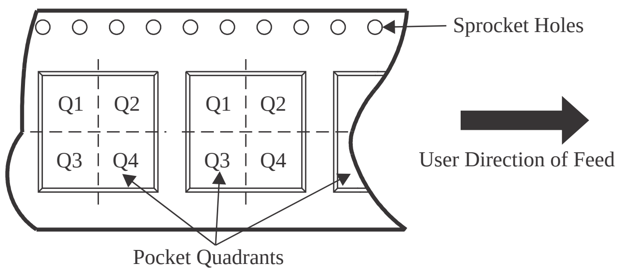


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

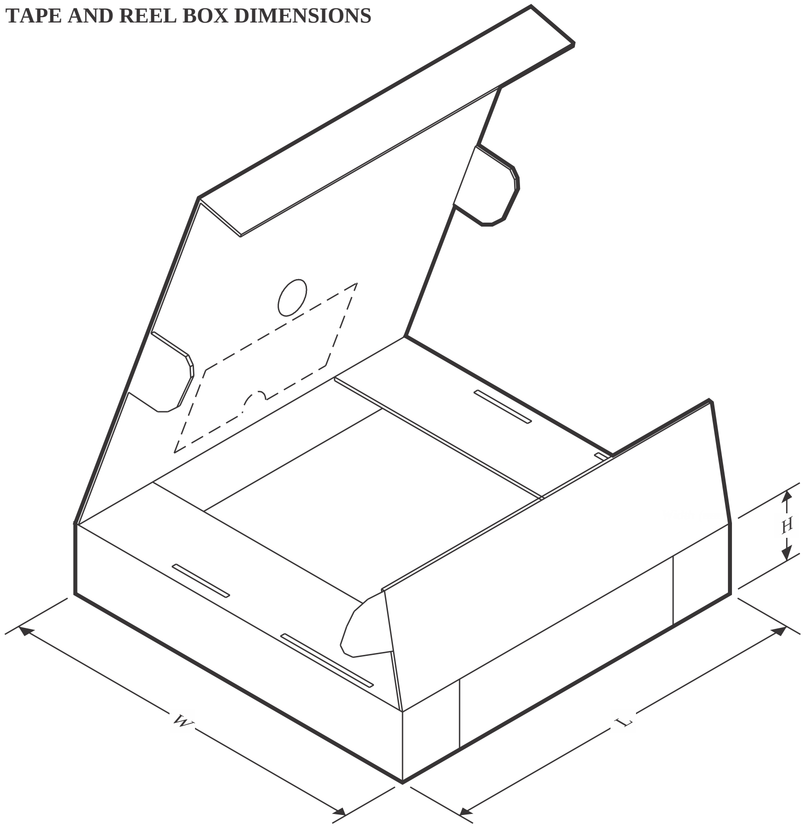
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

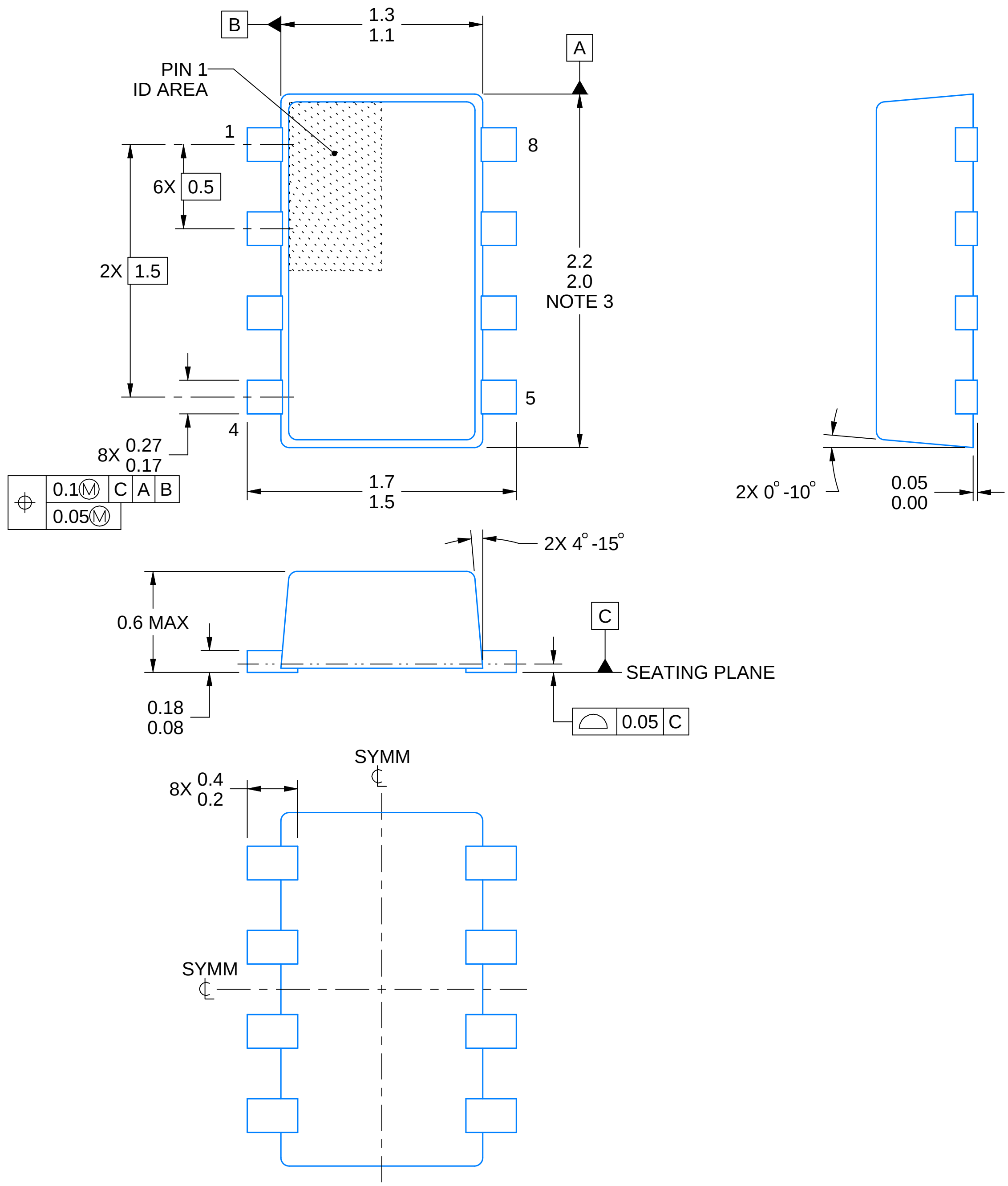
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TDEL1G52200DRLR	SOT-5X3	DRL	8	3000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TDEL1G52200DRLR	SOT-5X3	DRL	8	3000	210.0	185.0	35.0



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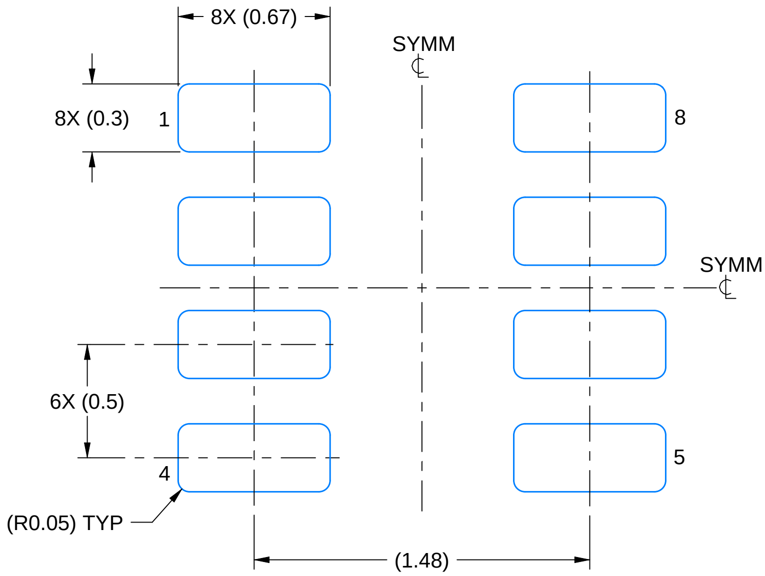
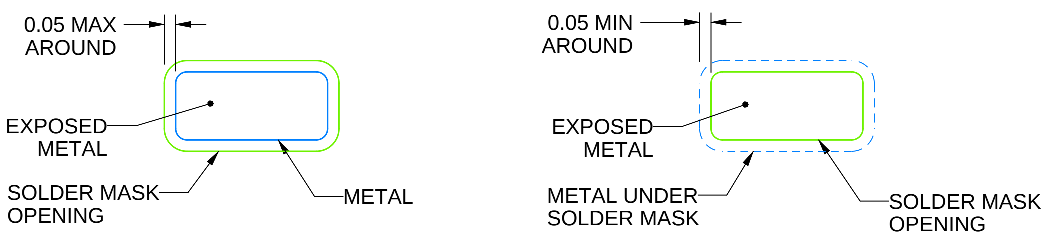
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDERMASK DETAILS

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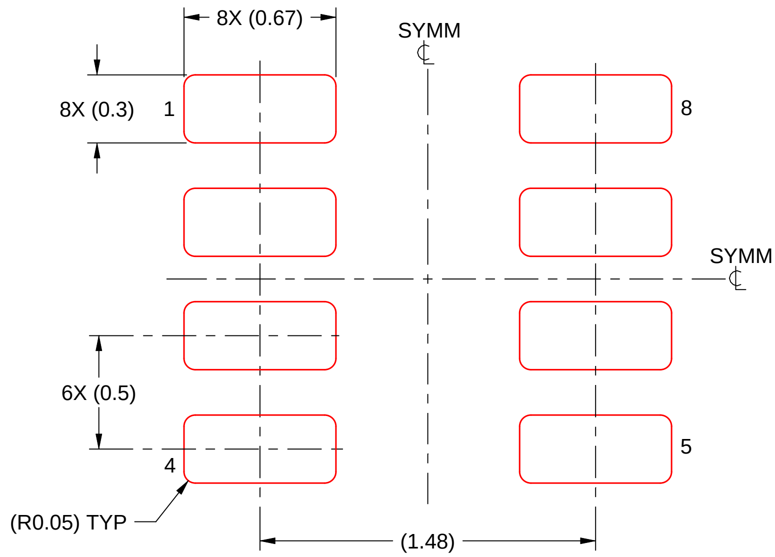
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.