THVD4431A Multiprotocol (RS-232, RS-422, RS-485) Transceiver With 120Ω Switchable Termination, Pin-Selectable Diagnostic Loopback, and IEC-ESD

1 Features

- Meets or exceeds the requirements of the TIA/EIA-485A and TIA/EIA-232F standards
- 3 transmitters, 5 receivers for RS-232
- 1 transmitter, 1 receiver for RS-485
- On-chip switchable 120Ω termination resistor for RS-485 mode
- Integrated charge-pump for RS-232 signaling
- 3V to 5.5V supply voltage
- 1.65V to 5.5V supply for logic data and control signals
- RS-485 differential output exceeds 2.1V for PROFIBUS compatibility with 5V supply
- Large output swing (typical ± 9V) for RS-232 mode
- SLR Pin Selectable Data Rates:
  - RS-232 3T5R mode: 250kbps and 1Mbps
  - RS-485 half-duplex and full-duplex mode: 500kbps and 20Mbps
- Bus I/O protection
  - ±16kV HBM ESD
  - ±8kV IEC 61000-4-2 contact and ±15kV air-gap discharge
  - ±4kV IEC 61000-4-4 fast transient burst
- Diagnostic loopback for both RS-232 and RS-485 modes
- Pin-selectable diagnostic loopback
- Shutdown pin for low current consumption (10µA typical) in disabled state
- Glitch-free power-up/down for hot plug-in capability
- 1/8 unit load (up to 256 bus nodes) for RS-485
- Open, short, and idle bus failsafe for RS-485 receiver
- Bus short-circuit protection, thermal shutdown
- Extended ambient temperature range: -40°C to 125°C
- Space-saving thermally efficient 6mm × 6mm VQFN-40 package
- Pin compatible with industry standard

2 Applications

- Industrial PC
- Factory automation and control
- HVAC systems
- Building automation
- Point-of-sale terminals
- Grid infrastructure
- Industrial Transport

3 Description

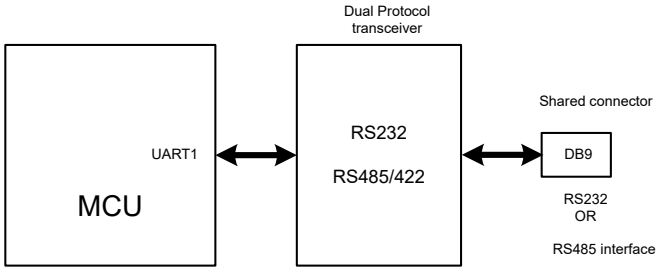
THVD4431A is a highly integrated and robust Multiprotocol transceiver supporting RS-232, RS-422 and RS-485 physical layers. The device has three transmitters and five receivers to enable 3T5R RS-232 port. The device also integrates one transmitter and one receiver to enable half and full duplex RS-485 port. MODE selection pins enable shared bus and logic pins for the protocols to share a common single connector. Integrated termination for RS-485 bus pins and for RS-232 receiver inputs need no external components to realize a fully-functional communication port. The device has a slew rate select feature that enables the device for use at two maximum speeds based on the SLR pin setting.

The device features integrated Level 4 IEC ESD protection, eliminating the need for external system-level protection components. Diagnostic loopback mode for both RS-232 and RS-485 is provided to check for logic to bus and bus to logic path functional integrity and check for cable and connector shorts. In addition, the RS-485 receiver fail-safe feature drives logic high on received logic output when the bus inputs are open or shorted together or when the bus is idle. Shutdown mode consumes ultra-low current (10µA typical), which is good for power-sensitive applications. The device needs 3 to 5.5V supply that powers the charge pump for RS-232 and the drivers or receivers for both RS-232 and RS-485. A separate logic supply V_{IO} (1.65V to 5.5V) enables interface with low level microcontrollers.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
THVD4431A	RHA (VQFN, 40)	6mm × 6mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Pin Configuration and Functions

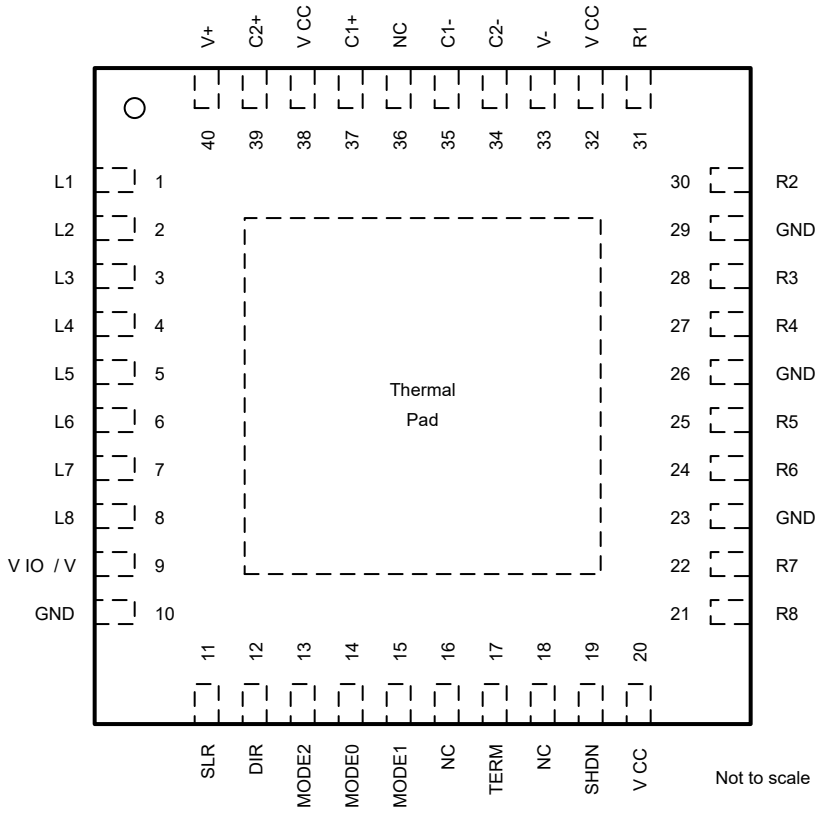


Figure 4-1. 40-Pin VQFN Package (RHA)
(Top View)

Table 4-1. Pin Functions

NAME	NO.	TYPE	DESCRIPTION
L1	1	O	Logic output (RS-232). Integrated weak pull-up resistor. An external pull-up resistor is recommended if leakage or other external current sink is expected on this node. See External Pull-up Resistors for more details.
L2	2	O	Logic output (RS-232/RS-485). Integrated weak pull-up resistor. An external pull-up resistor is recommended if leakage or other external current sink is expected on this node. See External Pull-up Resistors for more details.
L3	3	I	Logic input (RS-232/RS-485). Integrated weak pull-up resistor. An external pull-up resistor is recommended if leakage or other external current sink is expected on this node. See External Pull-up Resistors for more details.
L4	4	I	Logic input. Integrated weak pull-up resistor. An external pull-up resistor is recommended if leakage or other external current sink is expected on this node. See External Pull-up Resistors for more details.
L5	5	O	Logic output. Integrated weak pull-up resistor. An external pull-up resistor is recommended if leakage or other external current sink is expected on this node. SeeExternal Pull-up Resistors for more details.
L6	6	I	Logic input, Integrated weak pull-up resistor. An external pull-up resistor is recommended if leakage or other external current sink is expected on this node. SeeExternal Pull-up Resistors for more details.
L7	7	O	Logic output. Integrated weak pull-up resistor. An external pull-up resistor is recommended if leakage or other external current sink is expected on this node. See External Pull-up Resistors for more details.
L8	8	O	Logic output. Integrated weak pull-up resistor. An external pull-up resistor is recommended if leakage or other external current sink is expected on this node. See External Pull-up Resistors for more details.

Table 4-1. Pin Functions (continued)

NAME	NO.	TYPE	DESCRIPTION
V_{IO} / V_{CC}	9	P	1.65V to 5.5V logic supply voltage. Can also be shorted to V_{CC} if lower logic IO is not needed.
GND	10	G	GND
SLR	11	I	Slew rate control, internal pull-down resistor. SLR=H enables slow speed
DIR	12	I	RS-485 TX/RX enable/disable. Internal pull-down resistor.
MODE2	13	I	MODE control pins, Integrated weak pull-down resistor
MODE0	14	I	
MODE1	15	I	
NC	16	NC	Not connected internally. Can be connected to supply or left open on PCB.
TERM	17	I	Enable/disable 120Ω termination across R1/R2 in RS485-HD mode and across R3/R4 in RS485-FD mode. Internal Pull down resistor
NC	18	NC	Not connected internally. Can be left open or Grounded on PCB.
$\overline{SHDN}$	19	I	Device enable/disable. Internal pull-down resistor
V_{CC}	20	P	3 to 5.5V supply voltage
R8	21	I	RS-232 receiver input
R7	22	I	RS-232 receiver input
GND	23	G	Ground
R6	24	O	RS-232 driver output
R5	25	I	RS-232 receiver input
GND	26	G	Ground
R4	27	I/O	RS-232 driver output or RS-485 inverting receiver input (B)
R3	28	I/O	RS-232 driver output or RS-485 non-inverting receiver input (A)
GND	29	G	Ground
R2	30	I/O	RS-232 receiver input or RS-485 bus pin (Y or A)
R1	31	I/O	RS-232 receiver input or RS-485 bus pin (Z or B)
V_{CC}	32	P	3V to 5.5V supply voltage
V-	33		Negative charge pump rail
C2-	34		Negative terminal of charge pump capacitor
C1-	35		Negative terminal of charge pump capacitor
NC	36	NC	Not connected internally. Can be left open or Grounded on PCB.
C1+	37		Positive terminal of charge pump capacitor
V_{CC}	38	P	3V to 5.5V supply voltage
C2+	39		Positive terminal of charge pump capacitor
V+	40		Positive charge pump rail

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Bus supply voltage	V_{CC} to GND	–0.5	6	V
Logic supply voltage	V_{IO} to GND	–0.5	V_{CC} + 0.2	V
Charge pump positive-output supply voltage	V+ to GND	–0.3	14	V
Charge pump negative-output supply voltage	V- to GND	-14	0.3	V
Bus voltage	Voltage at any bus pin (R1, R2, R3, R4, R5, R6, R7, R8) with respect to GND	–16	16	V
Differential bus voltage	(R1-R2) or (R2-R1), (R3-R4) or (R4-R3) with termination disabled	-22	22	V
Differential bus voltage RS485 mode	(R1-R2) or (R2-R1), (R3-R4) or (R4-R3) with termination enabled	-6	6	V
Input voltage	Range at any logic pin (L3, L4, L6, SLR, $\overline{SHDN}$, TERM, MODE0, MODE1, MODE2, DIR)	–0.3	V_{IO} + 0.2	V
Receiver output current	I_O (L1, L2, L5, L7, L8)	–8	8	mA
Storage temperature	T_{stg}	–65	150	°C
Junction temperature	T_J	-40	170	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus terminals (R1, R2, R3, R4, R5, R6, R7, R8) and GND	±16,000	V
			All pins except bus terminals and GND	±4,000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1,500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings [IEC]

				VALUE	UNIT
$V_{(ESD)}$		Contact discharge, per IEC 61000-4-2	Bus terminals (R1, R2, R3, R4, R5, R6, R7, R8) and GND	±8,000	V
		Air-gap discharge, per IEC 61000-4-2		±15,000	
$V_{(EFT)}$	Electrical fast transient in RS485 HD or FD mode	Per IEC 61000-4-4	Bus terminals (R1, R2, R3, R4)	±4,000	V

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		5.5	V
V_{IO}	I/O supply voltage		1.65		V_{CC}	V
$V_{I\ (RS-485)}$	Input voltage at any bus terminal (R1, R2, R3, R4) in RS-485 mode(1)		–7		12	V
V_{ID}	Differential input voltage in RS-485 receive mode [(R1-R2) or (R2-R1), (R3-R4) or (R4-R3)] with on-chip termination resistor disabled		-12		12	V
V_{ID}	Differential input voltage in RS-485 receive mode [(R1-R2) or (R2-R1), (R3-R4) or (R4-R3)] with on-chip termination resistor enabled		- 5.5		5.5	V
$V_{I\ (RS-232)}$	Receiver input voltage in RS-232 mode		-15		15	V
V_{IH}	High-level input voltage (L3, L4, L6, SLR, $\overline{SHDN}$, TERM, MODE0, MODE1, MODE2, DIR inputs)		$0.7xV_{IO}$		V_{IO}	V
V_{IL}	Low-level input voltage (L3, L4, L6, SLR, $\overline{SHDN}$, TERM, MODE0, MODE1, MODE2, DIR inputs)		0		$0.3xV_{IO}$	V
I_O	Output current, driver in RS-485 mode		–60		60	mA
I_{OR}	Output current, receiver	V_{IO} = 1.8V or 2.5V	–2		2	mA
I_{OR}	Output current, receiver	V_{IO} = 3.3V or 5V	–4		4	mA
R_L	Differential load resistance in RS-485 mode		54	60		Ω
$1/t_{UI}$	Signaling rate in RS-485 mode	SLR = V_{IO}			500	kbps
		SLR = GND or floating			20	Mbps
	Signaling rate in RS-232 mode	SLR = V_{IO}			250	kbps
		SLR = GND or floating			1	Mbps
$1/t_{UI\ (loopback)}$	Signaling rate in RS-485 loopback mode				0.5	Mbps
	Signaling rate in RS-232 loopback mode				1	Mbps
T_A (2)	Operating ambient temperature		-40		125	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) Operation is specified for internal (junction) temperatures up to 150°C. Self-heating due to internal power dissipation must be considered for each application. Maximum junction temperature is internally limited by the thermal shut-down (TSD) circuit which disables the driver and receiver when the junction temperature reaches 170°C.

5.5 Thermal Information

THERMAL METRIC(1)		THVD4431A RHA (QFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.6 Power Dissipation

PARAMETER		TEST CONDITIONS			Typical	Max	UNIT
$P_{D\ (RS-485)}$	Full Duplex mode with DIR = V_{IO}, MODE2, MODE1, MODE0 = 011, R2/R1 are externally connected to R3/R4 in loopback fashion; V_{IO} = V_{CC} = 5.5V, T_A = 125 °C, L3 = square wave 50% duty	Unterminated, TERM = L	SLR = H	500kbps	160	200	mW
			SLR = L	20Mbps	390	450	
		TERM = V_{IO}	SLR = H	500kbps	430	500	mW
			SLR = L	20Mbps	500	575	
$P_{D\ (RS-232)}$	RS-232 mode with MODE2, MODE1, MODE0 = 001	V_{CC} = V_{IO} = 5.5V, R3, R4, R6 bus lines loaded with 3kΩ, R3 load cap = 1000pF, L3 toggling	SLR = L	1Mbps	320	500	mW
		V_{CC} = V_{IO} = 5.5V, R3, R4, R6 bus lines loaded with 3 kΩ, R3 load cap = 2500pF, L3 toggling	SLR = H	250kbps	185	200	mW

5.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5V, V_{IO} = 3.3V , unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver_RS-485							
$\lvert V_{OD}\rvert$	Driver differential output voltage magnitude	R_L = 60Ω, –7V ≤ V_{test} ≤ 12V (See Figure 6-1)		1.5	2		V
		R_L = 60Ω, –7V ≤ V_{test} ≤ 12V, 4.5V ≤ V_{CC} ≤ 5.5V (See Figure 6-1)		2.1	3		V
		R_L = 100Ω (See Figure 6-2)		2	2.5		V
		R_L = 54Ω, 4.5V ≤ V_{CC} ≤ 5.5V (See Figure 6-2)		2.1	3.3		V
		R_L = 54Ω (See Figure 6-2)		1.5	3.3		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage	R_L = 54Ω or 100Ω (See Figure 6-2)		–50		50	mV
V_{OC}	Common-mode output voltage	R_L = 54Ω or 100Ω (See Figure 6-2)			V_{CC}/2	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	R_L = 54Ω or 100Ω (See Figure 6-2)		–50		50	mV
I_{OS}	Short-circuit output current (bus terminals)	DIR = V_{IO}, -7V ≤ (V_{R2} or V_{R1}) ≤ 12V, or R1 shorted to R2		–250		250	mA
I_{OZD}	Driver High impedance output leakage current on R1 and R2 in Full duplex mode	MODE2, MODE1, MODE0 = 011, DIR = GND, V_{CC} = GND or 5.5V, V_O = -7V, +12V		-125		125	µA
		MODE2, MODE1, MODE0 = 011, DIR = GND, V_{CC} = 5.5V, V_O = -7V, +12V		- 325		350	µA
Receiver_RS-485							
I_I	Bus input current (termination disabled)	Half and full duplex modes, DIR = 0V, V_{CC} and V_{IO} = 0V or 5.5V	V_I = 12V		75	125	µA
			V_I = –7V	–125	–70		µA
I_{RXT}	Receiver bus input leakage current with termination enabled	Full duplex mode, V_{CC} and V_{IO} = 5.5V, TERM = V_{IO}	VI = - 7 to 12V	-325		325	µA
V_{TH+}	Positive-going input threshold voltage(1)	Over common-mode range of - 7V to 12V			- 70	- 40	mV
V_{TH-}	Negative-going input threshold voltage(1)			–200	–150		mV
V_{HYS}	Input hysteresis			25	80		mV
$C_{A,B}$	Input differential capacitance	Measured between R3 and R4, f = 1MHz			45		pF
V_{OH}	Output high voltage, L2 pin	I_{OH} = –4mA, V_{IO} = 3 to 3.6V or 4.5V to 5.5V		V_{IO} – 0.4	V_{IO} – 0.2		V
V_{OL}	Output low voltage, L2 pin	I_{OL} = 4mA, V_{IO} = 3 to 3.6V or 4.5V to 5.5V			0.2	0.4	V
V_{OH}	Output high voltage, L2 pin	I_{OH} = –2mA, V_{IO} = 1.65 to 1.95V or 2.25V to 2.75V		V_{IO} – 0.4	V_{IO} – 0.2		V
V_{OL}	Output low voltage, L2 pin	I_{OL} = 2mA, V_{IO} = 1.65 to 1.95V or 2.25V to 2.75V			0.2	0.4	V
I_{OZ}	Output high-impedance current, L2 pin	V_O = 0V or V_{IO}, DIR = VIO, MODE2, MODE1, MODE0= 010 (half duplex mode)		–8		2	µA
Driver_RS-232							

5.7 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5V, V_{IO} = 3.3V , unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	All DOUT (R3, R4, R6) at R_L = 3kΩ to GND, DIN (L3, L4, L6) = GND; V_{CC} = 3V to 3.6V			5	5.5	7.2	V
V_{OL}	Low-level output voltage	All DOUT (R3, R4, R6) at R_L = 3kΩ to GND, DIN (L3, L4, L6) = V_{IO} ; V_{CC} = 3V to 3.6V			–7.2	–5.5	-5	V
V_{OH}	High-level output voltage	All DOUT (R3, R4, R6) at R_L = 3kΩ to GND, DIN (L3, L4, L6) = GND; V_{CC} = 4.5V to 5.5V			7.8	9	11	V
V_{OL}	Low-level output voltage	All DOUT (R3, R4, R6) at R_L = 3kΩ to GND, DIN (L3, L4, L6) = V_{IO} ; V_{CC} = 4.5V to 5.5V			–11	–9	-7.8	V
I_{OS}	Short-circuit output current (2)	V_{CC} = 3.6V	V_O = 0V			±35	±60	mA
		V_{CC} = 5.5V	V_O = 0V					
r_o	Output resistance on R3, R4, R6	V_{CC} = 0V, V_+ = 0V, and V_- = 0V	V_O = ±2V		300	10M		Ω
I_{off}	Output leakage current on R3, R4, R6	$\overline{SHDN}$ = GND	V_O = ±12V	V_{CC} = 3 to 3.6V			±125	µA
			V_O = ±10V	V_{CC} = 4.5 to 5.5V			±125	µA
Receiver_RS-232								
V_{OH}	High-level output voltage L1/L2/L5/L7/L8	I_{OH} = –4mA, V_{IO} = 3 to 3.6V or 4.5V to 5.5V			V_{IO} – 0.5	V_{IO} – 0.2		V
		I_{OH} = –2mA, V_{IO} = 1.65 to 1.95V or 2.25V to 2.75V			V_{IO} – 0.48	V_{IO} – 0.2		V
V_{OL}	Low-level output voltage L1/L2/L5/L7/L8	I_{OL} = 4mA, V_{IO} = 3 to 3.6V or 4.5V to 5.5V					0.4	V
		I_{OL} = 2mA, V_{IO} = 1.65 to 1.95V or 2.25V to 2.75V					0.4	V
V_{IT+}	Positive-going input threshold voltage on RS-232 receiver inputs (R1, R2, R5, R7, R8)	V_{CC} = 3.3V				1.6	2.4	V
		V_{CC} = 5V				1.9	2.4	V
$V_{IT–}$	Negative-going input threshold voltage on RS-232 receiver inputs (R1, R2, R5, R7, R8)	V_{CC} = 3.3V			0.6	1.1		V
		V_{CC} = 5V			0.8	1.4		V
V_{hys}	Input hysteresis on receiver inputs (V_{IT+} – $V_{IT–}$)				0.4	0.5		V
I_{off}	Output leakage current on receiver output pins L1/L2/L5/L7/L8	$\overline{SHDN}$ = 0V				±0.05	±10	µA
r_I	Input resistance on receiver input pins	-15V ≤ V_I ≤ 15V			3	5	7	kΩ
Thermal Protection								
T_{SHDN}	Thermal shutdown threshold	Temperature rising			150	170		°C
T_{HYS}	Thermal shutdown hysteresis					15		°C
Supply								
UV_{VCC} (rising)	Rising under-voltage threshold on V_{CC}					2.5	2.8	V
UV_{VCC} (falling)	Falling under-voltage threshold on V_{CC}				1.9	2.1		V
$UV_{VCC(hys)}$	Hysteresis on under-voltage of V_{CC}				100	400		mV
UV_{VIO} (rising)	Rising under-voltage threshold on V_{IO}					1.5	1.6	V
UV_{VIO} (falling)	Falling under-voltage threshold on V_{IO}				1.2	1.4		V
$UV_{VIO(hys)}$	Hysteresis on under-voltage of V_{IO}				85	100		mV

5.7 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5V, V_{IO} = 3.3V , unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC_SHDN}	Supply current in shutdown mode	V_{CC} = 4.5V to 5.5V, $\overline{SHDN}$ = GND, All other logic input pins floating, no load on bus, $T_A \le 125$ °C			5	20	µA
		V_{CC} = 3V to 3.6V, $\overline{SHDN}$ = GND, All other logic input pins floating, no load on bus, $T_A \le 125$ °C			3	15	µA
		V_{CC} = 4.5V to 5.5V, $\overline{SHDN}$ = GND, All other logic input pins floating, no load on bus, $T_A \le 105$ °C			5	15	µA
		V_{CC} = 3V to 3.6V, $\overline{SHDN}$ = GND, All other logic input pins floating, no load on bus, $T_A \le 105$ °C			3	10	µA
I_{IO_SHDN}	Logic supply current in shutdown mode	V_{IO} = 1.65V to 5.5V, $\overline{SHDN}$ = GND, All other logic input pins floating				3	µA
I_{CC_485}	Supply current (quiescent), V_{CC} = 4.5V to 5.5V TERM = Floating or low, SLR = X	Driver and receiver enabled, DIR = V_{IO}, MODE2, MODE1, MODE0 = 011 (Full duplex)	No load		1.7	3.5	mA
		Driver enabled, receiver disabled, DIR = V_{IO}, MODE2, MODE1, MODE0 = 010 (Half duplex)	No load		1.3	2.8	mA
		Driver disabled, receiver enabled, DIR = GND, MODE2, MODE1, MODE0 = 010 (Half duplex)	No load		0.8	1.5	mA
I_{CC_485}	Supply current (quiescent), V_{CC} = 3V to 3.6V TERM = Floating or low, SLR = X	Driver and receiver enabled, DIR = V_{IO}, MODE2, MODE1, MODE0 = 011 (Full duplex)	No load		1.5	2.9	mA
		Driver enabled, receiver disabled, DIR = V_{IO}, MODE2, MODE1, MODE0 = 010 (Half duplex)	No load		1	2.4	mA
		Driver disabled, receiver enabled, DIR = GND, MODE2, MODE1, MODE0 = 010 (Half duplex)	No load		0.7	1.3	mA
I_{IO_485}	Logic supply current (quiescent), V_{IO} = 3 to 3.6V TERM = Floating	Driver disabled, Receiver enabled, SLR = GND, DIR = GND; MODE2, MODE1, MODE0 = 010 (half duplex)	No load		7	17	µA
		Driver disabled, Receiver enabled, SLR = V_{IO}; DIR = GND; MODE2, MODE1, MODE0 = 010 (half duplex)	No load		8	21	µA
I_{CCDT_485}	Supply current in RS-485 driver termination mode	Driver enabled with termination ON; MODE2, MODE1, MODE0 = 011 (full duplex)	DIR= V_{IO}		38	50	mA
I_{CCRT_485}	Supply current in RS-485 receiver termination mode	Receiver enabled with termination ON; MODE2, MODE1, MODE0 = 011 (full duplex)	DIR = GND, TERM = V_{IO}		1	1.5	mA
I_{CC_RS232}	Supply current in RS-232 mode	MODE2, MODE1, MODE0 = 001, $\overline{SHDN}$ = V_{IO}; other logic inputs floating	No load		4	6	mA
$I_{CC\_RS232\_LB}$	Supply current in RS-232 loopback mode	MODE2 = 1, MODE1 = 0, MODE0 = 0; L3 = L4 = L6 = static logic high, -40 °C ≤ T_A ≤ 85 °C	No extra load on RS-232 drivers or on logic output		25	31	mA
$I_{CC\_RS485\_LB}$	Supply current in RS-485 loopback mode	MODE2 = MODE1= MODE0 = V_{IO} ; L3 = static logic high	No load on bus or logic output		3	4	mA
On-Chip termination resistor_RS-485							
R_{TERM_FD}	120Ω termination across receiver output R3/R4 terminals	MODE2, MODE1, MODE0 = 011 (Full duplex); TERM = V_{IO}, V_{R3R4} = 2V, V_{R4} = -7V, 0V, 10V; See Figure 6-9		102	120	138	Ω
Logic							
I_{IN}	Input current (L3, L4, L6, DIR, $\overline{SHDN}$, SLR, TERM, MODE2, MODE1, MODE0)	1.65V ≤ V_{IO} ≤ 5.5V, 0V ≤ V_{IN} ≤ V_{IO}		-20		5	µA
$V_{IT+(IN)}$	Rising threshold: logic inputs	1.65V ≤ V_{IO} ≤ 5.5V			0.6xV_{IO}	0.7xV_{IO}	V
$V_{IT-(IN)}$	Falling threshold: logic inputs			0.3xV_{IO}	0.4xV_{IO}		V
$V_{IN(HYS)}$	Input threshold: logic inputs			0.1xV_{IO}	0.2xV_{IO}		V

(1) Under any specific conditions, V_{TH+} is verified to be at least V_{HYS} higher than V_{TH-}.
(2) Short-circuit durations must be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output must be shorted at a time.

5.8 Switching Characteristics_RS-485_500kbps

500kbps (with SLR = V_{IO}) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5V , V_{IO} = 3.3V, unless otherwise noted. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54Ω, C_L = 50pF See Figure 6-3	V_{CC} = 3to 3.6V, Typical at 3.3V	210	300	600	ns
			V_{CC} = 4.5to 5.5V, Typical at 5V	250	300	600	ns
t_{PHL}, t_{PLH}	Propagation delay		V_{CC} = 3to 3.6V, Typical at 3.3V		250	450	ns
			V_{CC} = 4.5to 5.5V, Typical at 5V		250	450	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$		V_{CC} = 3to 3.6V, Typical at 3.3V		2	15	ns
			V_{CC} = 4.5to 5.5V, Typical at 5V		2	15	ns
t_{PHZ}, t_{PLZ}	Disable time	MODE2, MODE1, MODE0= 010(half duplex) or 011(full duplex)	See Figure 6-4		80	150	ns
t_{PZH}, t_{PZL}	Enable time	MODE2, MODE1, MODE0= 011(full duplex): receiver enabled			200	650	ns
Receiver							
t_r, t_f	Output rise/fall time	C_L = 15pF	See Figure 6-4		5	10	ns
t_{PHL}, t_{PLH}	Propagation delay				700	1200	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$				10	45	ns
t_{PHZ}, t_{PLZ}	Disable time in half duplex mode	MODE2, MODE1, MODE0= 010	See Figure 6-7		30	80	ns
$t_{PZH(1)}$	Enable time in half duplex mode				60	155	ns
$t_{PZL(1)}$					450	1250	ns
$t_{PZH(2)}$, $t_{PZL(2)}$	Enable time from shutdown with TX disabled in full duplex mode	DIR = 0V; MODE2, MODE1, MODE0= 011	See Figure 6-8		7	16	µs

(1) R3, R4are RX input, R2/R1are driver output terminals in Full duplex mode

5.9 Switching Characteristics_RS-485_20Mbps

20Mbps (SLR = GND) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5V, V_{IO} = 3.3V. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54Ω, C_L = 50pF See Figure 6-3	V_{CC} = 3to 3.6V, Typical at 3.3V	5	10	15	ns
			V_{CC} = 4.5to 5.5V, Typical at 5V	5	10	15	ns
t_{PHL}, t_{PLH}	Propagation delay		V_{IO} = 1.65V to 1.95V	14	25	58	ns
			V_{IO} = 3V to 3.6V	9	20	46	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$		V_{CC} = 3to 3.6V, Typical at 3.3V		1	3.5	ns
			V_{CC} = 4.5to 5.5V, Typical at 5V		1	3.5	ns
t_{PHZ}, t_{PLZ}	Disable time	MODE2, MODE1, MODE0= 010(half duplex) or 011(full duplex)	See Figure 6-4		11	65	ns
t_{PZH}, t_{PZL}	Enable time	MODE2, MODE1, MODE0= 011(full duplex): receiver enabled			8	80	ns
Receiver							
t_r, t_f	Output rise/fall time	C_L = 15pF	See Figure 6-6		5	10	ns
t_{PHL}, t_{PLH}	Propagation delay				40	70	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$					10	ns

5.9 Switching Characteristics_RS-485_20Mbps (continued)

20Mbps (SLR = GND) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5V, V_{IO} = 3.3V. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHZ}, t_{PLZ}	Disable time in half duplex mode	MODE2, MODE1, MODE0= 010	See Figure 6-7		20	80	ns
$t_{PZH(1)}$, $t_{PZL(1)}$	Enable time in half duplex mode (includes driver disable time as per setup)				50	160	ns
$t_{PZH(2)}$, $t_{PZL(2)}$	Enable time from shutdown with TX disabled in full duplex mode	DIR = 0V; MODE2, MODE1, MODE0= 011	See Figure 6-8		4	15	µs

(1) R3, R4are RX input, R2/R1are driver output terminals in Full duplex mode.

5.10 Switching Characteristics, Driver_RS232

over recommended ranges of supply voltage and operating free-air temperature(unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
250kbps							
	Maximum data rate	R_L = 3kΩ One DOUT switching	C_L = 2500pF See Figure 6-16	250	500		kbps
t_{PHL}, t_{PHL}	Transmitter propagation delay	R_L = 3kΩ to 7kΩ	C_L = 150pF to 2500pF See Figure 6-16		0.8	2	µs
$t_{sk(p)}$	Transmitter Pulse skew(3)				220	600	ns
SR(tr)	Slew rate, transition region	V_{CC} = 3.3V ± 10%, 5V ± 10% , R_L = 3kΩ to 7kΩ, See Figure 6-17	C_L = 150pF to 1000pF	6		30	V/µs
			C_L = 150pF to 2500pF	4		30	
1Mbps							
	Maximum data rate	R_L = 3kΩ One DOUT switching, See Figure 6-16	C_L = 250pF, V_{CC} = 3to 3.6V	1000			kbps
			C_L = 1000pF, V_{CC} = 4.5to 5.5V	1000			kbps
t_{PLH}, t_{PHL}	Transmitter propagation delay	R_L = 3k to 7kΩ, See Figure 6-16	C_L = 150pF to 1000pF		300	800	ns
$t_{sk(p)}$	Pulse skew(3)				25	150	ns
SR(tr)	Slew rate, transition region	R_L = 3k to 7kΩ, V_{CC} = 4.5V to 5.5V	C_L = 150pF to 1000pF See Figure 6-17	18		150	V/µs
		R_L = 3k to 7kΩ, V_{CC} = 3V to 3.6V		15		150	V/µs

(1) Test conditions are C1–C4= 0.1µF at V_{CC} = 3.3V + 0.3V; V_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 3.3V or V_{CC} = 5V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

5.11 Switching Characteristics, Receiver_RS232

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
250kbps						
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150pF, See Figure 6-18		150	550	ns
t_{PHL}	Propagation delay time, high- to low-level output			150	550	ns
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 15pF, See Figure 6-18		130	520	ns
t_{PHL}	Propagation delay time, high- to low-level output			130	520	ns
t_{R_232}, t_{F_232}	Rise/fall time (receiver buffer output), V_{IO} = 3to 5.5V	C_L = 150pF, See Figure 6-18		20	50	ns
		C_L = 15pF, See Figure 6-18		5	10	ns
	Rise/fall time (receiver buffer output), V_{IO} = 1.65to 2.75V	C_L = 150pF, See Figure 6-18		40	90	ns
		C_L = 15pF, See Figure 6-18		10	20	ns
t_{en}	Output enable time	C_L = 150pF, R_L = 3kΩ, See Figure 6-19		6	14	µs
t_{dis}	Output disable time			100	200	ns

5.11 Switching Characteristics, Receiver_RS232 (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
$t_{sk(p)}$	Pulse skew(3)	C_L = 150pF, See Figure 6-18		50	135	ns
		C_L = 15pF, See Figure 6-18		50	135	ns
1Mbps						
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150pF, See Figure 6-18		150	550	ns
t_{PHL}	Propagation delay time, high- to low-level output			150	550	ns
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 15pF, See Figure 6-18		130	520	ns
t_{PHL}	Propagation delay time, high- to low-level output			130	520	ns
t_{R_232}, t_{F_232}	Rise/fall time (receiver buffer output), V_{IO} = 3to 5.5V	C_L = 150pF, See Figure 6-18		20	50	ns
		C_L = 15pF, See Figure 6-18		5	10	ns
	Rise/fall time (receiver buffer output), V_{IO} = 1.65to 2.75V	C_L = 150pF, See Figure 6-18		40	90	ns
		C_L = 15pF, See Figure 6-18		10	20	ns
t_{en}	Output enable time	C_L = 150pF, R_L = 3kΩ, See Figure 6-19		6	14	µs
t_{dis}	Output disable time			100	200	ns
$t_{sk(p)}$	Pulse skew(3)	C_L = 150pF, See Figure 6-18		50	125	ns
		C_L = 15pF, See Figure 6-18		50	125	ns

(1) Test conditions are C1–C4= 0.1µF at V_{CC} = 3.3V ± 0.3V; C1= 0.047µF, C2–C4= 0.33µF atV_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 3.3V or V_{CC} = 5V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

5.12 Switching Characteristics_MODE switching

Parameters over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5V , V_{IO} = 3.3V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RDY}	Time from Shutdown to RS-232 ready	MODE2, MODE1, MODE0 = 000 or floating; $\overline{SHDN}$ = GND to V_{IO}; rest of logic input pins floating, V_{CC} = 4.5V to 5.5V Time from 50% of rising SHDN to charge pump V- supply reaching -8V; See Figure 6-11		0.05	0.6	ms
		MODE2, MODE1, MODE0 = 000 or floating; SHDN = GND to V_{IO}; rest of logic input pins floating, V_{CC} = 3V to 3.6V Time from 50% of rising SHDN to charge pump V- supply reaching -5V; See Figure 6-11		0.1	0.6	ms
t_{R2_R4}	Time to switch from RS-232 3T5R mode to RS-485 Full duplex mode	L3 = Vio, MODE2 = GND, MODE1 from GND to Vio, MODE0 = Vio; $\overline{SHDN}$ = DIR = $V_{IO;}$ SLR, TERM= floating; Time from 50% of MODE1 rising edge to R2 reaching 2V; See Figure 6-12		0.04	0.1	µs
t_{R4_R2}	Time to switch from RS-485 full dupplex mode to RS-232 3T5R mode	L3 = Vio, MODE2 = GND, MODE1 from Vio to GND, MODE0 = Vio; $\overline{SHDN}$ = DIR = $V_{IO;}$ SLR, TERM= floating; Time from 50% of MODE1 falling edge to R2 reaching 300mV; See Figure 6-12		2	2.1	µs
t_{LP_RS232}	Time to switch from RS-232 loopback mode to normal RS-232 mode	MODE2 = MODE1 = VIO, MODE0 from GND to V_{IO}; $\overline{SHDN}$ = V_{IO}, L3 = GND; Time from 50% of MODE0 rising edge to L2 50% rising edge, -40 ℃ ≤ T_A ≤ 85 ℃; See Figure 6-13		2	2.4	µs
t_{RS232_LP}	Time to switch from normal RS-232 mode to RS-232 loopback mode	MODE2 = MODE1 = VIO, MODE0 from V_{IO} to GND; $\overline{SHDN}$ = V_{IO}, L3 = GND; Time from 50% of MODE0 falling edge to L2 50% falling edge, -40 ℃ ≤ T_A ≤ 85 ℃; See Figure 6-13		2	15	µs
t_{LP_RS485}	Time to switch from RS-485 loopback mode to RS-485 full duplex mode	MODE1 = MODE0 = V_{IO}; MODE2 from V_{IO} to GND; $\overline{SHDN}$ = V_{IO} , SLR, TERM_RX= floating; L3 = GND, Time from 50% of MODE2 falling edge to 50% of rising L2; See Figure 6-14		40	50	µs
t_{RS485_LP}	Time to switch from RS-485 full duplex mode to RS-485 loopback mode	MODE1 = MODE0 = V_{IO}; MODE2 from GND to V_{IO} ; $\overline{SHDN}$ = V_{IO} , SLR, TERM= floating; L3 = GND, Time from 50% of MODE2 rising edge to 50% of falling L2; See Figure 6-14		1	2	µs
t_{FHD_RS485}	Time to switch from RS-485 full duplex to half duplex mode	DIR= V_{IO}, MODE2 = GND, MODE1 = V_{IO}; MODE0 from V_{IO} to GND ; $\overline{SHDN}$ = V_{IO} , SLR, TERM= floating; L3= GND, 10k pull down resistor on L2, Time from 50% of MODE0 falling edge to 50% falling edge on L2; See Figure 6-15		0.5	1	µs

5.12 Switching Characteristics_MODE switching (continued)

Parameters over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5V , V_{IO} = 3.3V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{HFD_RS485}	Time to switch from RS-485 half duplex to full duplex mode	DIR= V_{IO}, MODE2 = GND, MODE1 = V_{IO}; MODE0 from GND to V_{IO} ; $\overline{SHDN}$ = V_{IO} , SLR, TERM= floating; L3= GND, 10k pull down resistor on L2, Time from 50% of MODE0 rising edge to 50% rising edge on L2; See Figure 6-15		0.5	1	µs

5.13 Switching Characteristics_RS-485_Termination resistor

Parameters over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5V , V_{IO} = 3.3V, unless otherwise noted.

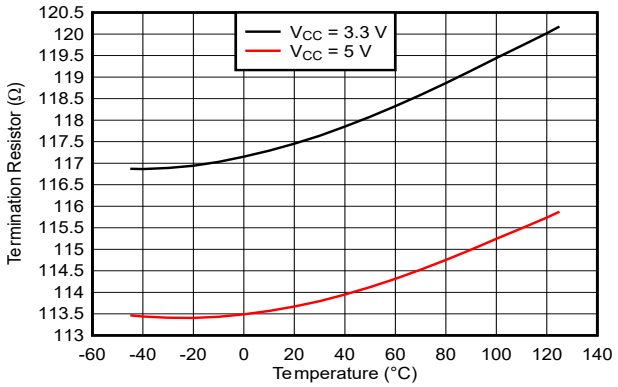
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DTEN}	Driver terminal Termination resistor turn-on time	MODE2, MODE1, MODE0= 011; V_{IO} = 3to 3.6V, DIR = GND, V_{R2R1} = 2V, V_{R1} = 0V; See Figure 6-10		1000	2200	ns
t_{DTZ}	Driver terminal Termination resistor turn-off time	MODE2, MODE1, MODE0= 011; V_{IO} = 3to 3.6V, DIR = GND, V_{R2R1} = 2V, V_{R1} = 0V; See Figure 6-10		2000	7200	ns

5.14 Switching Characteristics_Loopback mode

Parameters over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5V , V_{IO} = 3.3V, unless otherwise noted.

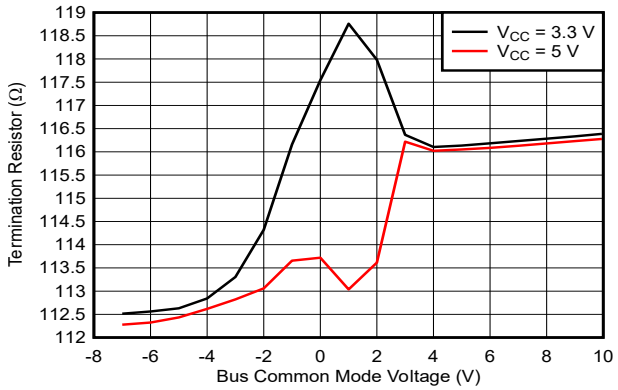
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{LB\_RS232\_rising}$	Delay from Logic input rising edge to logic output rising edge in RS-232Loopback mode	MODE2= VIO, MODE1, MODE0= GND; SLR = GND, Delay from 50% of L3/L4/L6rising edge to 50% L2/L1/L5, L7, L8rising edge, $\overline{SHDN}$ = Vio, TERM float, Load capacitance on output buffers = 15pF, R_L on all 3driver outputs = 3kΩ, -40°C ≤ T_A ≤ 85°C		410	920	ns
		MODE2= VIO, MODE1, MODE0= GND; SLR = Vio, Delay from 50% of L3/L4/L6rising edge to 50% L2/L1/L5, L7, L8rising edge, $\overline{SHDN}$ = Vio, TERM float, Load capacitance on output buffers = 15pF, R_L on all 3driver outputs = 3kΩ, -40°C ≤ T_A ≤ 85°C		640	1100	ns
$t_{LB\_RS232\_falling}$	Delay from Logic input falling edge to logic output falling edge in RS-232Loopback mode	MODE2= VIO, MODE1, MODE0= GND; SLR = GND, Delay from 50% of L3/L4/L6falling edge to 50% L2/L1/L5, L7, L8falling edge, $\overline{SHDN}$ = Vio, TERM float, Load capacitance on output buffers = 15pF, R_L on all 3driver outputs = 3kΩ, -40°C ≤ T_A ≤ 85°C		570	760	ns
		MODE2= VIO, MODE1, MODE0= GND; SLR = Vio, Delay from 50% of L3/L4/L6falling edge to 50% L2/L1/L5, L7, L8falling edge, $\overline{SHDN}$ = Vio, TERM float, Load capacitance on output buffers = 15pF, R_L on all 3driver outputs = 3kΩ, -40°C ≤ T_A ≤ 85°C		600	1500	ns
$t_{SKEW\_RS232\_LB}$	Pulse skew from logic input to logic output in RS232loopback mode	$\lvert t_{LB\_RS232\_rising} - t_{LB\_RS232\_falling} \rvert$, SLR = Vio, -40°C ≤ T_A ≤ 85°C		100	860	ns
		$\lvert t_{LB\_RS232\_rising} - t_{LB\_RS232\_falling} \rvert$, SLR = GND, -40°C ≤ T_A ≤ 85°C		70	250	ns
$t_{LB\_RS485\_rising}$	Delay from Logic input rising edge to logic output rising edge in RS-485Loopback mode	MODE2= MODE1= MODE0= Vio; SLR = Vio, Delay from 50% of L3rising edge to 50% L2rising edge, $\overline{SHDN}$ = Vio, TERM float, Load cap on L2= 15pF, Load on Driver output terminals (R2R1) = 54Ω		1060	1800	ns
$t_{LB\_RS485\_falling}$	Delay from Logic input falling edge to logic output falling edge in RS-485Loopback mode	MODE2= MODE1= MODE0= Vio; SLR = Vio, Delay from 50% of L3falling edge to 50% L2falling edge, $\overline{SHDN}$ = Vio, TERM float, Load cap on L2= 15pF, Load on Driver output terminals (R2R1) = 54 Ω		1060	1800	ns
$t_{SKEW\_RS485\_LB}$	Pulse skew from logic input to logic output in RS485loopback mode	$\lvert t_{LB\_RS485\_rising} - t_{LB\_RS485\_falling} \rvert$, SLR = Vio		5	50	ns

5.15 Typical Characteristics



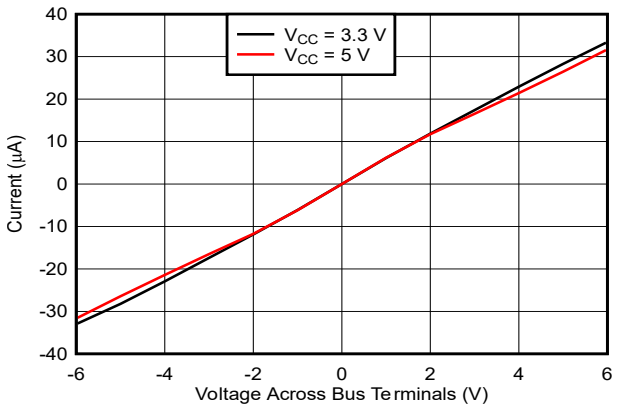
RS-485 Full Duplex mode V(R3R4) = 2V

Figure 5-1. RS-485 Termination Resistor vs Temperature



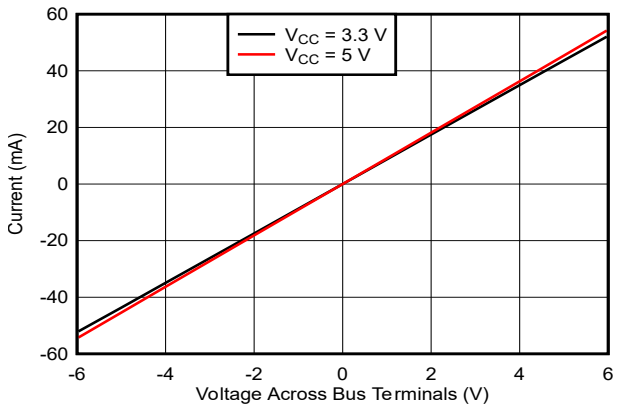
RS-485 Full Duplex mode V(R3R4) = 2V

Figure 5-2. Termination Resistor vs Bus Common Mode Voltage



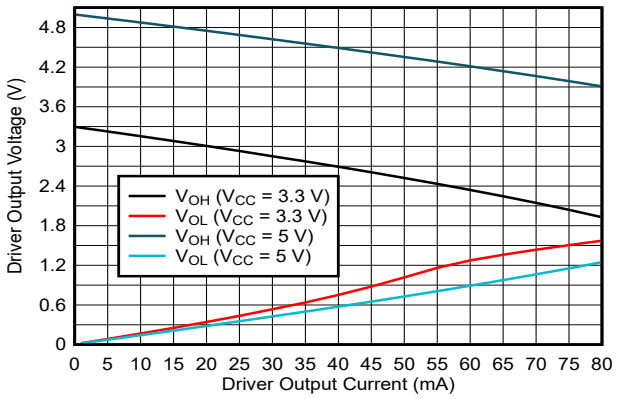
DIR = GND T_A = 25°C

Figure 5-3. Voltage vs Current across R2R1 Bus Pins with Termination OFF



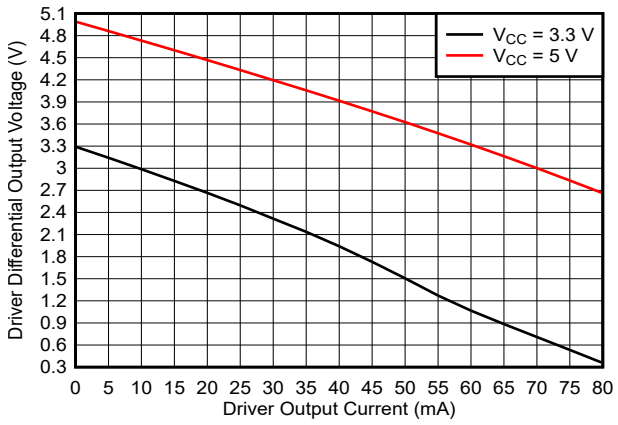
DIR = V_{IO} T_A = 25°C

Figure 5-4. Voltage vs Current across R2R1 Bus Pins with Termination ON



DIR = V_{IO} T_A = 25°C

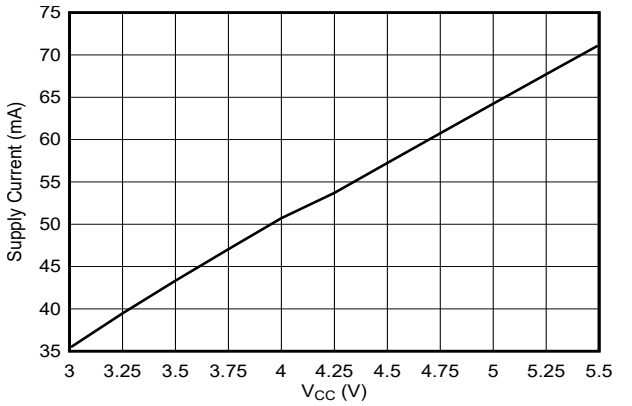
Figure 5-5. RS-485 Driver Output Voltage vs Driver Output Current



DIR = V_{IO} T_A = 25°C

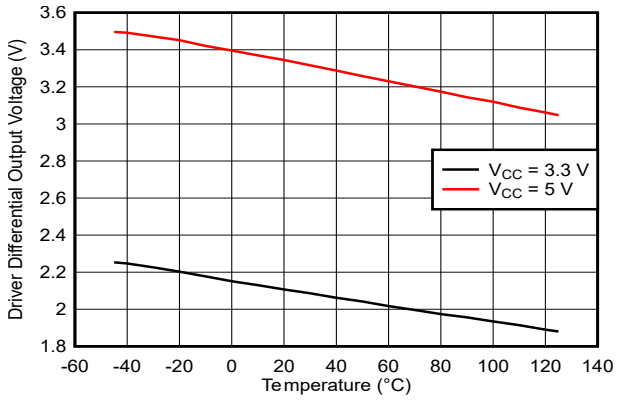
Figure 5-6. RS-485 Driver Differential Output Voltage vs Driver Output Current

5.15 Typical Characteristics (continued)



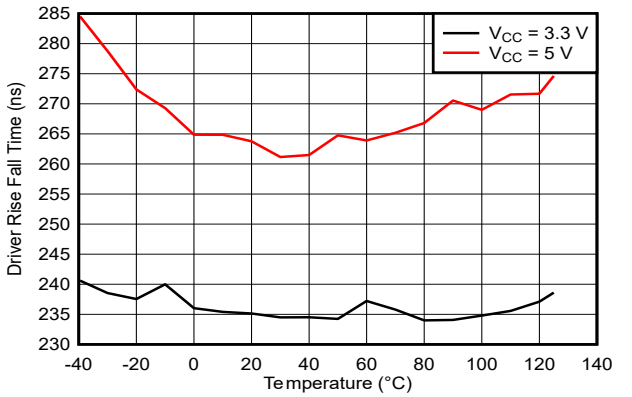
T_A = 25°C R_L = 54Ω DIR = L3 = V_{IO}
RS-485 Full Duplex mode

Figure 5-7. RS-485 Supply Current vs Supply Voltage



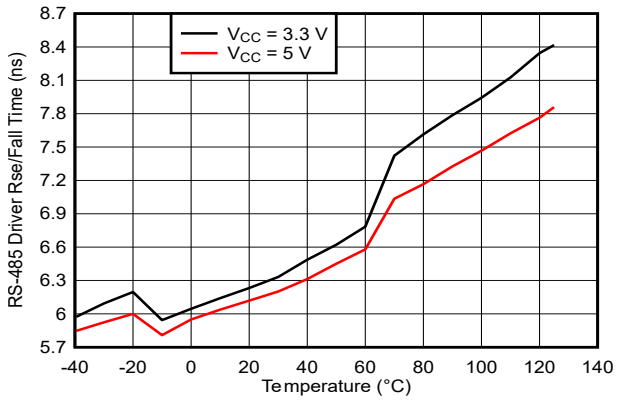
DIR = L3 = V_{IO} R_L = 54Ω
RS-485 Full Duplex mode

Figure 5-8. RS-485 Driver Differential Output Voltage vs Temperature



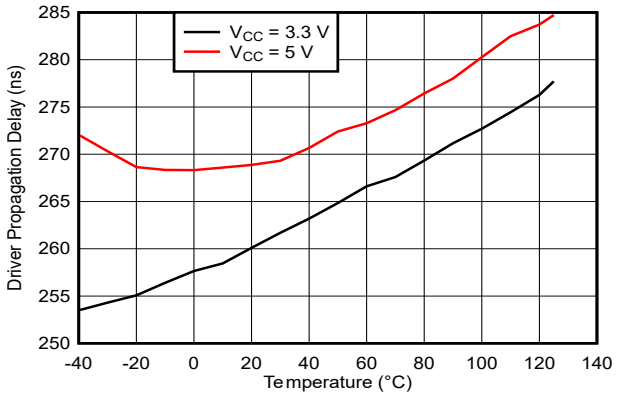
Bus Load = 54Ω || 50pF SLR = V_{IO} DIR = V_{IO}

Figure 5-9. RS-485 500kbps Driver Rise or Fall Time vs Temperature



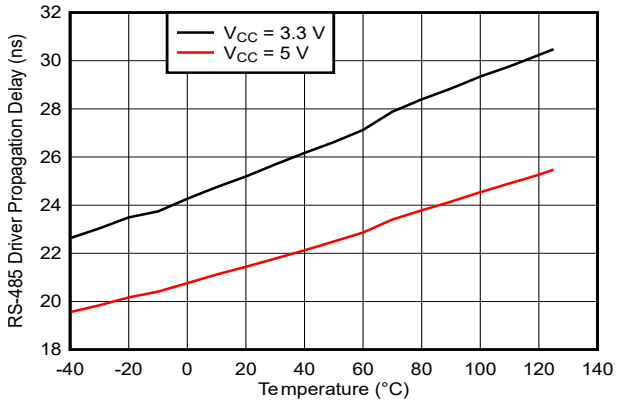
Bus Load = 5Ω || 50pF SLR = GND DIR = V_{IO}

Figure 5-10. RS-485 20Mbps Driver Rise or Fall Time vs Temperature



Bus Load = 54Ω || 50pF SLR = V_{IO} DIR = V_{IO}

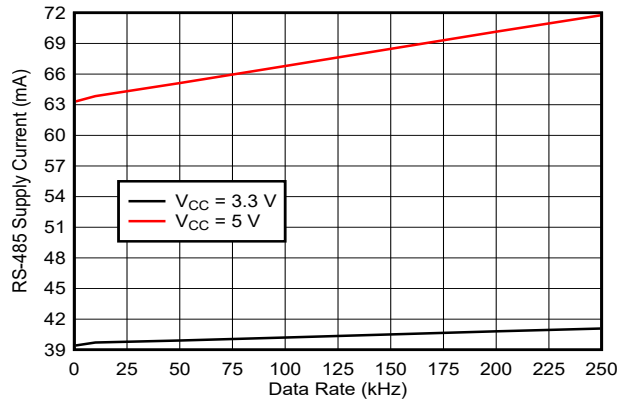
Figure 5-11. RS-485 500kbps Driver Propagation Delay vs Temperature



Bus Load = 54Ω || 50pF SLR = GND DIR = V_{IO}

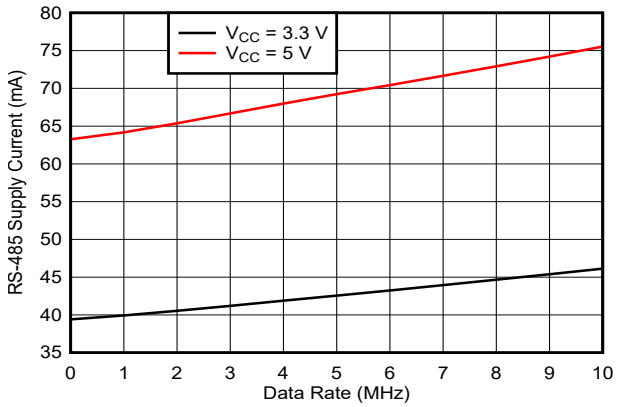
Figure 5-12. RS-485 20Mbps Driver Propagation Delay vs Temperature

5.15 Typical Characteristics (continued)



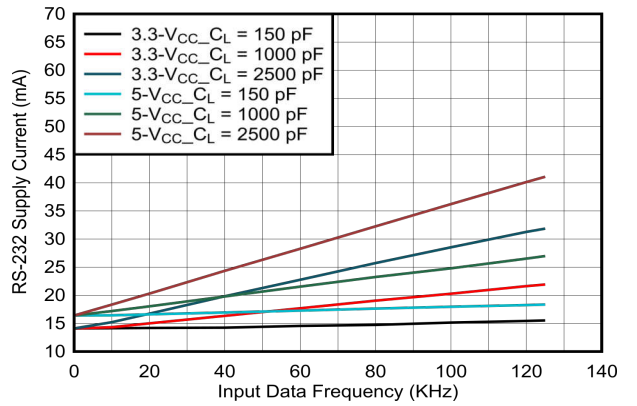
T_A = 25°C R_L = 54Ω DIR = V_{IO}

Figure 5-13. RS-485 500kbps Supply Current vs Signaling Rate



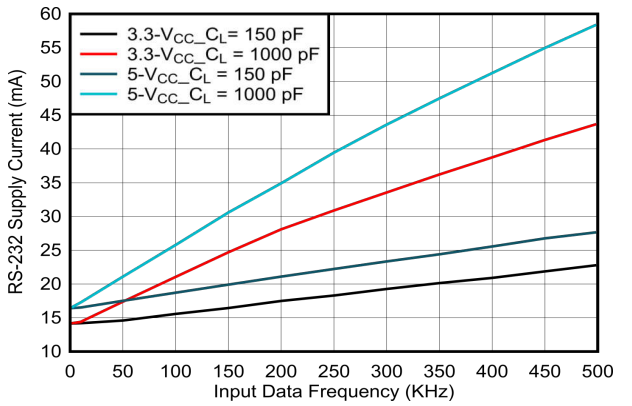
T_A = 25°C R_L = 54Ω DIR = V_{IO}

Figure 5-14. RS-485 20Mbps Supply Current vs Signaling Rate



T_A = 25°C SLR = V_{IO}
All 3 drivers loaded with 5kΩ ; device in RS-232 3T5R mode
L4, L6 = static L3 toggling

Figure 5-15. RS-232 Supply Current vs Signaling Rate for 250kbps Mode



T_A = 25°C SLR = GND
All 3 drivers loaded with 5kΩ ; device in RS-232 3T5R mode
L4, L6 = static L3 toggling

Figure 5-16. RS-232 Supply Current vs Signaling Rate for 1Mbps Mode

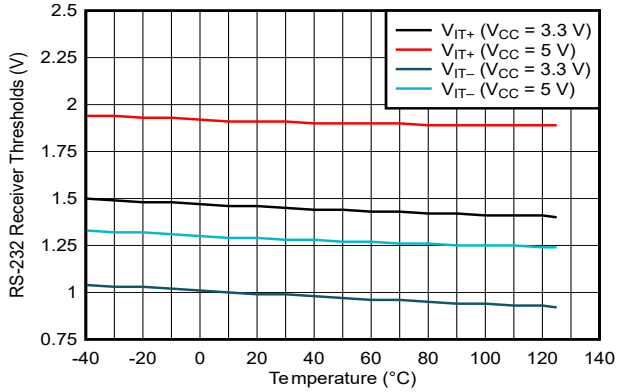


Figure 5-17. RS-232 Receiver Thresholds vs Temperature

6 Parameter Measurement Information

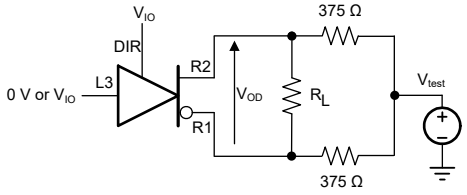


Figure 6-1. Measurement of RS-485 Driver Differential Output Voltage With Common-Mode Load

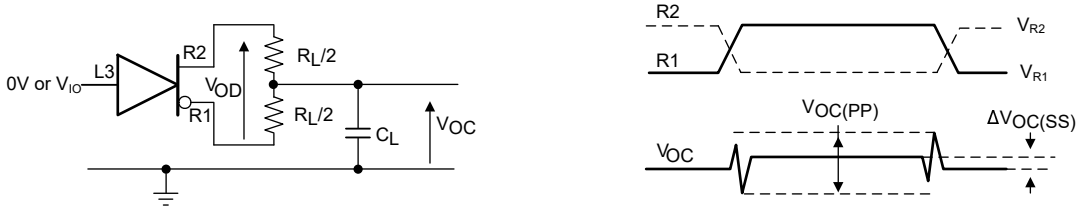


Figure 6-2. Measurement of RS-485 Driver Differential and Common-Mode Output With RS-485 Load

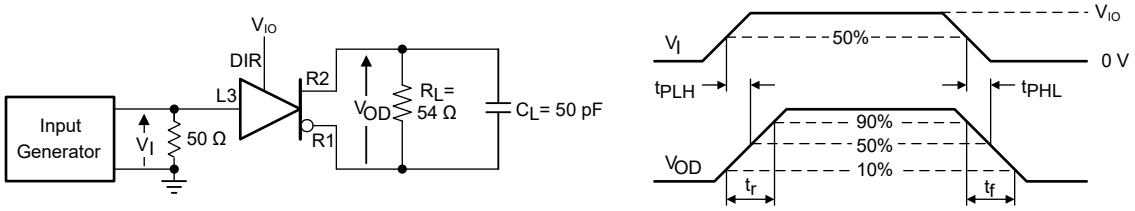


Figure 6-3. Measurement of RS-485 Driver Differential Output Rise and Fall Times and Propagation Delays

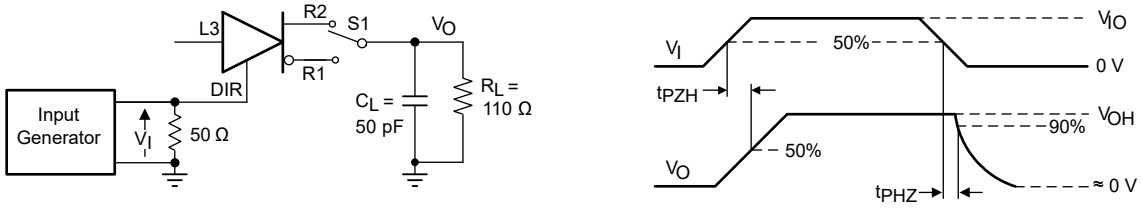


Figure 6-4. Measurement of RS-485 Driver Enable and Disable Times With Active High Output and Pull-Down Load

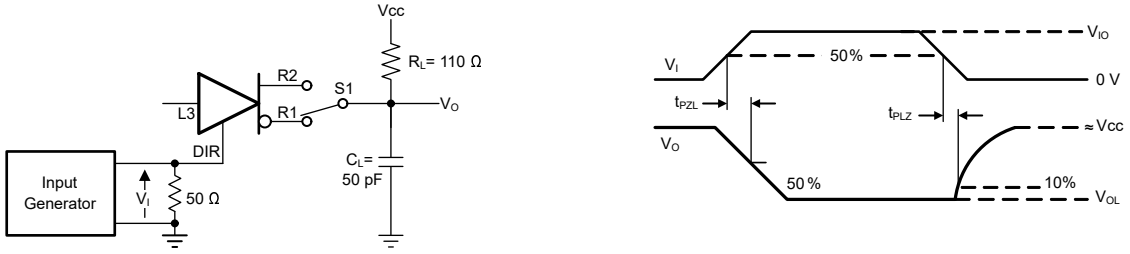


Figure 6-5. Measurement of RS-485 Driver Enable and Disable Times With Active Low Output and Pull-up Load

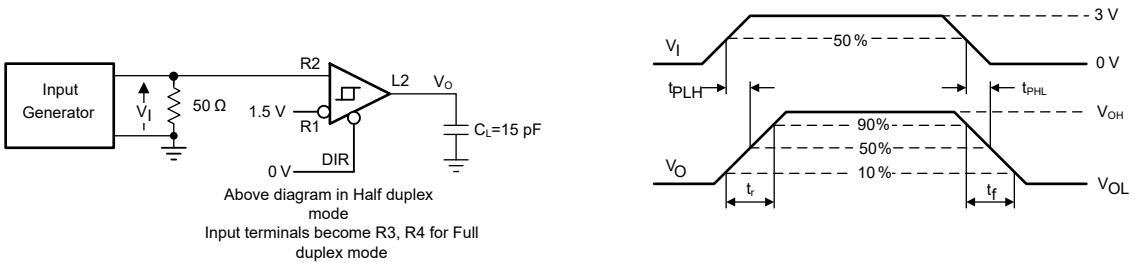


Figure 6-6. Measurement of RS-485 Receiver Output Rise and Fall Times and Propagation Delays

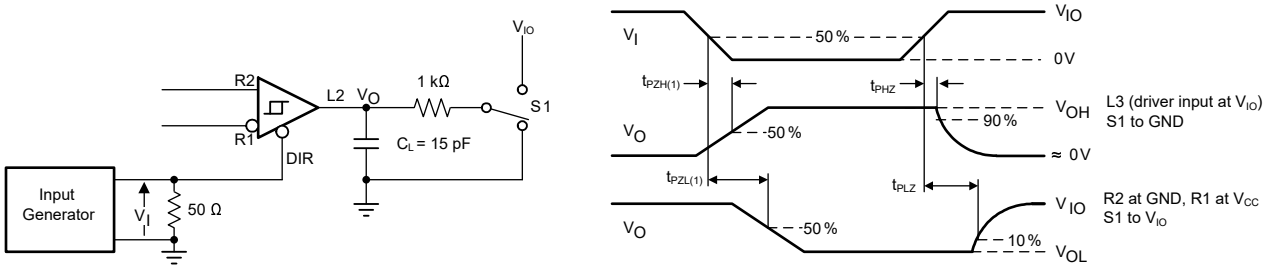


Figure 6-7. Measurement of RS-485 Receiver Enable and Disable Times in Half Duplex Mode

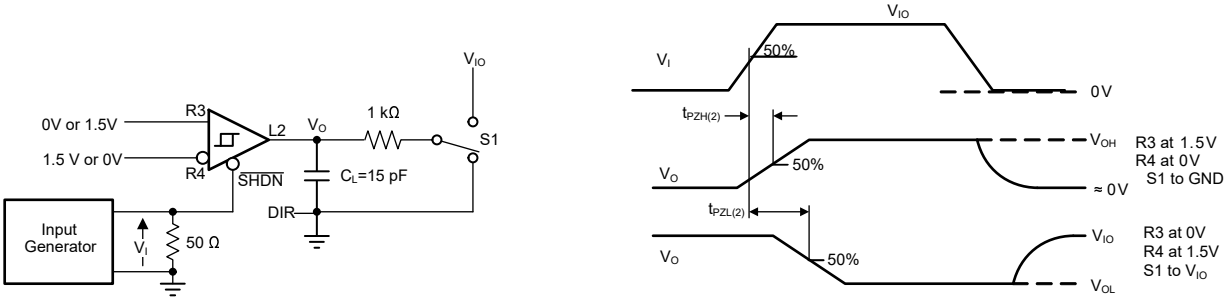


Figure 6-8. Measurement of RS-485 Receiver Enable Time from Shutdown with TX Disabled: Full Duplex Mode

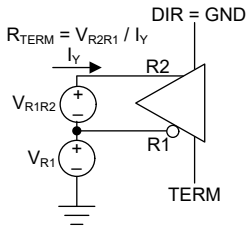


Figure 6-9. Termination Resistor Measurement

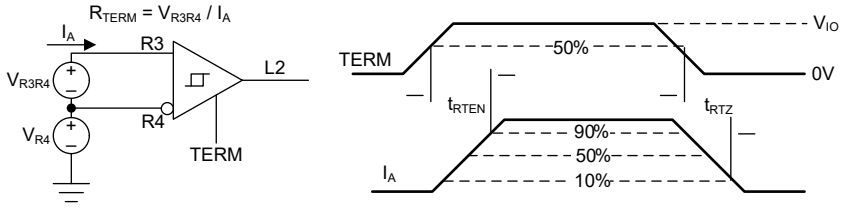


Figure 6-10. Termination Resistor Switching Measurement

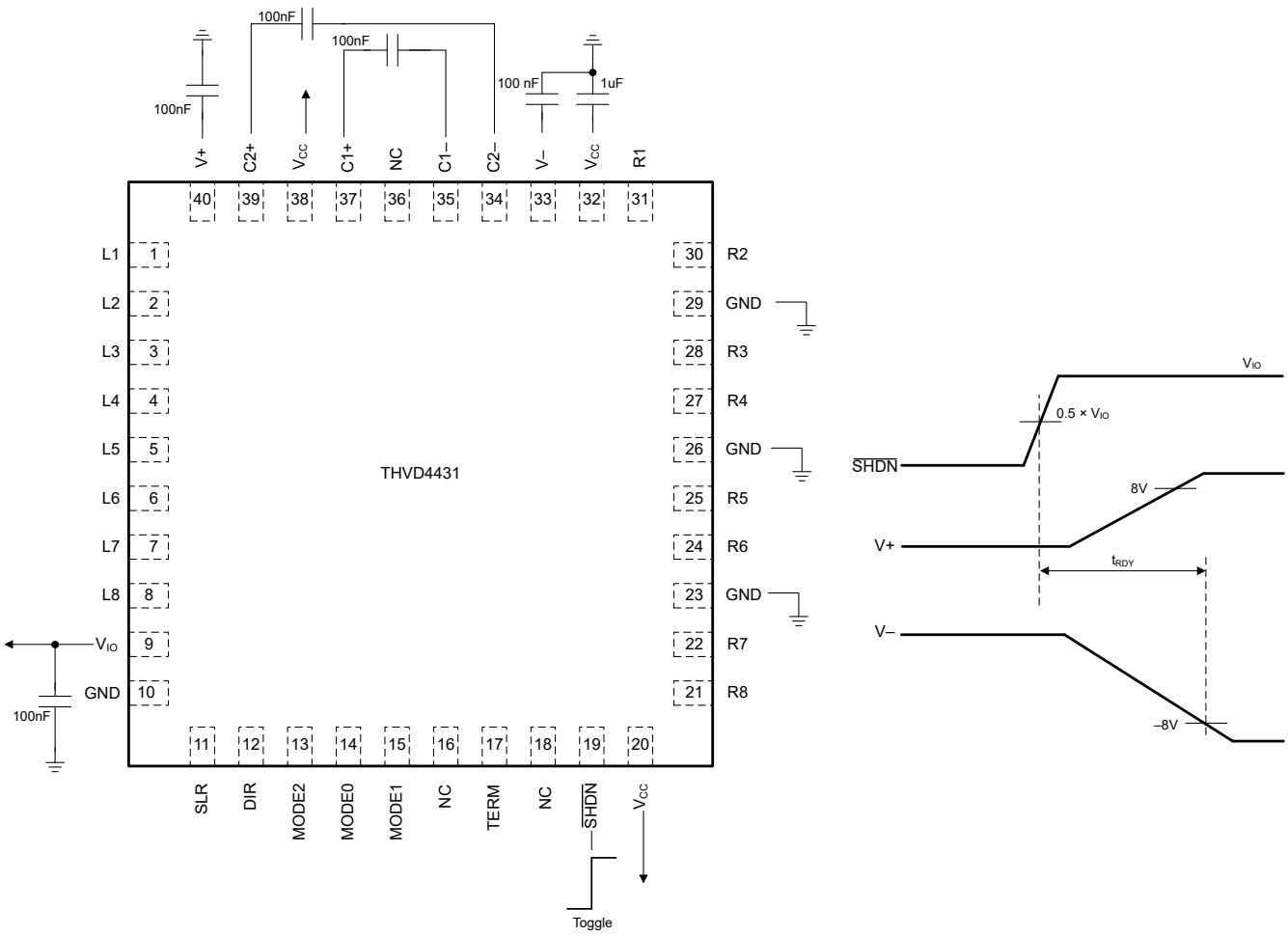


Figure 6-11. Time from Shutdown to RS-232 Ready

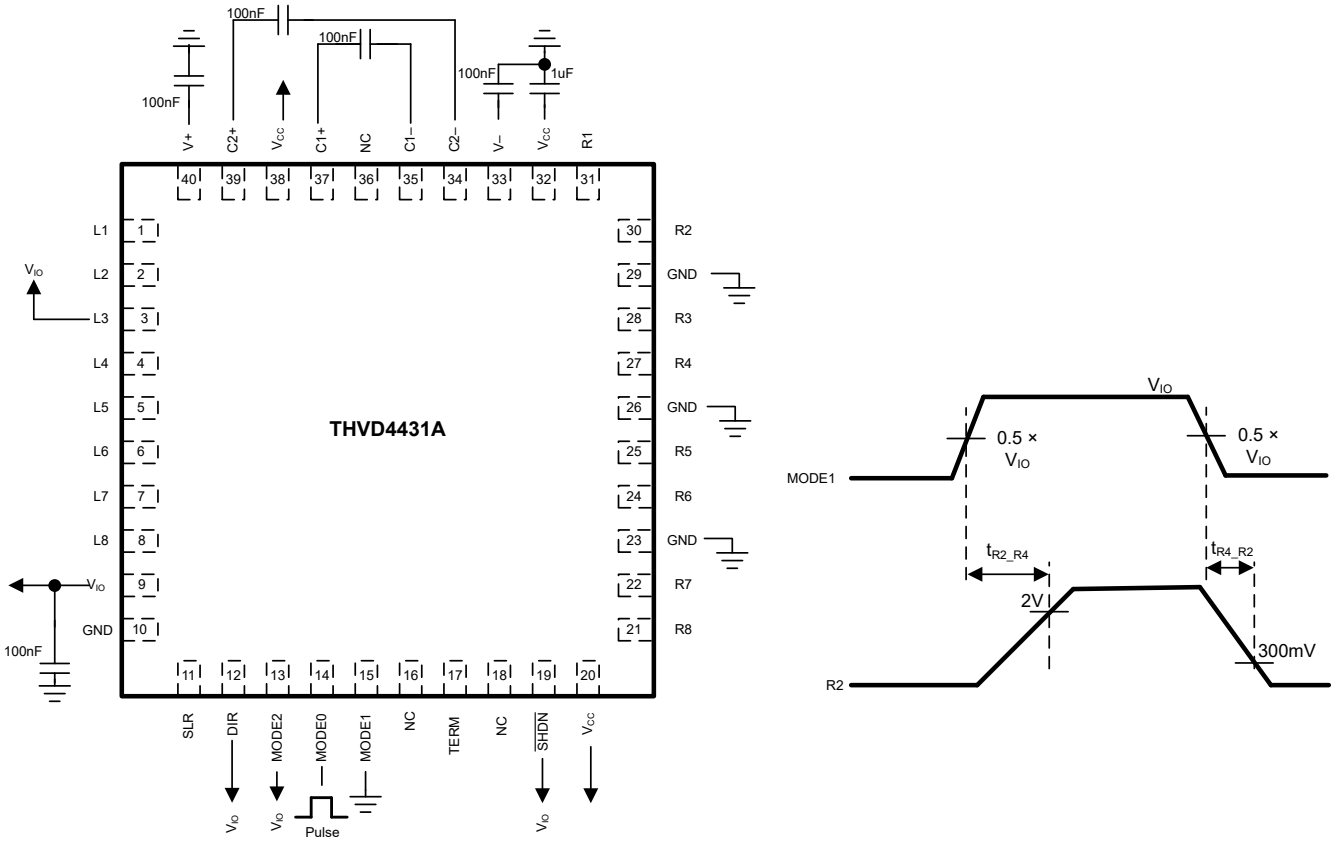


Figure 6-12. Time to Switch from RS-232 3T5R Mode to RS-485 Full Duplex Mode and Back

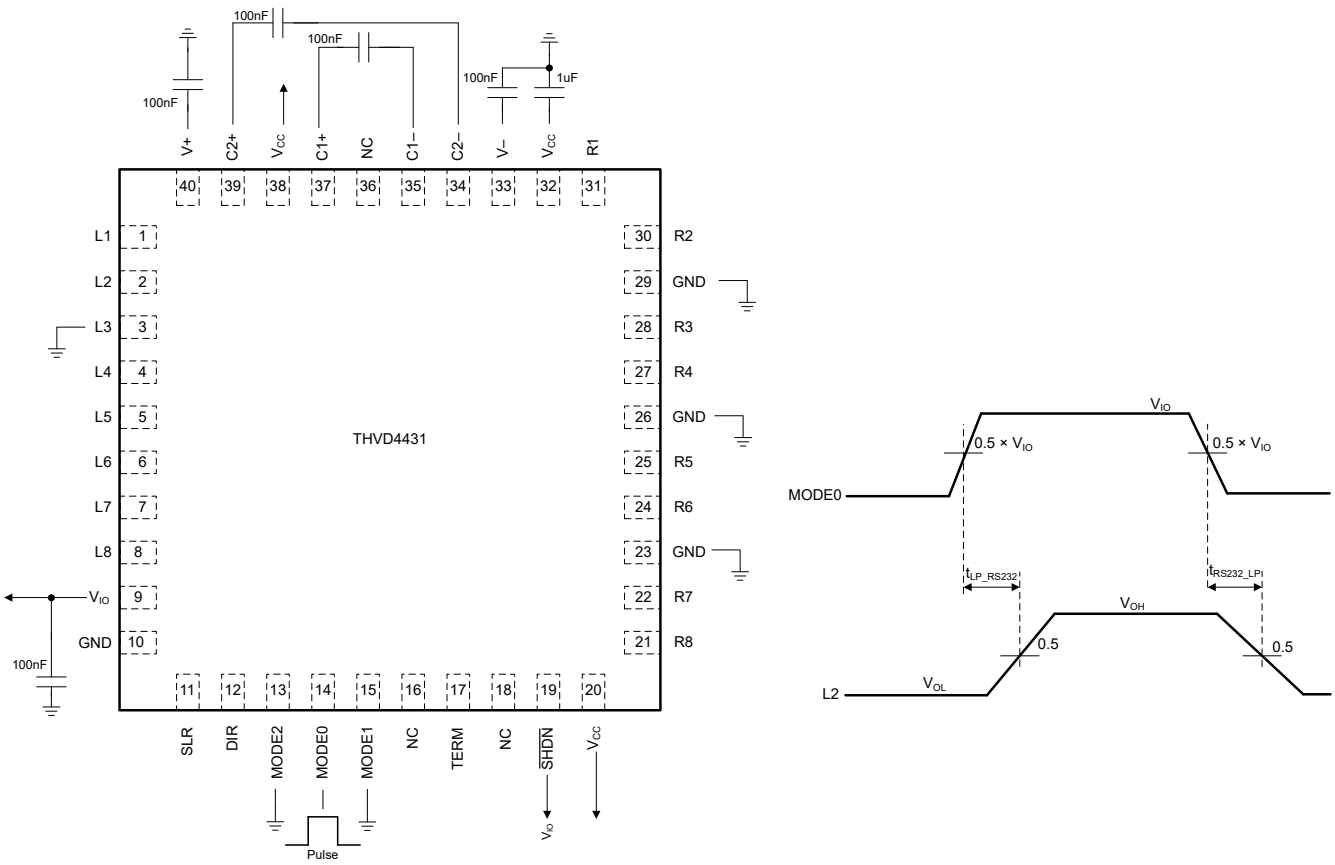


Figure 6-13. Time to Switch from RS-232 Loopback to Normal RS-232 3T5R Mode and Back

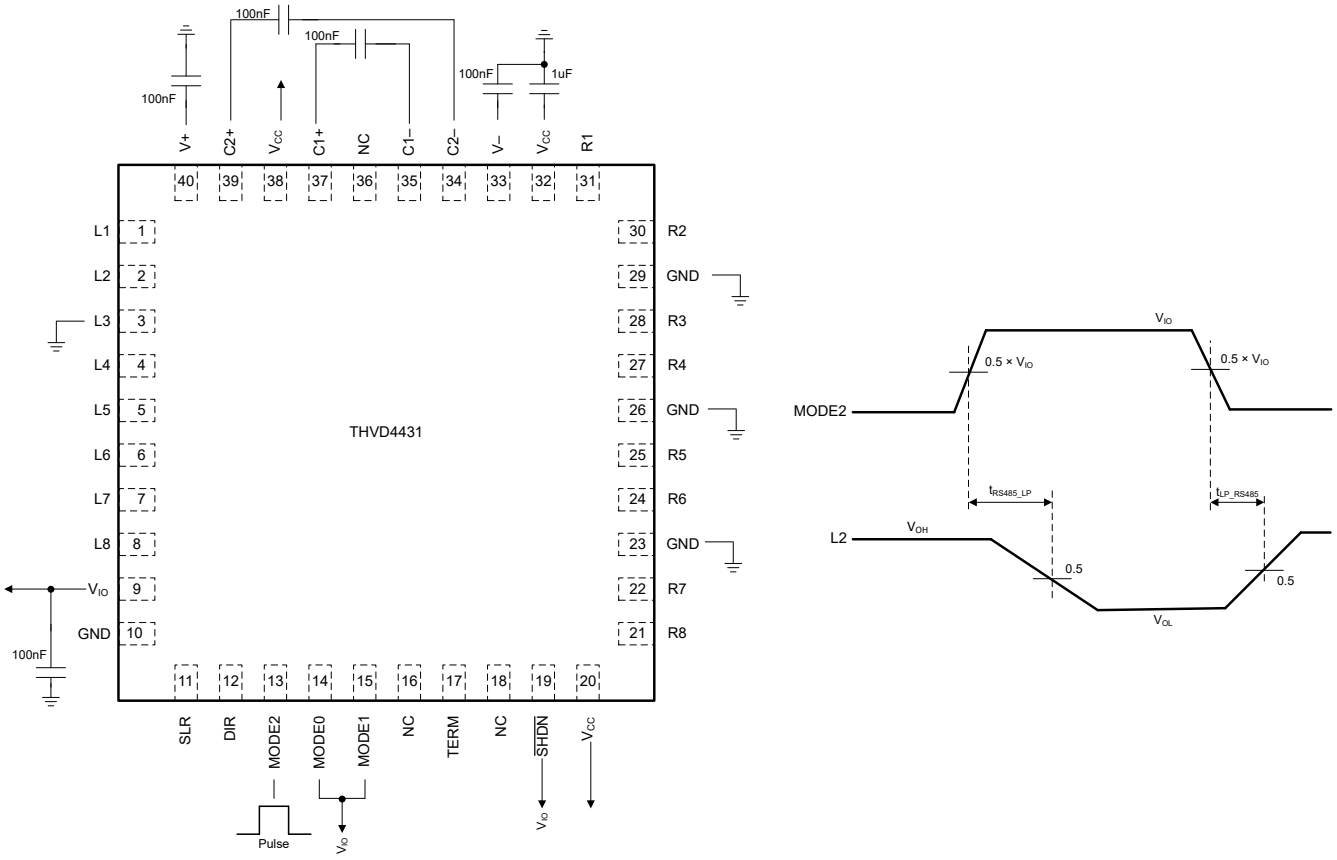


Figure 6-14. Time to Switch from RS-485 Loopback Mode to RS-485 Full Duplex Mode and Back

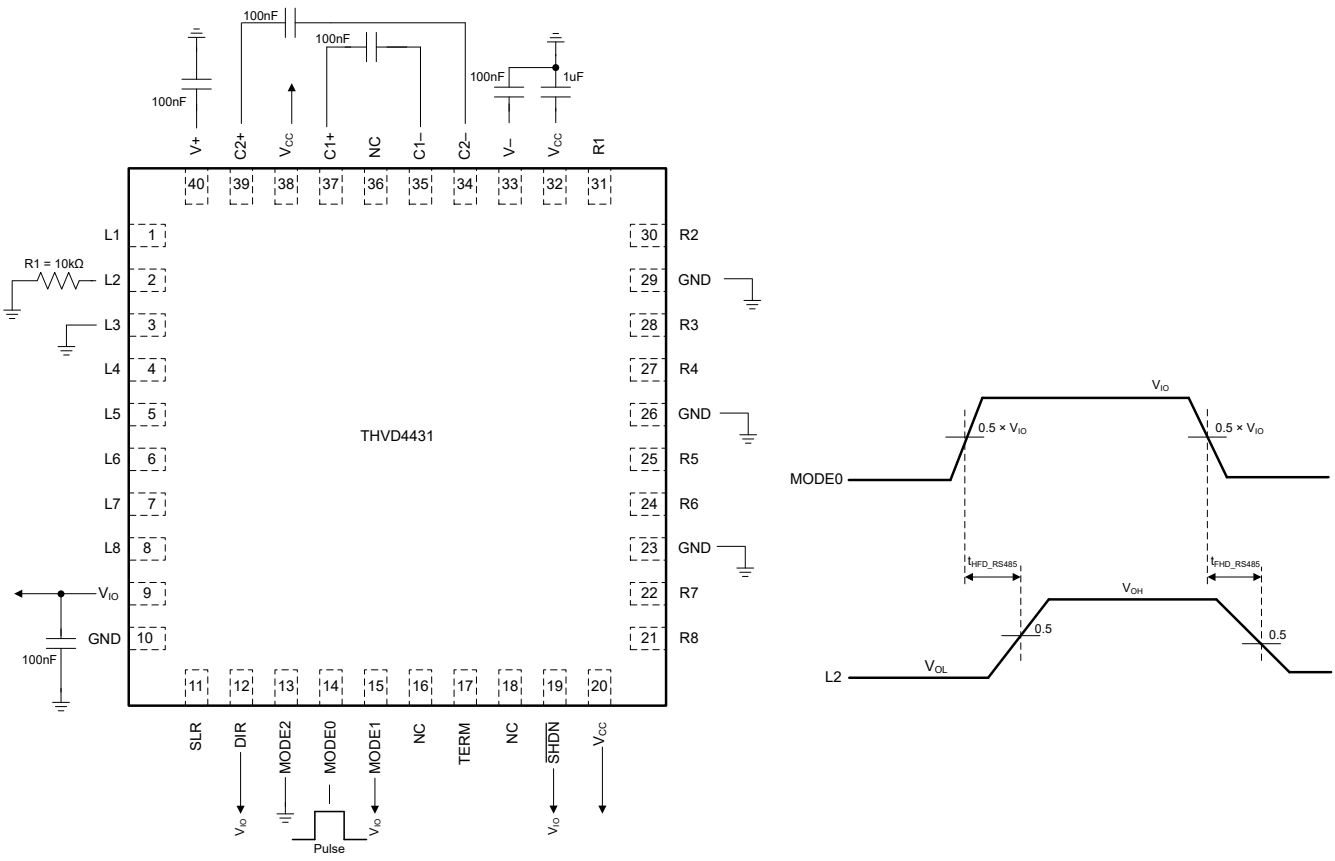
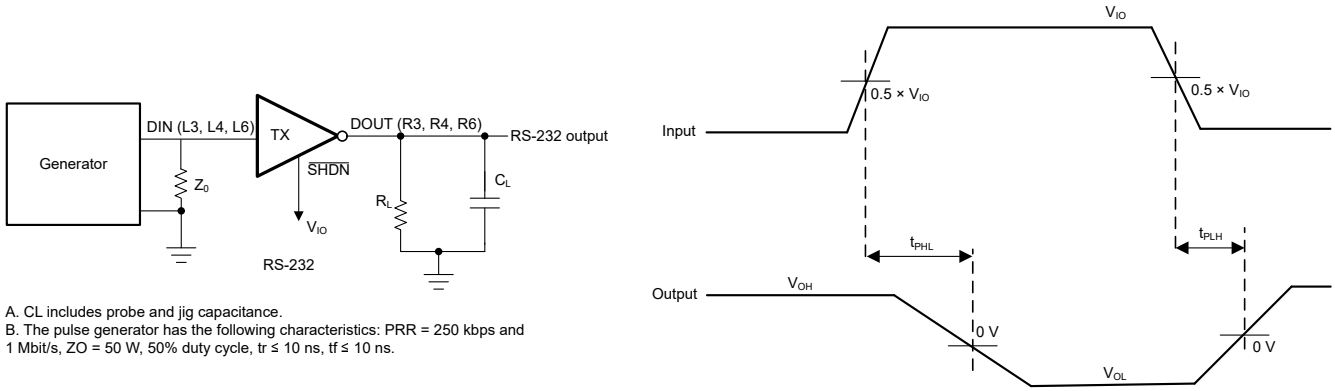
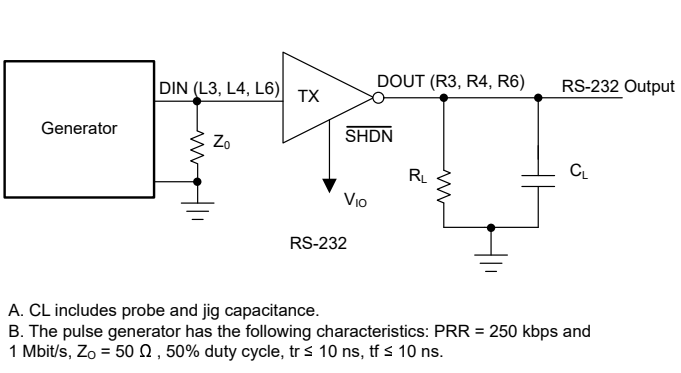


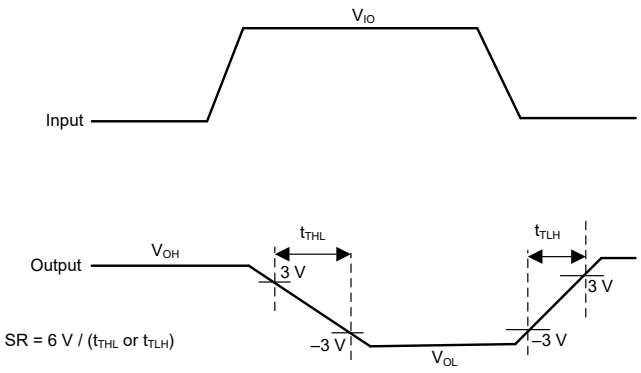
Figure 6-15. Time to Switch from RS-485 Full Duplex to Half Duplex and Back



A. CL includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbps and 1 Mbit/s, ZO = 50 W, 50% duty cycle, tr ≤ 10 ns, tf ≤ 10 ns.

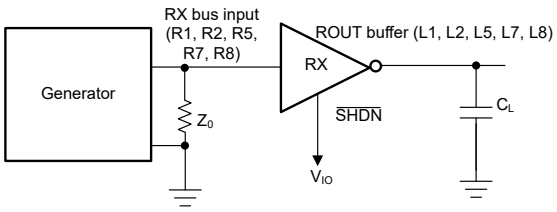
Figure 6-16. RS-232 Driver Prop Delay, Pulse Skew

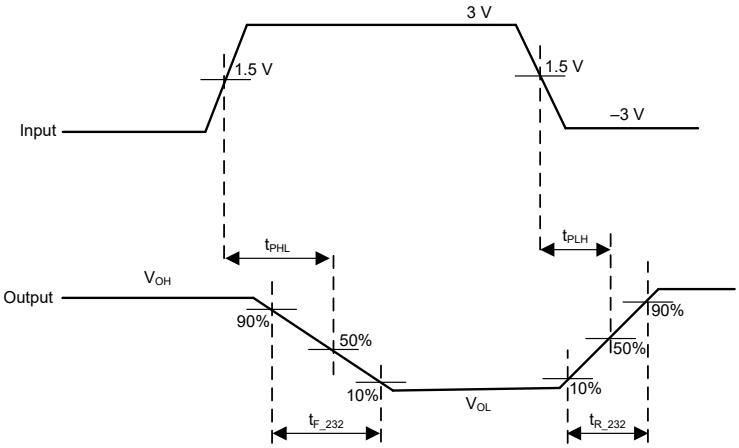




A. CL includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbps and 1 Mbit/s, Z_O = 50 Ω , 50% duty cycle, tr ≤ 10 ns, tf ≤ 10 ns.

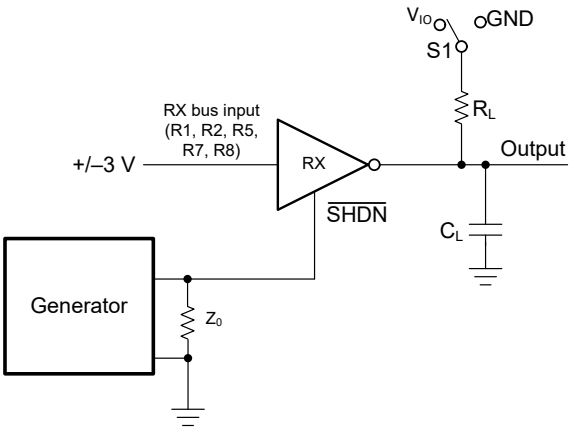
Figure 6-17. RS-232 Driver Slew Rate

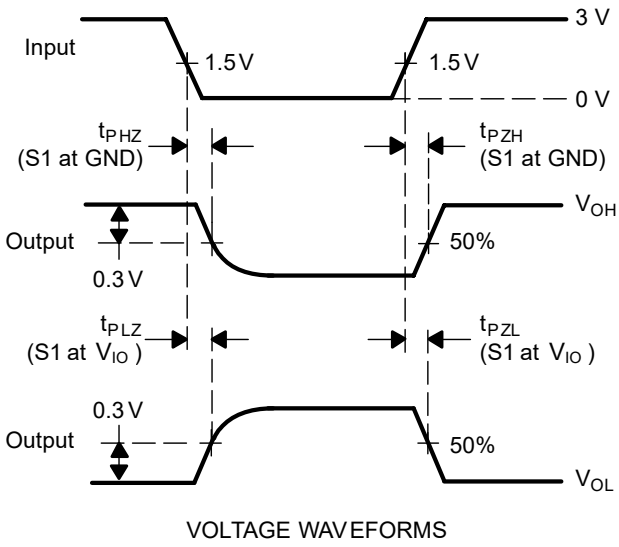




A. CL includes probe and jig capacitance.
B. The pulse generator has the following characteristics: ZO = 50 W, 50% duty cycle, tr ≤ 10 ns, tf ≤ 10 ns.

Figure 6-18. RS-232 Receiver Propagation Delay, Pulse Skew





VOLTAGE WAVEFORMS

A. CL includes probe and jig capacitance.
B. The pulse generator has the following characteristics: ZO = 50 Ω , 50% duty cycle, tr ≤ 10 ns, tf ≤ 10 ns.
C. t_{PLZ} and t_{PHZ} are same as t_{DIS}
D. t_{PZL} and t_{PZH} are same as t_{EN}

Figure 6-19. RS-232 Receiver Enable and Disable Time

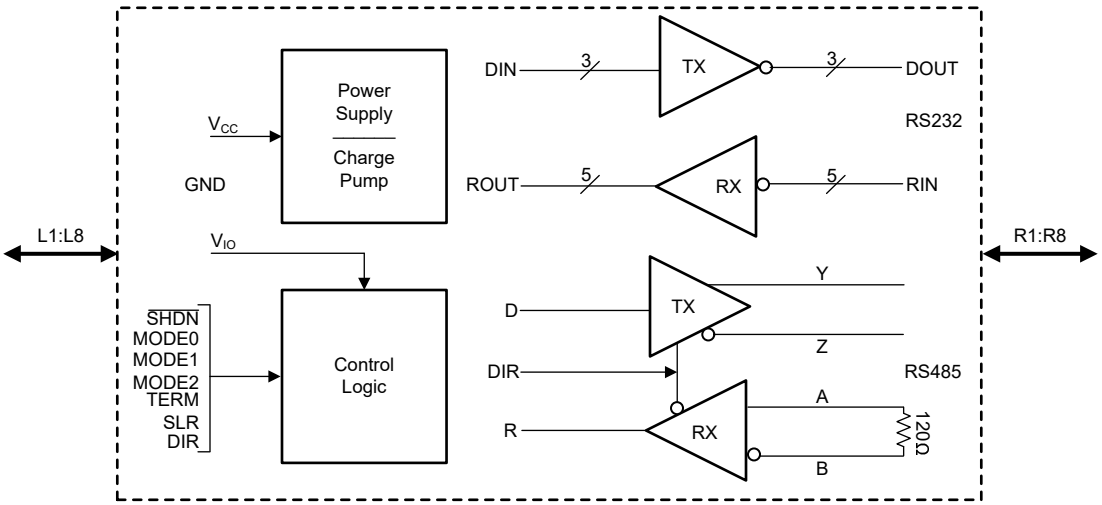
7 Detailed Description

7.1 Overview

THVD4431A is a highly integrated and robust multiprotocol transceiver supporting RS-232, RS-422 and RS-485 physical layers. The device has three transmitters and five receivers to enable 3T5R RS-232 port. Device also integrates one transmitter and one receiver to enable half and full duplex RS-485 port. MODE selection pins enable shared bus and logic pins for the protocols to share a common single connector.

The device has SLR pin which allows the device to be used for two different maximum speed settings for RS-232 and for RS-485. This is beneficial as customers can qualify one device and use the device in two separate end-applications. The devices also have flexible I/O supply pin V_{IO} which enables digital interface voltage range, from 1.65V to 5.5V, different from bus voltage supply 3V to 5.5V.

7.2 Functional Block Diagrams



7.3 Feature Description

7.3.1 Integrated IEC ESD and EFT Protection

Internal ESD protection circuits protect all the transceiver bus pins (driver and receiver) against electrostatic discharges (ESD) according to IEC 61000-4-2 up to ±8kV for contact discharge and ±15kV for air discharge for all operating modes. Bus lines in RS-485 mode can also withstand electrical fast transients (EFT) according to IEC 61000-4-4 for up to ±4kV.

7.3.2 Protection Features

The THVD4431A bus pins are protected against any DC supply shorts in the range of -16V to +16V. In the RS-485 mode, the short circuit current is limited to ±250mA to comply with the TIA/EIA-485A standard. In RS-232 mode, current limiting of ±60mA is applicable for scenarios where bus pins can short to ground.

The device also features thermal shutdown protection that disables the driver and the receiver if the junction temperature exceeds the T_{SHDN} threshold due to excessive power dissipation on-chip.

Supply undervoltage protection is present on both V_{CC} and V_{IO} supplies. This maintains the bus output and receiver logic output in known driven state when both the supplies are above the rising undervoltage thresholds. Table below describes the device behavior in various scenarios of supply levels.

Table 7-1. Supply Function Table

V_{CC}	V_{IO}	Driver Output	Receiver Output
> $UV_{VCC(rising)}$	> $UV_{VIO(rising)}$	For RS-485 mode, determined by DIR and L3 inputs. For RS-232 mode, determined by L3, L4, L6 inputs. For shutdown mode, Hi-Z	For RS-485 mode, determined by DIR and (R1R2) or (R3R4) inputs. For RS-232 mode, determined by R1, R2, R5, R7, R8 inputs. For shutdown mode, Hi-Z
< $UV_{VCC(falling)}$	> $UV_{VIO(rising)}$	High impedance	Undetermined
> $UV_{VCC(rising)}$	< $UV_{VIO(falling)}$	High impedance	High impedance
< $UV_{VCC(falling)}$	< $UV_{VIO(falling)}$	High impedance	High impedance

7.3.3 RS-485 Receiver Fail-Safe Operation

The RS-485 differential receiver of the THVD4431A is *failsafe* to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200mV, and must output a low when V_{ID} is more negative than –200mV. The receiver parameters which determine the failsafe performance are V_{TH+}, $V_{TH–}$, and V_{HYS} (the separation between V_{TH+} and $V_{TH–}$). As shown in the *Receiver Function table*, differential signals more negative than –200mV always causes a low receiver output, and differential signals more positive than 200mV always causes a high receiver output.

When the differential input signal is close to zero, the signal still above the V_{TH+} threshold, and the receiver output is high. Only when the differential input is more than V_{HYS} below V_{TH+} does the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value, V_{HYS}, as well as the value of V_{TH+}.

7.3.4 Low-Power Shutdown Mode

Driving the $\overline{SHDN}$ pin low puts the device into the shutdown mode. This is the lowest power mode of the device and current consumption is 10µA typical. All the blocks get disabled in this mode.

7.3.5 On-chip Switchable Termination Resistor

THVD4431A has a termination resistor of nominal 120Ω, across R3/R4 in RS-485 mode. Both termination resistors are enabled or disabled using pins as described in Table 7-2. This termination resistor can be enabled or disabled independent of the state of driver or receiver. Termination is OFF in RS-232 loopback, RS-232 3T5R, RS-485 loopback, unpowered and thermal shutdown modes.

Table 7-2. On-chip Termination Function

Signal state	Device mode	Function
TERM = V_{IO}	Half and full duplex mode	120Ω enabled between R3 and R4
TERM = GND or floating	Half and full duplex mode	120Ω disabled between R3 and R4

The on-chip 120Ω termination resistor is designed for minimum variation across temperature and across common mode voltage on bus pins. The termination block offers a resistive load to the bus, and does not alter the magnitude or phase of the bus signals from DC to 20Mbps signaling. See the typical characteristic curves for variation of termination resistor with voltage and temperature.

7.3.6 Operational Data Rate

THVD4431A can be used in slow speed or fast speed RS-485 and RS-232 applications by configuring Slew rate control (SLR) pin. Table 7-3 describes slew rate control function.

Table 7-3. Slew Rate Control Function

Signal state	Driver	Receiver	Comment
SLR = V_{IO}	Maximum speed of operation for RS-485 = 500kbps. Maximum speed of operation in RS-232 mode is 250kbps	Maximum speed of operation for RS-485 = 500kbps. Maximum speed of operation in RS-232 mode is 250kbps	Active high slew rate limiting applied on driver output. In this configuration, glitch filter in receiver path for RS-485 is enabled
SLR = GND or floating	Maximum speed of operation for RS-485= 20Mbps. Maximum speed of operation in RS-232 mode is 1Mbps	Maximum speed of operation for RS-485 = 20Mbps. Maximum speed of operation in RS-232 mode is 1Mbps	Slew rate limiting on driver output disabled.

For RS-485 half and full duplex modes, receiver path in the slow speed mode (500kbps) provides additional noise filtering. To attenuate high frequency noise pulses from the bus which can be wrongly interpreted as valid data, SLR = V_{IO} enables a low pass filter to filter out pulses with frequency higher than typical 700kHz.

7.3.7 Diagnostic Loopback

THVD4431A provides complete path diagnostic loopback modes for both RS-232 and RS-485. These modes internally short bus outputs to bus inputs. So, if data is toggled from logic input, data reaches bus and is reflected back on logic buffer output. This enables MCU to detect bus side short (due to connector/cable) by comparing logic input and logic output.

In RS-232 hardware loopback mode, L3 reflects on R3/R2/L2; L4 reflects on R4/R5/R8/R1/L5/L8/L1; L6 reflects on R6/R7/L7 enabling to detect short to ground on all bus pins from R1 through R8. RS-232 loopback mode is optimized for -40°C to 85°C ambient temperature. RS-232 diagnostic loopback can be performed on a node (DUT1) even with another node (DUT2) connected via cable, but listening node (DUT2) is not allowed to transmit anything on the RS232 lines while loopback check by DUT1 is ongoing.

In RS-485 loopback mode, internally R2 gets connected to R3 and R1 gets connected to R4. L3 input data is routed to driver output terminals and receiver input terminals and reflects on L2. DIR and TERM are not supported in this mode. Specific to this mode, external termination on R3/R4 is not supported, but R1/R2 can have internal or external termination. This is able to detect short between R1/R2 and between R3/R4 bus terminals. Recommended maximum data rate for RS-485 diagnostic loopback to detect cable or connector shorts is 500kbps with SLR = V_{IO}.

7.3.8 Integrated Charge pump for RS-232

THVD4431A has integrated high-efficiency and low-noise charge pump to generate large output voltages for RS-232 signals. Charge pump consists of a voltage doubler and an inverter to regulate the voltage to nominal ± 5.5V or to ±9.5V for 3.3V or 5V V_{CC} operation respectively. This also includes UV protection mechanism. Charge pump needs four external ceramic capacitors (2 flying capacitors and 2 storage capacitors) and allows for single supply operation for RS-232. For a generic description of RS-232 charge pump operation, please refer to the blog: How the RS-232 transceiver's regulated charge-pump circuitry works.

7.4 Device Functional Modes

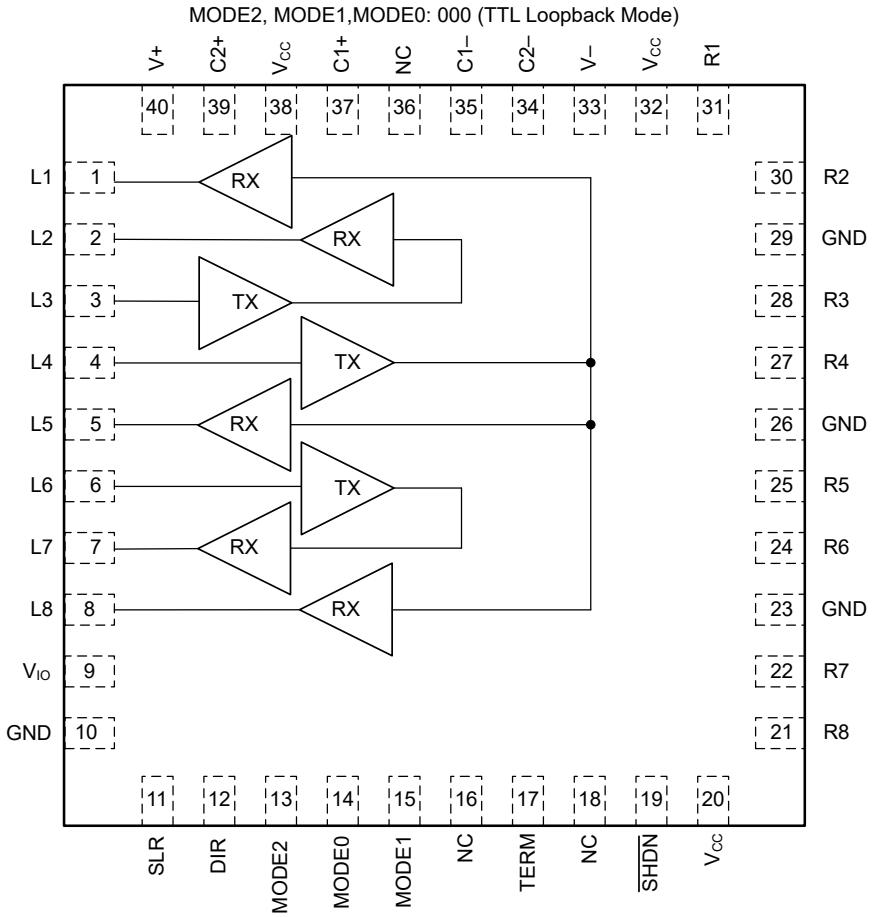
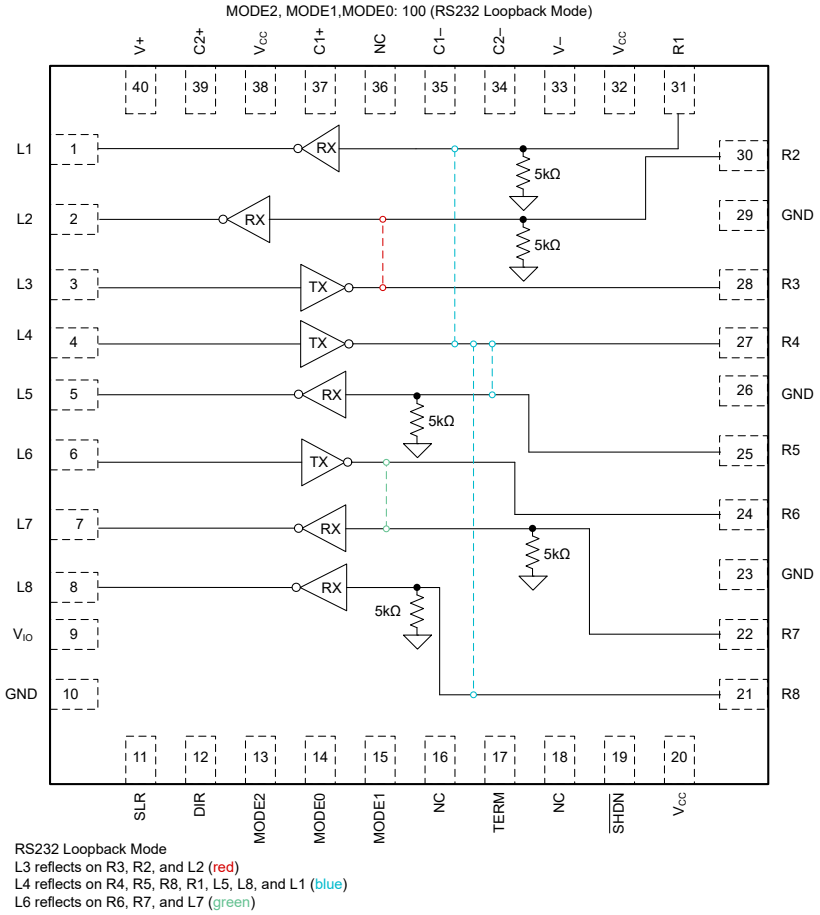


Figure 7-1. TTL Loopback Mode



RS232 Loopback Mode
L3 reflects on R3, R2, and L2 (red)
L4 reflects on R4, R5, R8, R1, L5, L8, and L1 (blue)
L6 reflects on R6, R7, and L7 (green)

Figure 7-2. RS-232 Loopback Mode

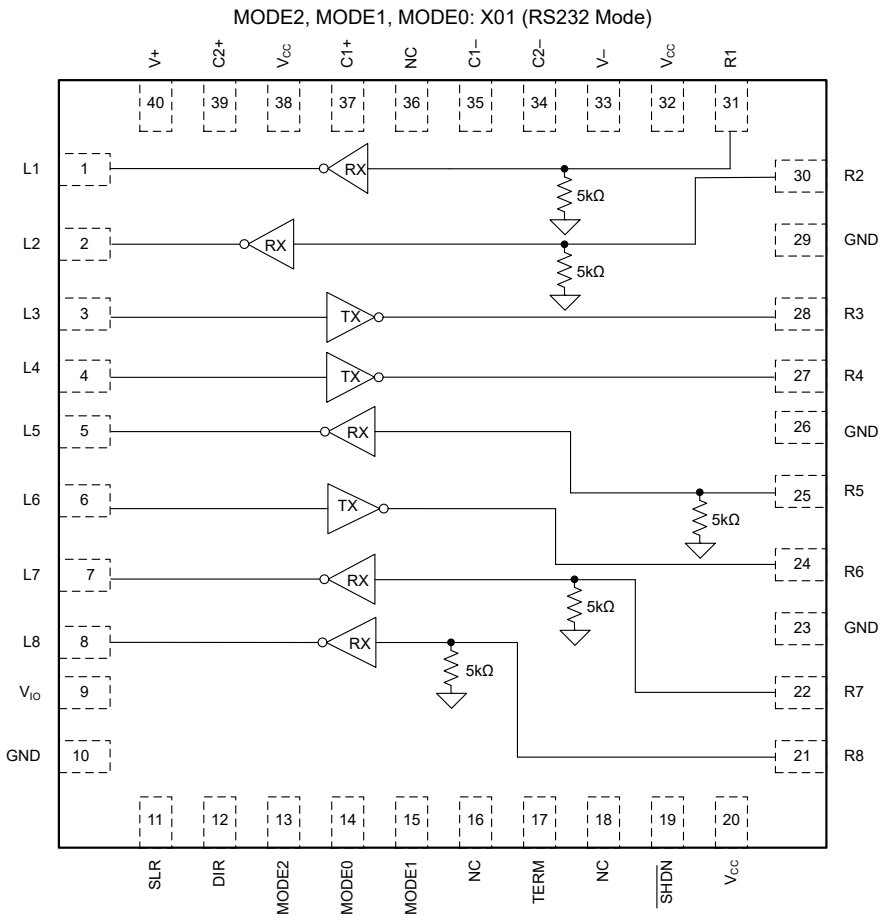


Figure 7-3. RS-232 3T5R Mode

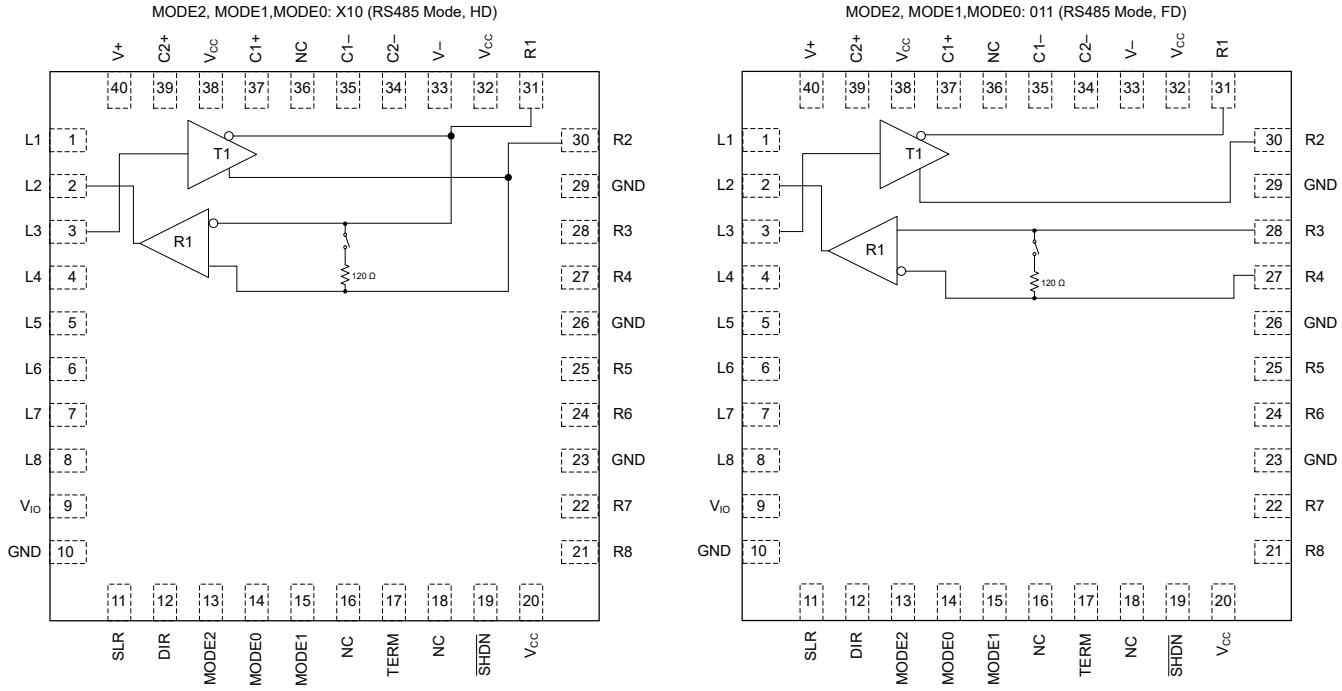


Figure 7-4. RS485 Half duplex and Full duplex mode

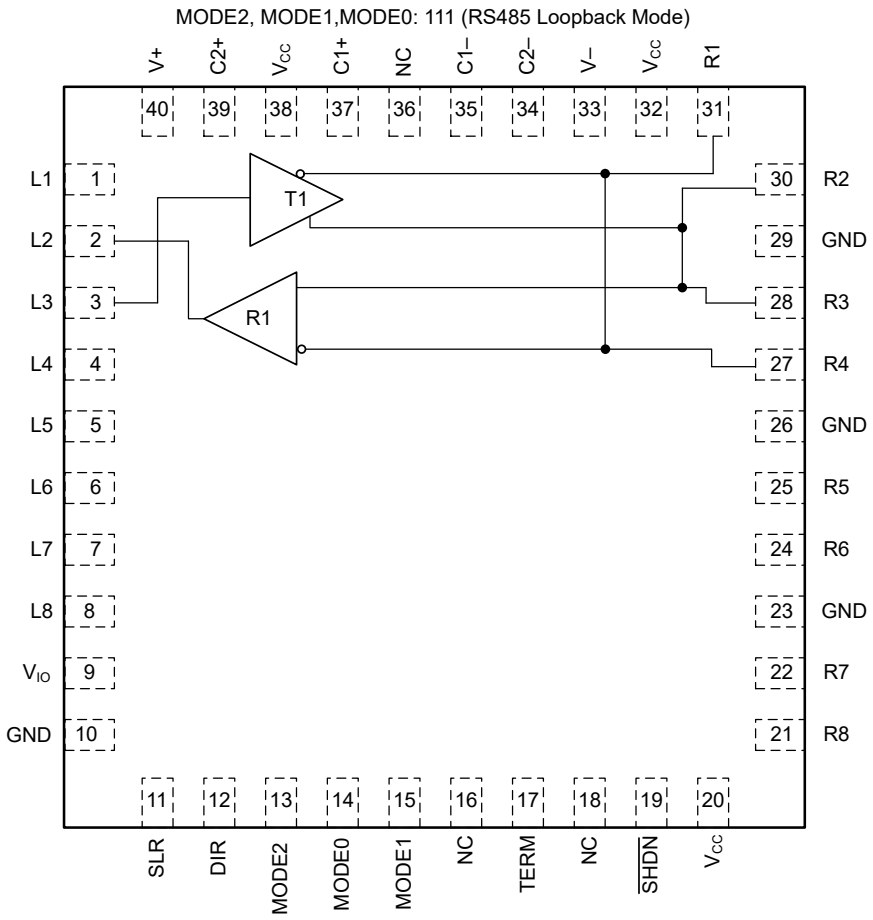


Figure 7-5. RS-485 Loopback Mode

7.4.1 RS-485 Functionality

When the driver enable pin, DIR, is logic high, the differential outputs R2 and R1 follow the logic states at data input L3. A logic high at L3 causes R2 to turn high and R1 to turn low. In this case, the differential output voltage defined as $V_{OD} = V_{R2} – V_{R1}$ is positive. When L3 is low, the output states reverse: R1 turns high, R2 becomes low, and V_{OD} is negative.

When DIR is low, both outputs turn high-impedance. In this condition, the logic state at L3 is irrelevant. The DIR pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The L3 pin has an internal pull-up resistor to V_{IO}, thus, when left open while the driver is enabled, output R2 turns high and R1 turns low.

Table 7-4 is valid for both half duplex and full duplex modes, and is independent of state of TERM and SLR pins.

Table 7-4. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
L3	DIR	R2	R1	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	High impedance	High impedance	Driver disabled
X	OPEN	High impedance	High impedance	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

In full duplex mode, if $\overline{SHDN}$ is high, receiver is always enabled. In half duplex mode, receiver is enabled if DIR = Low/floating and disabled if DIR = V_{IO}. When the differential input voltage defined as $V_{ID} = V_{R2} – V_{R1}$ or $V_{R3} – V_{R4}$ is higher than the positive input threshold, V_{TH+}, the receiver output, L2, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-}, the receiver output, L2, turns low. If V_{ID} is between V_{TH+} and V_{TH-} the output is indeterminate.

Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

In half duplex mode, when DIR is high, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. The receiver output includes a pull-up resistor with nominal value 1.2MΩ to bias the pin to logic high. In the scenario that leakage or another current sink is present on the receiver output node, this current can cause a voltage drop on the node that incorrectly resolves to a logic low, and the connected MCU or processor can incorrectly interpret this logic low as a start bit. An external pull-up can be connected to this node to ensure the correct logic state in the event of an external current sink. The value of this resistor depends on the current sink value, but TI recommends a value between 1kΩ and 10kΩ.

Table 7-5 is valid irrespective of state of the TERM and SLR pins. Other logic outputs L1, L5, L7 and L8 remain high in RS-485 mode.

Table 7-5. Receiver Function Table

DIFFERENTIAL INPUT	OUTPUT	FUNCTION
$V_{ID} = V_{R2} – V_{R1}$(Half duplex mode) or $V_{R3} – V_{R4}$(Full duplex mode)	L2	
$V_{TH+} < V_{ID}$	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	Receive valid bus low
X	High impedance for DIR = V_{IO} in Half duplex mode	Receiver disabled in half duplex mode for DIR = V_{IO}
Open-circuit bus	H	Fail-safe high output

Table 7-5. Receiver Function Table (continued)

DIFFERENTIAL INPUT	OUTPUT	FUNCTION
$V_{ID} = V_{R2} – V_{R1}$(Half duplex mode) or $V_{R3} – V_{R4}$(Full duplex mode)	L2	
Short-circuit bus	H	Fail-safe high output
Idle (terminated) bus	H	Fail-safe high output

7.4.2 RS-232 Functionality

In RS-232 mode, only way to disable driver is to go in shutdown mode by pulling $\overline{SHDN}$ pin low. A logic high at inputs for driver L3, L4 and L6 causes driver outputs R3, R4 and R6 to be driven low towards negative charge pump output V-. A logic low at inputs for driver L3, L4 and L6 causes driver outputs R3, R4 and R6 to be driven high towards positive charge pump output V+. If logic inputs are left floating due to the pull-up resistors on driver logic inputs, the driver outputs are driven low towards V-.

Table 7-6 is valid irrespective of the state of SLR pin.

Table 7-6. Driver Function Table

INPUT	ENABLE	OUTPUTS	FUNCTION
L3, L4, L6	$\overline{SHDN}$	R3, R4, R6	
H	H	Low (driven towards V-)	Normal operation with inverting logic
L	H	H (Driven towards V+)	Normal operation with inverting logic
X	L	High impedance	TX and RX are disabled in shutdown mode
Open	H	Low (driven towards V-)	Since pull-up on logic input pin, output driven low by default

For the RS-232 receiver, if the receiver bus inputs are above rising threshold V_{IT+}, corresponding received logic output goes low. Also, if the receiver bus inputs are below falling threshold V_{IT-}, corresponding received logic output goes high.

Table 7-7 is valid irrespective of the state of SLR pin.

Table 7-7. Receiver Function Table

RS-232 BUS INPUT	LOGIC OUTPUT	FUNCTION
V_{IRx} (voltage on R1, R2, R5, R7 or R8)	L1, L2, L5, L7, L8	
$V_{IT+} < V_{IRx}$	L	Normal operation with inverting logic
$V_{IT-} < V_{IRx} < V_{IT+}$	?	Indeterminate bus state
$V_{IRx} < V_{IT-}$	H	Normal operation with inverting logic
X	High impedance for $\overline{SHDN}$ = GND	Receiver disabled in shutdown mode
Open-circuit bus	H	Fail-safe high output

7.4.3 Mode Control

Table 7-8. MODE Control Function Table

MODE2	MODE1	MODE0	Operating mode	Function
Logic low or float	Logic low	Logic low	TTL loopback	L4 reflects on L1/L5/L8; L3 reflects on L2; L6 reflects on L7
X	Logic low	Logic high	RS-232 3T5R mode, charge pump is ON, V+/V- are regulated	3T5R mode; L3, L4, L6 are Logic inputs for RS232 driver; L1, L2, L5, L7, L8 are Logic outputs
X	Logic high	Logic low	RS-485 half duplex mode (charge pump is off)	L2 is RX Logic output; L3 is Driver Logic input; R1R2 are Bus inverting and non-inverting terminals respectively
Logic low or float	Logic high	Logic high	RS-485 full duplex mode (charge pump is off)	R1R2 are inverting and non-inverting driver terminals; R3R4 are non-inverting and inverting receiver terminals.
Logic high	Logic high	Logic high	RS-485 loopback mode (charge pump is off)	R1, R2, R3, R4 continue to be bus terminals and reflect data on L3; DIR is don't care in this mode; TERM not supported. External termination on R3/R4 not supported. R1/R2 can have internal or external termination.
Logic high	Logic low	Logic low	RS-232 loopback, charge pump is ON, V+/V- are regulated	L3 reflects on R3/R2/L2 L4 reflects on R4/R5/R8/R1/L5/L8/L1 L6 reflects on R6/R7/L7

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

THVD4431A is a highly integrated multiprotocol transceiver supporting RS-232, RS-422 and RS-485 physical layer and is used for asynchronous data transmissions. MODE pins allow for the configuration of different operating modes. Device allows point-to-point RS-232 communication port and multipoint RS-485 communication port over common connector. The device also features integrated 120Ω switchable termination resistor on RS-485 bus lines which enables same device to be used for middle nodes or end nodes in an RS-485 network. When the device is configured in RS-232 mode, RS-485 circuits and 120Ω termination are disabled and do not interfere in RS-232 communication. For RS-232 communication, charge pump and 5kΩ resistor to ground on receiver bus pins is integrated in the device. This 5kΩ resistor and charge pump is automatically disabled in RS-485 mode. Slew rate limiting pin is provided so that same device can be used in slow speed or fast speed RS-485 and RS-232 applications. When ultra low power consumption is needed, device can be put in shutdown mode using $\overline{\text{SHDN}}$ pin. All these features make the device completely flexible and designed for various application needs. Integration of termination resistor saves significant PCB area compared to discrete implementation.

8.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

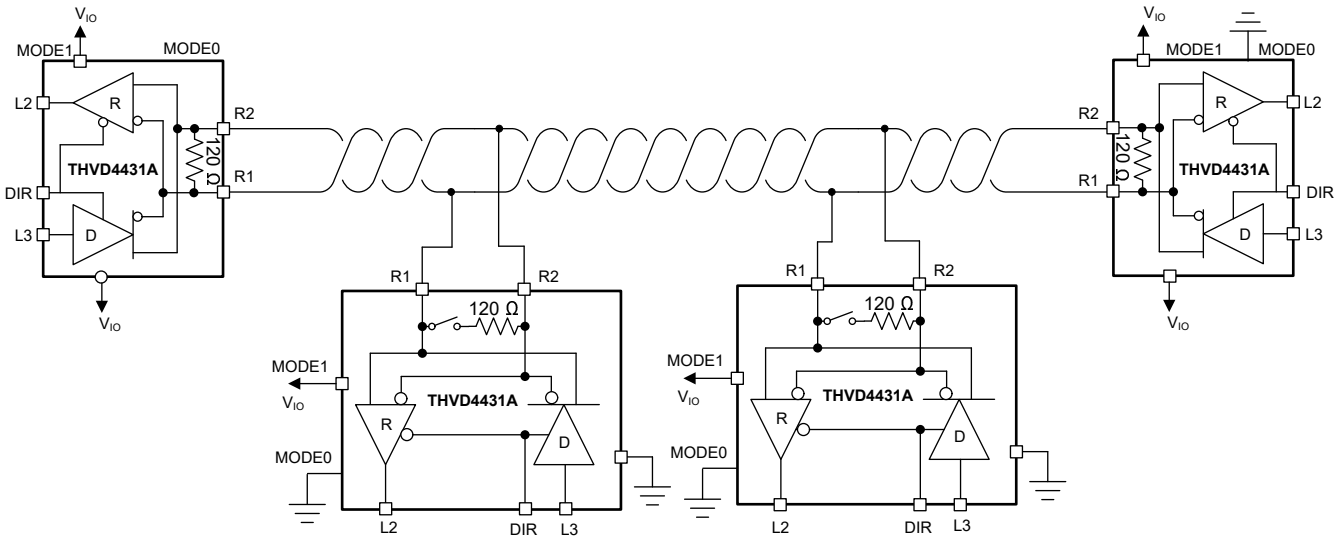


Figure 8-1. Typical RS-485 Network With Half-Duplex Transceivers

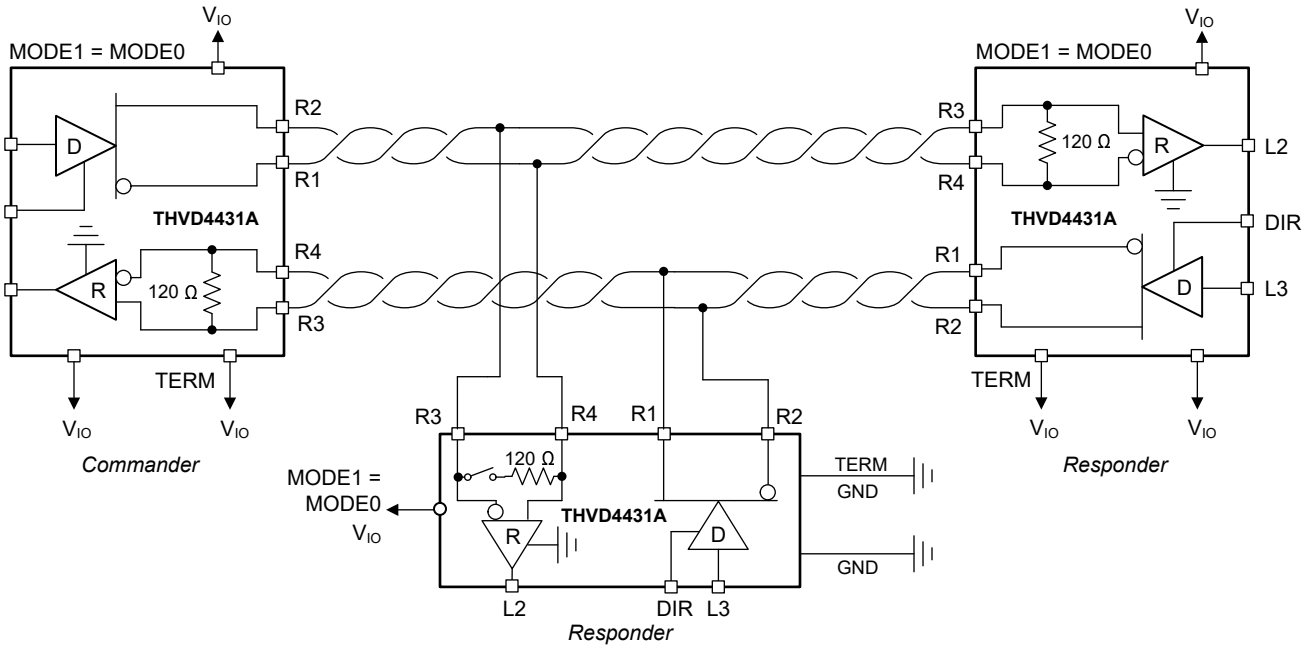


Figure 8-2. Typical RS-485 Network With Full-Duplex Transceivers

THVD4431A can be used in both networks (half and full duplex) and at all nodes (end node or middle nodes) since device has the configurability based on MODE2, MODE1, MODE0, and TERM pins.

THVD4431A also consists of three line drivers, five line receivers and dual charge pump circuit to enable RS-232 point-to-point serial communication. Full duplex transmission with hardware flow control is feasible with this device. This device provides the electrical interface between an asynchronous communication controller and the serial-port connector.

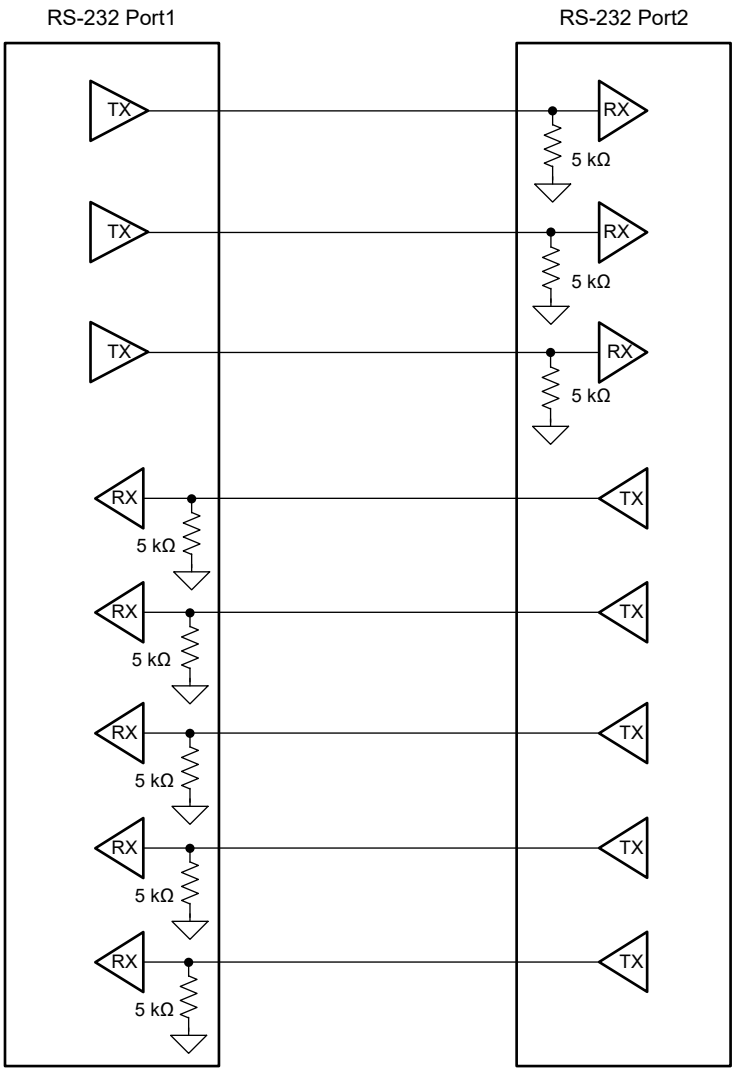


Figure 8-3. RS-232 serial communication

8.2.1 Design Requirements

RS-485 is a robust electrical standard that is applicable for long-distance networking that can be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes. RS-232 is more applicable for debug or configuration point to point applications.

8.2.1.1 Data Rate and Bus Length for RS-485

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the short the cable length. Conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10kbps and 100kbps, some applications require data rates up to 250kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

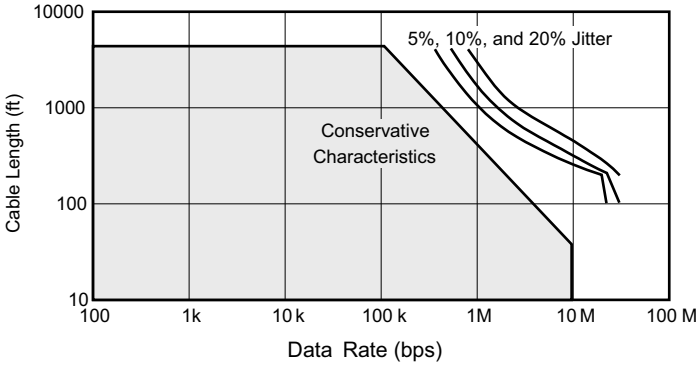


Figure 8-4. Cable Length vs Data Rate Characteristic

8.2.1.2 Stub Length for RS-485 Network

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, must be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections of varying phase as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub must be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8m/s)
- v is the signal velocity of the cable or trace as a factor of c

8.2.1.3 Bus Loading for RS-485 Network

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12kΩ. Because the THVD4431A in RS-485 half and full duplex mode consists of 1/8 UL transceivers which represents load resistance of approximately 96kΩ, connecting up to 256 receivers to the bus is possible for a limited common mode range of - 7V to 12V.

8.2.2 Detailed Design Procedure

Figure 8-5 suggests an application schematic for THVD4431A. The device has all logic pins on one side and bus side pins on other side to enable a flow-through layout in end application.

All V_{CC} power pins must have 1µF decoupling capacitor close to the respective device pins. RS-232 charge pump is designed such that 100nF charge pump capacitors work for both 3.3V and 5V operating V_{CC} supply.

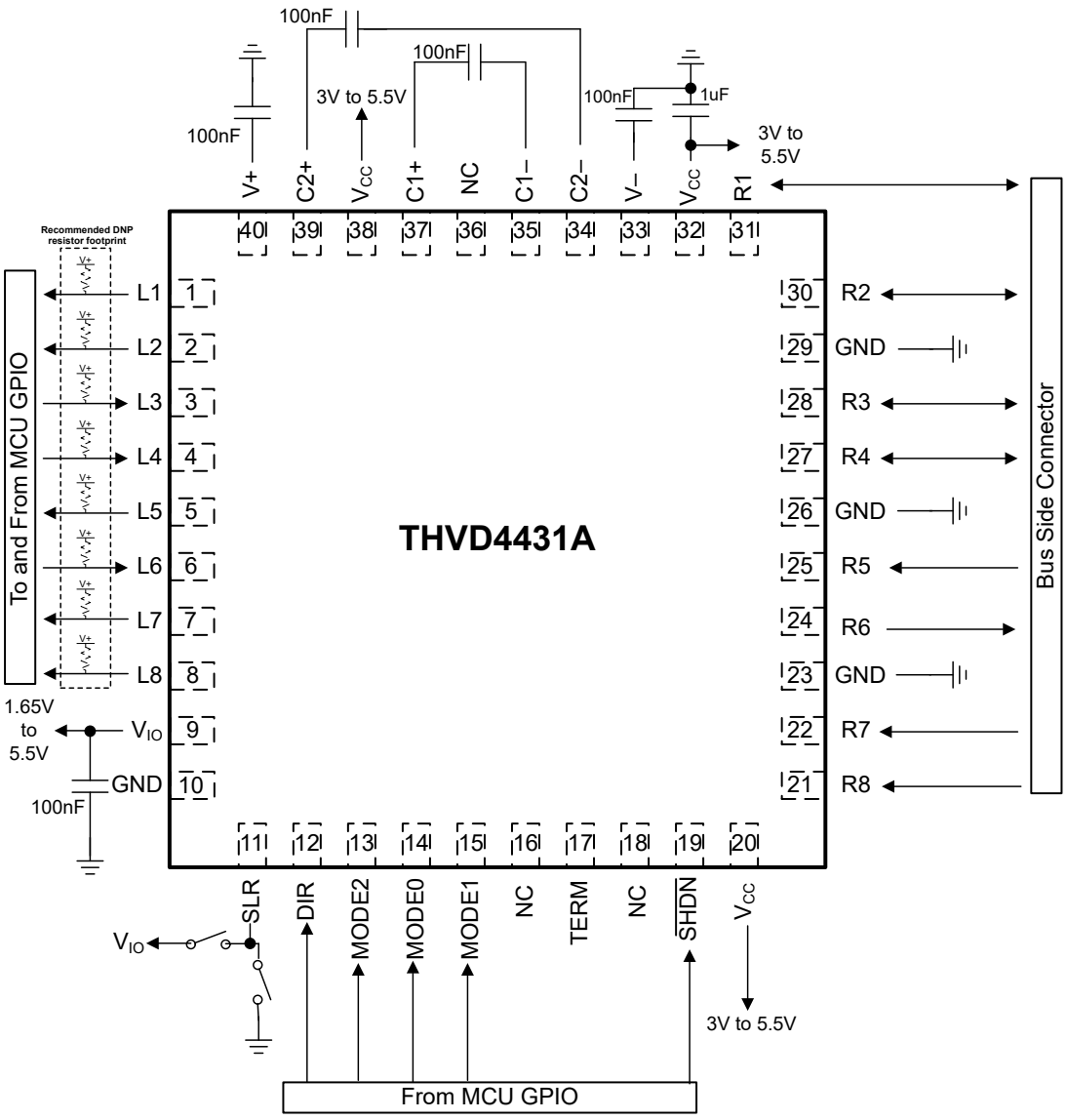
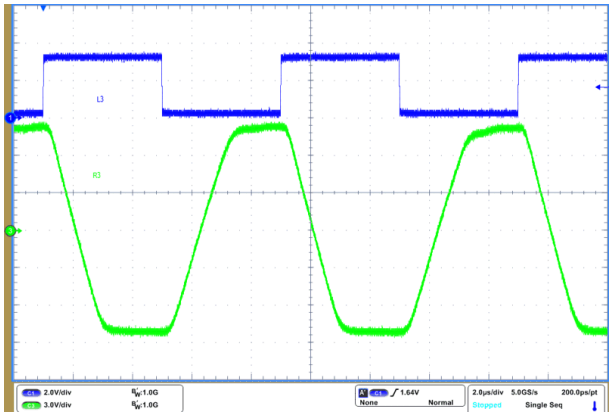


Figure 8-5. Typical Application Diagram for THVD4431A

8.2.2.1 External Pull-up Resistors

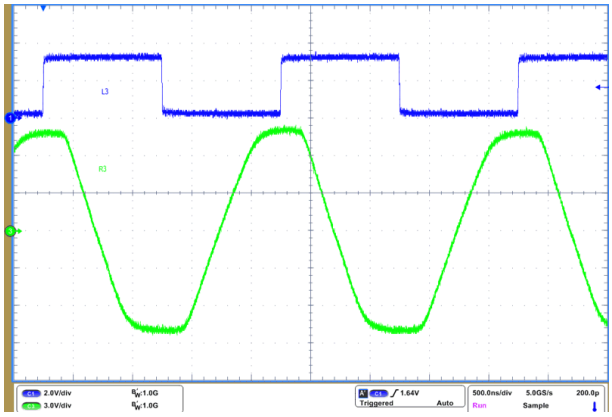
Pins L1 through L8 include a 1.2MΩ nominal pull-up resistor to bias the pin logic high when not being driven. If an external source such as a leakage path, conducted noise, or other current sink path occurs on these pins, the current can generate a large enough voltage drop across the pull-up resistor that the node is pulled to logic low. An external pull-up resistor can alleviate this issue by providing enough current to supply this sink while maintaining a logic high on the node. The value of this resistor depends on the current source, but generally, a resistor value in the range of 1kΩ to 10kΩ will provide sufficient margin. Designers are recommended to include an unpopulated resistor footprint on these pins in the case they are needed, and these resistors can remain unpopulated in the case that they are unneeded.

8.2.3 Application Curves



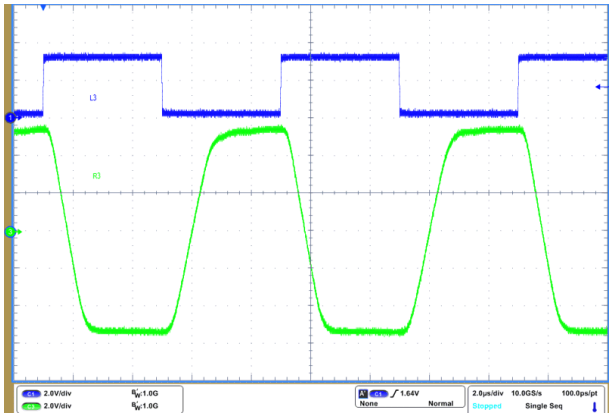
V_{CC} = 5V Bus Load = 5kΩ||2.5nF
250kbps SLR = V_{IO}

Figure 8-6. RS-232 Driver Waveform at 250kbps and V_{CC} = 5V



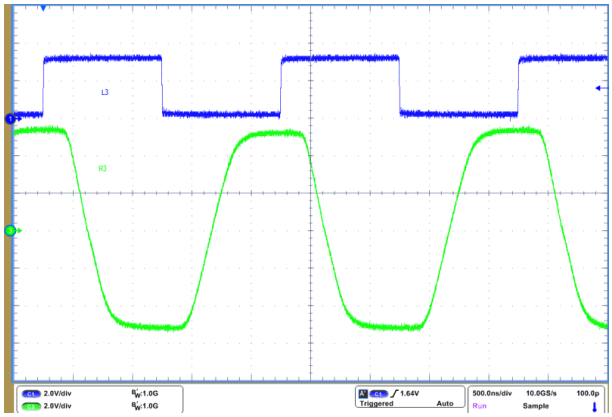
V_{CC} = 5V Bus Load = 5kΩ||1nF
1Mbps SLR = GND

Figure 8-7. RS-232 Driver Waveform at 1Mbps and V_{CC} = 5V



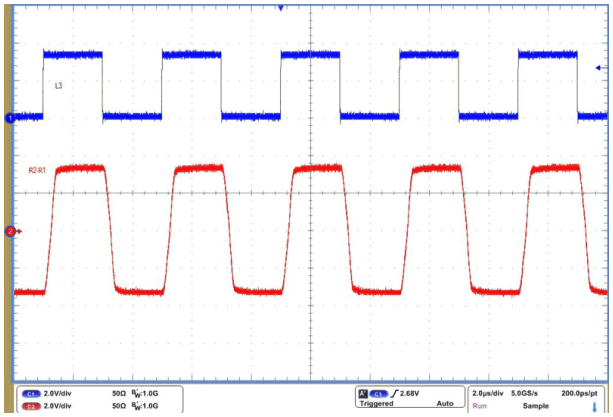
V_{CC} = 3.3V Bus Load = 5kΩ||2.5nF
250kbps SLR = V_{IO}

Figure 8-8. RS-232 Driver Waveform at 250kbps and V_{CC} = 3.3V



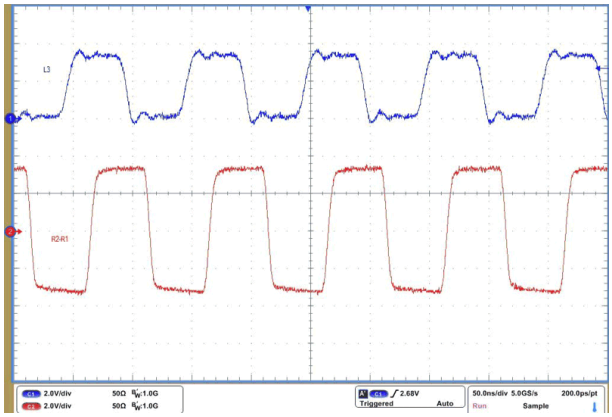
V_{CC} = 3.3V R_L = 5kΩ||1nF
1kbps SLR = GND

Figure 8-9. RS-232 Driver Waveform at 1Mbps and V_{CC} = 3.3V



V_{CC} = 5V Bus Load = 54Ω||50pF
SLR = V_{IO} Square wave at 500kbps

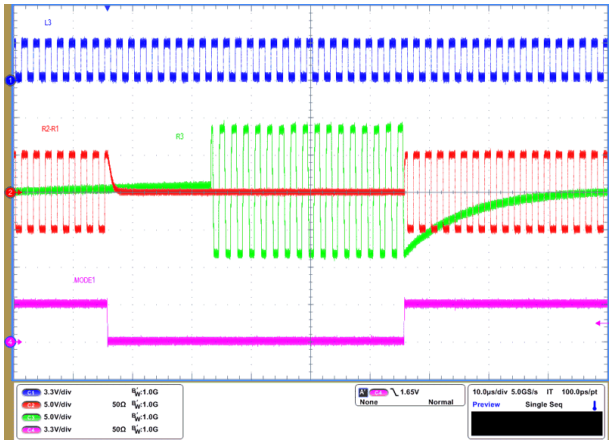
Figure 8-10. RS-485 Driver Waveform at 500kbps and V_{CC} = 5V



V_{CC} = 5V Bus Load = 54Ω||50pF
SLR = GND Square wave at 20kbps

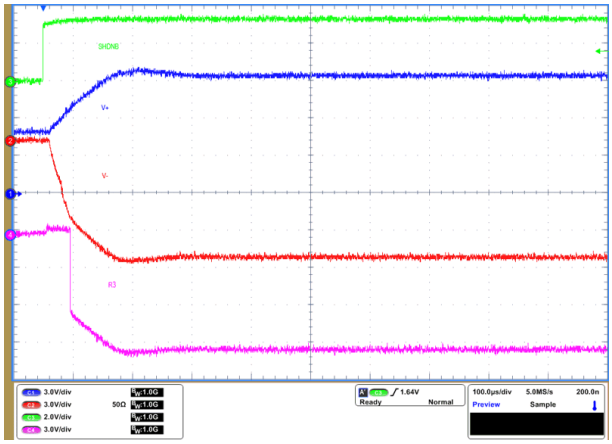
Figure 8-11. RS-485 Driver Waveform at 20Mbps and V_{CC} = 5V

8.2.3 Application Curves (continued)



V_{CC} = 5V L3 = 1Mbps square wave
SLR = GND MODE1 toggled at 10khz

Figure 8-12. RS-232 to RS-485 Mode Switching Waveform



V_{CC} = 5V L3 = GND
SHDN toggled

Figure 8-13. Mode Switching Waveform From Shutdown to RS-232 Mode

8.3 Power Supply Recommendations

For reliable operation at all data rates and supply voltages, each supply must be decoupled with a ceramic capacitor located as close to the supply pins as possible. Recommended bypass capacitor for V_{CC} is 1µF, for V_{IO} is 100nF, for V+, V- charge pump voltage supplies is 100nF. Besides this, two charge pump flying capacitors of 100nF each are needed between C1+, C1- terminals and between C2+, C2- terminals. For V_{CC} = 3.3V ±10%, V+ and V- voltages are regulated to +5.5V and -5.5V typically. If an application needs larger RS-232 output voltages, V_{CC} = 5V ± 10% is recommended because V+ and V- are regulated to ±9.5V.

8.4 Layout

8.4.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices to protect against surge transients that can occur in industrial environments. THVD4431A has integrated IEC ESD and EFT protection. So if the application does not need IEC Surge protection, external transient protection is not always needed. Since these transients have a wide frequency bandwidth (from approximately 3MHz to 300MHz), high-frequency layout techniques must be applied during PCB design.

1. Place the external protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply decoupling capacitors and charge pump capacitors as close as possible to the respective device pins such as V_{CC}, V_{IO}, V+, V-, C1+ to C1-, C2+ to C2- pins of transceiver.
5. Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Optionally, use 1kΩ to 10kΩ pullup and pulldown resistors for control lines to limit noise currents in these lines during transient events.

Use at least 9 vias for better thermal dissipation, but 0 vias is still acceptable as long the system can make sure die temp below recommend range (150C). A thermal analysis is done on different power dissipation levels and the effect on the die temperature with a 21, 9 and 0 vias. SeeTable 8-1 for this example.

Table 8-1. Effect of Number of Vias on Thermal Performance

	575mV			**200mV**		
Number of Vias	21	9	0	21	9	0
Max Die Temperature	100.2°C	102.4°C	109.4°C	90.3°C	91.1°C	93.6°C
Effective	26.2°C/W	30.1°C/W	42.3°C/W	26.5°C/W	30.4°C/W	42.7°C/W

8.4.2 Layout Example

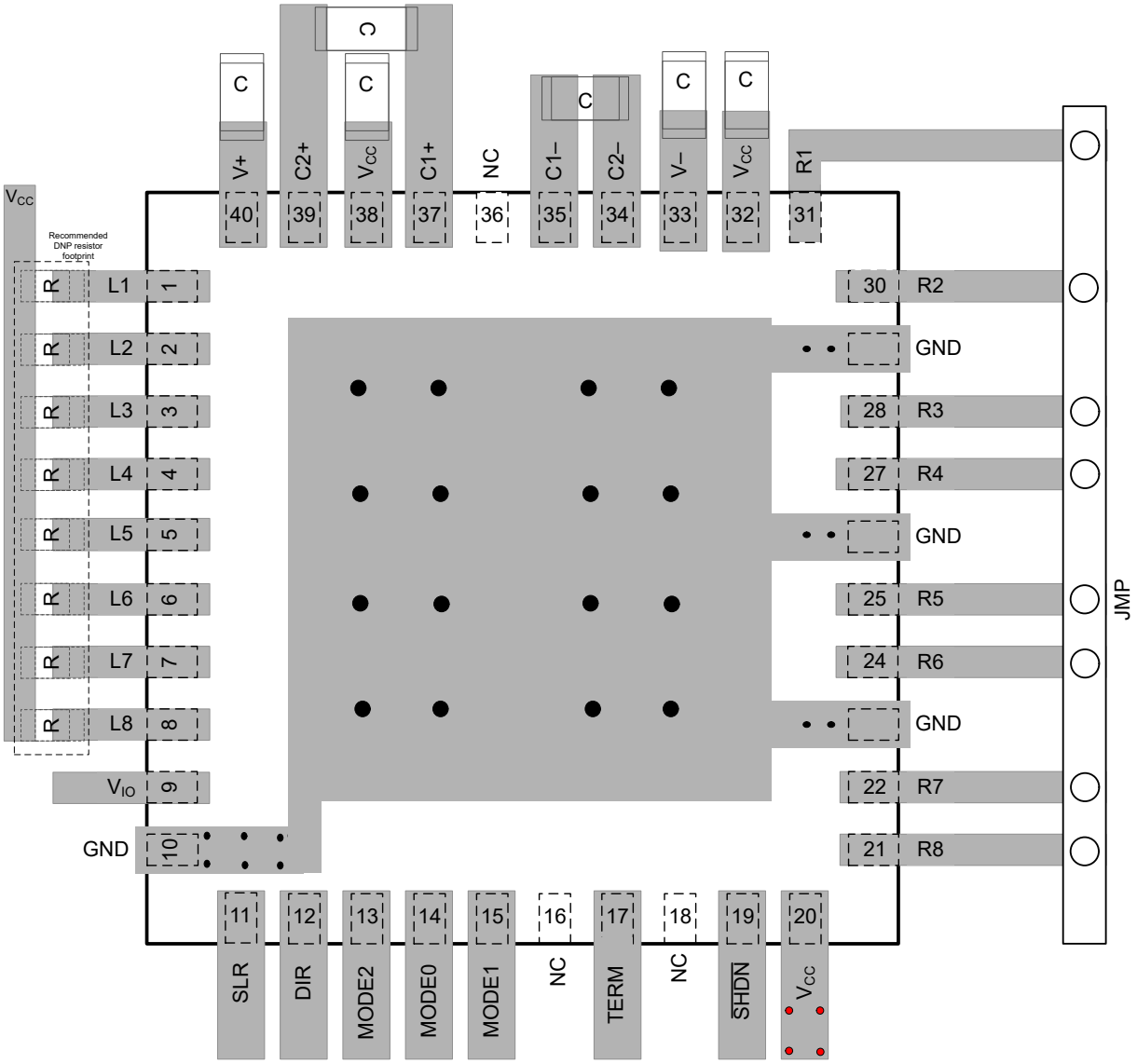


Figure 8-14. Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2025) to Revision A (July 2026) — **Page**

- Changed the document status from *Advanced Information* to *Production* data — 1
- Corrected pin 10 description from GND/NC to GND — 3
- Corrected RS-232 loopback mode diagram — 32
- Updated recommended layout image — 32

DATE	REVISION	NOTES
November 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THVD4431ARHAR	Active	Production	VQFN (RHA) | 40	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	THVD 4431A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

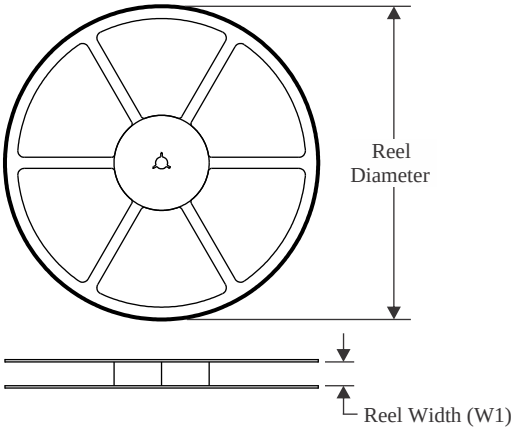
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

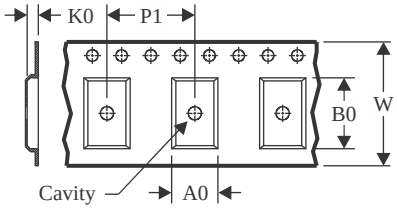
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

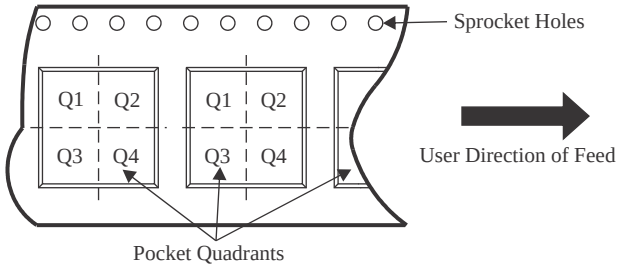


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

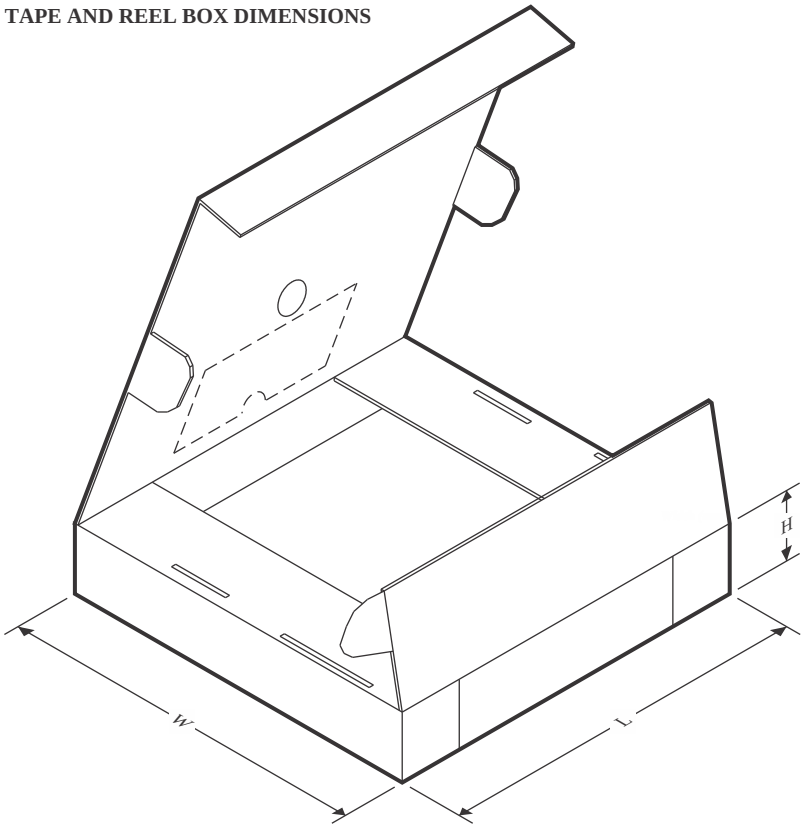
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD4431ARHAR	VQFN	RHA	40	4000	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD4431ARHAR	VQFN	RHA	40	4000	360.0	360.0	36.0

GENERIC PACKAGE VIEW

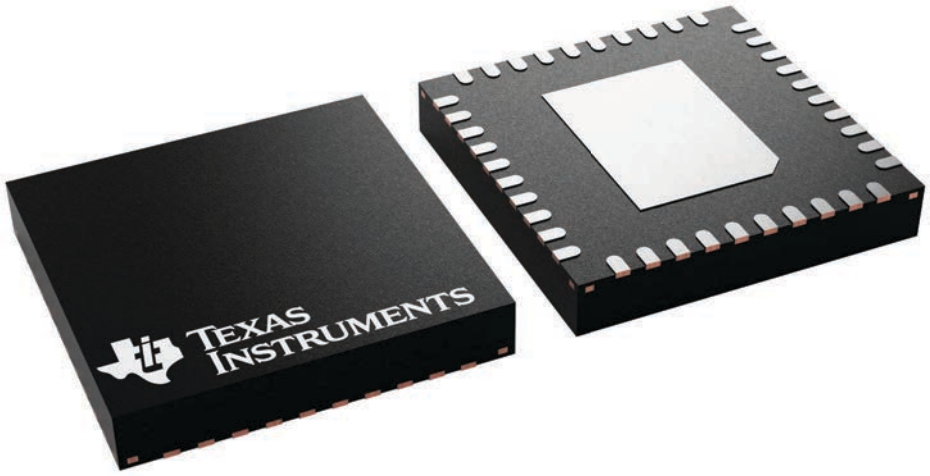
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225870/A

DATA BOOK
PACKAGE OUTLINE

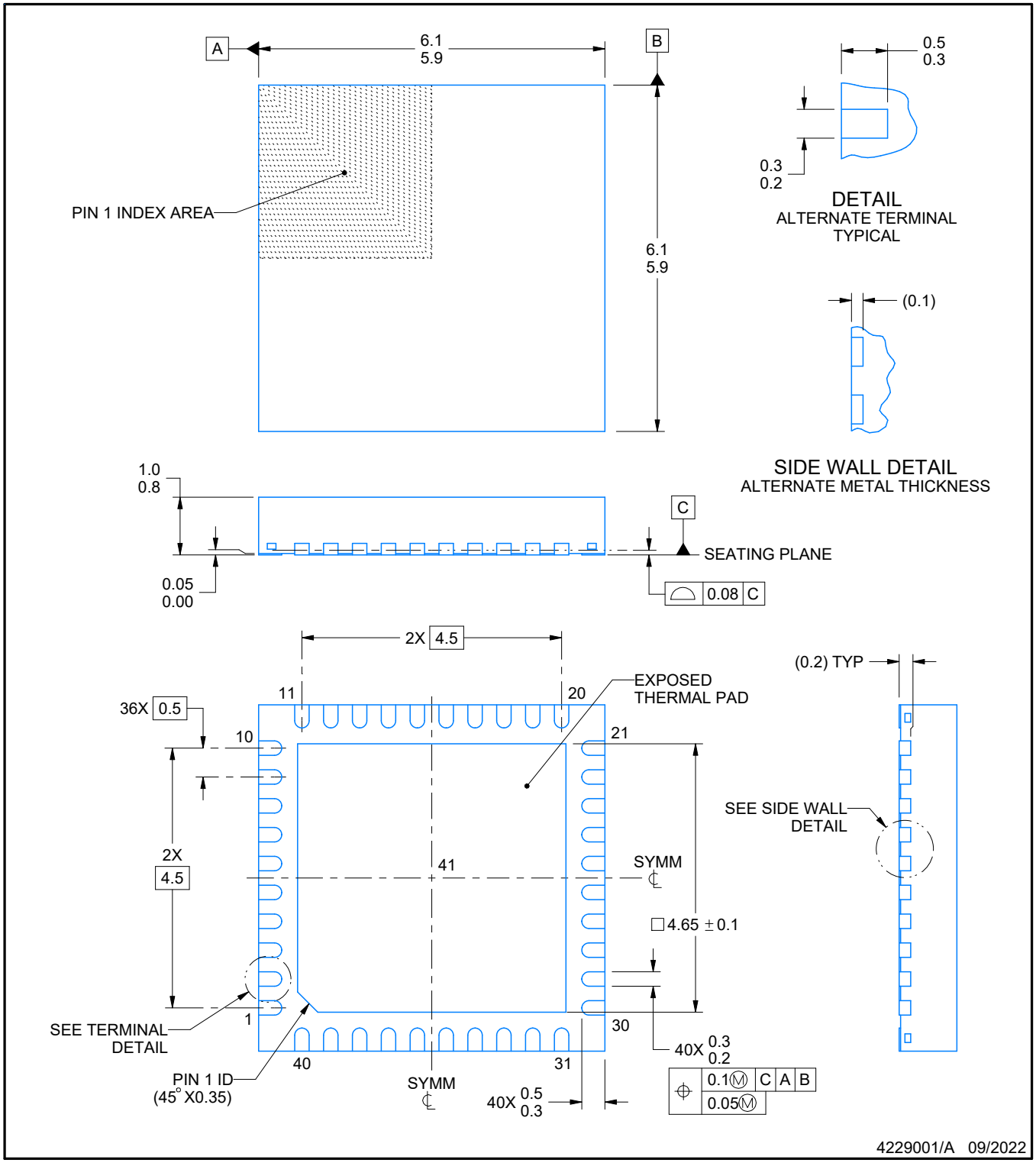
DRAFTER: K. SINCERBOX	DATE: 09/01/2022					DIMENSIONS IN MILLIMETERS	
DESIGNER:	DATE:	TEXAS INSTRUMENTS SEMICONDUCTOR OPERATIONS				CODE IDENTITY NUMBER 01295	
CHECKER: K. SINCERBOX	DATE: 09/01/2022						
ENGINEER: S. KUMMERL	DATE: 09/01/2022	ePOD, RHA0040R / VQFN, 40 PIN, 0.5 MM PITCH					
APPROVED: D. CHIN & D. KAN	DATE: 09/01/2022						
RELEASED: K. SINCERBOX	DATE: 09/01/2022						
TEMPLATE INFO: EDGE# 4218519	DATE: 04/07/2016	SCALE NTS	SIZE A	4229001		REV A	PAGE 1 OF 5

RHA0040R

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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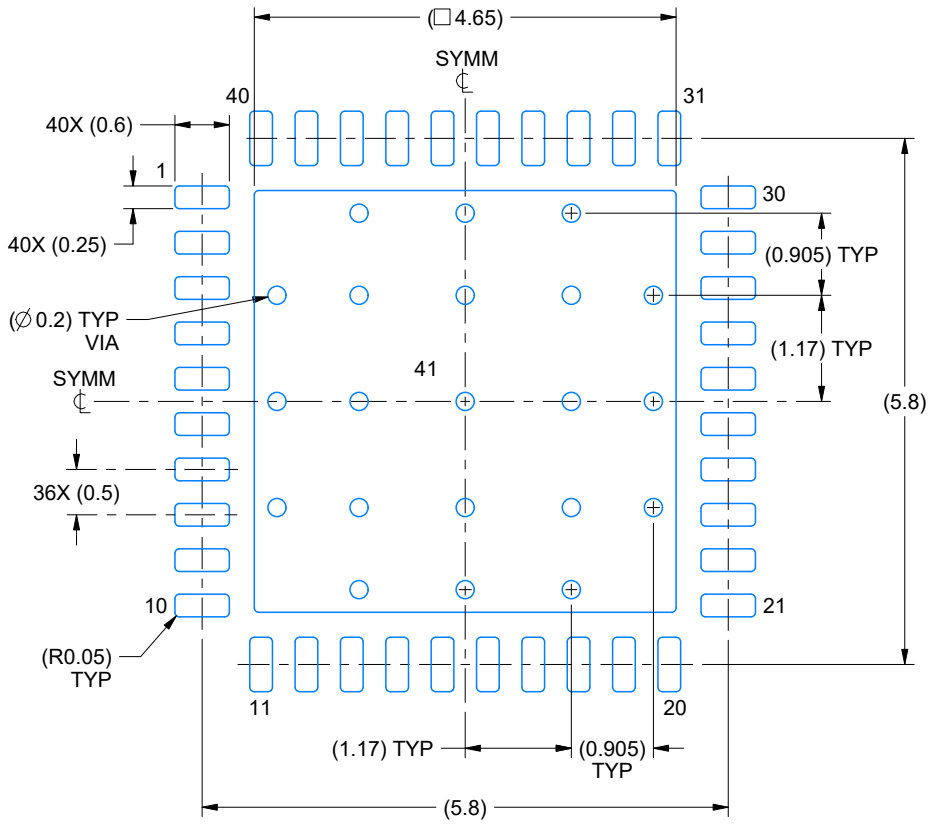
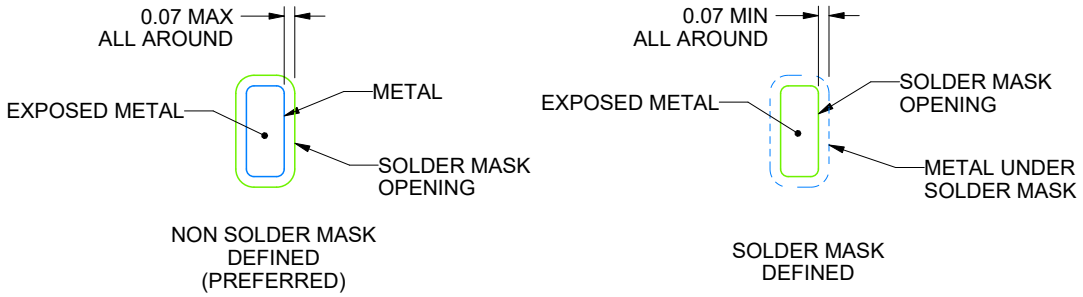
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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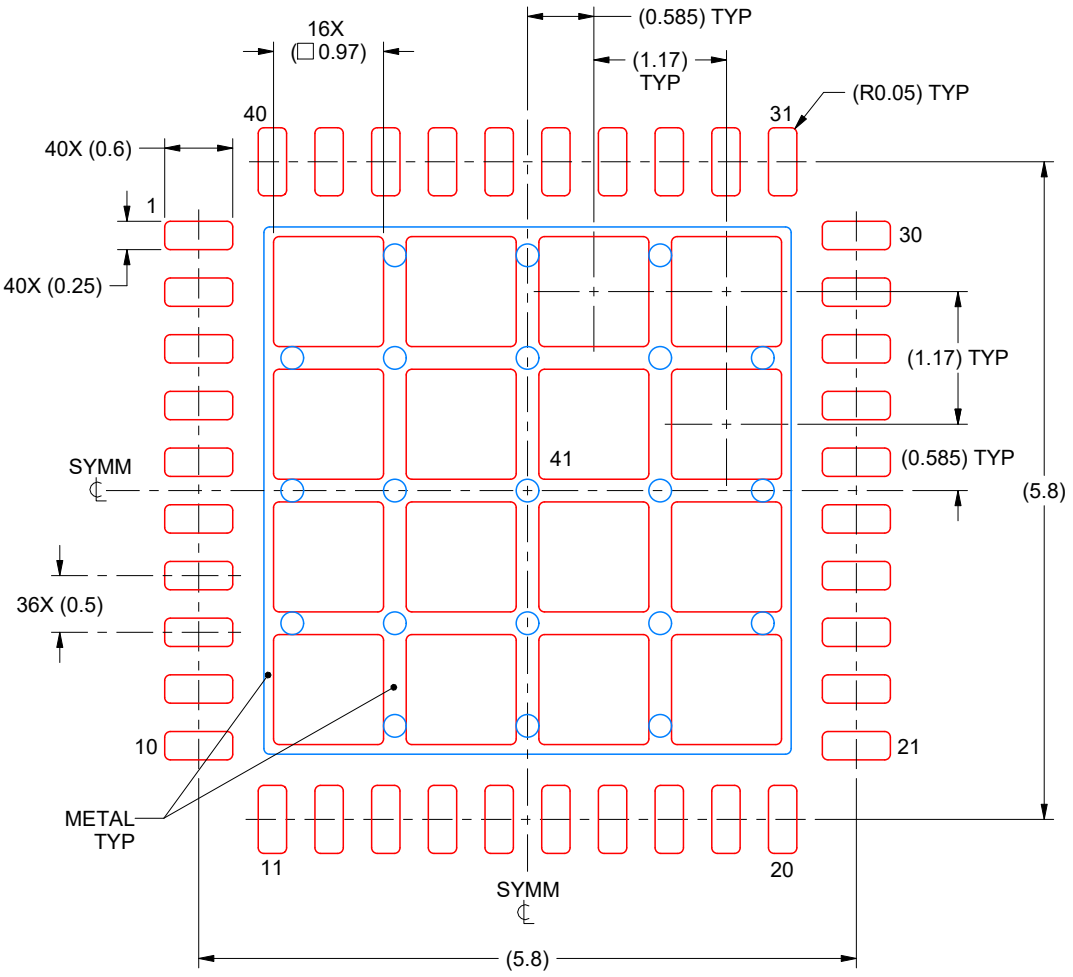
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
69% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTSMAN
A	RELEASE NEW DRAWING	2201054	09/01/2022	S. KUMMERL / K. SINCERBOX

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Last updated 10/2025