TL1431 Precision Programmable Reference

1 Features

- 0.4% Initial Voltage Tolerance
- 0.2Ω Typical Output Impedance
- Fast Turnon (500ns)
- Sink Current Capability (1mA to 100mA)
- Low Reference Current (REF)
- Adjustable Output Voltage ($V_{I(ref)}$ to 36V)

2 Applications

- Adjustable Voltage and Current Referencing
- Secondary Side Regulation in Flyback SMPSs
- Zener Replacement
- Voltage Monitoring
- Comparator With Integrated Reference

3 Description

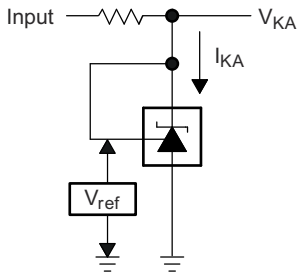
The TL1431 device is a precision programmable reference with specified thermal stability over automotive, commercial, and military temperature ranges. The output voltage can be set to any value between $V_{I(ref)}$ (approximately 2.5V) and 36V with two external resistors (see Figure 8-3). This device has a typical output impedance of 0.2Ω. Active output circuitry provides a sharp turnon characteristic, making the device an excellent replacement for Zener diodes and other types of references in applications such as onboard regulation, adjustable power supplies, and switching power supplies.

The TL1431C is characterized for operation over the commercial temperature range of 0°C to 70°C. The TL1431Q is characterized for operation over the full automotive temperature range of –40°C to 125°C. The TL1431M is characterized for operation over the full military temperature range of –55°C to 125°C.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TL1431D	SOIC (8)	3.90mm × 4.90mm
TL1431PW	TSSOP (8)	4.40mm × 3.00mm
TL1431LP	TO-92 (3)	4.83mm × 3.68mm
TL1431MJG	CDIP (8)	9.58mm x 6.67mm
TL1431MFK	LCCC (20)	8.89mm x 8.89mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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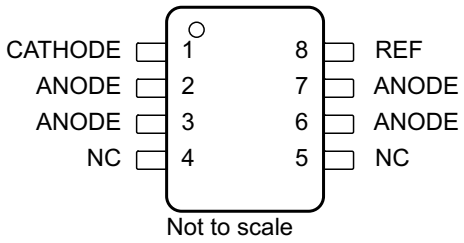
4 Pin Configuration and Functions



ANODE terminals are connected internally

Figure 4-1. D Package 8-Pin SOIC Top View

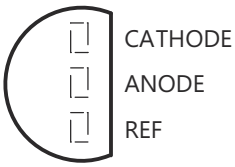


Figure 4-2. LP Package 3-Pin TO-92 Top View

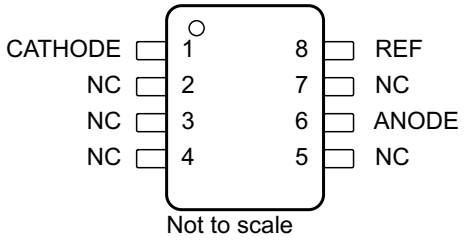


Figure 4-3. JG or PW Package 8-Pin CDIP or TSSOP Top View

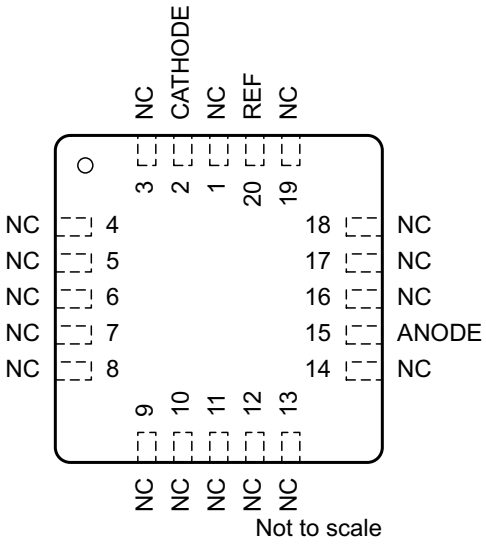


Figure 4-4. FK Package 20-Pin LCCC Top View

Table 4-1. Pin Functions

PIN					I/O	DESCRIPTION
NAME	SOIC	CDIP, TSSOP	TO-92	LCCC		
ANODE	2, 3, 6, 7	6	2	15	O	Common pin, normally connected to ground
CATHODE	1	1	1	2	I/O	Shunt current/voltage input
REF	8	8	3	20	I	Threshold relative to common ground
NC	4, 5	2, 3, 4, 5, 7	—	1, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 16, 17, 18, 19	—	No internal connection

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Cathode voltage, V_{KA} (2)		37	V
Continuous cathode current, I_{KA}	–100	150	mA
Reference input current, $I_{I(ref)}$	–0.05	10	mA
Lead temperature, 1.6mm (1/16in) from case for 10s		260	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ANODE, unless otherwise noted.

5.2 ESD Ratings – TL1431C, TL1431Q

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{KA}	Cathode voltage		$V_{I(ref)}$	36	V
I_{KA}	Cathode current		1	100	mA
T_A	Operating free-air temperature	TL1431C	0	70	°C
		TL1431Q	–40	125	
		TL1431M	–55	125	

5.4 Thermal Information

THERMAL METRIC(1)		TL1431			TL1431M(2)		UNIT
		LP (TO-92)	D (SOIC)	PW (TSSOP)	JG (CDIP)	FK (LCCC)	
		3 PINS	8 PINS	8 PINS	8 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	157	114.7	172.4	—	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.7	59	55.2	69.7	55.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	—	55.4	100.8	99	54.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.6	12	5	—	—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	136.4	54.8	99	—	—	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	21	9.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) $R_{\theta JC}$ based on MIL-STD-883, and $R_{\theta JB}$ based on JESD51.

5.5 Electrical Characteristics – TL1431C

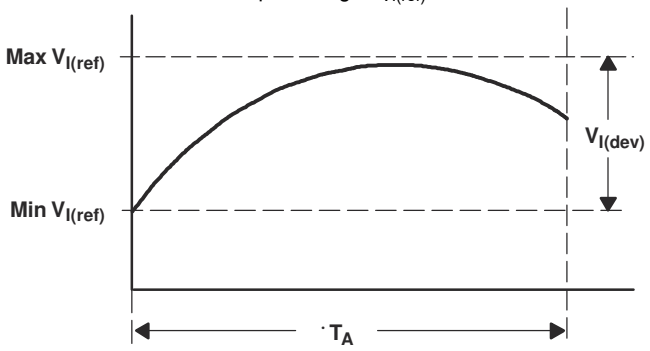
at specified free-air temperature and I_{KA} = 10mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{I(ref)}$	Reference input voltage	$V_{KA} = V_{I(ref)}$ (see Figure 6-1)	T_A = 25°C	2490	2500	2510	mV
			T_A = 0°C to 70°C	2480		2520	
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range(1)	$V_{KA} = V_{I(ref)}$, T_A = 0°C to 70°C (see Figure 6-1)			4	20	mV
$\frac{\Delta V_{I(ref)}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	ΔV_{KA} = 3V to 36V, T_A = 0°C to 70°C (see Figure 6-2)			–1.1	–2	mV/V
$I_{I(ref)}$	Reference input current	R1 = 10kΩ, R2 = ∞ (see Figure 6-2)	T_A = 25°C		1.5	2.5	μA
			T_A = 0°C to 70°C			3	
$I_{I(dev)}$	Deviation of reference input current over full temperature range(1)	R1 = 10kΩ, R2 = ∞, T_A = 0°C to 70°C (see Figure 6-2)			0.2	1.2	μA
I_{min}	Minimum cathode current for regulation	$V_{KA} = V_{I(ref)}$, T_A = 25°C (see Figure 6-1)			0.45	1	mA
I_{off}	Off-state cathode current	V_{KA} = 36V, $V_{I(ref)}$ = 0 (see Figure 6-3)	T_A = 25°C		0.18	0.5	μA
			T_A = 0°C to 70°C			2	
$\lvert z_{KA} \rvert$	Output impedance(2)	$V_{KA} = V_{I(ref)}$, f ≤ 1kHz, I_{KA} = 1mA to 100mA, T_A = 25°C (see Figure 6-1)			0.2	0.4	Ω

(1) The deviation parameters $V_{I(dev)}$ and $I_{I(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage $\alpha_{VI(ref)}$ is defined as:

$$\left|\alpha_{V_{I(ref)}}\right| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{I(dev)}}{V_{I(ref)\ at\ 25°C}}\right) \times 10^6}{T_A}$$

where:
ΔT_A is the rated operating temperature range of the device.



$\alpha_{VI(ref)}$ is positive or negative, depending on whether minimum $V_{I(ref)}$ or maximum $V_{I(ref)}$, respectively, occurs at the lower temperature.

(2) The output impedance is defined as: $|z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$
When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by:
$|z'| = \frac{\Delta V}{\Delta I}$, which is approximately equal to $|z_{KA}|\left(1 + \frac{R1}{R2}\right)$.

5.6 Electrical Characteristics – TL1431Q

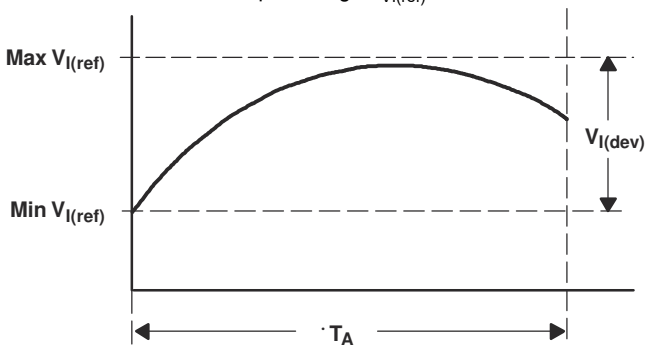
at specified free-air temperature and I_{KA} = 10mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{I(ref)}$	Reference input voltage	$V_{KA} = V_{I(ref)}$ (see Figure 6-1)	T_A = 25°C	2490	2500	2510	mV
			T_A = –40°C to 125°C	2470		2530	
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range(1)	$V_{KA} = V_{I(ref)}$, T_A = –40°C to 125°C (see Figure 6-1)			17	55	mV
$\frac{\Delta V_{I(ref)}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	ΔV_{KA} = 3V to 36V, T_A = –40°C to 125°C (see Figure 6-2)			–1.1	–2	mV/V
$I_{I(ref)}$	Reference input current	R1 = 10kΩ, R2 = ∞ (see Figure 6-2)	T_A = 25°C		1.5	2.5	μA
			T_A = –40°C to 125°C			4	
$I_{I(dev)}$	Deviation of reference input current over full temperature range(1)	R1 = 10kΩ, R2 = ∞, T_A = –40°C to 125°C (see Figure 6-2)			0.5	2	μA
I_{min}	Minimum cathode current for regulation	$V_{KA} = V_{I(ref)}$, T_A = 25°C (see Figure 6-1)			0.45	1	mA
I_{off}	Off-state cathode current	V_{KA} = 36V, $V_{I(ref)}$ = 0 (see Figure 6-3)	T_A = 25°C		0.18	0.5	μA
			T_A = –40°C to 125°C			2	
$\lvert z_{KA} \rvert$	Output impedance(2)	$V_{KA} = V_{I(ref)}$, f ≤ 1kHz, I_{KA} = 1mA to 100mA, T_A = 25°C (see Figure 6-1)			0.2	0.4	Ω

(1) The deviation parameters $V_{I(dev)}$ and $I_{I(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage $\alpha_{VI(ref)}$ is defined as:

$$\left|\alpha_{V_{I(ref)}}\right| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{I(dev)}}{V_{I(ref)\ at\ 25°C}}\right) \times 10^6}{T_A}$$

where:
ΔT_A is the rated operating temperature range of the device.



$\alpha_{VI(ref)}$ is positive or negative, depending on whether minimum $V_{I(ref)}$ or maximum $V_{I(ref)}$, respectively, occurs at the lower temperature.

(2) The output impedance is defined as: $|z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$
When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by:
$|z'| = \frac{\Delta V}{\Delta I}$, which is approximately equal to $|z_{KA}|\left(1 + \frac{R1}{R2}\right)$.

5.7 Electrical Characteristics – TL1431M

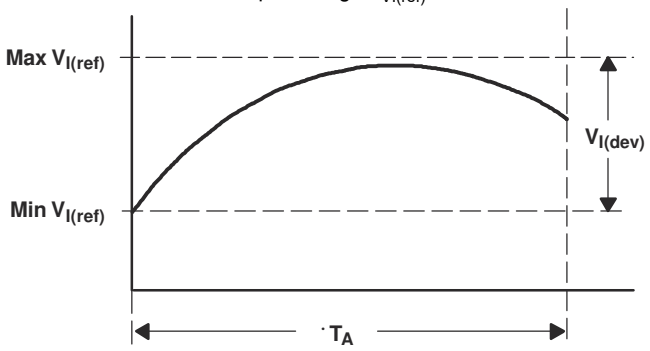
at specified free-air temperature and I_{KA} = 10mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{I(ref)}$	Reference input voltage	$V_{KA} = V_{I(ref)}$ (see Figure 6-1)	T_A = 25°C	2475	2500	2540	mV
			T_A = –55°C to 125°C	2460		2550	
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range(1)	$V_{KA} = V_{I(ref)}$, T_A = –55°C to 125°C (see Figure 6-1)			17	55(2)	mV
$\frac{\Delta V_{I(ref)}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	ΔV_{KA} = 3V to 36V, T_A = –55°C to 125°C (see Figure 6-2)			–1.1	–2	mV/V
$I_{I(ref)}$	Reference input current	R1 = 10kΩ, R2 = ∞ (see Figure 6-2)	T_A = 25°C		1.5	2.5	μA
			T_A = –55°C to 125°C			5	
$I_{I(dev)}$	Deviation of reference input current over full temperature range(1)	R1 = 10kΩ, R2 = ∞, T_A = –55°C to 125°C (see Figure 6-2)			0.5	3(2)	μA
I_{min}	Minimum cathode current for regulation	$V_{KA} = V_{I(ref)}$, T_A = 25°C (see Figure 6-1)			0.45	1	mA
I_{off}	Off-state cathode current	V_{KA} = 36V, $V_{I(ref)}$ = 0 (see Figure 6-3)	T_A = 25°C		0.18	0.5	μA
			T_A = –55°C to 125°C			2	
$\lvert z_{KA} \rvert$	Output impedance(3)	$V_{KA} = V_{I(ref)}$, f ≤ 1kHz, I_{KA} = 1mA to 100mA, T_A = 25°C (see Figure 6-1)			0.2	0.4	Ω

(1) The deviation parameters $V_{I(dev)}$ and $I_{I(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage $\alpha_{VI(ref)}$ is defined as:

$$\left|\alpha_{V_{I(ref)}}\right| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{I(dev)}}{V_{I(ref)\ at\ 25°C}}\right) \times 10^6}{T_A}$$

where:
ΔT_A is the rated operating temperature range of the device.



$\alpha_{VI(ref)}$ is positive or negative, depending on whether minimum $V_{I(ref)}$ or maximum $V_{I(ref)}$, respectively, occurs at the lower temperature.

(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(3) The output impedance is defined as: $|z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$
When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by:
$|z'| = \frac{\Delta V}{\Delta I}$, which is approximately equal to $|z_{KA}|\left(1 + \frac{R1}{R2}\right)$.

5.8 Typical Characteristics

Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

Table 5-1. Table Of Graphs

GRAPH	FIGURE
Reference voltage vs Free-air temperature	Figure 5-1
Reference current vs Fire-air temperature	Figure 5-2
Cathode current vs Cathode voltage	Figure 5-3, Figure 5-4
Off-state cathode current vs Free-air temperature	Figure 5-5
Ratio of delta reference voltage to delta cathode voltage vs Free-air temperature	Figure 5-6
Equivalent input-noise voltage vs Frequency	Figure 5-7
Equivalent input-noise voltage over a 10 second period	Figure 5-8
Small-signal voltage amplification vs Frequency	Figure 5-9
Reference impedance vs Frequency	Figure 5-10
Pulse response	Figure 5-11
Stability boundary conditions	Figure 5-12

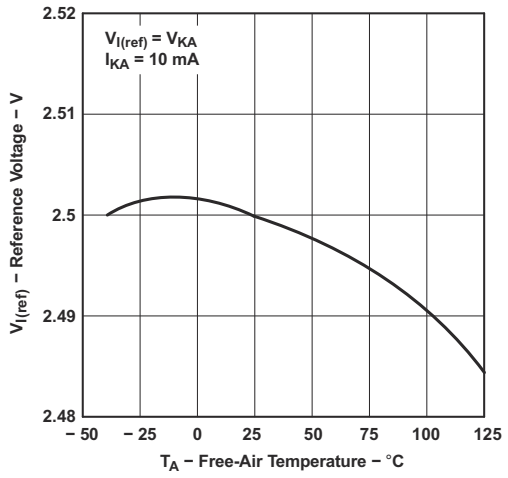


Figure 5-1. Reference Voltage vs Free-Air Temperature

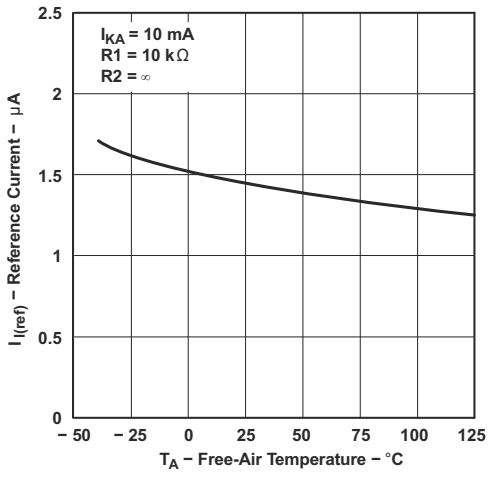


Figure 5-2. Reference Current vs Free-Air Temperature

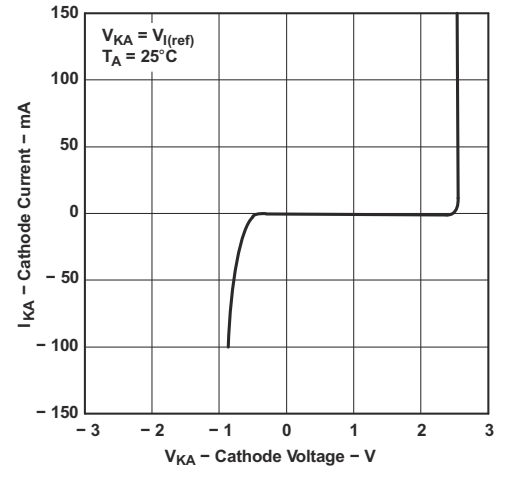


Figure 5-3. Cathode Current vs Cathode Voltage

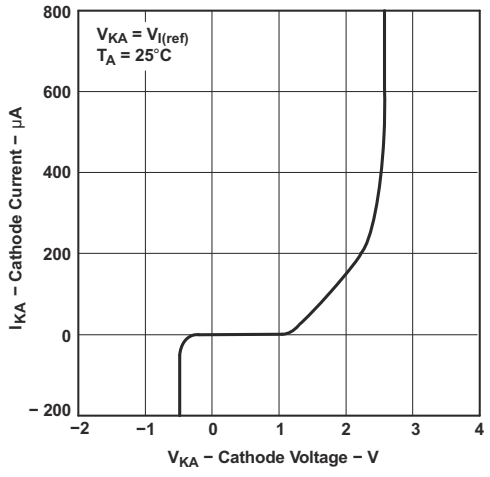


Figure 5-4. Cathode Current vs Cathode Voltage

5.8 Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

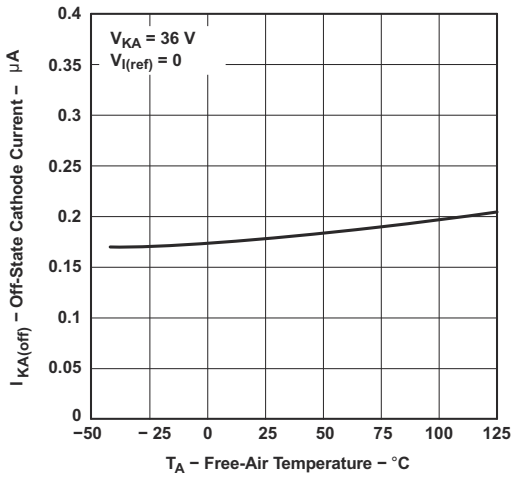


Figure 5-5. Off-State Cathode Current vs Free-Air Temperature

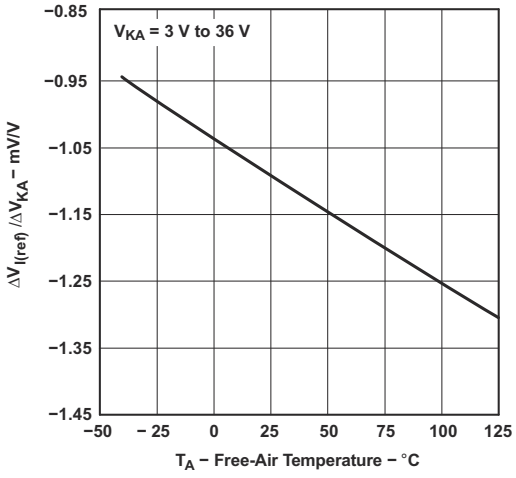


Figure 5-6. Ratio Of Delta Reference Voltage To Delta Cathode Voltage vs Free-Air Temperature

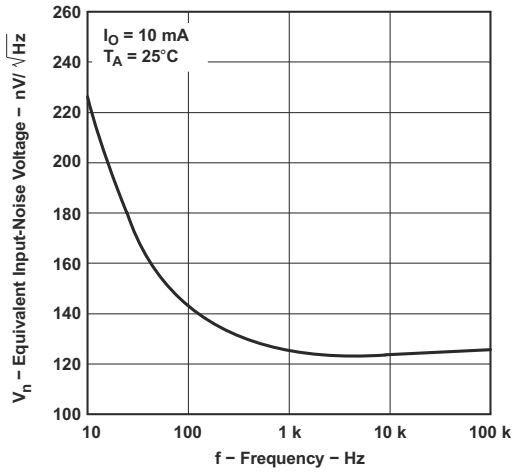


Figure 5-7. Equivalent Input-Noise Voltage vs Frequency

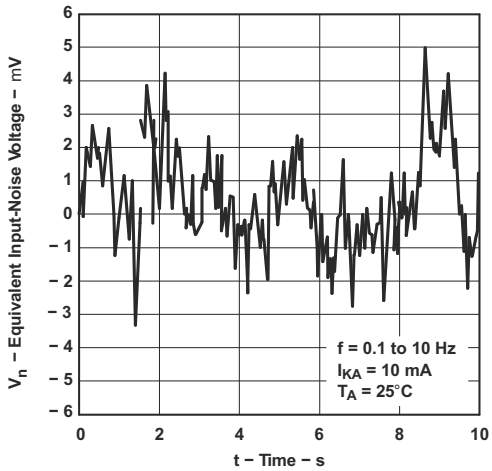


Figure 5-8. Equivalent Input-Noise Voltage Over A 10S Period

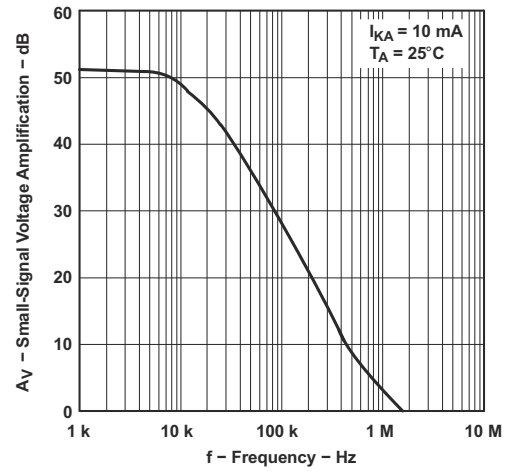


Figure 5-9. Small-Signal Voltage Amplification vs Frequency

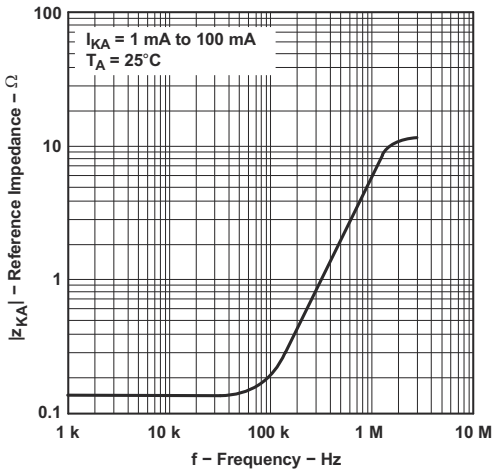


Figure 5-10. Reference Impedance vs Frequency

5.8 Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

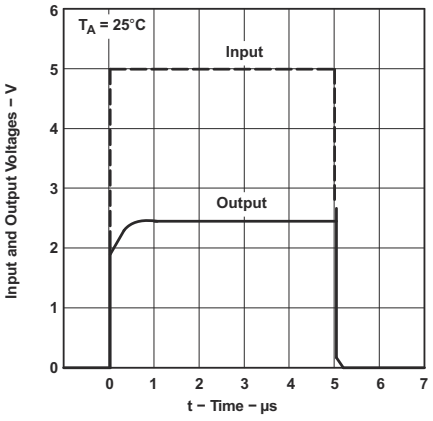
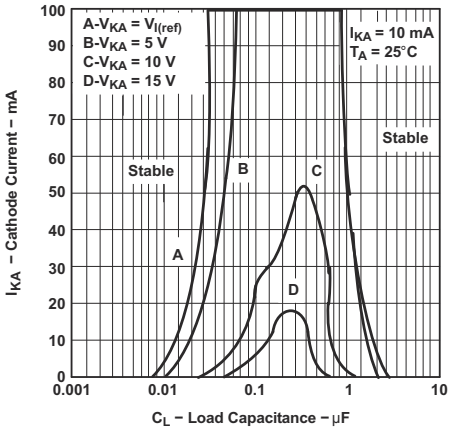


Figure 5-11. Pulse Response



The areas under the curves represent conditions that may cause the device to oscillate. For curves B, C, and D, R2 and V+ are adjusted to establish the initial V_{KA} and I_{KA} conditions, with C_L = 0. V_{BATT} and C_L then are adjusted to determine the ranges of stability.

Figure 5-12. Stability Boundary Conditions

6 Parameter Measurement Information

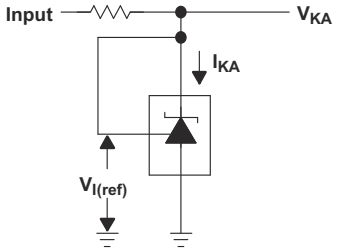


Figure 6-1. Test Circuit For $V_{(KA)} = V_{ref}$

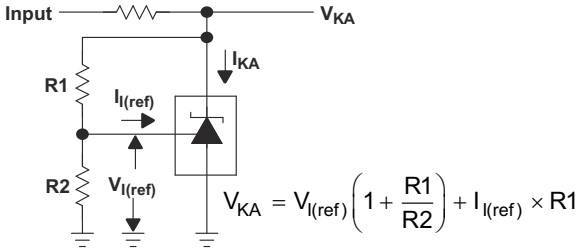


Figure 6-2. Test Circuit For $V_{(KA)} > V_{ref}$

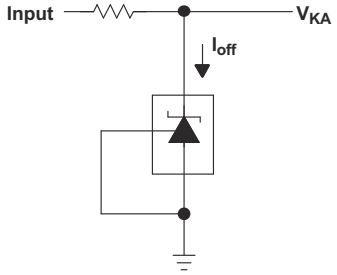


Figure 6-3. Test Circuit For I_{off}

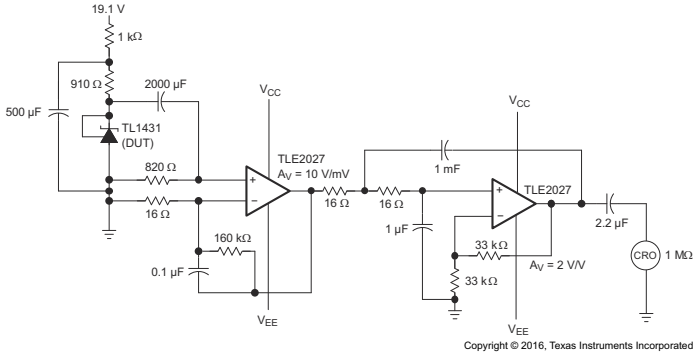


Figure 6-4. Test Circuit For 0.1Hz To 10Hz Equivalent Input-Noise Voltage

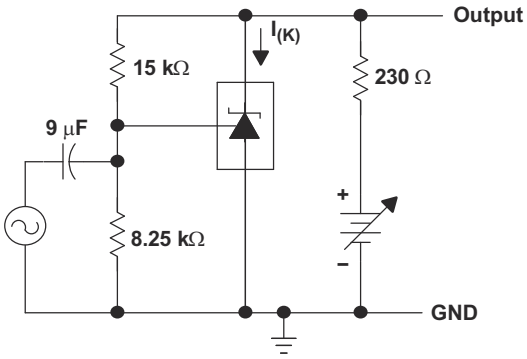


Figure 6-5. Test Circuit For Voltage Amplification

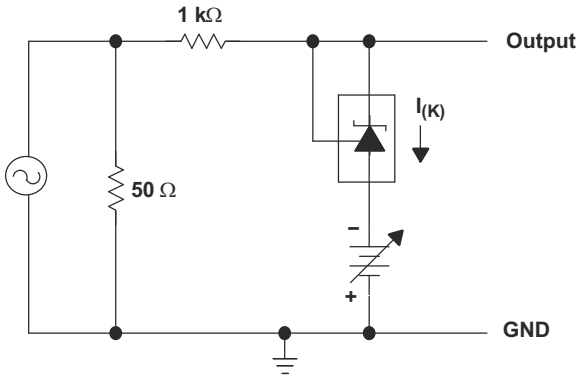


Figure 6-6. Test Circuit For Reference Impedance

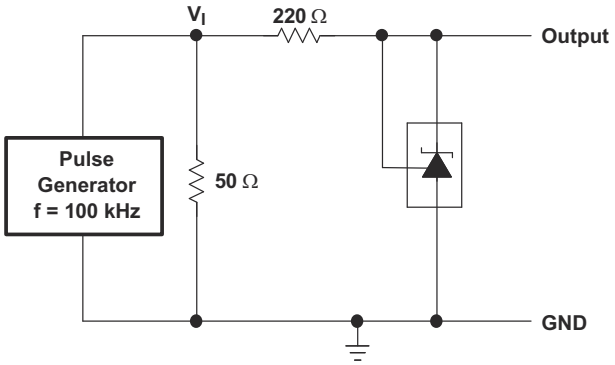
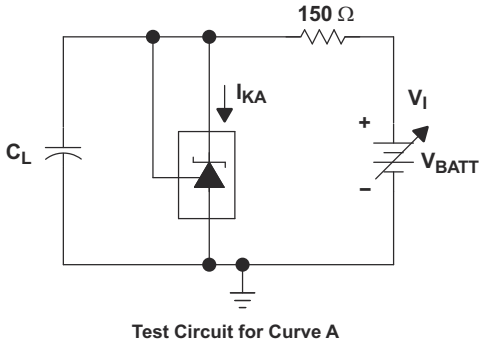


Figure 6-7. Test Circuit For Pulse Response



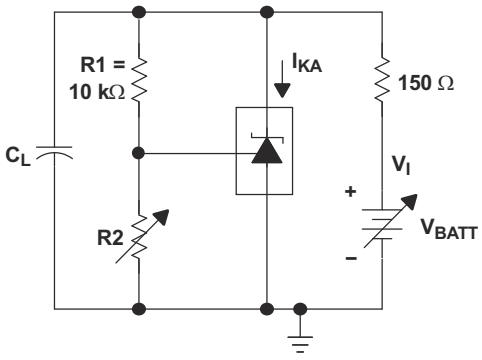


Figure 6-8. Test Circuits For Curves A Through D

7 Detailed Description

7.1 Overview

The TL1431 device has proven ubiquity and versatility across a wide range of applications, ranging from power to signal path. This is due to its key components containing an accurate voltage reference and op amp, which are very fundamental analog building blocks. TL1431 is used in conjunction with its key components to behave as a single voltage reference, error amplifier, voltage clamp, or comparator with integrated reference. TL1431 can be operated and adjusted to cathode voltages from 2.5V to 36V, making this part optimum for a wide range of end equipments in industrial, auto, telecom, and computing. In order for this device to behave as a shunt regulator or error amplifier, >1mA (Imin(max)) must be supplied in to the cathode pin. Under this condition, feedback can be applied from the Cathode and Ref pins to create a replica of the internal reference voltage. Various reference voltage options can be purchased with initial tolerances (at 25°C) of 0.4% and 1%. The TL1431C devices are characterized for operation from 0°C to 70°C, the TL1431Q devices are characterized for operation from –40°C to 125°C, and the TL1431M devices are characterized for operation from –55°C to 125°C.

7.2 Functional Block Diagram

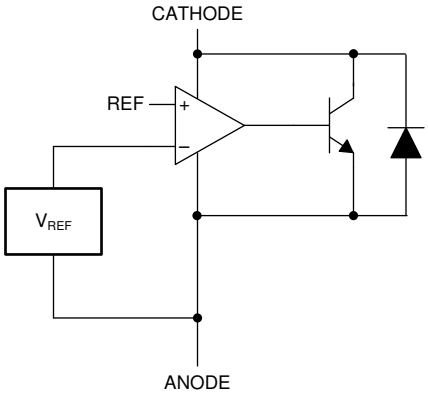
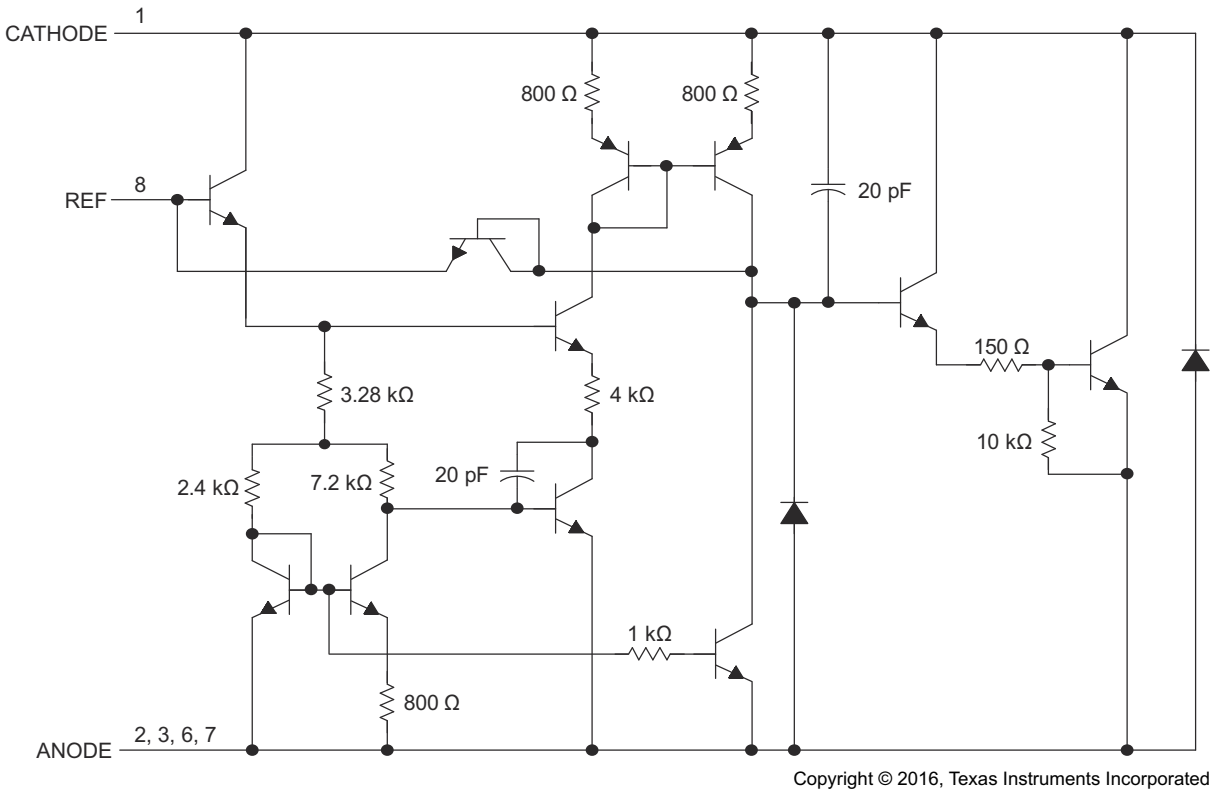


Figure 7-1. Equivalent Schematic



A. All component values are nominal.
B. Pin numbers shown are for the D package.

Figure 7-2. Detailed Schematic

7.3 Feature Description

TL1431 consists of an internal reference and amplifier that outputs a sink current base on the difference between the reference pin and the virtual internal pin. The sink current is produced by the internal Darlington pair, shown in Figure 7-2. A Darlington pair is used in order for this device to be able to sink a maximum current of 100mA. When operated with enough voltage headroom (≥ 2.5V) and cathode current (I_{KA}), TL1431 forces the reference pin to 2.5V. However, the reference pin can not be left floating, as it needs I_{REF} ≥ 5µA (see *Electrical Characteristics – TL1431M*). This is because the reference pin is driven into an npn, which needs base current to operate properly. When feedback is applied from the cathode and reference pins, TL1431 behaves as a Zener diode, regulating to a constant voltage dependent on current being supplied into the cathode. This is due to the internal amplifier and reference entering the proper operating regions. The same amount of current needed in the above feedback situation must be applied to this device in open loop, servo, or error amplifying implementations in order for it to be in the proper linear region giving TL1431 enough gain. Unlike many linear regulators, TL1431 is internally compensated to be stable without an output capacitor between the cathode and anode. However, if desired an output capacitor can be used as a guide to assist in choosing the correct capacitor to maintain stability.

7.4 Device Functional Modes

7.4.1 Open Loop (Comparator)

When the cathode or output voltage or current of TL1431 is not being fed back to the reference or input pin in any form, this device is operating in open loop. With proper cathode current (I_{KA}) applied to this device, TL1431 has the characteristics shown in Figure 7-2. With such high gain in this configuration, TL1431 is typically used as a comparator. With the reference integrated makes TL1431 the preferred choice when users are trying to monitor a certain level of a single signal.

7.4.2 Closed Loop

When the cathode or output voltage or current of TL1431 is being fed back to the reference or input pin in any form, this device is operating in closed loop. The majority of applications involving TL1431 use it in this manner to regulate a fixed voltage or current. The feedback enables this device to behave as an error amplifier, computing a portion of the output voltage and adjusting it to maintain the desired regulation. This is done by relating the output voltage back to the reference pin in a manner to make it equal to the internal reference voltage, which can be accomplished through resistive or direct feedback.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

As the TL1431 device has many applications and setups, there are many situations that this datasheet cannot characterize in detail. The linked application notes help the designer make the best choices when using this part. *Understanding Stability Boundary Conditions Charts in TL431, TL432 Data Sheet* (SLVA482) provides a deeper understanding of this devices stability characteristics and aid the user in making the right choices when choosing a load capacitor. *Setting the Shunt Voltage on an Adjustable Shunt Regulator* (SLVA445) assists designers in setting the shunt voltage to achieve optimum accuracy for this device.

8.2 Typical Application

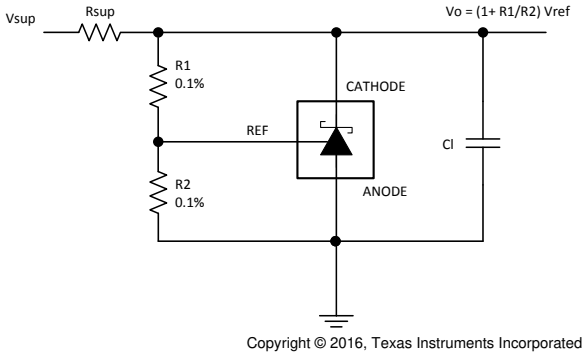


Figure 8-1. Comparator Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

PARAMETER	VALUE
Reference initial accuracy	0.4%
Supply voltage	48V
Cathode current (I_K)	50µA
Output voltage level	2.5V to 36V
Load capacitance	1nF
Feedback resistor values and accuracy (R1 and R2)	10kΩ

8.2.2 Detailed Design Procedure

When using TL1431 as a shunt regulator, determine the following:

- Input voltage range
- Temperature range
- Total accuracy
- Cathode current
- Reference initial accuracy
- Output capacitance

8.2.2.1 Programming Output/Cathode Voltage

To program the cathode voltage to a regulated voltage a resistive bridge must be shunted between the cathode and anode pins with the mid point tied to the reference pin. This can be seen in Figure 8-1, with R1 and R2 being the resistive bridge. The cathode/output voltage in the shunt regulator configuration can be approximated by the equation shown in Figure 8-1. The cathode voltage can be more accurately determined by taking the reference current into account:

$$V_O = \left(1 + \frac{R1}{R2}\right) \times V_{REF} + I_{REF} \times R1 \quad (1)$$

For the above equation to be valid, TL1431 must be fully biased so that it has enough open loop gain to mitigate any gain error. This can be done by meeting the I_{min} specification denoted in Section 5.

8.2.2.2 Total Accuracy

When programming the output above unity gain (V_{KA}=V_{REF}), TL1431 is susceptible to other errors that may effect the overall accuracy beyond V_{REF}. These errors include:

- R1 and R2 accuracies
- $V_{I(dev)}$ – Change in reference voltage over temperature
- ΔV_{REF} / ΔV_{KA} – Change in reference voltage to the change in cathode voltage
- $|z_{KA}|$ – Dynamic impedance, causing a change in cathode voltage with cathode current

Worst case cathode voltage can be determined taking all of the variables in to account.

8.2.2.3 Stability

Though TL1431 is stable with no capacitive load, the device that receives the shunt regulator's output voltage could present a capacitive load that is within the TL1431 region of stability, shown in Figure 5-12. Also, designers may use capacitive loads to improve the transient response or for power supply decoupling. When using additional capacitance between Cathode and Anode, refer to Figure 5-12.

8.2.2.4 Start-up Time

As shown in Figure 8-2, TL1431 has a fast response up to approximately 2V and then slowly charges to its programmed value. This is due to the compensation capacitance the TL1431 has to meet its stability criteria. Despite the secondary delay, TL1431 still has a fast response suitable for many clamp applications.

8.2.3 Application Curve

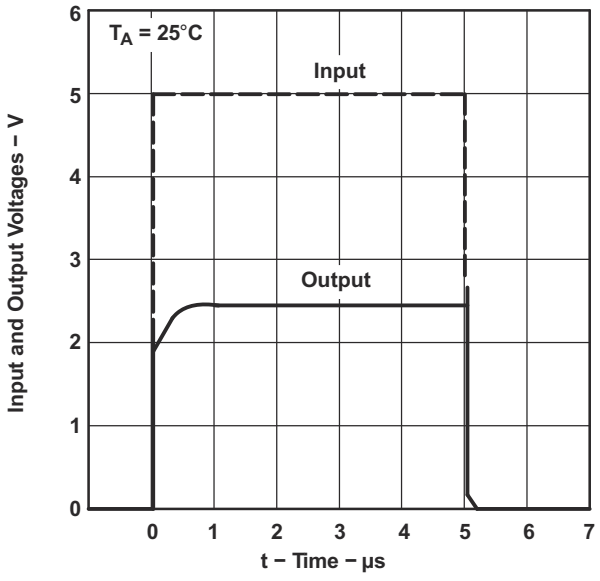


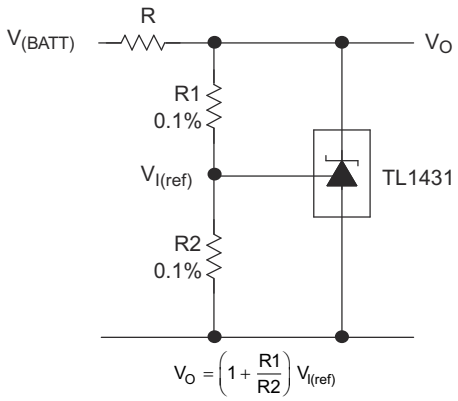
Figure 8-2. TL1431 Start-up Response

8.3 System Examples

Table 8-2 lists example circuits of the TL1431.

Table 8-2. Table of Example Circuits

APPLICATION	FIGURE
Shunt regulator	Figure 8-3
Single-supply comparator with temperature-compensated threshold	Figure 8-4
Precision high-current series regulator	Figure 8-5
Output control of a three-terminal fixed regulator	Figure 8-6
Higher-current shunt regulator	Figure 8-7
Crowbar	Figure 8-8
Precision 5V, 1.5A, 0.5% regulator	Figure 8-9
5V precision regulator	Figure 8-10
PWM converter with 0.5% reference	Figure 8-11
Voltage monitor	Figure 8-12
Delay timer	Figure 8-13
Precision current limiter	Figure 8-14
Precision constant-current sink	Figure 8-15



R must provide cathode current ≥1mA to the TL1431 at minimum $V_{(BATT)}$.

Figure 8-3. Shunt Regulator

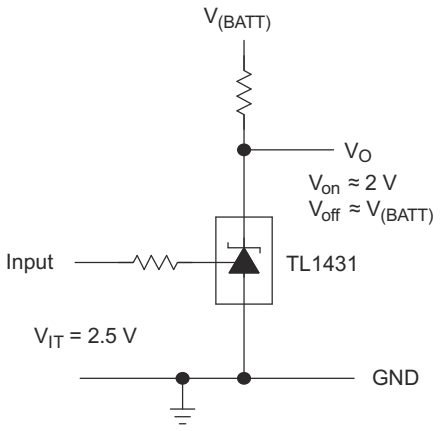
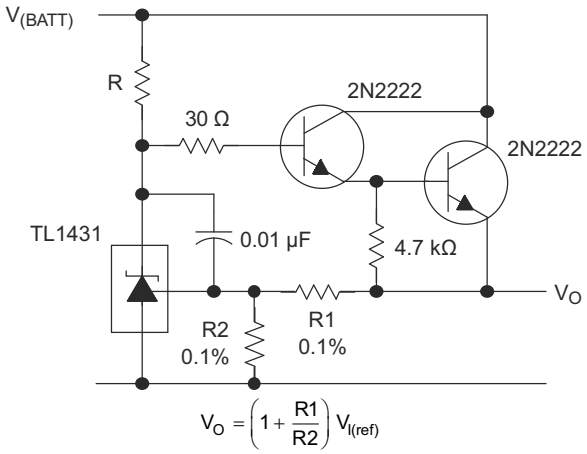


Figure 8-4. Single-Supply Comparator With Temperature-Compensated Threshold



R must provide cathode current ≥1mA to the TL1431 at minimum $V_{(BATT)}$.

Figure 8-5. Precision High-Current Series Regulator

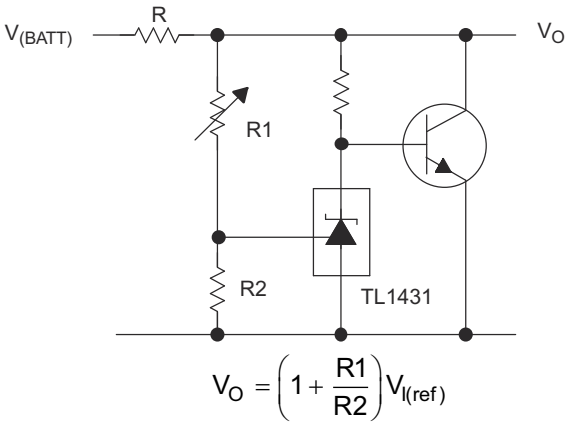


Figure 8-7. Higher-Current Shunt Regulator

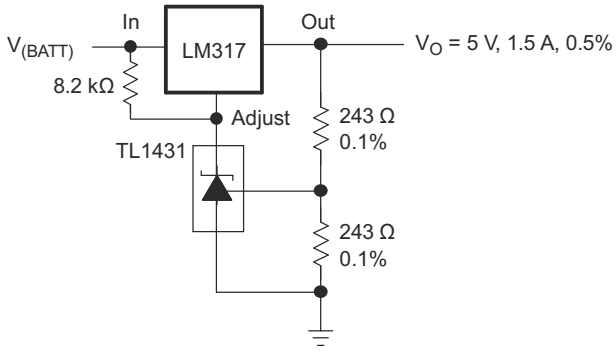


Figure 8-9. Precision 5V, 1.5A, 0.5% Regulator

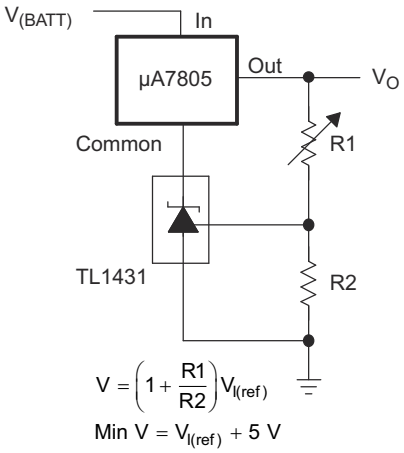
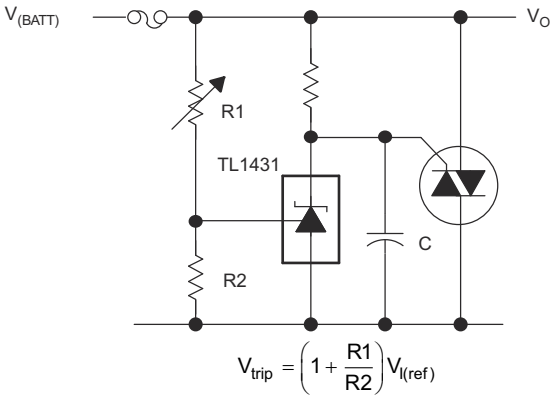
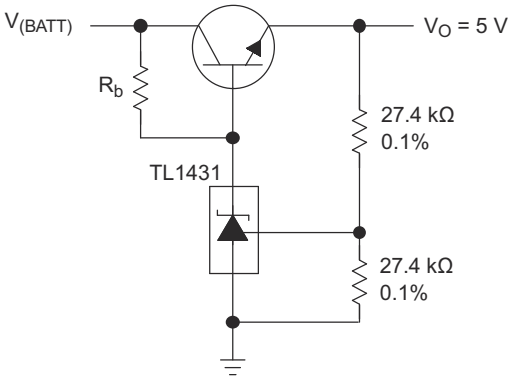


Figure 8-6. Output Control of a Three-Terminal Fixed Regulator



See the stability boundary conditions in Figure 5-12 to determine allowable values for C.

Figure 8-8. Crowbar



R_b must provide cathode current ≥1mA to the TL1431.

Figure 8-10. 5V Precision Regulator

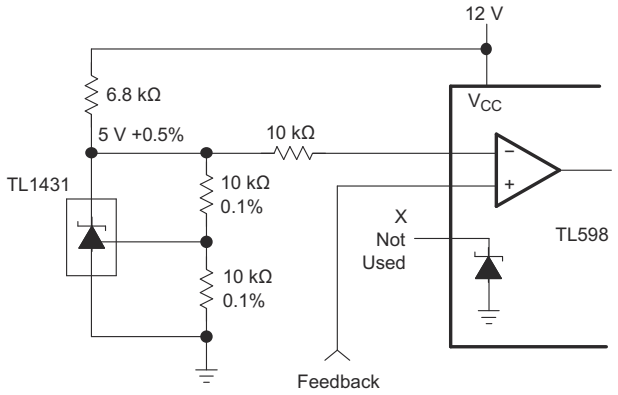
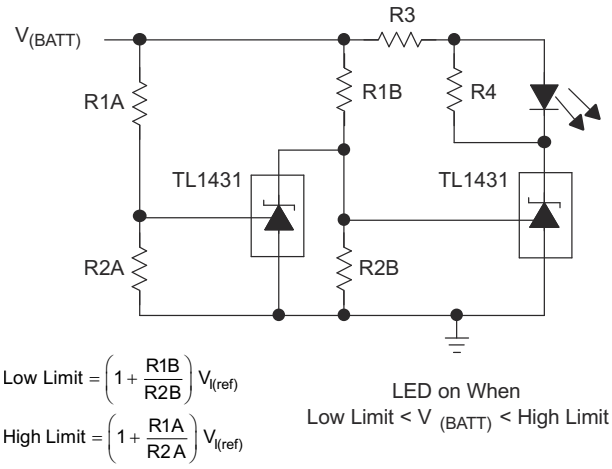


Figure 8-11. PWM Converter With 0.5% Reference



Select R3 and R4 to provide the desired LED intensity and cathode current ≥1mA to the TL1431.

Figure 8-12. Voltage Monitor

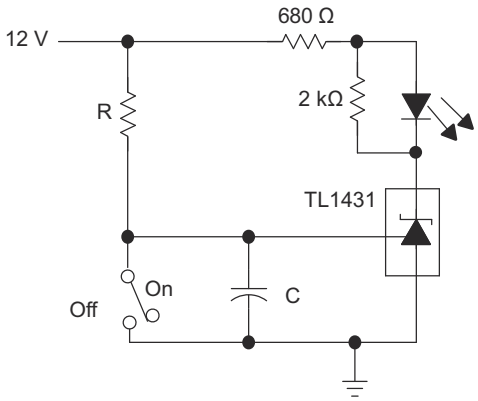


Figure 8-13. Delay Timer

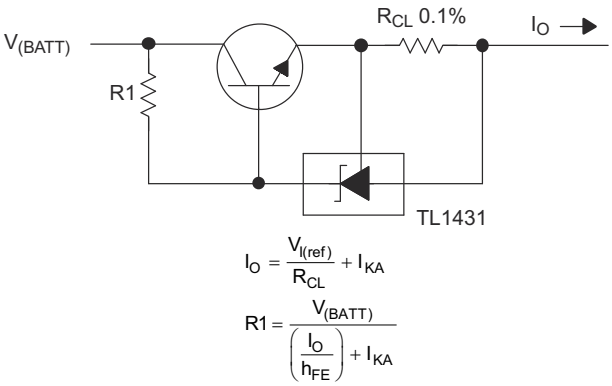


Figure 8-14. Precision Current Limiter

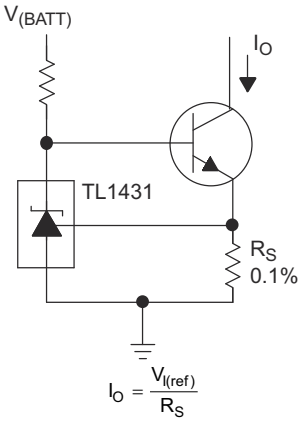


Figure 8-15. Precision Constant-Current Sink

9 Power Supply Recommendations

When using TL1431 as a linear regulator to supply a load, designers typically use a bypass capacitor on the output/cathode pin. When doing this, be sure that the capacitance is within the stability criteria shown in Figure 5-12. To not exceed the maximum cathode current, ensure the supply voltage is current limited. Also, be sure to limit the current being driven into the Ref pin, as not to exceed it's absolute maximum rating. For applications shunting high currents, pay attention to the cathode and anode trace lengths, adjusting the width of the traces to have the proper current density.

10 Layout

10.1 Layout Guidelines

Bypass capacitors must be placed as close to the part as possible. Current-carrying traces need to have widths appropriate for the amount of current they are carrying; in the case of the TL1431, these currents are low.

10.2 Layout Example

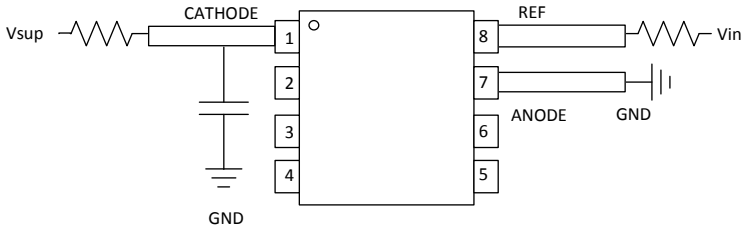


Figure 10-1. PW Package Layout Example

11 Device and Documentation Support

11.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Understanding Stability Boundary Conditions Charts in TL431, TL432 Data Sheet* (SLVA482)
- *Setting the Shunt Voltage on an Adjustable Shunt Regulator* (SLVA445)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision N (October 2016) to Revision O (October 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated Section 8.2.2.1	16

Changes from Revision M (April 2012) to Revision N (October 2016)	Page
• Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *ORDERING INFORMATION* table; see POA at the end of the data sheet	1
• Changed $R_{\theta JA}$ for D, LP and PW package from: 97 °C/W to 114.7 °C/W (D), 140 °C/W to 157 °C/W (LP) and 149 °C/W to 172.4 °C/W (PW) in the *Thermal Information* table	4
• Changed $R_{\theta JC(bot)}$ for FK and JG package from: 5.61 °C/W to 9.5 °C/W (FK) and 14.5 °C/W to 9.5 °C/W (JG) in the *Thermal Information* table	4

Changes from Revision L (October 2007) to Revision M (April 2012)	Page
• Added Ammo option to the LP package in the ORDERING INFORMATION table	0

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9962001Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9962001Q2A TL1431MFKB
5962-9962001QPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9962001QPA TL1431M
TL1431CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1431C
TL1431CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1431C
TL1431CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1431C
TL1431CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1431C
TL1431CLP	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 70	TL1431C
TL1431CLP.A	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 70	TL1431C
TL1431CLPME3	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 70	TL1431C
TL1431CLPME3.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 70	TL1431C
TL1431CLPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 70	TL1431C
TL1431CLPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 70	TL1431C
TL1431CPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	T1431
TL1431CPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T1431
TL1431MFK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL1431MFK
TL1431MFK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL1431MFK
TL1431MFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9962001Q2A TL1431MFKB
TL1431MFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9962001Q2A TL1431MFKB
TL1431MJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL1431MJG
TL1431MJG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL1431MJG
TL1431MJGB	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9962001QPA TL1431M
TL1431MJGB.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9962001QPA TL1431M

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL1431QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1431Q
TL1431QD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1431Q
TL1431QDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1431Q
TL1431QDG4.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1431Q
TL1431QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1431Q
TL1431QDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1431Q
TL1431QDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1431Q
TL1431QDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1431Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TL1431, TL1431M :

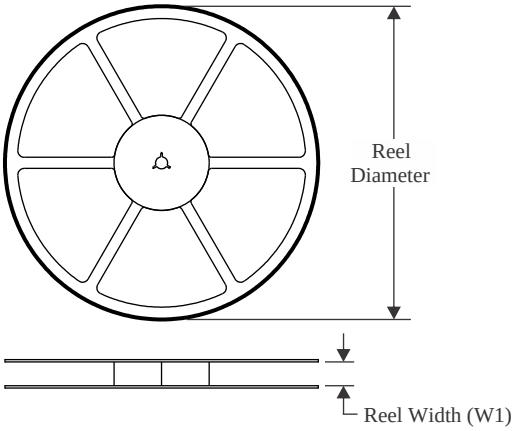
- Catalog : TL1431
- Automotive : TL1431-Q1, TL1431-Q1
- Enhanced Product : TL1431-EP, TL1431-EP
- Military : TL1431M
- Space : TL1431-SP, TL1431-SP

NOTE: Qualified Version Definitions:

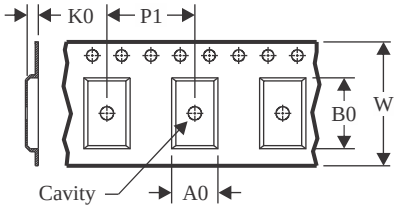
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

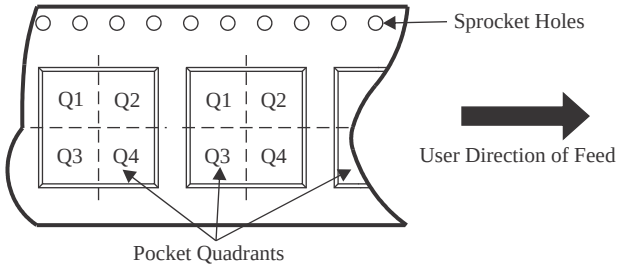


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

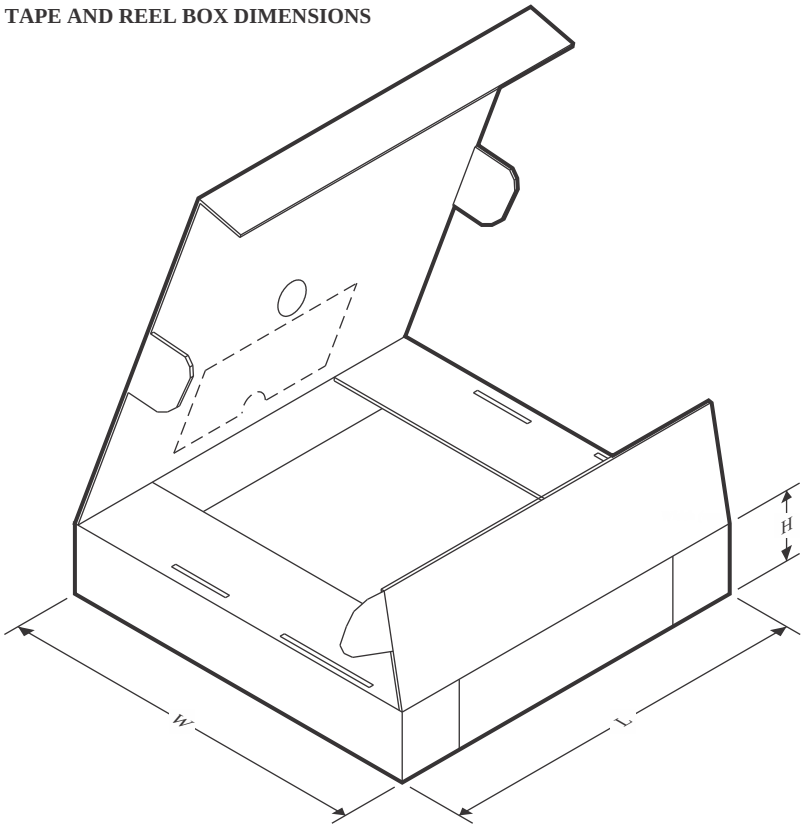
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL1431CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL1431CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL1431QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL1431QDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

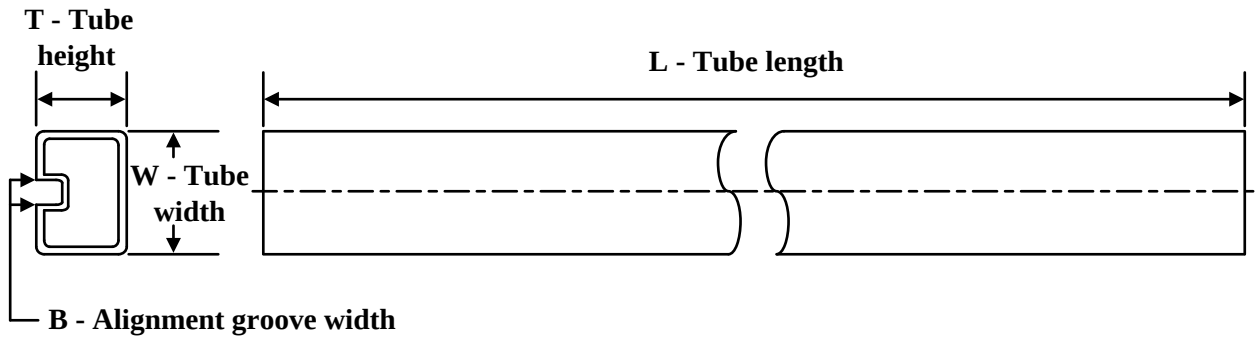
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL1431CDR	SOIC	D	8	2500	353.0	353.0	32.0
TL1431CPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TL1431QDR	SOIC	D	8	2500	353.0	353.0	32.0
TL1431QDRG4	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

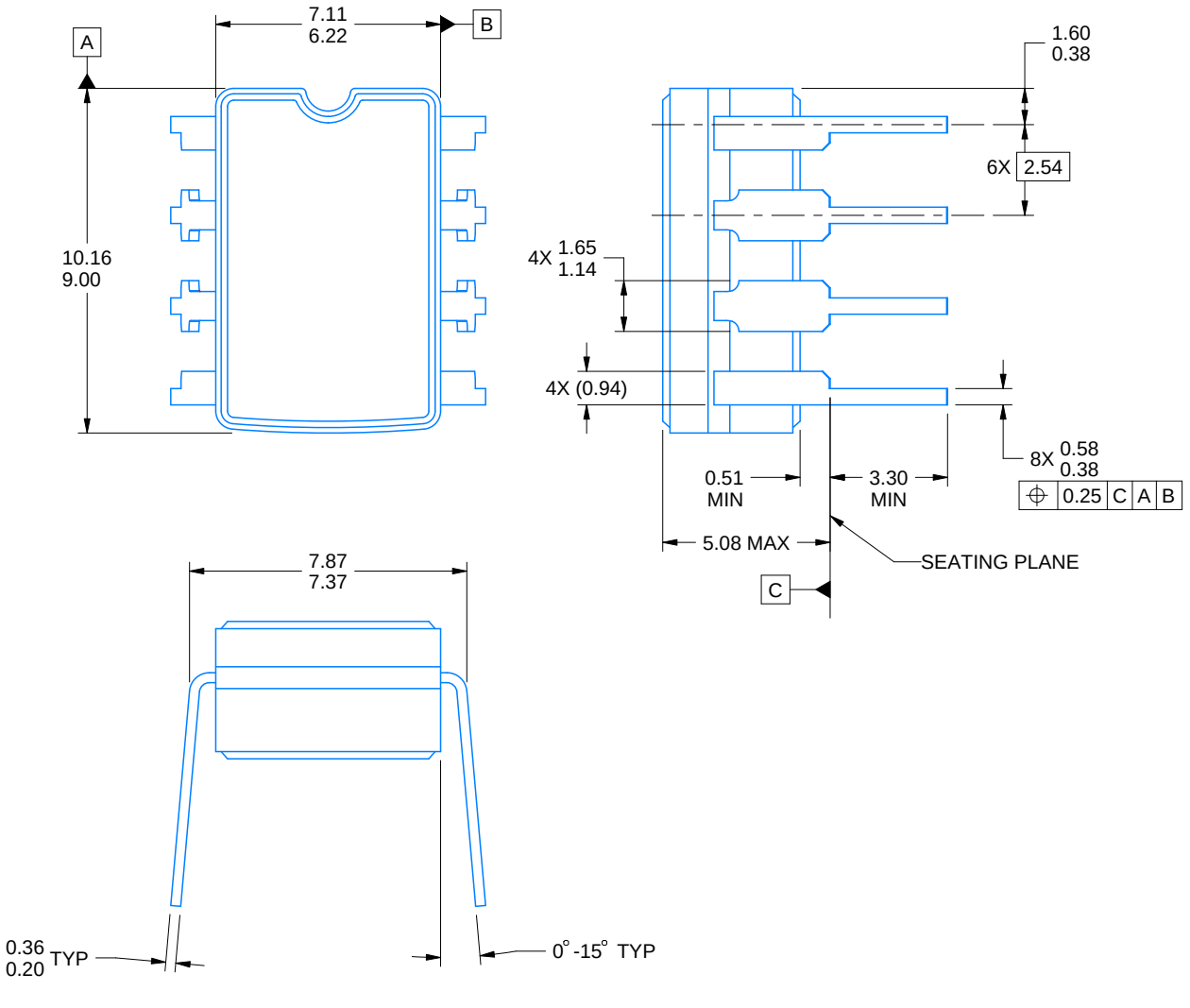
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9962001Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
TL1431CD	D	SOIC	8	75	507	8	3940	4.32
TL1431CD.A	D	SOIC	8	75	507	8	3940	4.32
TL1431MFK	FK	LCCC	20	55	506.98	12.06	2030	NA
TL1431MFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TL1431MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TL1431MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TL1431QD	D	SOIC	8	75	505.46	6.76	3810	4
TL1431QD.A	D	SOIC	8	75	505.46	6.76	3810	4
TL1431QDG4	D	SOIC	8	75	505.46	6.76	3810	4
TL1431QDG4.A	D	SOIC	8	75	505.46	6.76	3810	4

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

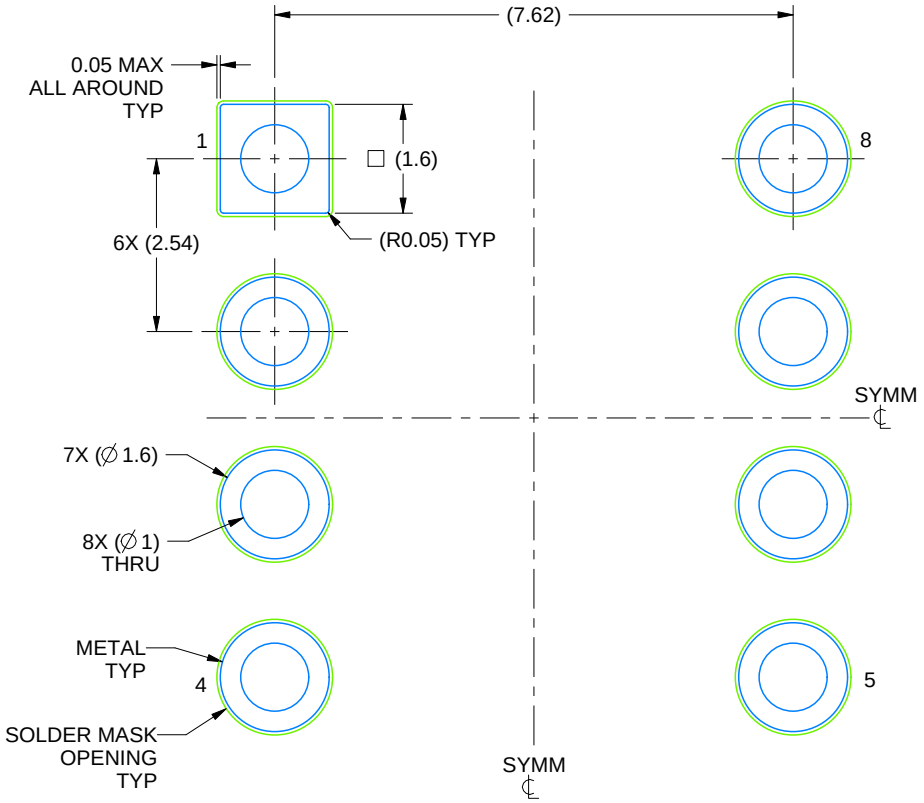
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

GENERIC PACKAGE VIEW

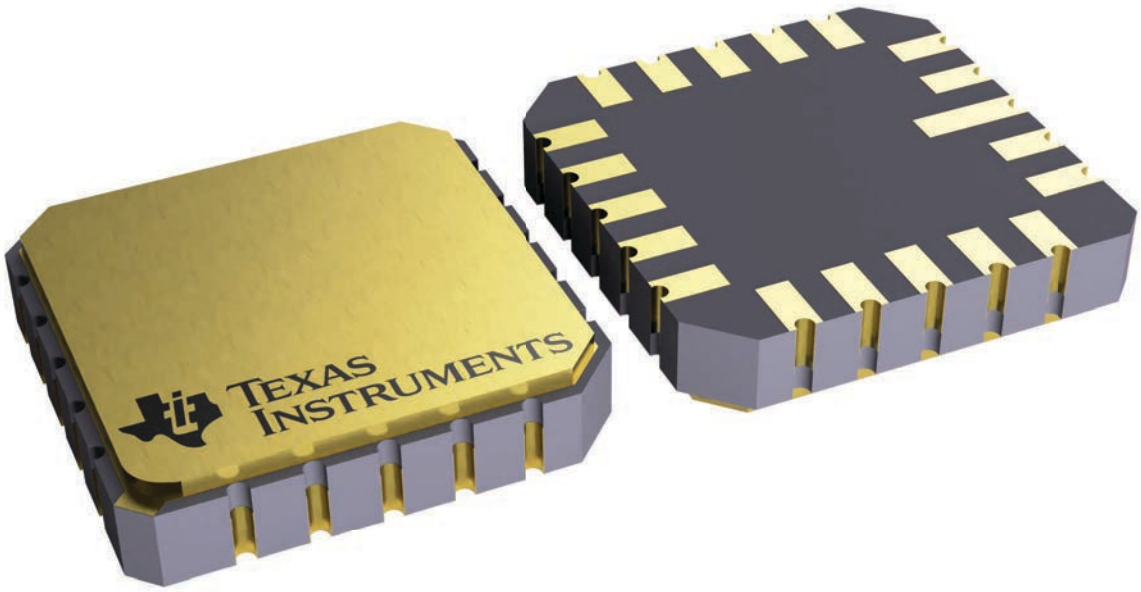
FK 20

LCCC - 2.03 mm max height

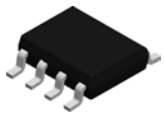
8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

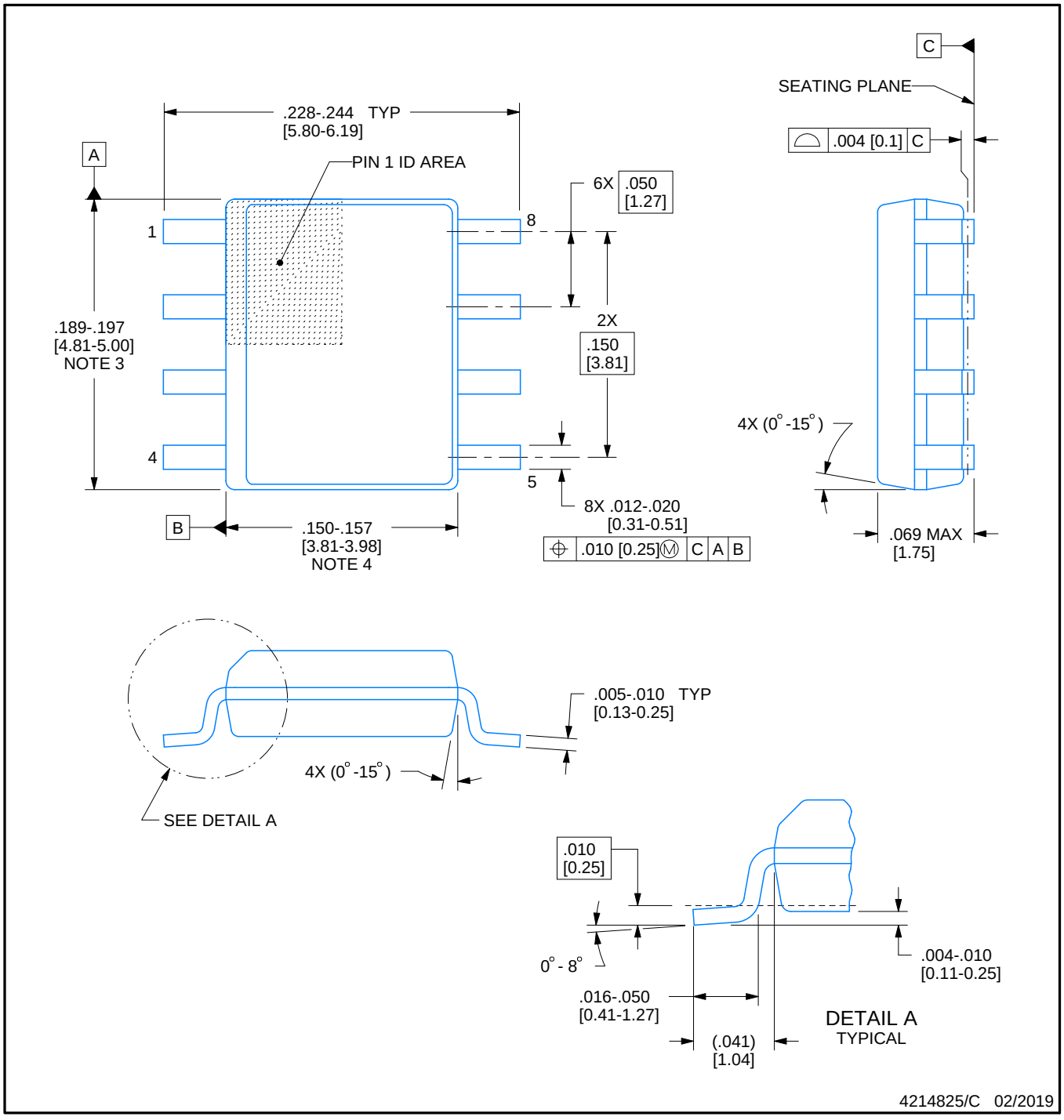


PACKAGE OUTLINE

D0008A

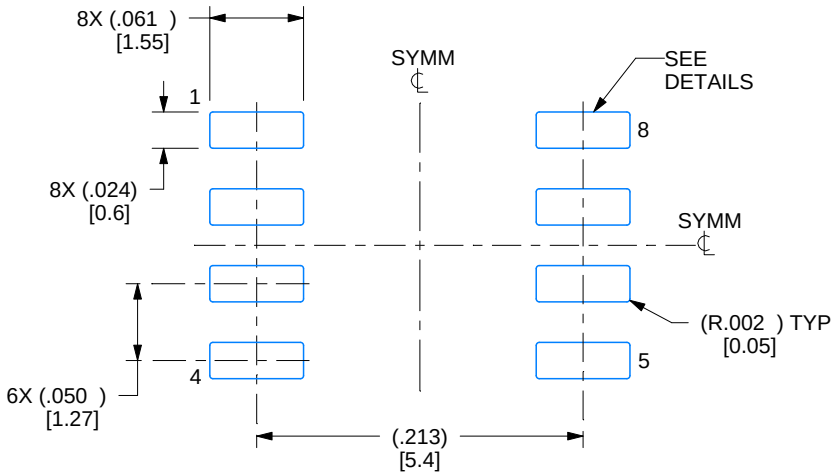
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

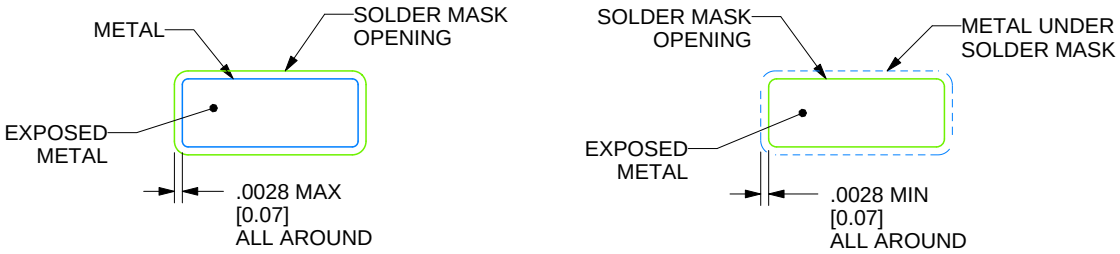


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

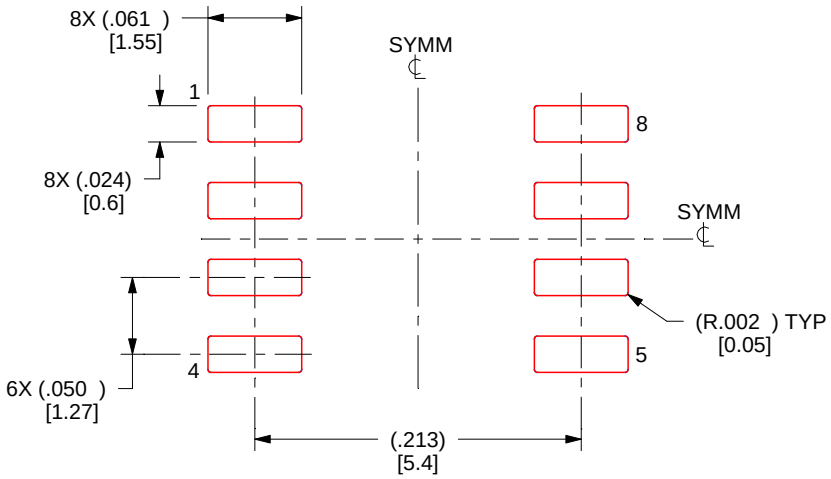
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

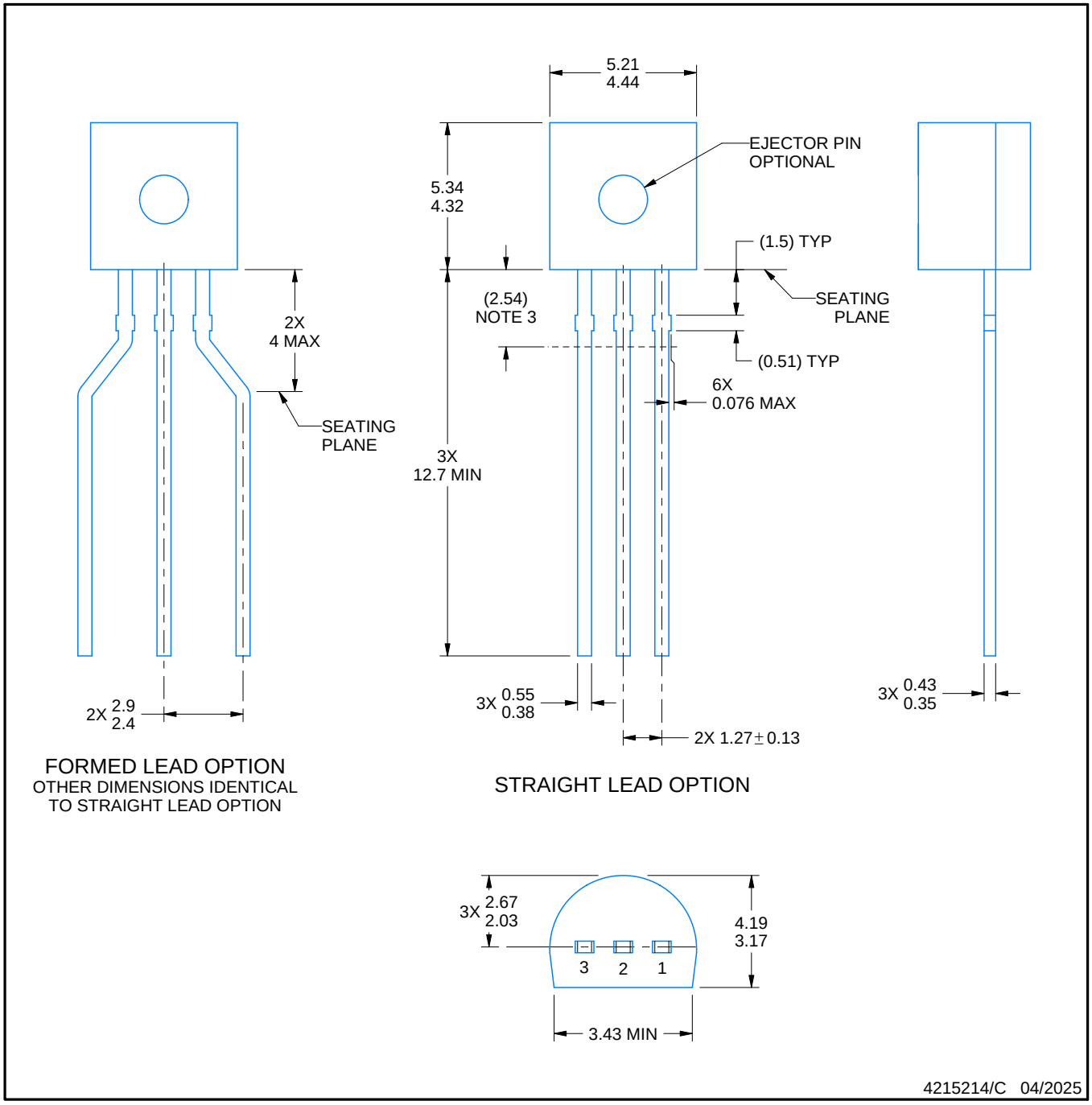
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

LP0003A

PACKAGE OUTLINE

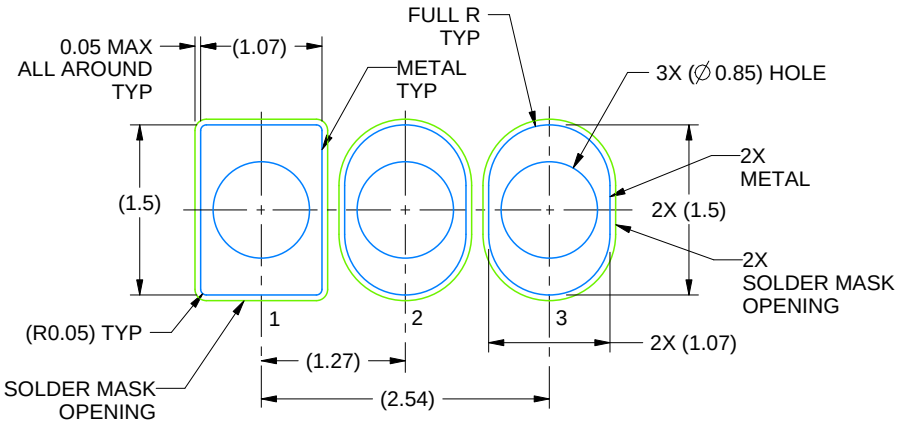
TO-92 - 5.34 mm max height

TO-92

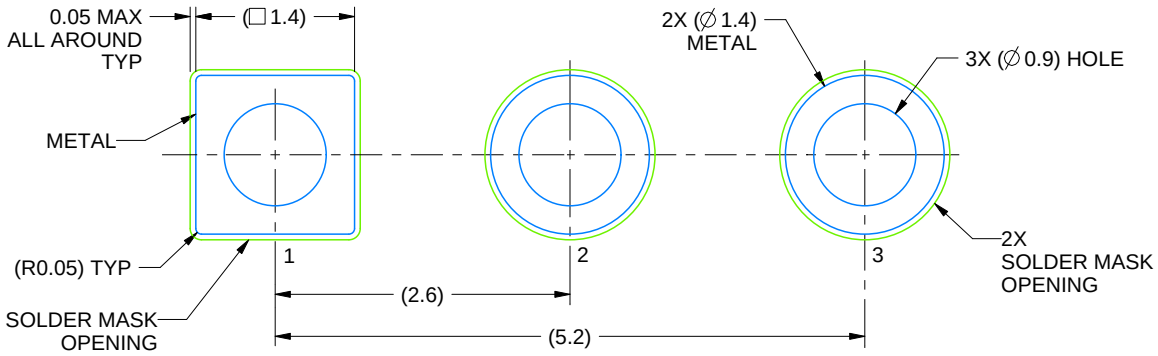


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



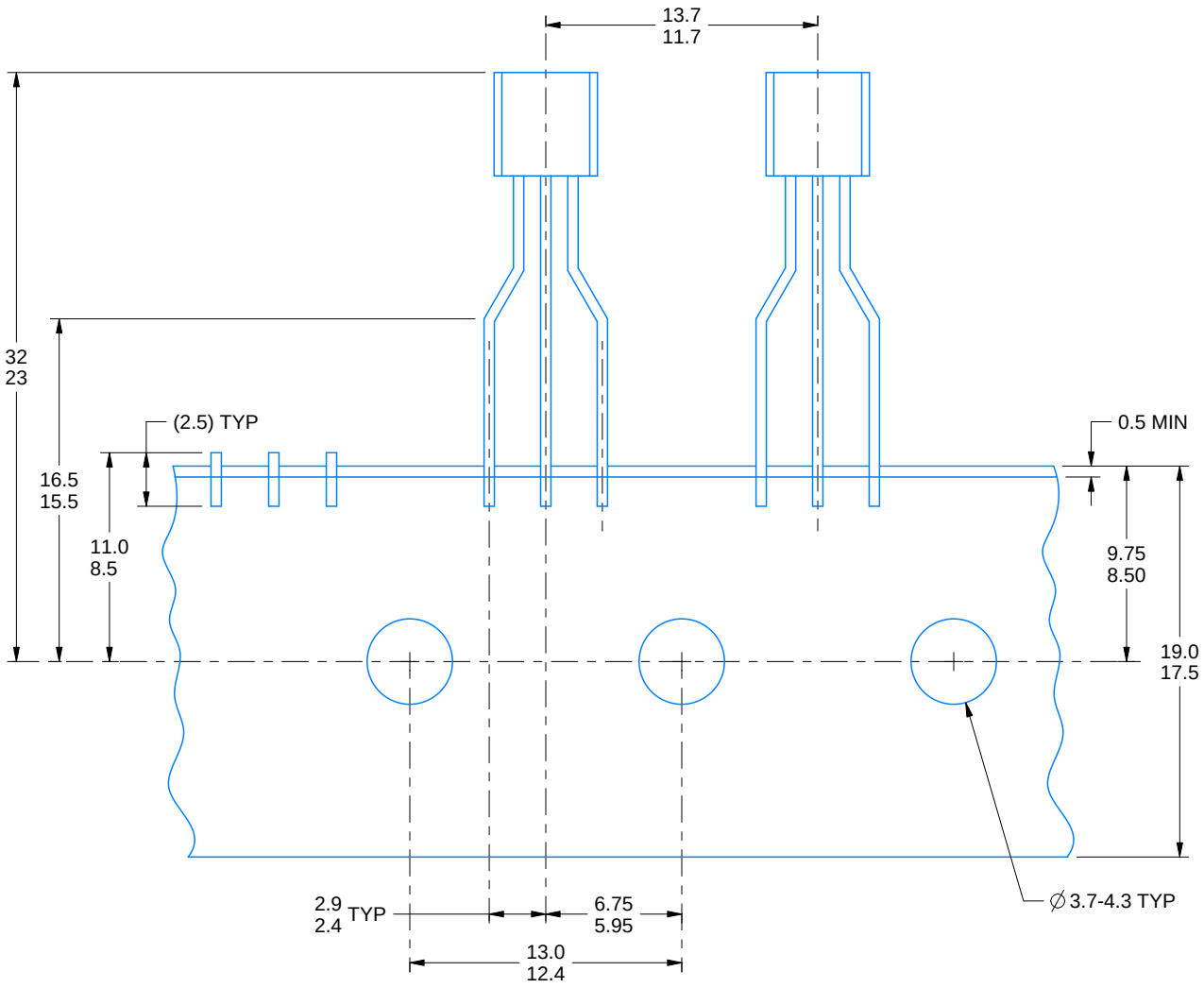
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/C 04/2025

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

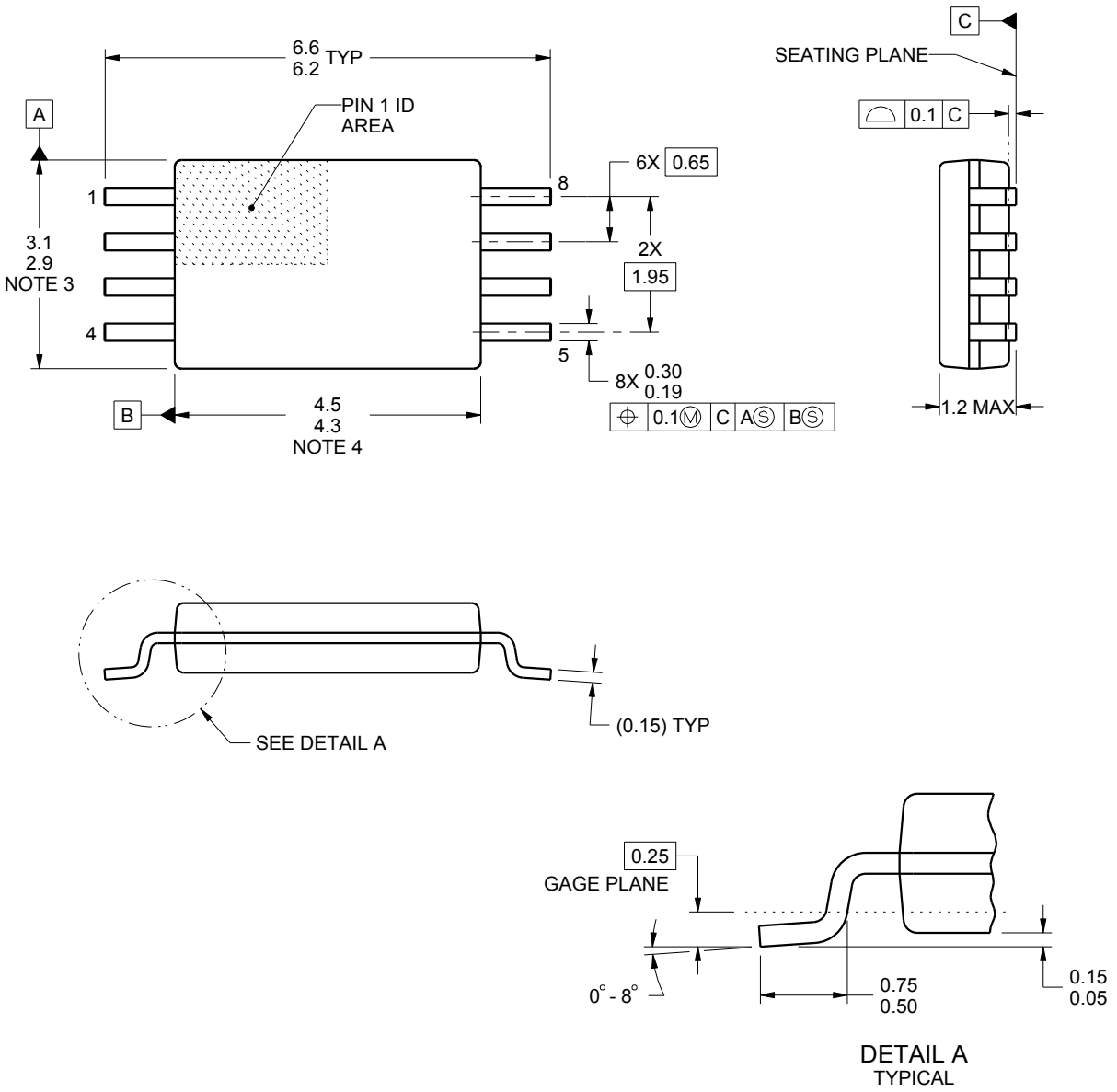
4215214/C 04/2025

PACKAGE OUTLINE

PW0008A

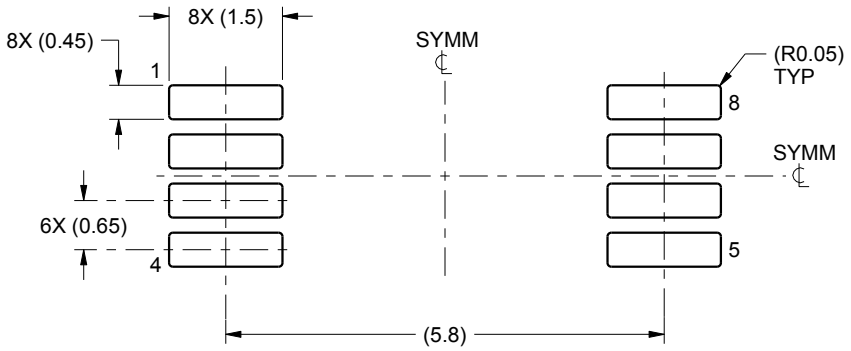
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

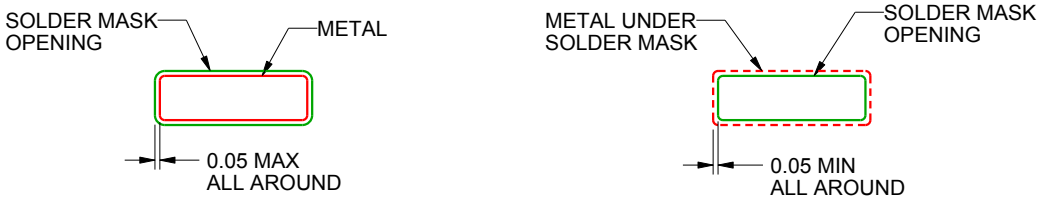


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

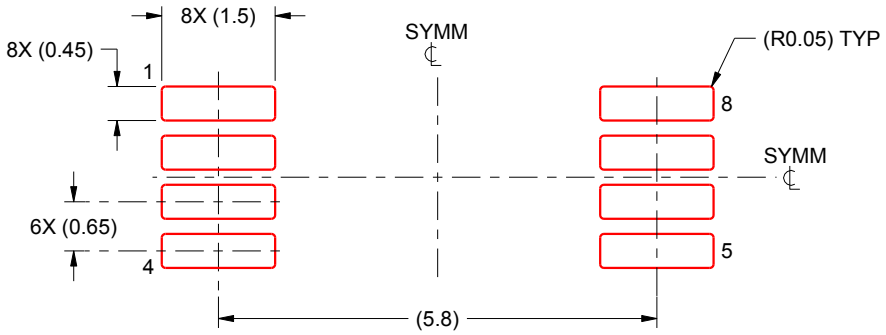


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025