TL97x Output Rail-To-Rail Very-Low-Noise Operational Amplifiers

1 Features

- Rail-to-Rail Output Voltage Swing: ±2.4 V at V_{CC} = ±2.5 V
- Very Low Noise Level: 4 nV/√Hz
- Ultra-Low Distortion: 0.003%
- High Dynamic Features: 12 MHz, 5 V/µs
- Operating Range: 2.7 V to 12 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model
  - 1500-V Charged-Device Model

2 Applications

- Portable Equipment
  - Music Players
  - Tablets
  - Cell Phones
- Instrumentation and Sensors
- Professional Audio Circuits

3 Description

The TL97x family of single, dual, and quad operational amplifiers operates at voltages as low as ±1.35 V and features output rail-to-rail signal swing. The TL97x boast characteristics that make them particularly well suited for portable and battery-supplied equipment. Very low noise and low distortion characteristics make them ideal for audio preamplification.

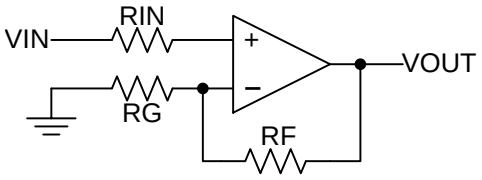
The TL971 is housed in the space-saving 5-pin SOT-23 package, which simplifies board design because of the ability to be placed anywhere (outside dimensions are 2.8 mm × 2.9 mm).

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
TL971	SOIC (8)	4.90 mm × 3.90 mm
	SOT-23 (5)	2.80 mm × 2.90 mm
TL972	MSOP (8)	3.00 mm × 3.00 mm
	PDIP (8)	9.60 mm × 6.40 mm
	SOIC (8)	4.90 mm × 3.90 mm
	TSSOP (8)	3.00 mm × 4.40 mm
TL974	PDIP (14)	19.30 mm × 6.40 mm
	SOIC (14)	8.60 mm × 3.90 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



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5 Revision History

Changes from Revision G (May 2012) to Revision H — **Page**

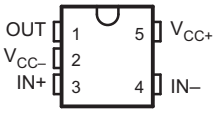
- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table. ... 1

Changes from Revision F (December 2009) to Revision G — **Page**

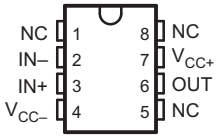
- Changed slew rate MIN value. ... 5

6 Pin Configuration and Functions

TL971...DBV PACKAGE
(TOP VIEW)

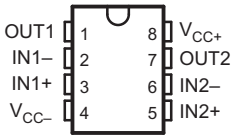


TL971...D PACKAGE
(TOP VIEW)

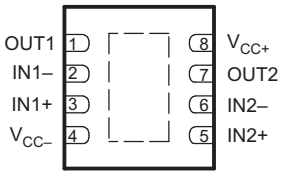


NC – No internal connection

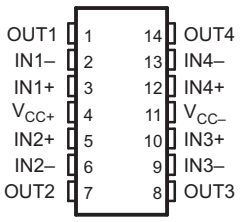
TL972...D, DGK, P, OR PW PACKAGE
(TOP VIEW)



TL972...DRG PACKAGE
(TOP VIEW)



TL974...D, N, OR PW PACKAGE
(TOP VIEW)



Pin Functions

PIN						TYPE	DESCRIPTION
NAME	TL971	TL971	TL972		TL974		
	DBV	D	D, DGK, P, PW	DRG	D, N, PW		
IN+	3	3	—	—	—	I	Noninverting input
IN–	4	2	—	—	—	I	Inverting input
IN1+	—	—	3	3	3	I	Noninverting input
IN1–	—	—	2	2	2	I	Inverting input
IN2+	—	—	5	5	5	I	Noninverting input
IN2–	—	—	6	6	6	I	Inverting input
IN3+	—	—	—	—	10	I	Noninverting input
IN3–	—	—	—	—	9	I	Inverting input
IN4+	—	—	—	—	12	I	Noninverting input
IN4–	—	—	—	—	13	I	Inverting input
NC	—	1 5 8	—	—	—	—	No Connect
OUT	1	6	—	—	—	O	Output
OUT1	—	—	1	1	1	O	Output
OUT2	—	—	7	7	7	O	Output
OUT3	—	—	—	—	8	O	Output
OUT4	—	—	—	—	14	O	Output
VCC+	5	7	8	8	4	-	Positive supply
VCC–	2	4	4	4	11	-	Negative supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	2.7	15	V
V_{ID}	Differential input voltage(2)		±1 V	V
V_{IN}	Input voltage range(3)	V_{CC-} – 0.3	V_{CC+} + 0.3	V
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Differential voltages for the noninverting input terminal are with respect to the inverting input terminal.
(3) The input and output voltages must never exceed V_{CC} + 0.3 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	12	V
V_{ICM}	Common-mode input voltage	V_{CC-} + 1.15	V_{CC+} – 1.15	V
T_A	Operating free-air temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TL971		TL972					TL974			UNIT
		D(2)	DBV(2)	D(2)	DGK(3)	DRG(3)	P(2)	PW(2)	D(2)	N(2)	PW(2)	
		8 PINS	5 PINS	8 PINS					14 PINS			
$R_{\theta JA}$	Package thermal impedance, junction to free air	97	206	97	172	44	85	149	86	80	113	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).
(2) Package thermal impedance is calculated in accordance with JESD 51-7.
(3) Package thermal impedance is calculated in accordance with JESD 51-5.

7.5 Electrical Characteristics

V_{CC+} = 2.5 V, $V_{CC–}$ = –2.5 V, full-range T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C		1	4	mV
			Full range			6	
αV_{IO}	Input offset voltage drift	V_{ICM} = 0 V, V_O = 0 V	25°C		5		µV/°C
I_{IO}	Input offset current	V_{ICM} = 0 V, V_O = 0 V	25°C		10	150	nA
I_{IB}	Input bias current	V_{ICM} = 0 V, V_O = 0 V	25°C		200	750	nA
			Full range			1000	
V_{ICM}	Common-mode input voltage		25°C	–1.35		1.35	V
CMRR	Common-mode rejection ratio	V_{ICM} = ±1.35 V	25°C	60	85		dB
SVR	Supply-voltage rejection ratio	V_{CC} = ±2 V to ±3 V	25°C	60	70		dB
A_{VD}	Large-signal voltage gain	R_L = 2 kΩ	25°C	70	80		dB
V_{OH}	High-level output voltage	R_L = 2 kΩ	25°C	2	2.4		V
V_{OL}	Low-level output voltage	R_L = 2 kΩ	25°C		–2.4	–2	V
I_{source}	Output source current		25°C	1.2	1.4		mA
		V_{OUT} = ±2.5 V	Full range	1			
I_{sink}	Output sink current		25°C	50	80		mA
		V_{OUT} = ±2.5 V	Full range	25			
I_{CC}	Supply current (per amplifier)	Unity gain, No load	25°C		2	2.8	mA
			Full range			3.2	
GBWP	Gain bandwidth product	f = 100 kHz, R_L = 2 kΩ, C_L = 100 pF	25°C	8.5	12		MHz
SR	Slew rate	A_V = 1, V_{IN} = ±1 V	25°C	2.8	5		V/µs
			Full range	2.8			
Φm	Phase margin at unity gain	R_L = 2 kΩ, C_L =100 pF	25°C		60		°
Gm	Gain margin	R_L = 2 kΩ, C_L =100 pF	25°C		10		dB
V_n	Equivalent input noise voltage	f = 100 kHz	25°C		4		nV/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = –1, R_L = 10 kΩ	25°C		0.003		%

7.6 Typical Characteristics

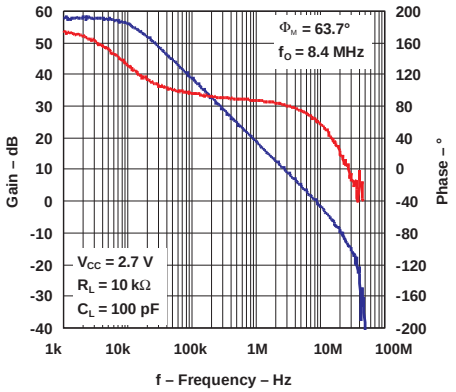


Figure 1. Gain And Phase vs Frequency

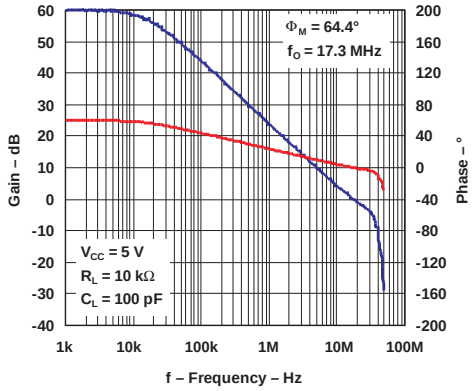


Figure 2. Gain And Phase vs Frequency

Typical Characteristics (continued)

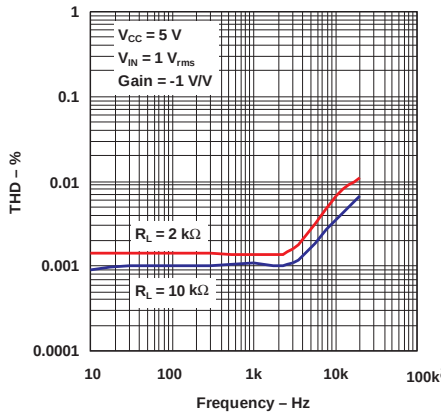


Figure 3. Total Harmonic Distortion vs Frequency

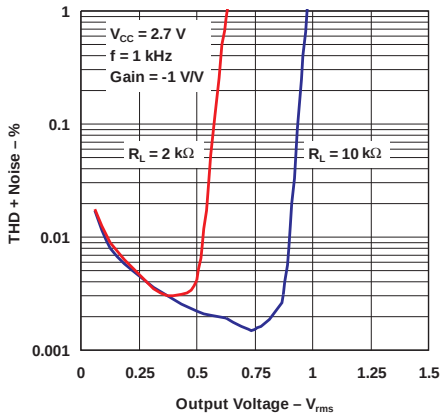


Figure 4. Total Harmonic Distortion + Noise vs Output Voltage

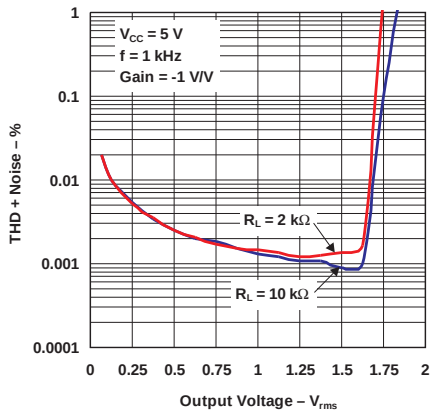


Figure 5. Total Harmonic Distortion + Noise vs Output Voltage

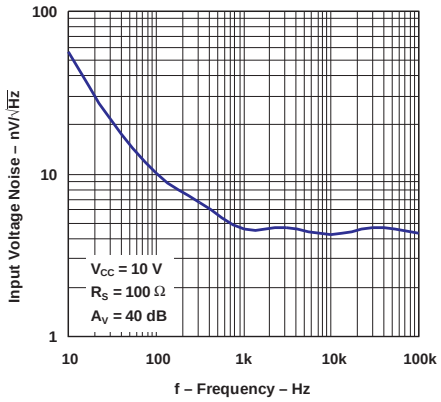


Figure 6. Input Voltage Noise vs Frequency

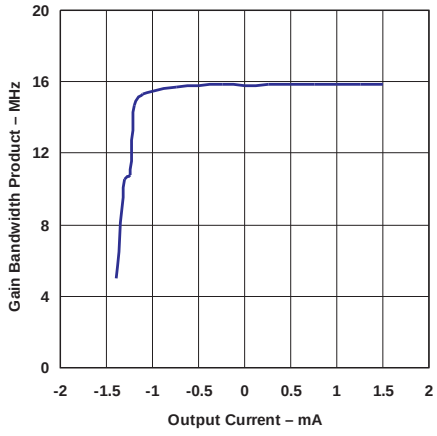


Figure 7. Gain Bandwidth Product vs Output Current

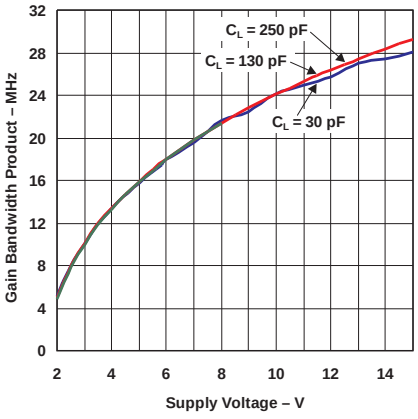


Figure 8. Gain Bandwidth Product vs Supply Voltage

Typical Characteristics (continued)

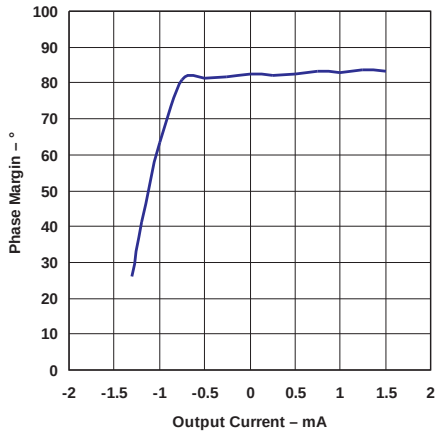


Figure 9. Phase Margin vs Output Current

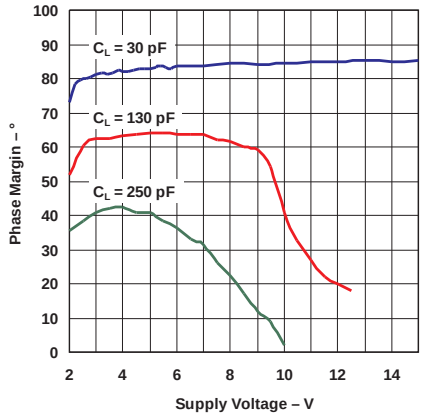


Figure 10. Phase Margin vs Supply Voltage

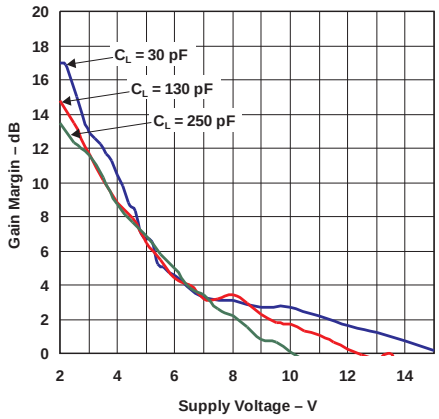


Figure 11. Gain Margin vs Supply Voltage

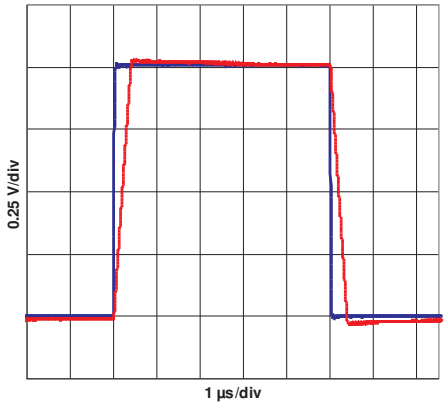


Figure 12. Input Response

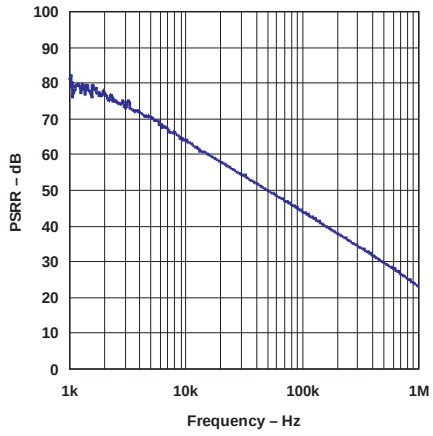


Figure 13. Power-Supply Ripple Rejection vs Frequency

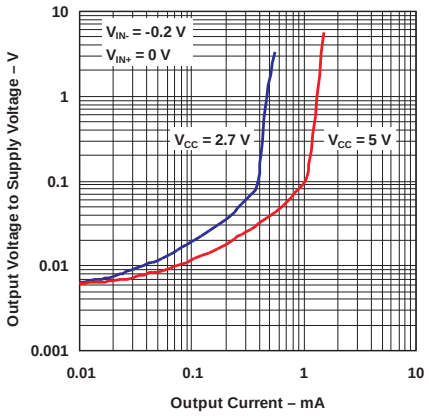


Figure 14. Output Voltage vs Output Current

Typical Characteristics (continued)

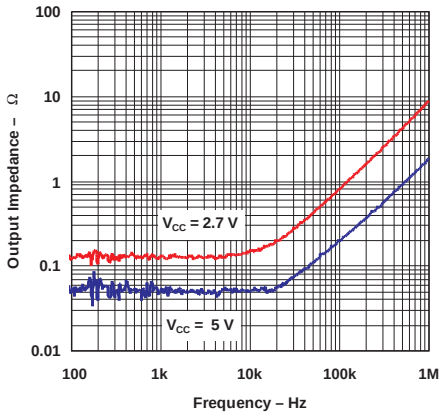


Figure 15. Output Impedance vs Frequency

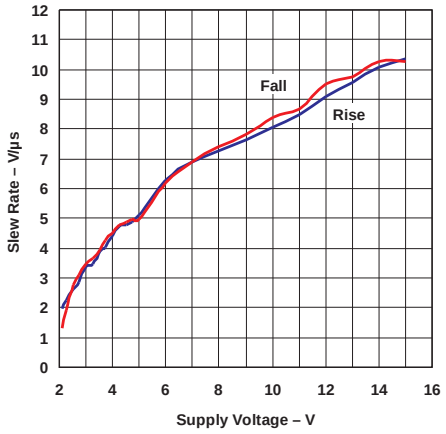


Figure 16. Slew Rate vs Supply Voltage

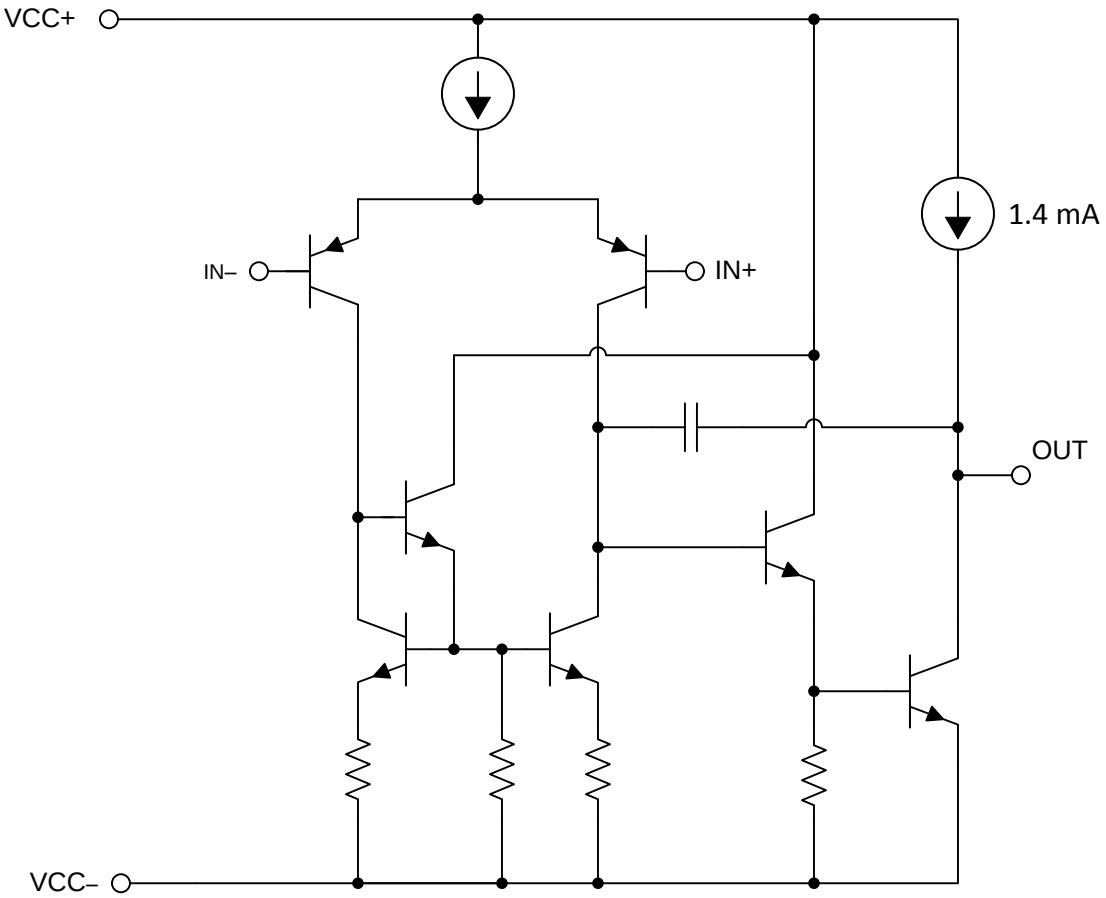
8 Detailed Description

8.1 Overview

The TL97x family of operational amplifiers operates at voltages as low as ±1.35 V and features output rail-to-rail signal swing. The TL97x boast characteristics that make them particularly well suited for portable and battery-supplied equipment. Very low noise and low distortion characteristics make them ideal for audio preamplification. The TL97x family comes in single, dual, and quad operational amplifier packages of varying sizes.

The TL971 is housed in the space-saving 5-pin SOT-23 package, which simplifies board design because of the ability to be placed anywhere (outside dimensions are 2.8 mm × 2.9 mm).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The TL97x devices have a 5 V/μs slew rate.

8.3.2 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. The TL97x devices have a 12-MHz unity-gain bandwidth.

Feature Description (continued)

8.3.3 Low Total Harmonic Distortion

Harmonic distortions to an audio signal are created by electronic components in a circuit. Total harmonic distortion (THD) is a measure of harmonic distortions accumulated by a signal in an audio system. The TL97x devices have a very low THD of 0.003% meaning that they will add little harmonic distortion when used in audio signal applications.

8.3.4 Operating Voltage

The TL97x devices are fully specified and ensured for operation from 2.7 V to 12 V. In addition, many specifications apply from –40°C to 125°C.

8.4 Device Functional Modes

The TL97x devices are powered on when the supply is connected. Each of these devices can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Typical Application

The voltage follower configuration of the operational amplifier is used for applications where a weak signal is used to drive a relatively high current load. This circuit is also called a buffer amplifier or unity gain amplifier. The inputs of an operational amplifier have a very high resistance which puts a negligible current load on the voltage source. The output resistance of the operational amplifier is almost negligible, so it can provide as much current as necessary to the output load.

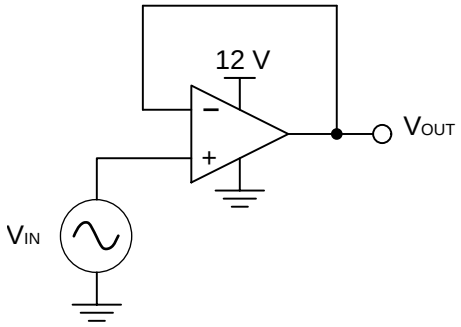


Figure 17. Voltage follower schematic

9.1.1 Design Requirements

- Input at positive Terminal
- Output range of 0 V to 12 V
- Input range of 0 V to 12 V
- Short-circuit feedback to negative input for unity gain

9.1.2 Detailed Design Procedure

9.1.2.1 Output Voltage Swing

The output voltage of an operational amplifier is limited by its internal circuitry to some level below the supply rails. For this amplifier, the output voltage must be within ±12 V.

9.1.2.2 Supply and Input Voltage

For correct operation of the amplifier, neither input must be higher than the recommended positive supply rail voltage or lower than the recommended negative supply rail voltage. The chosen amplifier must be able to operate at the supply voltage that accommodates the inputs. Because the input for this application goes up to 12 V, the supply voltage must be 15 V. Using a negative voltage on the lower rail rather than ground, allows the amplifier to maintain linearity for the full range of inputs.

Typical Application (continued)

9.1.3 Application Curves for Output Characteristics

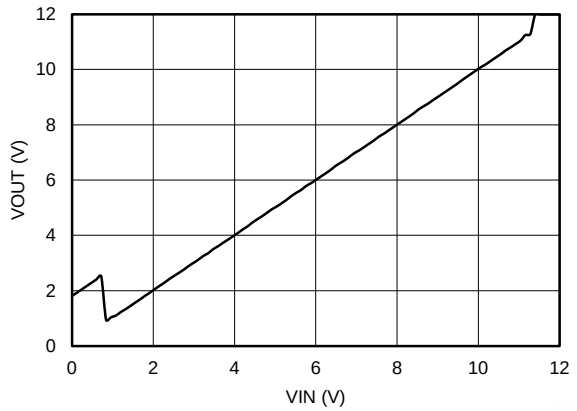


Figure 18. Output Voltage vs Input Voltage

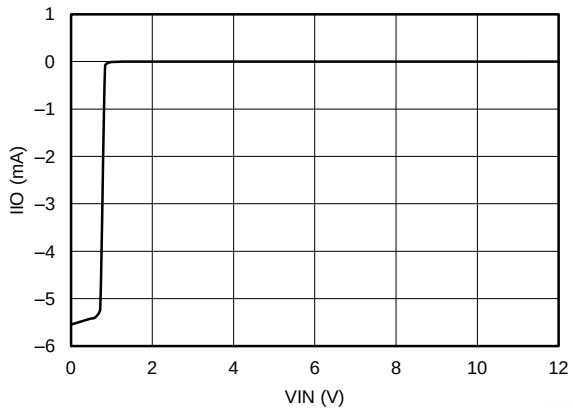


Figure 19. Current Drawn by Input of Voltage Follower (I_{IO}) vs Input Voltage

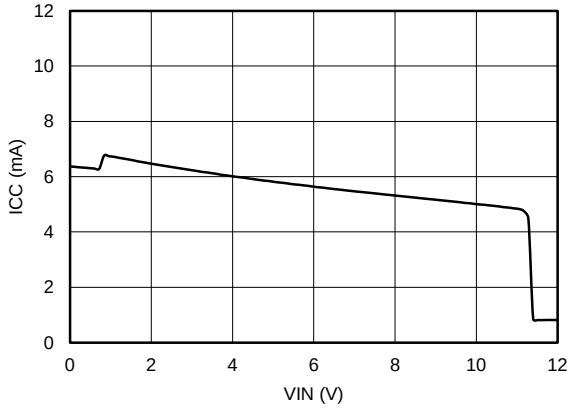


Figure 20. Current Dawn from Supply (I_{CC}) vs Input Voltage

10 Power Supply Recommendations

The TL97x devices are specified for operation from 2.7 to 12 V; many specifications apply from -40 °C to 125 °C.

CAUTION

Supply voltages larger than 15 V can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to Circuit Board Layout Techniques, SLOA089.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

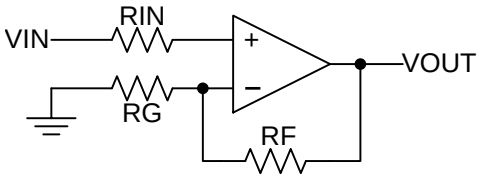


Figure 21. Operational Amplifier Schematic for Noninverting Configuration

Layout Example (continued)

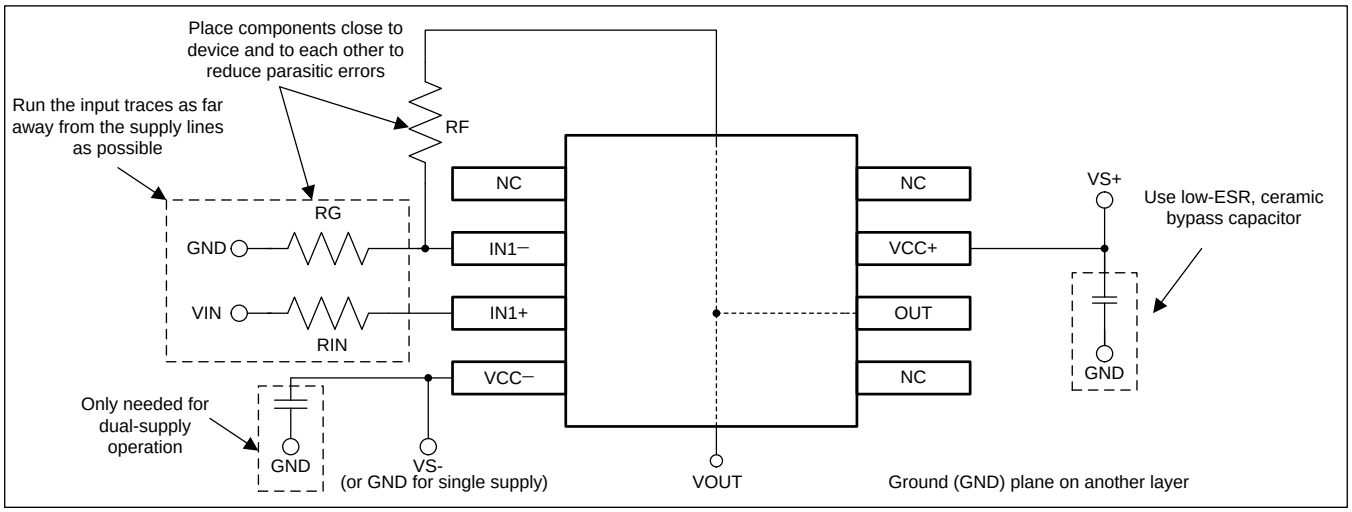


Figure 22. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TL971	Click here	Click here	Click here	Click here	Click here
TL972	Click here	Click here	Click here	Click here	Click here
TL974	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL971ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	Z971
TL971IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z971
TL971IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z971
TL971IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TL972ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	Z972
TL972IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TSA
TL972IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TSA
TL972IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972
TL972IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972
TL972IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972
TL972IDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972
TL972IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TL972IP
TL972IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TL972IP
TL972IPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	-40 to 125	
TL972IPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972
TL972IPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z972
TL974ID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL974I
TL974ID.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL974I
TL974IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL974I
TL974IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL974I
TL974IN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TL974IN
TL974IN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TL974IN
TL974INE4	Active	Production	PDIP (N) | 14	25 | TUBE	-	Call TI	Call TI	-40 to 125	
TL974IPW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z974
TL974IPW.A	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z974
TL974IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	Z974
TL974IPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z974
TL974IPWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Z974

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TL971, TL972, TL974 :

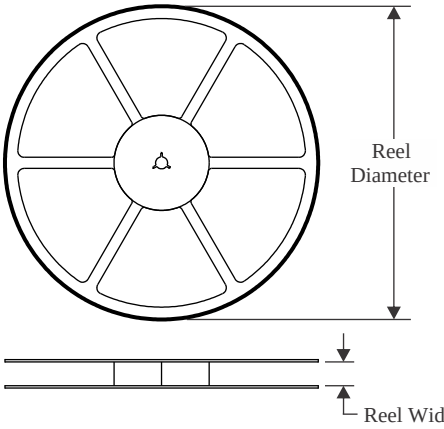
- Automotive : TL971-Q1, TL972-Q1, TL974-Q1

NOTE: Qualified Version Definitions:

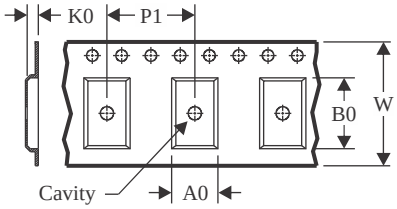
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

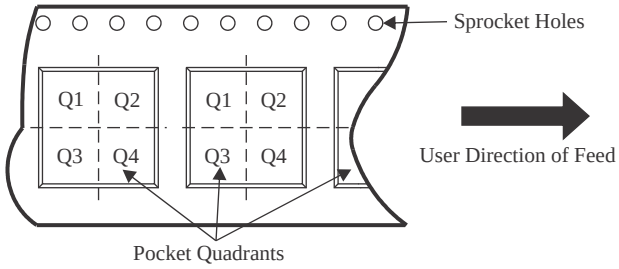


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

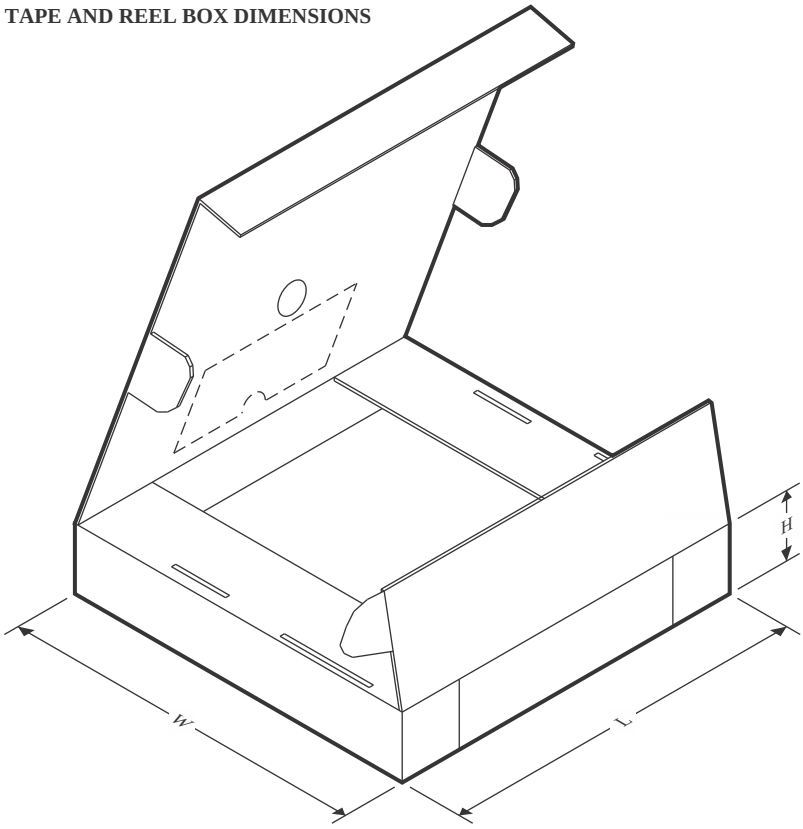
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL971IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL972IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TL972IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL972IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL972IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL972IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL974IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL974IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL974IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL974IPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL974IPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

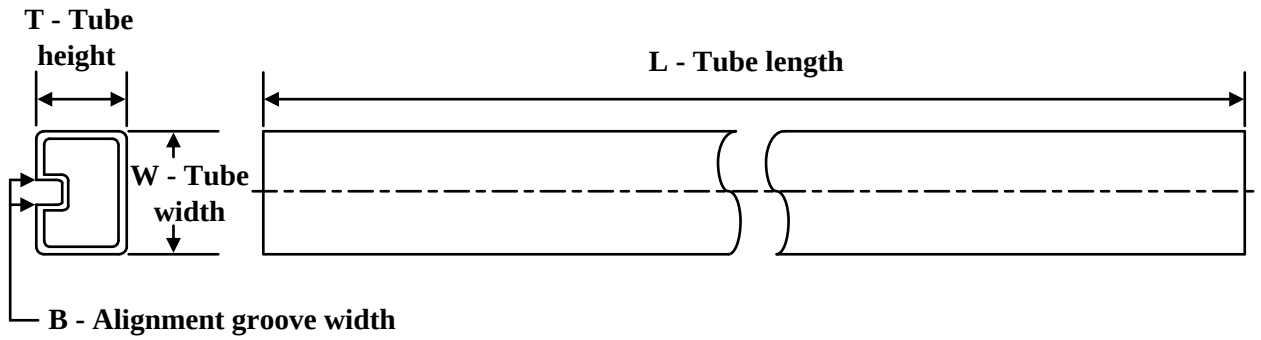
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL971IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL972IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TL972IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL972IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL972IDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TL972IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TL974IDR	SOIC	D	14	2500	353.0	353.0	32.0
TL974IDR	SOIC	D	14	2500	353.0	353.0	32.0
TL974IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL974IPWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
TL974IPWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

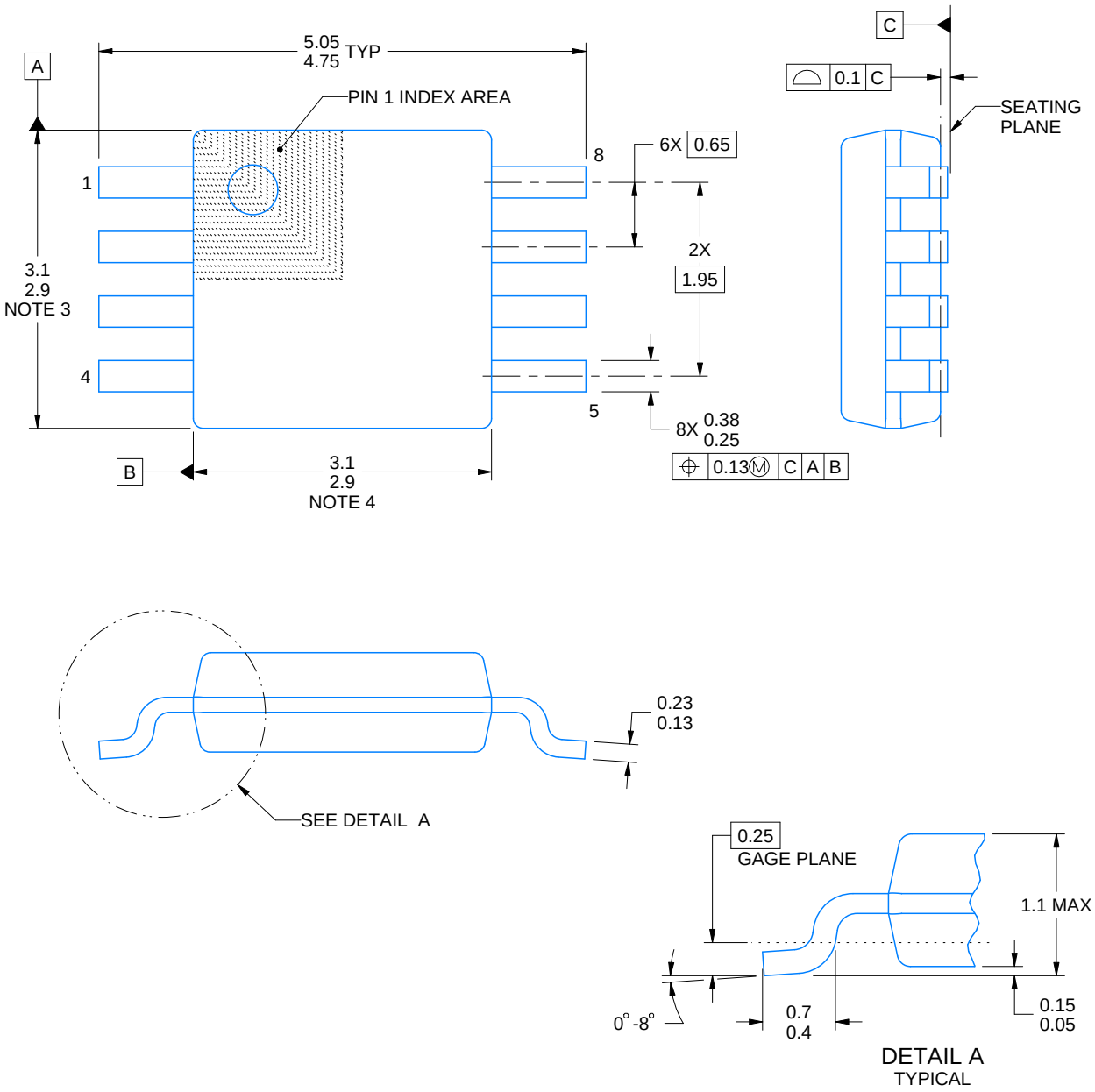
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL972IP	P	PDIP	8	50	506	13.97	11230	4.32
TL972IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL974ID	D	SOIC	14	50	507	8	3940	4.32
TL974ID.A	D	SOIC	14	50	507	8	3940	4.32
TL974IN	N	PDIP	14	25	506	13.97	11230	4.32
TL974IN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL974IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TL974IPW.A	PW	TSSOP	14	90	530	10.2	3600	3.5

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

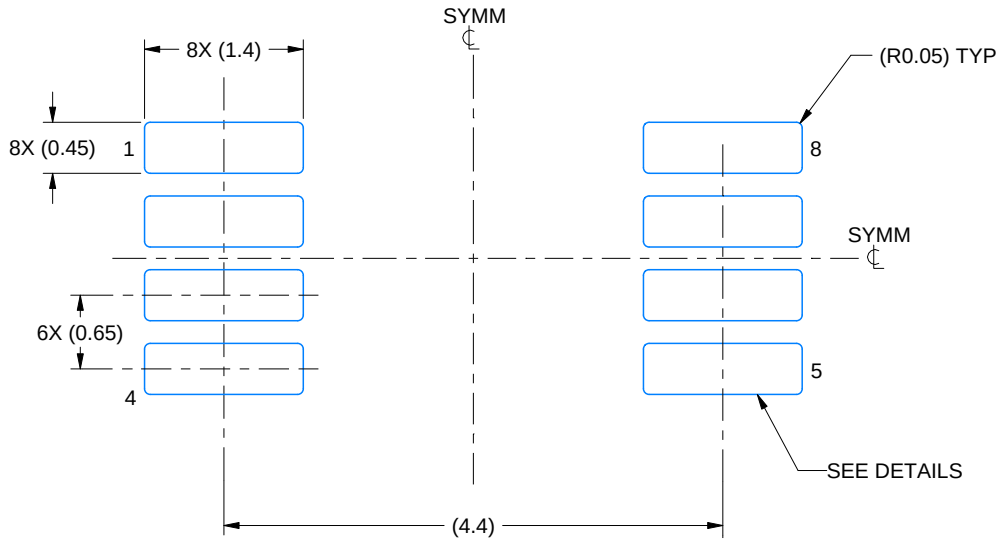
SMALL OUTLINE PACKAGE



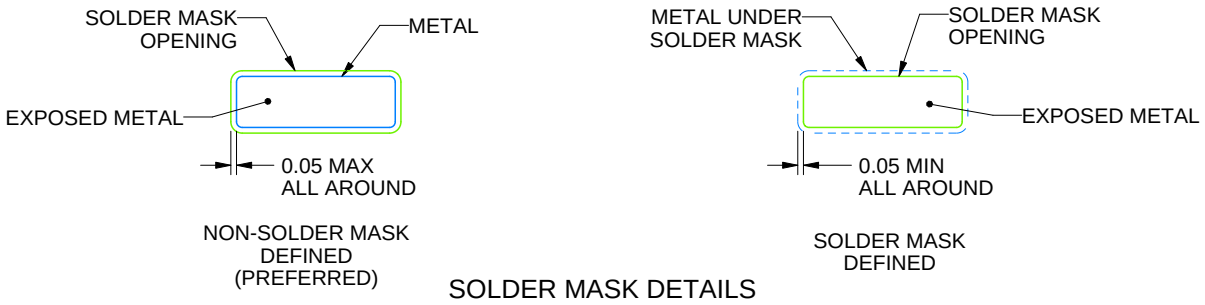
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

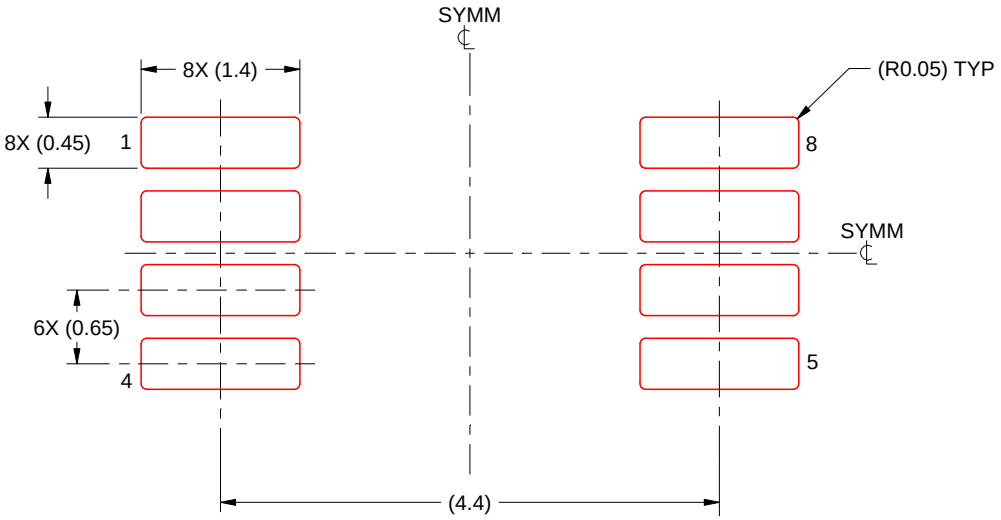


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

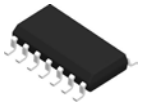


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

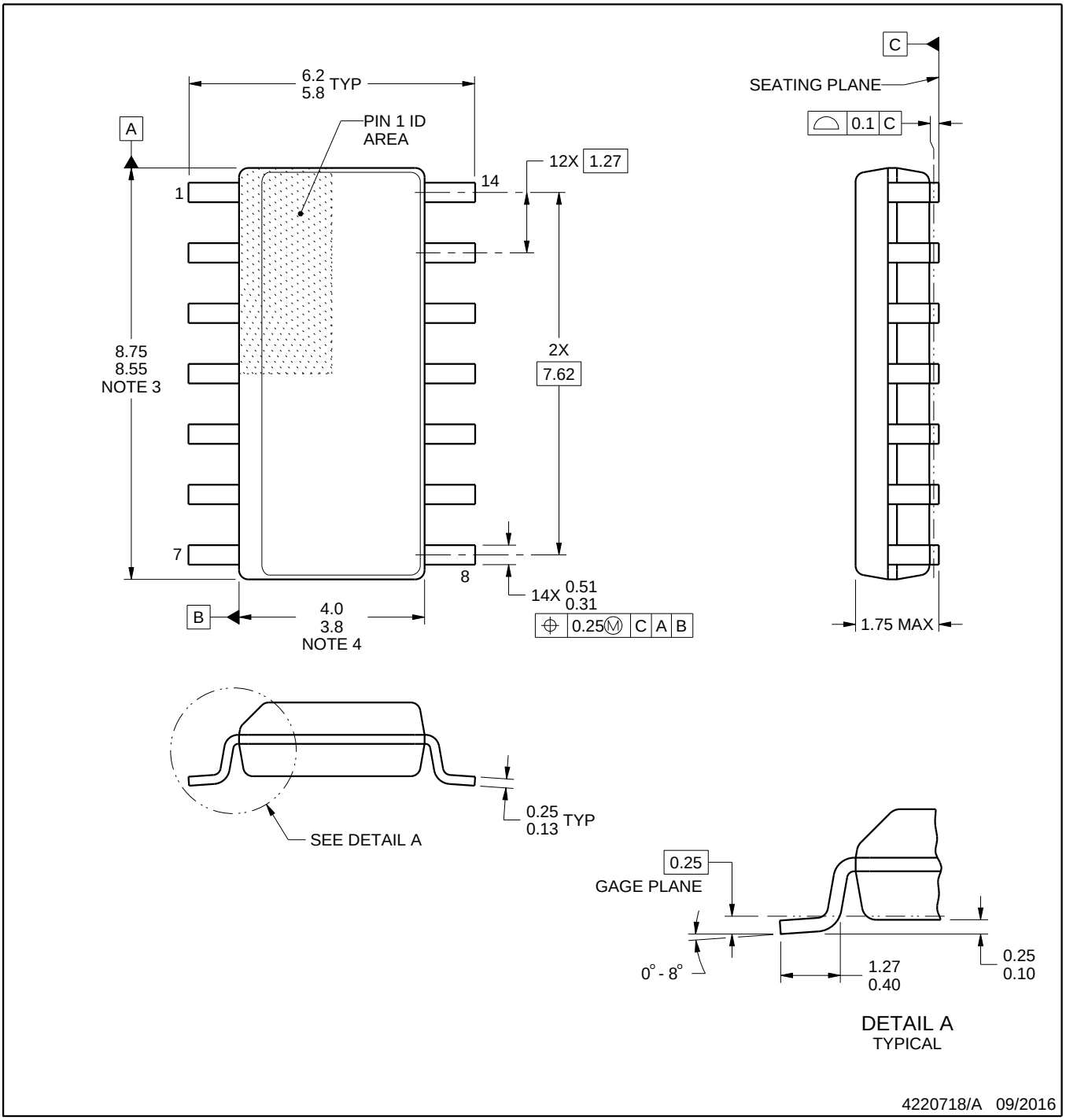


PACKAGE OUTLINE

D0014A

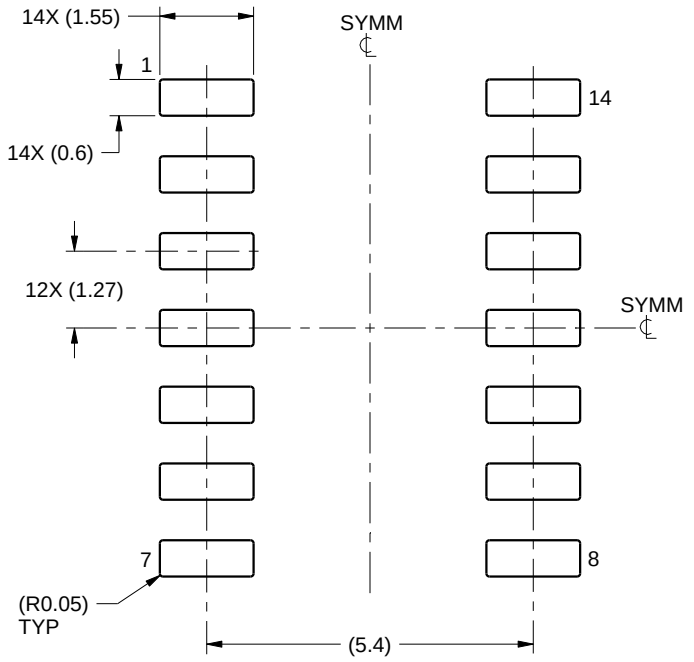
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

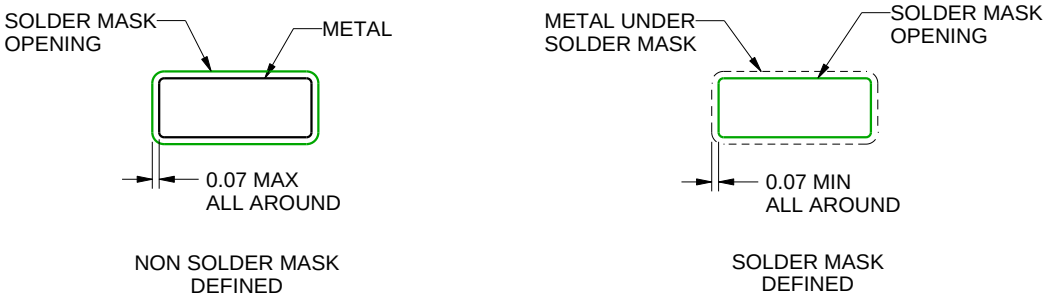


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

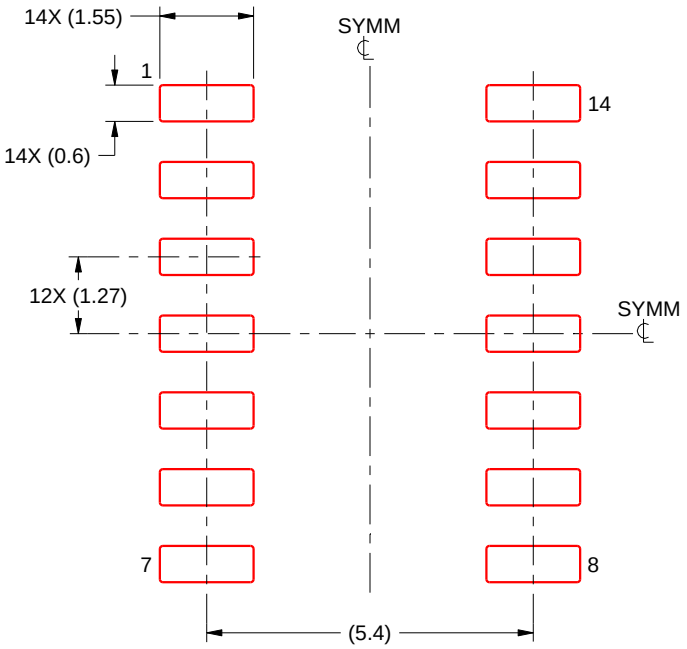
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

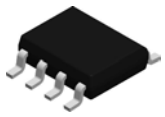


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

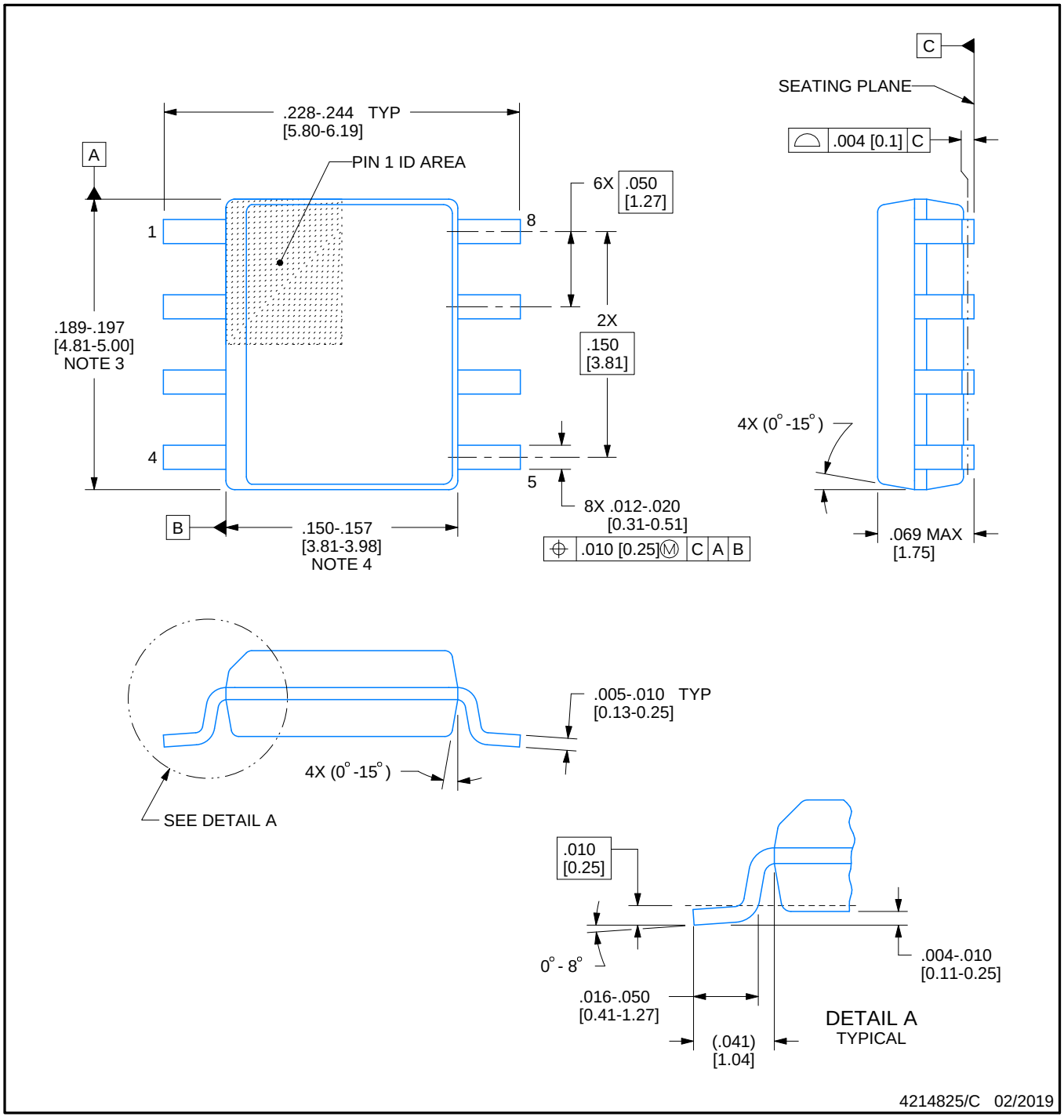


PACKAGE OUTLINE

D0008A

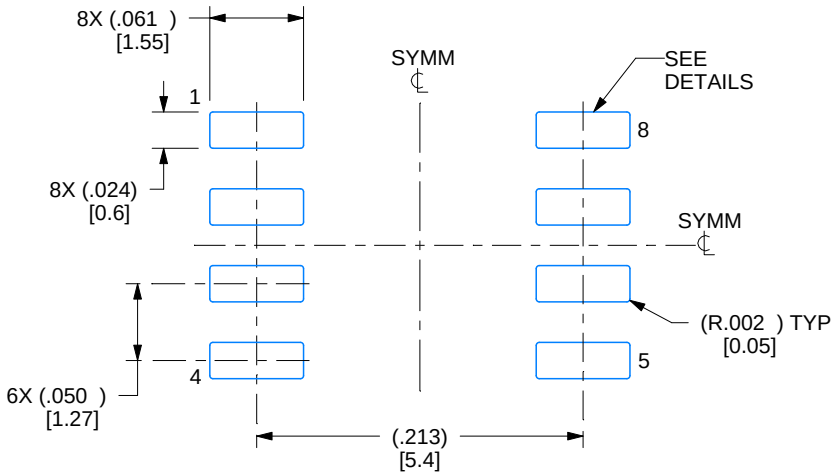
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

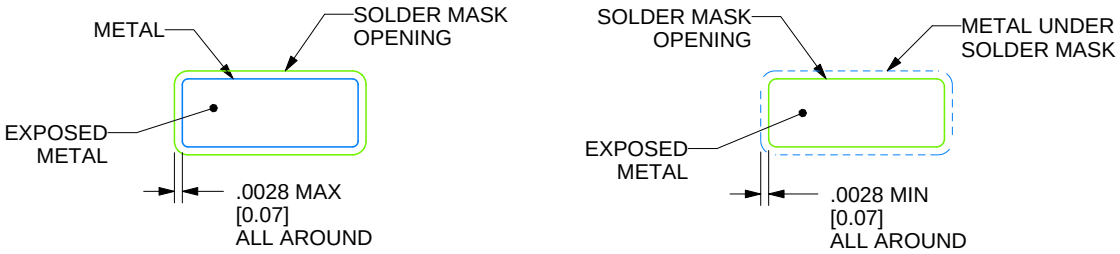


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

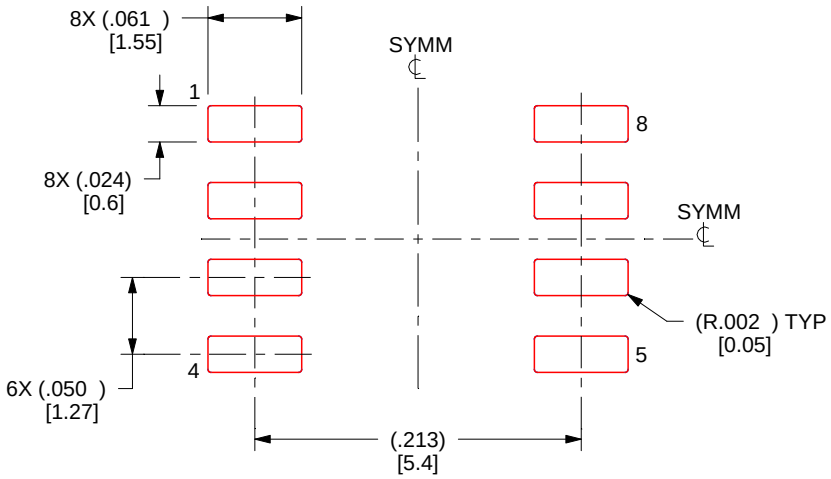
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



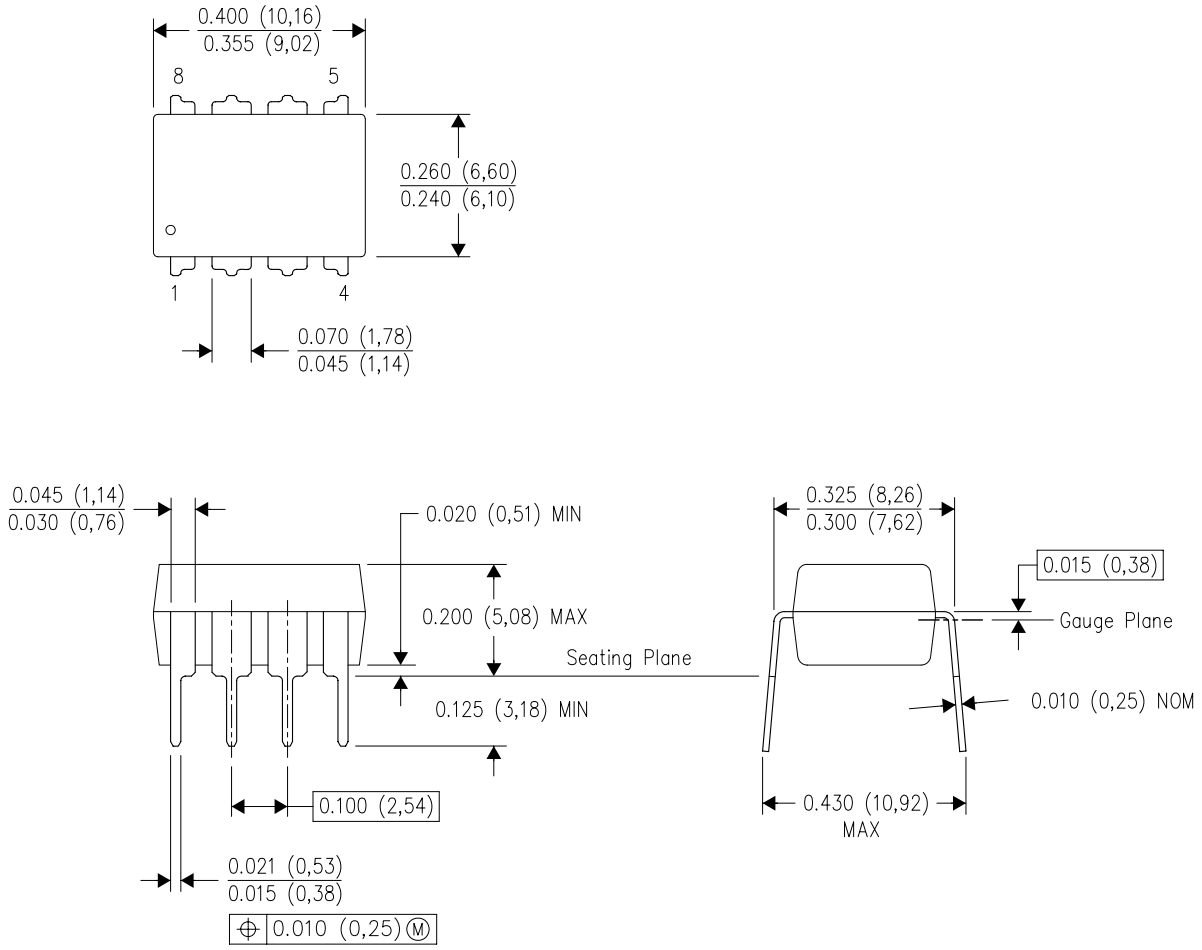
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

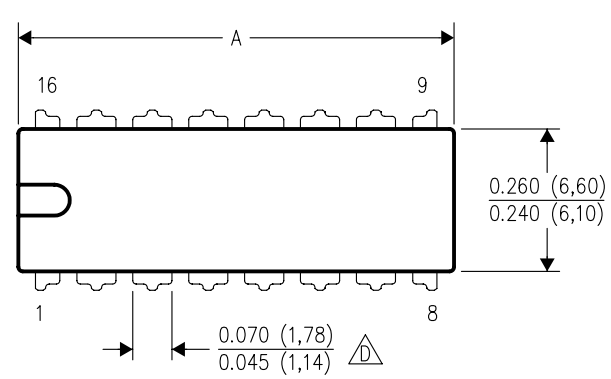


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

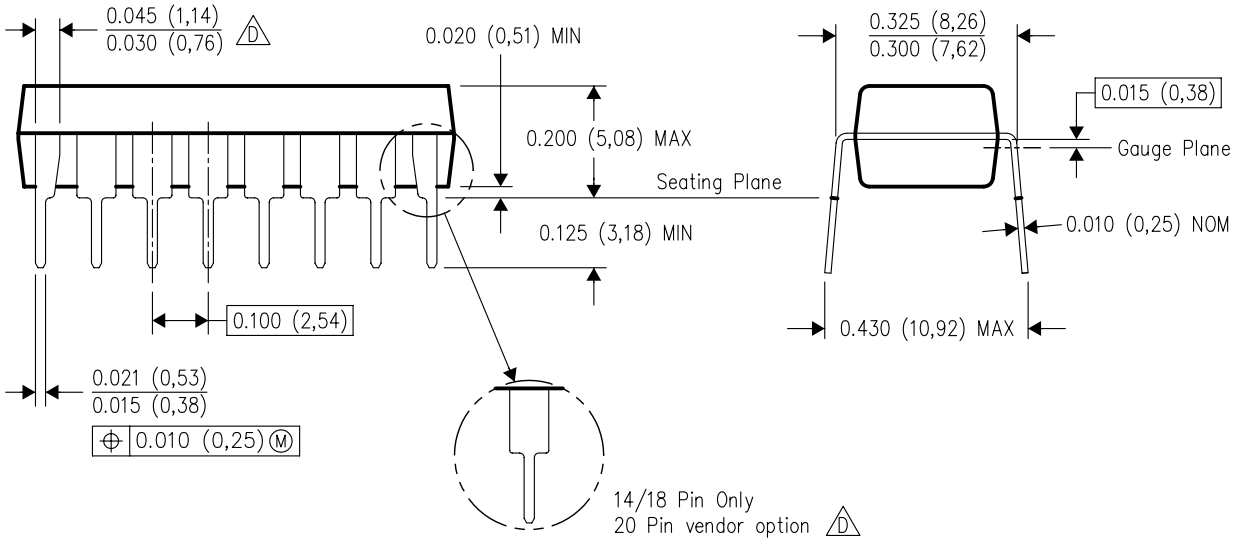
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

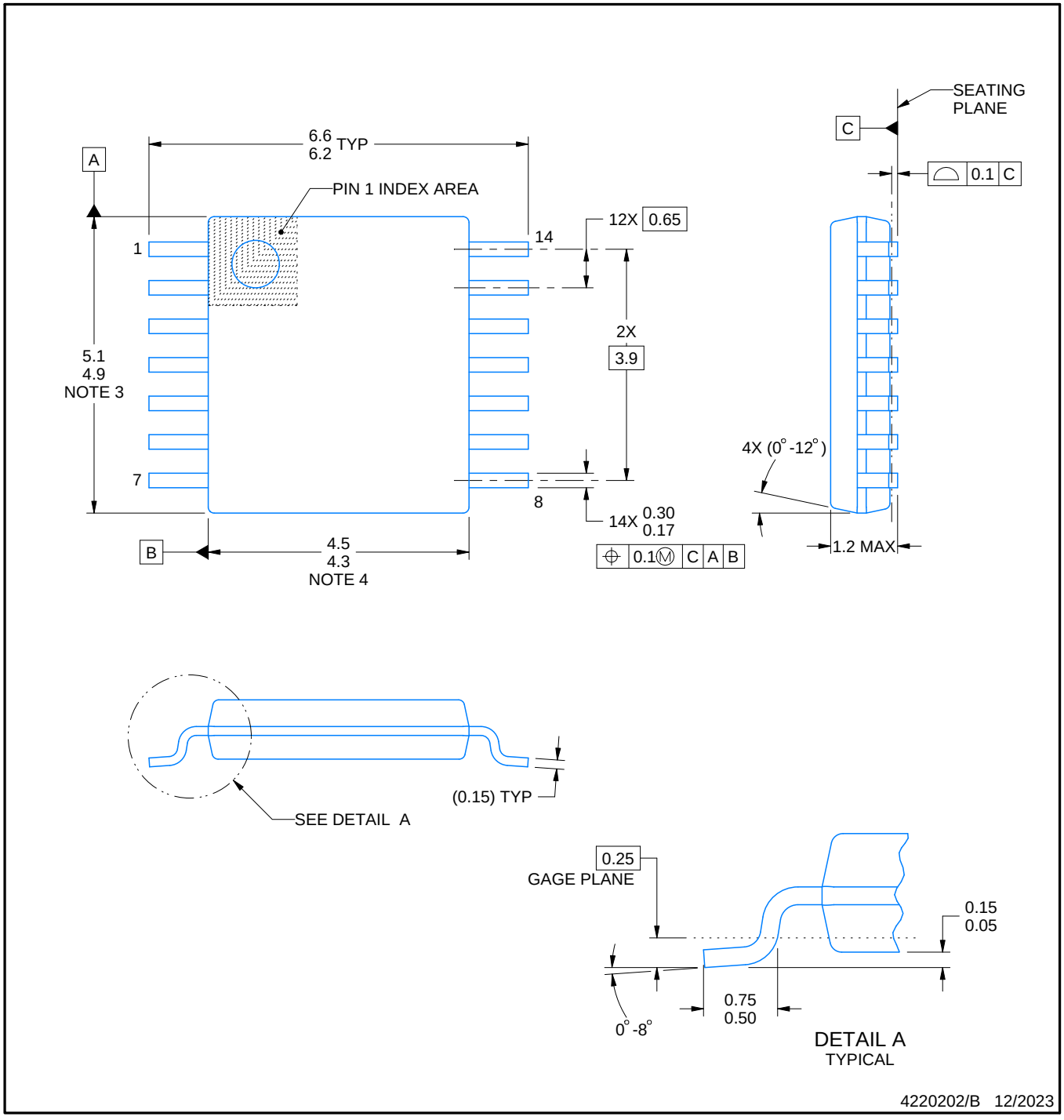
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

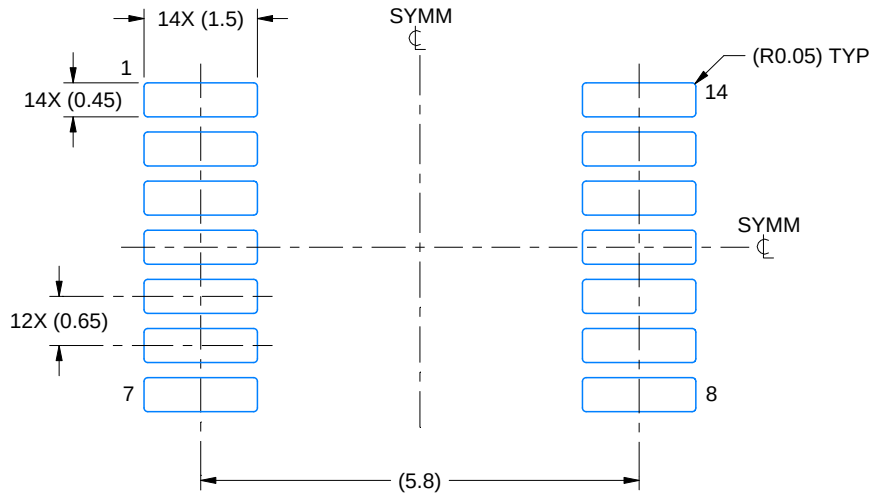
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

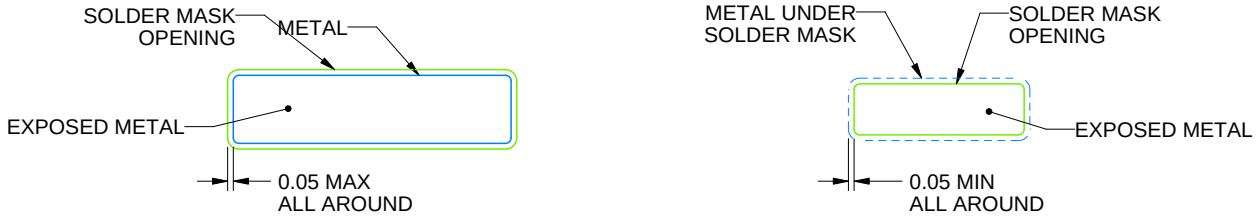


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

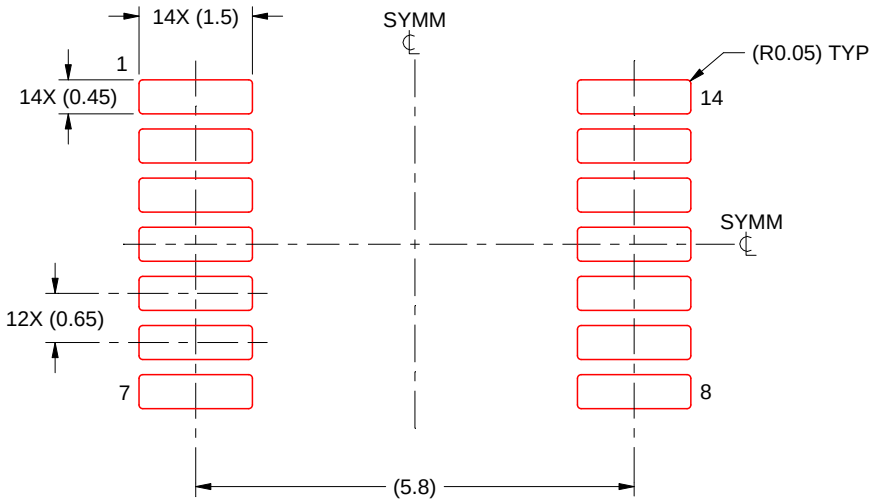


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

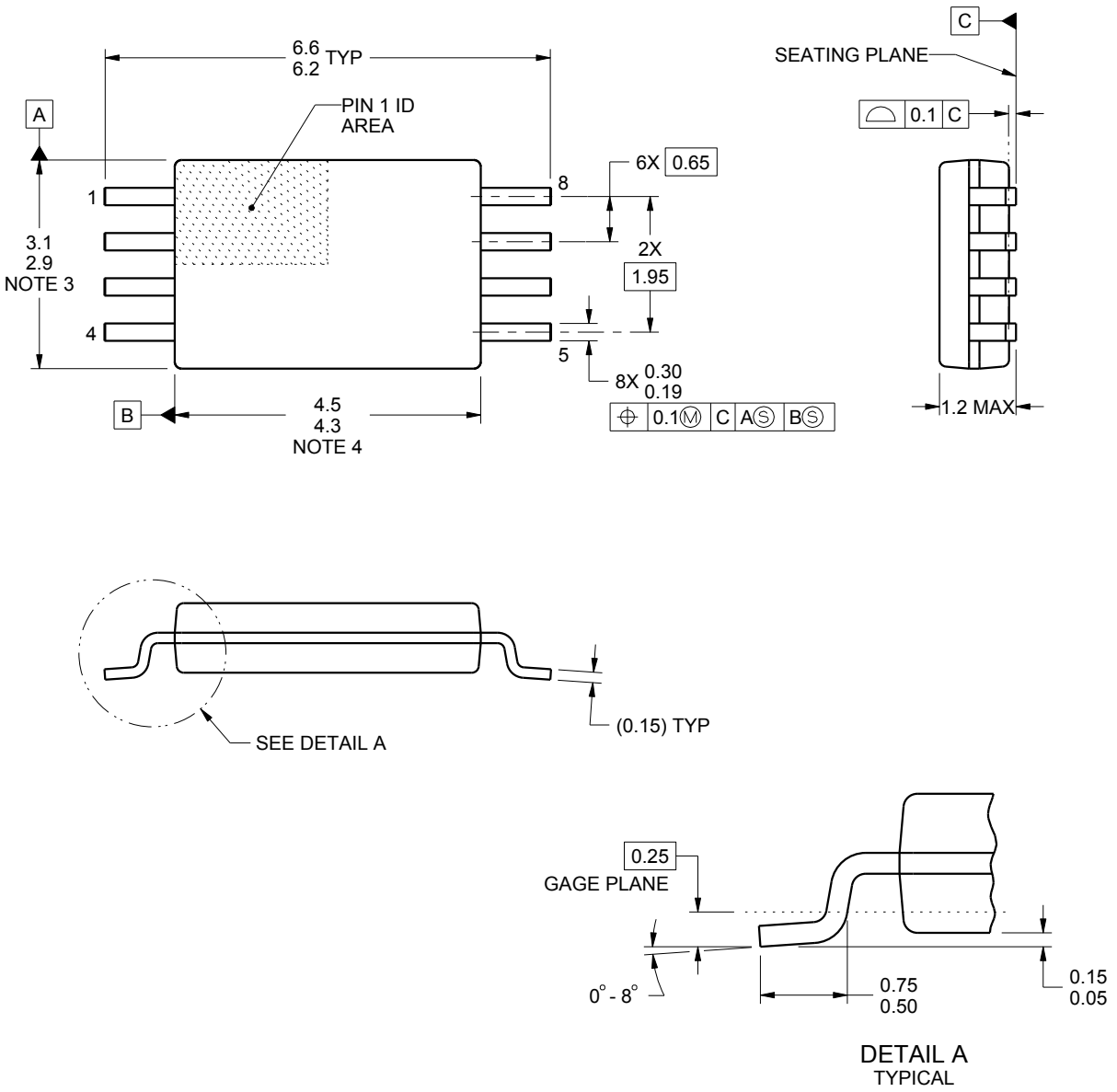
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

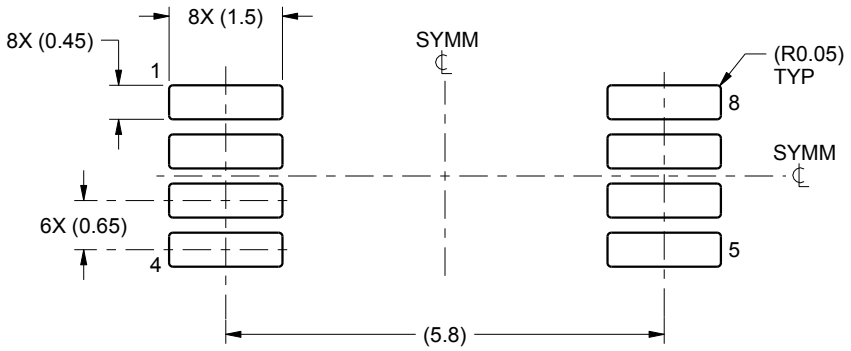
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

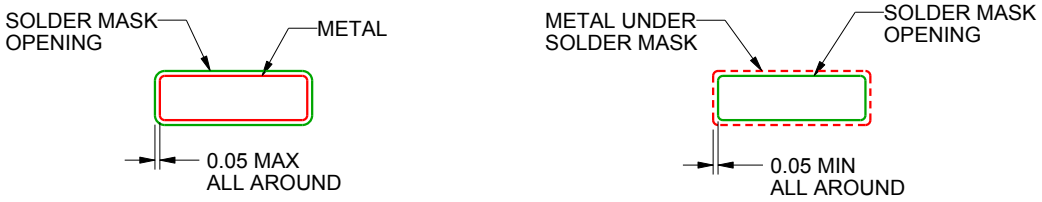


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

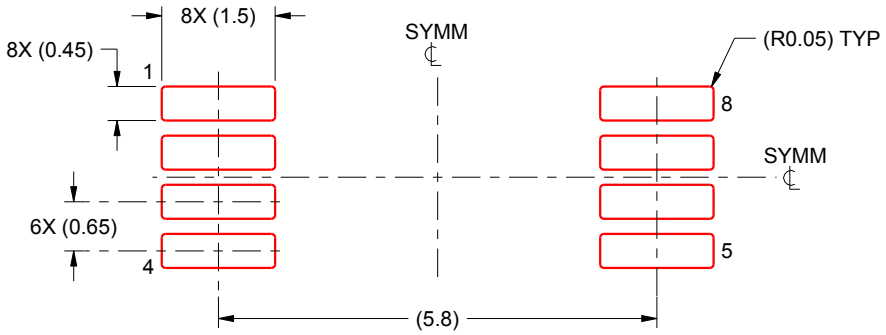


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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