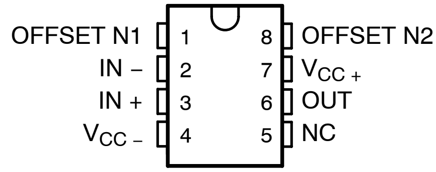
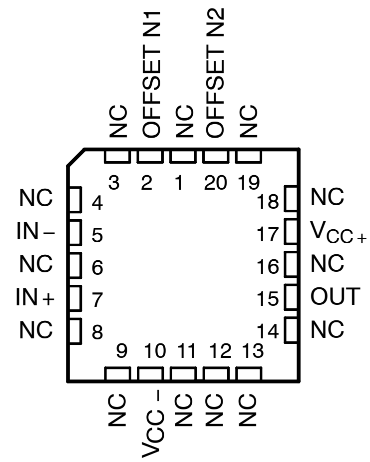
- **Outstanding Combination of dc Precision and AC Performance:**
  Unity-Gain Bandwidth . . . 15 MHz Typ
  V_n ..... 3.3 nV/$\sqrt{Hz}$ at f = 10 Hz Typ,
  2.5 nV/$\sqrt{Hz}$ at f = 1 kHz Typ
  V_{IO} .... 25 µV Max
  A_{VD} .... 45 V/µV Typ With R_L = 2 kΩ,
  19 V/µV Typ With R_L = 600 Ω
- **Available in Standard-Pinout Small-Outline Package**
- **Output Features Saturation Recovery Circuitry**
- **Macromodels and Statistical information**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



description

The TLE20x7 and TLE20x7A contain innovative circuit design expertise and high-quality process control techniques to produce a level of ac performance and dc precision previously unavailable in single operational amplifiers. Manufactured using Texas Instruments state-of-the-art Excalibur process, these devices allow upgrades to systems that use lower-precision devices.

In the area of dc precision, the TLE20x7 and TLE20x7A offer maximum offset voltages of 100 µV and 25 µV, respectively, common-mode rejection ratio of 131 dB (typ), supply voltage rejection ratio of 144 dB (typ), and dc gain of 45 V/µV (typ).

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				CHIP FORM‡ (Y)
		SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	25 µV	TLE2027ACD TLE2037ACD	— —	— —	TLE2027ACP TLE2037ACP	TLE2027Y TLE2037Y
	100 µV	TLE2027CD TLE2037CD	— —	— —	TLE2027CP TLE2037CP	TLE2027Y TLE2037Y
−40°C to 105°C	25 µV	TLE2027AID TLE2037AID	— —	— —	TLE2027AIP TLE2037AIP	—
	100 µV	TLE2027ID TLE2037ID	— —	— —	TLE2027IP TLE2037IP	—
−55°C to 125°C	25 µV	TLE2027AMD TLE2037AMD	TLE2027AMFK TLE2037AMFK	TLE2027AMJG TLE2037AMJG	TLE2027AMP TLE2037AMP	—
	100 µV	TLE2027MD TLE2037MD	TLE2027MFK TLE2037MFK	TLE2027MJG TLE2037MJG	TLE2027MP TLE2037MP	—

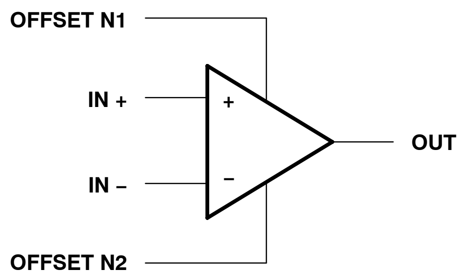
† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2027ACDR).
‡ Chip forms are tested at 25°C only.

description (continued)

The ac performance of the TLE2027 and TLE2037 is highlighted by a typical unity-gain bandwidth specification of 15 MHz, 55° of phase margin, and noise voltage specifications of 3.3 nV/$\sqrt{Hz}$ and 2.5 nV/$\sqrt{Hz}$ at frequencies of 10 Hz and 1 kHz respectively. The TLE2037 and TLE2037A have been decompensated for faster slew rate (–7.5 V/μs, typical) and wider bandwidth (50 MHz). To ensure stability, the TLE2037 and TLE2037A should be operated with a closed-loop gain of 5 or greater.

Both the TLE20x7 and TLE20x7A are available in a wide variety of packages, including the industry-standard 8-pin small-outline version for high-density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 105°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

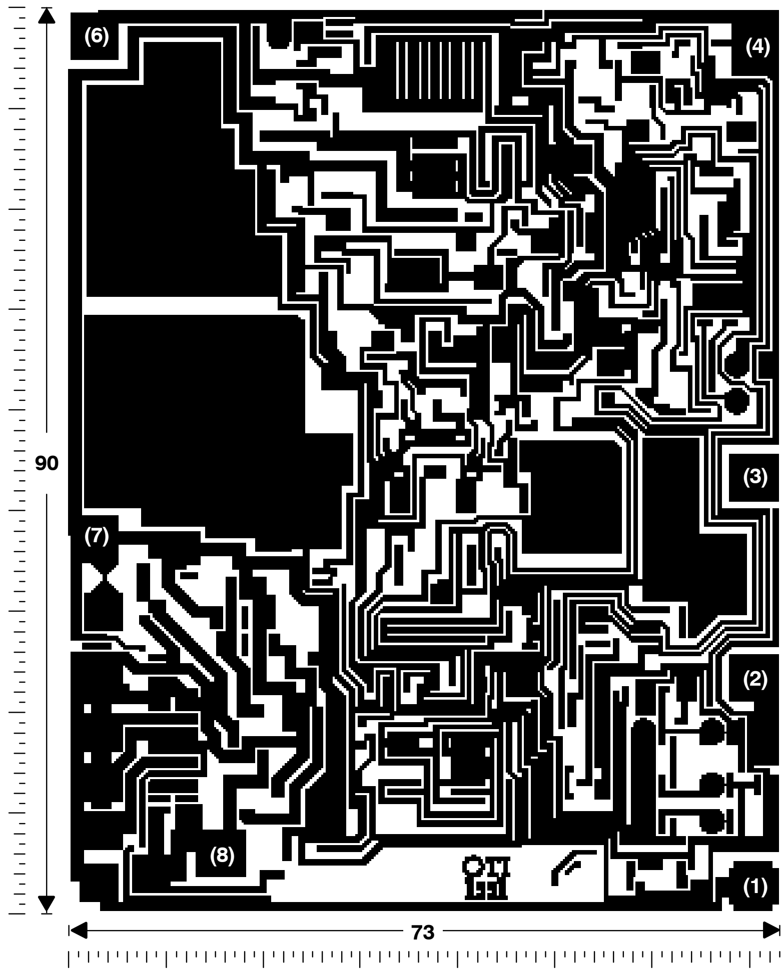
symbol

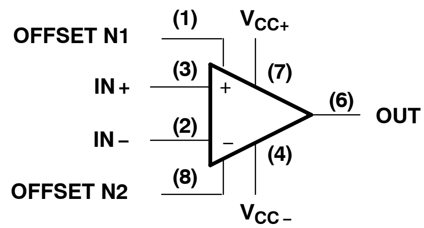


TLE202xY chip information

This chip, when properly assembled, displays characteristics similar to the TLE202xC. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

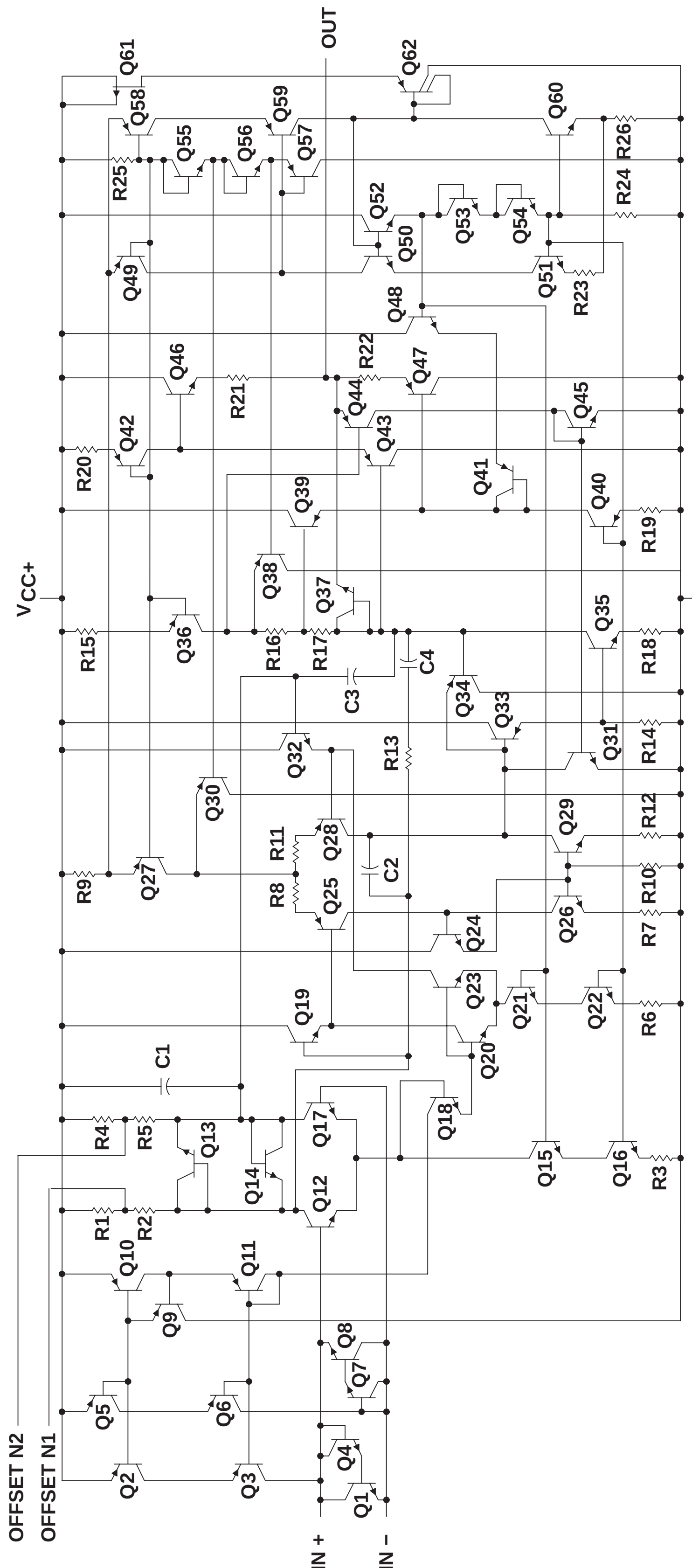
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic



ACTUAL DEVICE COMPONENT COUNT		
COMPONENT	TLE2027	TLE2037
Transistors	61	61
Resistors	26	26
epiFET	1	1
Capacitors	4	4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) . . . . 19 V
Supply voltage, V_{CC-} . . . . − 19 V
Differential input voltage, V_{ID} (see Note 2) . . . . ±1.2 V
Input voltage range, V_I (any input) . . . . $V_{CC\pm}$
Input current, I_I (each Input) . . . . ±1 mA
Output current, I_O . . . . ± 50 mA
Total current into V_{CC+} . . . . 50 mA
Total current out of V_{CC-} . . . . 50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . unlimited
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . . 0°C to 70°C
I suffix . . . . − 40°C to 105°C
M suffix . . . . − 55°C to 125°C
Storage temperature range, T_{stg} . . . . − 65°C to 150°C
Case temperature for 60 seconds, T_C: FK package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−. Excessive current flows if a differential input voltage in excess of approximately ±1.2 V is applied between the inputs unless some limiting resistance is used.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 105°C POWER RATING	T_A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	495 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	378 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	360 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±4	± 19	±4	±19	±4	±19	V
Common-mode input voltage, V_{IC}	T_A = 25°C	−11	11	−11	11	−11	11	V
	T_A = Full range‡	−10.5	10.5	−10.4	10.4	−10.2	10.2	
Operating free-air temperature, T_A		0	70	−40	105	−55	125	°C

‡ Full range is 0°C to 70°C for C-suffix devices, −40°C to 105°C for I-suffix devices, and −55°C to 125°C for M-suffix devices.

TLE20x7C electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE20x7C MIN	TLE20x7C TYP	TLE20x7C MAX	TLE20x7AC MIN	TLE20x7AC TYP	TLE20x7AC MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		20	100		10	25	µV
			Full range			145			70	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1		0.2	1	µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006	1		0.006	1	µV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	−11 to 11	−13 to 13		−11 to 11	−13 to 13		V
			Full range	−10.5 to 10.5			−10.5 to 10.5			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 600\ \Omega$	25°C	10.5	12.9		10.5	12.9		V
			Full range	10			10			
		$R_L = 2\ k\Omega$	25°C	12	13.2		12	13.2		
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 600\ \Omega$	25°C	−10.5	−13		−10.5	−13		V
			Full range	−10			−10			
		$R_L = 2\ k\Omega$	25°C	−12	−13.5		−12	−13.5		
			Full range	−11			−11			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 11$ V, $R_L = 2\ k\Omega$	25°C	5	45		10	45		V/µV
		$V_O = \pm 10$ V, $R_L = 2\ k\Omega$	Full range	2			4			
		$V_O = \pm 10$ V, $R_L = 1\ k\Omega$	25°C	3.5	38		8	38		
			Full range	1			2.5			
		$V_O = \pm 10$ V, $R_L = 600\ \Omega$	25°C	2	19		5	19		
			Full range	0.5			2			
C_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	$I_O = 0$	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$	25°C	100	131		117	131		dB
			Full range	98			114			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 4$ V to ± 18 V, $R_S = 50\ \Omega$	25°C	94	144		110	144		dB
		$V_{CC\pm} = \pm 4$ V to ± 18 V, $R_S = 50\ \Omega$	Full range	92			106			
I_{CC}	Supply current	$V_O = 0$, No load	25°C		3.8	5.3		3.8	5.3	mA
			Full range			5.6			5.6	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE20x7C operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$ (unless otherwise specified)

PARAMETER		TEST CONDITIONS		TLE20x7C MIN	TLE20x7C TYP	TLE20x7C MAX	TLE20x7AC MIN	TLE20x7AC TYP	TLE20x7AC MAX	UNIT
SR	Slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1	TLE2027	1.7	2.8		1.7	2.8		V/μs
			TLE2037	6	7.5		6	7.5		
		R_L = 2 kΩ, C_L = 100 pF, T_A = 0°C to 70°C, See Figure 1	TLE2027	1.2			1.2			
			TLE2037	5			5			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω,	f = 10 Hz		3.3	8		3.3	4.5	nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		2.5	4.5		2.5	3.8	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			50	250		50	130	nV
I_n	Equivalent input noise current	f = 10 Hz			10	25		10	25	pA/√Hz
		f = 1 kHz			0.8	1.8		0.8	1.8	
THD	Total harmonic distortion	V_O = +10 V, A_{VD} = 1, See Note 5	TLE2027		<0.002%			<0.002%		
		V_O = +10 V, A_{VD} = 5, See Note 5	TLE2037		<0.002%			<0.002%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 2 kΩ, C_L = 100 pF	TLE2027	9(6)	13		9(6)	13		MHz
GBW	Gain bandwidth product	R_L = 2 kΩ, C_L = 100 pF	TLE2037	35	50		35	50		
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ	TLE2027		30			30		kHz
			TLE2037		80			80		
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 2 kΩ, C_L = 100 pF	TLE2027		55°			55°		
			TLE2037		50°			50°		

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.
NOTE 6: This parameter is not production tested

TLE20x7I electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE20x7I			TLE20x7AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		20	100		10	25	μV
			Full range			180			105	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1		0.2	1	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006	1		0.006	1	μV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	–11 to 11	–13 to 13		–11 to 11	–13 to 13		V
			Full range	–10.4 to 10.4			–10.4 to 10.4			
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 600\ \Omega$	25°C	10.5	12.9		10.5	12.9		V
			Full range	10			10			
		$R_L = 2\ k\Omega$	25°C	12	13.2		12	13.2		
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 600\ \Omega$	25°C	–10.5	–13		–10.5	–13		V
			Full range	–10			–10			
		$R_L = 2\ k\Omega$	25°C	–12	–13.5		–12	–13.5		
			Full range	–11			–11			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm11$ V, $R_L = 2\ k\Omega$	25°C	5	45		10	45		V/μV
		$V_O = \pm10$ V, $R_L = 2\ k\Omega$	Full range	2			3.5			
		$V_O = \pm10$ V, $R_L = 1\ k\Omega$	25°C	3.5	38		8	38		
			Full range	1			2.2			
		$V_O = \pm10$ V, $R_L = 600\ \Omega$	25°C	2	19		5	19		
			Full range	0.5			1.1			
C_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	$I_O = 0$	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$	25°C	100	131		117	131		dB
			Full range	96			113			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm4$ V to ±18 V, $R_S = 50\ \Omega$	25°C	94	144		110	144		dB
		$V_{CC\pm} = \pm4$ V to ±18 V, $R_S = 50\ \Omega$	Full range	90			105			
I_{CC}	Supply current	$V_O = 0$, No load	25°C		3.8	5.3		3.8	5.3	mA
			Full range			5.6			5.6	

† Full range is – 40°C to 105°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE20x7I operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$ (unless otherwise specified)

PARAMETER		TEST CONDITIONS		TLE20x7I			TLE20x7AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1	TLE2027	1.7	2.8		1.7	2.8		V/μs
			TLE2037	6	7.5		6	7.5		
		R_L = 2 kΩ, C_L = 100 pF, T_A = −40°C to 85°C, See Figure 1	TLE2027	1.1			1.1			
			TLE2037	4.7			4.7			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω,	f = 10 Hz		3.3	8		3.3	4.5	nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		2.5	4.5		2.5	3.8	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			50	250		50	130	nV
I_n	Equivalent input noise current	f = 10 Hz			10	25		10	25	pA/√Hz
		f = 1 kHz			0.8	1,8		0.8	1.8	
THD	Total harmonic distortion	V_O = +10 V, A_{VD} = 1, See Note 5	TLE2027		< 0.002%			< 0.002%		
		V_O = +10 V, A_{VD} = 5, See Note 5	TLE2037		< 0.002%			< 0.002%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 2 kΩ, C_L = 100 pF	TLE2027	9(6)	13		9(6)	13		MHz
GBW	Gain bandwidth product	R_L = 2 kΩ, C_L = 100 pF	TLE2037	35	50		35	50		
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ	TLE2027		30			30		kHz
			TLE2037		80			80		
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 2 kΩ, C_L = 100 pF	TLE2027		55°			55°		
			TLE2037		50°			50°		

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.
NOTE 6: This parameter is not production tested.

TLE20x7M electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE20x7M MIN	TLE20x7M TYP	TLE20x7M MAX	TLE20x7AM MIN	TLE20x7AM TYP	TLE20x7AM MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		20	100		10	25	μV
			Full range			200			105	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1*		0.2	1*	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006	1*		0.006	1*	μV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	–11 to 11	–13 to 13		–11 to 11	–13 to 13		V
			Full range	–10.3 to 10.3			–10.4 to 10.4			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 600 Ω	25°C	10.5	12.9		10.5	12.9		V
			Full range	10			10			
		R_L = 2 kΩ	25°C	12	13.2		12	13.2		
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 600 Ω	25°C	–10.5	–13		–10.5	–13		V
			Full range	–10			–10			
		R_L = 2 kΩ	25°C	–12	–13.5		–12	–13.5		
			Full range	–11			–11			
A_{VD}	Large-signal differential voltage amplification	V_O = ±11 V, R_L = 2 kΩ	25°C	5	45		10	45		V/μV
		V_O = ±10 V, R_L = 2 kΩ	Full range	2.5			3.5			
		V_O = ±10 V, R_L = 1 kΩ	25°C	3.5	38		8	38		
			Full range	1.8			2.2			
		V_O = ±10 V, R_L = 600 Ω	25°C	2	19		5	19		
C_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	I_O = 0	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, R_S = 50 Ω	25°C	100	131		117	131		dB
			Full range	96			113			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	25°C	94	144		110	144		dB
		$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	Full range	90			105			
I_{CC}	Supply current	V_O = 0, No load	25°C		3.8	5.3		3.8	5.3	mA
			Full range			5.6			5.6	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† Full range is – 55°C to 125°C.
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE20x7M operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$ (unless otherwise specified)

PARAMETER		TEST CONDITIONS		TLE20x7M MIN	TLE20x7M TYP	TLE20x7M MAX	TLE20x7AM MIN	TLE20x7AM TYP	TLE20x7AM MAX	UNIT
SR	Slew rate at unity gain	$R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1	TLE2027	1.7	2.8		1.7	2.8		V/μs
			TLE2037	6*	7.5		6*	7.5		
		$R_L = 2$ kΩ, $C_L = 100$ pF, $T_A = -55°C$ to 125°C, See Figure 1	TLE2027	1			1			
			TLE2037	4.4*			4.4*			
V_n	Equivalent input noise voltage (see Figure 2)	$R_S = 20$ Ω,	f = 10 Hz		3.3	8*		3.3	8*	nV/√Hz
		$R_S = 20$ Ω,	f = 1 kHz		2.5	4*		2.5	4*	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			225	375*		225	375*	nV
I_n	Equivalent input noise current	f = 10 Hz			25			25		pA/√Hz
		f = 1 kHz			2.5			2.5		
THD	Total harmonic distortion	$V_O = +10$ V, $A_{VD} = 1$, See Note 5	TLE2027		< 0.002%			< 0.002%		
		$V_O = +10$ V, $A_{VD} = 5$, See Note 5	TLE2037		< 0.002%			< 0.002%		
B_1	Unity-gain bandwidth (see Figure 3)	$R_L = 2$ kΩ, $C_L = 100$ pF	TLE2027	7*	13		9*	13		MHz
			TLE2037	35	50		35	50		
B_{OM}	Maximum output-swing bandwidth	$R_L = 2$ kΩ	TLE2027		30			30		kHz
			TLE2037		80			80		
ϕ_m	Phase margin at unity gain (see Figure 3)	$R_L = 2$ kΩ, $C_L = 100$ pF	TLE2027		55°			55°		
			TLE2037		50°			50°		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

TLE20x7Y electrical characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLE20x7Y MIN	TLE20x7Y TYP	TLE20x7Y MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$		20		μV
	Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0$, $R_S = 50\ \Omega$		0.006		μV/mo
I_{IO}	Input offset current	$V_{IC} = 0$, $R_S = 50\ \Omega$		6		nA
I_{IB}	Input bias current	$V_{IC} = 0$, $R_S = 50\ \Omega$		15		nA
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$		−13 to 13		V
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 600\ \Omega$		12.9		V
		$R_L = 2\ k\Omega$		13.2		
V_{OM-}	Maximum negative peak output voltage swing	$R_L = 600\ \Omega$		−13		V
		$R_L = 2\ k\Omega$		−13.5		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm11$ V, $R_L = 2\ k\Omega$		45		V/μV
		$V_O = \pm10$ V, $R_L = 1\ k\Omega$		38		
		$V_O = \pm10$ V, $R_L = 600\ \Omega$		19		
C_i	Input capacitance			8		pF
z_o	Open-loop output impedance	$I_O = 0$		50		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$		131		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm4$ V to ±18 V, $R_S = 50\ \Omega$		144		dB
I_{CC}	Supply current	$V_O = 0$, No load		3.8		mA

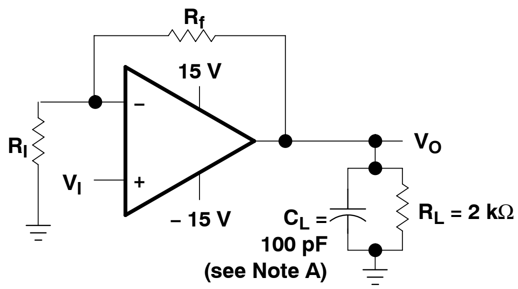
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE20x7Y operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V

PARAMETER		TEST CONDITIONS		TLE20x7Y MIN	TLE20x7Y TYP	TLE20x7Y MAX	UNIT
SR	Slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1	TLE2027		2.8		V/μs
			TLE2037		7.5		
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω, f = 10 Hz			3.3		nV/√Hz
		R_S = 20 Ω, f = 1 kHz			2.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			50		nV
I_n	Equivalent input noise current	f = 10 Hz			10		pA/√Hz
		f = 1 kHz			0.8		
THD	Total harmonic distortion	V_O = +10 V, A_{VD} = 1, See Note 5	TLE2027		<0.002%		
		V_O = +10 V, A_{VD} = 5, See Note 5	TLE2037		<0.002%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 2 kΩ, C_L = 100 pF	TLE2027		13		MHz
			TLE2037		50		
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ	TLE2027		30		kHz
			TLE2037		80		
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 2 kΩ, C_L = 100 pF	TLE2027		55°		
			TLE2037		50°		

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

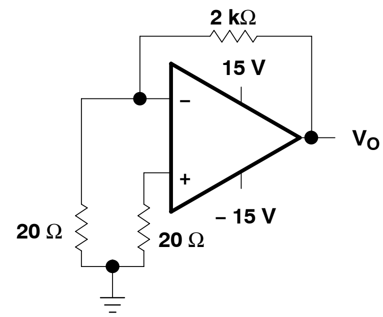
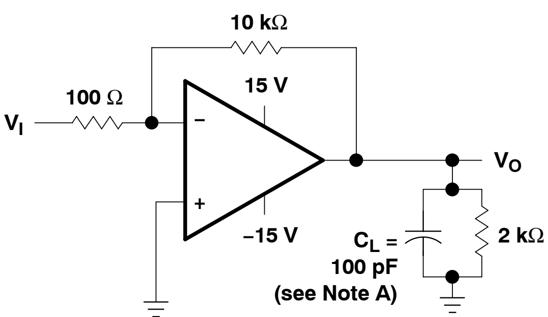
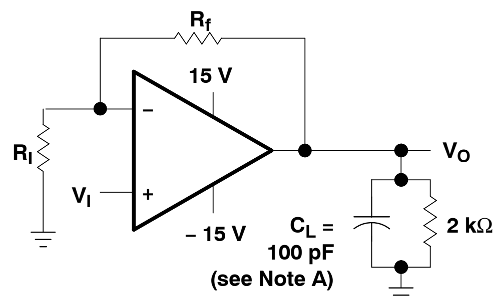


Figure 2. Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase-Margin Test Circuit (TLE2027 Only)



NOTES: A. C_L includes fixture capacitance.
B. For the TLE2037 and TLE2037A, A_{VD} must be ≥ 5.

Figure 4. Small-Signal Pulse-Response Test Circuit

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

initial estimates of parameter distributions

In the ongoing program of improving data sheets and supplying more information to our customers, Texas Instruments has added an estimate of not only the typical values but also the spread around these values. These are in the form of distribution bars that show the 95% (upper) points and the 5% (lower) points from the characterization of the initial wafer lots of this new device type (see Figure 5). The distribution bars are shown at the points where data was actually collected. The 95% and 5% points are used instead of ± 3 sigma since some of the distributions are not true Gaussian distributions.

The number of units tested and the number of different wafer lots used are on all of the graphs where distribution bars are shown. As noted in Figure 5, there were a total of 835 units from two wafer lots. In this case, there is a good estimate for the within-lot variability and a possibly poor estimate of the lot-to-lot variability. This is always the case on newly released products since there can only be data available from a few wafer lots.

The distribution bars are not intended to replace the minimum and maximum limits in the electrical tables. Each distribution bar represents 90% of the total units tested at a specific temperature. While 10% of the units tested fell outside any given distribution bar, this should not be interpreted to mean that the same individual devices fell outside every distribution bar.

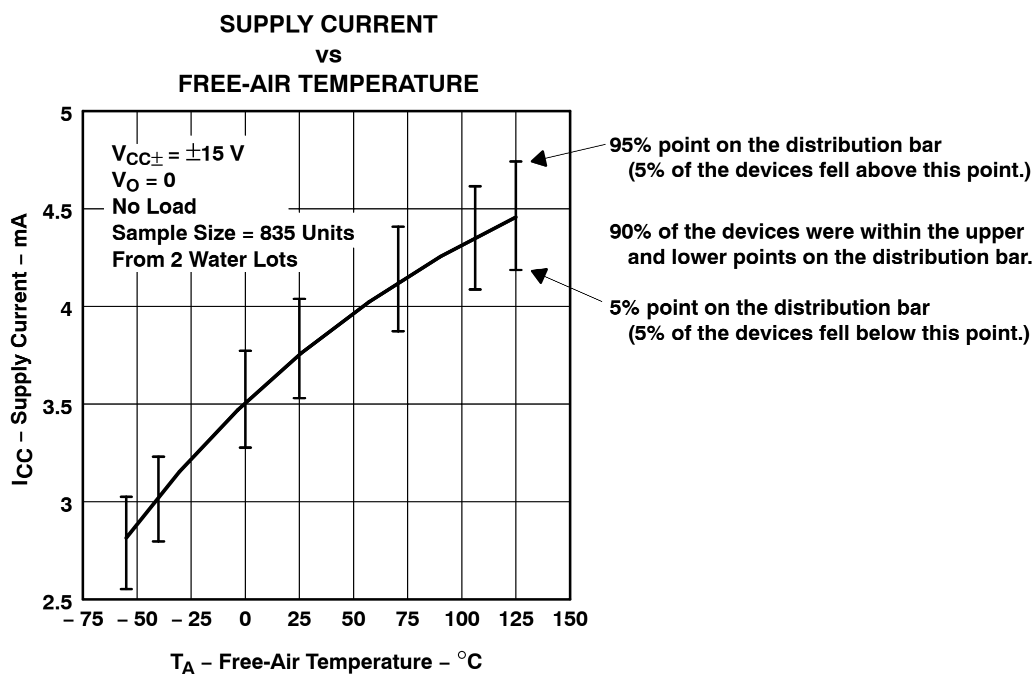


Figure 5. Sample Graph With Distribution Bars

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6, 7
ΔV_{IO}	Input offset voltage change	vs Time after power on	8, 9
I_{IO}	Input offset current	vs Free-air temperature	10
I_{IB}	Input bias current	vs Free-air temperature vs Common-mode input voltage	11 12
I_I	Input current	vs Differential input voltage	13
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	14, 15
V_{OM}	Maximum (positive/negative) peak output voltage	vs Load resistance vs Free-air temperature	16, 17 18, 19
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Load resistance vs Frequency vs Free-air temperature	20 21 22 – 25 26
z_o	Output impedance	vs Frequency	27
CMRR	Common-mode rejection ratio	vs Frequency	28
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	29
I_{OS}	Short-circut output current	vs Supply voltage vs Elapsed time vs Free-air temperature	30, 31 32, 33 34, 35
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	36 37
	Voltage-follower pulse response	Small signal Large signal	38, 40 39, 41
V_n	Equivalent input noise voltage	vs Frequency	42
	Noise voltage (referred to input)	Over 10-second interval	43
B_1	Unity-gain bandwidth	vs Supply voltage vs Load capacitance	44 45
	Gain bandwidth product	vs Supply voltage vs Load capacitance	46 47
SR	Slew rate	vs Free-air temperature	48, 49
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance vs Free-air temperature	50, 51 52, 53 54, 55
	Phase shift	vs Frequency	22 – 25

TYPICAL CHARACTERISTICS

**DISTRIBUTION
INPUT OFFSET VOLTAGE**

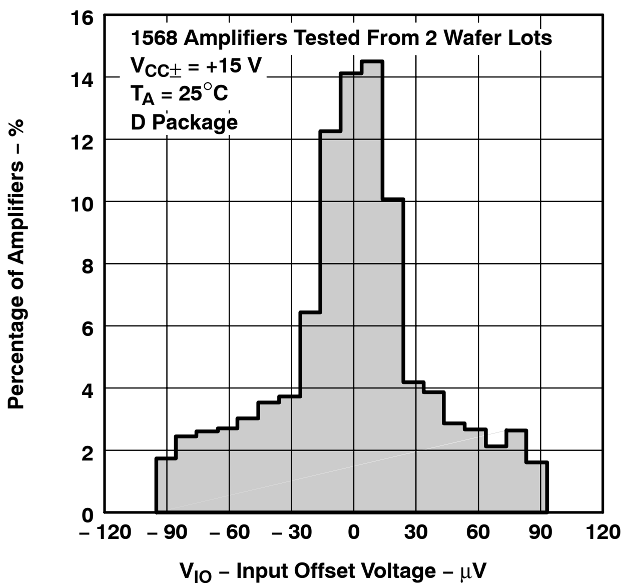


Figure 6

**INPUT OFFSET VOLTAGE CHANGE
vs
TIME AFTER POWER ON**

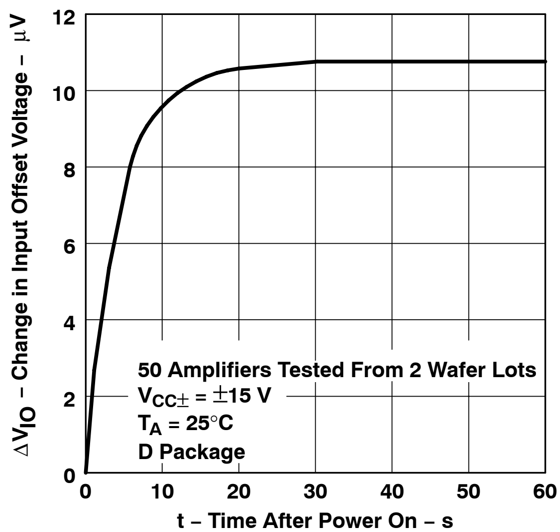


Figure 7

**INPUT OFFSET VOLTAGE CHANGE
vs
TIME AFTER POWER ON**

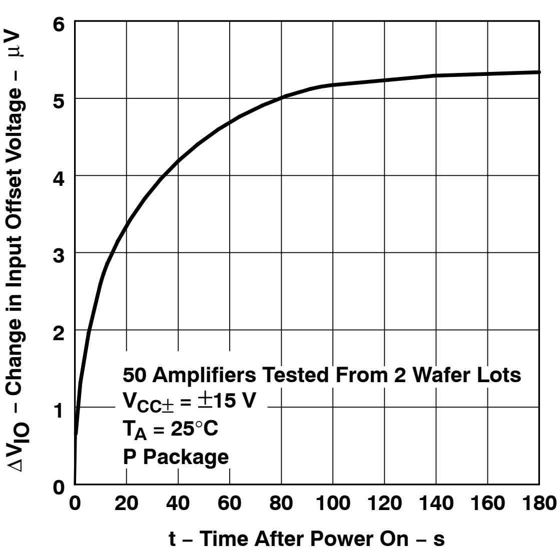


Figure 8

**INPUT OFFSET CURRENT†
vs
FREE-AIR TEMPERATURE**

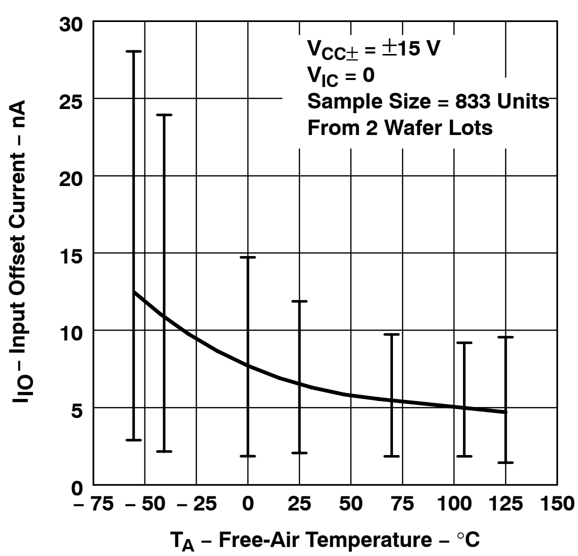


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT † vs FREE-AIR TEMPERATURE

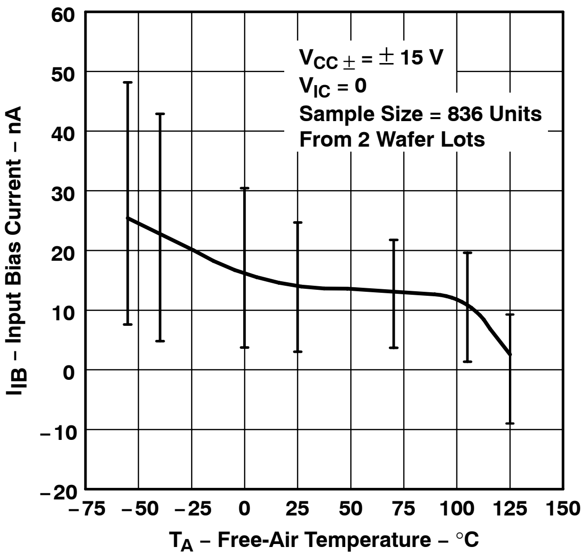


Figure 10

INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

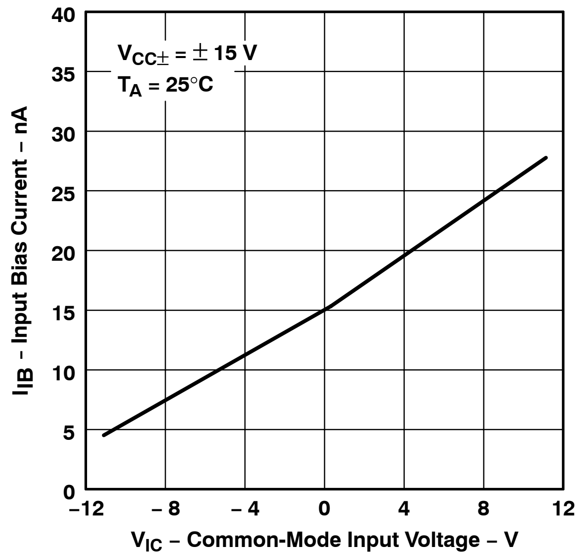


Figure 11

INPUT CURRENT vs DIFFERENTIAL INPUT VOLTAGE

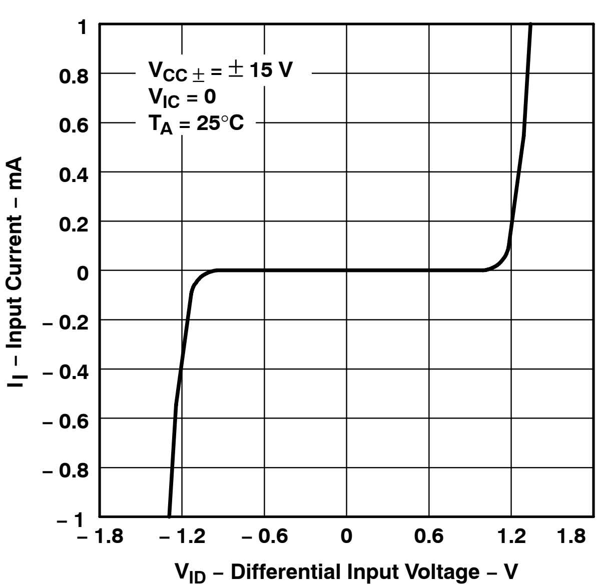


Figure 12

TLE2027 MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE † vs FREQUENCY

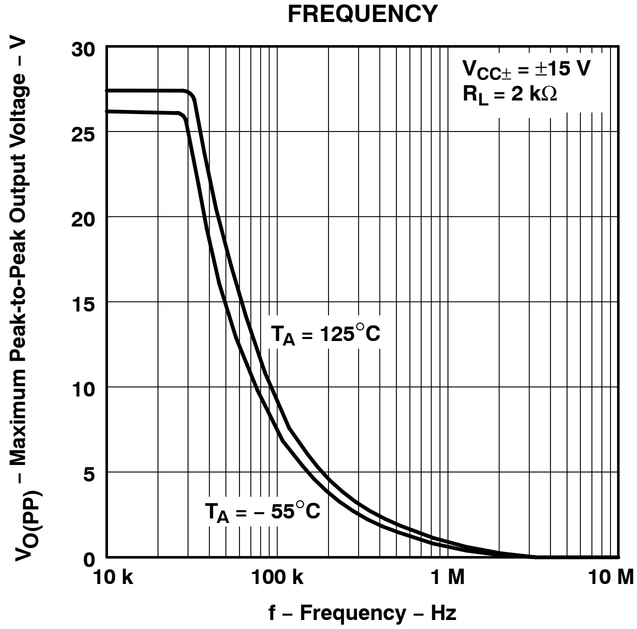


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

TLE2037
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE†
vs
FREQUENCY

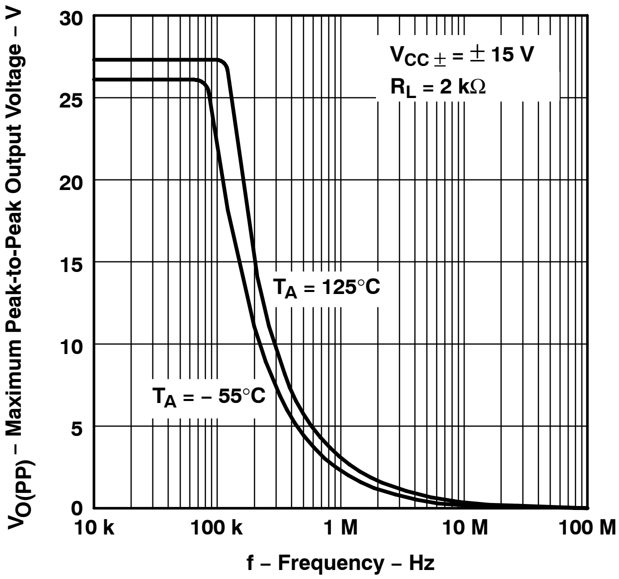


Figure 14

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

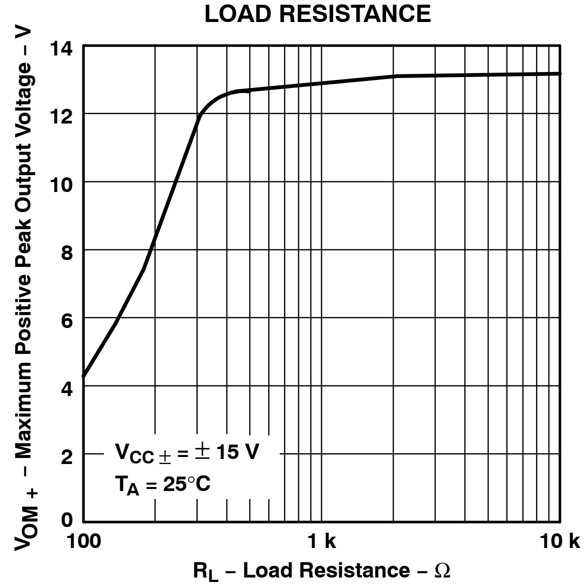


Figure 15

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

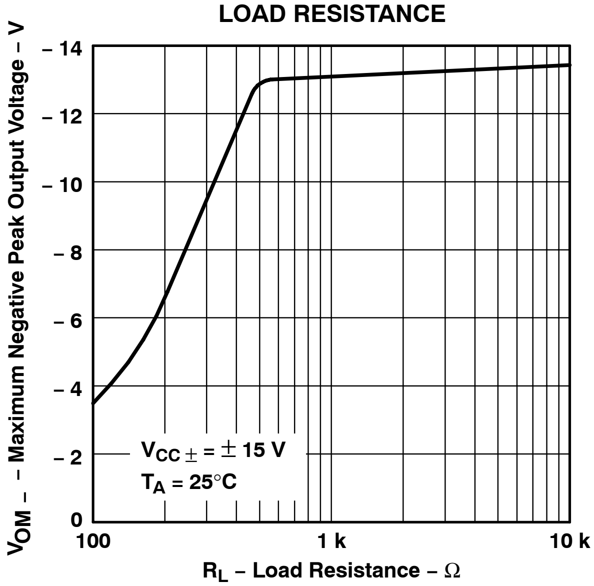


Figure 16

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE†
vs
FREE-AIR TEMPERATURE

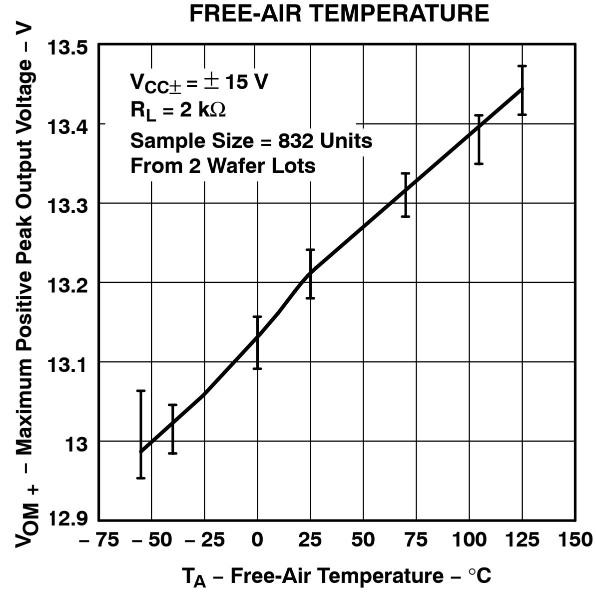


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE† vs FREE-AIR TEMPERATURE

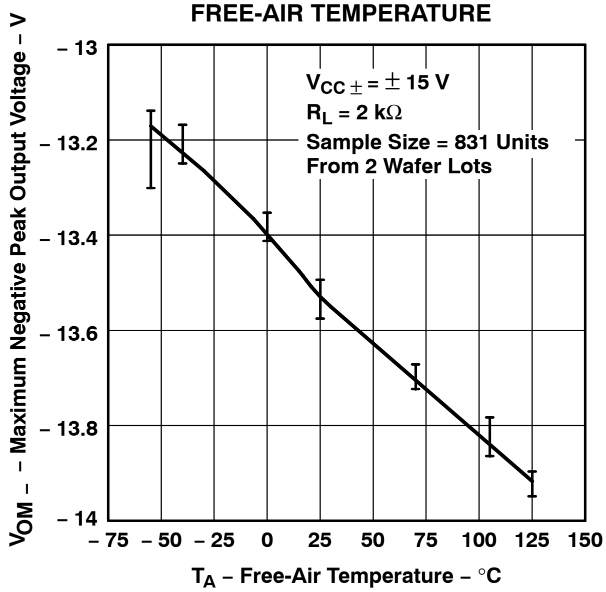


Figure 18

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

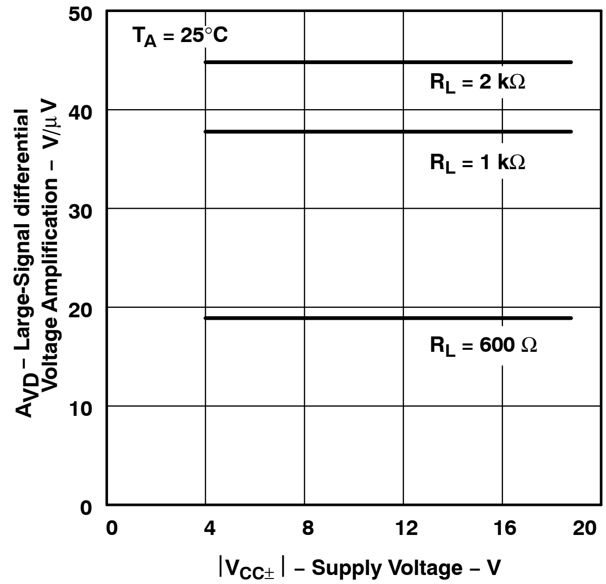


Figure 19

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

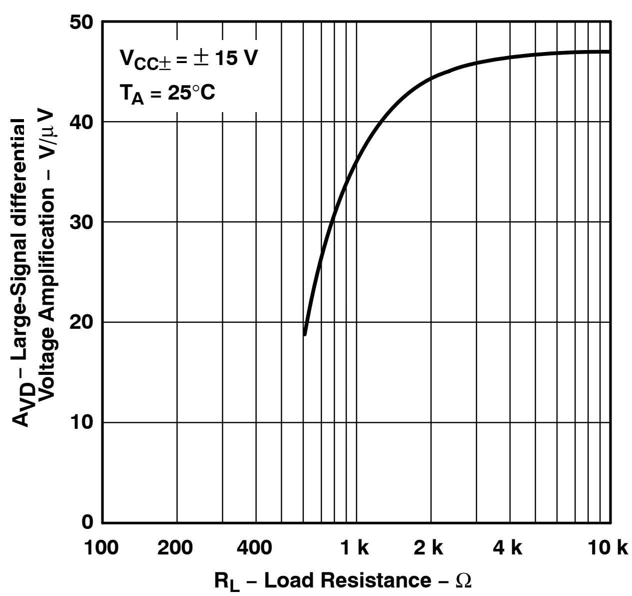


Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

TLE2027
LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

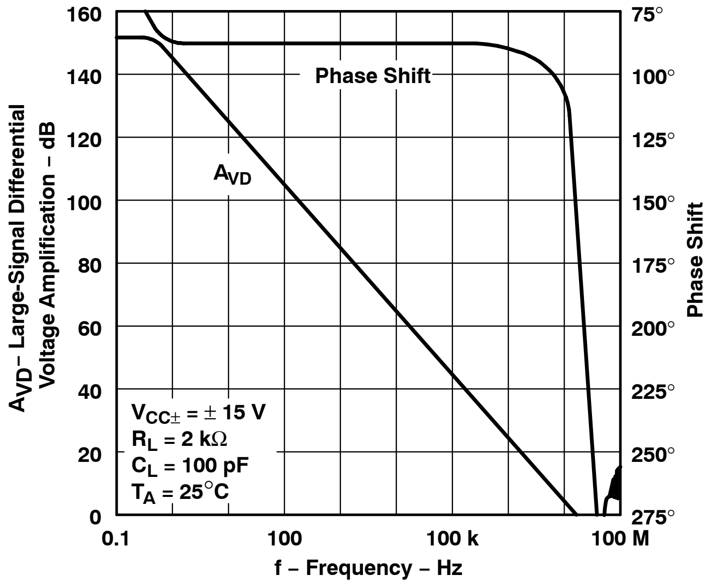


Figure 21

TLE2037
LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

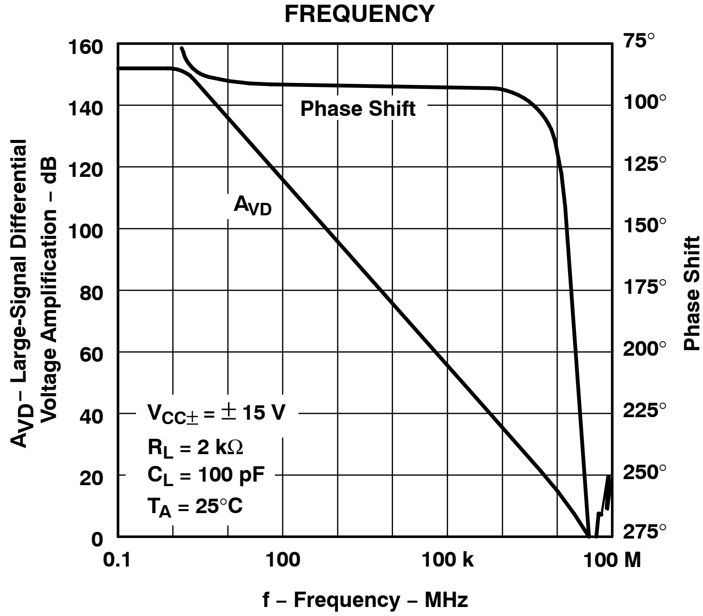


Figure 22

TYPICAL CHARACTERISTICS

TLE2027
LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

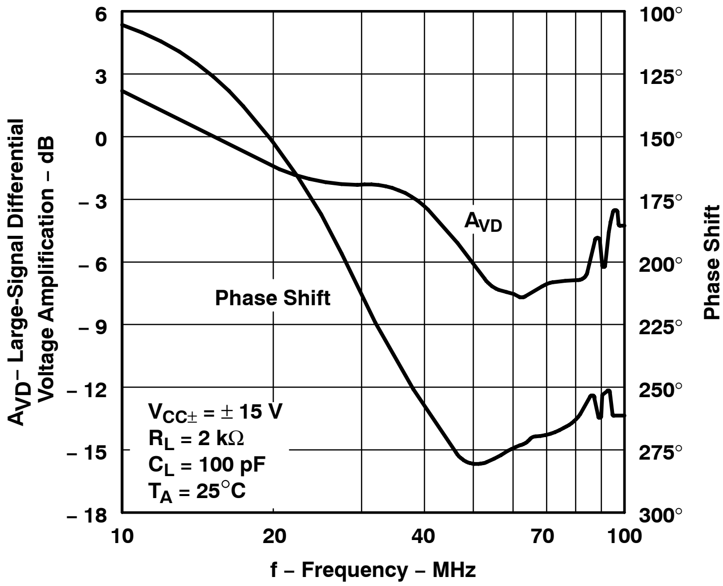


Figure 23

TLE2037
LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

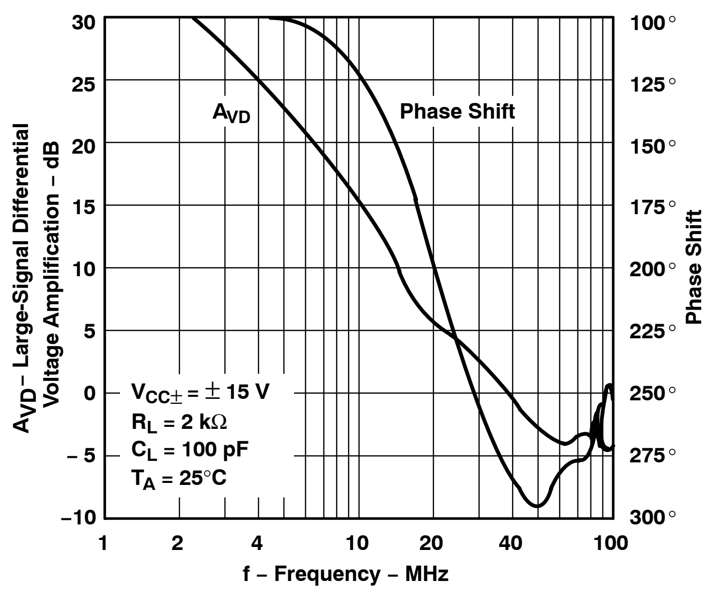


Figure 24

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION† vs FREE-AIR TEMPERATURE

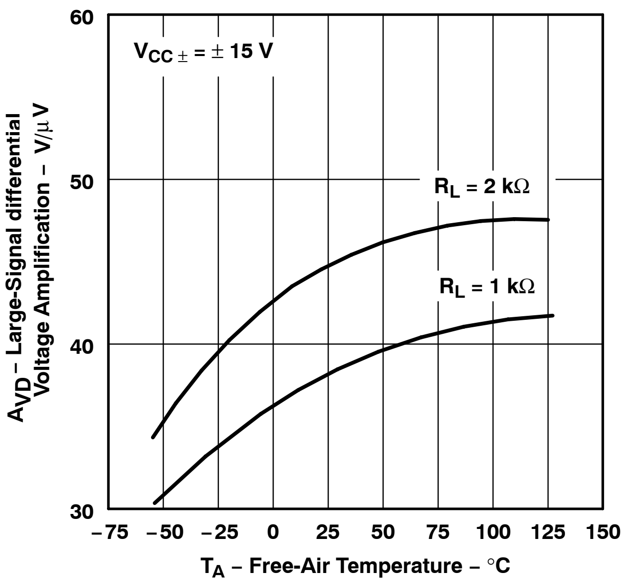
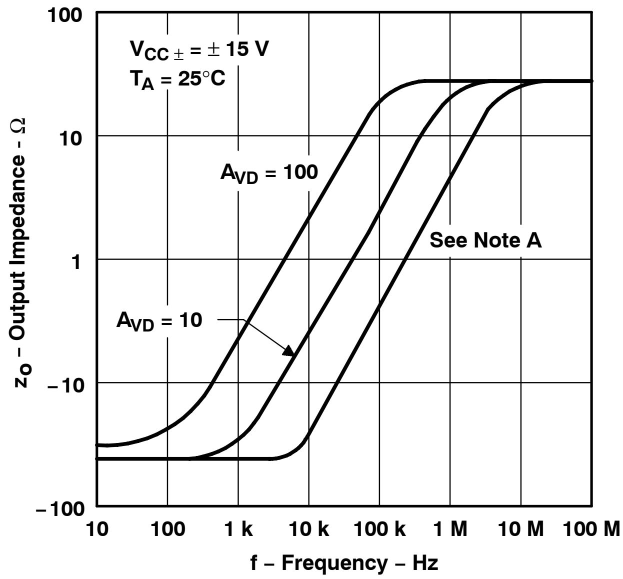


Figure 25

OUTPUT IMPEDANCE vs FREQUENCY



NOTE A: For this curve, the TLE2027 is $A_{VD} = 1$ and the TLE2037 is $A_{VD} = 5$.

Figure 26

COMMON-MODE REJECTION RATIO vs FREQUENCY

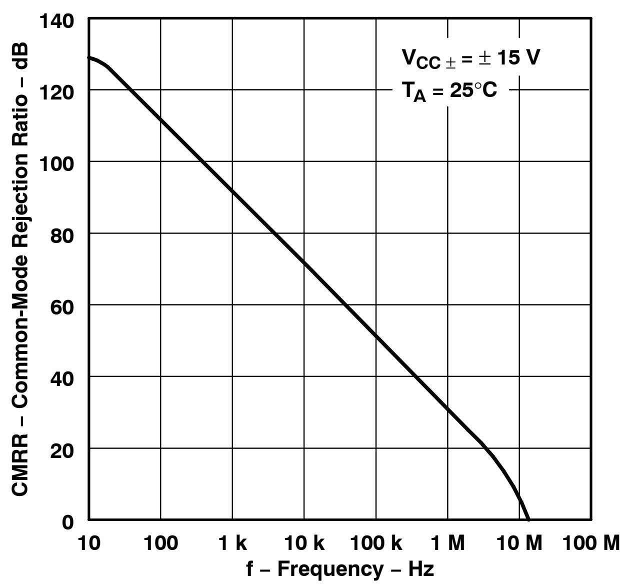


Figure 27

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

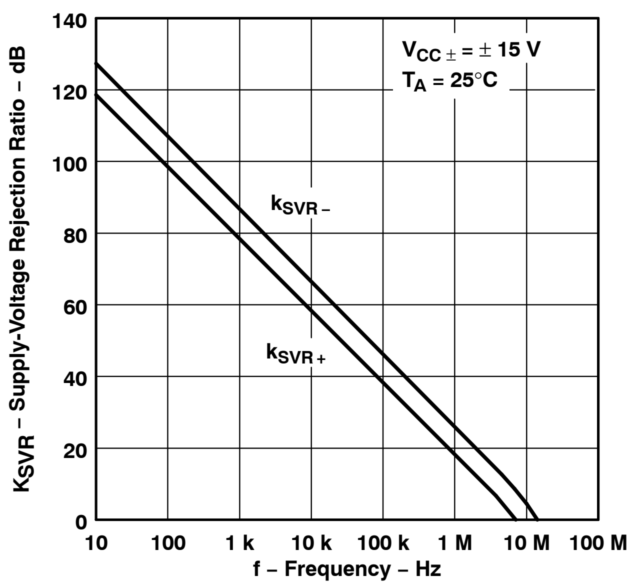


Figure 28

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

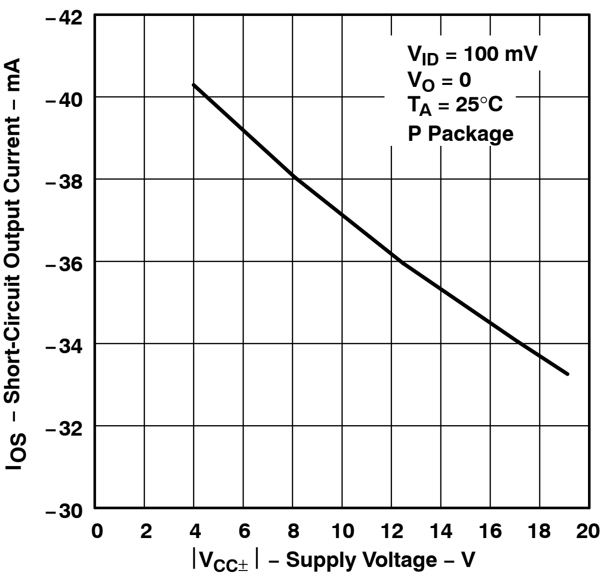


Figure 29

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

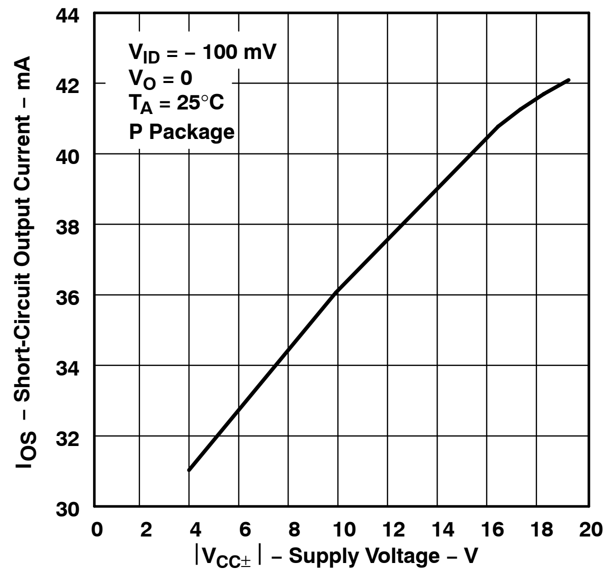


Figure 30

SHORT-CIRCUIT OUTPUT CURRENT vs ELAPSED TIME

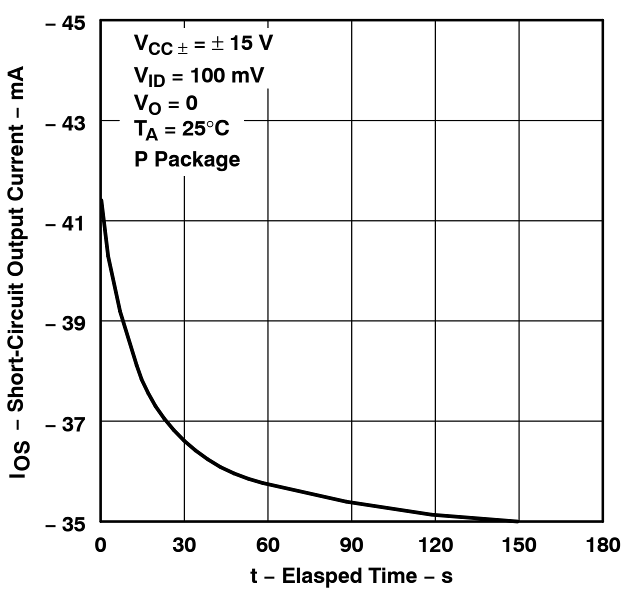


Figure 31

SHORT-CIRCUIT OUTPUT CURRENT vs ELAPSED TIME

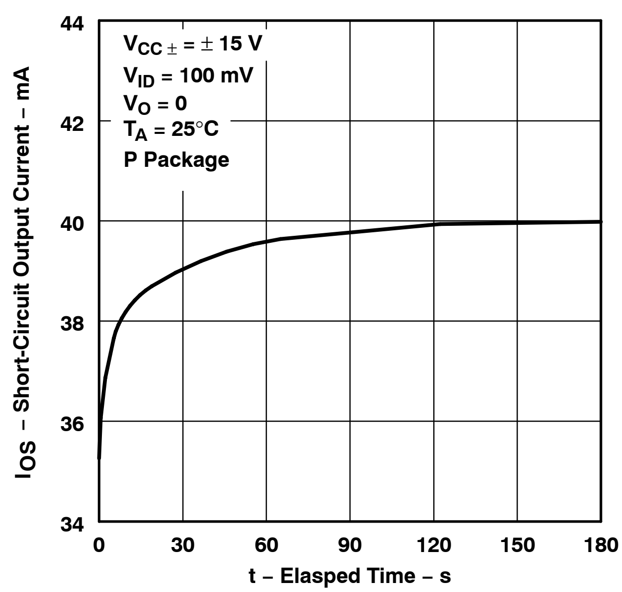


Figure 32

TYPICAL CHARACTERISTICS

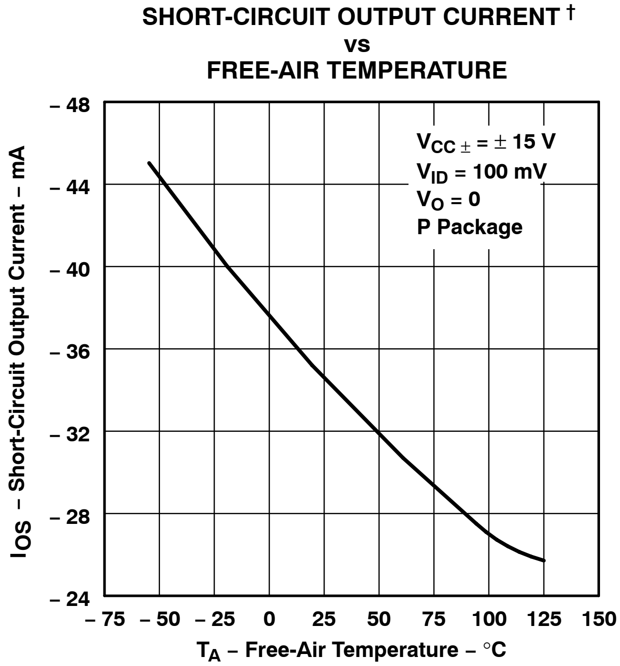


Figure 33

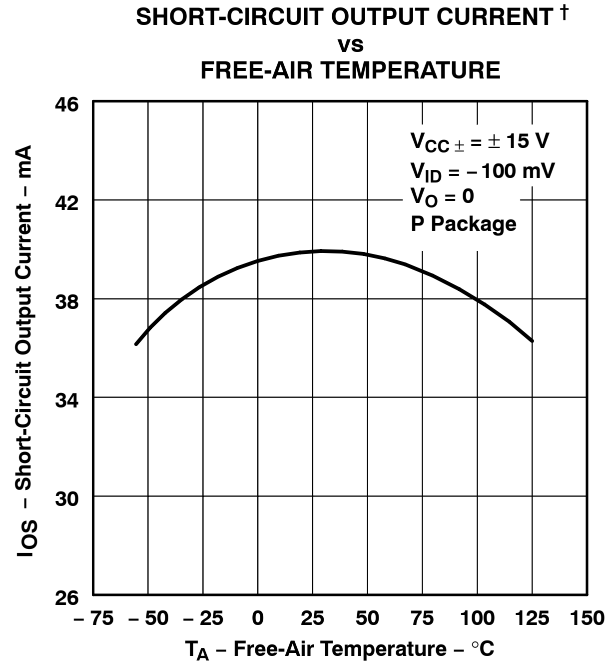


Figure 34

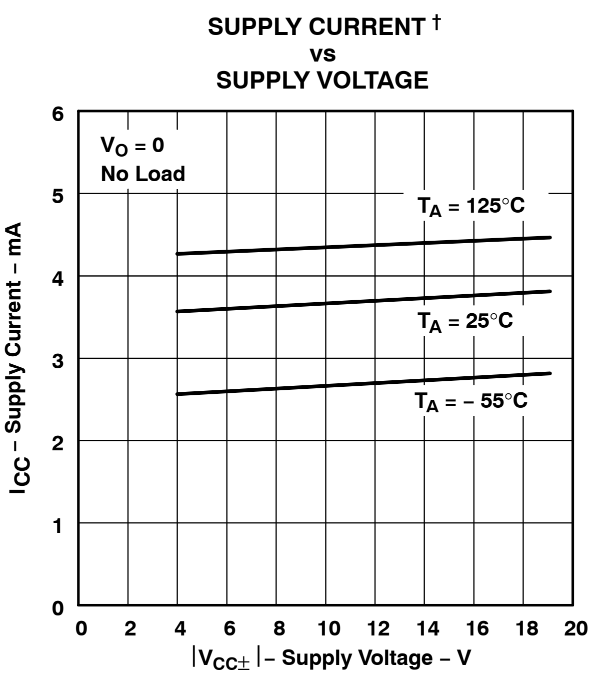


Figure 35

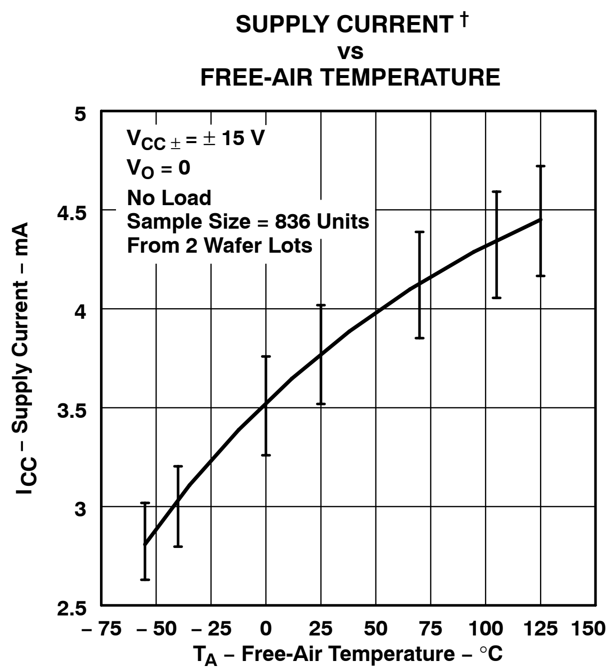


Figure 36

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

TLE2027
VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

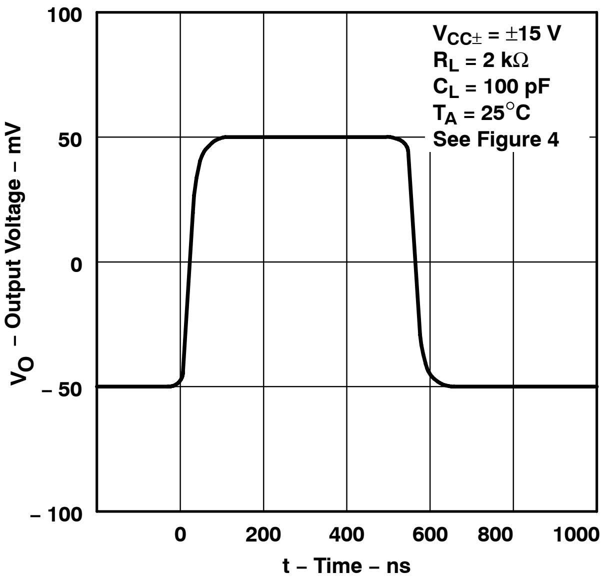


Figure 37

TLE2027
VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

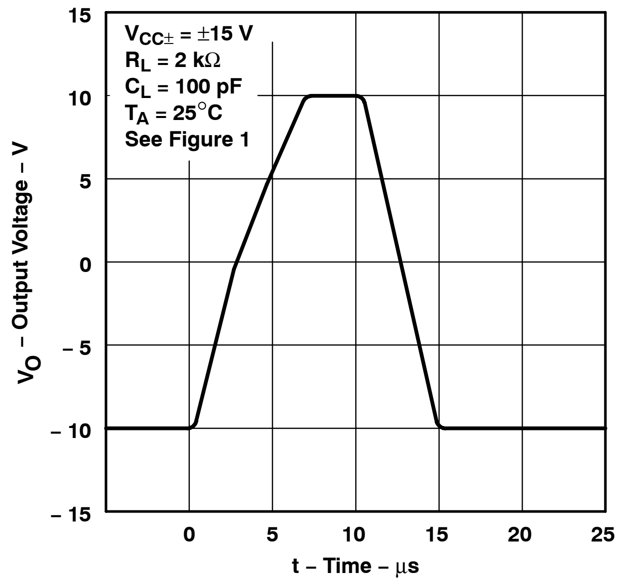


Figure 38

TLE2037
VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

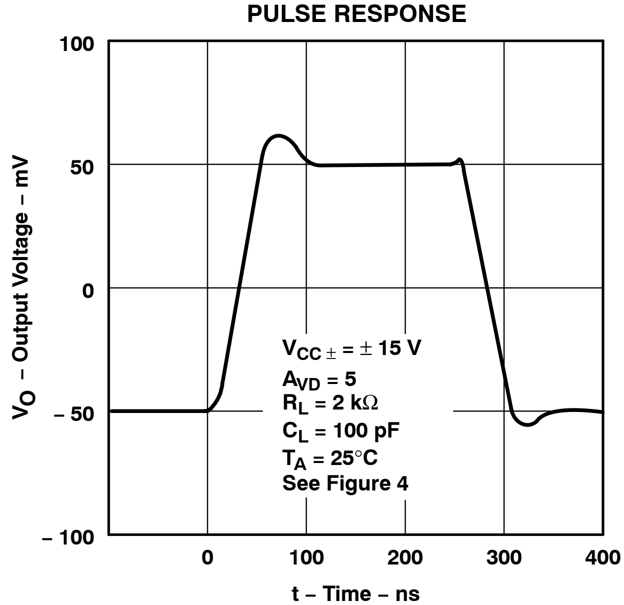


Figure 39

TLE2037
VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

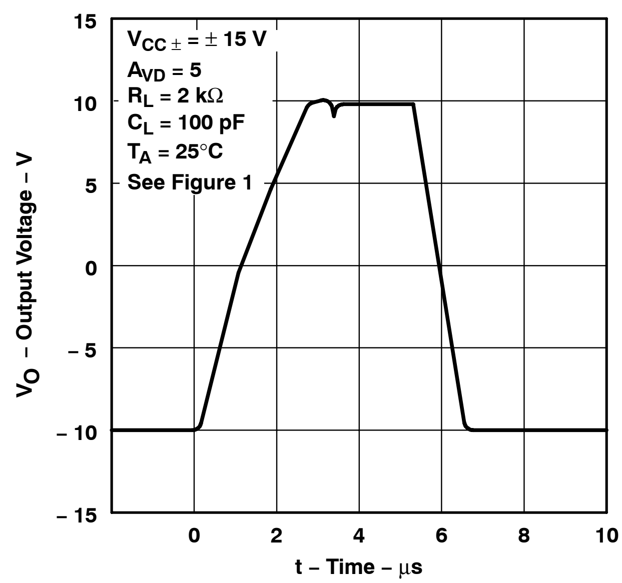


Figure 40

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

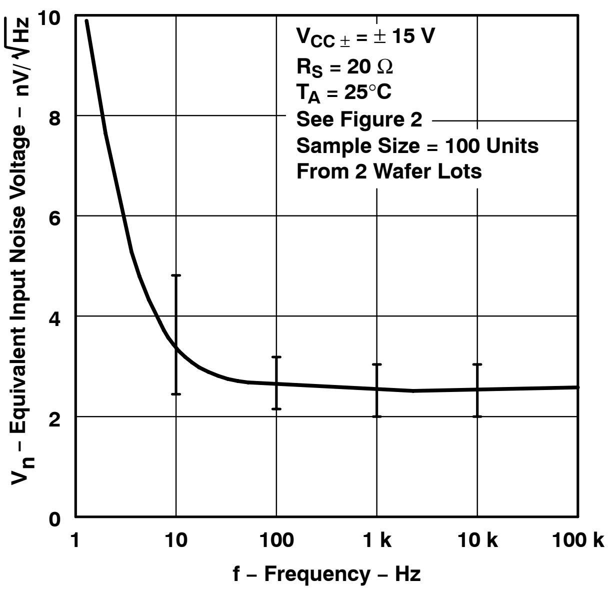


Figure 41

NOISE VOLTAGE
(REFERRED TO INPUT)
OVER A 10-SECOND INTERVAL

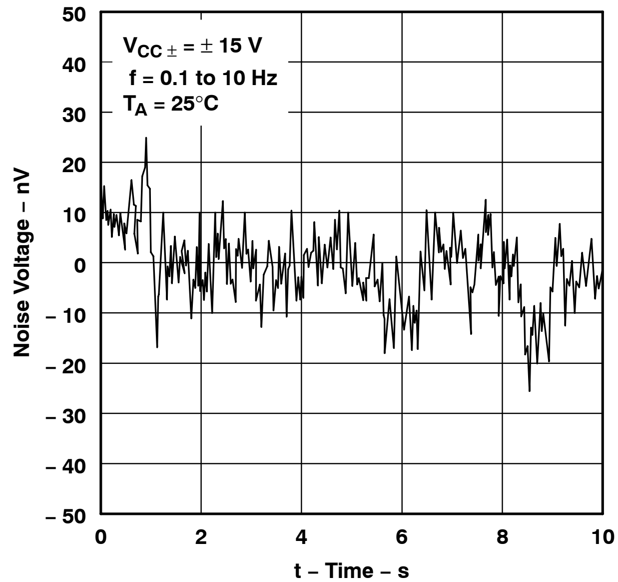


Figure 42

TLE2027
UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

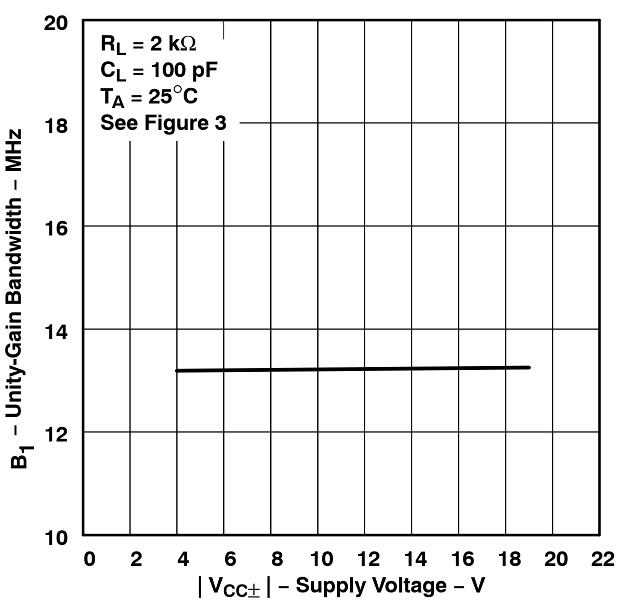


Figure 43

TLE2037
GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

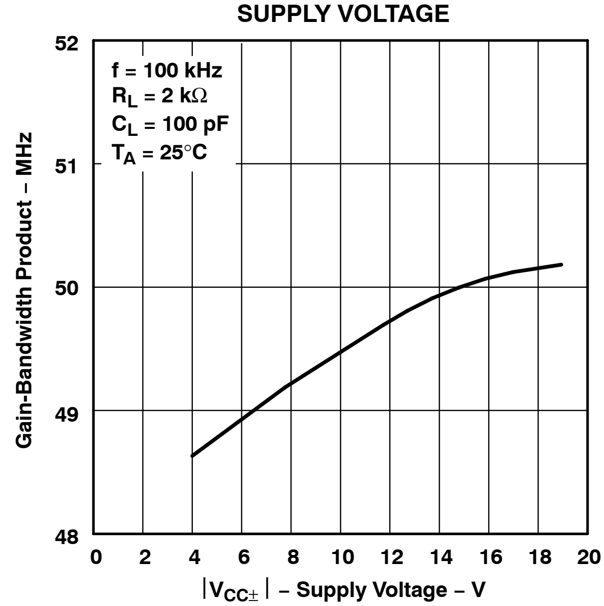


Figure 44

TYPICAL CHARACTERISTICS

TLE2027
UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

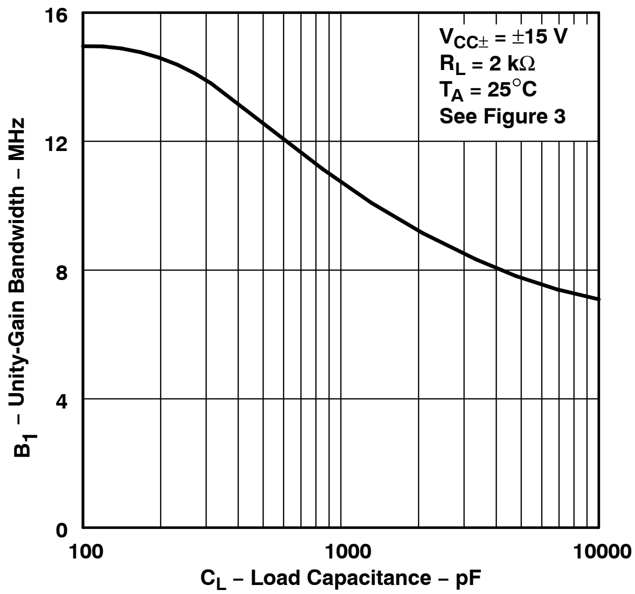


Figure 45

TLE2037
GAIN-BANDWIDTH PRODUCT
vs
LOAD CAPACITANCE

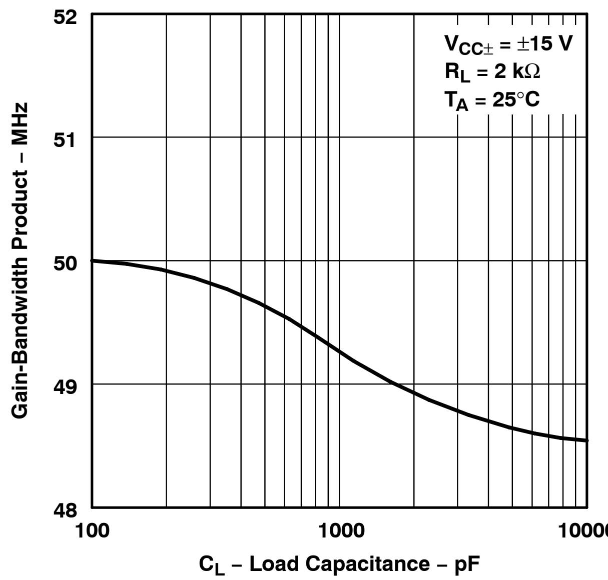


Figure 46

TLE2027
SLEW RATE†
vs
FREE-AIR TEMPERATURE

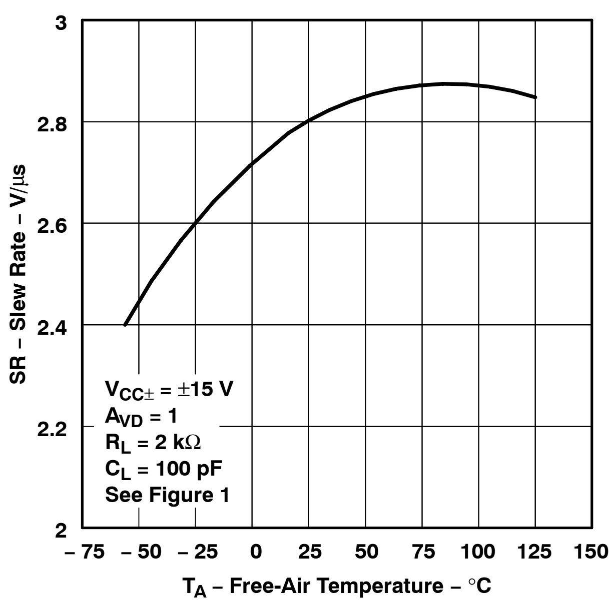


Figure 47

TLE2037
SLEW RATE†
vs
FREE-AIR TEMPERATURE

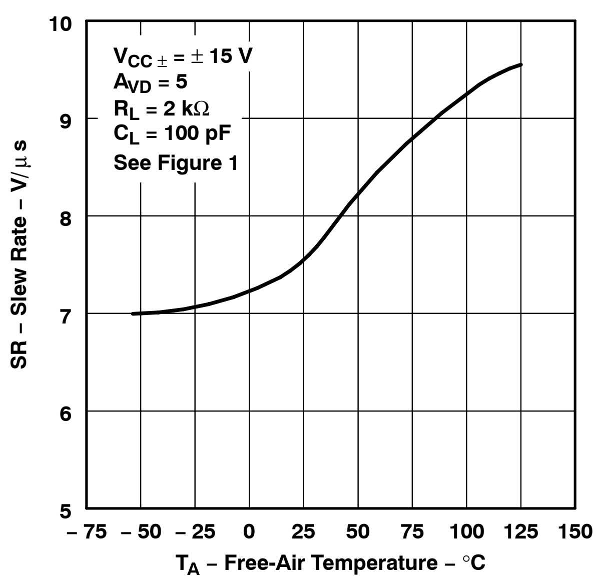


Figure 48

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

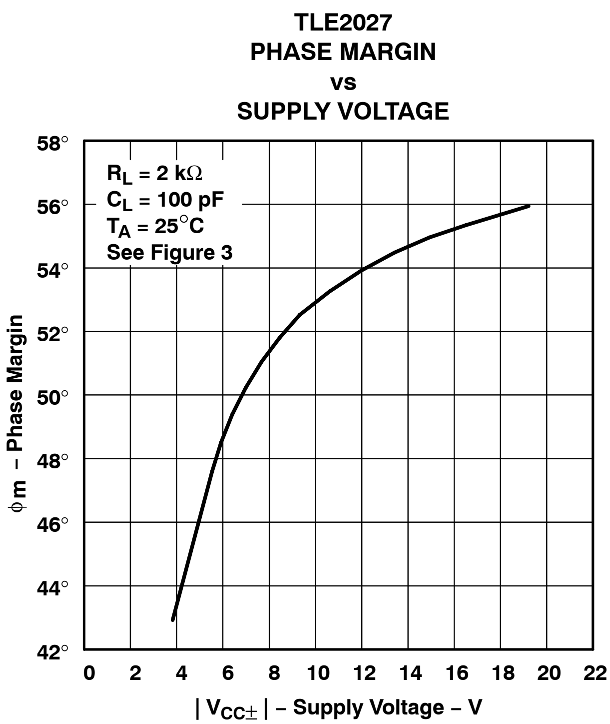


Figure 49

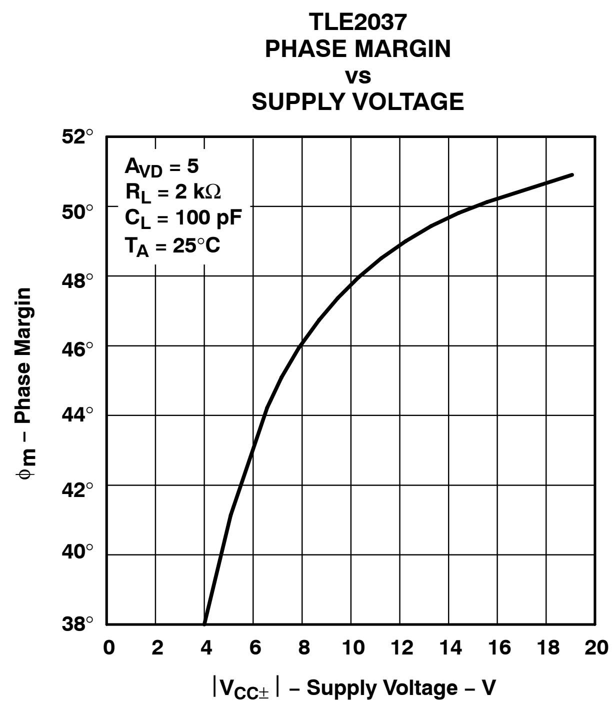


Figure 50

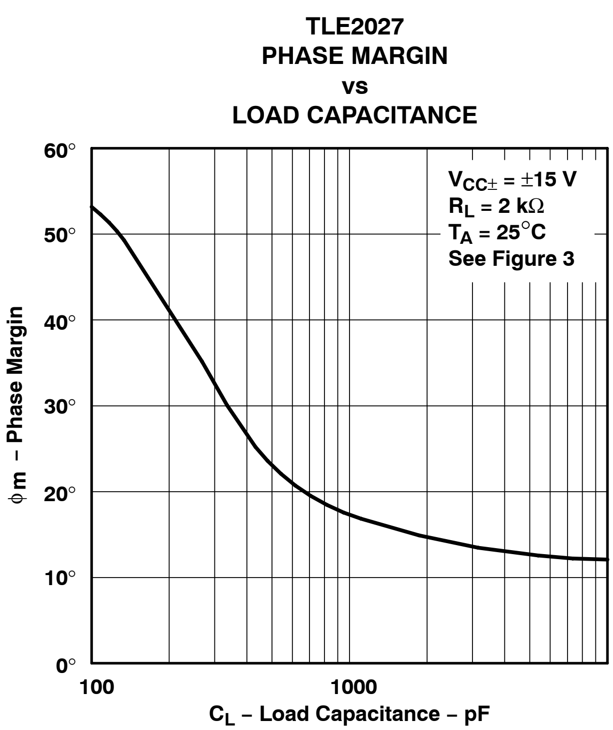


Figure 51

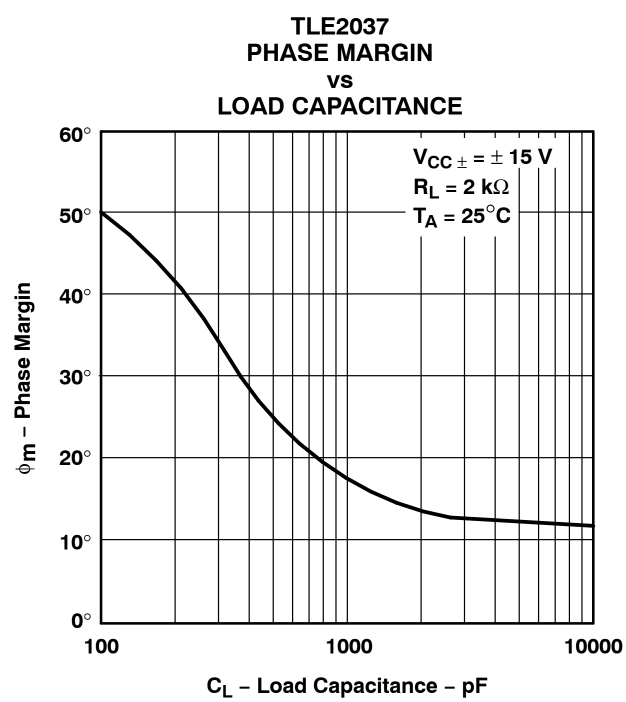


Figure 52

TYPICAL CHARACTERISTICS

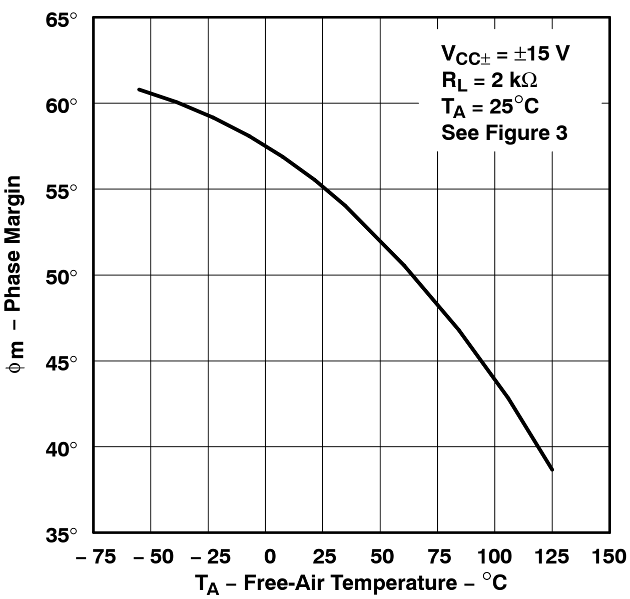


Figure 53

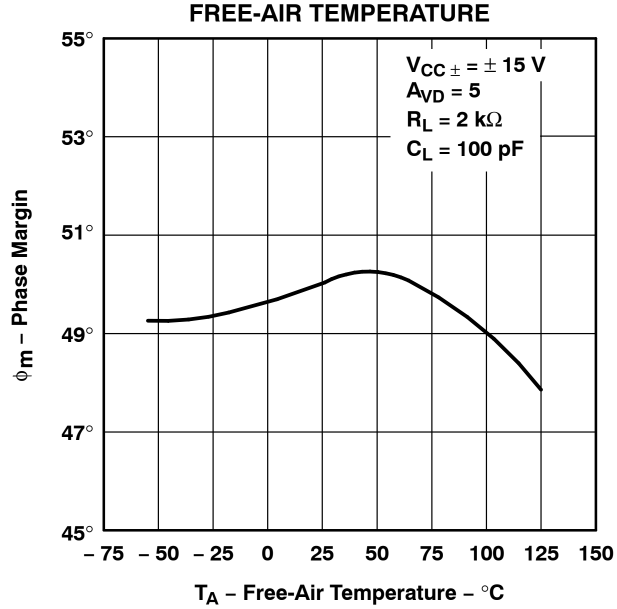


Figure 54

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

input offset voltage nulling

The TLE2027 and TLE2037 series offers external null pins that can be used to further reduce the input offset voltage. The circuits of Figure 55 can be connected as shown if the feature is desired. If external nulling is not needed, the null pins may be left disconnected.

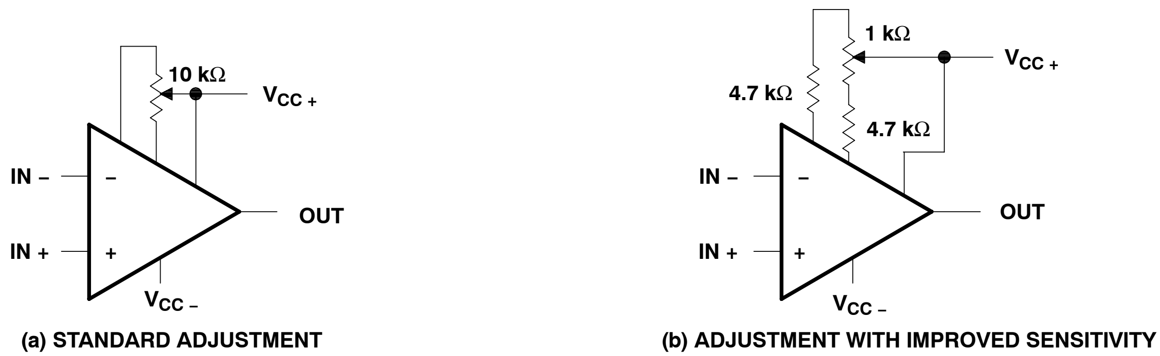


Figure 55. Input Offset Voltage Nulling Circuits

voltage-follower applications

The TLE2027 circuitry includes input-protection diodes to limit the voltage across the input transistors; however, no provision is made in the circuit to limit the current if these diodes are forward biased. This condition can occur when the device is operated in the voltage-follower configuration and driven with a fast, large-signal pulse. It is recommended that a feedback resistor be used to limit the current to a maximum of 1 mA to prevent degradation of the device. Also, this feedback resistor forms a pole with the input capacitance of the device. For feedback resistor values greater than 10 kΩ, this pole degrades the amplifier phase margin. This problem can be alleviated by adding a capacitor (20 pF to 50 pF) in parallel with the feedback resistor (see Figure 56).

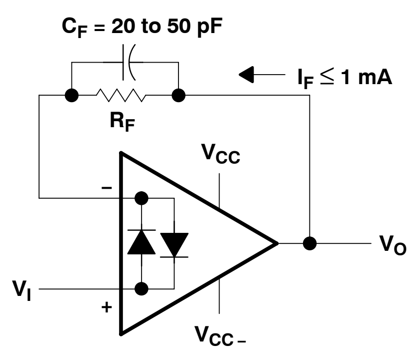


Figure 56. Voltage Follower

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 6) and subcircuit in Figure 57, Figure 58, and Figure 59 were generated using the TLE20x7 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Gain-bandwidth product
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers”, IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

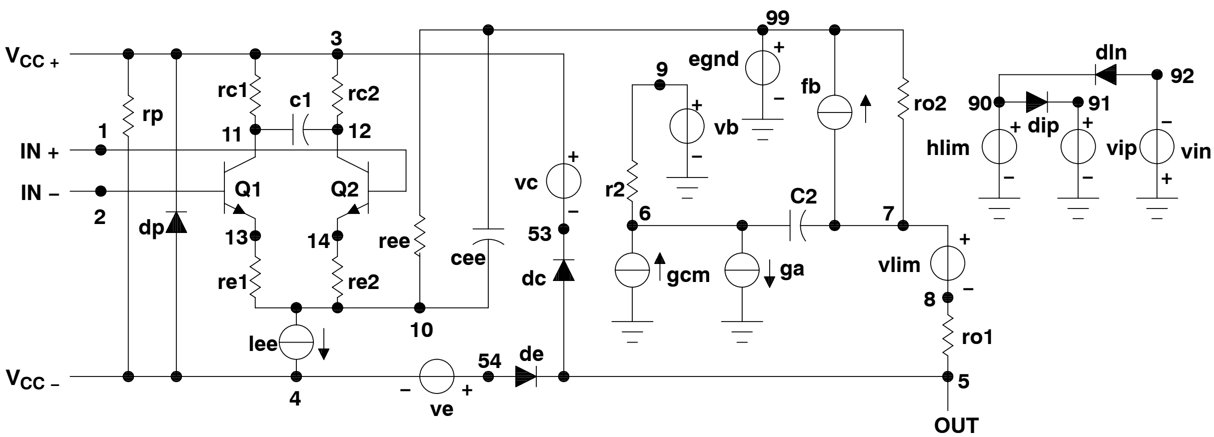


Figure 57. Boyle Macromodel

PSpice and *Parts* are trademarks of MicroSim Corporation.

APPLICATION INFORMATION

macromodel information (continued)

```
.subckt TLE2027 1 2 3 4 5
*
  c1      11   12   4.003E-12
  c2       6    7   20.00E-12
  dc       5   53   dz
  de      54    5   dz
  dlp     90   91   dz
  dln     92   90   dx
  dp       4    3   dz
  egnd    99    0   poly(2) (3,0)
(4,0) 0 5 .5
  fb       7   99   poly(5) vb vc
ve vlp vln 0 954.8E6 -1E9 1E9 1E9
-1E9
  ga       6    0   11  12
2.062E-3
  gcm      0    6   10  99
531.3E-12
  iee     10    4   dc  56.01E-6
  hlim    90    0   vlim 1K
  q1      11    2   13 qx
q2       12    1   14 qx
r2        6    9   100.0E3
rc1       3   11   530.5
rc2       3   12   530.5
re1      13   10   -393.2
re2      14   10   -393.2
ree      10   99   3.571E6
ro1       8    5   25
ro2       7   99   25
rp        3    4   8.013E3
vb        9    0   dc  0
vc        3   53   dc  2.400
ve       54    4   dc  2.100
vlim      7    8   dc  0
vlp      91    0   dc  40
vln       0   92   dc  40
.modeldx D(Is=800.0E-18)
.modelqx NPN(Is=800.0E-18
Bf=7.000E3)
.ends
```

Figure 58. TLE2027 Macromodel Subcircuit

```
.subckt TLE2037 1 2 3 4 5
*
  c1      11   12   4.003E-12
  c2       6    7   7.500E-12
  dc       5   53   dz
  de      54    5   dz
  dlp     90   91   dz
  dln     92   90   dx
  dp       4    3   dz
  egnd    99    0   poly(2)  (3,0)
     (4,0)  0   .5   .5
  fb       7   99   poly(5)  vb vc
     ve vip vln 0 923.4E6 A800E6
     800E6 800E6 A800E6
  ga       6    0   11 12 2.121E-3
  gcm      0    6   10 99 597.7E-12
  iee     10    4   dc 56.26E-6
  hlim    90    0   vlim 1K
  q1      11    2   13 qx
  q2      12    1   14 qz
  r2       6    9   100.0E3
  rc1      3   11   471.5
  rc2      3   12   471.5
  re1     13   10   A448
  re2     14   10   A448
  ree     10   99   3.555E6
  ro1      8    5   25
  ro2      7   99   25
  rp       3    4   8.013E3
  vb       9    0   dc 0
  vc       3   53   dc  2.400
  ve      54    4   dc  2.100
  vlim     7    8   dc  0
  vlp     91    0   dc  40
  vln      0   92   dc  40
.model     dxD(Is=800.0E-18)
.model     qxNPN(Is=800.0E-18
   Bf=7.031E3)
.ends
```

Figure 59. TLE2037 Macromodel Subcircuit

REVISION HISTORY

Changes from Revision B (October 2006) to Revision C

- Changed values of V_n, $V_{N(PP)}$, and I_n 11

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9089601M2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9089601M2A TLE2027MFKB
5962-9089601MPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9089601MPA TLE2027M
5962-9089603Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9089603Q2A TLE2027AMFKB
5962-9089603QPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9089603QPA TLE2027AM
TLE2027AMD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2027AM
TLE2027AMD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2027AM
TLE2027AMFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9089603Q2A TLE2027AMFKB
TLE2027AMFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9089603Q2A TLE2027AMFKB
TLE2027AMJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLE2027 AMJG
TLE2027AMJG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLE2027 AMJG
TLE2027AMJGB	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9089603QPA TLE2027AM
TLE2027AMJGB.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9089603QPA TLE2027AM
TLE2027CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	2027C
TLE2027CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2027C
TLE2027CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2027C
TLE2027CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2027C
TLE2027ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	2027I
TLE2027ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2027I
TLE2027IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	2027I

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLE2027IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2027I
TLE2027MD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2027M
TLE2027MD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2027M
TLE2027MFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9089601M2A TLE2027MFKB
TLE2027MFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9089601M2A TLE2027MFKB
TLE2027MJGB	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9089601MPA TLE2027M
TLE2027MJGB.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9089601MPA TLE2027M
TLE2037AMD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2037AM
TLE2037AMD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2037AM
TLE2037AMDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2037AM
TLE2037AMDG4.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2037AM
TLE2037CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	2037C
TLE2037CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2037C
TLE2037CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	2037C
TLE2037CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2037C
TLE2037ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	2037I
TLE2037ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2037I
TLE2037IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	2037I
TLE2037IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2037I
TLE2037MD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2037M
TLE2037MD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2037M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLE2027, TLE2027M, TLE2037A :

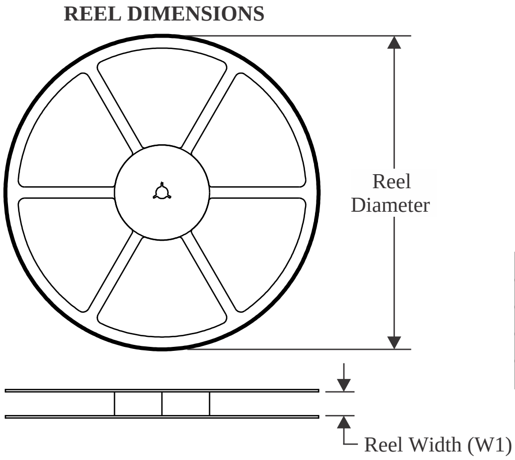
- Catalog : TLE2027
- Automotive : TLE2037A-Q1
- Enhanced Product : TLE2027-EP, TLE2027-EP
- Military : TLE2027M

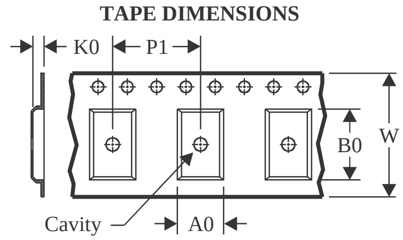
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

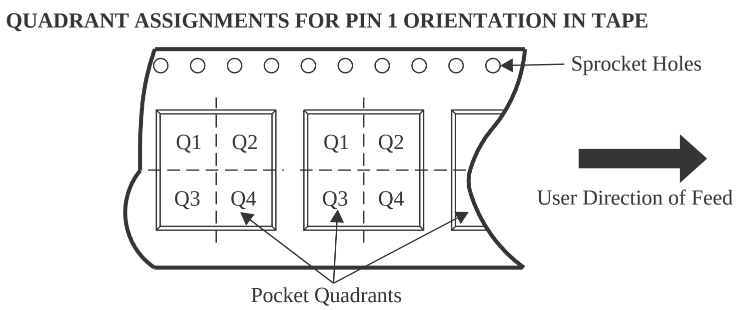
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION





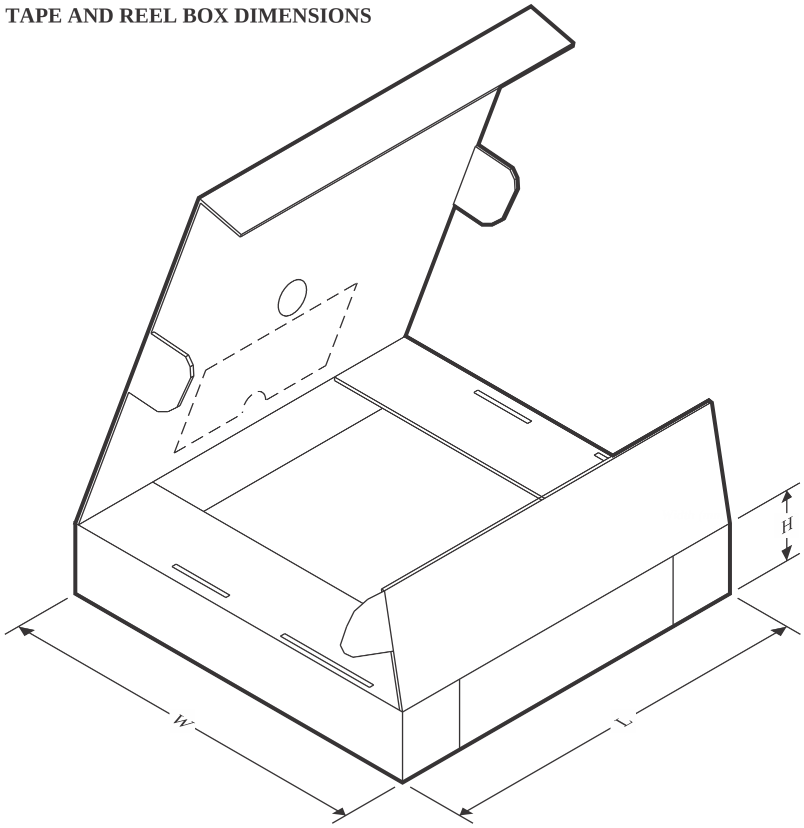
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE2027CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2027IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2037CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2037IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

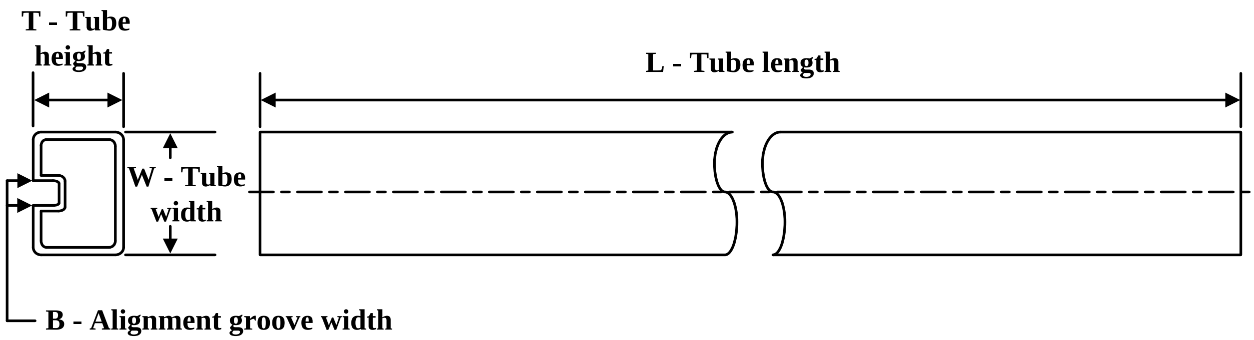
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE2027CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLE2027IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLE2037CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLE2037IDR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9089601M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9089603Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
TLE2027AMD	D	SOIC	8	75	505.46	6.76	3810	4
TLE2027AMD.A	D	SOIC	8	75	505.46	6.76	3810	4
TLE2027AMFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TLE2027AMFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TLE2027CD	D	SOIC	8	75	505.46	6.76	3810	4
TLE2027CD	D	SOIC	8	75	507	8	3940	4.32
TLE2027CD.A	D	SOIC	8	75	507	8	3940	4.32
TLE2027CD.A	D	SOIC	8	75	505.46	6.76	3810	4
TLE2027ID	D	SOIC	8	75	505.46	6.76	3810	4
TLE2027ID	D	SOIC	8	75	507	8	3940	4.32
TLE2027ID.A	D	SOIC	8	75	507	8	3940	4.32
TLE2027ID.A	D	SOIC	8	75	505.46	6.76	3810	4
TLE2027MD	D	SOIC	8	75	505.46	6.76	3810	4
TLE2027MD.A	D	SOIC	8	75	505.46	6.76	3810	4
TLE2027MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TLE2027MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TLE2037AMD	D	SOIC	8	75	505.46	6.76	3810	4
TLE2037AMD.A	D	SOIC	8	75	505.46	6.76	3810	4
TLE2037AMDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLE2037AMDG4.A	D	SOIC	8	75	505.46	6.76	3810	4
TLE2037CD	D	SOIC	8	75	505.46	6.76	3810	4
TLE2037CD	D	SOIC	8	75	507	8	3940	4.32
TLE2037CD.A	D	SOIC	8	75	507	8	3940	4.32
TLE2037CD.A	D	SOIC	8	75	505.46	6.76	3810	4
TLE2037ID	D	SOIC	8	75	505.46	6.76	3810	4
TLE2037ID	D	SOIC	8	75	507	8	3940	4.32
TLE2037ID.A	D	SOIC	8	75	507	8	3940	4.32

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLE2037ID.A	D	SOIC	8	75	505.46	6.76	3810	4
TLE2037MD	D	SOIC	8	75	505.46	6.76	3810	4
TLE2037MD.A	D	SOIC	8	75	505.46	6.76	3810	4

GENERIC PACKAGE VIEW

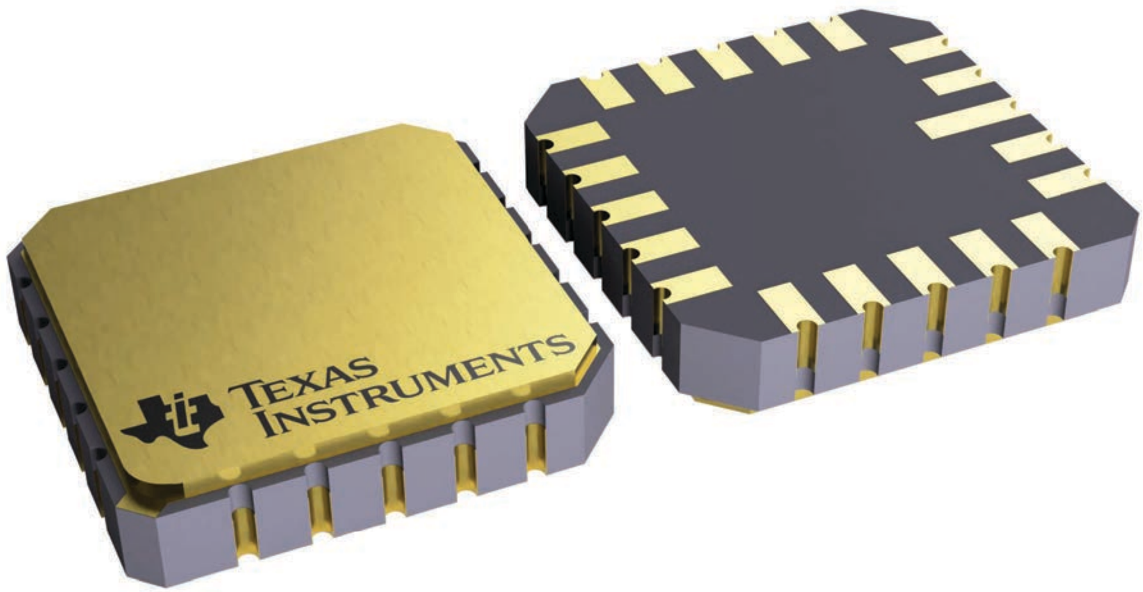
FK 20

LCCC - 2.03 mm max height

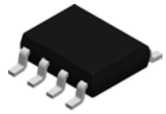
8.89 x 8.89, 1.27 mm pitch

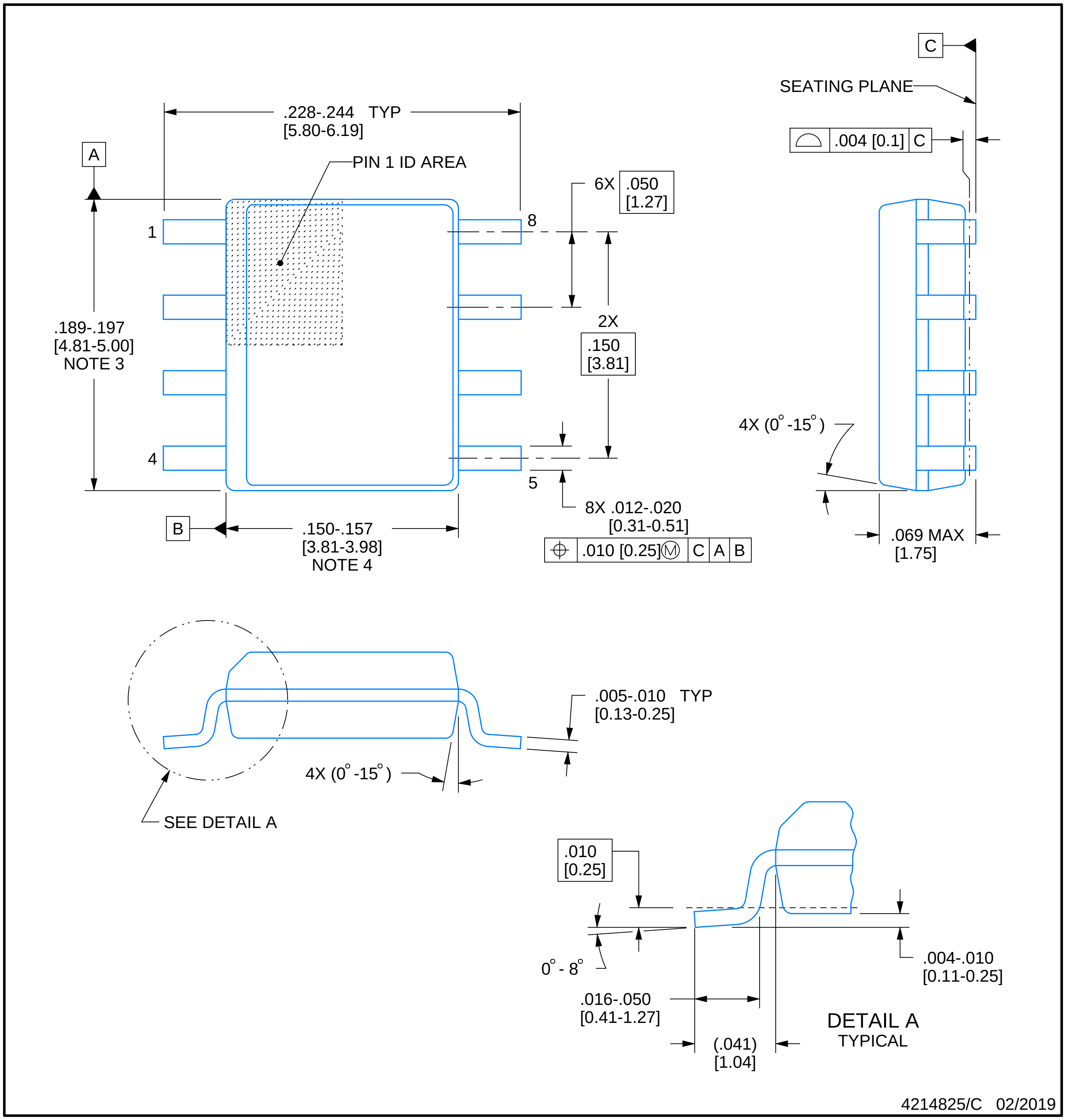
LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



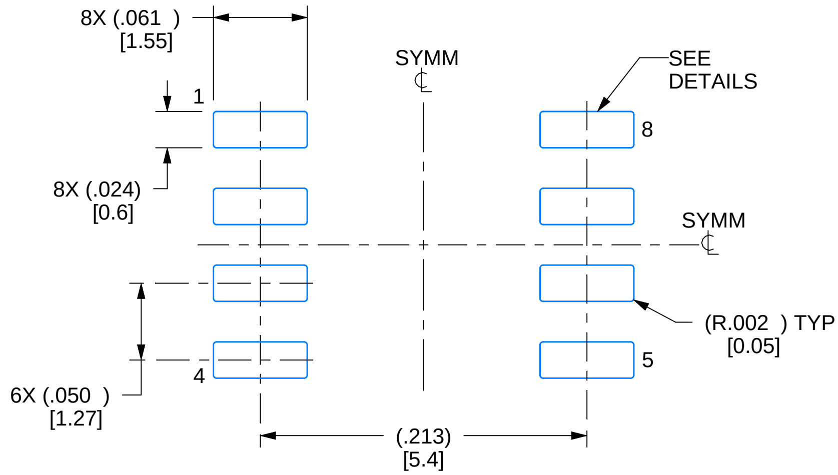
4229370\/A\



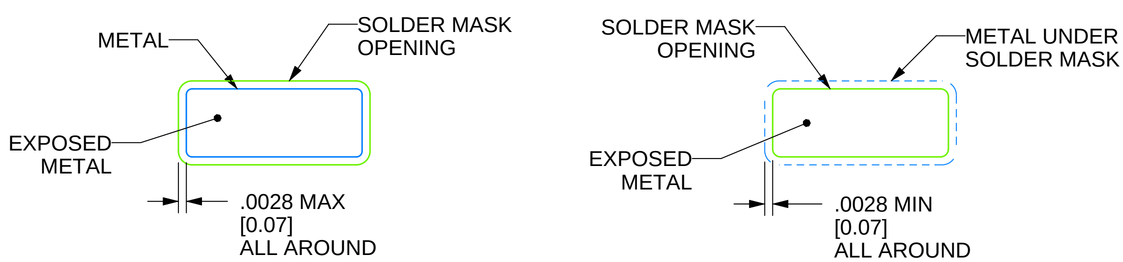


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

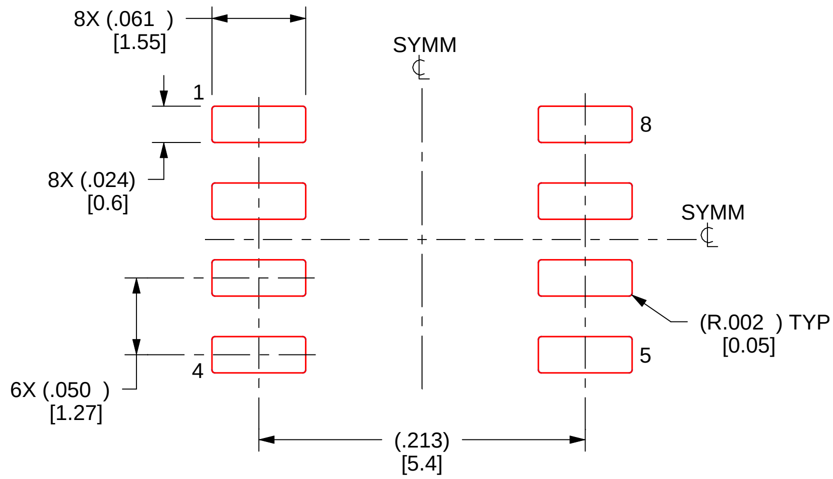
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

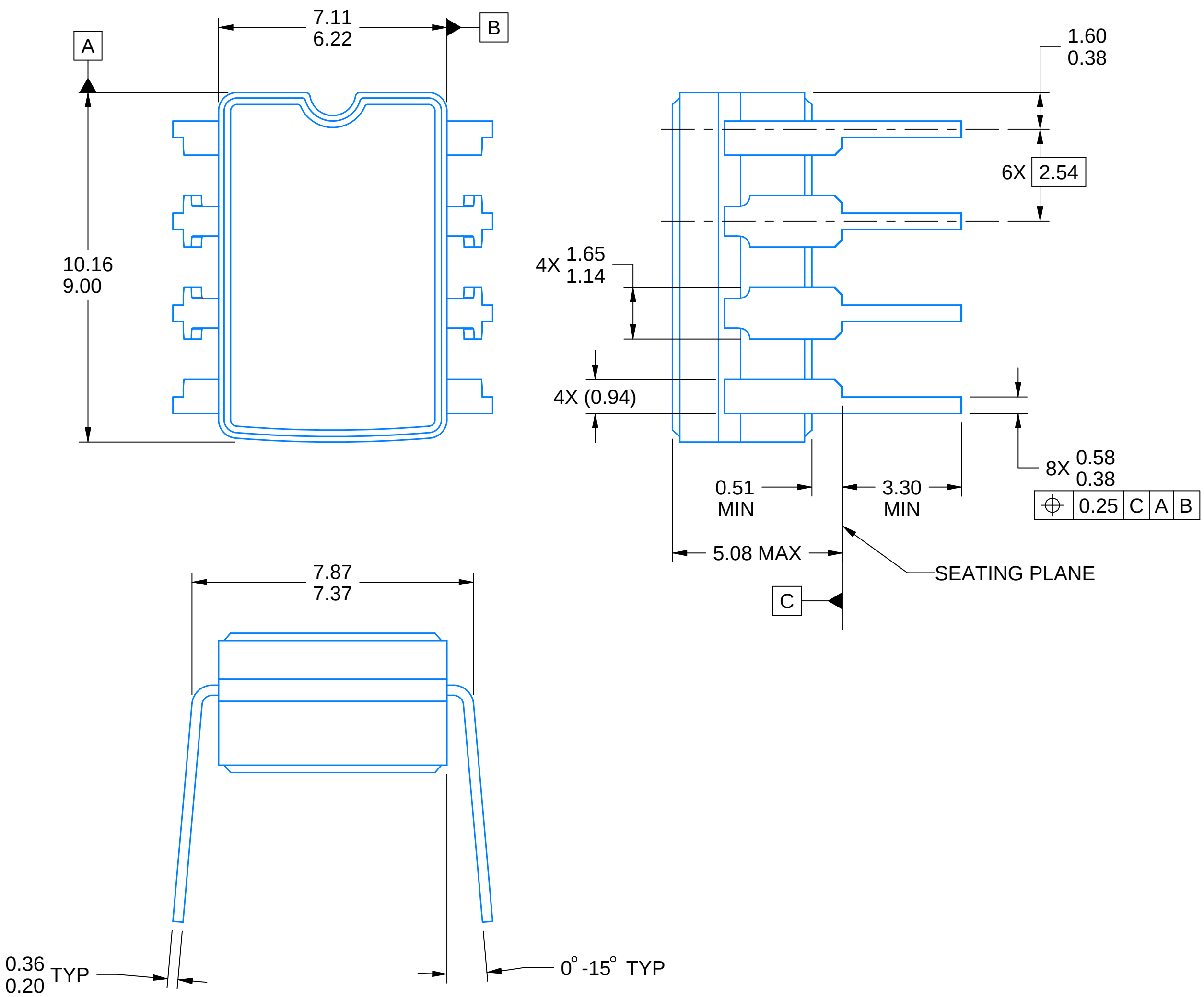


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

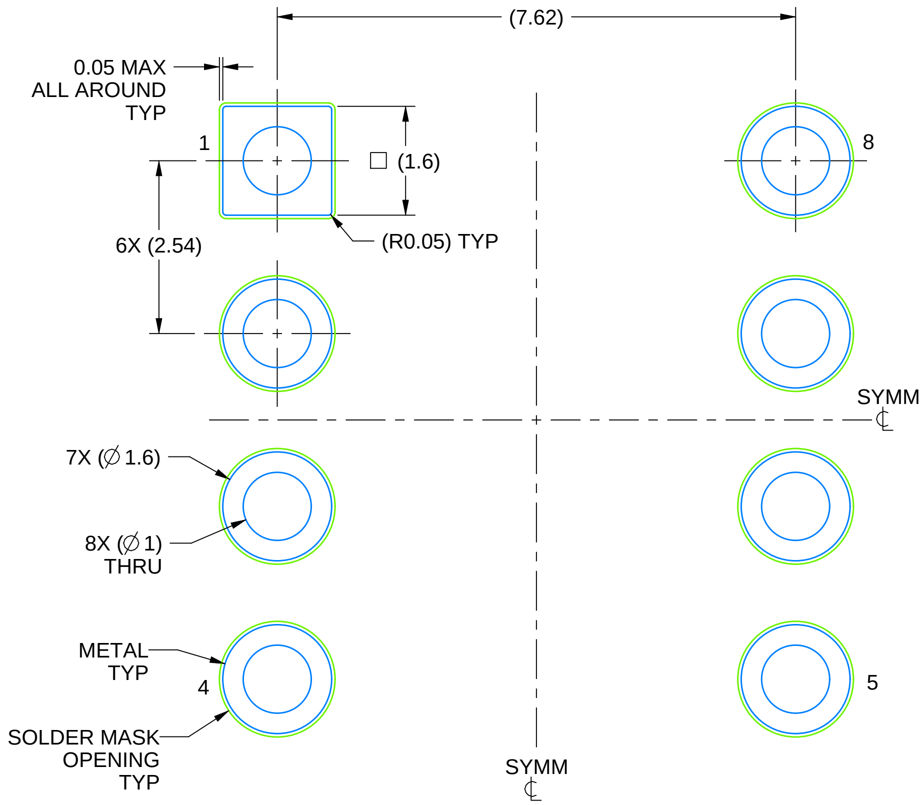
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4230036/A 09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023