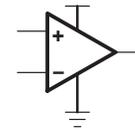


# TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

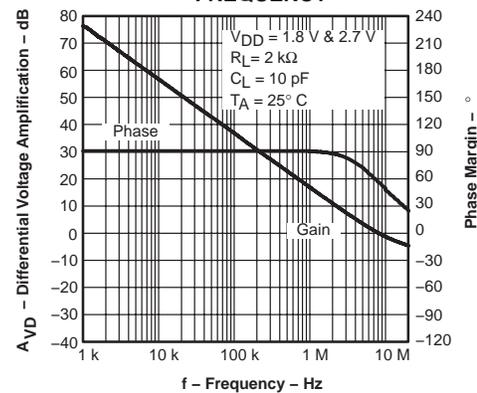
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- Supply Voltage Range . . . 1.8 V to 3.6 V
- Rail-to-Rail Input/Output
- High Bandwidth . . . 8 MHz
- High Slew Rate . . . 4.8 V/ $\mu$ s
- $V_{ICR}$  Exceeds Rails . . .  $-0.2$  V to  $V_{DD} + 0.2$
- Supply Current . . . 650  $\mu$ A/Channel
- Input Noise Voltage . . . 9 nV/ $\sqrt{\text{Hz}}$  at 10 kHz
- Specified Temperature Range:  
0°C to 70°C . . . Commercial Grade  
-40°C to 125°C . . . Industrial Grade
- Ultrasmall Packaging
- Universal Operational Amplifier EVM

## Operational Amplifier



DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE  
VS  
FREQUENCY



## description

The TLV278x single supply operational amplifiers provide rail-to-rail input and output capability. The TLV278x takes the minimum operating supply voltage down to 1.8 V over the extended industrial temperature range ( $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ) while adding the rail-to-rail output swing feature. The TLV278x also provides 8 MHz bandwidth from only 650  $\mu$ A of supply current. The maximum recommended supply voltage is 3.6 V, which allows the devices to be operated from ( $\pm 1.8$  V supplies down to  $\pm 0.9$  V) two rechargeable cells.

The combination of wide bandwidth, low noise, and low distortion makes it ideal for high speed and high resolution data converter applications.

All members are available in PDIP, SOIC, and the newer, smaller SOT-23 (singles), MSOP (duals), and TSSOP (quads).

FAMILY PACKAGE TABLE

DEVICE	$V_{DD}$ [V]	$V_{IO}$ [ $\mu$ V]	$I_{DD}/\text{ch}$ [ $\mu$ A]	$I_{IB}$ [pA]	GBW [MHz]	SLEW RATE [V/ $\mu$ s]	$V_n$ , 1 kHz [nV/ $\sqrt{\text{Hz}}$ ]	$I_O$ [mA]	SHUTDOWN	RAIL-TO-RAIL
TLV278x(A)	1.8–3.6	250	650	2.5	8	5	18	10	Y	I/O
TLV276x(A)	1.8–3.6	550	20	3	0.5	0.23	95	5	Y	I/O
TLV246x(A)	2.7–6	150	550	1300	6.4	1.6	11	25	Y	I/O
TLV247x(A)	2.7–6	250	600	2.5	2.8	1.5	15	20	Y	I/O
TLV244x(A)	2.7–10	300	750	1	1.81	1.4	16	2	—	O
TLV277x(A)	2.5–5.5	360	1000	2	5.1	10.5	17	6	Y	O



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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# TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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## TLV2780 and TLV2781 AVAILABLE OPTIONS(1)

T <sub>A</sub>	V <sub>IOmax</sub> AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE (D)†	SOT-23		PLASTIC DIP (P)
			(DBV)‡	SYMBOL	
0°C to 70°C	3000 μV	TLV2780CD TLV2781CD	TLV2780CDBV TLV2781CDBV	VASC VATC	— —
-40°C to 125°C	3000 μV	TLV2780ID TLV2781ID	TLV2780IDBV TLV2781IDBV	VASI VATI	TLV2780IP TLV2781IP
	2000 μV	TLV2780AID TLV2781AID	— —	— —	— —

† This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2780CDR).

‡ This package is only available taped and reeled. For standard quantities (3,000 pieces per reel), add an **R** suffix (i.e., TLV2780CDBVR). For smaller quantities (250 pieces per mini-reel), add a **T** suffix to the part number (e.g., TLV2780CDBVT).

## TLV2782 and TLV2783 AVAILABLE OPTIONS(1)

T <sub>A</sub>	V <sub>IOmax</sub> AT 25°C	PACKAGED DEVICES						
		SMALL OUTLINE† (D)	MSOP				PLASTIC DIP (N)	PLASTIC DIP (P)
			(DGK)†	SYMBOL	(DGS)†	SYMBOL		
0°C to 70°C	3000 μV	TLV2782CD TLV2783CD	TLV2782CDGK —	xxTIADL —	— TLV2783CDGS	— xxTIADN	— —	
-40°C to 125°C	3000 μV	TLV2782ID TLV2783ID	TLV2782IDGK —	xxTIADM —	— TLV2783IDGS	— xxTIADO	— TLV2783IN	TLV2782IP —
	2000 μV	TLV2782AID TLV2783AID	— —	— —	— —	— —	— —	— —

† This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2782CDR).

## TLV2784 and TLV2785 AVAILABLE OPTIONS(1)

T <sub>A</sub>	V <sub>IOmax</sub> AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP† (PW)
0°C to 70°C	3000 μV	TLV2784CD TLV2785CD	— —	TLV2784CPW TLV2785CPW
-40°C to 125°C	3000 μV	TLV2784ID TLV2785ID	TLV2784IN TLV2785IN	TLV2784IPW TLV2785IPW
	2000 μV	TLV2784AID TLV2785AID	— —	TLV2784AIPW TLV2785AIPW

† This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2784CDR).

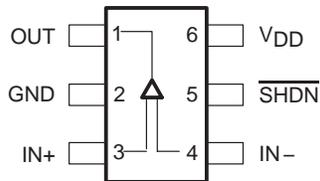
- For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

# TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

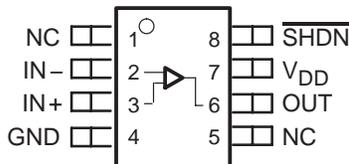
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## TLV278x PACKAGE PINOUTS

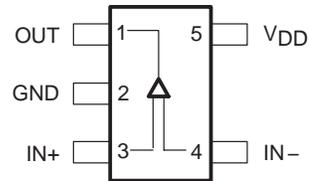
**TLV2780  
DBV PACKAGE  
(TOP VIEW)**



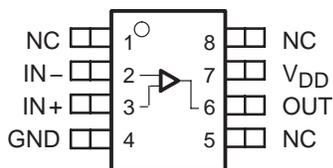
**TLV2780  
D OR P PACKAGE  
(TOP VIEW)**



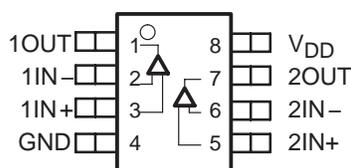
**TLV2781  
DBV PACKAGE  
(TOP VIEW)**



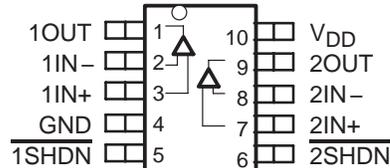
**TLV2781  
D OR P PACKAGE  
(TOP VIEW)**



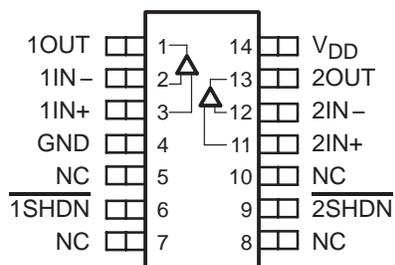
**TLV2782  
D, DGK, OR P PACKAGE  
(TOP VIEW)**



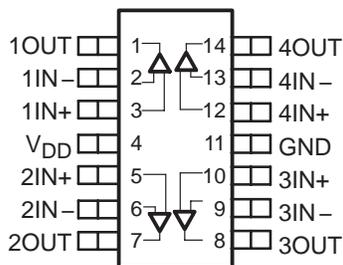
**TLV2783  
DGS PACKAGE  
(TOP VIEW)**



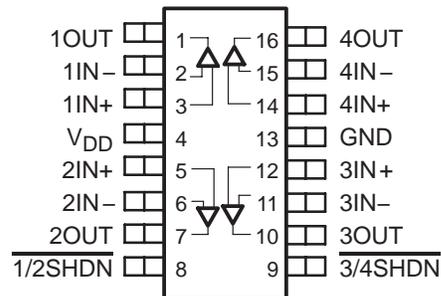
**TLV2783  
D OR N PACKAGE  
(TOP VIEW)**



**TLV2784  
D, N, OR PW PACKAGE  
(TOP VIEW)**



**TLV2785  
D, N, OR PW PACKAGE  
(TOP VIEW)**



NC – No internal connection



**TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA**  
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electrical characteristics at specified free-air temperature,  $V_{DD} = 1.8 \text{ V}, 2.7 \text{ V}$  (unless otherwise noted)

**dc performance**

PARAMETER	TEST CONDITIONS	$T_A$ †	MIN	TYP	MAX	UNIT
$V_{IO}$ Input offset voltage	$V_O = V_{DD}/2,$ $R_L = 2 \text{ k}\Omega,$ $R_S = 50 \Omega$	TLV278x	25°C	250	3000	$\mu\text{V}$
			Full range	4500		
		TLV278xA	25°C	250	2000	
			Full range	3000		
$\alpha_{VIO}$ Temperature coefficient of input offset voltage			8		$\mu\text{V}/^\circ\text{C}$	
CMRR Common-mode rejection ratio	$V_{IC} = 0 \text{ to } V_{DD},$ $R_S = 50 \Omega$	$V_{DD} = 1.8 \text{ V}$	25°C	50	76	dB
			Full range	50		
		$V_{DD} = 2.7 \text{ V}/3.6 \text{ V}$	25°C	55	80	
	Full range		50			
	$V_{IC} = 1.2 \text{ V to } V_{DD},$ $R_S = 50 \Omega$	$V_{DD} = 2.7 \text{ V}/3.6 \text{ V}$	25°C	70	100	
			Full range	70		
$A_{VD}$ Large-signal differential voltage amplification	$R_L = 2 \text{ k}\Omega,$ $V_{O(PP)} = 1 \text{ V}$	$V_{DD} = 1.8 \text{ V}$	25°C	200	600	V/mV
			Full range	50		
		$V_{DD} = 2.7 \text{ V}/3.6 \text{ V}$	25°C	200	1000	
			Full range	70		

† Full range is 0°C to 70°C for the C-suffix and –40°C to 125°C for the I-suffix. If not specified, full range is –40°C to 125°C.

**input characteristics**

PARAMETER	TEST CONDITIONS	$T_A$ †	MIN	TYP	MAX	UNIT
$I_{IO}$ Input offset current	$V_O = V_{DD}/2,$ $R_L = 2 \text{ k}\Omega,$ $R_S = 50 \Omega$	25°C	2.5	15	$\text{pA}$	
		TLV278xC	Full range	100		
		TLV278xI	Full range	300		
$I_{IB}$ Input bias current	$V_O = V_{DD}/2,$ $R_L = 2 \text{ k}\Omega,$ $R_S = 50 \Omega$	25°C	2.5	15	$\text{pA}$	
		TLV278xC	Full range	100		
		TLV278xI	Full range	300		
$r_{i(d)}$ Differential input resistance		25°C	1000		$\text{G}\Omega$	
$C_{i(c)}$ Common-mode input capacitance	$f = 1 \text{ kHz}$	25°C	19		$\text{pF}$	

† Full range is 0°C to 70°C for the C-suffix and –40°C to 125°C for the I-suffix. If not specified, full range is –40°C to 125°C.

**TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA**  
**FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT**  
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electrical characteristics at specified free-air temperature,  $V_{DD} = 1.8\text{ V}, 2.7\text{ V}$  (unless otherwise noted) (continued)

**output characteristics**

PARAMETER	TEST CONDITIONS		$T_A$ †	MIN	TYP	MAX	UNIT	
$V_{OH}$ High-level output voltage	$I_{OH} = -1\text{ mA}$	$V_{DD} = 1.8\text{ V}$	25°C	1.7	1.77		V	
			Full range	1.63				
		$V_{DD} = 2.7\text{ V}$	25°C	2.6	2.68			
			Full range	2.6				
	$I_{OH} = -5\text{ mA}$	$V_{DD} = 1.8\text{ V}$	25°C	1.5	1.55			
			Full range	1.46				
		$V_{DD} = 2.7\text{ V}$	25°C	2.5	2.55			
			Full range	2.45				
$V_{OL}$ Low-level output voltage	$I_{OL} = 1\text{ mA}$		25°C			70	mV	
			Full range			80		
	$I_{OL} = 5\text{ mA}$	$V_{DD} = 1.8\text{ V}$	25°C	180	240			
			Full range	290				
		$V_{DD} = 2.7\text{ V}$	25°C	120	170			
			Full range	200				
	$I_O$ Output current	$V_{DD} = 1.8\text{ V},$ $V_O = 0.5\text{ V from}$	Positive rail	25°C		10		mA
			Negative rail		15			
$V_{DD} = 2.7\text{ V},$ $V_O = 0.5\text{ V from}$		Positive rail	17					
		Negative rail	23					
$I_{OS}$ Short-circuit output current	Sourcing	$V_{DD} = 1.8\text{ V}$	25°C		13	mA		
		$V_{DD} = 2.7\text{ V}$		35				
	Sinking	$V_{DD} = 1.8\text{ V}$		21				
		$V_{DD} = 2.7\text{ V}$		45				

† Full range is 0°C to 70°C for the C-suffix and -40°C to 125°C for the I-suffix. If not specified, full range is -40°C to 125°C.

**power supply**

PARAMETER	TEST CONDITIONS		$T_A$ †	MIN	TYP	MAX	UNIT
$I_{DD}$ Supply current (per channel)	$V_O = V_{DD}/2,$	$\overline{\text{SHDN}} = V_{DD}$	25°C	650	770		$\mu\text{A}$
			Full range			820	
$k_{SVR}$ Supply voltage rejection ratio ( $\Delta V_{DD} / \Delta V_{IO}$ )	$V_{DD} = 1.8\text{ V to } 2.7\text{ V},$ $V_{IC} = V_{DD}/2$	No load,	25°C	60	75		dB
			Full range	58			
	$V_{DD} = 2.7\text{ V to } 3.6\text{ V},$ $V_{IC} = V_{DD}/2$	No load,	25°C	75	90		
			Full range	70			
	$V_{DD} = 1.8\text{ V to } 3.6\text{ V},$ $V_{IC} = V_{DD}/2$	No load,	25°C	65	80		
			Full range	60			

† Full range is 0°C to 70°C for the C-suffix and -40°C to 125°C for the I-suffix. If not specified, full range is -40°C to 125°C.

**TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA**  
**FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT**  
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electrical characteristics at specified free-air temperature,  $V_{DD} = 1.8\text{ V}, 2.7\text{ V}$  (unless otherwise noted) (continued)

**dynamic performance**

PARAMETER		TEST CONDITIONS		$T_A$ †	MIN	TYP	MAX	UNIT
UGBW	Unity gain bandwidth	$R_L = 2\text{ k}\Omega$ ,	$C_L = 25\text{ pF}$	25°C		8		MHz
SR+	Positive slew rate at unity gain	$V_{O(PP)} = 1\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $C_L = 50\text{ pF}$	$V_{DD} = 1.8\text{ V}$	25°C	3.3	4.3	V/ $\mu$ s	
				Full range	3.1			
			$V_{DD} = 2.7\text{ V}$	25°C	3.8	4.8		
				Full range	3.5			
			$V_{DD} = 3.6\text{ V}$	25°C	4	5		
				Full range	3.6			
SR-	Negative slew rate at unity gain	$V_{O(PP)} = 1\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $C_L = 50\text{ pF}$	$V_{DD} = 1.8\text{ V}$	25°C	2.1	2.8		
				Full range	1.89			
			$V_{DD} = 2.7\text{ V}$	25°C	2.2	2.8		
				Full range	1.97			
			$V_{DD} = 3.6\text{ V}$	25°C	3.5	4.2		
				Full range	3.4			
$\phi_m$	Phase margin	$R_L = 2\text{ k}\Omega$ ,	$C_L = 25\text{ pF}$	25°C	58°			
	Gain margin				8		dB	
$t_s$	Settling time	$V_{DD} = 1.8\text{ V}$ , $V_{(STEP)PP} = 1\text{ V}$ , $A_V = -1$ , $C_L = 10\text{ pF}$ , $R_L = 2\text{ k}\Omega$	0.1%	25°C	1.7		$\mu$ s	
			0.01%		2.8			
		$V_{DD} = 2.7\text{ V}$ , $V_{(STEP)PP} = 1\text{ V}$ , $A_V = -1$ , $C_L = 10\text{ pF}$ , $R_L = 2\text{ k}\Omega$	0.1%		1.7			
			0.01%		2.4			

† Full range is 0°C to 70°C for the C-suffix and -40°C to 125°C for the I-suffix. If not specified, full range is -40°C to 125°C.

**noise/distortion performance**

PARAMETER		TEST CONDITIONS		$T_A$	MIN	TYP	MAX	UNIT
THD + N	Total harmonic distortion plus noise	$V_{O(PP)} = V_{DD}/2$ , $R_L = 2\text{ k}\Omega$ , $f = 10\text{ kHz}$	$A_V = 1$	25°C	0.055%			
			$A_V = 10$		0.08%			
			$A_V = 100$		0.45%			
$V_n$	Equivalent input noise voltage	$f = 1\text{ kHz}$	$f = 10\text{ kHz}$	25°C	18		nV/ $\sqrt{\text{Hz}}$	
			$f = 10\text{ kHz}$		9			
$I_n$	Equivalent input noise current	$f = 1\text{ kHz}$		25°C	0.9		fA/ $\sqrt{\text{Hz}}$	

**shutdown characteristics**

PARAMETER		TEST CONDITIONS	$T_A$ †	MIN	TYP	MAX	UNIT
$I_{DD(SHDN)}$	Supply current, per channel in shutdown mode (TLV2780, TLV2783, TLV2785)	$\overline{\text{SHDN}} = 0\text{ V}$	25°C	900	1400	1700	nA
			Full range				
$t_{(on)}$	Amplifier turnon time‡	$R_L = 2\text{ k}\Omega$	25°C	800			ns
$t_{(off)}$	Amplifier turnoff time‡	$R_L = 2\text{ k}\Omega$		200			

† Full range is 0°C to 70°C for the C-suffix and -40°C to 125°C for the I-suffix. If not specified, full range is -40°C to 125°C.

‡ Disable time and enable time are defined as the interval between application of the logic signal to  $\overline{\text{SHDN}}$  and the point at which the supply current has reached half its final value.

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**TYPICAL CHARACTERISTICS**

**Table of Graphs**

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$V_{IO}$	Input offset voltage	vs Common-mode input voltage	1, 2
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$I_{DD(SHDN)}$	Shutdown supply current	vs Supply voltage	27
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# TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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## TYPICAL CHARACTERISTICS

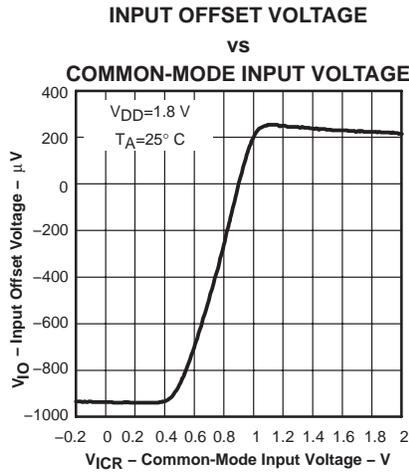


Figure 1

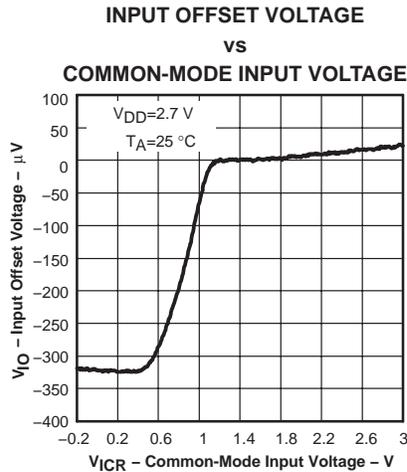


Figure 2

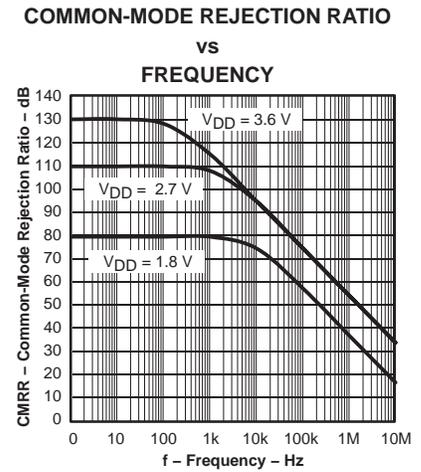


Figure 3

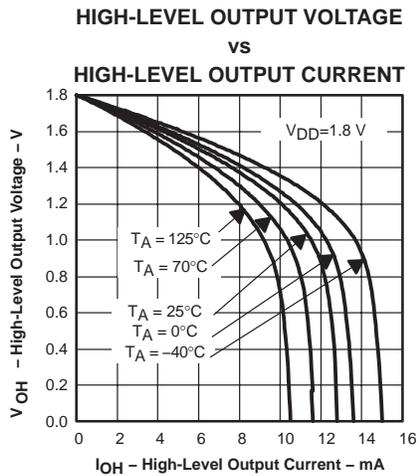


Figure 4

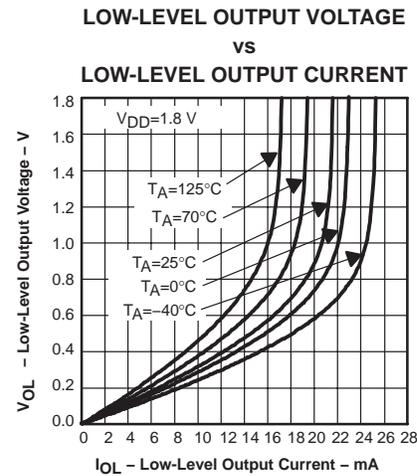


Figure 5

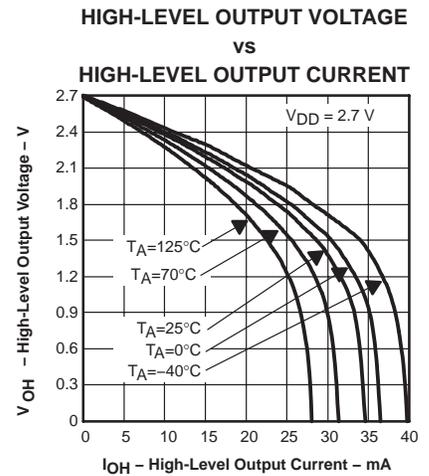


Figure 6

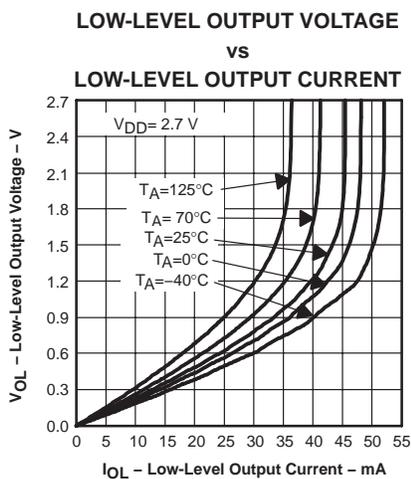


Figure 7

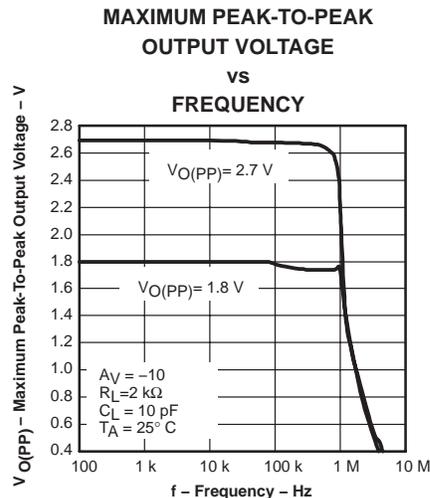


Figure 8

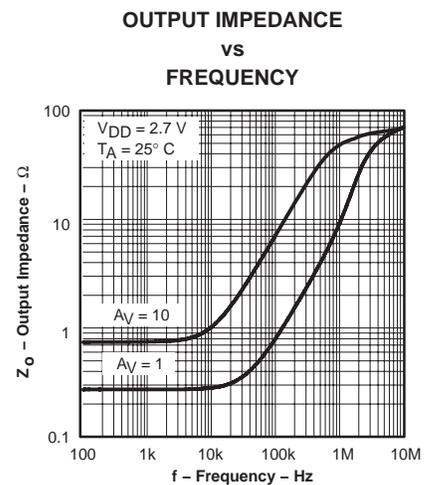


Figure 9

# TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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## TYPICAL CHARACTERISTICS

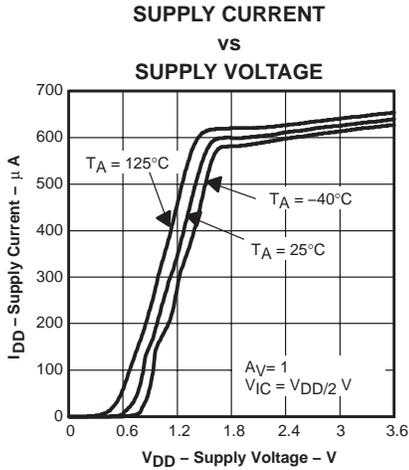


Figure 10

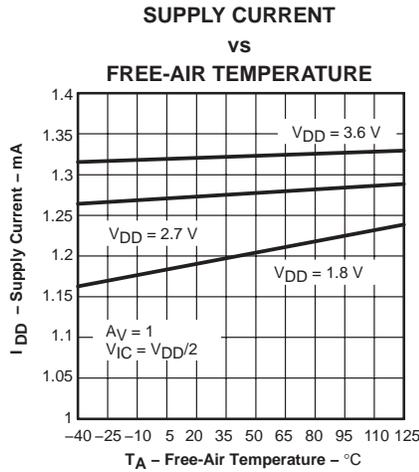


Figure 11

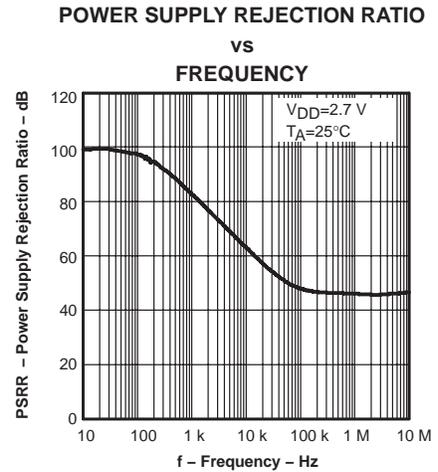


Figure 12

### DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE

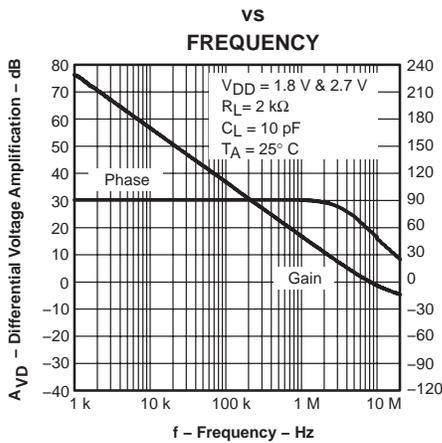


Figure 13

### GAIN-BANDWIDTH PRODUCT

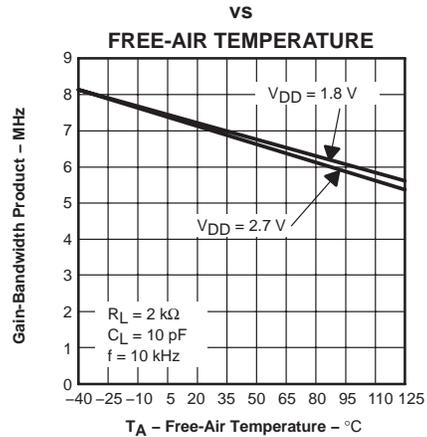


Figure 14

### SLEW RATE

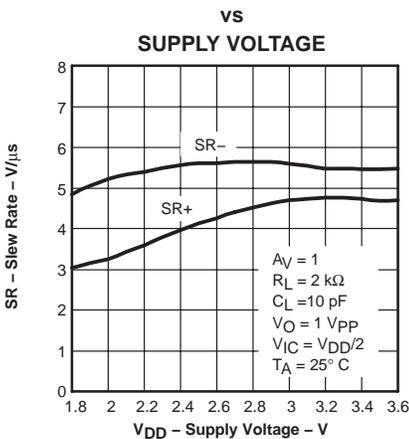


Figure 15

### SLEW RATE

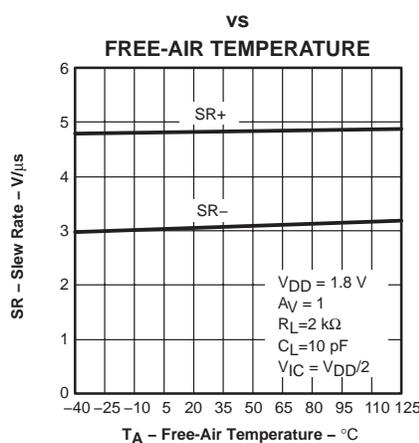


Figure 16

### SLEW RATE

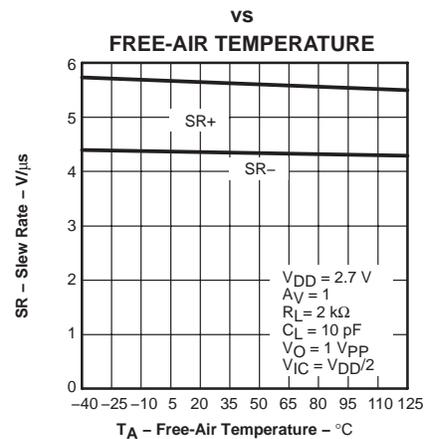


Figure 17

# TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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## TYPICAL CHARACTERISTICS

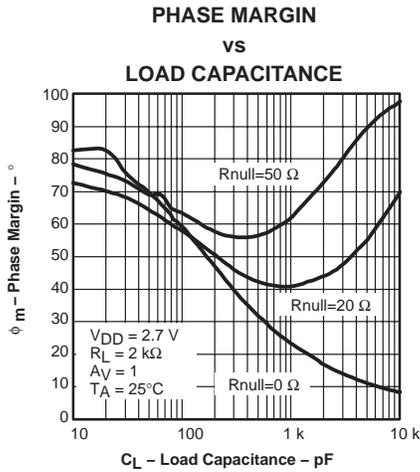


Figure 18

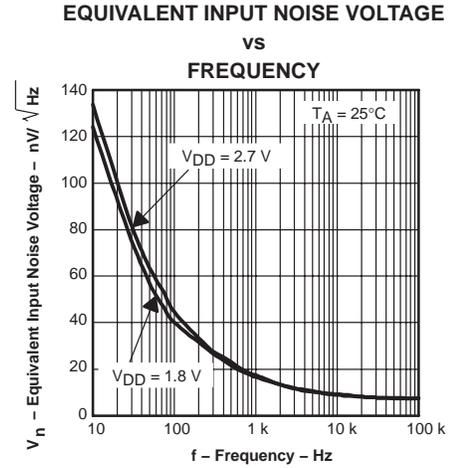


Figure 19

### VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

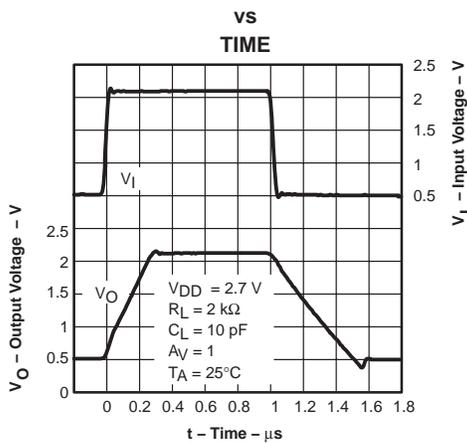


Figure 20

### VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

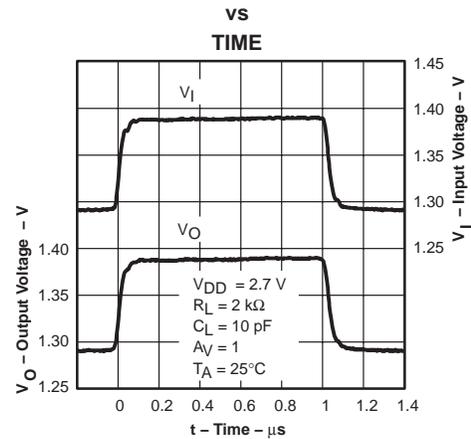


Figure 21

### INVERTING LARGE-SIGNAL PULSE RESPONSE

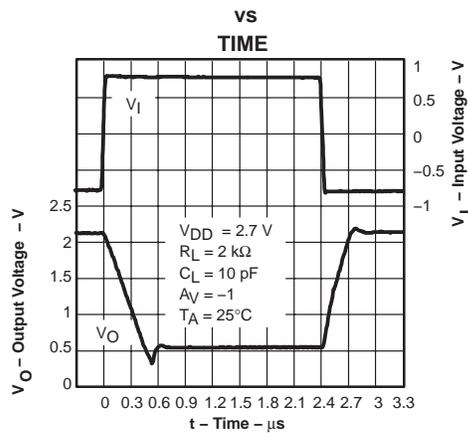


Figure 22

### INVERTING SMALL-SIGNAL PULSE RESPONSE

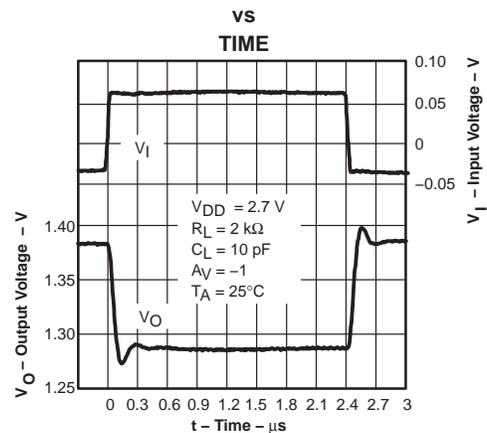
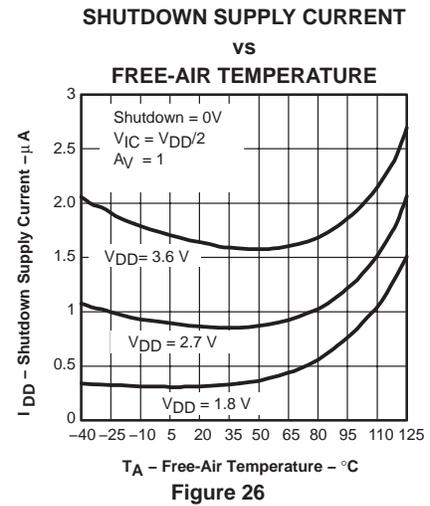
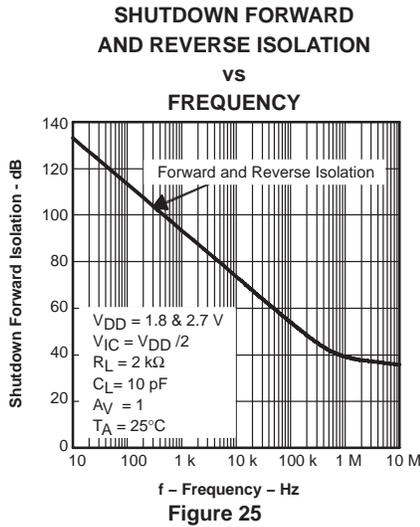
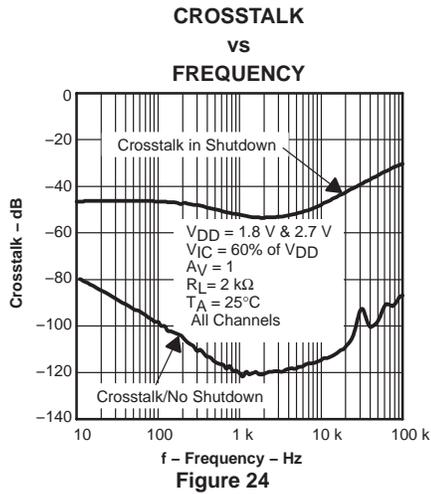


Figure 23

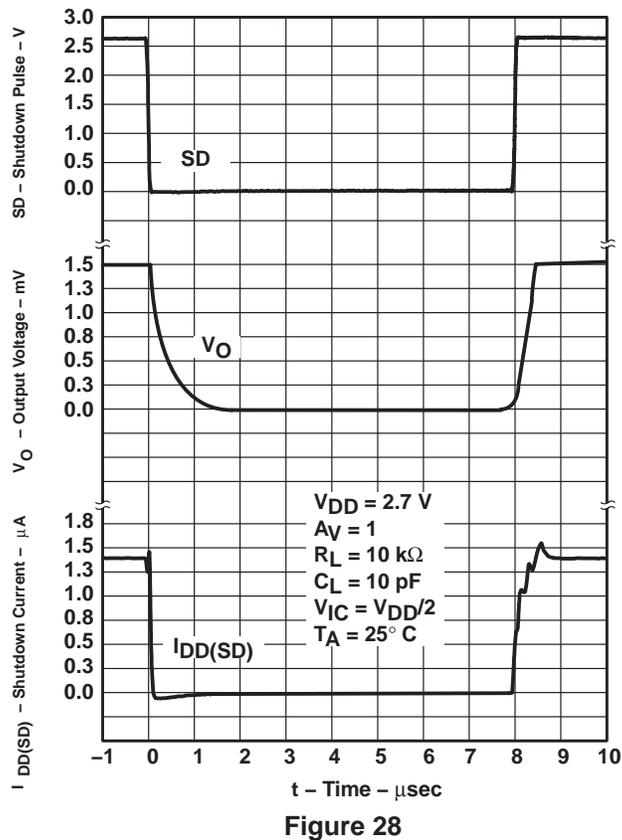
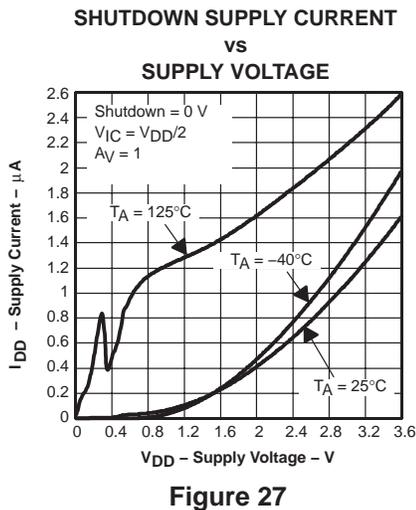
# TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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## TYPICAL CHARACTERISTICS



## SHUTDOWN SUPPLY CURRENT / OUTPUT VOLTAGE vs TIME



PARAMETER MEASUREMENT INFORMATION

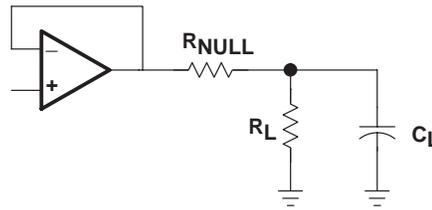


Figure 29

APPLICATION INFORMATION

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series ( $R_{NULL}$ ) with the output of the amplifier, as shown in Figure 30.

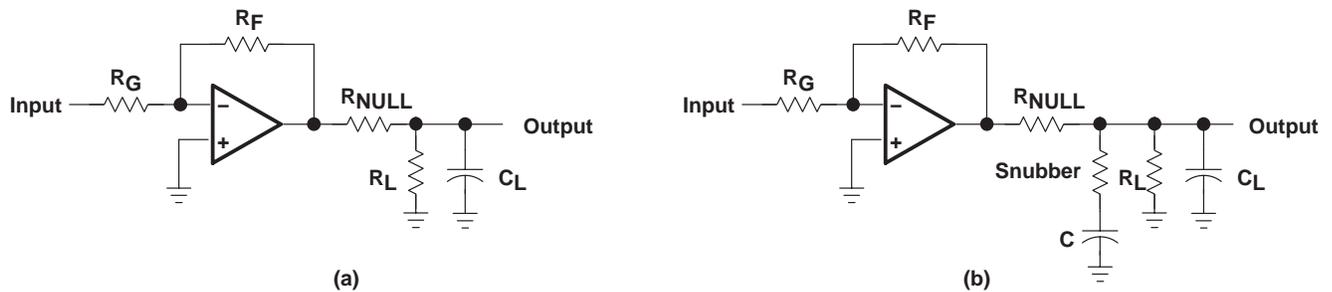


Figure 30. Driving a Capacitive Load

offset voltage

The output offset voltage, ( $V_{OO}$ ) is the sum of the input offset voltage ( $V_{IO}$ ) and both input bias currents ( $I_{IB}$ ) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

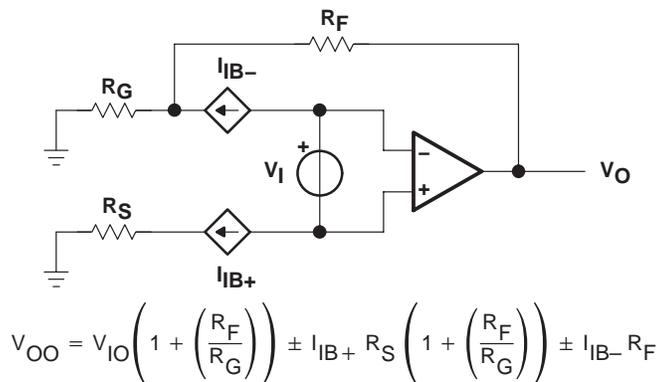


Figure 31. Output Offset Voltage Model

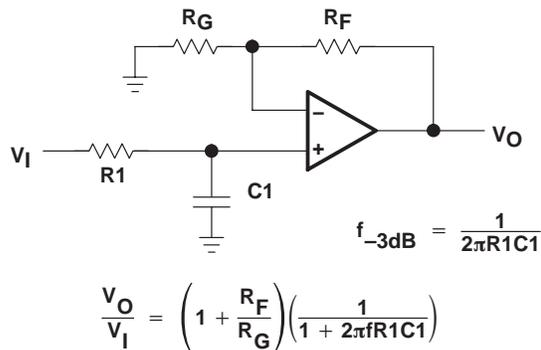
**TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA**  
**FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT**  
**OPERATIONAL AMPLIFIERS WITH SHUTDOWN**

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**APPLICATION INFORMATION**

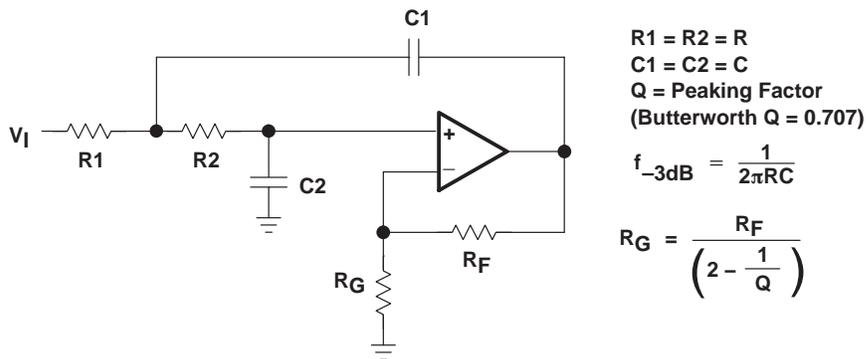
**general configurations**

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 32).



**Figure 32. Single-Pole Low-Pass Filter**

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.



**Figure 33. 2-Pole Low-Pass Sallen-Key Filter**

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## APPLICATION INFORMATION

### circuit layout considerations

To achieve the levels of high performance of the TLV278x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8- $\mu$ F tantalum capacitor in parallel with a 0.1- $\mu$ F ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- $\mu$ F ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- $\mu$ F capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

### shutdown function

Three members of the TLV278x family (TLV2780/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 900 nA/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown.

# TLV2780, TLV2781, TLV2782, TLV2783, TLV2784, TLV2785, TLV278xA FAMILY OF 1.8 V HIGH-SPEED RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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## APPLICATION INFORMATION

### general power dissipation considerations

For a given  $\theta_{JA}$ , the maximum power dissipation is shown in Figure 34 and is calculated by the following formula:

$$P_D = \left( \frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

$P_D$  = Maximum power dissipation of TLV278x IC (watts)

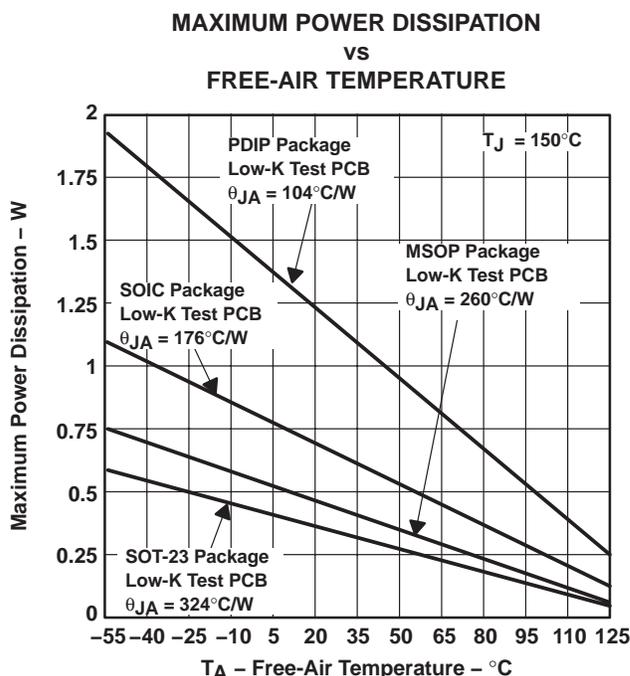
$T_{MAX}$  = Absolute maximum junction temperature (150°C)

$T_A$  = Free-ambient air temperature (°C)

$\theta_{JA}$  =  $\theta_{JC} + \theta_{CA}$

$\theta_{JC}$  = Thermal coefficient from junction to case

$\theta_{CA}$  = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

**Figure 34. Maximum Power Dissipation vs Free-Air Temperature**



**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TLV2780CDBVR</a>	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	VASC
TLV2780CDBVR.A	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	VASC
<a href="#">TLV2780CDBVT</a>	Obsolete	Production	SOT-23 (DBV)   6	-	-	Call TI	Call TI	0 to 70	VASC
<a href="#">TLV2780IDBVR</a>	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VASI
TLV2780IDBVR.A	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VASI
<a href="#">TLV2780IDBVT</a>	Active	Production	SOT-23 (DBV)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VASI
TLV2780IDBVT.A	Active	Production	SOT-23 (DBV)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VASI
<a href="#">TLV2780IDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T2780I
TLV2780IDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T2780I
<a href="#">TLV2781CDBVR</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	VATC
TLV2781CDBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	VATC
<a href="#">TLV2781CDBVT</a>	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	VATC
TLV2781CDBVT.A	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	VATC
<a href="#">TLV2781ID</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T2781I
TLV2781ID.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T2781I
<a href="#">TLV2781IDBVR</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VATI
TLV2781IDBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VATI
<a href="#">TLV2781IDBVT</a>	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VATI
TLV2781IDBVT.A	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VATI
<a href="#">TLV2781IDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T2781I
TLV2781IDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T2781I
<a href="#">TLV2782AID</a>	Obsolete	Production	SOIC (D)   8	-	-	Call TI	Call TI	-40 to 125	2782AI
<a href="#">TLV2782CD</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2782C
TLV2782CD.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2782C
TLV2782CDG4	Active	Production	SOIC (D)   8	75   TUBE	-	Call TI	Call TI	0 to 70	
<a href="#">TLV2782CDGK</a>	Active	Production	VSSOP (DGK)   8	80   TUBE	Yes	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	0 to 70	ADL
TLV2782CDGK.A	Active	Production	VSSOP (DGK)   8	80   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ADL
<a href="#">TLV2782CDGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	0 to 70	ADL
TLV2782CDGKR.A	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ADL

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TLV2782CDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2782C
TLV2782CDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2782C
<a href="#">TLV2782ID</a>	Obsolete	Production	SOIC (D)   8	-	-	Call TI	Call TI	-40 to 125	2782I
<a href="#">TLV2782IDGK</a>	Active	Production	VSSOP (DGK)   8	80   TUBE	Yes	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ADM
TLV2782IDGK.A	Active	Production	VSSOP (DGK)   8	80   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ADM
<a href="#">TLV2782IDGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ADM
TLV2782IDGKR.A	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ADM
<a href="#">TLV2782IDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2782I
TLV2782IDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2782I
<a href="#">TLV2782IP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV2782IP
TLV2782IP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV2782IP
<a href="#">TLV2783IDGS</a>	Obsolete	Production	VSSOP (DGS)   10	-	-	Call TI	Call TI	-40 to 125	ADO
<a href="#">TLV2783IDGSR</a>	Active	Production	VSSOP (DGS)   10	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ADO
TLV2783IDGSR.A	Active	Production	VSSOP (DGS)   10	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ADO
<a href="#">TLV2783IN</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV2783I
TLV2783IN.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV2783I
<a href="#">TLV2784AID</a>	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2784AI
TLV2784AID.A	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2784AI
<a href="#">TLV2784AIDR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2784AI
TLV2784AIDR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2784AI
<a href="#">TLV2784CPWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2784C
TLV2784CPWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2784C
<a href="#">TLV2784ID</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 125	TLV2784I
<a href="#">TLV2784IDR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2784I
TLV2784IDR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2784I
<a href="#">TLV2784IPW</a>	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2784I
TLV2784IPW.A	Active	Production	TSSOP (PW)   14	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2784I
<a href="#">TLV2784IPWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2784I
TLV2784IPWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2784I
<a href="#">TLV2785AID</a>	Active	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2785AI
TLV2785AID.A	Active	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2785AI

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TLV2785CPWR</a>	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2785C
TLV2785CPWR.A	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2785C
<a href="#">TLV2785IN</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV2785I
TLV2785IN.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV2785I
<a href="#">TLV2785IPWR</a>	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2785I
TLV2785IPWR.A	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2785I

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

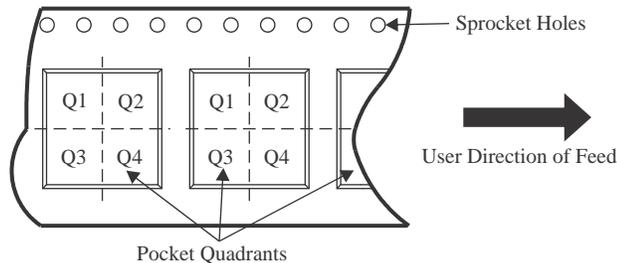
**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2780CDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2780IDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2780IDBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2780IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2781CDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2781CDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2781IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2781IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2781IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2782CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2782CDGKR	VSSOP	DGK	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2782CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2782CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2782IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2782IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2782IDGKR	VSSOP	DGK	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2782IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2783IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2784AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2784CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2784CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2784IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2784IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2784IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2784IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2785CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2785IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

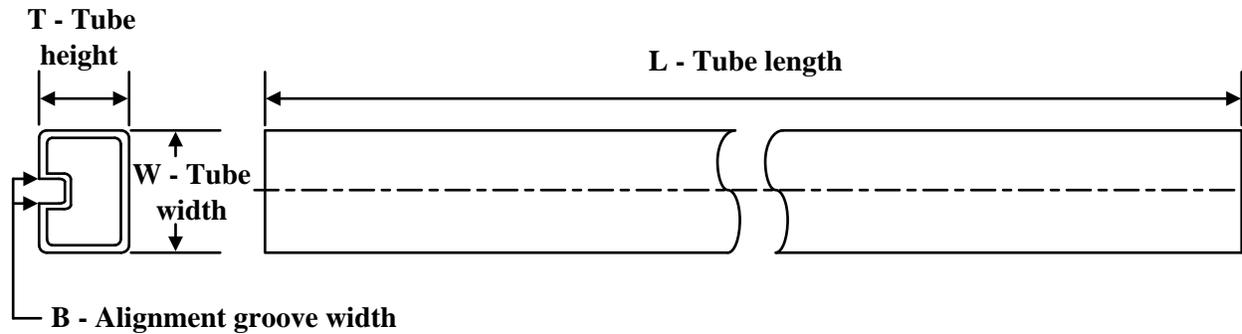
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2780CDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV2780IDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV2780IDBVT	SOT-23	DBV	6	250	210.0	185.0	35.0
TLV2780IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2781CDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV2781CDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV2781IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV2781IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV2781IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2782CDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV2782CDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV2782CDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV2782CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV2782IDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV2782IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV2782IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV2782IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2783IDGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2784AIDR	SOIC	D	14	2500	350.0	350.0	43.0
TLV2784CPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TLV2784CPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TLV2784IDR	SOIC	D	14	2500	350.0	350.0	43.0
TLV2784IDR	SOIC	D	14	2500	353.0	353.0	32.0
TLV2784IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TLV2784IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TLV2785CPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TLV2785IPWR	TSSOP	PW	16	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV2781ID	D	SOIC	8	75	505.46	6.76	3810	4
TLV2781ID	D	SOIC	8	75	507	8	3940	4.32
TLV2781ID.A	D	SOIC	8	75	507	8	3940	4.32
TLV2781ID.A	D	SOIC	8	75	505.46	6.76	3810	4
TLV2782CD	D	SOIC	8	75	507	8	3940	4.32
TLV2782CD	D	SOIC	8	75	505.46	6.76	3810	4
TLV2782CD.A	D	SOIC	8	75	505.46	6.76	3810	4
TLV2782CD.A	D	SOIC	8	75	507	8	3940	4.32
TLV2782CDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
TLV2782CDGK.A	DGK	VSSOP	8	80	330	6.55	500	2.88
TLV2782IDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
TLV2782IDGK.A	DGK	VSSOP	8	80	330	6.55	500	2.88
TLV2782IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2782IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLV2783IN	N	PDIP	14	25	506	13.97	11230	4.32
TLV2783IN.A	N	PDIP	14	25	506	13.97	11230	4.32
TLV2784AID	D	SOIC	14	50	505.46	6.76	3810	4
TLV2784AID.A	D	SOIC	14	50	505.46	6.76	3810	4
TLV2784IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLV2784IPW.A	PW	TSSOP	14	90	530	10.2	3600	3.5
TLV2785AID	D	SOIC	16	40	505.46	6.76	3810	4
TLV2785AID.A	D	SOIC	16	40	505.46	6.76	3810	4
TLV2785IN	N	PDIP	16	25	506	13.97	11230	4.32
TLV2785IN.A	N	PDIP	16	25	506	13.97	11230	4.32



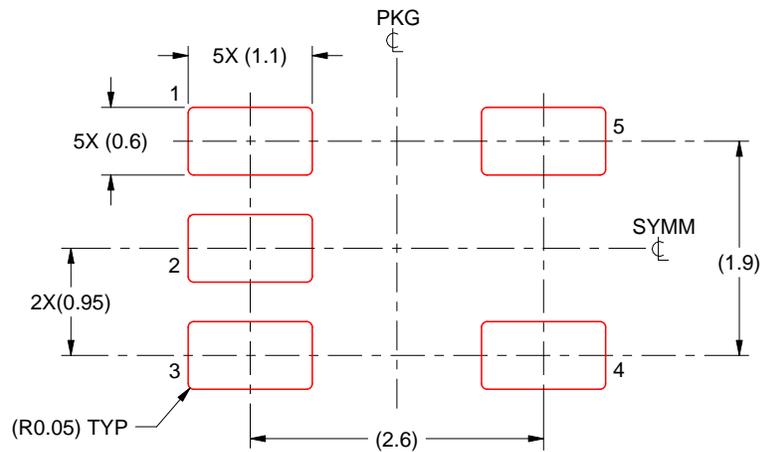


# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

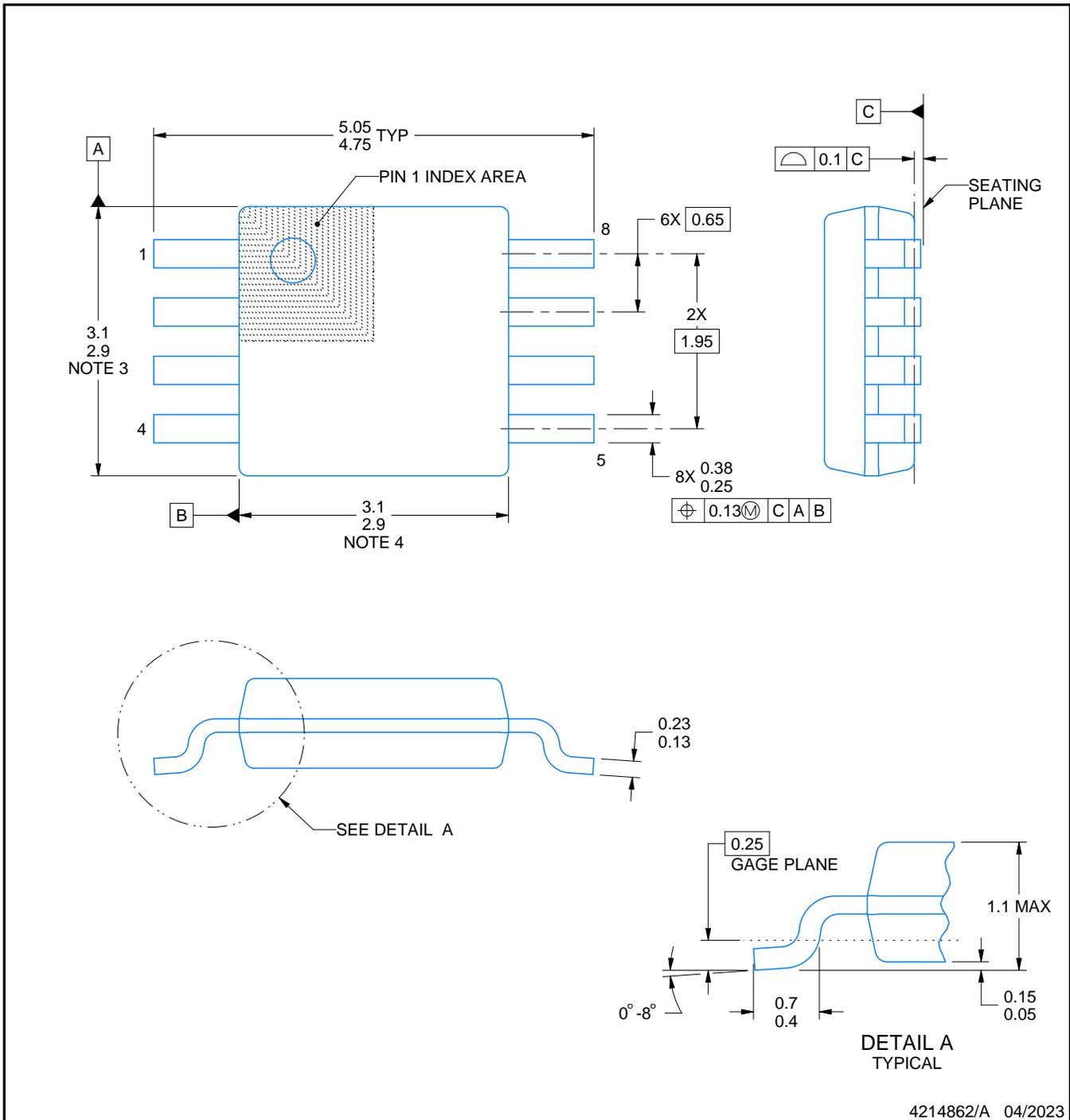
# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

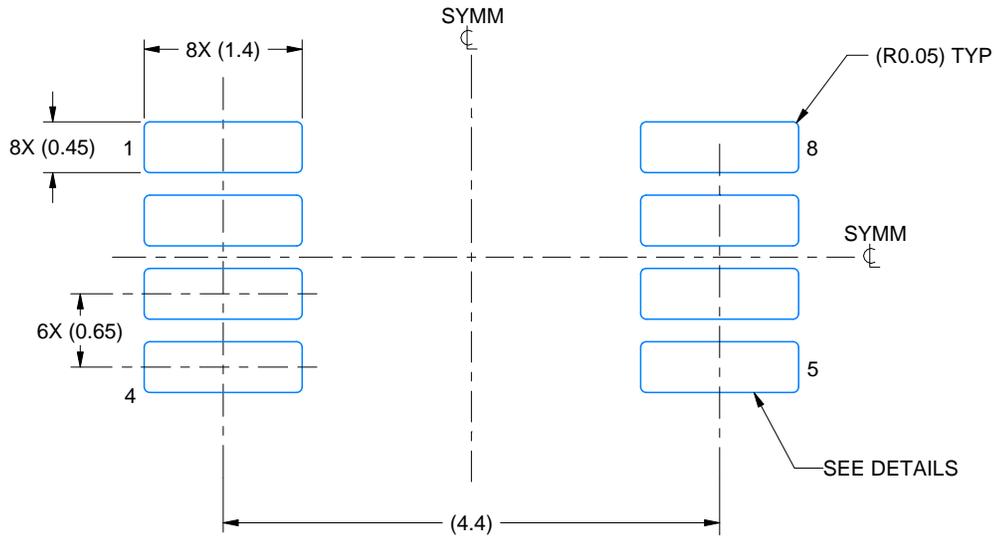
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

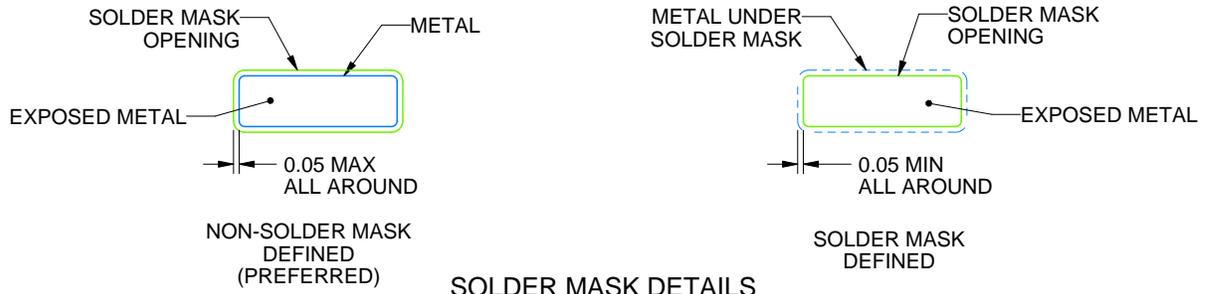
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

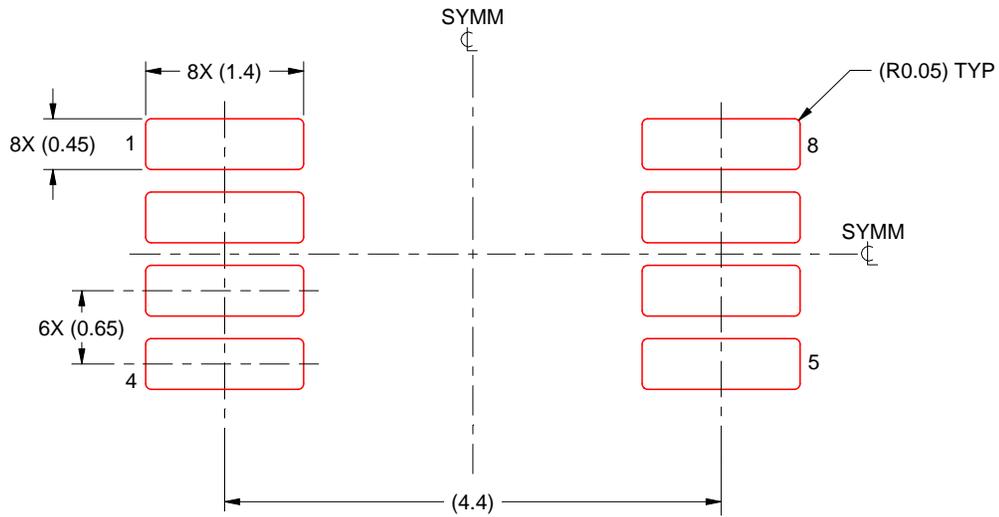
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

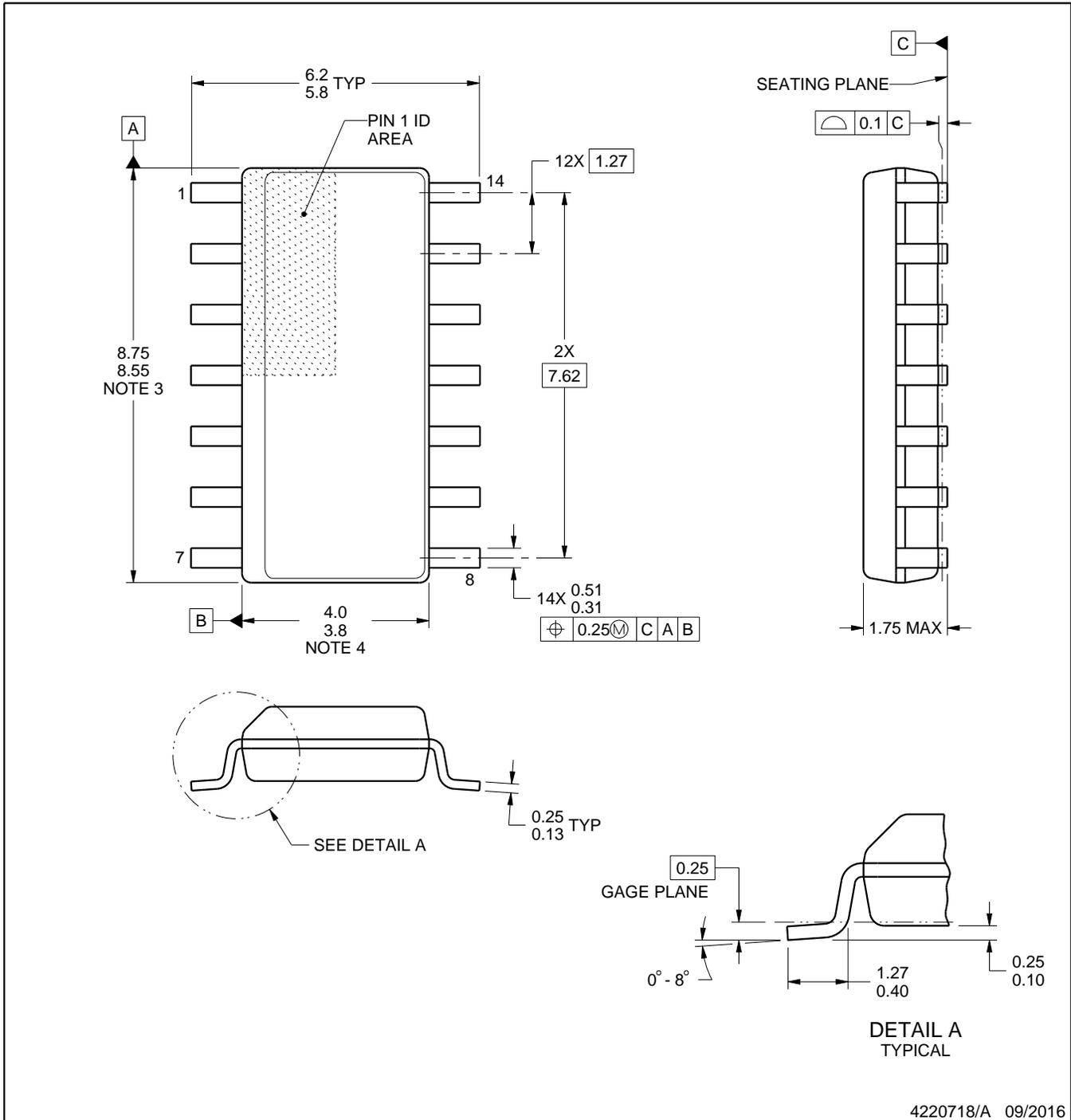
D0014A



# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

**NOTES:**

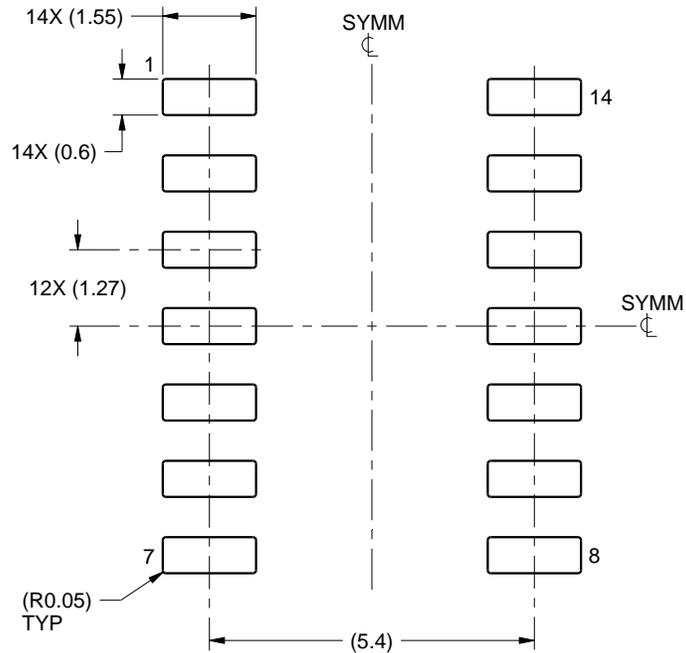
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

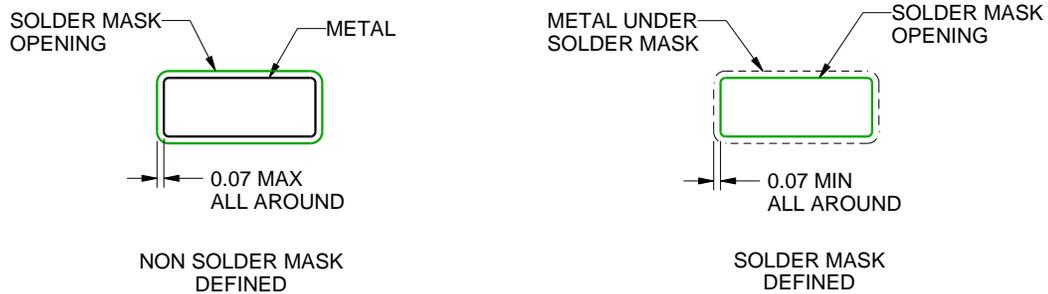
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

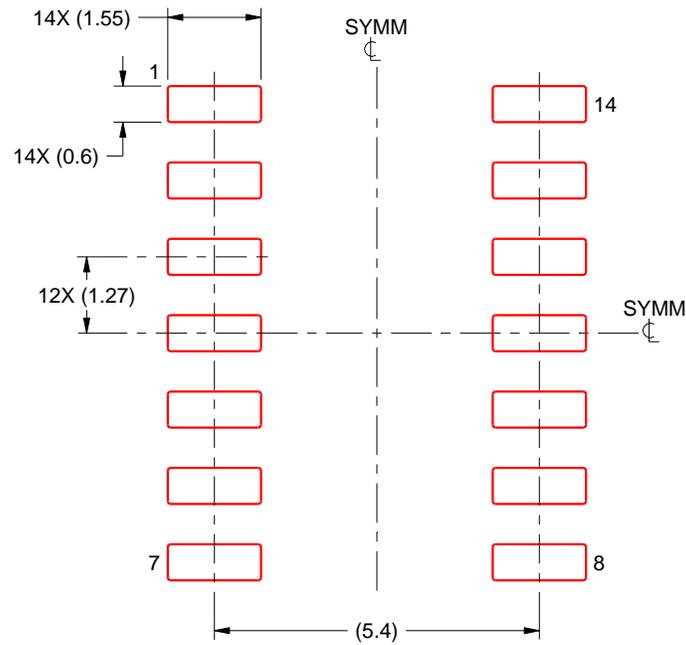
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

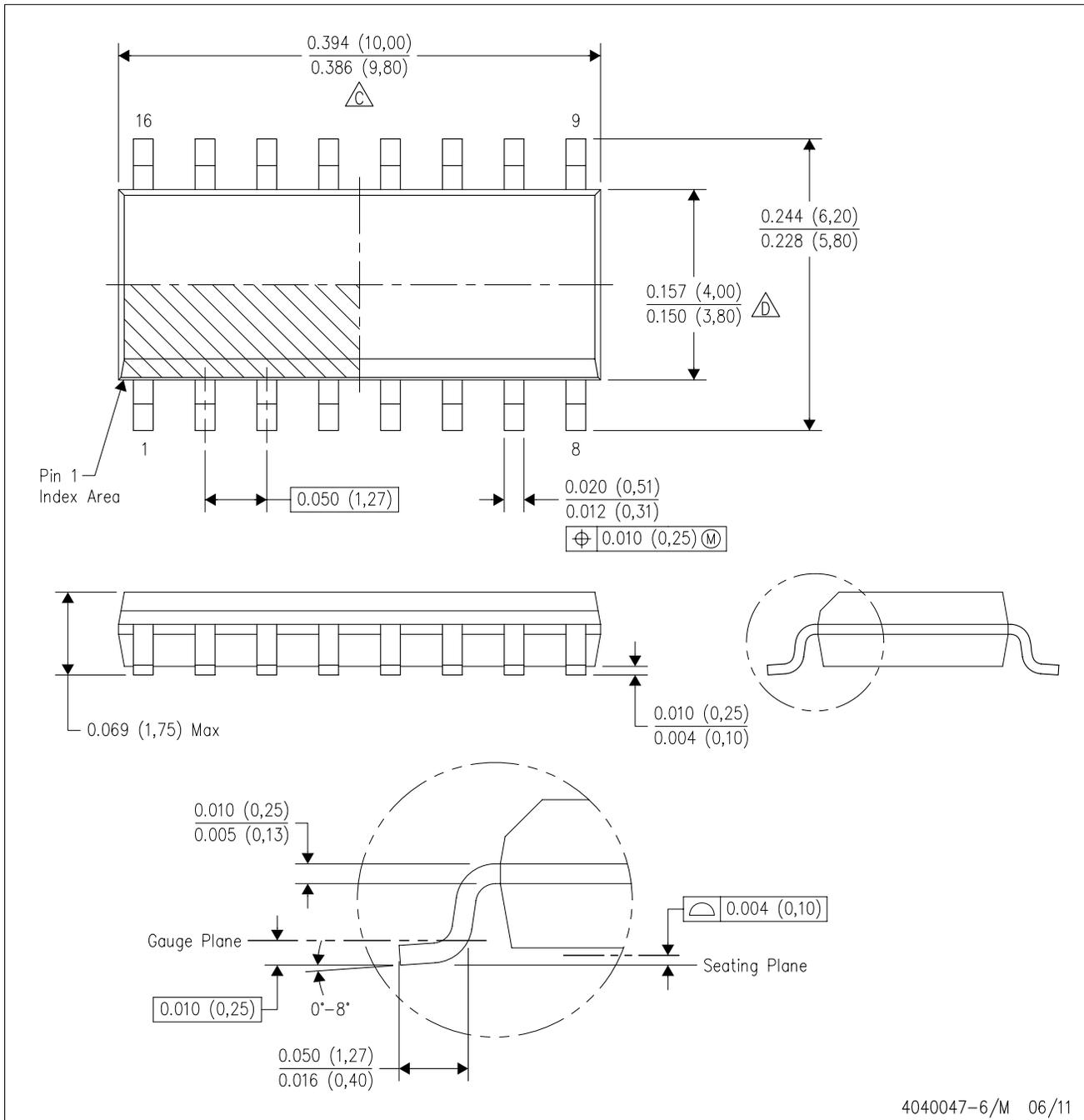
4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

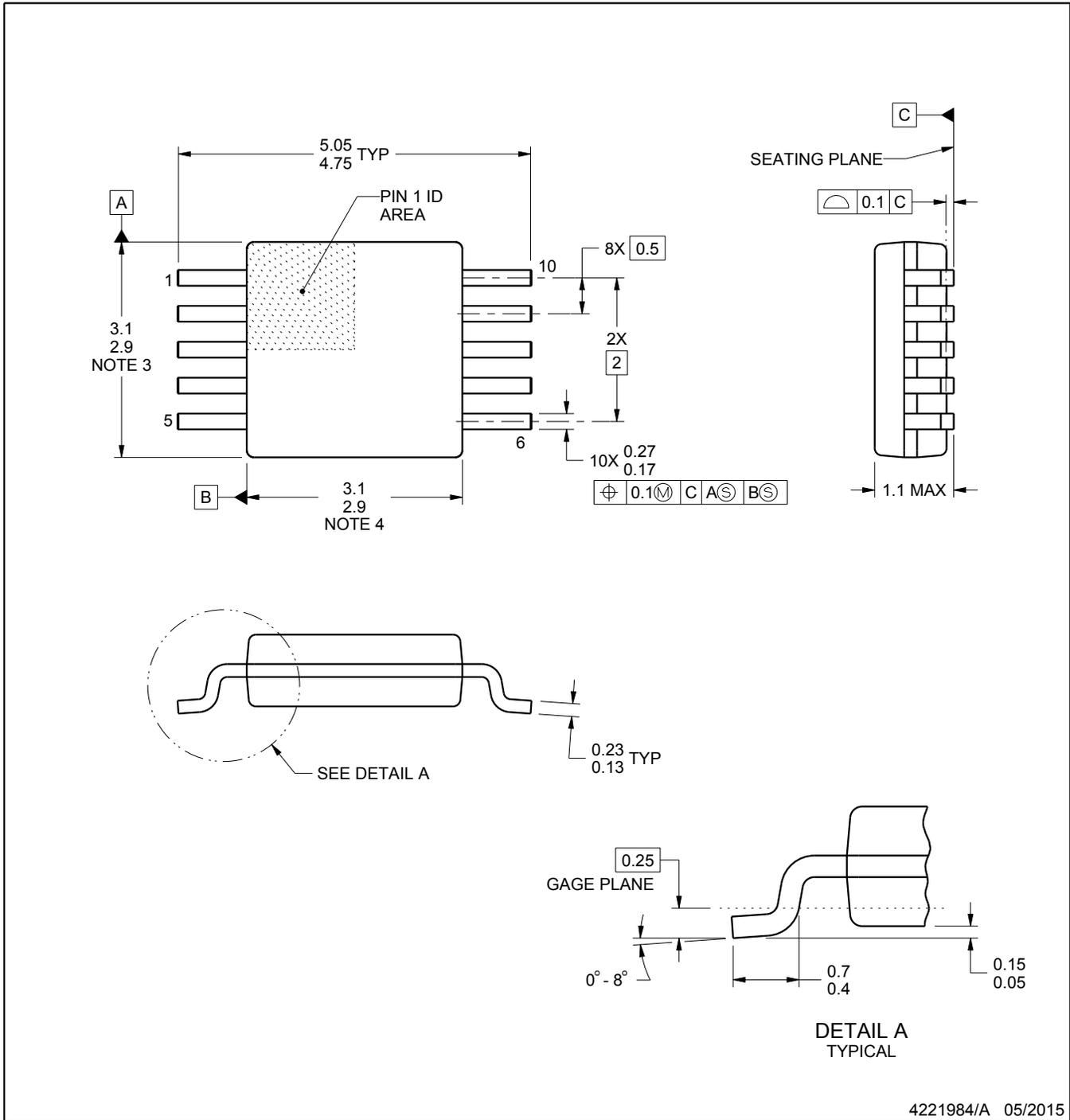
# DGS0010A



# PACKAGE OUTLINE

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4221984/A 05/2015

### NOTES:

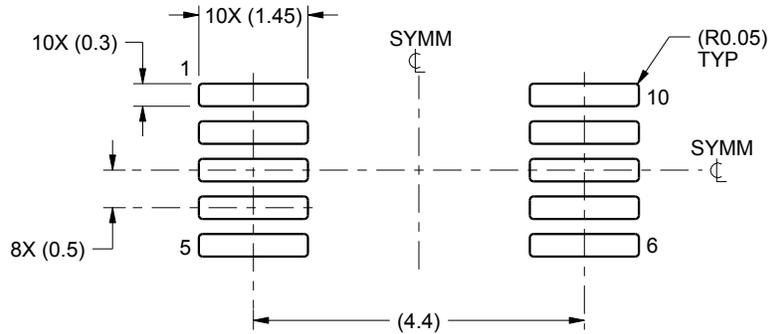
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

# EXAMPLE BOARD LAYOUT

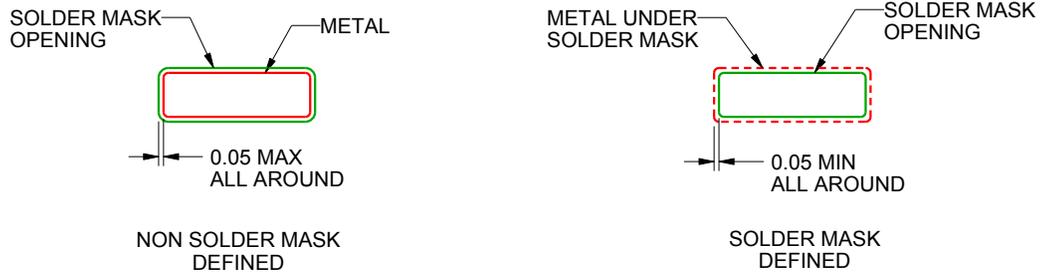
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

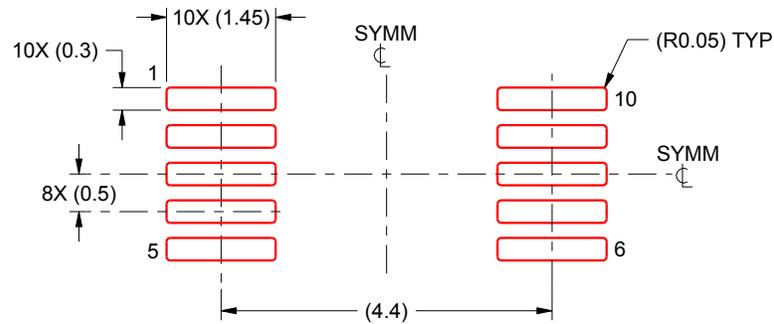
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

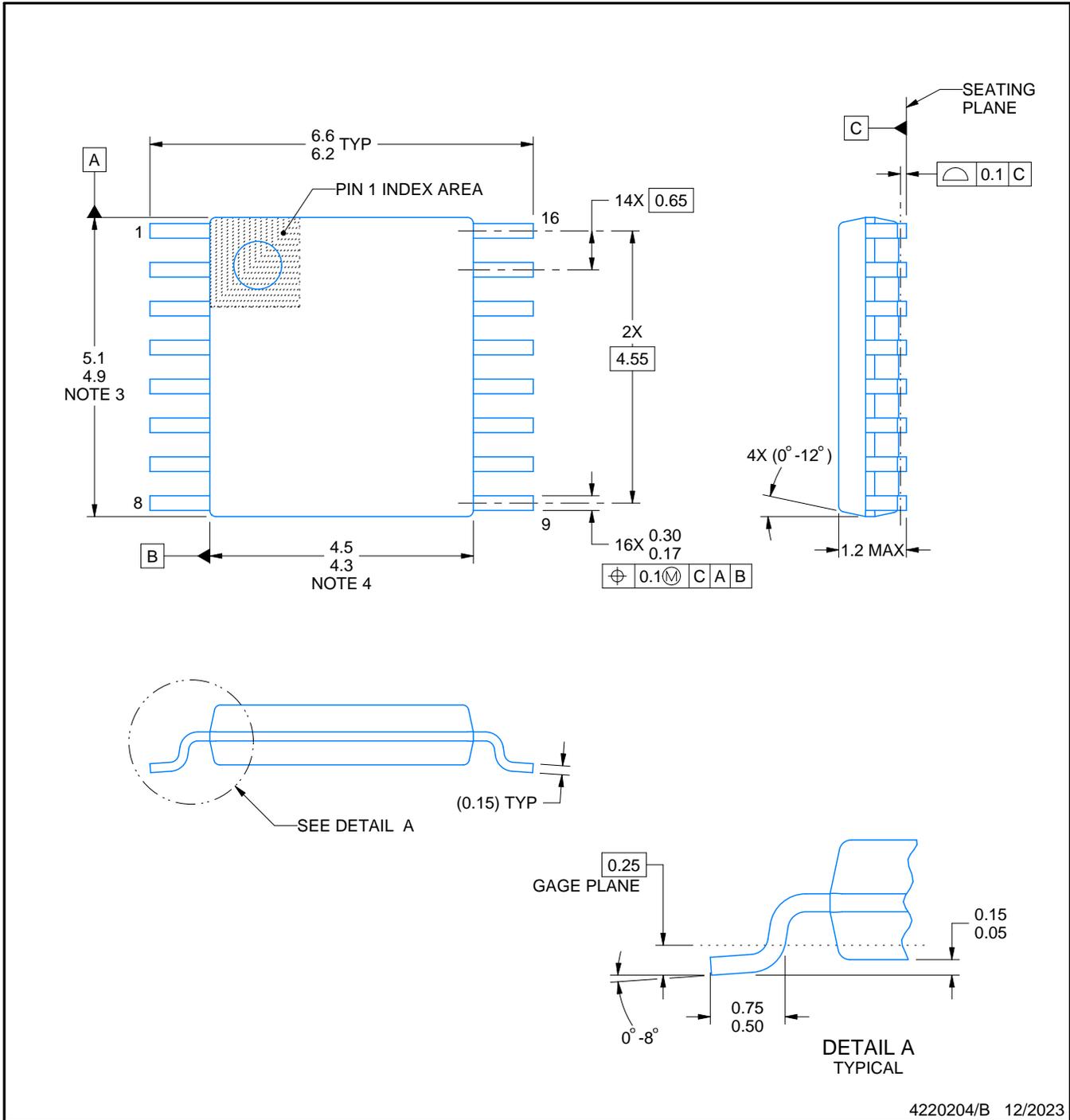


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220204/B 12/2023

NOTES:

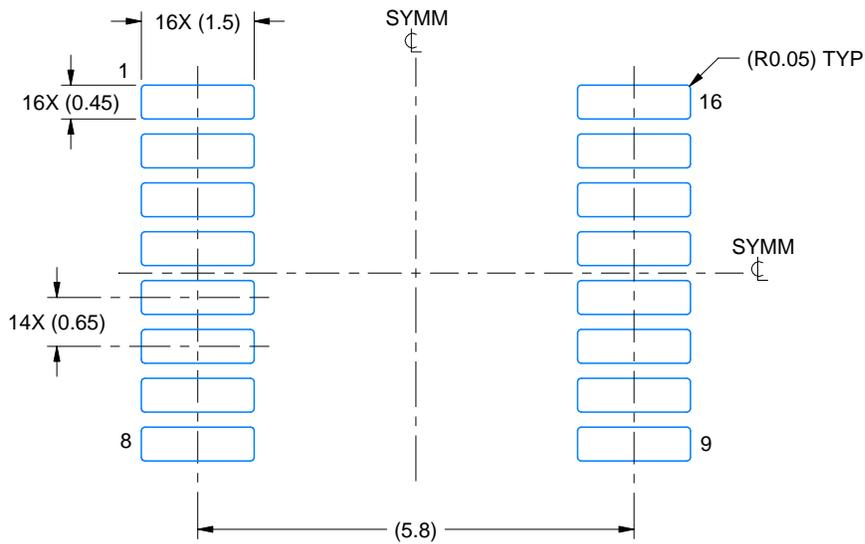
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

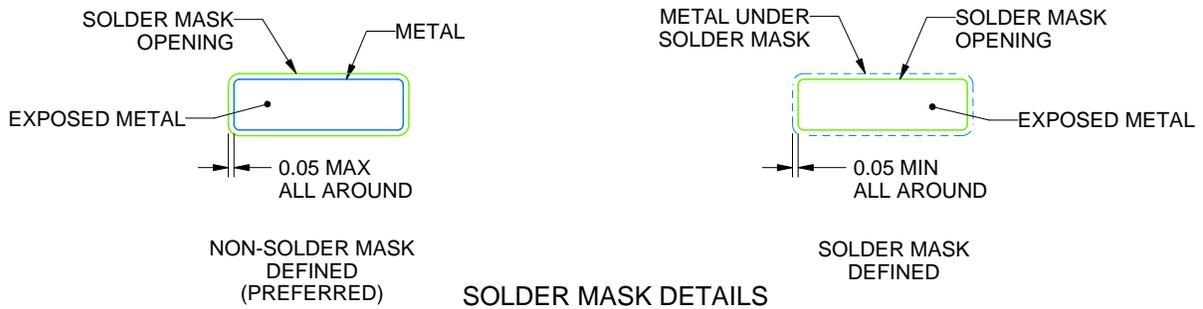
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

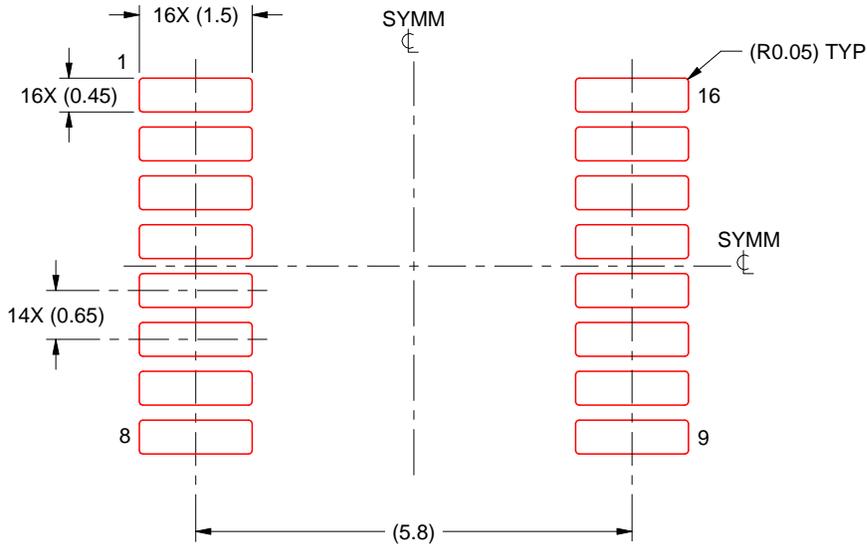
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

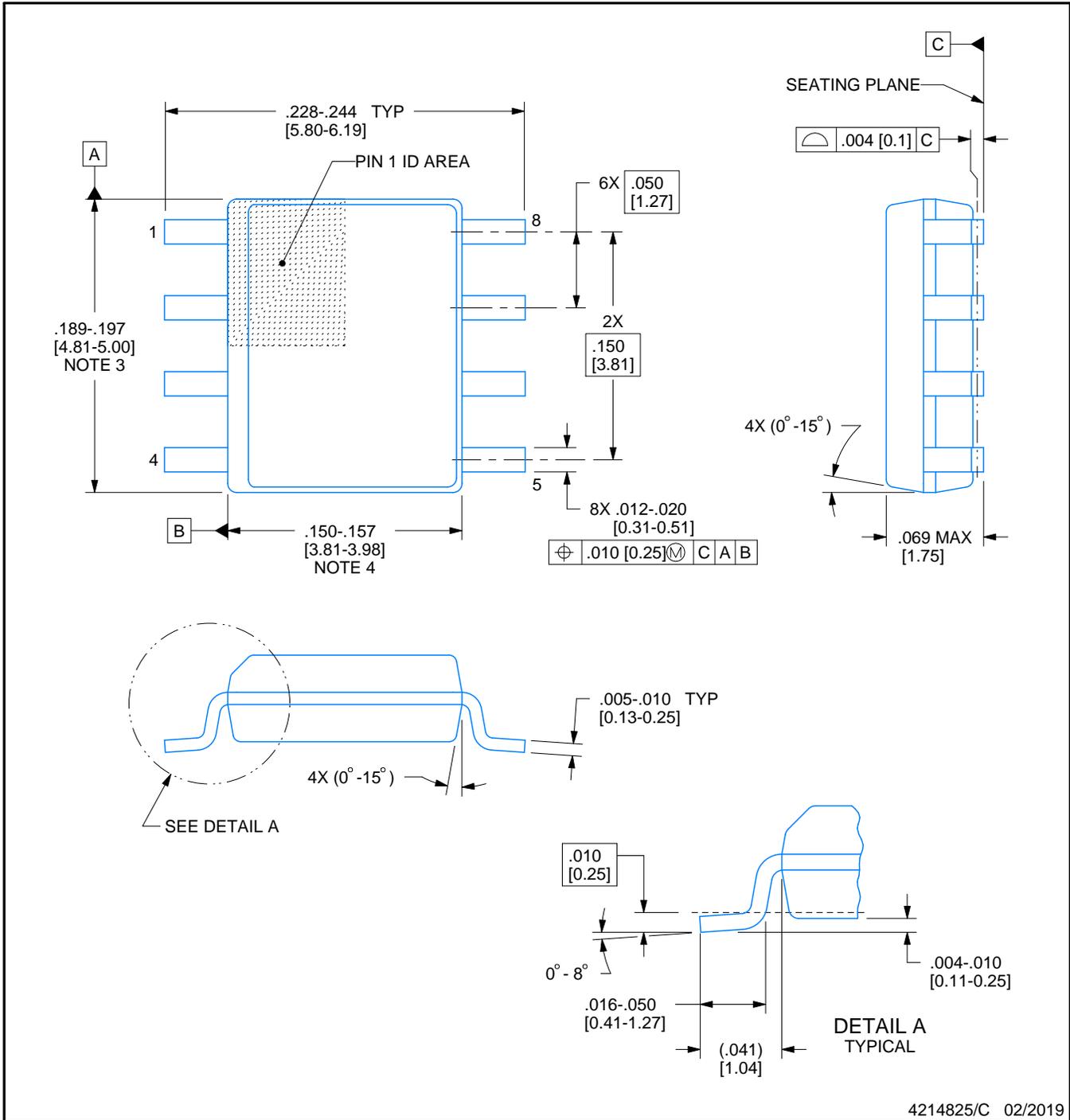


D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

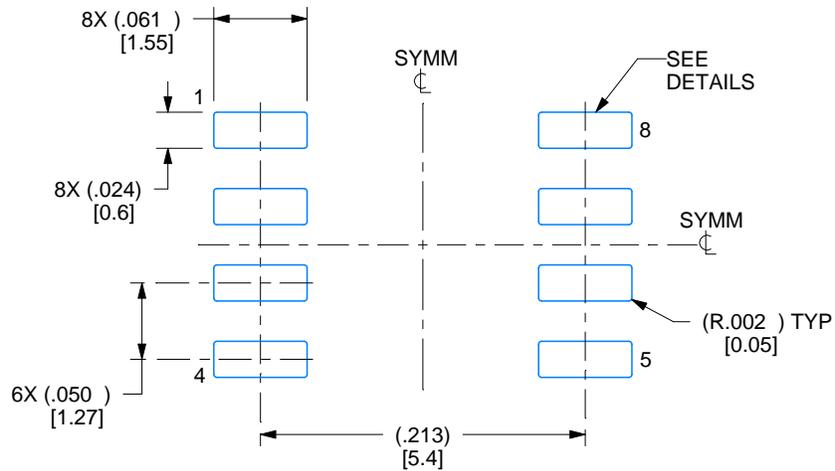
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

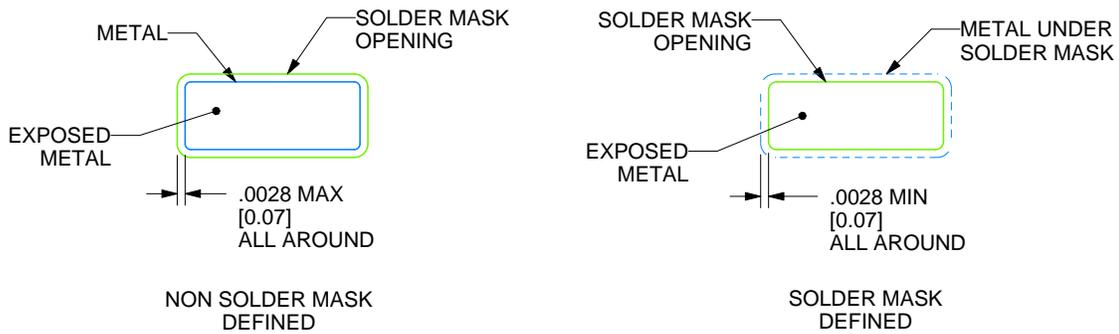
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

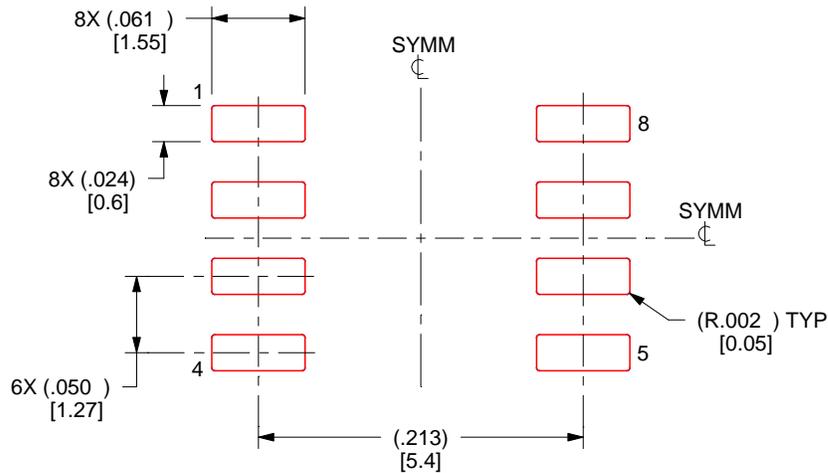
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

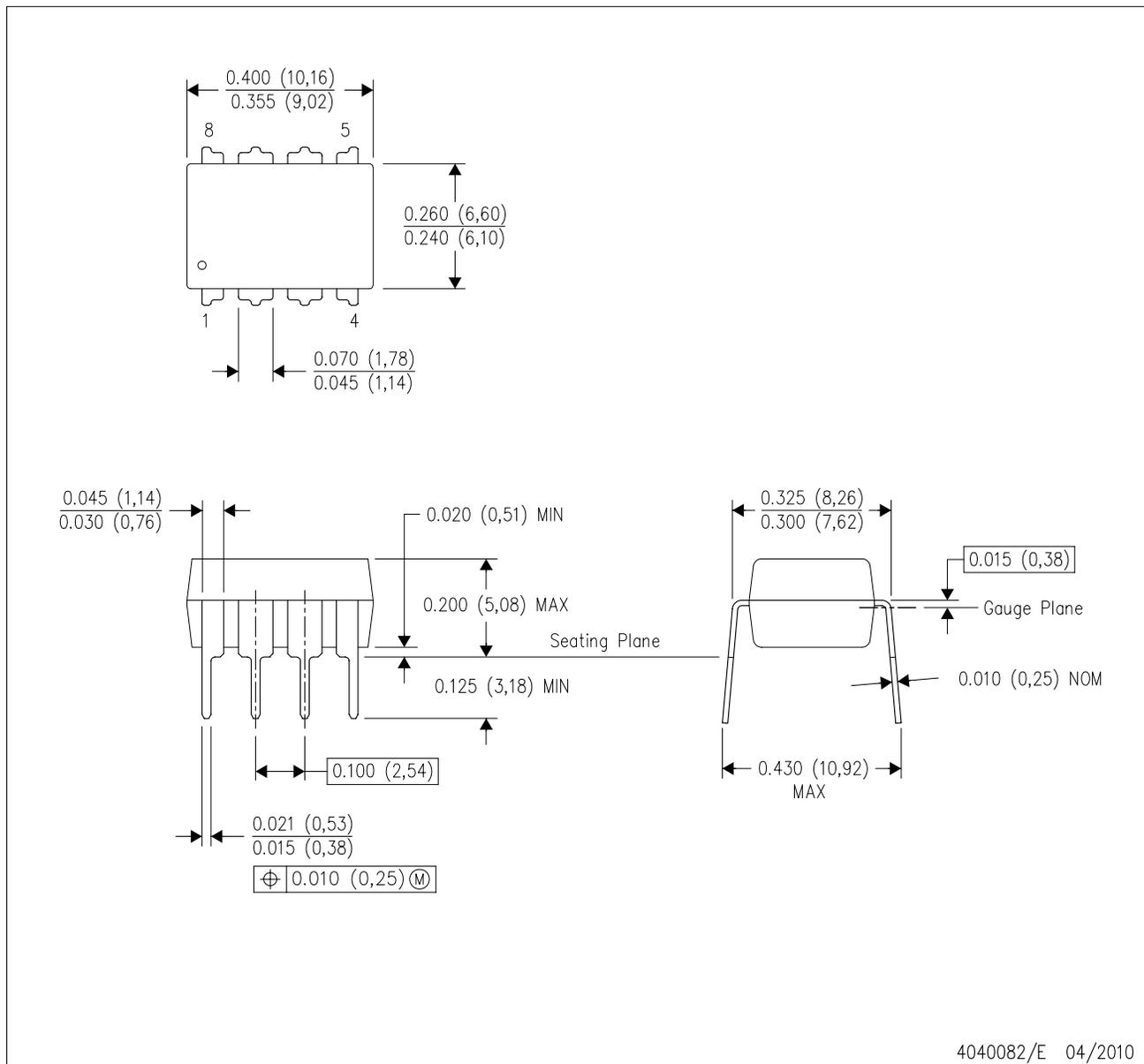
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

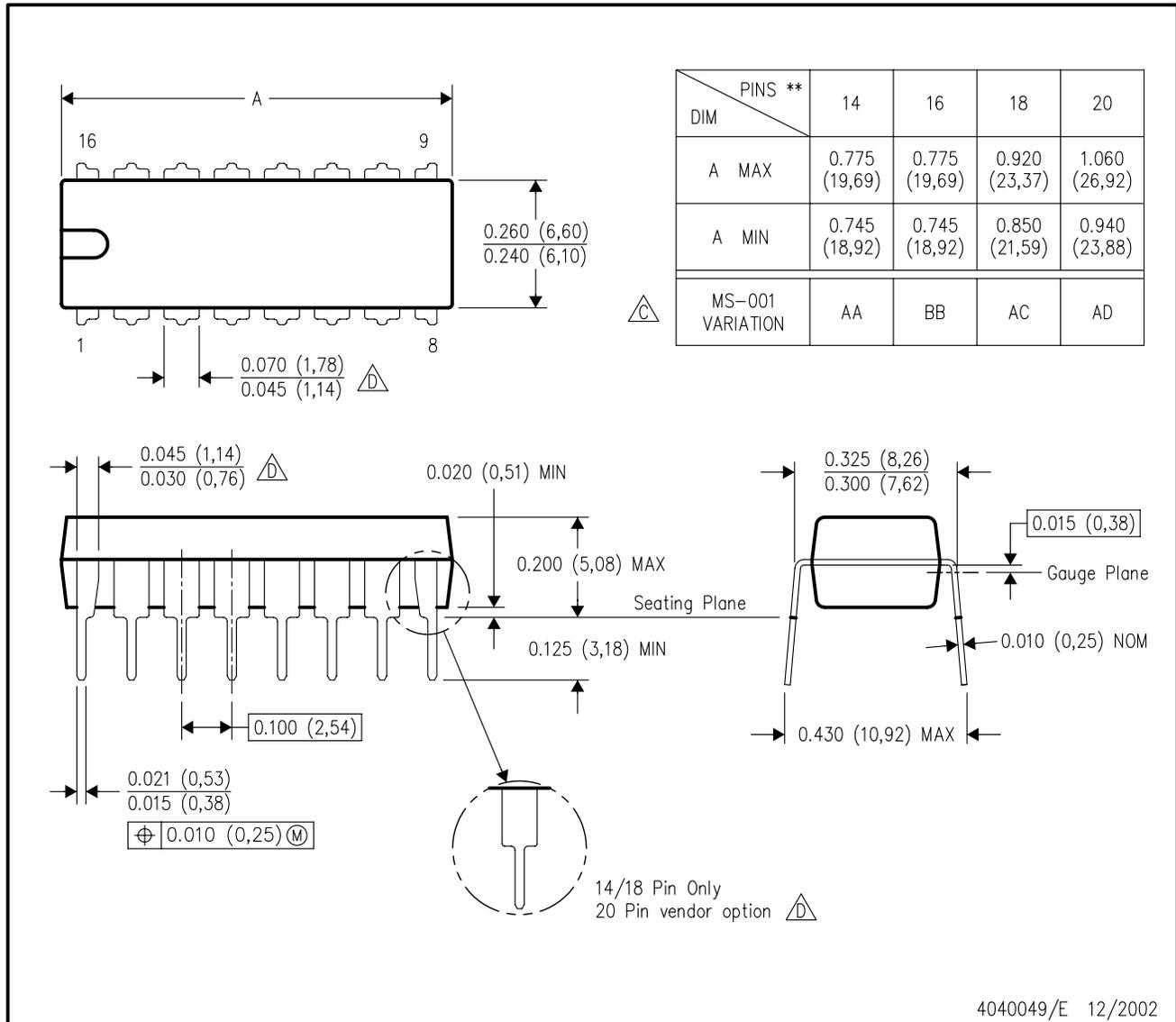


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

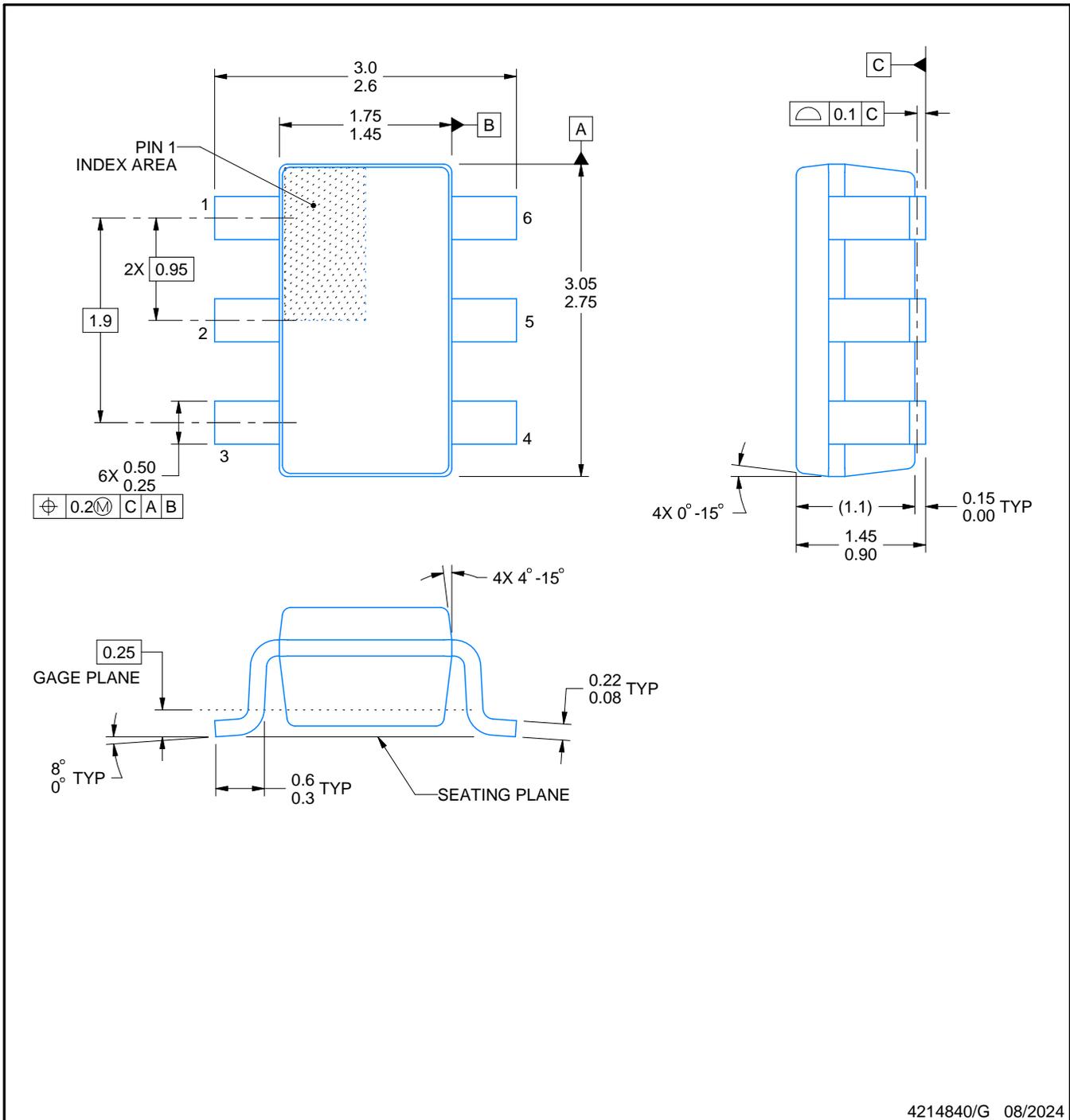


# DBV0006A

# PACKAGE OUTLINE

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

### NOTES:

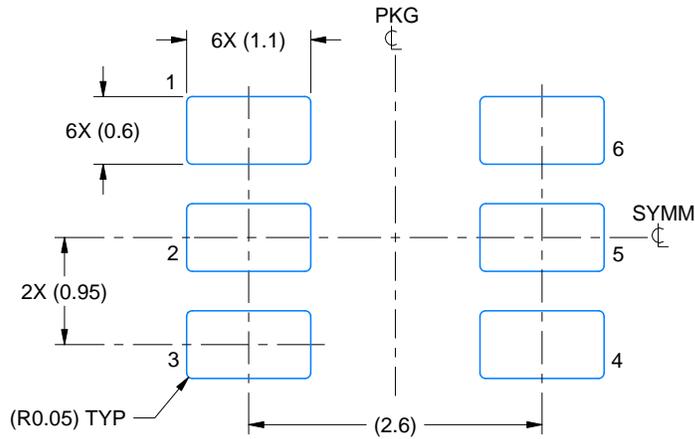
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

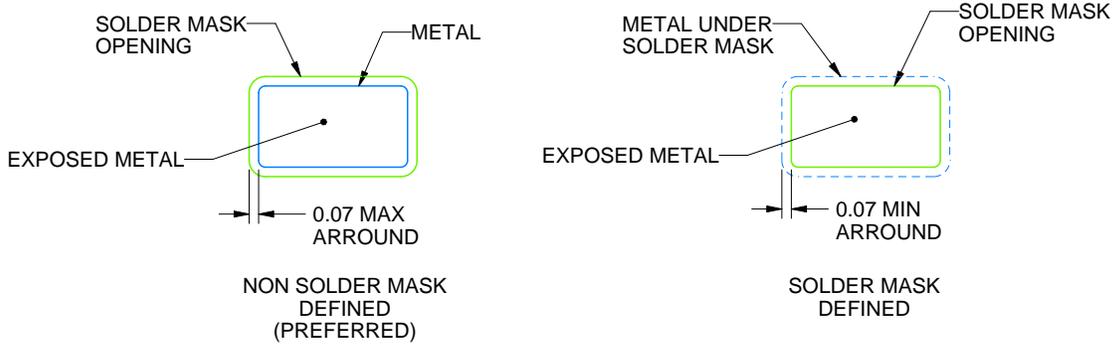
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

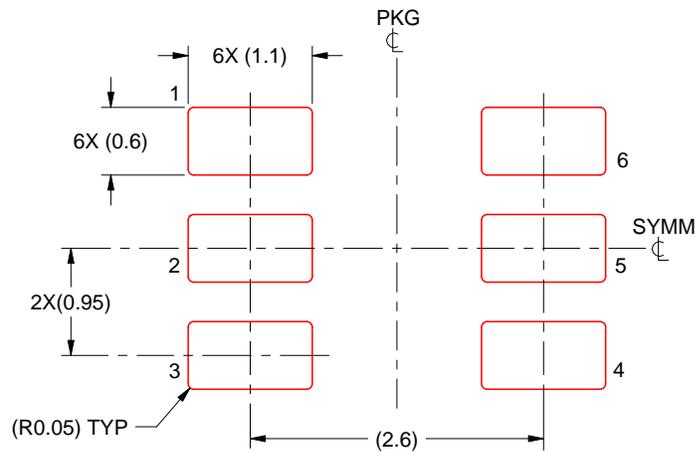
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

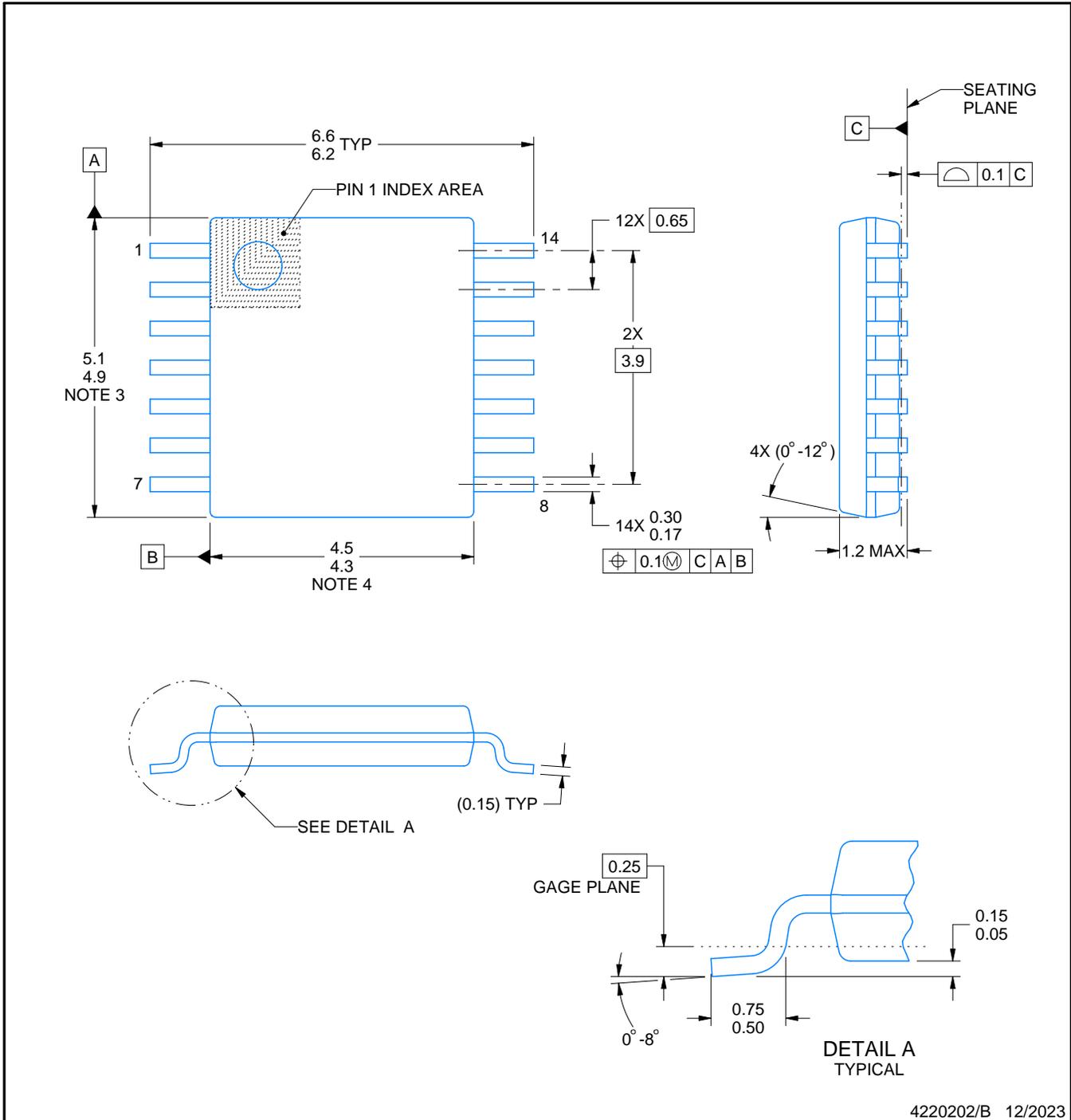
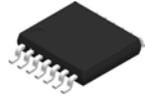


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220202/B 12/2023

NOTES:

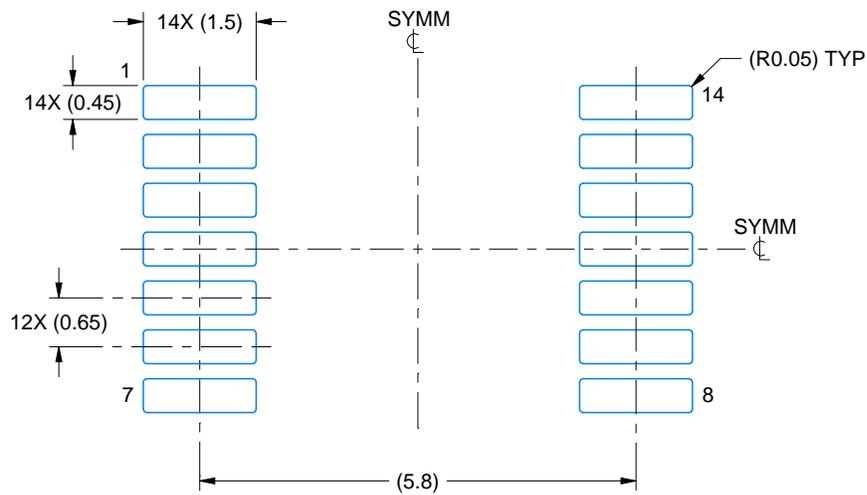
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

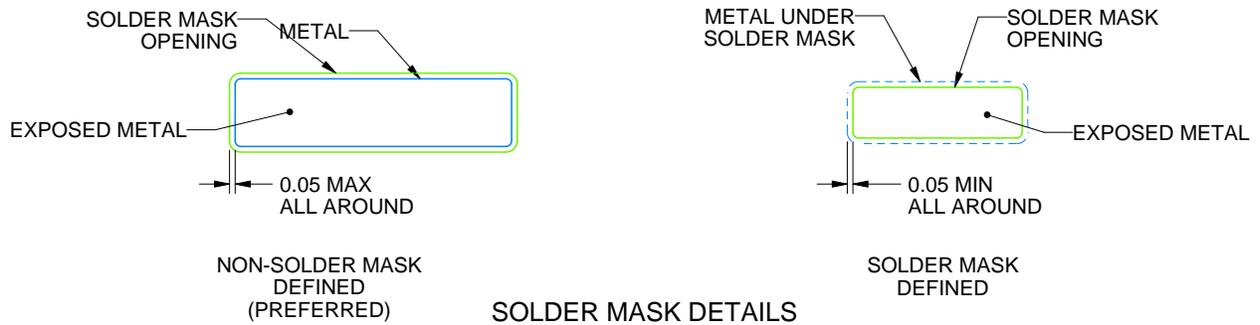
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

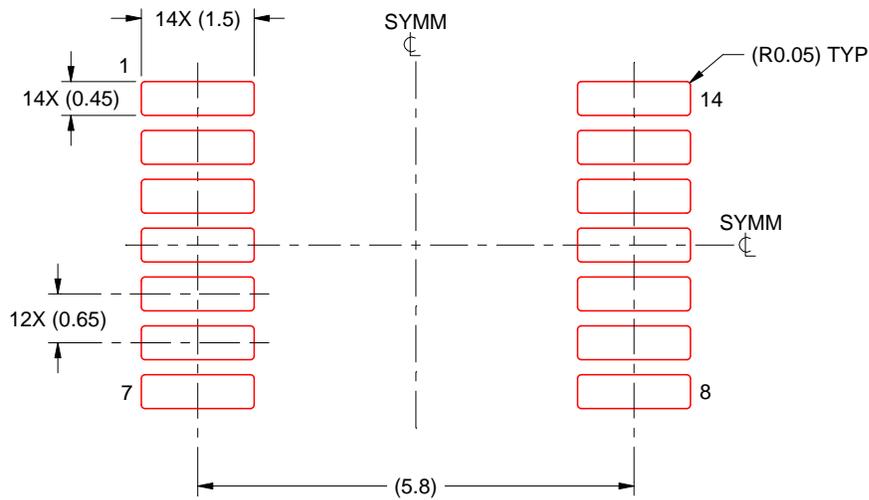
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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