TMF0020 20K bit FRAM with 64-bit unique ID, SDQ™ Single-Wire Serial Interface compatible with 1-Wire® Protocol

1 Features

- 20480 Bits of FRAM for storage of user-programmable configuration data partitioned into multiple pages
- Single-wire interface (1-wire® compatible) to reduce circuit board routing
- Communicates using single-wire protocol (compatible with 1-wire® protocol): 15.4Kbps (standard Speed) and 90Kbps (Overdrive Speed)
- Switch-point hysteresis and filtering embedded in the device to improve performance in the presence of noise
- IEC 61000-4-2 level 4 ESD protection (±8kV contact, ±15kV air, typical)
- Factory-programmed unique 64-bit identification number
- Operating temperature range: -10°C to 85°C
- Operating voltage range: 5V ±5% (Standard and Overdrive Speed), 3.3V ±5% (Standard Speed only)
- Available in TO-92 (LP) and VSON (DRP) packages

2 Applications

- Medical Cable Identification
- Asset trackers
- Connected peripherals & printers
- Counterfeit hardware prevention

3 Description

The TMF0020 is a 20K bit serial non-volatile memory (NVM) device containing a unique factory-programmed 48-bit identification number and an 8-bit family code. The memory is FRAM-based and has high endurance (10^6 R/W cycles) compared to other NVM technologies.

The device communicates over an SDQ™ single-wire interface compatible with 1-wire® protocol and supports both 15.4Kbps and 90Kbps speeds. The SDQ single-wire serial interface pin acts as both the communication pin and power pin for the device. The memory is organized as 80 memory pages with 256 bits per page. Data is first written to a 32-byte scratchpad. Then the data is verified before copying to FRAM memory.

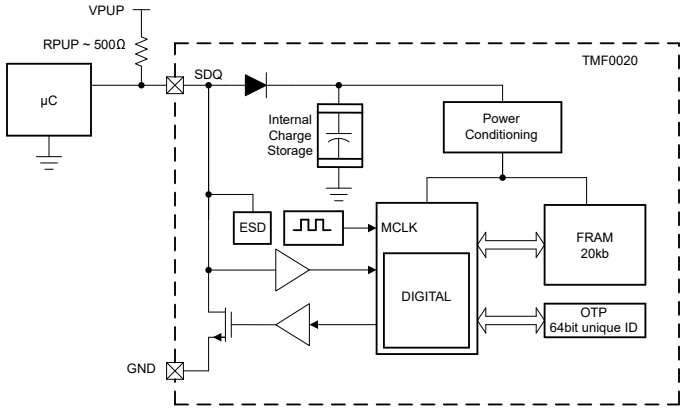
The device operates at two supply voltage ranges, 3.3V ±5% and 5V ±5%, and is specified from -10°C to 85°C. The operating range covers most applications and enables peak design for low-cost development.

1-Wire® is a registered trademark of Maxim Integrated Products, Inc.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)
TMF0020	VSON (DRP)	3mm × 3mm	3mm × 3mm
	TO-92 (LP)	5.2mm × 3.68mm	4.83mm × 4.83mm

(1) For more information, see Mechanical, Packaging, and Orderable Information. These package options are compatible with 1-Wire® devices.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Block Diagram

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4 Pin Configuration and Functions

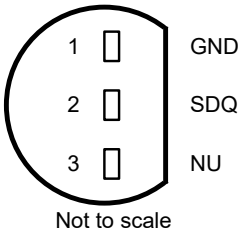

Figure 4-1. LP Package, 3-Pin TO-92 (Bottom View)

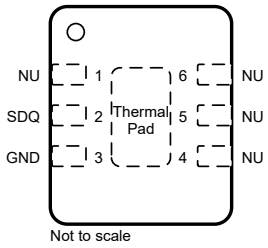

Figure 4-2. DRP Package, 6-Pin VSON (Top View)

Table 4-1. Pin Functions

PIN			Type [1]	DESCRIPTION
NAME	NO.			
	TO-92	VSON		
EP	—	EP	—	Exposed thermal pad. Connect to GND.
GND	1	3	GND	Ground
NU	3	1, 4, 5, 6	—	Non-usable terminal. Do not connect.
SDQ single-wire serial interface	2	2	I/O	Data. Open drain, requires external pullup resistor.

(1) GND = ground, I/O = bidirectional

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{PUP}	DC voltage applied to data	–0.3	5.5	V
I_{OL}	Low-level output current		30	mA
T_{STG}	Storage temperature	–40	125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute maximum ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±250	
		ESD IEC 61000-4-2 Air discharge, SDQ single-wire serial interface and GND	±15000	V

(1) JEDEC document JEP155 states that 500VHBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250VCDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{PUP}	Operational pull-up voltage	3.13		5.25	V
R_{PUP}	Serial communication interface pull-up resistance		500		Ω
T_A	Operating free-air temperature	-10		85	°C

5.4 Thermal Information

THERMAL METRIC(1)		DRP (VSON) 6 PINS	TO-92 (LP) 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.1	129.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.3	93.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.8	99.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	23.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.7	99.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.9	-	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

Minimum and Maximum specifications apply from T_A of -10°C to 85°C. Typical specifications are at 25°C and V_{PUP} = 3.3V and 5V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I/O PIN: GENERAL DATA						
V_{PUP}	Pull-up Voltage	±5% variation (3.3V - Standard speed only)	3.13	3.3	3.46	V
			4.75	5	5.25	V
R_{PUP}	Pull-up Resistance	(1) (2) (3)		500		Ω
C_{CABLE}	Cable Capacitance	(4) (5)			1.7	nF
C_{IO}	Input Capacitance	(6) (4)		2000		pF
I_L	Input Load Current	(7)		7	14	µA
V_{IL}	Input Low Voltage	(8)			0.5	V
V_{OL}	Output Low Voltage	Measured with R_{PUP} = 500Ω, V_{PUP} = 3.3V		0.4	0.5	V
		Measured with R_{PUP} = 500Ω, V_{PUP} = 5V		0.4	0.5	V
V_{TL}	High-to-Low Switching threshold (4) (3) (9)	V_{PUP} = 3.3V	0.84		1.72	V
		V_{PUP} = 5V	2		3	V
V_{TH}	Low-to-High Switching Threshold (4) (3) (10)	V_{PUP} = 3.3V	1.64		2.75	V
		V_{PUP} = 5V	3.2		4.3	V
V_{HY}	Switching Hysteresis (4) (3) (11)	V_{PUP} = 3.3V	0.44		1.1	V
		V_{PUP} = 5V	0.9		1.3	V

(1) Maximum allowable pull-up resistance is dependent on the number of devices connected and the recovery time. The specified value is assuming six devices are connected in the system and minimum recovery time.
(2) Resistance tolerance to be within 1% or less.
(3) V_{TL}, V_{TH}, and V_{HY} are a function of the internal supply voltage, which is a function of V_{PUP}, R_{PUP}, single-wire timing, and capacitive loading on SDQ single-wire serial interface pin. Lower VPUP, higher R_{PUP}, shorter t_{REC}, and heavier capacitive loading all lead to lower values of V_{TL}, V_{TH}, and V_{HY}.
(4) Specified by design, characterization or simulation only. Not production tested.
(5) System requirement.
(6) Maximum Capacitance value represents the internal parasitic capacitance when V_{PUP} is first applied. Once the parasitic charge storage capacitance is charged, normal logic transitions are not affected.
(7) Applicable when SDQ single-wire serial interface is HIGH (at V_{PUP}) and the device is in idle mode (no digital activity or memory access). The numbers indicates the stand-by current consumption.
(8) The voltage on SDQ single-wire serial interface needs to be less or equal to V_{ILMAX} at all times the host is driving SDQ single-wire serial interface to a logic 0 level.
(9) Voltage below which, during a falling edge on SDQ single-wire serial interface, logic 0 is detected.
(10) Voltage above which, during a rising edge on SDQ single-wire serial interface, logic 1 is detected.
(11) After V_{TH} is crossed during a rising edge on SDQ single-wire serial interface pin, the voltage on SDQ single-wire serial interface must drop by at least V_{HY} to be detected as logic 0.

5.6 Timing Requirements

Minimum and Maximum specifications apply from T_A of −10°C to 85°C. Typical specifications are at 25°C and V_{PUP} = 3.3V and 5V (unless otherwise noted).

			MIN	NOM	MAX	UNIT
I/O PIN: GENERAL DATA						
$t_{STARTUP}$	Start-up time	Minimum time SDQ single-wire serial interface must be HIGH before device responds with a presence pulse		10		ms
t_{REC}	Recovery Time	Standard speed(1) (2)	5			µs
		Overdrive speed(1) (2)	5			µs
t_{REH}	Rising-Edge Hold-Off Time	Standard speed(1) (2)	0.5		5	µs
t_{SLOT}	Time Slot Duration	Standard speed(3)	65			µs
		Overdrive speed(3)	11			µs
I/O PIN: SINGLE-WIRE RESET, PRESENCE-DETECT CYCLE						
t_{RSTL}	Reset Low Time	Standard speed	480		550	µs
		Overdrive speed	48		80	µs
t_{PDH}	Presence-Detect High Pulse	Standard speed	15		60	µs
		Overdrive speed	2		6	µs
t_{PDL}	Presence-Detect Low Time	Standard speed	60		240	µs
		Overdrive speed	8		24	µs
t_{PDS}	Presence-Detect Sample Time (4),(5)	Standard speed	60	70	75	µs
		Overdrive speed	6	8.7	10	µs
IO PIN: SINGLE-WIRE WRITE						
t_{W0L}	Write-Zero Low Time	Standard speed(6)	60		120	µs
		Overdrive speed(6)	6		15.5	µs
t_{W1L}	Write-One Low Time	Standard speed(6)	1		15	µs
		Overdrive speed(6)	1		2	µs
IO PIN: SINGLE-WIRE READ						
t_{RL}	Read Low Time	Standard speed(2) (7)	5		15 - t_{RC}	µs
		Overdrive speed(2) (7)	1		2 - t_{RC}	µs
t_{RDS}	Read Sample Time (8)	Standard speed(2) (7)	t_{RL} + t_{RC}		15	µs
		Overdrive speed(2) (7)	t_{RL} + t_{RC}		3	µs
FRAM						
NCY	Write/Erase Cycles (Endurance)(2)				1M	Cycles
t_{PROG}	Programming Time(2)	For all 20Kb of memory			1	ms
t_{DR}	Data Retention(9)	At 80°C		10		Years
		At 85°C		7		

(1) Make sure the voltage on SDQ single-wire serial interface is less or equal to V_{ILMAX} at all times when the host is driving SDQ single-wire serial interface to a logic 0 level.
(2) Specified by design, characterization or simulation only. Not production tested.
(3) Defines maximum possible bit rate.
(4) Interval after t_{RSTL} during which a bus host can read logic 0 on SDQ single-wire serial interface if a TMF0020 is present. The presence detect pulse can be outside this interval, but is complete within 2ms after power-up. This behavior addresses the scenario where the one-wire device has been powered off (bus low) for a long time. Bus power is then applied. The device is allowed to malfunction, and generate a presence pulse that violates the presence timing specification. However, the abnormal condition is resolved typically within 10ms.
(5) System requirement.
(6) t_ε in Figure 6-18 and Figure 6-19 represents the time required for the pullup circuitry to raise the voltage on the SDQ single-wire serial interface pin from V_{IL} to V_{TH}. Hence the actual maximum duration for the host to pull the line low is t_{W1LMAX} + t_F – t_ε and t_{W0LMAX} + t_F – t_ε, respectively.
(7) t_{RC} in Figure 6-20 represents the time required for the pullup circuitry to raise the voltage on the SDQ single-wire serial interface pin from V_{IL} to the input-high threshold of the host device. Hence, the actual maximum duration for the host to pull the line low is t_{RLMAX} + t_F.

(8) Refers to the minimum time after which the recognition of negative edge is possible after V_{TH} has been reached on the preceding rising edge.
(9) Data retention time is degraded as T_A increases. Long-term storage at elevated temperatures is not recommended.

5.7 Functional Tests

Over operating free-air temperature range and V_{PUP} = 3.3V and 5V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Multi- target bus	Any TMF0020 must be able to communicate in a network where there are multiple target devices. An example configuration of 3 target devices (including the DUT) is shown in Figure 6-6.(1)		0		Multi-target bus Fails

(1) See Test Procedures for Functional Tests.

5.8 Typical Characteristics

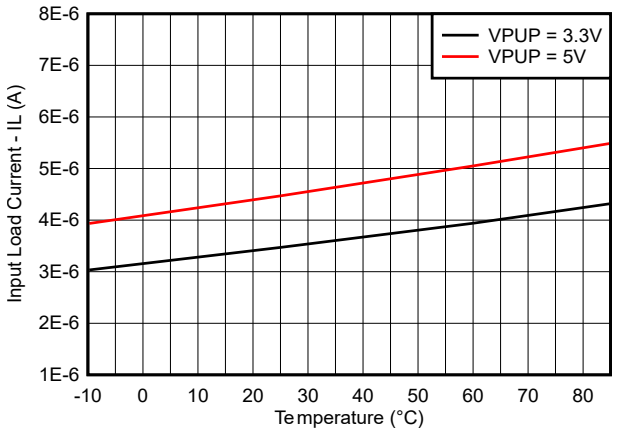

Figure 5-1. Input Load Current (I_L) vs Temperature (Standard Speed)

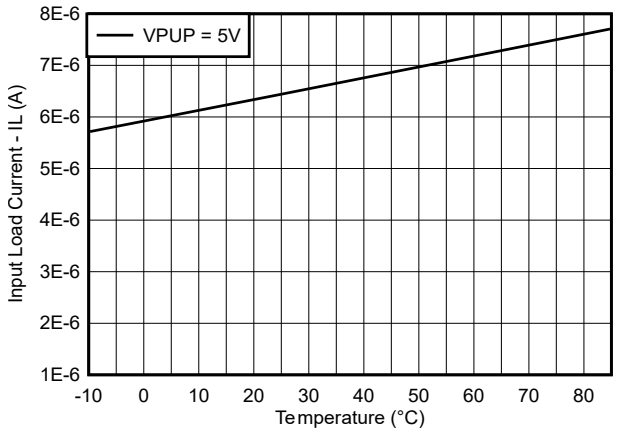

Figure 5-2. Input Load Current (I_L) vs Temperature (Overdrive Speed)

6 Detailed Description

6.1 Overview

The Functional Block Diagram section presents the on-chip block level components of the TMF0020 device. The device has the following data components: a 20480-bit FRAM data memory, and a 64-bit factor-programmed ROM, which contains an 8-bit family code, a 48-bit identification number, and an 8-bit CRC value. Power for read and write operations is derived from the SDQ single-wire serial interface pin. An internal capacitor stores energy while the signal line is high and releases energy during the low times of the SDQ single-wire serial interface pin until the pin returns high to replenish the charge on the capacitor.

6.2 Functional Block Diagram

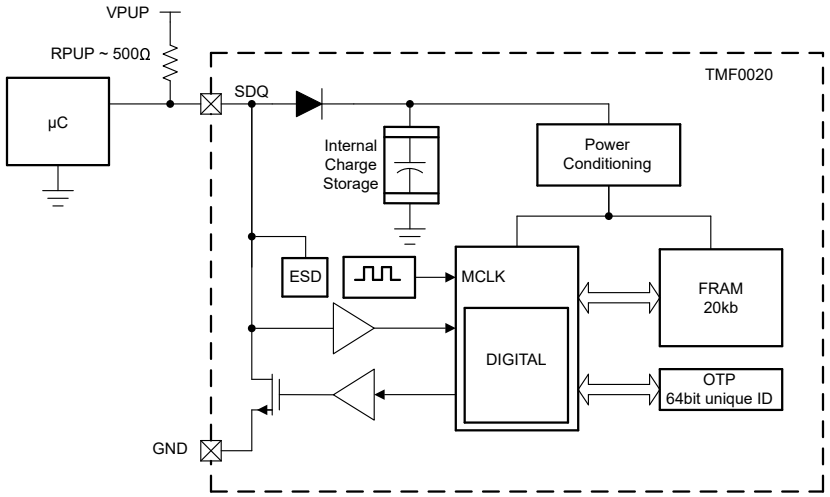

Figure 6-1. Functional Block Diagram

6.3 Feature Description

6.3.1 20480-Bit FRAM

Table 6-1 is a memory map of the 20480-bit FRAM section of the TMF0020 device, configured as 80 pages with 32-bytes each. Eight adjacent pages form one 256-byte block. The FRAM memory is programmed using the 32-byte volatile scratchpad buffer. The process for writing to the FRAM memory includes two steps. Data is first written to the scratchpad buffer. The data is then verified by reading the scratchpad buffer which confirms proper receipt of the data. If the buffer content is correct, a copy scratchpad command is issued to copy the scratchpad buffer to the FRAM memory. This process verifies data integrity when programming the memory. The details for programming and reading the 20480-bit FRAM portion of the TMF0020 are in the Memory Function Commands section of this data sheet.

Table 6-1. FRAM Data Memory Map

ADDRESS RANGE	TYPE (1)	DESCRIPTION	PROTECTION CODES (NOTES)
0000h to 00FFh	R/(W)	Data Memory Pages 0 to 7 (Block 0)	(Protection controlled by address 1FA0h)
0100h to 01FFh	R/(W)	Data Memory Pages 8 to 15 (Block 1)	(Protection controlled by address 1FA1h)
0200h to 02FFh	R/(W)	Data Memory Pages 16 to 23 (Block 2)	(Protection controlled by address 1FA2h)
0300h to 03FFh	R/(W)	Data Memory Pages 24 to 31 (Block 3)	(Protection controlled by address 1FA3h)
0400h to 04FFh	R/(W)	Data Memory Pages 32 to 39 (Block 4)	(Protection controlled by address 1FA4h)
0500h to 05FFh	R/(W)	Data Memory Pages 40 to 47 (Block 5)	(Protection controlled by address 1FA5h)
0600h to 06FFh	R/(W)	Data Memory Pages 48 to 55 (Block 6)	(Protection controlled by address 1FA6h)
0700h to 07FFh	R/(W)	Data Memory Pages 56 to 63 (Block 7)	(Protection controlled by address 1FA7h)
0800h to 08FFh	R/(W)	Data Memory Pages 64 to 71 (Block 8)	(Protection controlled by address 1FA8h)

Table 6-1. FRAM Data Memory Map (continued)

ADDRESS RANGE	TYPE (1)	DESCRIPTION	PROTECTION CODES (NOTES)
0900h to 09FFh	R/(W)	Data Memory Pages 72 to 79 (Block 9)	(Protection controlled by address 1FA9h)

(1) R = Read, W = Write

In FRAM devices, digital information is stored as polarization in a dielectric. This polarization can be lost at a temperature-dependent rate. Increasing temperatures increase the de-polarization rate. Data Retention metrics are listed in the Section 5.6 table.

6.3.2 FRAM Status Memory

As shown in Table 6-1, the data memory of the TMF0020 consists of 10 contiguous blocks of FRAM memory. Blocks 0 to 9 are 256 bytes each, and each block is formed by eight adjacent memory pages.

In addition to the data memory, the TMF0020 consists of the status memory starting at address 1FA0h as shown in Table 6-2. The register page in the status memory consists of 10 protection control bytes and one byte each to lock the memory block and the register page.

Both the 10 protection control bytes and the memory block lock byte control the access to the 10 data memory blocks. By default, the memory blocks are set to open access. A protection byte value of 55h sets the corresponding memory block to write protection mode, whereas a protection byte value of AAh sets the corresponding memory block to EPROM mode.

If the memory block lock byte is programmed to either 55h or AAh, copy protection is set for all write-protected data memory blocks (memory blocks in EPROM mode are not affected). Similarly, if the register page lock byte is programmed to either 55h or AAh, copy protection is set for the entire register page.

Setting a memory location into write protection mode allows the copy-scratch pad operation, but prevents data from being changed. This allows memory to be reprogrammed with the same data, refreshing the polarization for data retention longevity.

As compared to write protection, copy protection blocks the copy-scratchpad function. Only use the copy-protect feature after setting all write-protected blocks and associated protection control bytes to the final values. Note that copy protection does not prevent copying data across devices. When set to 55h or AAh, the protection control registers and the lock bytes self-write-protect. Any other setting allows unrestricted write access.

Addresses 1FC3h and 1FC4h are available for programming an optional manufacturer ID. These values are read by the host, for example, to associate an end-user product with a TMF0020. At address 1FC2h, the TMF0020 stores a byte for locking the manufacturer ID, with a default value of 00h. After writing AAh or 55h to this location, the manufacturer ID and lock byte are permanently write protected.

Table 6-2. FRAM Status Memory Map

ADDRESS RANGE	TYPE (1)	DESCRIPTION	PROTECTION CODES (NOTES)
1FA0h	R/W	Protection Control Byte (Block 0)	55h: Write Protect Block 0
			AAh: EPROM Mode Block 0
			55h or AAh: Write Protect 1FA0h
1FA1h	R/W	Protection Control Byte (Block 1)	55h: Write Protect Block 1
			AAh: EPROM Mode Block 1
			55h or AAh: Write Protect 1FA1h
1FA2h	R/W	Protection Control Byte (Block 2)	55h: Write Protect Block 2
			AAh: EPROM Mode Block 2
			55h or AAh: Write Protect 1FA2h
1FA3h	R/W	Protection Control Byte (Block 3)	55h: Write Protect Block 3
			AAh: EPROM Mode Block 3
			55h or AAh: Write Protect 1FA3h

Table 6-2. FRAM Status Memory Map (continued)

ADDRESS RANGE	TYPE (1)	DESCRIPTION	PROTECTION CODES (NOTES)
1FA4h	R/W	Protection Control Byte (Block 4)	55h: Write Protect Block 4
			AAh: EPROM Mode Block 4
			55h or AAh: Write Protect 1FA4h
1FA5h	R/W	Protection Control Byte (Block 5)	55h: Write Protect Block 5
			AAh: EPROM Mode Block 5
			55h or AAh: Write Protect 1FA5h
1FA6h	R/W	Protection Control Byte (Block 6)	55h: Write Protect Block 6
			AAh: EPROM Mode Block 6
			55h or AAh: Write Protect 1FA6h
1FA7h	R/W	Protection Control Byte (Block 7)	55h: Write Protect Block 7
			AAh: EPROM Mode Block 7
			55h or AAh: Write Protect 1FA7h
1FA8h	R/W	Protection Control Byte (Block 8)	55h: Write Protect Block 8
			AAh: EPROM Mode Block 8
			55h or AAh: Write Protect 1FA8h
1FA9h	R/W	Protection Control Byte (Block 9)	55h: Write Protect Block 9
			AAh: EPROM Mode Block 9
			55h or AAh: Write Protect 1FA9h
1FAAh - 1FBFh	-	RESERVED	
1FC0h	R/W	Memory Block Lock	55h or AAh: Copy Protect
			Write-Protected Data Memory Pages
			55h or AAh: Write Protect 1FC0h
1FC1h	R/W	Register Page Lock	55h or AAh: Copy Protect 1FA0h-1FC1h
1FC2h	R/W	Factory Byte	55h or AAh: Write protect 1FC2h-1FC4h
			Other: 1FC2h-1FC4h are programmable
1FC3h	R/W	Manufacturer ID	
1FC4h	R/W	Manufacturer ID	
1FC5h	R	RESERVED	

(1) R = Read, W = Write

6.3.3 Address Registers and Transfer Status

The TMF0020 uses three address registers: TA1, TA2, and E/S (Figure 6-2, Figure 6-3, and Figure 6-4).

The registers TA1 and TA2 are loaded with the target address where the data is written and read. Register E/S is a read-only transfer status register used to verify data integrity with write commands. During a Write Scratchpad command, the E/S bits E[4:0] initially load with the incoming T[4:0] and then increment on each incoming subsequent data byte. Thus, E[4:0] is the ending offset counter within the 32-byte scratchpad. The PF bit of the E/S register is a partial byte flag and is set when the received byte is partial (data bits not an integer multiple of 8) or if the scratchpad data is invalid due to a loss of power.

The PF bit clears when there is a successful scratchpad write. The Authorization Accepted (AA) bit of the E/S register is set when there is an authorization match during a Copy Scratchpad command. If AA=1 and PF=0, these values indicate the data stored in the scratchpad has already been copied to the target memory. The AA flag is cleared whenever data is written into the scratchpad. The AA flag is valid only if the PF flag is 0.

Figure 6-2. Target Address (TA1)

7	6	5	4	3	2	1	0

Figure 6-2. Target Address (TA1) (continued)

T7	T6	T5	T4	T3	T2	T2	T0

Figure 6-3. Target Address (TA2)

7	6	5	4	3	2	1	0
T15	T14	T13	T12	T11	T10	T9	T8

Figure 6-4. Ending Address with Data Status (E/S) (Read Only)

7	6	5	4	3	2	1	0
AA	0	PF	E4	E3	E2	E1	E0

6.3.4 Writing Data to the FRAM

The TMF0020 device does not allow writes to the FRAM memory directly by the host. Writing to the FRAM memory directly by the host is achieved by using the scratchpad as an interim repository. To write into the scratchpad, the host first issues the Write Scratchpad command followed by the desired 16-bit target address (LSB first) and the data to be written into the scratchpad. Depending on the conditions described in the Write Scratchpad Command section, the host can receive an inverted CRC16 of the entire write scratchpad sequence (the write scratchpad is commanded, the address and the data) at the end of the Write Scratchpad command sequence.

If the host receives the CRC16 value, the host can compare the received value to the expected computed value. If there is a match, the write scratchpad communication is successful and the host decides on whether to proceed to the Copy Scratchpad command.

If the host does not receive the CRC16 value, then the host can use the Read Scratchpad command to verify integrity of the data stored in the scratchpad. After the Read Scratchpad command is received, the TMF0020 initially transmits the contents of the target address registers (TA1, TA2) and the E/S register. If the PF flag is set, or if the AA flag is set but PF flag cleared, the previous Write Scratchpad command is not successful. In this case, the host can terminate the Read Scratchpad sequence and start another attempt to write data to the scratchpad. If the previous Write Scratchpad is successful, both flags are cleared and the E[4:0] that is read indicates the address of the last byte written to the scratchpad. In this case, the host can continue reading from the TMF0020, verifying all the data bytes. If there is a match, the host can send the Copy Scratchpad command followed by the exact data of the registers TA1, TA2, and E/S that the host obtained by reading the scratchpad. At the end of the Copy Scratchpad sequence, if the authorization pattern matches, the TMF0020 starts copying the scratchpad data to the requested location, provided copy protection is not set, the PF flag is cleared, and there are no Read Memory or Extended Read Memory commands issued between Write and Copy Scratchpad commands.

6.3.5 TMF0020 Device ID

The 64-bit ID identifies each TMF0020. The 48-bit serial number is unique and programmed by Texas Instruments. The default Family code is 43h.

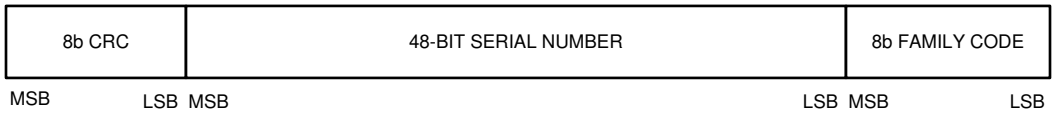

Figure 6-5. 64 bit Factory Programmed EPROM

6.3.6 Bus Termination

The drive output of the TMF0020 is an open-drain, N-channel MOSFET. For proper operation, connect a 500Ω external pull-up resistor on the SDQ single-wire serial interface bus (see Figure 7-1).

6.4 Device Functional Modes

6.4.1 Test Procedures for Functional Tests

This section outlines the specific test procedures used to obtain the parameters listed in the Functional Tests section of the data sheet.

6.4.1.1 Multiple Target Configurations

This test verifies the operation of the TMF0020 in a multi-drop use case. Make sure the host can communicate with multiple devices on the SDQ single-wire serial interface bus. Verify that the presence of other DUTs impacts communication to the selected DUT.

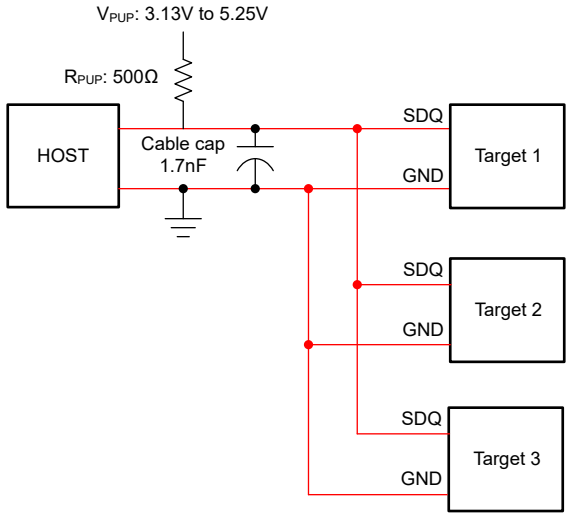

Figure 6-6. Multiple Target Configuration

Successful communication implies executing the following sequence of instructions without failure:

1. Issue RESET in standard speed and check for a presence pulse.
2. Issue SEARCH ROM command to identify the IDs of targets on the SDQ single-wire serial interface bus.
3. Issue RESET in standard speed and check for presence pulse.
4. Select one of the targets by issuing MATCH ROM command with the specific ID of the target identified from the SEARCH ROM command.
5. Issue MEMORY Commands to program or read from the memory.
6. Repeat steps 3, 4, and 5 for other target devices on the SDQ single-wire serial interface bus.

6.5 Programming

6.5.1 Serial Communication

The host reads, programs, or checks the status of the TMF0020 through the command structure of the SDQ single-wire serial interface interface compatible with 1-wire® protocol as shown in Figure 6-7. The command structure includes ROM and MEMORY commands.

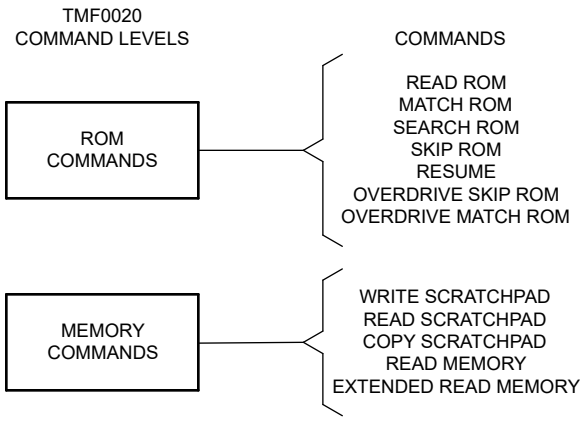

Figure 6-7. Command Structure for the TMF0020

6.5.2 Initialization

The host always begins the transaction with the TMF0020 (target) devices through an initialization process. The initialization process consists of the RESET and PRESENCE pulses. The host generates the RESET pulse, while the TMF0020 devices acknowledge the RESET pulse with the PRESENCE pulse. The host resets the TMF0020 devices by driving the SDQ single-wire serial interface bus low for at least 480µs. The PRESENCE pulse lets the host know that there are one or more TMF0020 devices on the SDQ single-wire serial interface bus.

6.5.3 ROM Commands

After the host detects the presence of one or more target devices on the SDQ single-wire serial interface bus, the host can send one of the 8-bit ROM function commands that the TMF0020 supports depending on the use case scenario. This section describes the scenarios where each of the ROM command can be issued. See Figure 6-7 for the list of these commands.

6.5.3.1 READ ROM Command [33h]

The READ ROM command sequence (shown in Figure 6-8) starts with the host generating the RESET pulse of at least 480µs. The device responds with a PRESENCE pulse. Next, the host continues by issuing the READ ROM command, 33h, and then reads back the 8-bit Family code, 48-bit serial number followed by the 8-bit CRC using the READ signaling (see the Section 6.5.5.2 section) during the data frame. The READ ROM command can be issued by the host only if there is a single TMF0020 device on the SDQ single-wire serial interface bus. If the host issues the command when there are more than 1 target device on the SDQ single-wire serial interface bus, then a data collision occurs since all the target devices try to respond to the host. The host can identify the data collision by comparing the CRC from the READ ROM sequence with the computed CRC, which results in a mismatch.

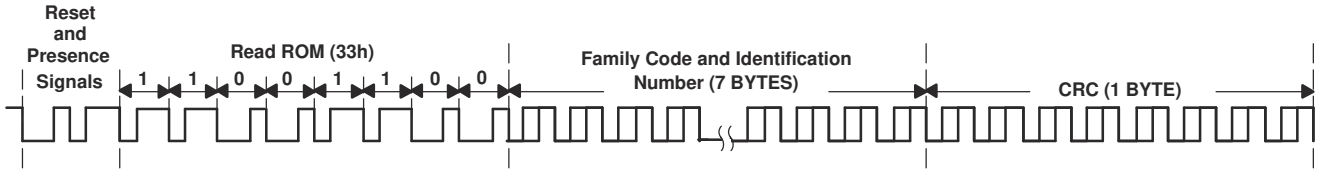

Figure 6-8. READ ROM Sequence

6.5.3.2 MATCH ROM Command [55h]

When there are multiple targets on the bus, the Match ROM command, 55h, is used by the host to select a specific target device when the family code and identification number is known. The host issues the Match ROM command followed by the family code, serial number, and the CRC byte. The target device that matches the 64-bit serial ID is selected and available to perform subsequent memory function commands. The MATCH ROM command can also be used with a single TMF0020 on the bus.

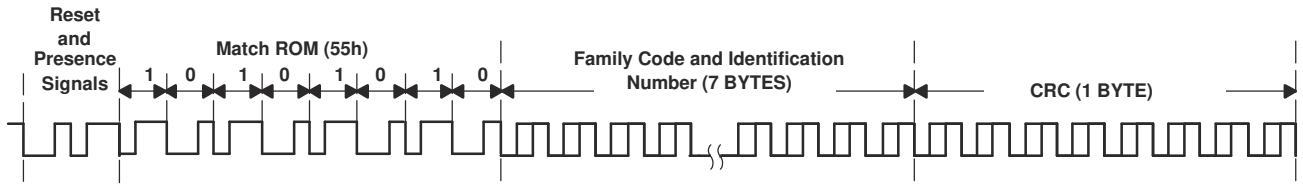

Figure 6-9. MATCH ROM Sequence

6.5.3.3 SKIP ROM Command [CCh]

The SKIP ROM command sequence (shown in Figure 6-10) is the fastest sequence that allows the host to begin transacting with the target device. The Skip ROM command, CCh, allows the host to access the memory functions without issuing the 64-bit serial ID. The Skip ROM command is directly followed by a memory function command. The Skip ROM command is only issued with one device present on the SDQ single-wire serial interface bus. If the SKIP ROM command is issued, when there are multiple targets on the SDQ single-wire serial interface bus, all the targets respond to the subsequent memory command, resulting in a data collision on the bus.

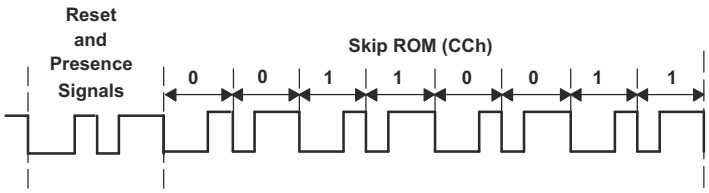

Figure 6-10. SKIP ROM Sequence

6.5.3.4 SEARCH ROM Command [F0h]

The SEARCH ROM command helps to identify the number of devices and the 64-bit unique ID of each of the devices during the initial system bring-up when the host is not aware of the number of devices on the SDQ single-wire serial interface bus. The SEARCH ROM command sequence begins with the host generating a RESET pulse of at least 480µs. All the target devices on the SDQ single-wire serial interface bus responds with a PRESENCE pulse. Next, the host continues by issuing the SEARCH ROM command, F0h. Following the SEARCH ROM command, the host issues three time slots for each bit of the 64-bit serial ID as shown in Figure 6-11. In the first time slot, the target devices begins to transmit the bit of the 64 serial ID starting with the least significant bit. In the second time slot, the target devices transmit the complement of the bit. In the third time slot, the host writes the bit to be selected. The process continues until the end of the 64-bit serial ID. All the target devices that do not match the bit written by the host in the third time slot exits from the search process. If the host read zeros in the first two time slots, then a collision condition has occurred. The host knows there is more than one device on the SDQ single-wire serial interface bus. By choosing the bit value to write, the host is branching out to eliminate one or more contending target devices. At the end of the first run sequence, the host knows the serial ID of a single device. The sequence is then repeated to identify the serial IDs of the remaining devices on the SDQ single-wire serial interface bus.

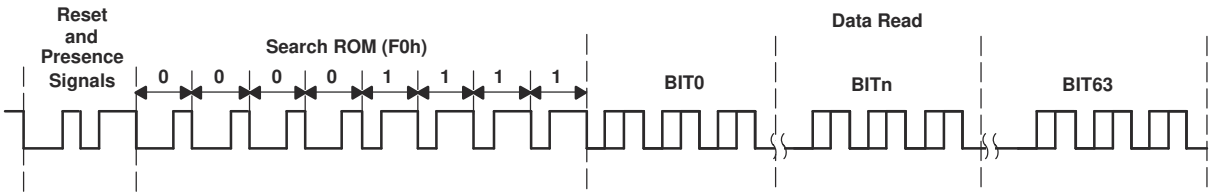

Figure 6-11. SEARCH ROM Sequence

6.5.3.5 RESUME Command [A5h]

When there are multiple targets on the SDQ single-wire serial interface bus, the RESUME command, A5h, can be used to maximize the data throughput by reducing the number of bit transactions needed to select the target

device. Before issuing the RESUME command, the host must first select the target device by issuing the MATCH ROM or OVERDRIVE MATCH ROM command sequence. This selects the target device. All other targets do not respond to subsequent memory function commands and RESUME command function.

6.5.3.6 OVERDRIVE SKIP ROM Command [3Ch]

The TMF0020 supports a high-speed mode called the Overdrive mode. The OVERDRIVE SKIP ROM command sequence starts with the host generating the RESET pulse of at least 480µs. The TMF0020 responds with a PRESENCE pulse. Next, the host continues by issuing the OVERDRIVE SKIP ROM command, 3Ch, in standard speed. The device now enters Overdrive mode. Make sure all subsequent communication with the target device is at overdrive speed. The host can bring all the target devices back to standard speed by issuing a reset pulse of at least 480µs.

If the OVERDRIVE SKIP ROM command is issued when there are multiple targets on the SDQ single-wire serial interface bus, all the target devices enter Overdrive mode. All subsequent communication addresses a specific device. This procedure is initiated by issuing a reset pulse at overdrive speed followed by an OVERDRIVE MATCH ROM or SEARCH ROM command sequence. This speeds up the time for the search process. If the OVERDRIVE SKIP ROM command issues when there are multiple targets on the SDQ single-wire serial interface bus, all the targets begin responding to the subsequent memory command resulting in a bus data collision.

6.5.3.7 OVERDRIVE MATCH ROM Command [69h]

The OVERDRIVE MATCH ROM command is used to select a specific target device when there are multiple target devices on the SDQ single-wire serial interface bus and set the selected target into Overdrive mode at the same time. The OVERDRIVE MATCH ROM command can also be used with a single target device on the bus. The target device that matches the 64-bit serial ID is selected and available to perform subsequent memory function commands in overdrive speed. Other target devices that are already in Overdrive mode continue to be in Overdrive mode until the host brings all the target devices back to standard speed by issuing a reset pulse of at least 480 µs.

6.5.4 Memory Function Commands

6.5.4.1 Write Scratchpad Command [0Fh]

The Write Scratchpad command, 0Fh, is used to write to the scratchpad. After selecting the target TMF0020 using the ROM command, the host provides the 2-byte target address (LSB first) followed by the data. The device sets the 5 LSB bits of the 2-byte address as the scratchpad offset address. Additionally, the 5 LSB bits of the E/S register (E[4:0]) are also loaded with the scratchpad offset address. For each subsequent data byte, both the scratchpad offset address and the E/S bits (E[4:0]) are incremented. If the data byte is partial, that data byte is ignored and an error flag called the partial byte flag (PF) is set. This flag is also set if full 2-byte address is not received. This flag is cleared once the device receives a complete 2-byte address.

During the execution of the Write Scratchpad command, the internal CRC generator computes the 16-bit CRC based on the data stream, which includes the write scratchpad command (0Fh), the 2-byte address, and the data bytes. The CRC is generated using the CRC16 polynomial ($X^{16} + X^{15} + X^2 + 1$) by first clearing the CRC generator. The host can terminate the Write Scratchpad command sequence at any time by issuing a RESET command. The host can read the 16-bit CRC generated by the TMF0020 device when the scratchpad offset address reaches 11111b.

The TMF0020 memory address range is 0000h to 1FC5h, therefore, if the host attempts to write beyond the address range, the internal circuitry of the device sets the six most significant address bits to zero as the 2-byte address is shifted into the internal address register. This modified address can be read back from the Read Scratchpad command. If the host issues a Copy Scratchpad command without reading the scratchpad and verifying the address and the data bytes, the memory contents in the scratchpad is not copied to the destination FRAM memory. If the host attempts to write to a memory location that is write-protected, the device copies the data byte from the 2-byte address from the FRAM memory into the scratchpad instead of the data byte written by the host. In a similar manner, if the host attempts to write to a memory location that is EPROM-protected,

the device copies the bit-wise logical AND of the data byte written by the host and the data byte from the 2-byte address from the FRAM memory into the scratchpad.

6.5.4.2 Read Scratchpad Command [AAh]

To read the scratchpad, the host issues the Read Scratchpad command (AAh) and then reads the 2-byte address, the Ending Offset/Data Status byte (E/S), and finally the scratchpad data starting at the scratchpad offset address. The host verifies the address, E/S byte, and the scratchpad data match with the information transmitted during the Write Scratchpad command. The validity of the 2-byte address and the scratchpad data can be verified with the Read Scratchpad command. The host can read the inverted CRC16 once reaching the end of the scratchpad. If the host continues reading after reading the 2 CRC bytes, the host only receives 1s.

6.5.4.3 Copy Scratchpad [55h]

To copy the data from the scratchpad to the FRAM memory, the host can issue the Copy Scratchpad command (55h), followed by the 2-byte address and the E/S byte (referred to as Authorization code) obtained from the Read Scratchpad command. The device copies the scratchpad to the FRAM memory beginning with the target address and ending with the target address plus the scratchpad offset address listed in the E/S byte only if the authorization code matches with the E/S byte, the PF flag is not set, and the target address is within the addressable range. If the host continues to read, the device transmits alternating 0s and 1s. The host can terminate the Copy Scratchpad command sequence by issuing a reset pulse, but only after t_{PROG} duration has elapsed. The TMF0020 does not allow the memory copy by resetting the AA flag if the memory pages are copy-protected pages or if the PF flag is set. This operation can be verified by reading the AA flag bit in the E/S byte through the Read Scratchpad command.

6.5.4.4 Read Memory [F0h]

The host can read the FRAM memory by issuing the Read Memory command (F0h), followed by the 2-byte address (LSB first). If the host issues an address greater than 1FC5h, the device sets the six most significant address bits to zero. The host then reads the data from either the address within the address range or the modified address until address 1FC5h is reached. If the host continues to read further, the TMF0020 transmits 1s. The host can terminate the Read Memory command sequence by issuing a reset pulse.

6.5.4.5 Extended Read Memory [A5h]

The Extended Read Memory command works similar to the Read Memory command, except for the 2-byte CRC that is transmitted at the end of each memory page. The host can read the FRAM memory by issuing the Extended Read Memory command (A5h), followed by the 2-byte address (LSB first). If the host issues an address greater than 1FC5h, the device sets the six most significant address bits to zero. The host can then read the data from either the address within the address range or the modified address until the end of a 32-byte page. At the end of the memory page, the host reads the 2-byte inverted CRC. If the host continues to read, the host receives the data corresponding to the beginning of next page and so on until the end address 1FC4h is reached. If the host continues to read further, the TMF0020 transmits 1s. The host can terminate the Read Memory command sequence by issuing a reset pulse.

6.5.4.6 Memory Command Flow Charts

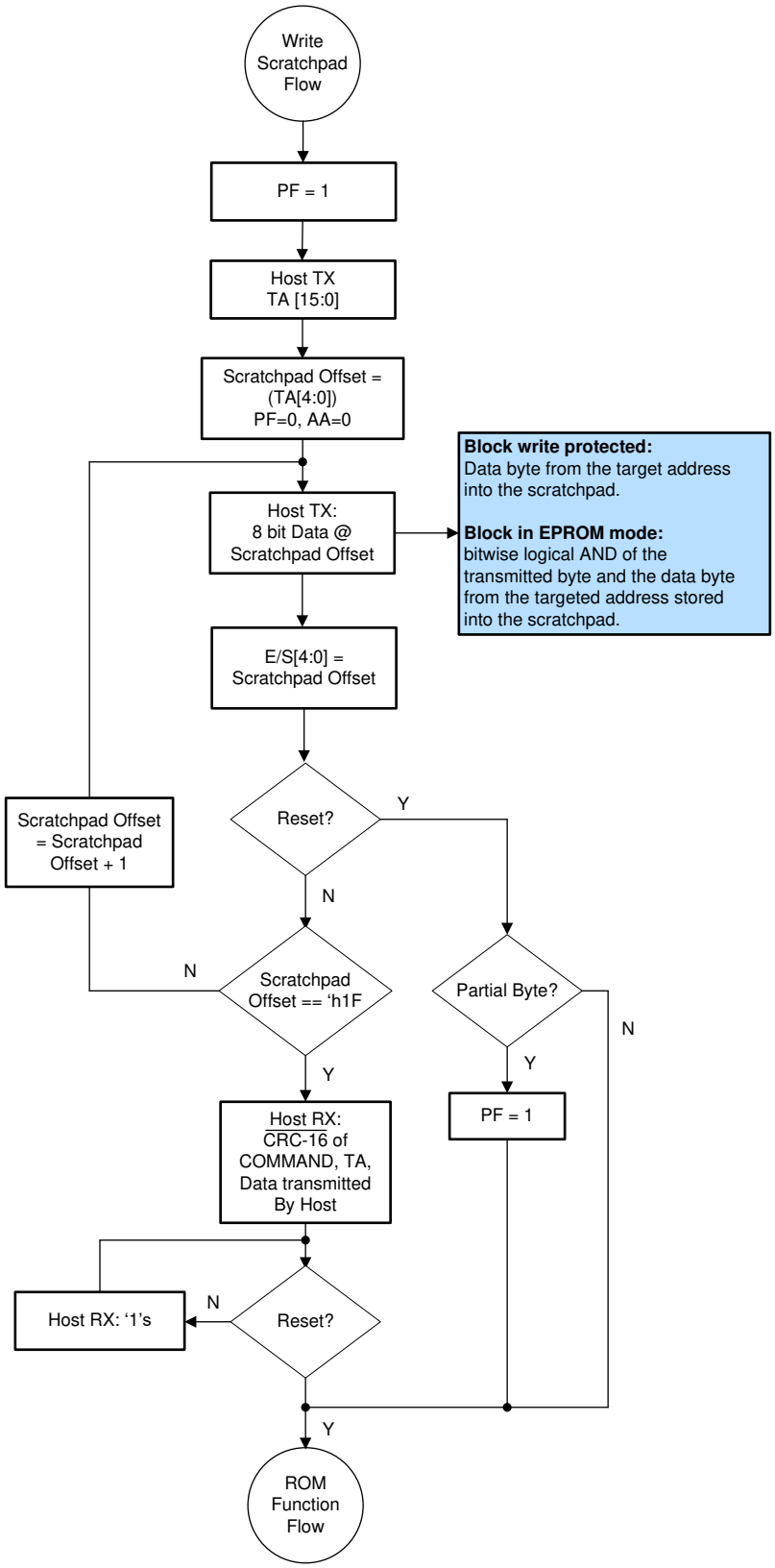

Figure 6-12. Write Scratch Pad Flowchart

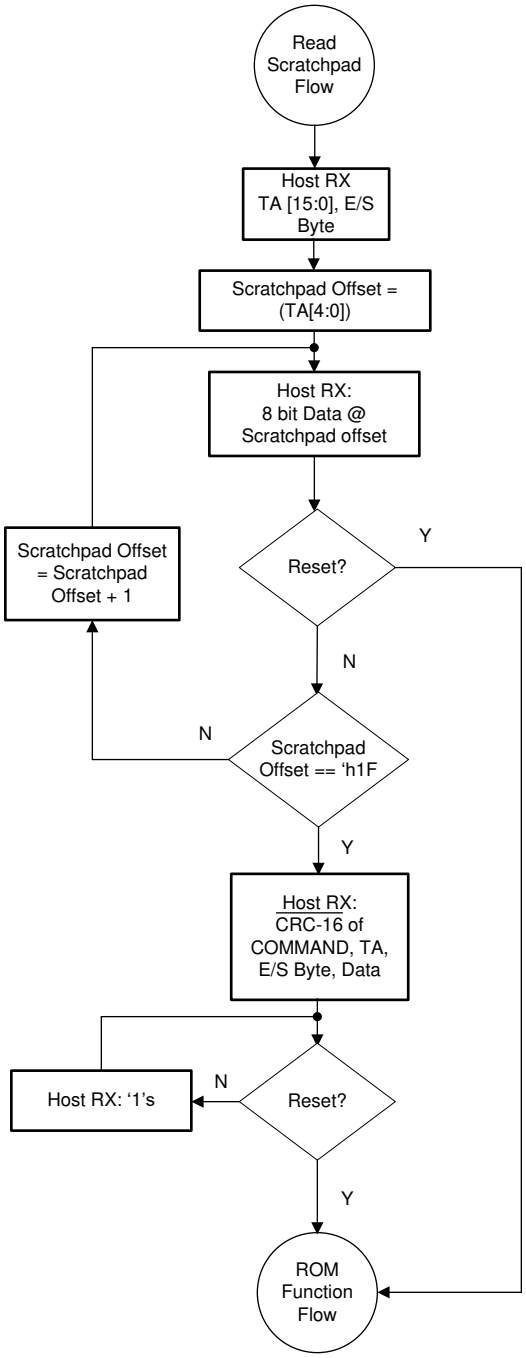

Figure 6-13. Read Scratch Pad Flowchart

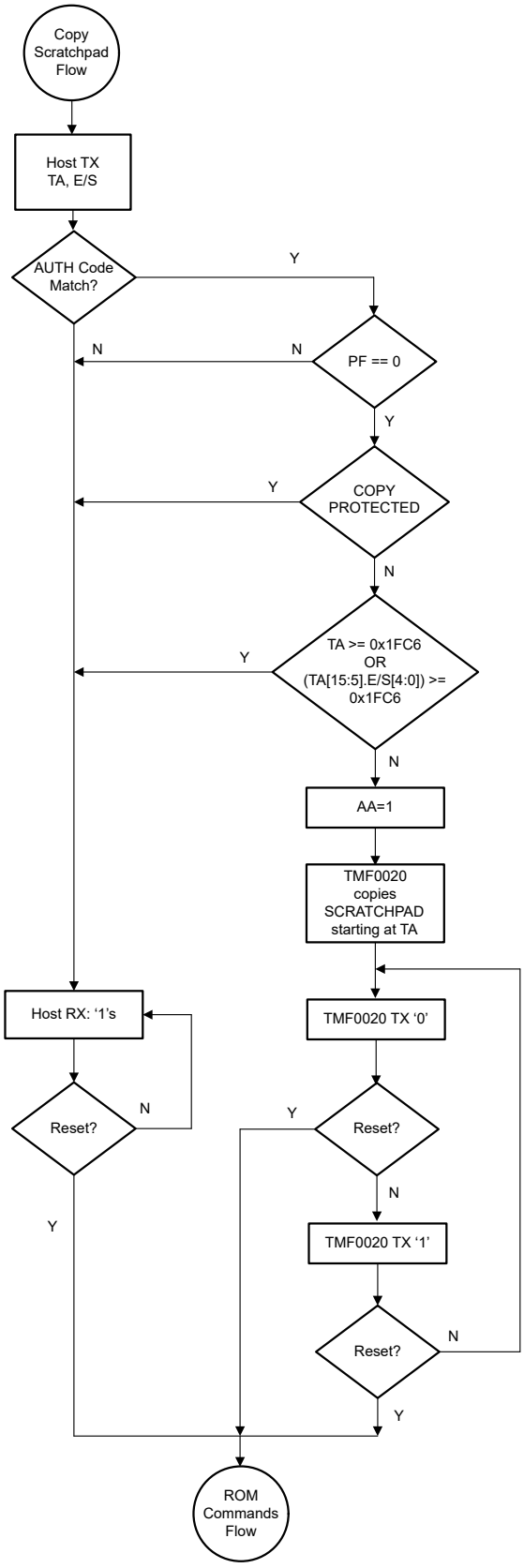

Figure 6-14. Copy Scratch Pad Flowchart

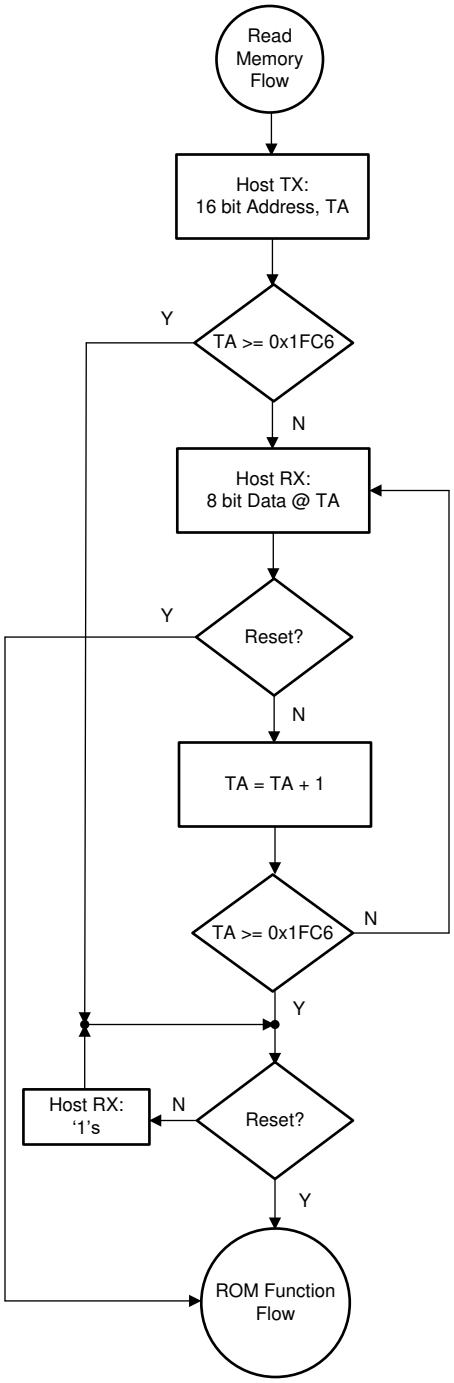

Figure 6-15. Memory Read Flowchart

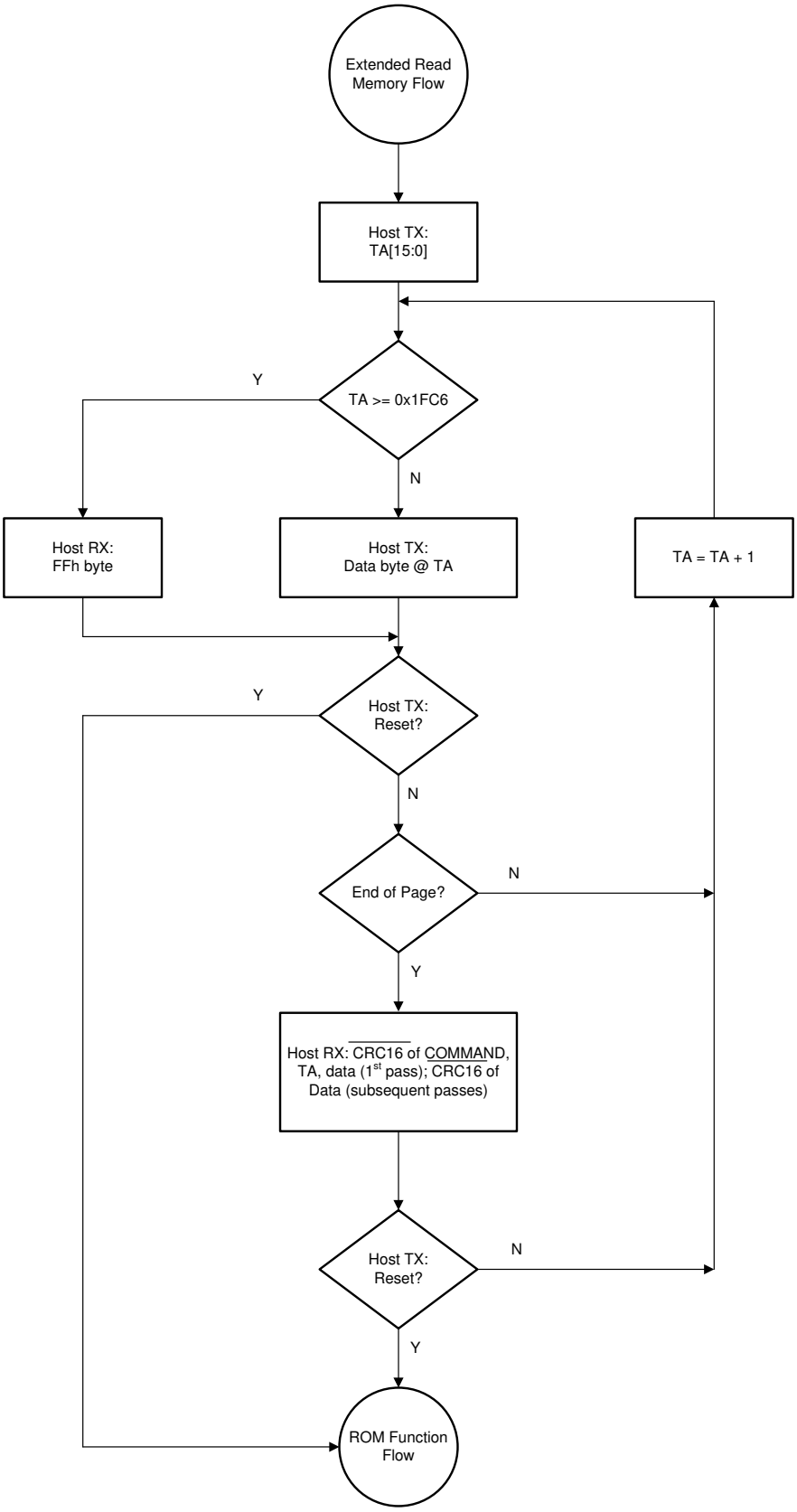

Figure 6-16. Extended Memory Read Flowchart

6.5.5 SDQ single-wire serial interface Signaling

The single wire communication does not have a reference clock, and adhering to stringent timing protocols to maintain the data integrity is critical. The timing protocol (compatible with 1-wire® protocol) consists of four types of signaling:

1. Reset sequence with reset pulse and presence pulse
2. Write-zero timing sequence
3. Write-one timing sequence
4. Read-data timing sequence

The host initiates the communication by pulling the SDQ single-wire serial interface line low, except for the presence pulse, which is initiated by the target devices on the SDQ single-wire serial interface bus. The target devices can communicate at two different speeds: standard and overdrive. The target device by default only communicates at standard speed unless the device is set into the Overdrive mode, in which case the target device responds to commands issued in the Overdrive timing (fast timing). All of the timing waveforms below are applicable to both Standard timing and Overdrive timing.

All SDQ single-wire serial interface signaling begins with initializing the device, followed by the host driving the bus low either to write a 1 or 0, or to begin the start frame for a bit read. Reset Sequence Timing Diagram shows the initialization timing, whereas Write-One Timing Diagram, Write-Zero Timing Diagram, and Read-Data Timing Diagram show that the host initiates each bit by driving the SDQ single-wire serial interface bus low for the start period, t_{W1L} / t_{W0L} / t_{RL}. After the bit is initiated, either the host continues controlling the bus during a WRITE, or the target device controls the bus to transfer a 0 bit during a READ.

6.5.5.1 RESET and PRESENCE PULSE

During the reset sequence, if the SDQ single-wire serial interface bus is driven low for more than 120µs, the target devices can be reset. If the SDQ single-wire serial interface bus is driven low for more than 480µs, then the target devices reset and indicate that the devices are ready for communication by responding with a presence pulse. If the TMF0020 is in Overdrive mode and a t_{RSTL} duration of 480µs or longer is issued by the host, the device exits the Overdrive mode returning to standard speed. If the device is in Overdrive mode and t_{RSTL} is no longer than 80µs, the device remains in Overdrive mode. If the device is in Overdrive mode and t_{RSTL} is between 80µs and 480µs, the device resets, but the communication speed is undetermined.

Reset Sequence Timing Diagram shows the reset pulse initiated by host and the presence pulse response initiated by TMF0020 (target).

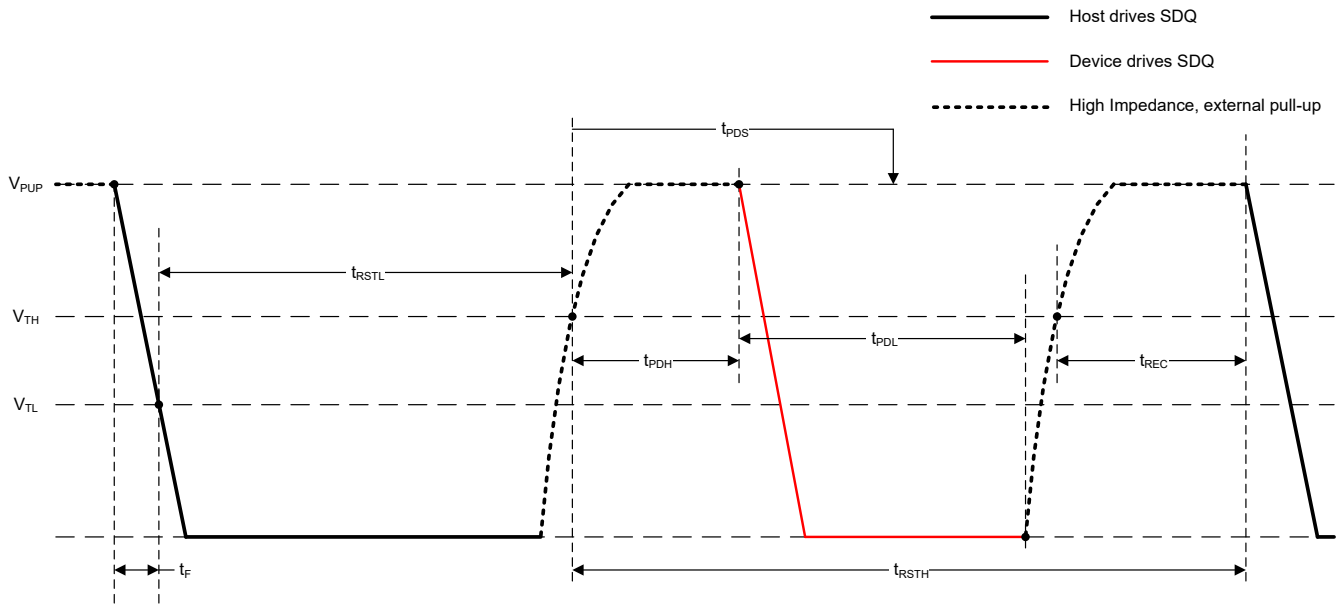

Figure 6-17. Reset Sequence Timing Diagram

6.5.5.2 Write-Read-Time Slots

The single wire interface communication does not have a reference clock. Hence, all communication is performed asynchronously with fixed time slot (t_{SLOT}) widths and variable pulse width to indicate logic 0 and 1. In idle state, the external pullup resistor holds the line high. The host initiates the communication by driving the data line low regardless of if the communication is a write or a read, and the bit value is decoded as the time for which the data line is held low.

Even though the communication is one bit at a time, the data exchanged between the host and device is performed at byte boundary. Every byte is sent least significant bit first. The device behavior is not verified when incomplete bytes are sent.

The Write-One timing diagram in Write-One Timing Diagram shows that the host initiates the write-one transmission by pulling the SDQ single-wire serial interface bus low for the t_F + t_{W1L} - t_ε duration and then releasing the SDQ single-wire serial interface bus. Similarly, the Write-Zero timing diagram in Write-Zero Timing Diagram shows that the host initiates the write-zero transmission by the pulling the SDQ single-wire serial interface bus low for the t_F + t_{W0L} - t_ε duration and then releasing the SDQ single-wire serial interface bus. As the voltage on the SDQ single-wire serial interface bus falls below the threshold V_{TL}, the device starts the internal timing generator that determines when the SDQ single-wire serial interface line is sampled during a write-time slot to determine whether the bit is 1 or 0. The device samples the SDQ single-wire serial interface line some time between the max t_{W1L} duration and the min t_{W0L} duration.

The read-data timing diagram in Read-Data Timing Diagram shows that the host initiates the transmission of the bit by pulling the SDQ single-wire serial interface bus low for the t_F + t_{RL} duration. The device then responds by either driving the SDQ single-wire serial interface bus low to transmit a READ 0 or releasing the SDQ single-wire serial interface bus to transmit a READ 1. The host must factor the rise time due to the pullup resistor and bus capacitance, to determine the sampling window to sample the bit level sent by the device or driving the next read bit time slot.

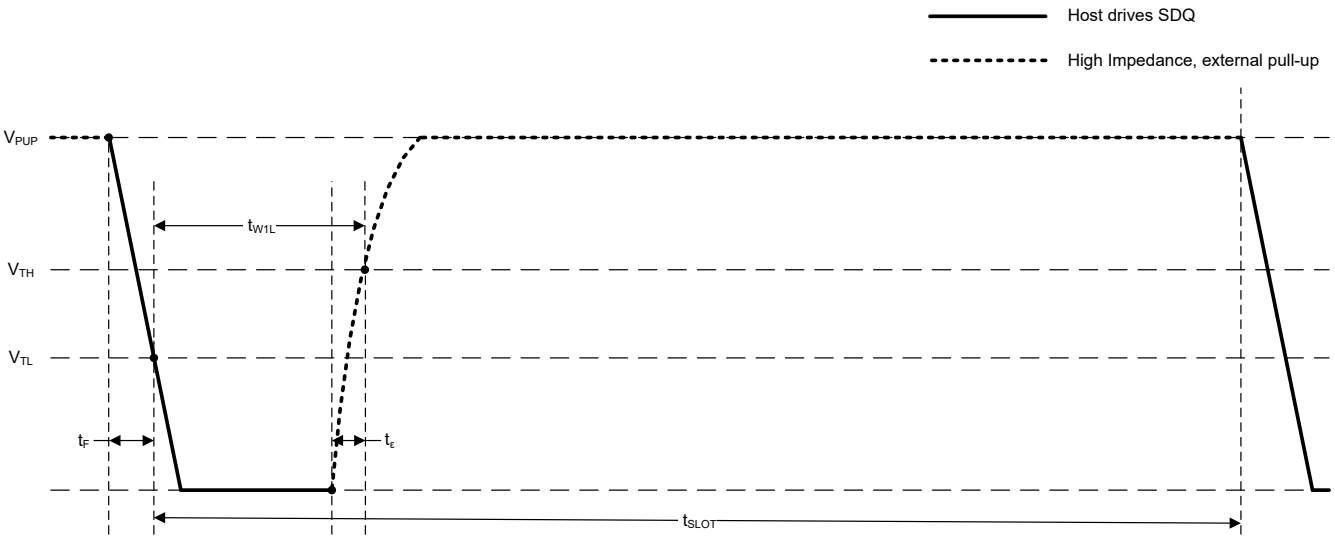

Figure 6-18. Write-One Timing Diagram

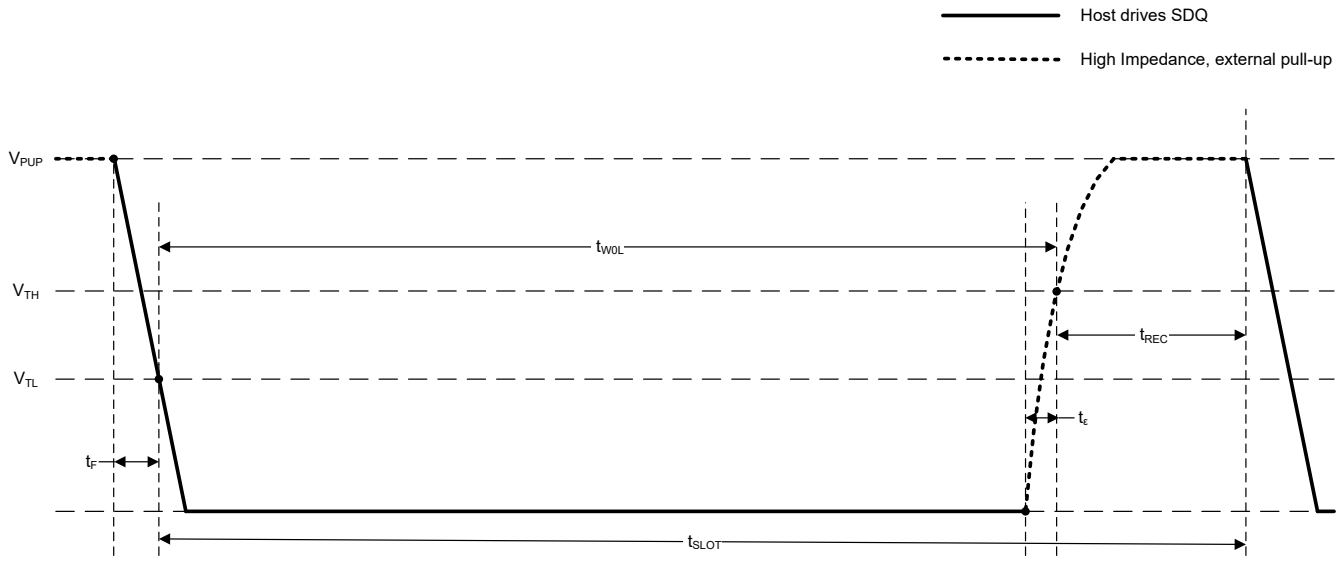

Figure 6-19. Write-Zero Timing Diagram

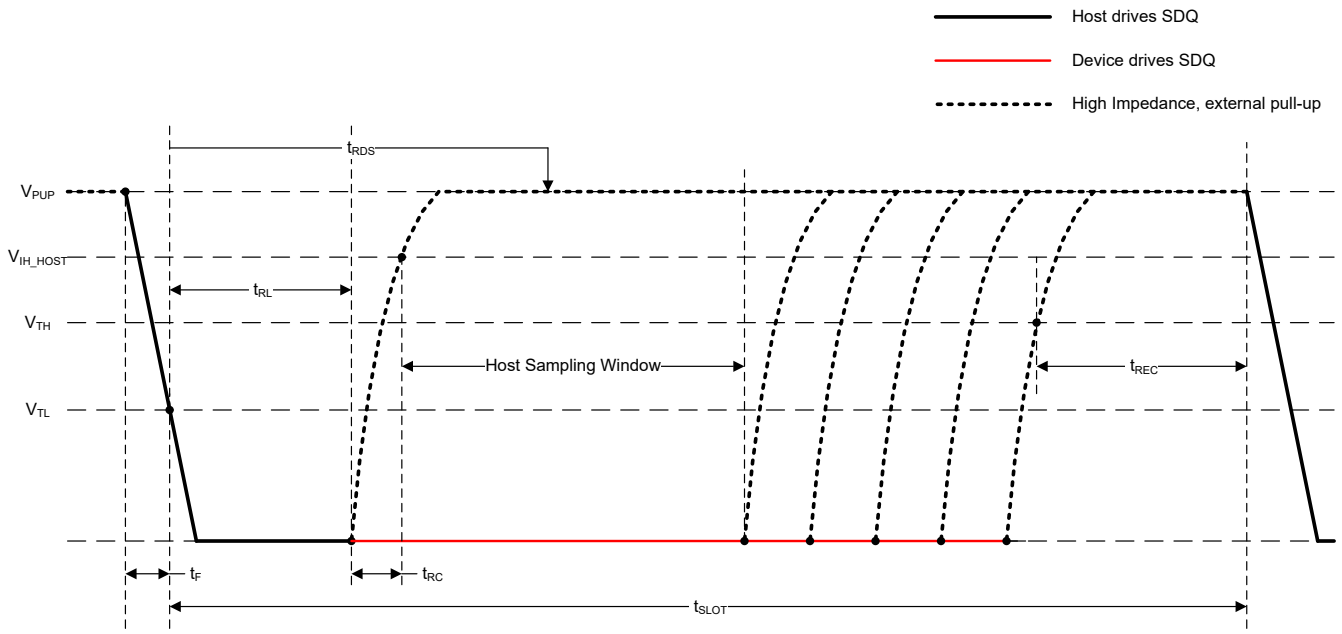

Figure 6-20. Read-Data Timing Diagram

6.5.6 IDLE

If the SDQ single-wire serial interface bus is high, the bus is in the IDLE state. Suspend bus transactions by leaving the SDQ single-wire serial interface bus in IDLE. Bus transactions can resume at any time from the IDLE state.

6.5.7 CRC Generation

The TMF0020 has an 8-bit CRC stored in the most significant byte of the 64-bit ROM. The bus host can compute a CRC value from the first 56 bits of the 64-bit ROM and compare the CRC value to the value stored within the TMF0020 to determine if the ROM data the bus host receives is error-free. The equivalent polynomial function of this CRC is:

$$X^8 + X^5 + X^4 + 1 \quad (1)$$

The bus host entirely determines the comparison of CRC values and decision to continue with an operation. No circuitry on the TMF0020 prevents a command sequence from proceeding if the CRC stored in or calculated by the device does not match the value generated by the bus host. Proper use of the CRC can result in a communication channel with a high level of integrity.

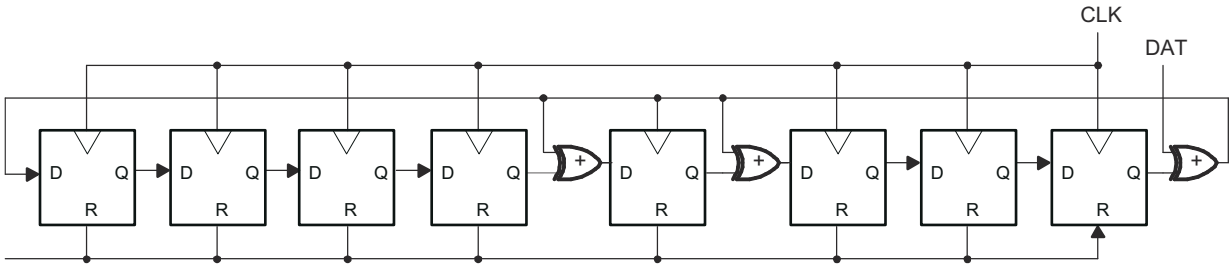

Figure 6-21. 8-Bit CRC Generator Circuit ($X^8 + X^5 + X^4 + 1$)

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

A typical application consists of a microcontroller configured as the SDQ single-wire serial interface communication host device, and a TMF0020 as the SDQ single-wire serial interface target device. The host and target have open drain functionality for which a pull-up resistor (typically 500Ω) is required connected to a pull-up voltage in the range of 3.13V to 5.25V.

7.2 Typical Application

Avoid additional capacitances on the SDQ single-wire serial interface bus. Any capacitance greater than C_{CABLE} can result in a communication failure. Do not add decoupling or bypass capacitors to the SDQ single-wire serial interface line.

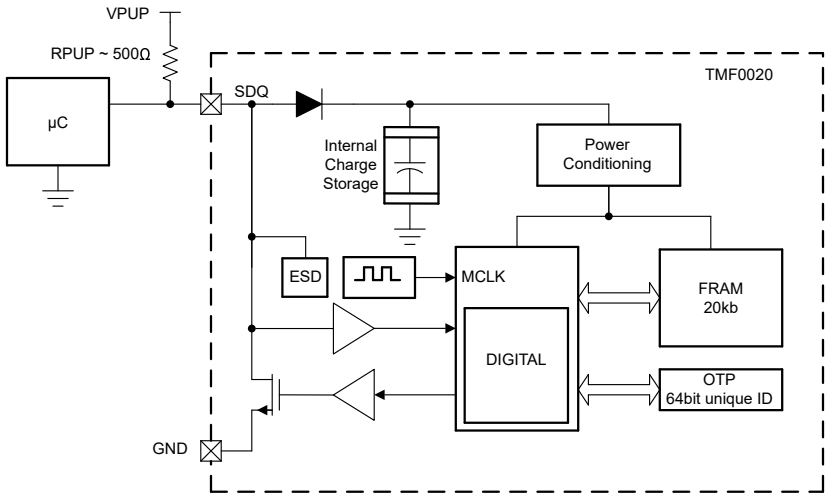

Figure 7-1. Typical Application Circuit

7.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Pull-up voltage	3.13V to 5.25V
Operating free-air temperature	-10 ℃ to 85 ℃
Pull-up resistor	500Ω

7.2.2 Detailed Design Procedure

Implementing the SDQ single-wire serial interface host using bit-banging over GPIO is possible. In this case, consider additional error checking for the reset routine of the TMF0020 to verify that the target operates as expected on the bus.

Whenever the host sends a reset, the target devices acknowledge the reset with a presence pulse. Before the presence pulse, the host must confirm that the bus releases and returns to a high level, indicating that nothing is holding the bus unexpectedly low. As the minimum t_{PDH} is 15µs, the host look for a logic high on the bus 10µs after releasing the bus at the end of the reset is sufficient to confirm the bus released for the target devices to acknowledge.

7.2.3 Application Curves

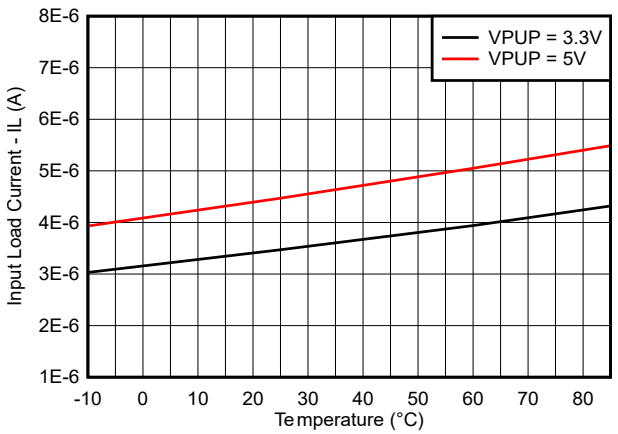

Figure 7-2. Input Load Current (I_L) vs Temperature (Standard Speed)

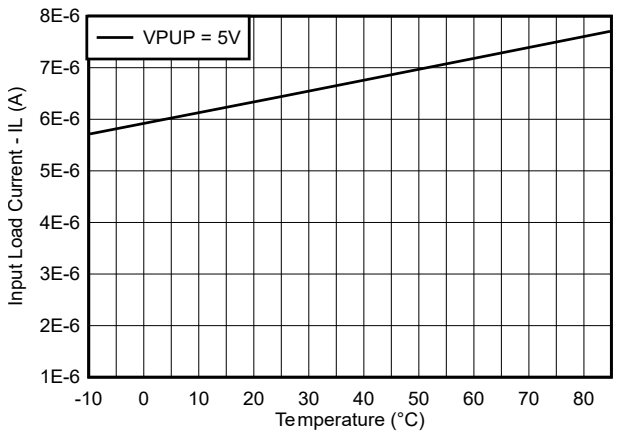

Figure 7-3. Input Load Current (I_L) vs Temperature (Overdrive Speed)

7.3 Power Supply Recommendations

The TMF0020 is a low-power device that only needs to turn on when communicating. The device power comes from the voltage supply used for digital I/O in the system. A dedicated VCC pin does not exist in the device; a supply input bypass capacitor is not required or recommended. The device obtains power from the SDQ single-wire serial interface communication input which is sustainable during normal communication activity.

The ramp time of the SDQ single-wire serial interface voltage when power is initially applied can be slow due to current limiting from the source. Ramp times greater than 200µs can cause undesired bouncing of the POR circuit and result in the device not generating a presence pulse. To account for this undesired effect on the device, a best practice for the communication host is to issue a *hard* reset to the device by pulling down the SDQ single-wire serial interface line for >5ms and then releasing the SDQ single-wire serial interface bus before issuing the reset pulse that is approximately 480µs long.

Figure 7-4 illustrates the best practice for dealing with initial power on ramps.

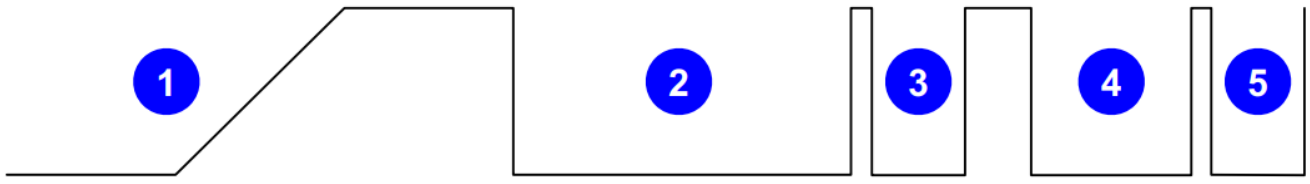

Figure 7-4. Power-Up Best Practice

1. Initial power-on ramps can be long in duration.
2. The host issues a *hard* reset of > 5ms, resetting the device

3. TMF0020 responds to the hard reset by issuing a presence pulse.
4. Apply a *soft* reset of approximately 480µs after the previous presence pulse.
5. TMF0020 responds to the soft reset by issuing a presence pulse.

7.4 Layout

7.4.1 Layout Guidelines

The TMF0020 only has one signal, SDQ single-wire serial interface. Routing the signal trace directly from the SDQ single-wire serial interface pin of TMF0020 to the external connector of the application system or to the host device is advised. Shield the signal trace properly with a parallel ground plane as shown in Figure 7-5. If a ground plane is not available to the TMF0020, then connect the GND pin with a large trace surrounding most of the device and have the SDQ single-wire serial interface trace parallel with GND back to the host.

7.4.2 Layout Example

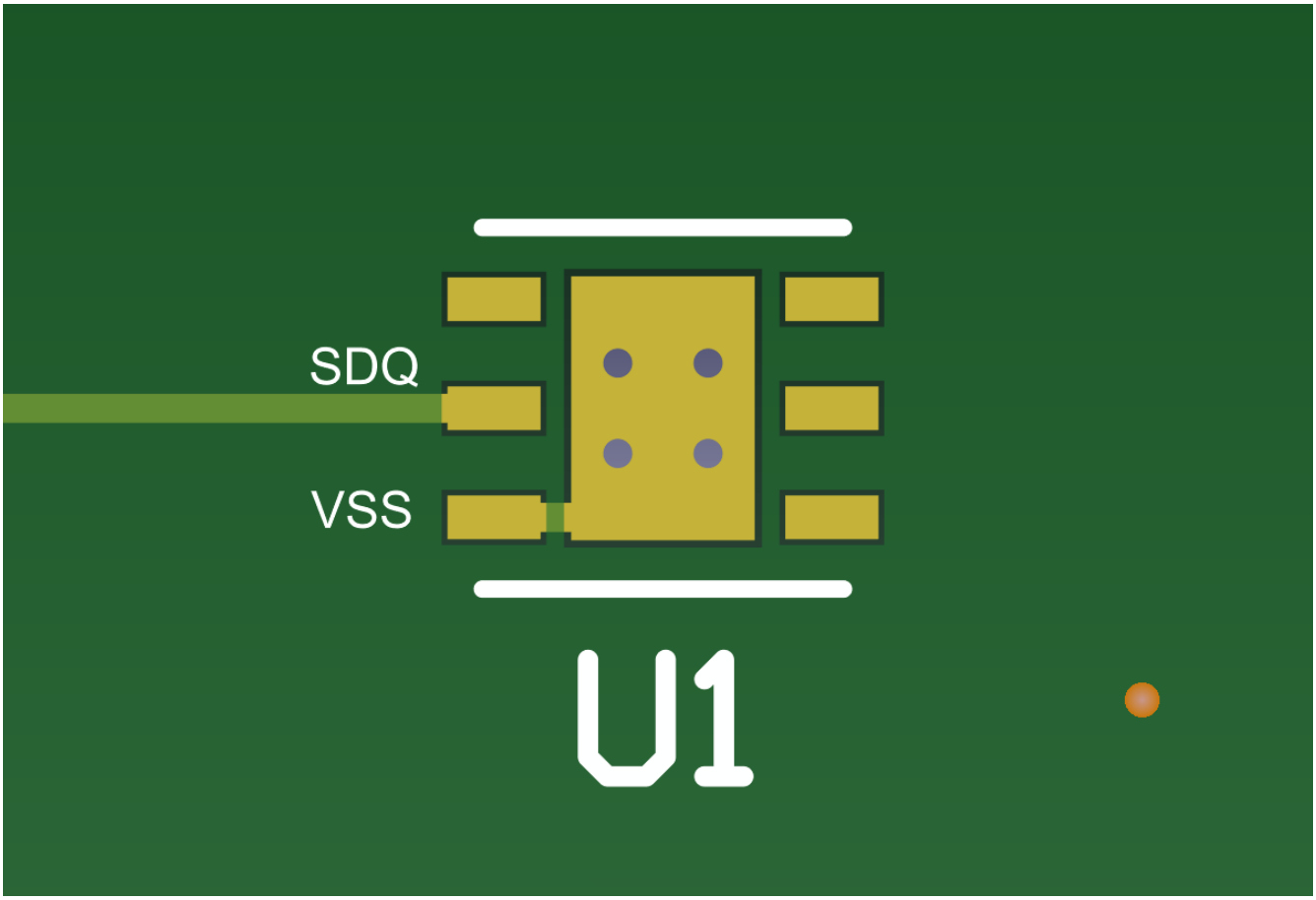

Figure 7-5. Example Board Layout

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

SDQ™ and TI E2E™ are trademarks of Texas Instruments.
1-Wire® is a registered trademark of Texas Instruments.
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8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2026	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
TMF0020DRPR	ACTIVE	SON	DRP	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-10°C to 85°C	TMF0020

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

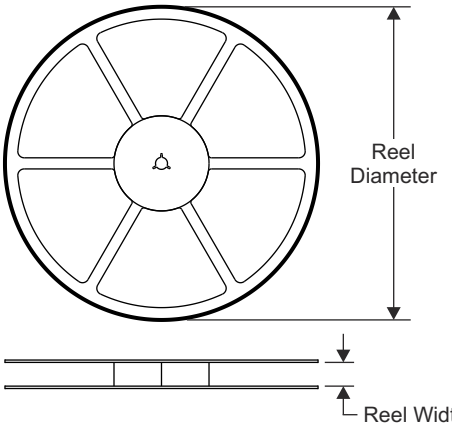
(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

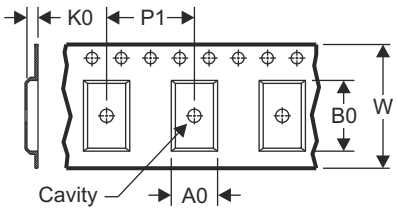
(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

10.2 Tape and Reel Information

REEL DIMENSIONS

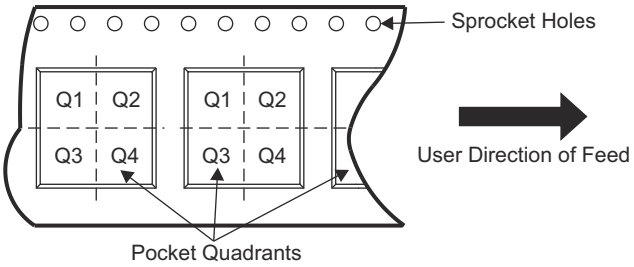


TAPE DIMENSIONS



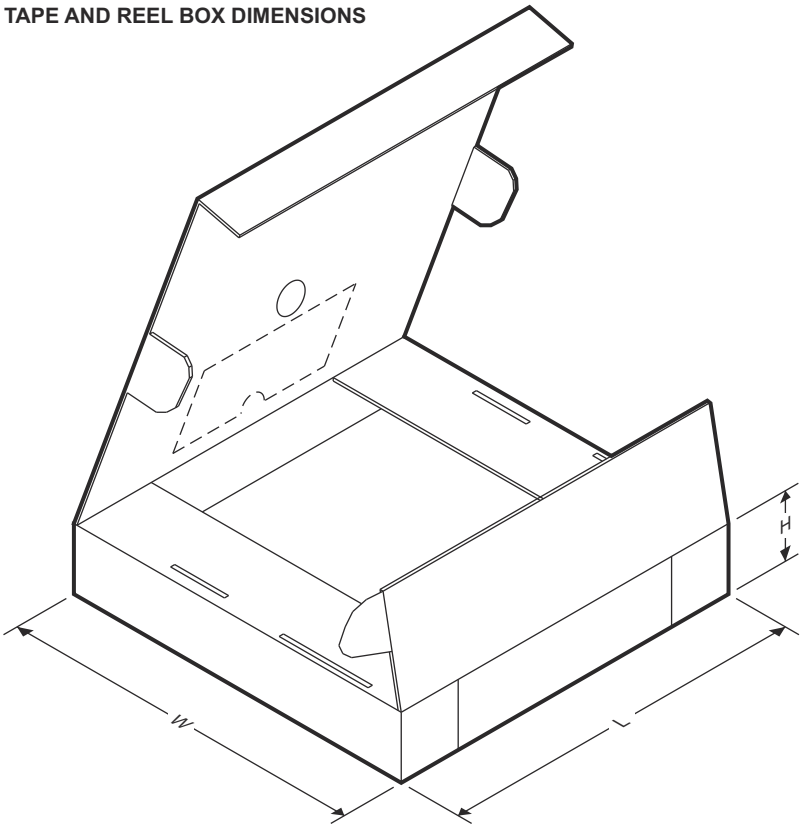
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMF0020DRPR	SON	DRP	6	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

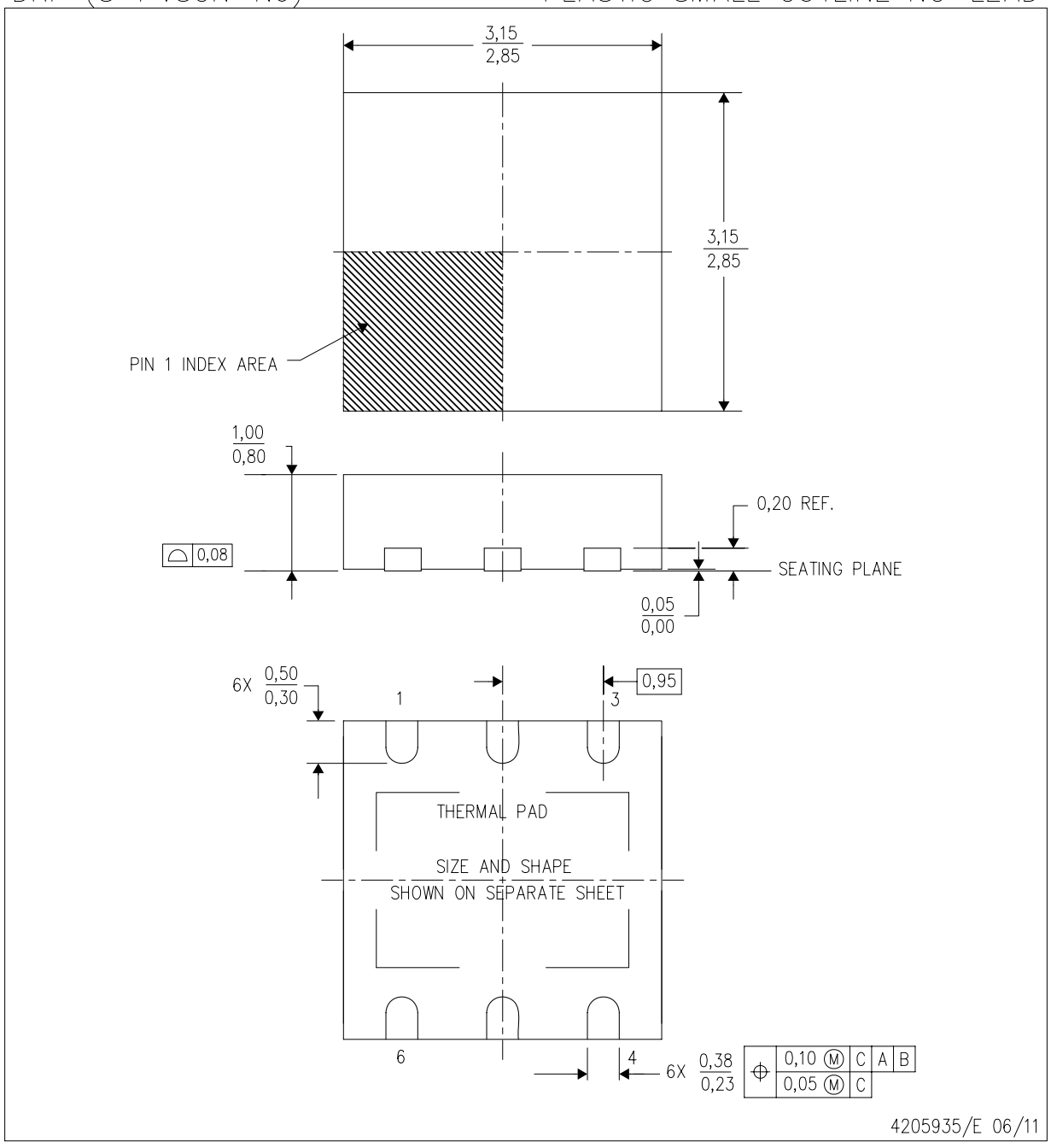
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMF0020DRPR	SON	DRP	6	3000	367.0	367.0	35.0

MECHANICAL DATA

DRP (S–PVSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL PAD MECHANICAL DATA

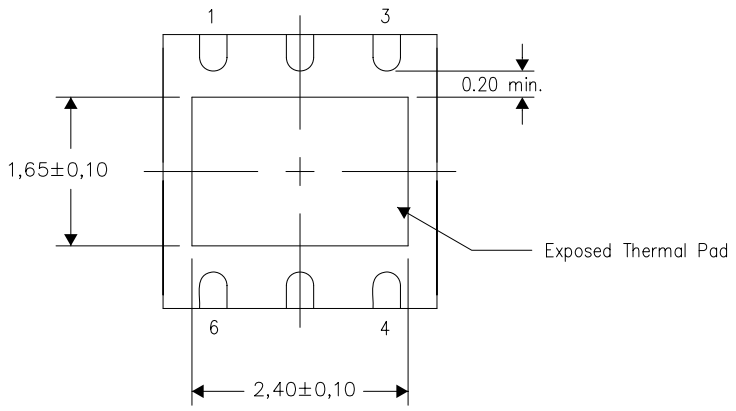
DRP (S–PVSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

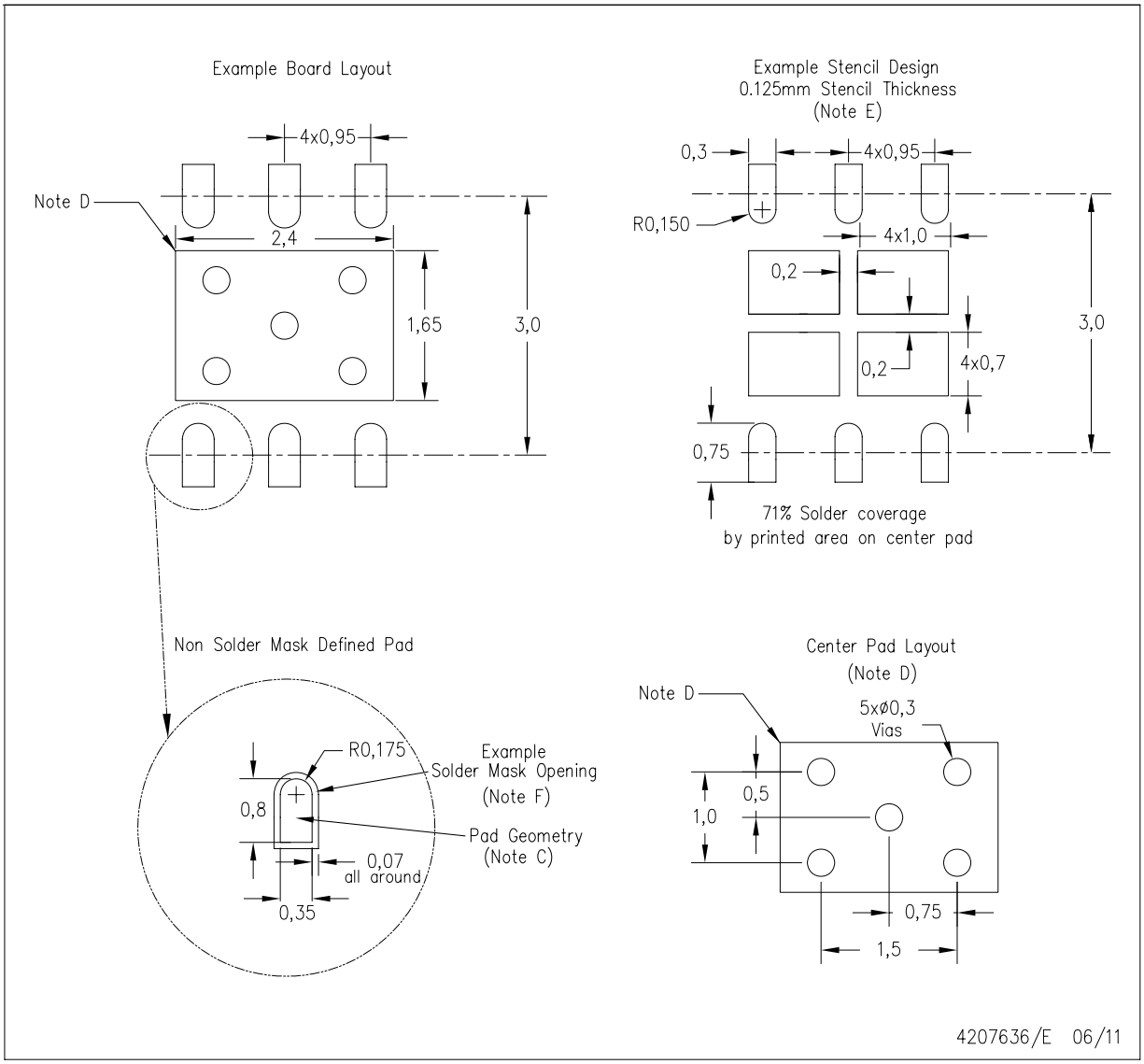
Exposed Thermal Pad Dimensions

4207637/G 06/11

NOTE: All linear dimensions are in millimeters

LAND PATTERN DATA

DRP (S–PVSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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Last updated 10/2025