TMP108 Low Power Digital Temperature Sensor With Two-Wire Serial Interface in WCSP

1 Features

- Dynamically-programmable limit window with under- and overtemperature alerts
- Accuracy:
  ±0.75°C (maximum) from –20°C to +85°C
  ±1°C (maximum) from –40°C to +125°C
- Low quiescent current:
  6 μA active (maximum) from –40°C to +125°C
- Supply range: 1.4 V to 3.6 V
- Resolution: 12 bits (0.0625°C)
- Package: 1.2-mm × 0.8-mm, 6-ball WCSP

2 Applications

- Smartphone and tablet thermal management
- Battery management
- Thermostat control
- Under- and overtemperature protection
- Environmental monitoring and HVAC

3 Description

TMP108 is a digital-output temperature sensor with a dynamically-programmable limit window, and under- and overtemperature alert functions. These features provide optimized temperature control without the need of frequent temperature readings by the controller or application processor.

The TMP108 features SMBus and two-wire interface compatibility, and allows up to four devices on one bus with the SMBus alert function.

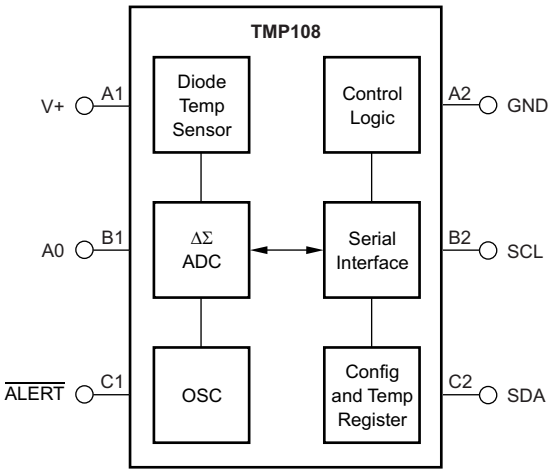
The TMP108 is designed for thermal management optimization in a variety of consumer, computer, and environmental applications. The device is specified over a temperature range of –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMP108	DSBGA (6)	1.20 mm × 0.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Original (April 2013) to Revision A **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed supply voltage maximum value from: 3.6 V to: 4 V ... 3
- Changed input voltage maximum value for the SDA and SCL pins from: 3.6 V to: 4 V ... 3
- Changed input voltage maximum value for the A0 and $\overline{\text{ALERT}}$ pins from: (V+) + 0.3 V to: ((V+) + 0.5) and ≤ 4 V ... 3
- Changed *Temperature Error at +25°C* graph ... 8

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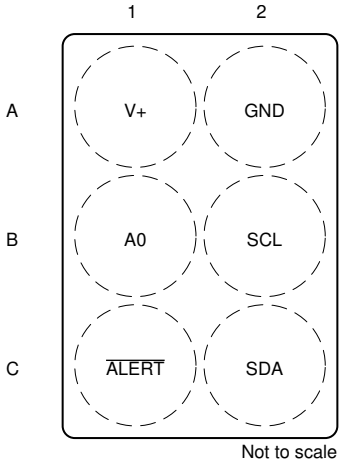
5 Pin Configuration and Functions

YFF Package
6-Pin DSBGA
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A0	B1	I	Address selection pin. Connect to GND, V+, SDA, or SCL.
$\overline{\text{ALERT}}$	C1	O	Alert output pin
GND	A2	—	Ground
SCL	B2	I	Input clock pin
SDA	C2	I/O	Input/output data pin
V+	A1	I	Supply voltage (1.4 V to 3.6 V)

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Supply voltage			4	V
Input voltage	SDA and SCL(2)	–0.5	4	V
	A0 and $\overline{\text{ALERT}}$	–0.5	((V+) + 0.5) and ≤ 4	V
Operating temperature		–55	150	°C
Junction temperature			150	°C
Storage temperature, T_{stg}		–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If A0 is connected to SCL or SDA, the input voltage rating for A0 applies to SCL or SDA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V+	Supply voltage	1.4	3.6	V
T_A	Operating free-air temperature	–40	+125	°C

6.4 Thermal Information

THERMAL METRIC		TMP108 YFF (DSBGA) 6 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	132.7	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	1.7	°C/W
θ_{JB}	Junction-to-board thermal resistance	23	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.6	°C/W
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

6.5 Electrical Characteristics

At T_A = +25°C, and V+ = +1.8 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE INPUT						
	Range		–40		+125	°C
	Accuracy (temperature error)	–20°C to +85°C	–0.75	±0.15	0.75	°C
		–40°C to +125°C	–1	±0.3	1	°C
	Accuracy vs supply		–0.3	±0.03	0.3	°C/V
DIGITAL INPUT/OUTPUT						
V_{IH}	Input logic high level		0.7 (V+)		V+	V
V_{IL}	Input logic low level		–0.5		0.3 (V+)	V
I_{IN}	Input current	0 V < V_{IN} < (V+) +0.3 V			1	µA
V_{OL}	Output logic low level	V+ > 2 V, I_{OUT} = 3 mA			0.4	V
		V+ < 2 V, I_{OUT} = 3 mA			0.2 (V+)	V
	$\overline{\text{ALERT}}$ internal pullup resistor	$\overline{\text{ALERT}}$ to V+	80	100	120	kΩ
	Resolution			12		Bit
	Conversion time	One-Shot mode	21	27	33	ms
	Conversion modes	CR1 = 0, CR0 = 0		0.25		Conv/s
		CR1 = 0, CR0 = 1 (default)		1		Conv/s
		CR1 = 1, CR0 = 0		4		Conv/s
		CR1 = 1, CR0 = 1		16		Conv/s
	Timeout time		21	28	35	ms
POWER SUPPLY						
I_Q	Quiescent current	Serial bus inactive, CR1 = 0, CR0 = 1 (default)		2	3.5	µA
		Serial bus inactive, CR1 = 0, CR0 = 1 (default), –40°C to +125°C			6	µA
		Serial bus active, SCL frequency = 400 kHz, CR1 = 0, CR0 = 1 (default)		12		µA
		Serial bus active, SCL frequency = 3.4 MHz, CR1 = 0, CR0 = 1 (default)		82		µA
I_{SD}	Shutdown current	Serial bus inactive		0.3	1	µA
		Serial bus active, SCL frequency = 400 kHz		10		µA
		Serial bus active, SCL frequency = 3.4 MHz		80		µA

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6.6 Timing Diagrams

The TMP108 is two-wire and SMBus compatible. Figure 1 to Figure 4 describe the various operations on the TMP108. Parameters for Figure 1 are defined in Table 1. Bus definitions are:

Bus Idle: Both SDA and SCL lines remain high.

Start Data Transfer: A change in the state of the SDA line, from high to low, while the SCL line is high defines a start condition. Each data transfer is initiated with a start condition.

Stop Data Transfer: A change in the state of the SDA line from low to high while the SCL line is high defines a stop condition. Each data transfer is terminated with a repeated start or stop condition.

Data Transfer: The number of data bytes transferred between a start and a stop condition is not limited, and is determined by the master device. The receiver acknowledges the transfer of data. It is also possible to use the TMP108 for single-byte updates. To update only the MS byte, terminate communication by issuing a start or stop condition on the bus.

Acknowledge: Each receiving device, when addressed, must generate an acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable low during the high period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a master receives data, the termination of the data transfer can be signaled by the master generating a *not-acknowledge* (1) on the last byte transmitted by the slave.

Table 1. Timing Diagram Definitions

		FAST MODE		HIGH-SPEED MODE		
		MIN	MAX	MIN	MAX	UNIT
$f_{(SCL)}$	SCL operating frequency, V+ ≥ 1.8 V	0.001	0.4	0.001	3.4	MHz
	SCL operating frequency, V+ < 1.8 V	0.001	0.4	0.001	2.5	MHz
$t_{(BUF)}$	Bus free time between stop and start conditions, V+ ≥ 1.8 V	1300		160		ns
	Bus free time between stop and start conditions, V+ < 1.8 V	1300		260		ns
$t_{(HDSTA)}$	Hold time after repeated start condition. After this period, the first clock is generated.	600		160		ns
$t_{(SUSTA)}$	Repeated start condition setup time	600		160		ns
$t_{(SUSTO)}$	Stop condition setup time	600		160		ns
$t_{(HDDAT)}$	Data hold time, V+ ≥ 1.8 V	0	900	0	70	ns
	Data hold time, V+ < 1.8 V	0	900	0	130	ns
$t_{(SUDAT)}$	Data setup time, V+ ≥ 1.8 V	100		10		ns
	Data setup time, V+ < 1.8 V	100		50		ns
$t_{(LOW)}$	SCL clock low period, V+ ≥ 1.8 V	1300		160		ns
	SCL clock low period, V+ < 1.8 V	1300		260		ns
$t_{(HIGH)}$	SCL clock high period	600		60		ns
t_R , t_F - SDA	Data rise/fall time		300		80	ns
t_R , t_F - SCL	Clock rise/fall time		300		40	ns
t_R	Clock/data rise time for SCLK ≤ 100 kHz		1000			ns

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6.6.1 Two-Wire Timing Diagrams

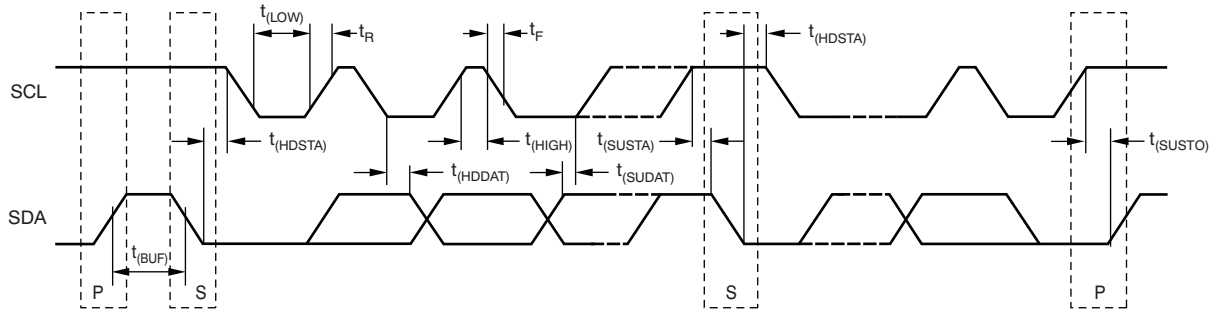
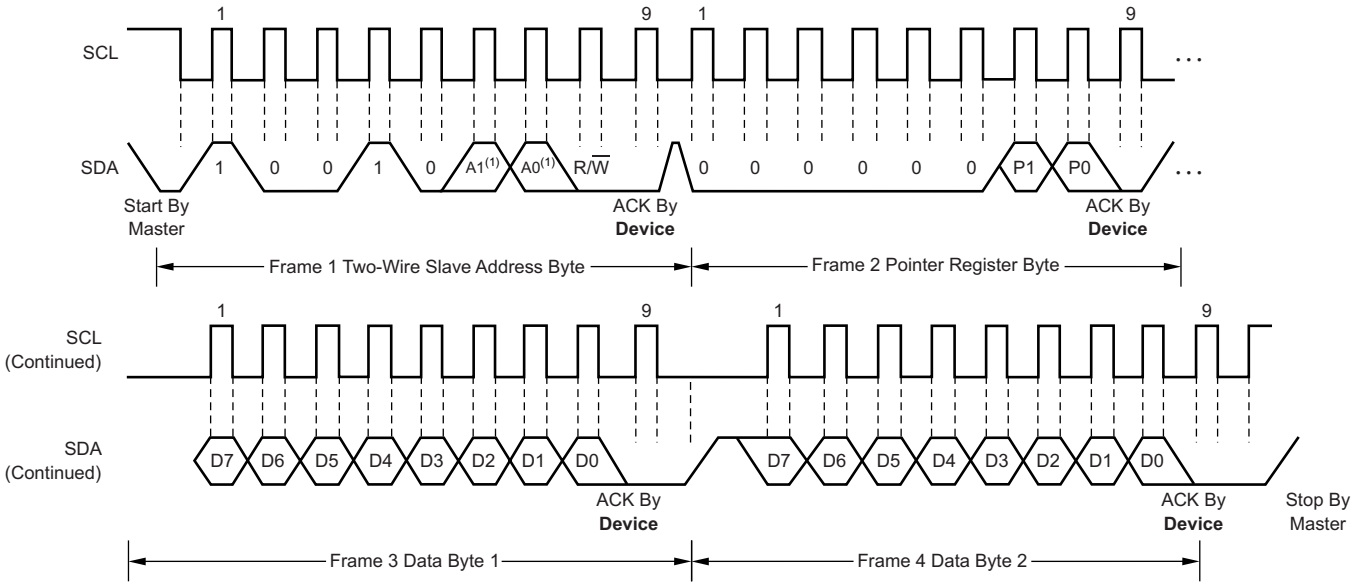


Figure 1. Two-Wire Timing Diagram



(1) The value of A0 and A1 are determined by the A0 pin.

Figure 2. Two-Wire Timing Diagram for Write Word Format

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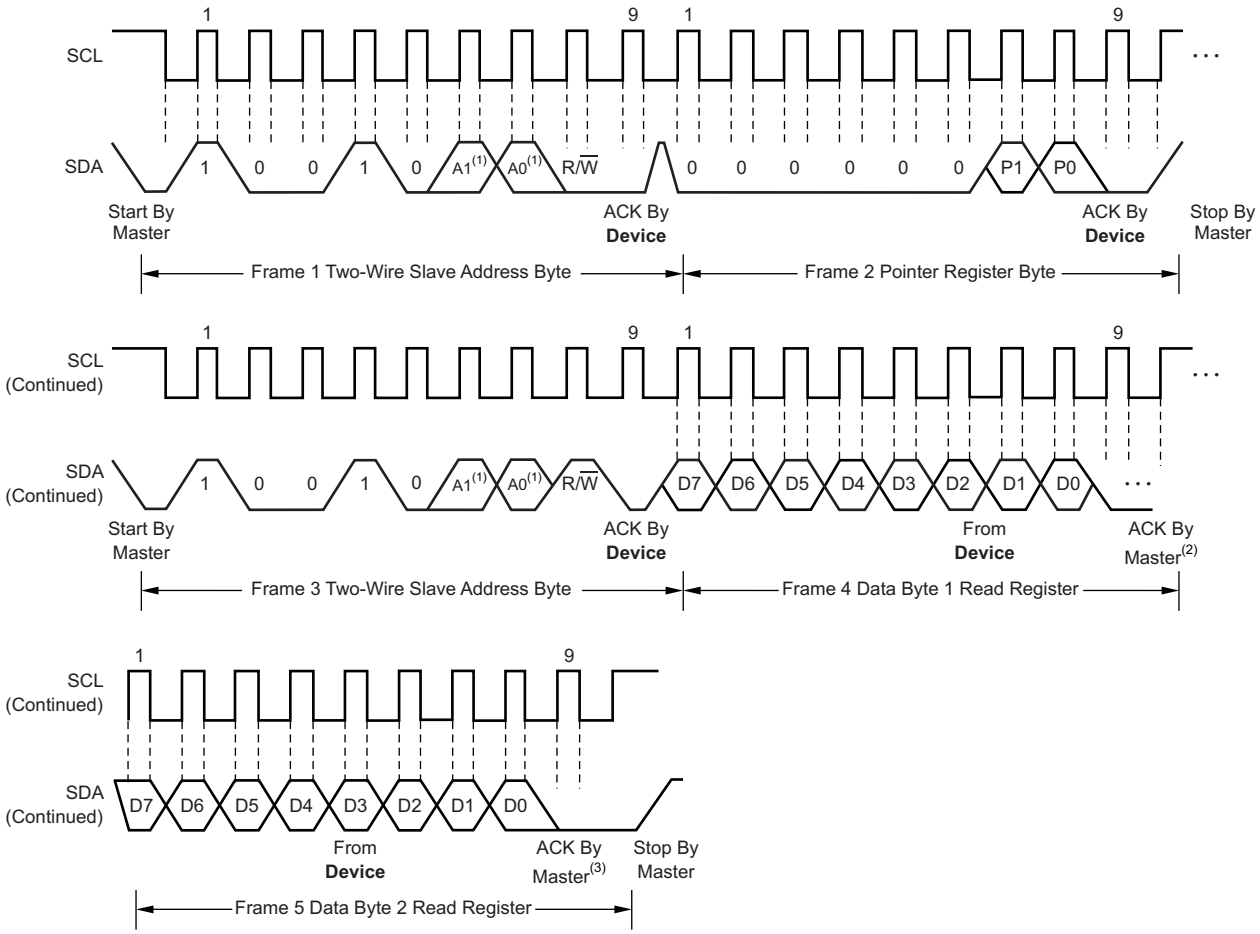
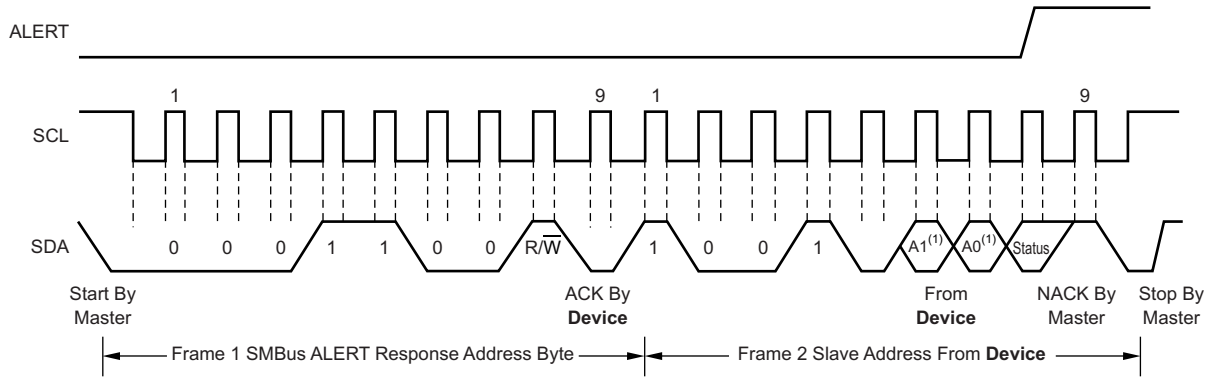


(1) The value of A0 and A1 are determined by the A0 pin.

(2) Master should leave SDA high to terminate a single-byte read operation.

(3) Master should leave SDA high to terminate a two-byte read operation.

Figure 3. Two-Wire Timing Diagram for Read Word Format



(1) The value of A0 and A1 are determined by the A0 pin.

Figure 4. Timing Diagram for SMBus Alert

6.7 Typical Characteristics

At T_A = +25°C and V+ = 1.8 V, unless otherwise noted.

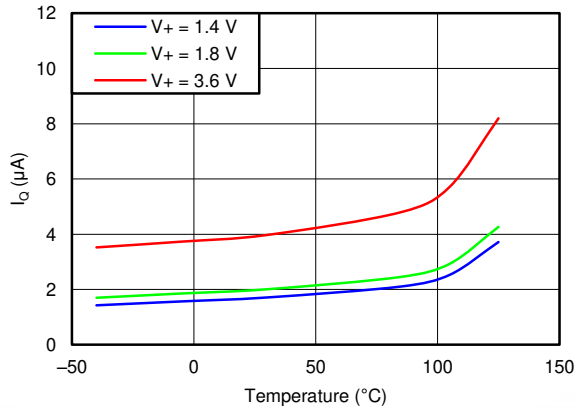


Figure 5. Quiescent Current vs Temperature (1 Conversion per Second)

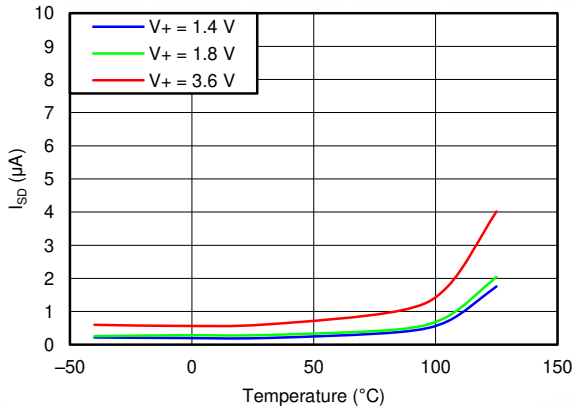


Figure 6. Shutdown Current vs Temperature

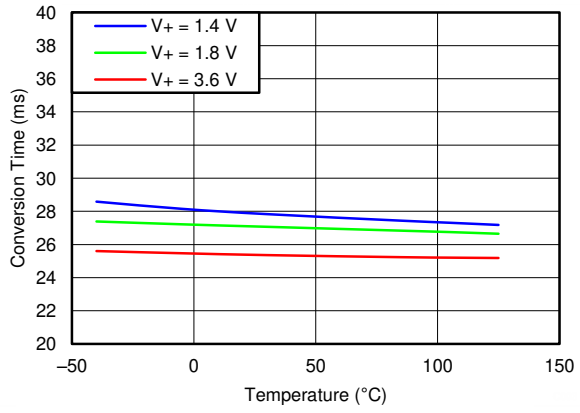


Figure 7. Conversion Time vs Temperature

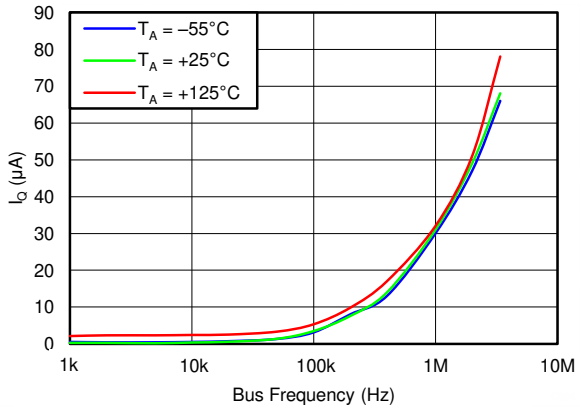


Figure 8. Quiescent Current vs Bus Frequency

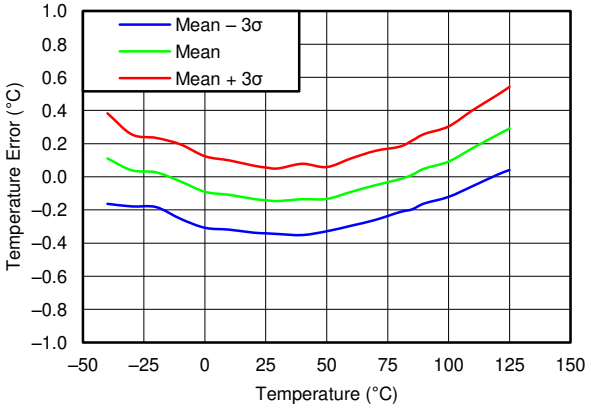


Figure 9. Temperature Error vs Temperature

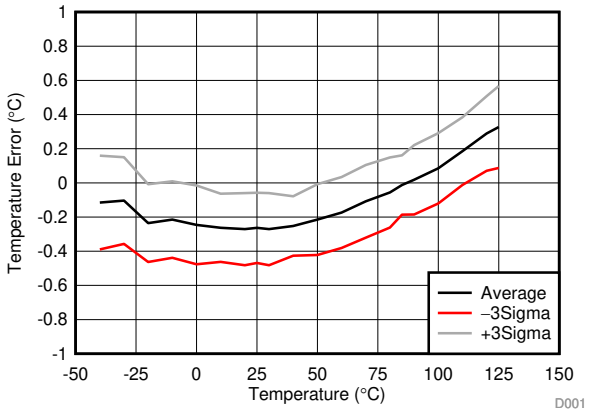


Figure 10. Temperature Error at +25°C

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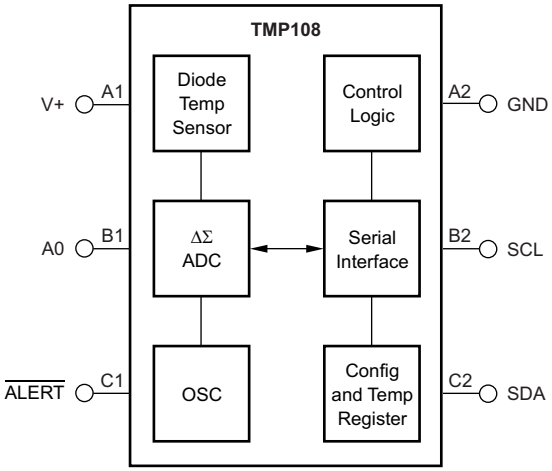
7 Detailed Description

7.1 Overview

The TMP108 is a digital temperature sensor optimal for thermal management and thermal protection applications. The TMP108 is two-wire and SMBus Interface compatible, and is specified over a temperature range of –40°C to +125°C.

The TMP108 temperature sensor is the chip itself. The solder bumps provide the primary thermal path as a result of the lower thermal resistance of metal. The temperature sensor result is equivalent to the local temperature of the printed-circuit board (PCB) on which the sensor is mounted.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Serial Interface

The TMP108 operates as a slave device only on the two-wire bus and SMBus. Connections to the bus are made using the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP108 supports the transmission protocol for both fast (1 kHz to 400 kHz) and high-speed (1 kHz to 3.4 MHz) modes. All data bytes are transmitted MSB first.

7.3.2 Serial Bus Address

To communicate with the TMP108, the master must first communicate with slave devices using a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing either a read or write operation. The TMP108 features an address pin that allows up to four devices to be addressed on a single bus. The TMP108 latches the status of the address pin at the start of a communication. Table 2 describes the pin logic levels and the corresponding address values. Other values for the fixed address bits are available by request.

Table 2. Address Pin and Slave Addresses

DEVICE TWO-WIRE ADDRESS		A0 PIN CONNECTION
TMP108		
1001000		Ground
1001001		V+
1001010		SDA
1001011		SCL

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7.3.3 Bus Overview

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the start and stop conditions.

To address a specific device, initiate a start condition by pulling the data line (SDA) from a high to a low logic level while SCL is high. All slaves on the bus shift in the slave address byte, and the last bit indicates whether a read or write operation follows. During the ninth clock pulse, the slave being addressed responds to the master by generating an acknowledge bit and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit. During data transfer, SDA must remain stable while SCL is high because any change in SDA while SCL is high is interpreted as a start or stop signal.

After all data have been transferred, the master generates a stop condition indicated by pulling SDA from low to high, while SCL is high.

7.3.4 Writing and Reading Operation

Accessing a particular register on the TMP108 is accomplished by writing the appropriate value to the pointer register. The value for the pointer register is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit low. Every write operation to the TMP108 requires a value for the pointer register (see Figure 2).

When reading from the TMP108, the last value stored in the pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the pointer register. This action is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit low, followed by the pointer register byte. No additional data are required. The master can then generate a start condition and send the slave address byte with the R/$\overline{W}$ bit high to initiate the read command. See Figure 3 for details of this sequence. If repeated reads from the same register are desired, it is not necessary to continually send the pointer register bytes because the TMP108 stores the pointer register value until it is changed by the next write operation.

Note that register bytes are sent with the most significant byte first, followed by the least significant byte.

7.3.5 Slave Mode Operations

The TMP108 can operate as a slave receiver or slave transmitter.

7.3.5.1 Slave Receiver Mode:

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit low. The TMP108 then acknowledges reception of a valid address. The next byte transmitted by the master is the pointer register. The TMP108 then acknowledges reception of the pointer register byte. The next byte or bytes are written to the register addressed by the pointer register. The TMP108 acknowledges reception of each data byte. The master can terminate data transfer by generating a start or stop condition.

7.3.5.2 Slave Transmitter Mode:

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the pointer register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master can terminate data transfer by generating a not-acknowledge bit on reception of any data byte, or by generating a start or stop condition.

7.3.6 SMBus Alert Function

The TMP108 supports the SMBus alert function. When the TMP108 operates in interrupt mode (TM = 1), the $\overline{ALERT}$ pin may be connected as an SMBus alert signal. When a master senses that an alert condition is present on the $\overline{ALERT}$ line, the master sends an SMBus alert command (00011001) to the bus. If the $\overline{ALERT}$ pin is active, the device acknowledges the SMBus alert command and responds by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates whether the alert condition is caused by the temperature exceeding T_{HIGH} or falling below T_{LOW}. The LSB is high if the temperature is greater than T_{HIGH}, or low if the temperature is less than T_{LOW}. See Figure 4 for details of this sequence.

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If multiple devices on the bus respond to the SMBus alert command, arbitration during the slave address portion of the SMBus alert command determines which device clears its alert status first. If the TMP108 wins the arbitration, its ALERT pin becomes inactive at the completion of the SMBus alert command. If the TMP108 loses the arbitration, its ALERT pin remains active.

7.3.7 General Call

The TMP108 responds to a two-wire general call address (0000000) if the eighth bit is 0. The device acknowledges the general call address and responds to commands in the second byte. If the second byte is 00000100, the TMP108 latches the status of the address pin, but does not reset. If the second byte is 00000110, the TMP108 internal registers are reset to power-up values. The TMP108 does not support the general address acquire command.

7.3.8 High-Speed (Hs) Mode

In order for the two-wire bus to operate at frequencies above 400 kHz, the master device must issue an SMBus Hs-mode master code (00001xxx) as the first byte after a start condition to switch the bus to high-speed operation. The TMP108 does not acknowledge this byte, but does switch its input filters on SDA and SCL and its output filters on SDA to operate in Hs-mode, allowing transfers at up to 3.4 MHz. After the Hs-mode master code has been issued, the master transmits a two-wire slave address to initiate a data-transfer operation. The bus continues to operate in Hs-mode until a stop condition occurs on the bus. Upon receiving the stop condition, the TMP108 switches the input and output filters back to fast-mode operation.

7.3.9 Timeout Function

The TMP108 resets the serial interface if SCL or SDA are held low for 28 ms (typical) between a start and stop condition. If the TMP108 is pulled low, it releases the bus and then waits for a start condition. To avoid activating the timeout function, it is necessary to maintain a communication speed of at least 1 kHz for the SCL operating frequency.

7.4 Device Functional Modes

The mode bits, M1 and M0, can be set to three different modes: shutdown, one-shot, or continuous conversion.

7.4.1 Shutdown Mode (M1 = 0, M0 = 0)

Shutdown mode saves power by shutting down all device circuitry other than the serial interface, thus reducing current consumption to typically less than 0.5 μA. Shutdown mode is enabled when M1 and M0 = 00. The device shuts down when current conversion is completed.

7.4.2 One-Shot Mode (M1 = 0, M0 = 1)

The TMP108 features a *one-shot* temperature measurement mode. When the device is in shutdown mode, writing a '01' to the M1 and M0 bits starts a single temperature conversion. During the conversion, the M1 and M0 bits reads 01. The device returns to the shutdown state at the completion of the single conversion. After the conversion, the M1 and M0 bits read 00. This feature is useful for reducing the power consumption of the TMP108 when continuous temperature monitoring is not required.

As a result of the short conversion time, the TMP108 can achieve a higher conversion rate. A single conversion typically takes 27 ms and a read can take place in less than 20 μs. However, when using one-shot mode, 30 or more conversions per second are possible.

7.4.3 Continuous Conversion Mode (M1 = 1)

When the TMP108 is in continuous conversion mode (M1 = 1), a single conversion is performed at a rate determined by the conversion rate bits (CR1 and CR0 in the configuration register). The TMP108 performs a single conversion, and then goes in standby and waits for the appropriate delay set by the CR1 and CR0 bits. See Table 10 for CR1 and CR0 settings.

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7.5 Programming

7.5.1 Pointer Register

Figure 11 shows the internal register structure of the TMP108. Use the 8-bit pointer register to address a given data register. The pointer register uses the two LSBs (see Table 12) to identify which of the data registers respond to a read or write command. Table 3 identifies the bits of the pointer register byte. Table 4 describes the pointer address of the registers available in the TMP108. The power-up reset value of the P1 and P0 bits is 00.

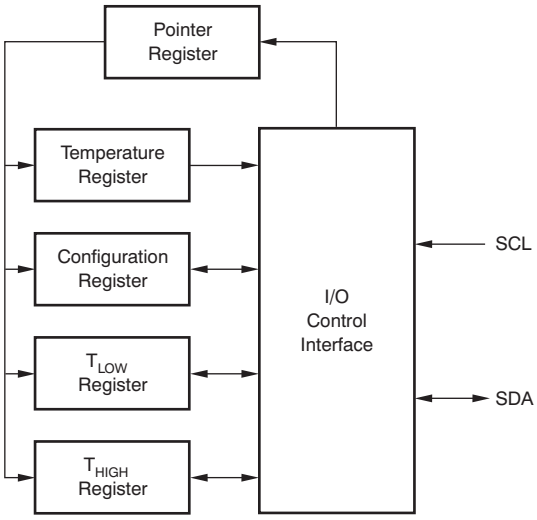

Figure 11. Internal Register Structure

Table 3. Pointer Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

Table 4. Pointer Addresses

P1	P0	REGISTER
0	0	Temperature register (read only, default)
0	1	Configuration register (read/write)
1	0	T_{LOW} register (read/write)
1	1	T_{HIGH} register (read/write)

7.5.2 Temperature Register

The temperature register is configured as a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, as shown in Table 5 and Table 6. Note that byte 1 is the most significant byte, followed by byte 2, the least significant byte. The first 12 bits are used to indicate temperature. There is no requirement to read the least significant byte if that information is not needed (for example, for resolution lower than 1°C). Table 7 summarizes the temperature data format. One LSB equals 0.0625°C. Negative numbers are represented in binary twos complement format. Following power-up or reset, the temperature register reads 0°C until the first conversion is complete. The unused bits in the temperature register always read 0.

Table 5. Byte 1 of Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T11	T10	T9	T8	T7	T6	T5	T4

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Table 6. Byte 2 of Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T3	T2	T1	T0	0	0	0	0

Table 7. Temperature Data Format(1)

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	HEX
128	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
–0.25	1111 1111 1100	FFC
–25	1110 0111 0000	E70
–55	1100 1001 0000	C90

(1) The temperature sensor ADC resolution is 0.0625°C/count.

Table 7 does not supply a full list of all temperatures. Use the following rules to obtain the digital data format for a given temperature.

To convert positive temperatures to a digital data format:

Divide the temperature by the resolution. Then, convert the result to binary code with a 12-bit, left-justified format, and MSB = 0 to denote a positive sign.

Example: (+50°C)/(0.0625°C/count) = 800 = 320h = 0011 0010 0000

To convert negative temperatures to a digital data format:

Divide the absolute value of the temperature by the resolution, and convert the result to binary code with a 12-bit, left-justified format. Then, generate the twos complement of the result by complementing the binary number and adding one. Denote a negative number with MSB = 1.

Example: (|–25°C|)/(0.0625°C/count) = 400 = 190h = 0001 1001 0000

Twos complement format: 1110 0110 1111 + 1 = 1110 0111 0000

7.5.3 Configuration Register

The configuration register is a 16-bit read and write register used to store bits that control the operational modes of the temperature sensor. Read and write operations are performed MSB first. The format and power-up (reset) default value of the configuration register is shown in Table 8, followed by an explanation of the register bits. Other options for the default values are available by request.

Table 8. Configuration and Power-Up/Reset Format

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	ID	CR1	CR0	FH	FL	TM	M1	M0
	0	0	1	0	0	0	1	0
2	POL	0	HYS1	HYS0	0	0	0	0
	0	0	0	1	0	0	0	0

7.5.3.1 Hysteresis Control (HYS1 and HYS0)

When operating in comparator mode, the hysteresis control bits (HYS1 and HYS0) configure the hysteresis for the limit comparison of the TMP108 to 0°C, 1°C, 2°C, or 4°C. The default hysteresis is 1°C. Table 9 shows the settings for HYS1 and HYS0.

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Table 9. Hysteresis Settings

HYS1	HYS0	HYSTERESIS
0	0	0°C
0	1	1°C (default)
1	0	2°C
1	1	4°C

7.5.3.2 Polarity (POL)

The polarity of the $\overline{\text{ALERT}}$ pin can be programmed using the POL bit. If POL = 0 (default), the $\overline{\text{ALERT}}$ is active low. For POL = 1, the $\overline{\text{ALERT}}$ pin is active high, and the state of the $\overline{\text{ALERT}}$ pin is inverted.

7.5.3.3 Thermostat Mode (TM)

The thermostat mode bit indicates to the device whether to operate in comparator mode (TM = 0, default) or interrupt mode (TM = 1). For more information on comparator and interrupt modes, see the *High- and Low-Limit Registers* section.

7.5.3.4 Temperature Watchdog Flags (FL and FH)

The TMP108 uses temperature watchdog flags in the configuration register that indicate the result of comparing the device temperature at the end of every conversion to the values stored in the temperature limit registers (T_{HIGH} and T_{LOW}). If the temperature of the TMP108 exceeds the value in the T_{HIGH} register, then the flag-high bit (FH) in the configuration register is set to 1. If the temperature falls below the value in the T_{LOW} register, then the flag-low bit (FL) is set to 1. If both flag bits remain 0, then the temperature is within the temperature range set by the temperature limit registers. In interrupt mode, when any of the flags is set by an under- or overtemperature event, the SMBus ALERT Response only clears the pin and not the flags. Reading the configuration register clears both the flags and the pin.

7.5.3.5 Conversion Rate

The conversion rate bits, CR1 and CR0, configure the TMP108 for conversion rates of 0.25 Hz, 1 Hz, 4 Hz, or 16 Hz. The default rate is 1 Hz. The TMP108 has a typical conversion time of 27 ms. To achieve different conversion rates, the TMP108 makes a conversion, and then powers down and waits for the appropriate delay set by CR1 and CR0. Table 10 shows the settings for CR1 and CR0.

Table 10. Conversion Rate Settings

CR1	CR0	CONVERSION RATE	I_Q (TYP)
0	0	0.25 Hz	1 µA
0	1	1 Hz (default)	2 µA
1	0	4 Hz	5 µA
1	1	16 Hz	18 µA

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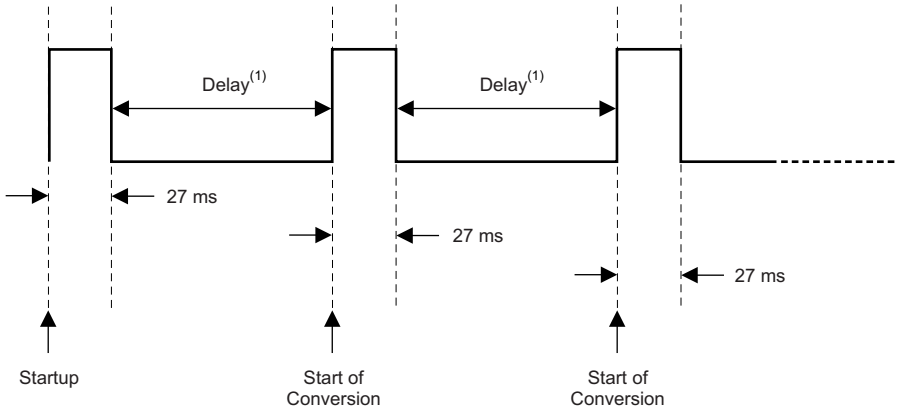
After power-up or a general-call reset, the TMP108 immediately starts a conversion, as shown in Figure 12. The first result is available after 27 ms (typical). The active quiescent current during conversion is 40 μA (typical at +25°C). The quiescent current during delay is 0.7 μA (typical at +25°C).



(1) Delay is set by the CR1 and CR0 bits in the configuration register.

Figure 12. Conversion Start

7.5.4 High- and Low-Limit Registers

In comparator mode (TM = 0), the $\overline{\text{ALERT}}$ pin becomes active when the temperature exceeds the value in the T_{HIGH} register or drops below the value in the T_{LOW} register. The $\overline{\text{ALERT}}$ pin remains active until the temperature returns to a value that is within the range set by:

(T_{LOW} + HYS) and (T_{HIGH} – HYS)

where

- HYS is the hysteresis set by the hysteresis control bits (HYS1 and HYS0). (1)

In interrupt mode (TM = 1), the $\overline{\text{ALERT}}$ pin becomes active when the temperature exceeds the value in the T_{HIGH} register or drops below the value in the T_{LOW} register, and remains active until a read operation of the configuration register occurs (also clears the values latched in the watchdog flags, FL and FH), or the device successfully responds to the SMBus alert response address. The $\overline{\text{ALERT}}$ pin is also cleared by resetting the device with the general call reset command.

Both operational modes are represented in Figure 13 and Figure 14.

Table 11 and Table 12 describe the format for the T_{HIGH} and T_{LOW} registers. Note that the most significant byte is sent first, followed by the least significant byte. Power-up (reset) default values are T_{HIGH} = +127.9375°C (0x7FF8) and T_{LOW} = –128°C (0x8000). These values ensure that upon power-up, the limit window is set to maximum, and the $\overline{\text{ALERT}}$ pin does not become active until the desired limit values are programmed in the registers. Other default values for the temperature limits are available by request. The format of the data for T_{HIGH} and T_{LOW} is the same as for the temperature register.

Table 11. Bytes 1 and 2 of T_{HIGH} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	H11	H10	H9	H8	H7	H6	H5	H4
BYTE	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
2	H3	H2	H1	H0	0	0	0	0

Table 12. Bytes 1 and 2 of T_{LOW} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	L11	L10	L9	L8	L7	L6	L5	L4
BYTE	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
2	L3	L2	L1	L0	0	0	0	0

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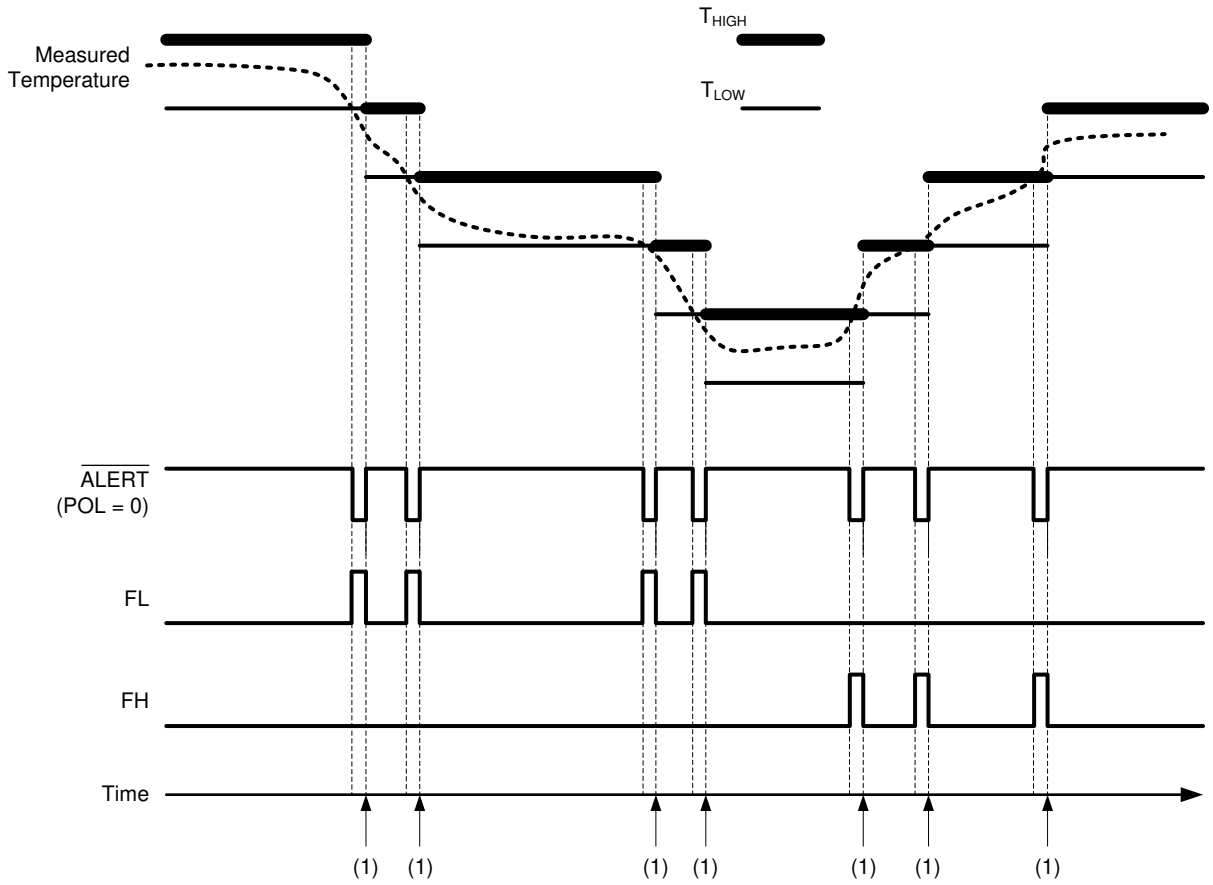

(1) Update T_{HIGH} and T_{LOW} limit. Read the configuration register to clear the flags and the $\overline{ALERT}$ pin.

Figure 13. Interrupt Mode

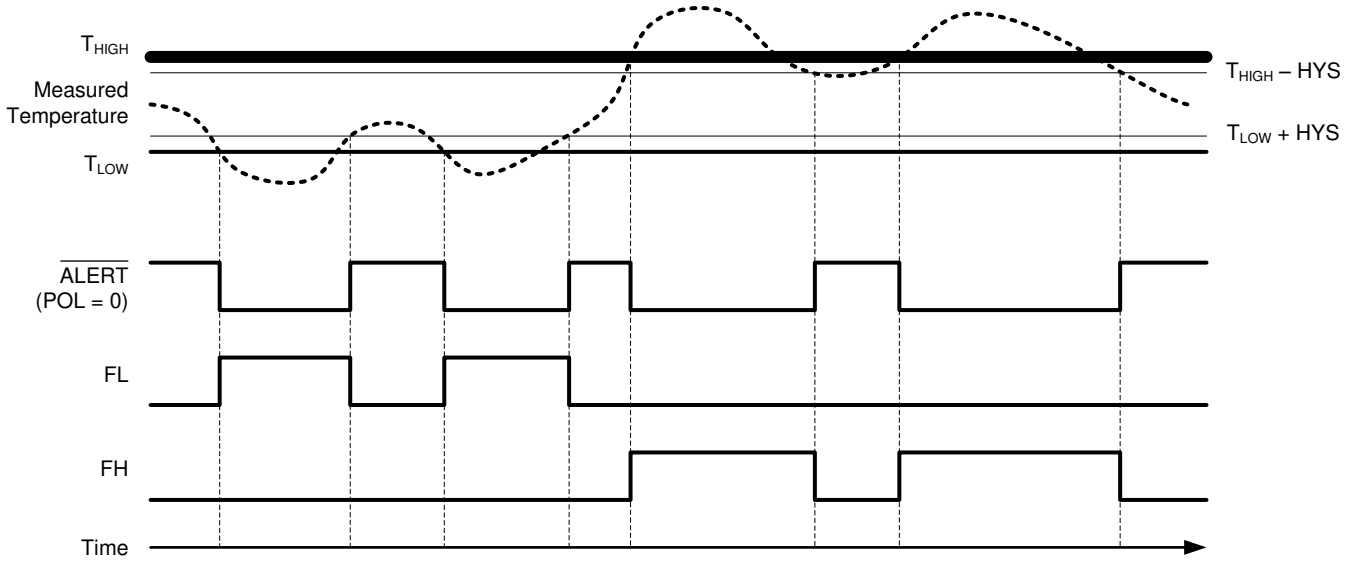

Figure 14. Comparator Mode

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMP108 is used to measure the temperature of the board location where the device is mounted. The programmable address options allow up to four locations on the board to be monitored with a single serial bus.

8.2 Typical Application

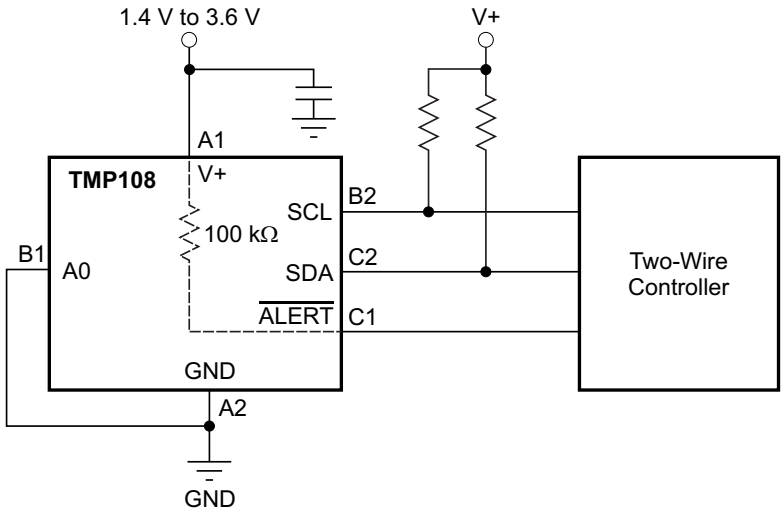

Figure 15. Typical Application Circuit

8.2.1 Design Requirements

The TMP108 only requires pullup resistors on SCL and SDA, but TI also recommends to use a 0.01-μF bypass capacitor as shown in Figure 15. There is an internal 100-kΩ pullup resistor connected to supply on the ALERT pin. If required, use an external resistor of smaller value on the ALERT pin for a stronger pullup to V+. The SCL and SDA lines can be pulled up to a supply that is equal to or higher than V+ through the pullup resistors. To configure one of four different addresses on the bus, connect A0 to either V+, GND, SCL, or SDA. If A0 is connected to SCL or SDA, make their pullup supply equal to V+.

8.2.2 Detailed Design Procedure

The TMP108 devices must be placed in close proximity to the heat source that must be monitored, with a proper layout for good thermal coupling. This placement ensures that temperature changes are captured within the shortest possible time interval. To maintain accuracy in applications that require air or surface temperature measurement, take care to isolate the package and leads from PCB heat sources.

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Typical Application (continued)

8.2.3 Application Curves

Figure 16 shows the step response of the TMP108 device to a submersion in an oil bath of 100°C from room temperature (25°C.) The time constant, or the time for the output to reach 63% of the input step, is about 1 second. Figure 17 shows the step response of the TMP108 device to an insertion in an air chamber of 100°C from room temperature (25°C.) The time-constant is 68 seconds. The time-constant result depends on the printed-circuit board (PCB) that the TMP108 device is mounted. For this test, the PCB is 0.5 in × 0.5 in, and the PCB thickness is 32 mils.

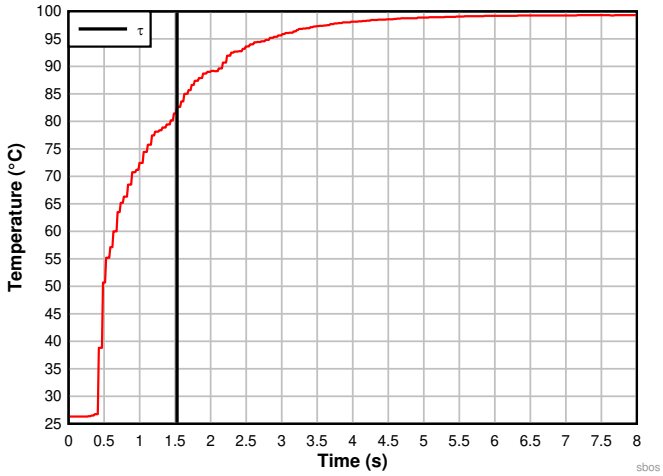

Figure 16. Moving Oil Thermal Response

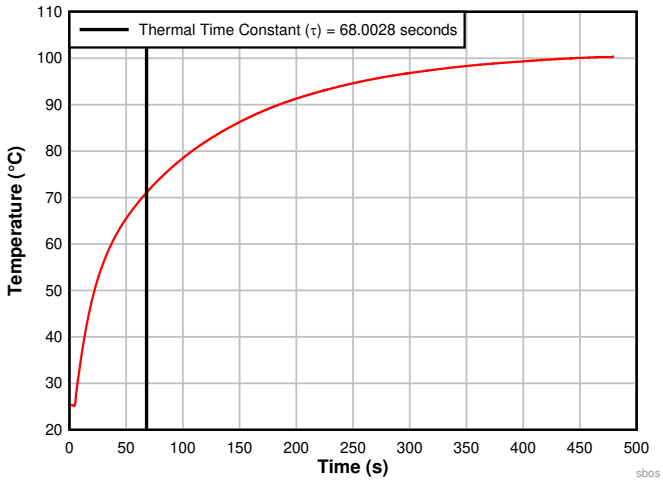

Figure 17. Still Air Thermal Response

9 Power Supply Recommendations

The TMP108 operates on a power supply range from 1.4 V to 3.6 V. A power-supply bypass capacitor is required, which must be placed as close to the supply and ground pins of the device as possible. A typical supply bypass capacitor is 100 nF.

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10 Layout

10.1 Layout Guidelines

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.01 μF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. Pull up the open-drain output pins (SDA , SCL and ALERT) through 5-kΩ pullup resistors.

10.2 Layout Example

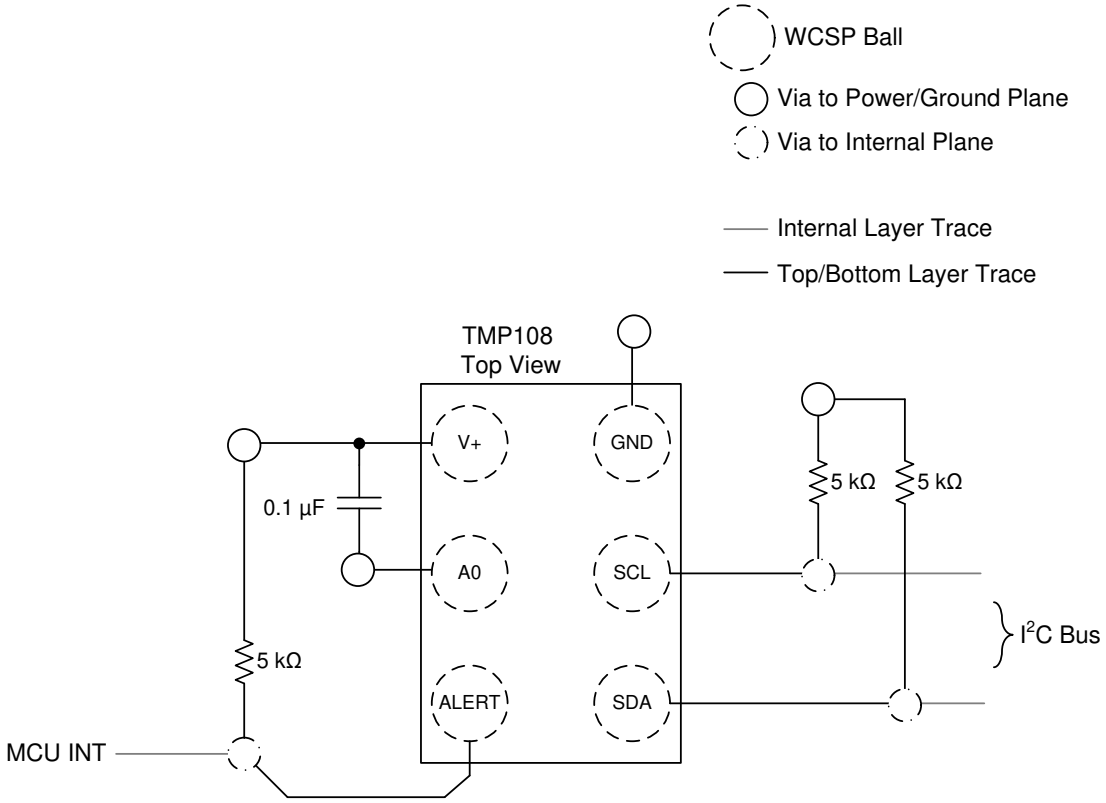

Figure 18. TMP108 Layout

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMP108AIYFFR	Active	Production	DSBGA (YFF) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T8
TMP108AIYFFR.B	Active	Production	DSBGA (YFF) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T8

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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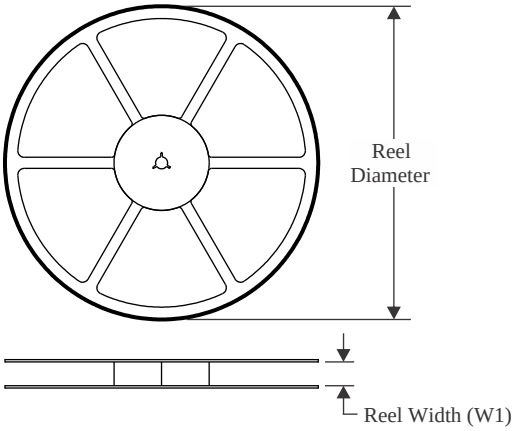
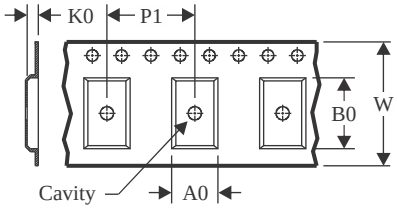
TAPE AND REEL INFORMATION

REEL DIMENSIONS

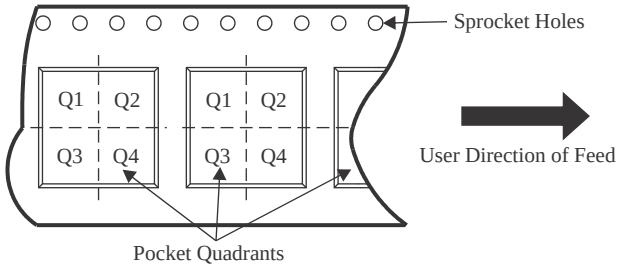


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

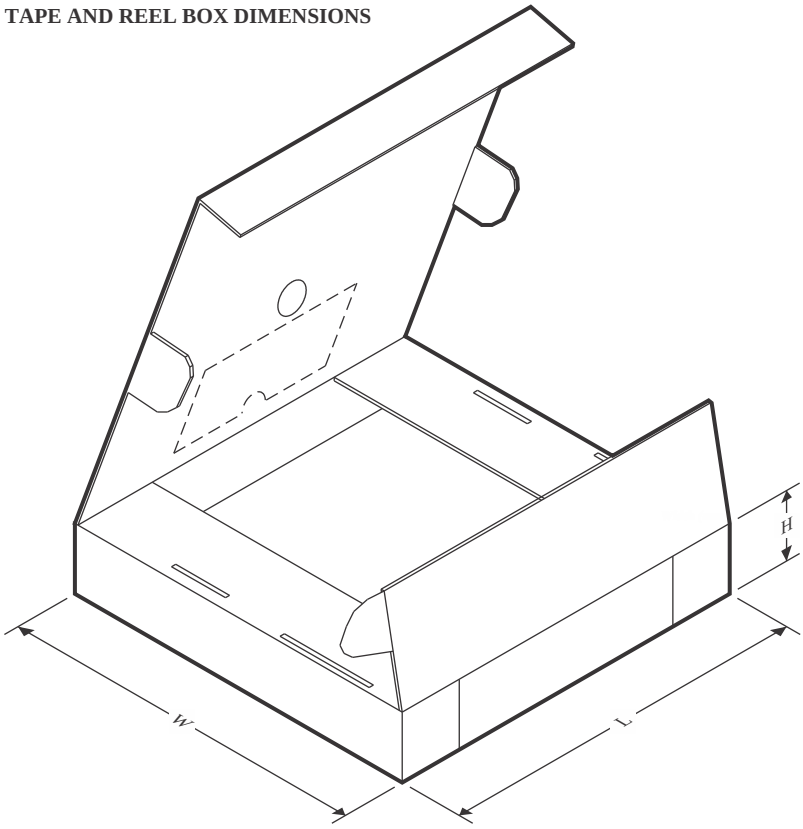
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP108AIYFFR	DSBGA	YFF	6	3000	180.0	8.4	0.89	1.29	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

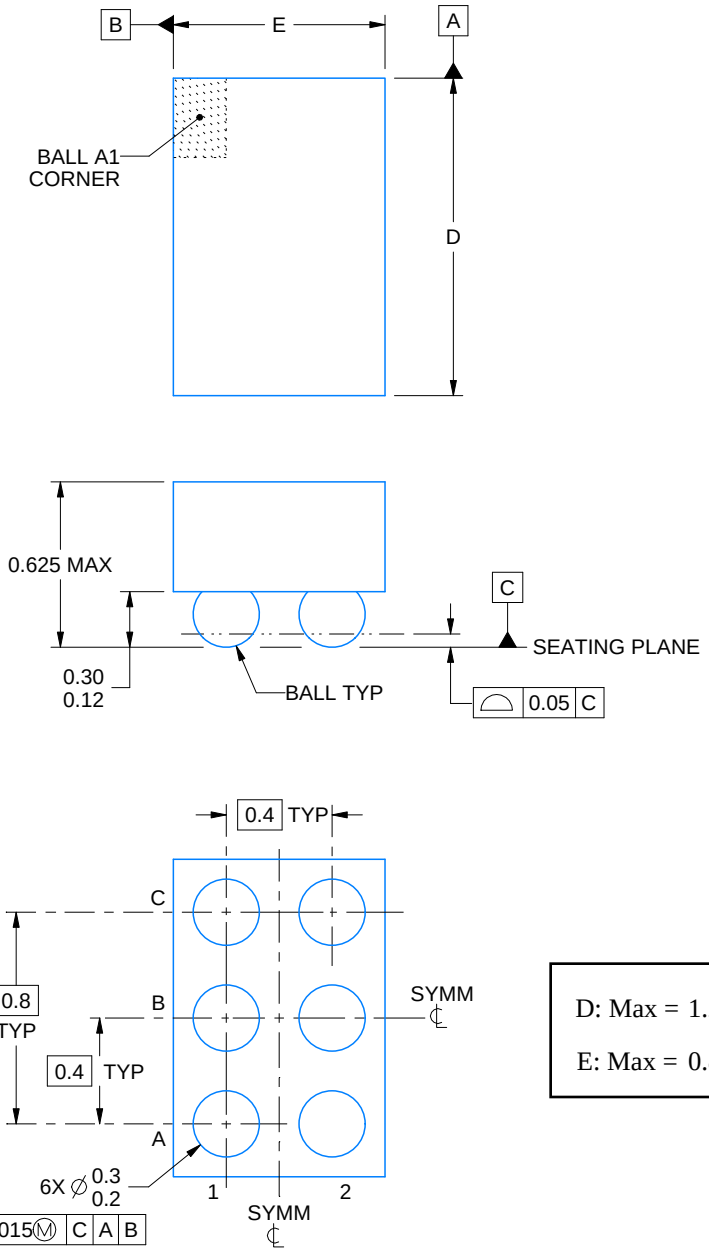
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP108AIYFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



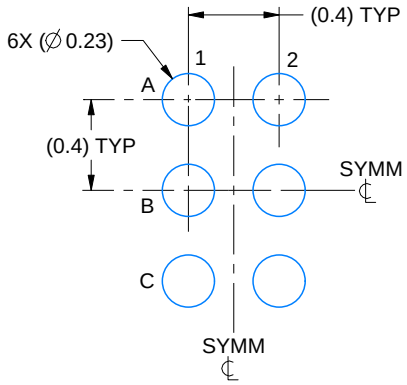
D: Max = 1.216 mm, Min =1.156 mm

E: Max = 0.816 mm, Min =0.756 mm

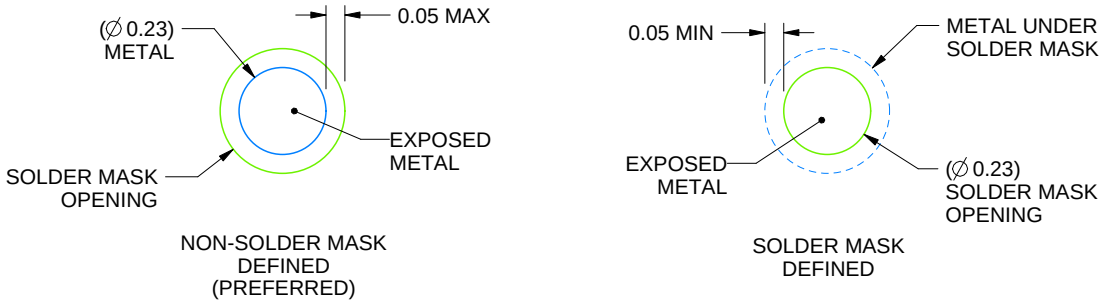
4223785/A 06/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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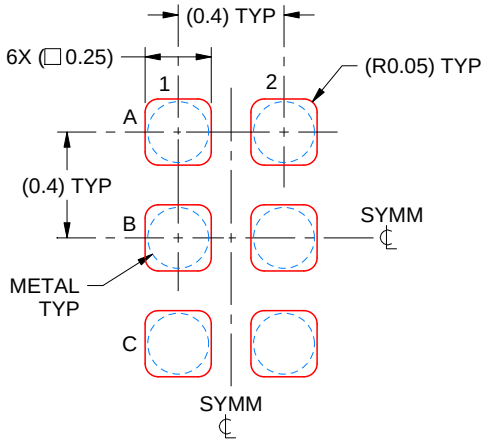
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:35X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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