TMP411-Q1 ±1°C and TMP411D-Q1 ±0.8°C Remote and Local Temperature Sensors with N-Factor and Series Resistance Correction

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- **TMP411-Q1**:
  - ±1°C local (on-chip) temp accuracy
  - ±1°C remote junction temp accuracy
  - Supply range: 2.7V to 5.5V
  - Available in VSSOP 8-pin package
- **TMP411D-Q1**:
  - ±0.8°C local (on-chip) temp accuracy
  - ±0.8°C remote junction temp accuracy
  - Supply range: 1.62V to 5.5V
  - Available in SOT-23 8-pin package
- I^2C interface (SMBus compatible)
  - Programmable resolution: 9 to 12 bits
  - Multiple interface addresses
- Integrated calibration/protection features:
  - Programmable non-ideality factor
  - Series resistance cancellation
  - Remote BJT/diode fault detection
  - Alert function
    - $\overline{\text{ALERT}}$ / $\overline{\text{THERM2}}$ pin configuration
  - Programmable threshold limits
  - Minimum and maximum temperature monitors

2 Applications

- Advanced driver assistance systems (ADAS)
- Body electronics and lighting
- Infotainment and cluster
  - Head unit and digital cockpit
  - Automotive display
- Hybrid, electric, and powertrain systems
- Processor and FPGA temperature monitoring

3 Description

The TMP411-Q1/TMP411D-Q1 is a remote temperature sensor monitor with a built-in local temperature sensor. The remote temperature-sensor diode-connected transistors are typically low-cost, NPN- or PNP-type transistors or diodes that are an integral part of microcontrollers, microprocessors, or FPGAs.

Remote accuracy is ±1°C (TMP411-Q1) or ±0.8°C (TMP411D-Q1) for multiple IC manufacturers, with no calibration needed. The two-wire serial interface accepts SMBus write byte, read byte, send byte, and receive byte commands to program the alarm thresholds and to read temperature data.

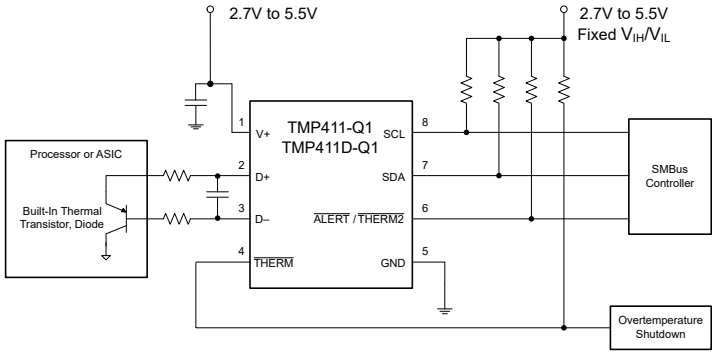
Features included in the TMP411-Q1/TMP411D-Q1 are: series resistance cancellation, programmable non-ideality factor, programmable resolution, programmable threshold limits, minimum and maximum temperature monitors, wide remote temperature measurement range (up to 150°C), diode fault detection, and temperature alert function.

The TMP411-Q1 is available in a VSSOP-8 package, and the TMP411D-Q1 is available in an SOT23-8 package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMP411-Q1	DGK (VSSOP, 8)	3.00mm × 4.90mm
TMP411D-Q1	DDF (SOT23, 8)	2.9mm × 2.8mm

(1) For all available packages, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Device Comparison

Table 4-1. Device Comparison

FEATURE	TMP411-Q1	TMP411D-Q1 (2) (4)	TMP421-Q1	TMP451-Q1 (1) (4)
V_{DD} (V)	2.7 to 5.5	1.62 to 5.5	2.7 to 5.5	1.7 to 3.6
Local Temperature Accuracy (°C)				
–40°C (max)	±2.5 (2)	±1	±2.5 (2)	±2
-25°C (max)	±2.5 (2)	±0.8	±2.5 (2)	±2
-10°C (max)	±2.5 (2)	±0.8	±2.5 (2)	±2
0°C (max)	±2.5 (2)	±0.8	±2.5 (2)	±1
15°C (max)	±1 (1)	±0.8	±1.5 (1)	±1
70°C (max)	±1 (1)	±0.8	±1.5 (1)	±1
85°C (max)	±1 (1)	±0.8	±1.5 (1)	±2
100°C (max)	±2.5 (2)	±1	±2.5 (2)	±2
125°C (max)	±2.5 (2)	±1	±2.5 (2)	±2
Remote Temperature Accuracy (°C)				
–40°C (max)	±3 (1) (3)	±1	±3 (1) (3)	±2
-25°C (max)	±3 (1) (3)	±0.8	±3 (1) (3)	±2
-10°C (max)	±3 (1) (3)	±0.8	±3 (1) (3)	±2
0°C (max)	±3 (1) (3)	±0.8	±3 (1) (3)	±1
15°C (max)	±1 (1) (3)	±0.8	±1 (1) (3)	±1
70°C (max)	±1 (1) (3)	±0.8	±1 (1) (3)	±1
75°C (max)	±1 (1) (3)	±0.8	±1 (1) (3)	±2
85°C (max)	±3 (1) (3)	±0.8	±1 (1) (3)	±2
100°C (max)	±3 (1) (3)	±1	±3 (1) (3)	±2
105°C (max)	±5 (1) (3)	±1	±5 (2), (3)	±4
125°C (max)	±5 (1) (3)	±1.25	±5 (2) (3)	±4
Digital Input/Output				
Resolution (Bit) (Local and Remote)	L = 9 to 12 R = 12	L = 9 to 12 R = 12	L = 12 R = 12	L = 12 R = 12
V_{IH}/V_{IL}	2.1 / 0.8	2.1 / 0.8 and 70% / 30% V_{DD}	2.1 / 0.8	1.4 / 0.45
Current Consumption and Conversion Time (Typ: V_{DD}=3.3V and 25°C)				
T_{Conv} (ms) (per channel)	115÷2	17.7	115	31÷2
I_{AVG} at 0.0625Hz (µA)	28	1.5	32	27
I_{SB} (µA)	7.5	1	—	—
I_{SD} (µA)	3	0.6	3	3
Features: R_{Series}Cancellation, N-Factor Correction, Diode Fault Detection				
I^2C Addresses	4 orderables	4 orderables	9 (A1/A0 pins)	3 orderables
Packaging Dimension				
Dimensions [mm × mm × mm]	**VSSOP** (8-pin) 3 × 4.9 × 1.1	**SOT-23** (8-pin) 2.9 × 2.8 × 1.1	**SOT-23** (8-pin) 2.9 × 2.8 × 1.1	**WSON** (8-pin) 2 × 2 × 0.8 **WSON (WF)** (8-pin) 2.5 × 2 × 0.8

(1) Temperature accuracy is specified over V_{DD}= 3.3V.
(2) Temperature accuracy is specified over the whole power supply.
(3) Remote temperature accuracy is specified over T_{DIODE} = –40°C to 150°C.
(4) Remote temperature accuracy is specified over T_{DIODE} = –55°C to 150°C.

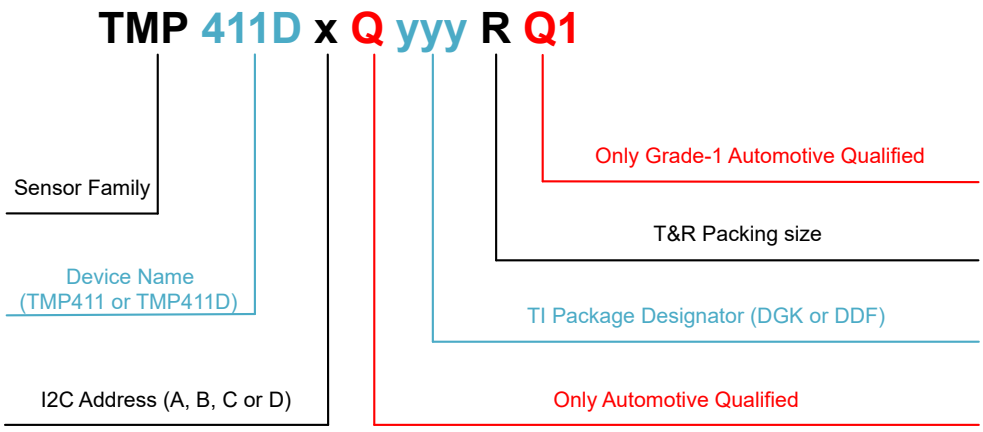


Figure 4-1. TMP411-Q1 and TMP411D-Q1 Device Nomenclature

Table 4-2. TMP411-Q1 and TMP411D-Q1 Device Nomenclature Description

FIELD DESCRIPTION	FIELD DETAIL
Sensor Family	TMP: Temperature Sensors
Device Name	411 or 411D
I^2C Address	• TMP411**A**-Q1/ TMP411D**A**-Q1 - 4Ch/ 1001100'b - 85°C default local/remote high temperature limit • TMP411**B**-Q1/ TMP411D**B**-Q1 - 4Dh/ 1001101'b - 85°C default local/remote high temperature limit • TMP411**C**-Q1/ TMP411D**C**-Q1 - 4Eh/ 1001110'b - 85°C default local/remote high temperature limit • TMP411**D**-Q1/ TMP411D**D**-Q1 - 4Ch/ 1001100'b - 110°C default local/remote high temperature limit
Automotive qualified	Applies to only automotive-qualified devices
TI Package Designator	**TMP411-Q1**: • DGK, VSSOP package, 1.1mm (max) height
	TMP411D-Q1: • DDF, SOT23 package, 1.1mm (max) height
T and R Packing Size	Large T and R, SPQ (**TMP411-Q1**) = 2,500 units and SPQ (**TMP411D-Q1**) = 3,000 units
Automotive grade-1 qualified	AEC-Q100 Qualified for automotive applications

Table 4-3. TMP411-Q1 and TMP411D-Q1 devices Device Nomenclature Detail

PRODUCT	OUT
TMP411**x**Q**yyy**RQ1	**x** indicates that the device has **A**, **B**, **C,** or **D** variant. These devices can ship with the legacy chip (CSO: DM5) or the new chip (CSO: RFB). The reel packaging label provides date code information to distinguish which chip is being used. Device performance for new and legacy chips is denoted throughout the document. **yyy** indicates that the package type of the device is **DGK** (VSSOP 8-pin).
TMP411D**x**Q**yyy**RQ1	**x** indicates that the device has **A**, **B**, **C**, or **D** variant. TMP411D-Q1 has only CSO: RFB. **yyy** indicates that the package type of the device is **DDF** (SOT23 8-pin).

5 Pin Configuration and Functions

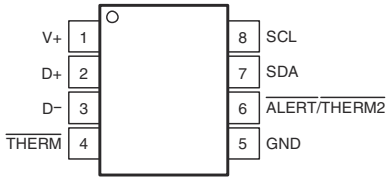


Figure 5-1. DGK and DDF Packages
8-Pin VSSOP and SOT-23
(TOP VIEW)

Pin Functions

PIN	NAME	Type[1]	DESCRIPTION
1	V+	P	Positive supply (2.7V to 5.5V for **TMP411-Q1**) and (1.62V to 5.5V for **TMP411D-Q1**)
2	D+	Analog I	Positive connection to the remote temperature sensor
3	D−	Analog I	Negative connection to the remote temperature sensor
4	$\overline{\text{THERM}}$	Digital O	Thermal flag, active-low, open-drain; requires pullup resistor to V+
5	GND	G	Ground
6	$\overline{\text{ALERT}}$/ $\overline{\text{THERM2}}$	Digital O	Alert (reconfigurable as second thermal flag), active-low, open-drain; requires pullup resistor to V+
7	SDA	Digital I/O	Serial data line for SMBus, open-drain; requires pullup resistor to V+
8	SCL	Digital I	Serial clock line for SMBus, open-drain; requires pullup resistor to V+

(1) O = Output, I = Input; I/O = Input or Output; G = Ground; P = Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Input voltage	Pins 2, 3, 4 only	TMP411-Q1 (Legacy chip)	–0.5	(V+) + 0.5	V
	Pins 6, 7, 8 only		–0.5	7	
	Pins 2, 3 only	TMP411-Q1 (New chip) TMP411D-Q1	–0.5	2	V
	Pins 4, 6, 7, 8 only		–0.5	6	
Input current				10	mA
Power supply, V+		TMP411-Q1 (Legacy chip)		7	V
		TMP411-Q1 (New chip) TMP411D-Q1		6	
Operating temperature range			–55	127	°C
Junction temperature, $T_{J(max)}$				150	°C
Storage temperature, T_{stg}			–60	130	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	TMP411-Q1 (Legacy chip)	±2000	V
			TMP411-Q1 (New chip) TMP411D-Q1	±3000	
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	TMP411-Q1 (Legacy chip)	±750	
			TMP411-Q1 (New chip) TMP411D-Q1	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V+	Supply voltage, TMP411-Q1	2.7	3.3	5.5	V
	Supply voltage, TMP411D-Q1	1.62	3.3	5.5	
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMP411-Q1		TMP411D-Q1	UNIT
		DGK (VSSOP) Legacy chip	DGK (VSSOP) New chip	DDF (SOT-23)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	161.5	182.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	N/A	71.1	98.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	96.6	99.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	N/A	9.2	10.4	°C/W

6.4 Thermal Information (continued)

THERMAL METRIC[1]		TMP411-Q1		TMP411D-Q1	UNIT
		DGK (VSSOP) Legacy chip	DGK (VSSOP) New chip	DDF (SOT-23)	
		8 PINS	8 PINS	8 PINS	
ψ_{JB}	Junction-to-board characterization parameter	N/A	95.0	98.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics (TMP411-Q1)

At T_A = –40°C to +125°C and V+ = 2.7V to 5.5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
TEMPERATURE ERROR								
$T_{ERROR(LOCAL)}$	Local temperature sensor		T_A = 15°C to 85°C V+ = 3.3V		–1	±0.0625	1	°C
			T_A = –40°C to 125°C		–2.5	±1.25	2.5	
$T_{ERROR(REMOTE)}$	Remote temperature sensor[1]		T_A = 15°C to 75°C T_{DIODE} = –40°C to 150°C V+ = 3.3V		–1	±0.0625	1	°C
			T_A = –40°C to 100°C T_{DIODE} = –40°C to 150°C V+ = 3.3V		–3	±1	3	
			T_A = –40°C to 125°C T_{DIODE} = –40°C to 150°C V+ = 3.3V		–5	±3	5	
T_{ERROR_PS}	Temperature error power supply sensitivity (local and remote)		V+ = 2.7V to 5.5V T_{DIODE} = –40°C to 150°C		–0.5	±0.2	0.5	°C/V
TEMPERATURE MEASUREMENT								
t_{CONV}	Conversion time (Local + Remote)		One-Shot mode	Legacy chip	105	115	125	ms
				New chip	30	35	40	
T_{RES}	Resolution	Local temperature sensor (programmable)			9		12	Bits
		Remote temperature sensor				12		
R_{SERIES}	Remote sensor source current	High	Series resistance: 3kΩ maximum			120		µA
		Medium high				60		
		Medium low		Legacy chip only		12		
		Low				6		
η	Remote transistor ideality factor		Optimized ideality factor			1.008		
SMBus INTERFACE								
V_{IH}	Logic input high voltage (SCL, SDA)				2.1			V
V_{IL}	Logic input low voltage (SCL, SDA)						0.8	V
V_{HYST}	Hysteresis					170		mV
	SMBus output low sink current				6			mA
I_{LI} and I_{LO}	Logic input current			Legacy chip	–1		1	µA
				New chip	–0.2		0.2	

6.5 Electrical Characteristics (TMP411-Q1) (continued)

At T_A = –40°C to +125°C and V+ = 2.7V to 5.5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{IN}	SMBus input capacitance (SCL, SDA)				3		pF
	SMBus clock frequency					3.4	MHz
	SMBus timeout			25	30	35	ms
	SCL falling edge to SDA valid time					1	µs
DIGITAL OUTPUTS							
V_{OL}	Output low voltage	I_{OUT} = 6mA	Legacy chip		0.15	0.4	V
			New chip		0.3	0.4	
I_{OH}	High-level output leakage current	V_{OUT} = V+	Legacy chip		0.1	1	µA
			New chip		0.05	0.2	
	$\overline{ALERT}$ or $\overline{THERM2}$ output low sink current	$\overline{ALERT}$/$\overline{THERM2}$ forced to 0.4V		6			mA
	$\overline{THERM}$ output low sink current	$\overline{THERM}$ forced to 0.4V		6			mA
POWER SUPPLY							
V+	Specific voltage range			2.7		5.5	V
I_{DD_AVG}	Quiescent current	0.0625Hz conversion V+ = 3.3V	Legacy chip		28	30	µA
			New chip		1.5	8.2	
		8Hz conversion V+ = 3.3V	Legacy chip		400	475	
			New chip		45	85	
I_{DD_SD}	Shutdown current	Serial bus inactive	Legacy chip		3	10	µA
			New chip		0.6	7	
		Serial bus active, f_s = 400kHz	Legacy chip		90		
			New chip		7		
		Serial bus active, f_s = 3.4MHz	Legacy chip		350		
			New chip		55		
	Undervoltage lockout(2)		Legacy chip	2.3	2.4	2.6	V
		This behavior is combined with Power-on-reset (POR). For more information, please see Section 7.3.6 and footnote(2)	New chip				
POR	Power-on-reset threshold		Legacy chip		1.6	2.3	V
			New chip		1.23	1.4	
	Brownout detect		New chip	1	1.14		V

(1) Tested with less than 5Ω effective series resistance and 100pF differential input capacitance. T_A is the ambient temperature of the TMP411-Q1. T_{DIODE} is the temperature at the remote diode sensor.
(2) When there is no remote diode connected, the first remote conversion should be ignored with the power supply ramp rate less than 240V/s.

6.6 Electrical Characteristics (TMP411D-Q1)

At T_A = –40°C to +125°C and V+ = 1.62V to 5.5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE ERROR							
$T_{ERROR(LOCAL)}$	Local temperature sensor		T_A = -25°C to 85°C	–0.8	±0.1	0.8	°C
			T_A = –40°C to 125°C	–1		1	
$T_{ERROR(REMOTE)}$	Remote temperature sensor(1)		T_A = -25°C to 85°C T_{DIODE} = -55°C to 150°C	–0.8	±0.25	0.8	°C
			T_A = –40°C to 105°C T_{DIODE} = -55°C to 150°C	–1		1	
			T_A = –40°C to 125°C T_{DIODE} = -55°C to 150°C	–1.25		1.25	
T_{ERROR_PS}	Temperature error power supply sensitivity (local and remote)		V+ = 1.62V to 5.5V T_{DIODE} = -55°C to 150°C	–0.2	±0.1	0.2	°C/V
TEMPERATURE MEASUREMENT							
T_{RES}	Resolution	Local temperature sensor (programmable)		9		12	Bits
		Remote temperature sensor			12		
T_{REPEAT}	Repeatability	Local sensor	V+ = 3.3V, 1Hz conversion cycle		±1		LSB
R_{SERIES}	Remote sensor source current	High	Series resistance: 3kΩ maximum		120		µA
		Medium			60		
		Low			6		
t_{CONV}	Conversion time	Local conversion only	one-shot mode		17.7		ms
		Remote + Local conversion		30	35	40	
t_{VAR}	Timing variation		Conversion period	-15	±5	15	%
η	Remote transistor ideality factor		Optimized ideality factor		1.008		
SMBus INTERFACE							
C_{IN}	SMBus input capacitance (SCL, SDA)				3		pF
V_{IH}	Logic input high voltage (SCL, SDA)		V+ ≥ 2.7V	2.1			V
			V+ < 2.7V	0.7×V+			
V_{IL}	Logic input low voltage (SCL, SDA)		V+ ≥ 2.7V			0.8	V
			V+ < 2.7V			0.3×V+	
I_{LI} and I_{LO}	Logic input/output current			–0.2		0.2	µA
V_{HYST}	Hysteresis				170		mV
	SMBus clock frequency		V+ ≥ 2.7V			3.4	MHz
	SMBus timeout			25	30	35	ms
	SCL falling edge to SDA valid time					1	µs
DIGITAL OUTPUTS							
V_{OL}	Output low voltage		I_{OUT} = 6mA V+ ≥ 2.7V		0.3	0.4	V
			I_{OUT} = 3mA V+ < 2.7V		0.17	0.4	
I_{OH}	High-level output leakage current		V_{OUT} = V+		0.05	0.2	µA
POWER SUPPLY							

6.6 Electrical Characteristics (TMP411D-Q1) (continued)

At T_A = –40°C to +125°C and V+ = 1.62V to 5.5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V+	Specific voltage range			1.62		5.5	V
I_{DD_ACTIVE}	Active conversion current	Local sensor			100	150	µA
		Remote sensor			220	320	
I_{DD_SB}	Standby current		Serial bus inactive		1	7.5	µA
I_{DD_AVG}	Average current consumption		0.0625Hz conversion V+ = 3.3V		1.5	8.2	µA
			8Hz conversion V+ = 3.3V		45	85	
I_{DD_SD}	Shutdown current		Serial bus inactive		0.6	7	µA
			Serial bus active, f_s = 400kHz		7		
			Serial bus active, f_s = 3.4MHz		55		
POR	Power-on-reset threshold				1.23	1.4	V
	Brownout detect			1	1.14		

(1) Tested with less than 5Ω effective series resistance and 100pF differential input capacitance. T_A is the ambient temperature of the TMP411D-Q1. T_{DIODE} is the temperature at the remote diode sensor.

6.7 Timing Characteristics

			FAST MODE		HIGH-SPEED MODE		UNIT
			MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency		0.001	0.4	0.001	3.4	MHz
$t_{(BUF)}$	Bus free time between STOP and START condition		600		160		ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.		100		100		ns
$t_{(SUSTA)}$	Repeated START condition setup time		100		100		ns
$t_{(SUSTO)}$	STOP condition setup time		100		100		ns
$t_{(HDDAT)}$	Data hold time		0(1)		0(2)		ns
$t_{(SUDAT)}$	Data setup time	TMP411-Q1 (Legacy chip)	100		10		ns
		TMP411-Q1 (New chip) TMP411D-Q1	100		20		
$t_{(LOW)}$	SCL clock LOW period		1300		160		ns
$t_{(HIGH)}$	SCL clock HIGH period		600		60		ns
t_F	Clock and data fall time			300		160	ns
t_R	Clock and data rise time			300		160	ns
	SCLK ≤ 100kHz			1000			ns

(1) For cases with an SCL fall time of less than 20ns, or an SDA rise or fall time of less than 20ns, the hold time must be greater than 20ns.
(2) For cases with an SCL fall time of less than 10ns, or an SDA rise or fall time of less than 10ns, the hold time must be greater than 10ns.

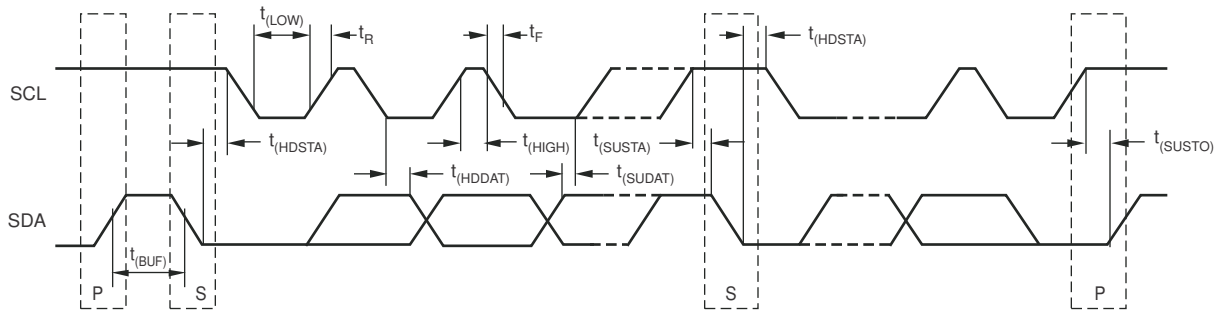


Figure 6-1. Two-Wire Timing Diagram

6.9 Typical Characteristics (TMP411-Q1)

At T_A = 25°C and V+ = V_S = 5V (unless otherwise noted)

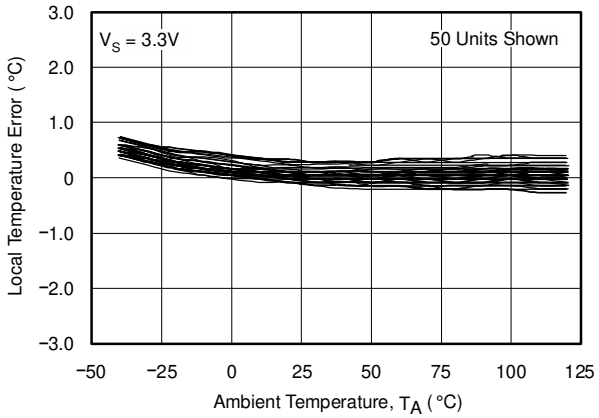


Figure 6-2. Local Temperature Error vs TMP411-Q1 Ambient Temperature (Legacy Chip)

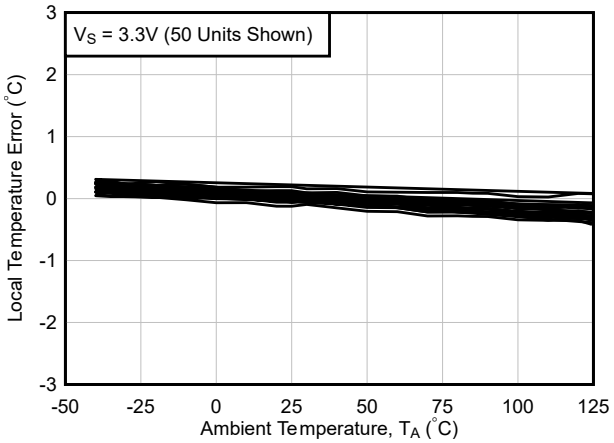


Figure 6-3. Local Temperature Error vs TMP411-Q1 Ambient Temperature (New Chip)

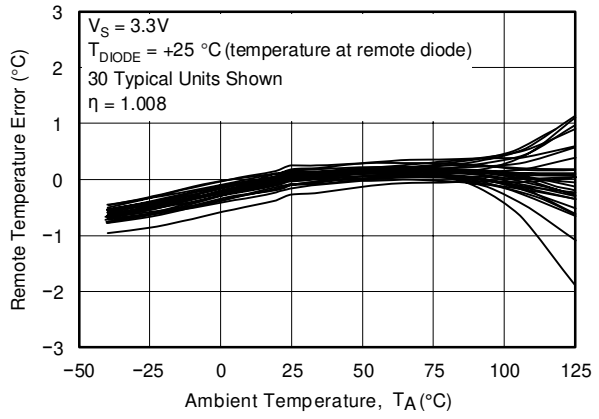


Figure 6-4. Remote Temperature Error vs TMP411-Q1 Ambient Temperature (Legacy Chip)

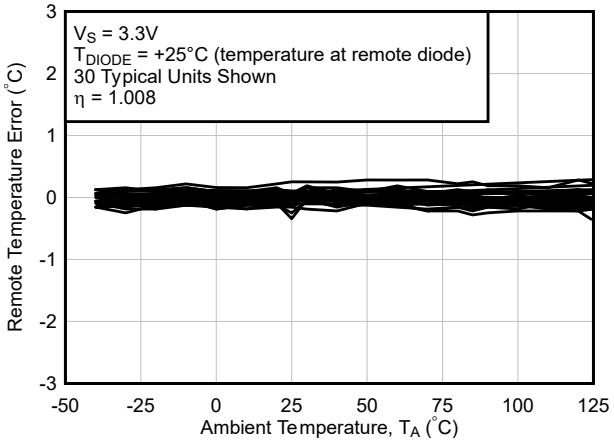


Figure 6-5. Remote Temperature Error vs TMP411-Q1 Ambient Temperature (New Chip)

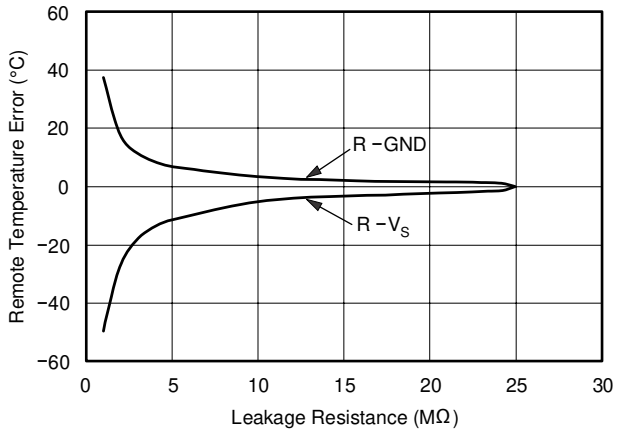


Figure 6-6. Remote Temperature Error vs Leakage Resistance (Legacy Chip)

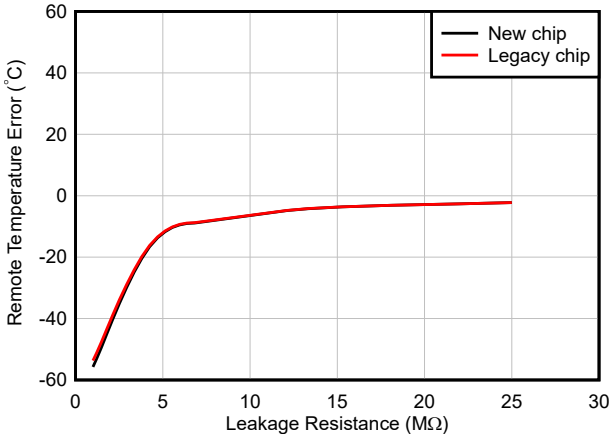


Figure 6-7. Remote Temperature Error vs Leakage Resistance (Comparison of Legacy Chip and New Chip)

6.9 Typical Characteristics (TMP411-Q1) (continued)

At T_A = 25°C and V+ = V_S = 5V (unless otherwise noted)

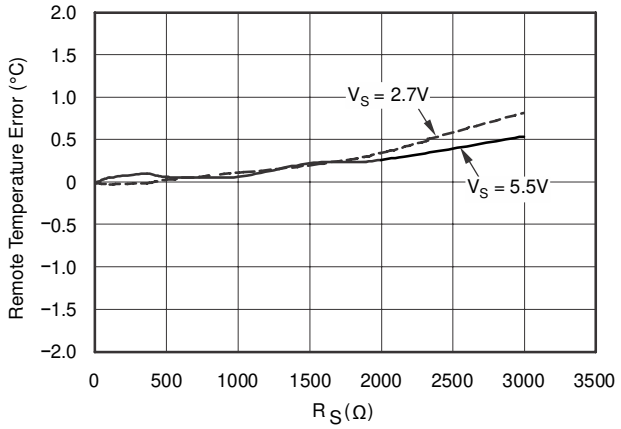


Figure 6-8. Remote Temperature Error vs Series Resistance (Diode-Connected Transistor, 2N3906 PNP) (Legacy Chip)

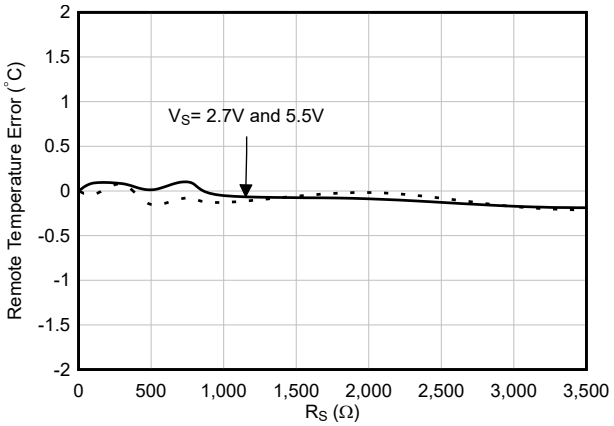


Figure 6-9. Remote Temperature Error vs Series Resistance (Diode-Connected Transistor, 2N3906 PNP) (New Chip)

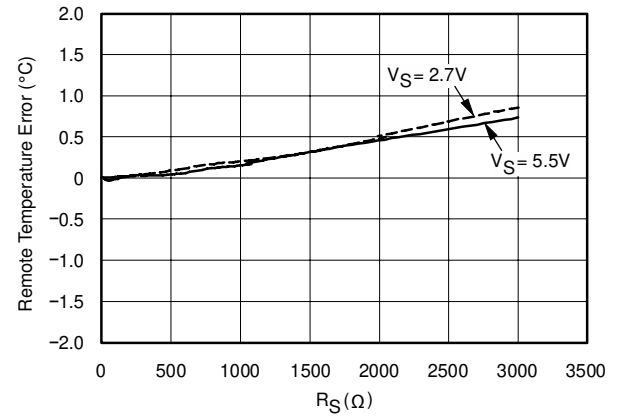


Figure 6-10. Remote Temperature Error vs Series Resistance (GND Collector-Connected Transistor, 2N3906 PNP) (Legacy Chip)

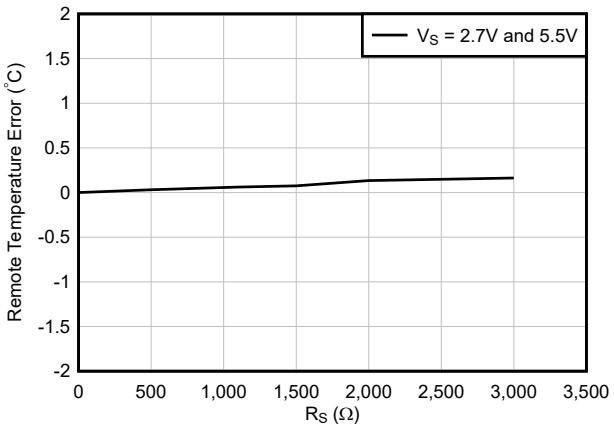


Figure 6-11. Remote Temperature Error vs Series Resistance (GND Collector-Connected Transistor, 2N3906 PNP) (New Chip)

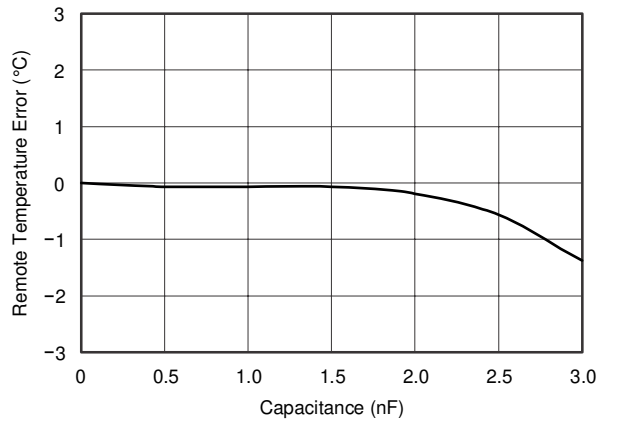


Figure 6-12. Remote Temperature Error vs Differential Capacitance (Legacy Chip)

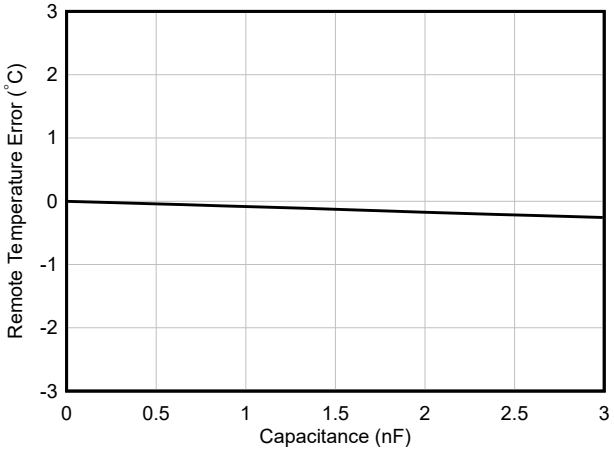


Figure 6-13. Remote Temperature Error vs Differential Capacitance (New Chip)

6.9 Typical Characteristics (TMP411-Q1) (continued)

At T_A = 25°C and V+ = V_S = 5V (unless otherwise noted)

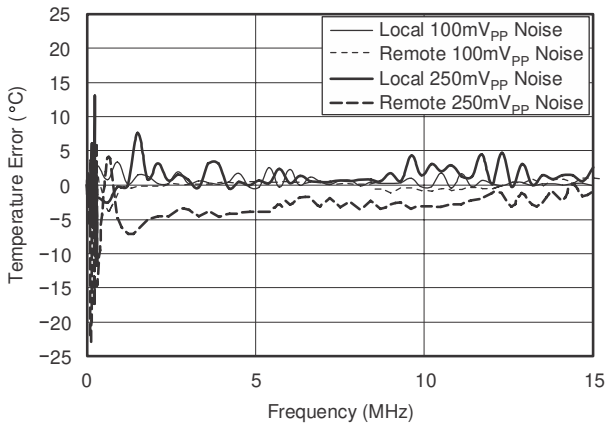


Figure 6-14. Temperature Error vs Power-Supply Noise Frequency (Legacy Chip)

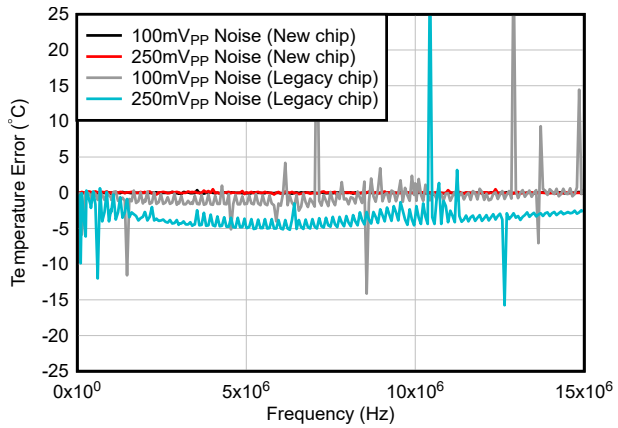


Figure 6-15. Remote Temperature Error vs Power-Supply Noise Frequency (Comparison of Legacy Chip and New Chip)

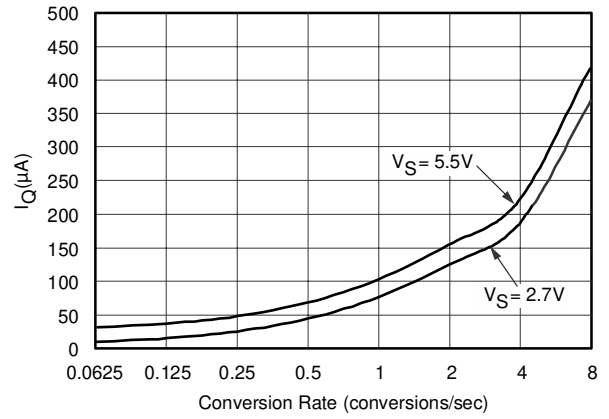


Figure 6-16. Quiescent Current vs Conversion Rate (Legacy Chip)

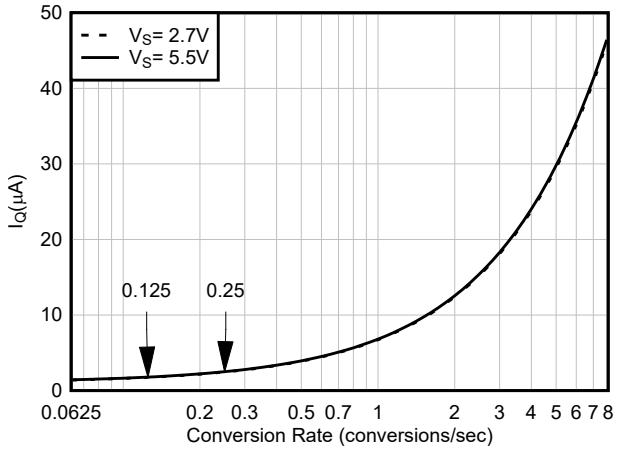


Figure 6-17. Quiescent Current vs Conversion Rate (New Chip)

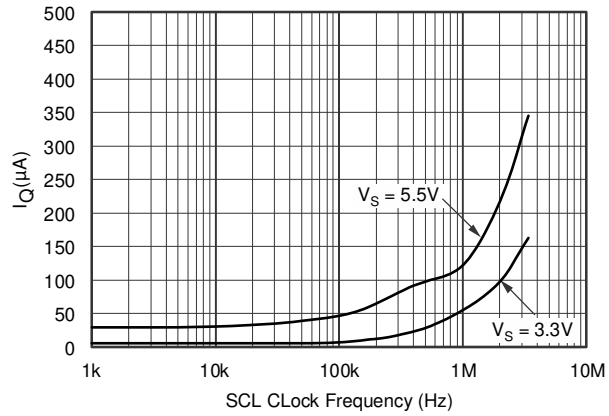


Figure 6-18. Shutdown Quiescent Current vs SCL Clock Frequency (Legacy Chip)

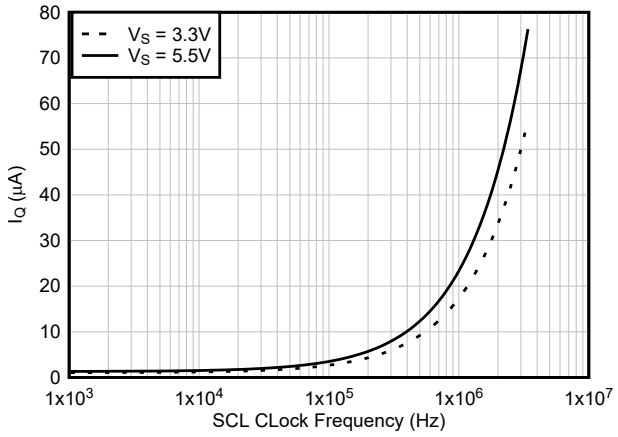


Figure 6-19. Shutdown Quiescent Current vs SCL Clock Frequency (New Chip)

6.9 Typical Characteristics (TMP411-Q1) (continued)

At T_A = 25°C and V+ = V_S = 5V (unless otherwise noted)

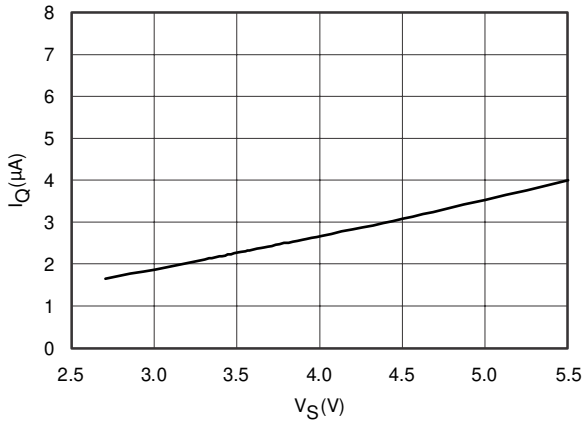


Figure 6-20. Shutdown Quiescent Current vs Supply Voltage (Legacy Chip)

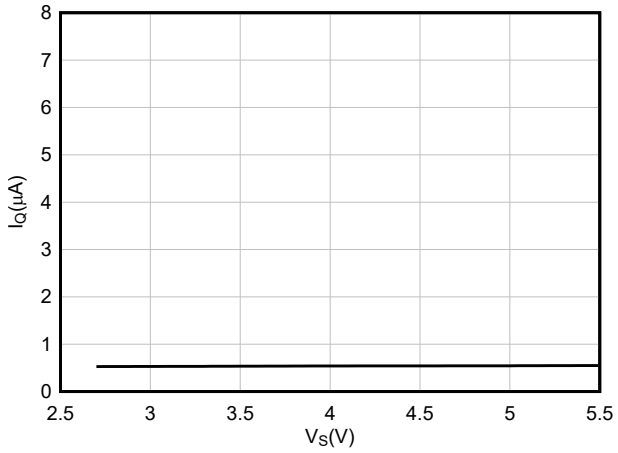


Figure 6-21. Shutdown Quiescent Current vs Supply Voltage (New Chip)

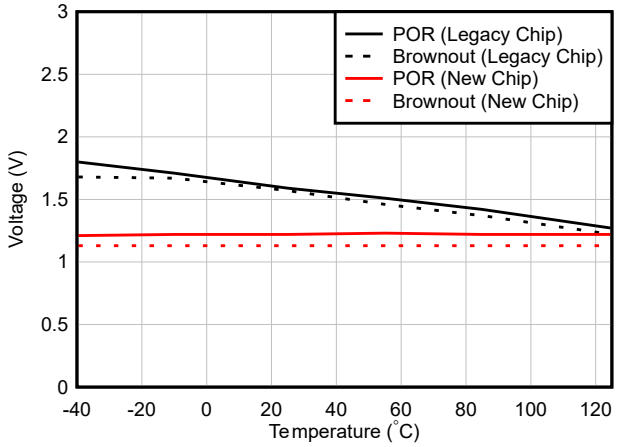


Figure 6-22. POR threshold and Brownout detect voltages vs Temperature (Comparison of Legacy Chip and New Chip)

6.10 Typical Characteristics (TMP411D-Q1)

At T_A = 25°C and V+ = 3.3V (unless otherwise noted)

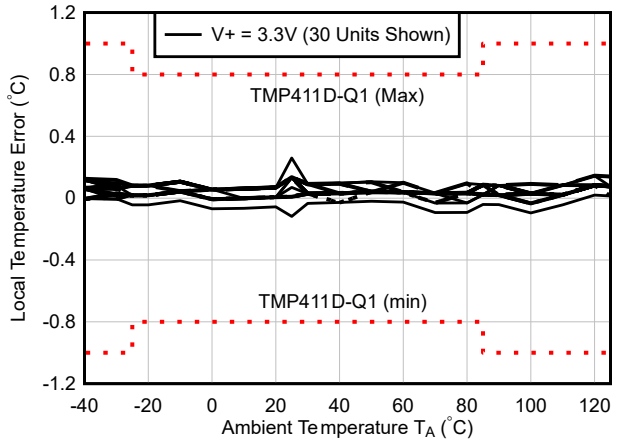


Figure 6-23. Local Temperature Error vs TMP411D-Q1 Ambient Temperature

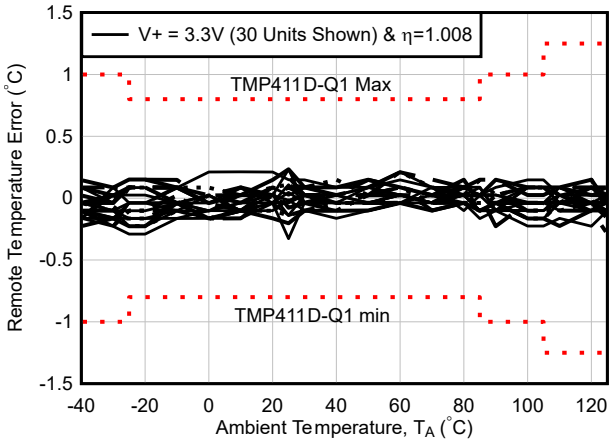


Figure 6-24. Remote Temperature Error vs TMP411D-Q1 Ambient Temperature

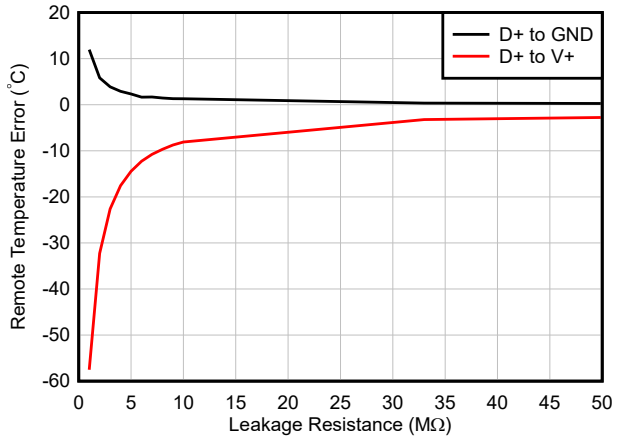


Figure 6-25. Remote Temperature Error vs Leakage Resistance

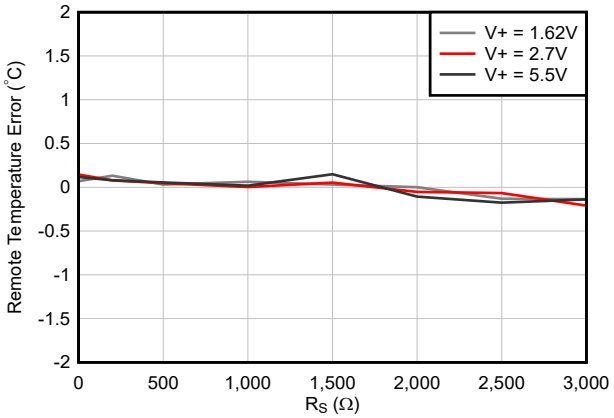


Figure 6-26. Remote Temperature Error vs Series Resistance (Diode-Connected Transistor, 2N3906 PNP)

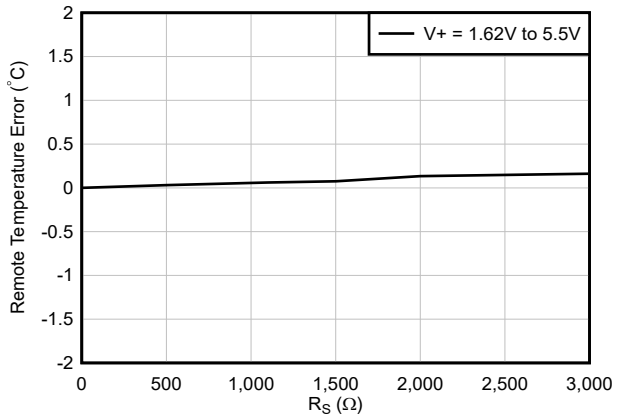


Figure 6-27. Remote Temperature Error vs Series Resistance (GND Collector-Connected Transistor, 2N3906 PNP)

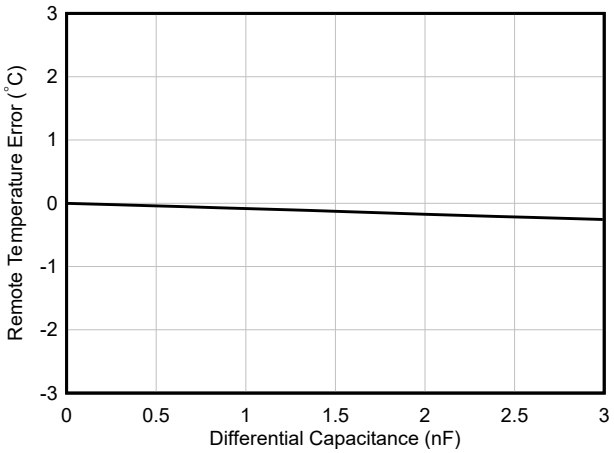


Figure 6-28. Remote Temperature Error vs Differential Capacitance

6.10 Typical Characteristics (TMP411D-Q1) (continued)

At T_A = 25°C and V+ = 3.3V (unless otherwise noted)

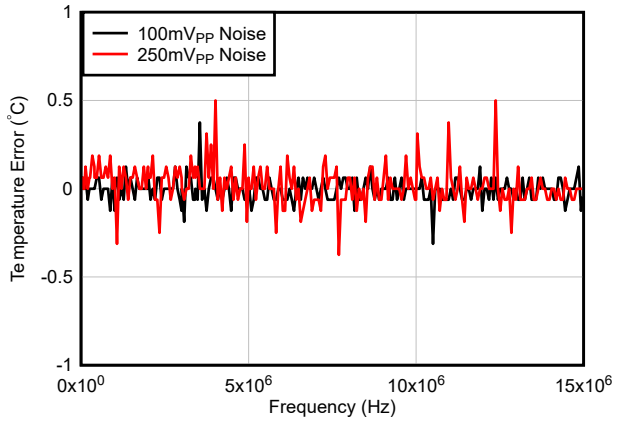


Figure 6-29. Temperature Error vs Power-Supply Noise Frequency

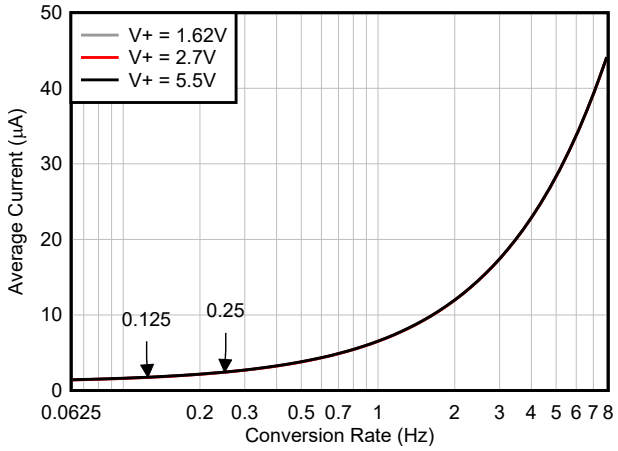


Figure 6-30. Average Current vs Conversion Rate

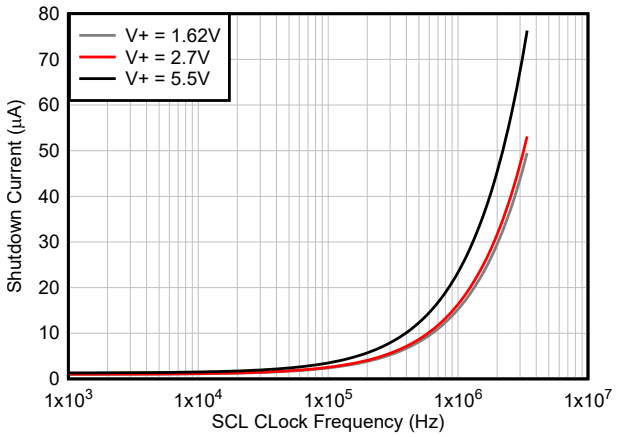


Figure 6-31. Shutdown Current vs SCL Clock Frequency

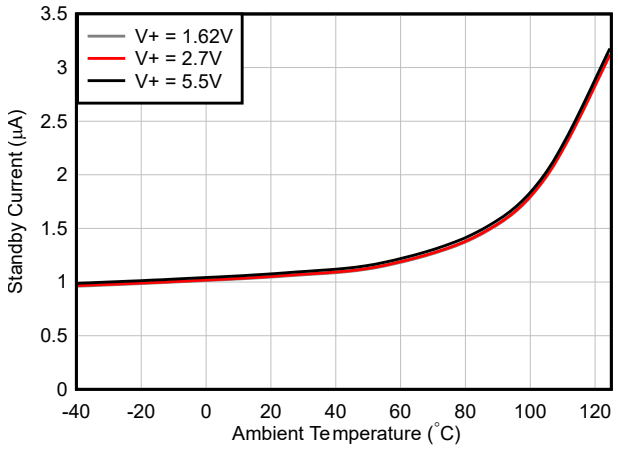


Figure 6-32. Standby Current vs Temperature

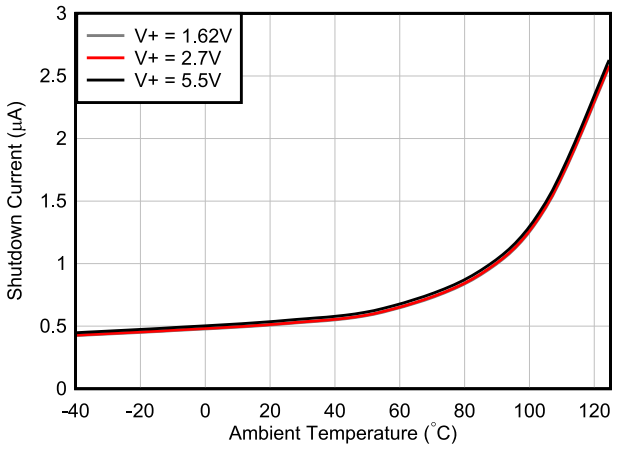


Figure 6-33. Shutdown Current vs Temperature

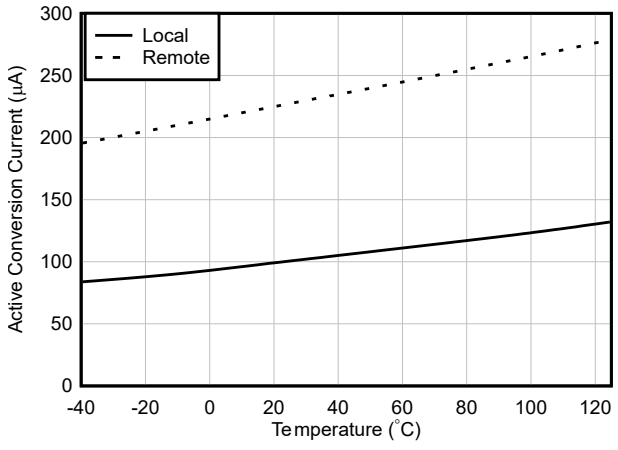


Figure 6-34. Active Current vs Temperature (Local and Remote)

6.10 Typical Characteristics (TMP411D-Q1) (continued)

At T_A = 25°C and V+ = 3.3V (unless otherwise noted)

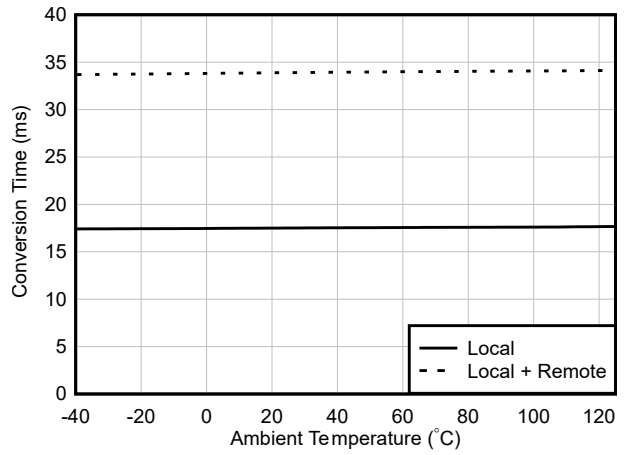


Figure 6-35. Conversion Time vs Temperature (Local and Local + Remote)

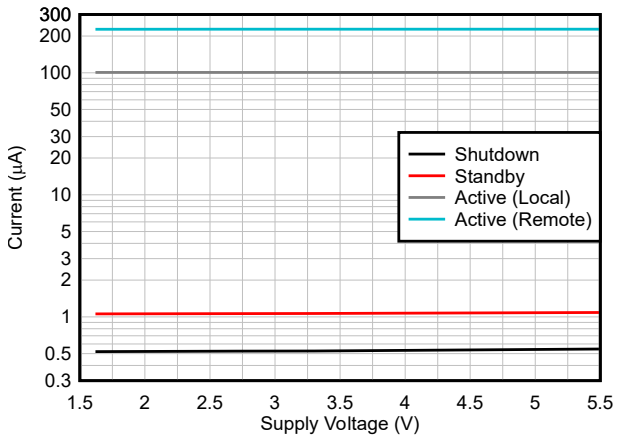


Figure 6-36. Shutdown, Standby, Active (Local) and Active (Remote) Currents vs Supply Voltage (Temperature at 25°C)

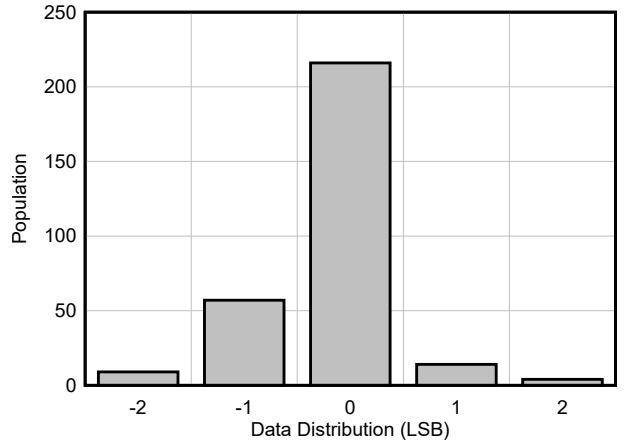


Figure 6-37. Remote Temperature Noise Data Distribution (300 Samples)

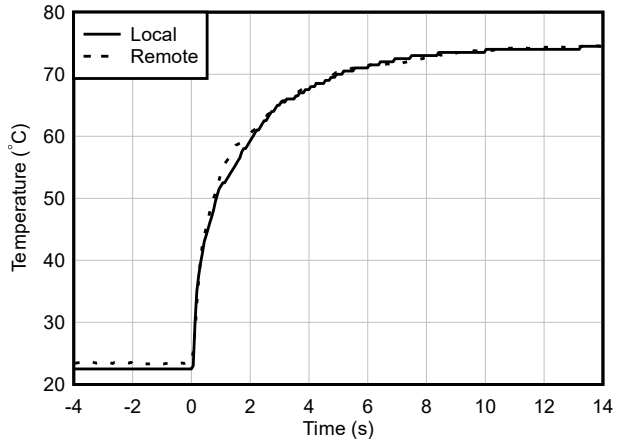


Figure 6-38. Temperature Response Time (Stirred Liquid, Soldered Device, and 2N3906 PNP Transistor on 62mil 2-Layer FR4 PCB)

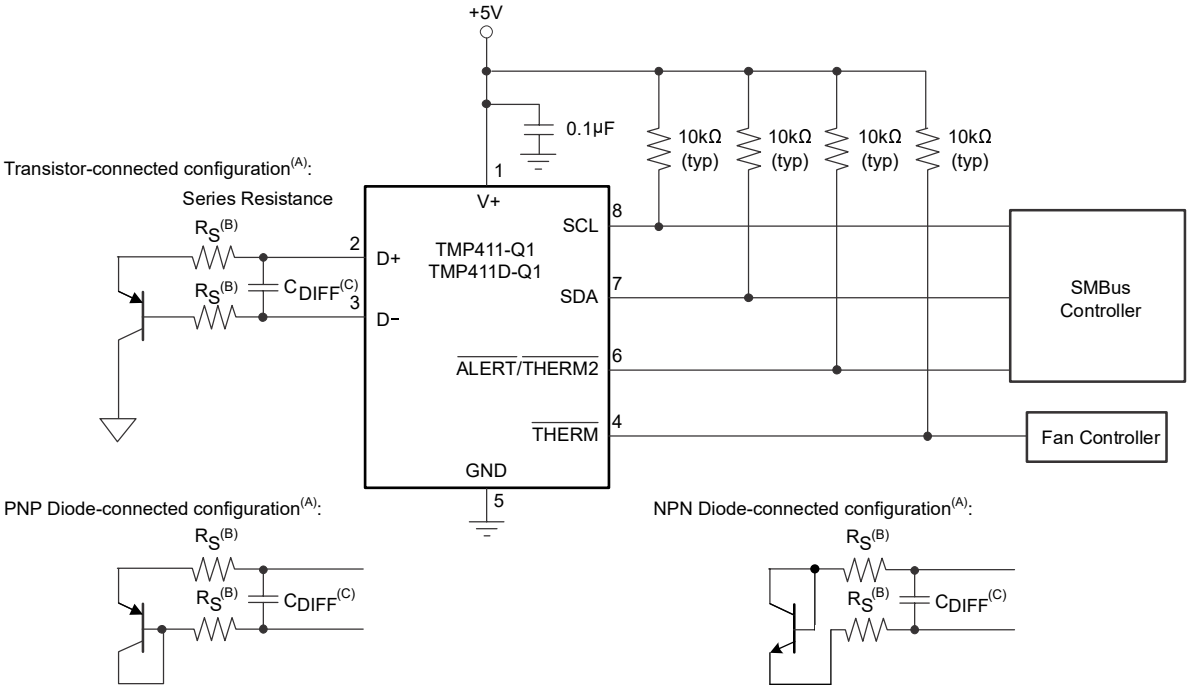
7 Detailed Description

7.1 Overview

The TMP411-Q1 and TMP411D-Q1 devices are dual-channel digital temperature sensors that combine a local die-temperature measurement channel and a remote junction-temperature measurement channel in a single VSSOP-8 or SOT23-8 package. The TMP411-Q1 and TMP411D-Q1 devices are two-wire-compatible and SMBus interface-compatible and are specified over an ambient temperature range of –40°C to 125°C. The TMP411-Q1 and TMP411D-Q1 devices contain multiple registers for holding configuration information, temperature measurement results, temperature comparator maximum/minimum limits, and status information.

User-programmed high- and low-temperature limits stored in the TMP411-Q1 and TMP411D-Q1 devices can be used to trigger an overtemperature alarm ($\overline{\text{ALERT}}$) on local and remote temperatures. Additional thermal limits can be programmed into the TMP411-Q1 and TMP411D-Q1 devices and used to trigger another flag ($\overline{\text{THERM}}$) that initiates a system response to rising temperatures.

The TMP411-Q1 and TMP411D-Q1 devices require only a transistor connected between D+ and D− for proper remote temperature sensing operation. The SCL and SDA interface pins require pullup resistors as part of the communication bus, whereas $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins are open-drain outputs that also need pullup resistors. $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins can be shared with other devices if desired for a wired-OR implementation. A 0.1µF power-supply bypass capacitor is recommended for good local bypassing. Figure 7-1 shows a typical configuration for the TMP411-Q1 and TMP411D-Q1 devices.



A. A diode-connected configuration provides better settling time. The transistor-connected configuration provides better series resistance cancellation. NPN transistors must be diode-connected. PNP transistors can either be transistor-connected or diode-connected. TI recommends this layout for the MMBT3906LP and MMBT3904LP devices.

B. R_S (optional) must be < 1.5kΩ in most applications. Selection of R_S depends on the specific application; see Filtering.

C. C_{DIFF} (optional) must be < 1000pF in most applications. Selection of C_{DIFF} depends on the specific application; see Filtering, Figure 6-12 (Figure 6-13 for the new chip), and Figure 6-28.

Figure 7-1. Basic Connections

7.2 Functional Block Diagram

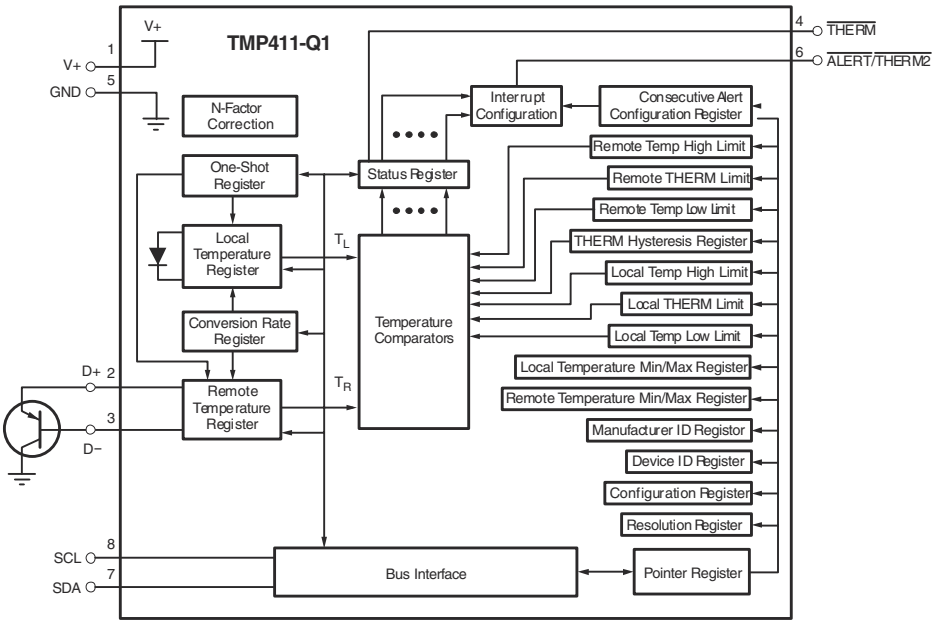


Figure 7-2. Functional Block Diagram

7.3 Feature Description

7.3.1 Series Resistance Cancellation

Figure 7-1 shows series resistance in an application circuit that results from printed circuit board (PCB) trace resistance and remote line length. The TMP411-Q1 and TMP411D-Q1 devices automatically cancel the resistance, which prevents a temperature offset.

The TMP411-Q1 and TMP411D-Q1 devices cancel up to 3kΩ of series line resistance, which eliminates the need for additional characterization and temperature offset correction.

See Figure 6-8 (Figure 6-9 for a new chip), Figure 6-10 (Figure 6-11 for a new chip), Figure 6-26 and Figure 6-27 for details on the effect of series resistance and power-supply voltage on sensed remote temperature error.

7.3.2 Differential Input Capacitance

The TMP411-Q1 and TMP411D-Q1 devices tolerate differential input capacitance of up to 1000pF with minimal change in temperature error. The effect of capacitance on the sensed remote temperature error is shown in Figure 6-12 (Figure 6-13 for new chip) and Figure 6-28.

7.3.3 Temperature Measurement Data

Temperature measurement data is taken over a default range of 0°C to 127°C for both local and remote locations. Measurements from –55°C to 150°C can be made both locally and remotely by reconfiguring the TMP411-Q1 and TMP411D-Q1 devices for the extended temperature range. To change the TMP411-Q1 and TMP411D-Q1 configuration from the standard to the extended temperature range, switch bit 2 (RANGE) of the Configuration Register from low to high.

Temperature data resulting from conversions within the default measurement range are represented in binary form, as listed in the standard binary column of Table 7-1. Note that any temperature below 0°C results in a data value of zero (00h). Likewise, temperatures above 127°C result in a value of 127 (7Fh). The device can be set to measure over an extended temperature range by changing bit 2 of the Configuration Register from low to high. The change in measurement range and data format from standard binary to extended binary occurs at the next temperature conversion. For data captured in the extended temperature range configuration, an

offset of 64 (40h) is added to the standard binary value, as listed in the extended binary column of Table 7-1. This configuration allows measurement of temperatures below 0°C. Note that binary values corresponding to temperatures as low as –64°C, and as high as 191°C are possible; however, most temperature-sensing diodes only measure within the range of –55°C to 150°C. Additionally, the TMP411-Q1 and TMP411D-Q1 devices are rated only for ambient local temperatures ranging from –40°C to 125°C. Parameters in the Absolute Maximum Ratings table must be observed.

Table 7-1. Temperature Data Format (Local and Remote Temperature High Bytes)

TEMP (°C)	LOCAL/REMOTE TEMPERATURE REGISTER HIGH BYTE VALUE (1°C RESOLUTION)			
	STANDARD BINARY		EXTENDED BINARY	
	BINARY	HEX	BINARY	HEX
−64	0000 0000	00	0000 0000	00
−50	0000 0000	00	0000 1110	0E
−25	0000 0000	00	0010 0111	27
0	0000 0000	00	0100 0000	40
1	0000 0001	01	0100 0001	41
5	0000 0101	05	0100 0101	45
10	0000 1010	0A	0100 1010	4A
25	0001 1001	19	0101 1001	59
50	0011 0010	32	0111 0010	72
75	0100 1011	4B	1000 1011	8B
100	0110 0100	64	1010 0100	A4
125	0111 1101	7D	1011 1101	BD
127	0111 1111	7F	1011 1111	BF
150	0111 1111	7F	1101 0110	D6
175	0111 1111	7F	1110 1111	EF
191	0111 1111	7F	1111 1111	FF

The TMP411-Q1 and TMP411D-Q1 devices' temperature sensor does not utilize 2's complement format to read in temperature values. For this reason, the decode does not cast them into a signed type. The way the TMP411-Q1 and TMP411D-Q1 devices express a negative temperature is by enabling a RANGE bit, which adds 64°C to the result. When RANGE is enabled, the decode must subtract 64, causing a raw value of 0 to become –64°C output.

Table 7-2. 12-Bit Q4 Parameters

PARAMETER	VALUE
Bits	12
Q	4
Resolution	0.0625
Range (+)	127.9375
Range (–)	0
First Byte Integer C	Yes
25˚C	0x1900

Table 7-3. 12-Bit Q4 Bit Values in °C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	64	32	16	8	4	2	1	0.5	0.25	0.125	0.0625	—	—	—	—
—	64	32	16	8	4	2	1	1/2	1/4	1/8	1/16	—	—	—	—
—	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	—	—	—	—

```
/* 12-bit format will have 4 bits discarded by right shift
 q4 is 0.062500 resolution
 the following bytes represent 24.5C
 there is no cast into signed type */
uint8_t byte1 = 0x18;
uint8_t byte2 = 0x80;
float f = ((byte1 << 8 | byte2) >> 4) * 0.0625f;
int mC = ((byte1 << 8 | byte2) >> 4) * 1000 >> 4;
int C = byte1;
```

Note

Whenever changing between standard and extended temperature ranges, be aware that the temperatures stored in the temperature limit registers are NOT automatically reformatted to correspond to the new temperature range format. These temperature limit values must be reprogrammed in the appropriate binary or extended binary format.

Both local and remote temperature data use two bytes for data storage. The high byte stores the temperature with 1°C resolution. The second or low byte stores the decimal fraction value of the temperature and allows a higher measurement resolution; see Table 7-4. The measurement resolution for the remote channel is 0.0625°C and is not adjustable. The measurement resolution for the local channel is adjustable; the resolution can be set for 0.5°C, 0.25°C, 0.125°C, or 0.0625°C by setting the RES1 and RES0 bits of the Resolution Register; see Table 8-4.

Table 7-4. Decimal Fraction Temperature Data Format (Local and Remote Temperature Low Bytes)

TEMP (°C)	REMOTE TEMPERATURE REGISTER LOW BYTE VALUE		LOCAL TEMPERATURE REGISTER LOW BYTE VALUE							
	0.0625°C RESOLUTION		0.5°C RESOLUTION		0.25°C RESOLUTION		0.125°C RESOLUTION		0.0625°C RESOLUTION	
	STANDARD AND EXTENDED BINARY	HEX	STANDARD AND EXTENDED BINARY	HEX	STANDARD AND EXTENDED BINARY	HEX	STANDARD AND EXTENDED BINARY	HEX	STANDARD AND EXTENDED BINARY	HEX
0.0000	0000 0000	00	0000 0000	00	0000 0000	00	0000 0000	00	0000 0000	00
0.0625	0001 0000	10	0000 0000	00	0000 0000	00	0000 0000	00	0001 0000	10
0.1250	0010 0000	20	0000 0000	00	0000 0000	00	0010 0000	20	0010 0000	20
0.1875	0011 0000	30	0000 0000	00	0000 0000	00	0010 0000	20	0011 0000	30
0.2500	0100 0000	40	0000 0000	00	0100 0000	40	0100 0000	40	0100 0000	40
0.3125	0101 0000	50	0000 0000	00	0100 0000	40	0100 0000	40	0101 0000	50
0.3750	0110 0000	60	0000 0000	00	0100 0000	40	0110 0000	60	0110 0000	60
0.4375	0111 0000	70	0000 0000	00	0100 0000	40	0110 0000	60	0111 0000	70
0.5000	1000 0000	80	1000 0000	80	1000 0000	80	1000 0000	80	1000 0000	80
0.5625	1001 0000	90	1000 0000	80	1000 0000	80	1000 0000	80	1001 0000	90
0.6250	1010 0000	A0	1000 0000	80	1000 0000	80	1010 0000	A0	1010 0000	A0
0.6875	1011 0000	B0	1000 0000	80	1000 0000	80	1010 0000	A0	1011 0000	B0
0.7500	1100 0000	C0	1000 0000	80	1100 0000	C0	1100 0000	C0	1100 0000	C0
0.8125	1101 0000	D0	1000 0000	80	1100 0000	C0	1100 0000	C0	1101 0000	D0
0.8750	1110 0000	E0	1000 0000	80	1100 0000	C0	1110 0000	E0	1110 0000	E0
0.9375	1111 0000	F0	1000 0000	80	1100 0000	C0	1110 0000	E0	1111 0000	F0

7.3.4 $\overline{\text{THERM}}$ (PIN 4) and $\overline{\text{ALERT}}$/ $\overline{\text{THERM2}}$ (PIN 6)

The TMP411-Q1 and TMP411D-Q1 devices have two pins dedicated to alarm functions, the $\overline{\text{THERM}}$ and $\overline{\text{ALERT}}$/ $\overline{\text{THERM2}}$ pins. Both pins are open-drain outputs that each require a pullup resistor to V+. These pins can be wire-ORed together with other alarm pins for system monitoring of multiple sensors. The $\overline{\text{THERM}}$ pin provides a thermal interrupt that cannot be software-disabled. The $\overline{\text{ALERT}}$ pin is intended for use as an earlier warning interrupt, and can be software disabled, or masked. The $\overline{\text{ALERT}}$/ $\overline{\text{THERM2}}$ pin can also be configured for use as a $\overline{\text{THERM2}}$ pin, which is a second $\overline{\text{THERM}}$ pin (Configuration Register: AL/TH bit = 1). The default setting configures pin 6 to function as the $\overline{\text{ALERT}}$ pin (AL/TH = 0).

The $\overline{\text{THERM}}$ pin asserts low when either the measured local or remote temperature is outside of the temperature range programmed in the corresponding Local or Remote THERM Limit Register. The THERM temperature limit range can be programmed with a wider range than that of the limit registers, which allows the $\overline{\text{ALERT}}$ pin to provide an earlier warning than the $\overline{\text{THERM}}$ pin. The $\overline{\text{THERM}}$ alarm resets automatically when the measured temperature falls within the THERM temperature limit range minus the hysteresis value stored in the THERM Hysteresis Register. The permitted hysteresis values are shown in Table 8-8. The default hysteresis is 10°C. When the $\overline{\text{ALERT}}$/ $\overline{\text{THERM2}}$ pin is configured as a second thermal alarm (Configuration Register: bit 7 = 0, bit 5 = 1), the pin functions the same as the $\overline{\text{THERM}}$ pin, but uses the temperatures stored in the Local/Remote Temperature High/Low Limit Registers to set the comparison range.

When $\overline{\text{ALERT}}$/ $\overline{\text{THERM2}}$ (pin 6) is configured as $\overline{\text{ALERT}}$ pin (Configuration Register: bit 7 = 0, bit 5 = 0), the pin asserts low when either the measured local or remote temperature violates the range limit set by the corresponding Local/Remote Temperature High/Low Limit Registers. This alert function can be configured to assert only if the range is violated a specified number of consecutive times (1, 2, 3, or 4). The consecutive violation limit is set in the Consecutive Alert Register. False alerts that occur as a result of environmental noise can be prevented by requiring consecutive faults. The $\overline{\text{ALERT}}$ pin also asserts low if the remote temperature sensor is open-circuit. When the MASK function is enabled (Configuration Register: bit 7 = 1), the $\overline{\text{ALERT}}$ pin is disabled (that is, masked). The $\overline{\text{ALERT}}$ pin resets when the controller reads the device address, as long as the condition that caused the alert no longer persists, and the Status Register is reset.

7.3.5 Sensor Fault

The TMP411-Q1 and TMP411D-Q1 devices sense a fault at the D+ input resulting from incorrect diode connection or an open circuit. The detection circuitry consists of a voltage comparator that trips when the voltage at D+ exceeds (V+) – 0.6V (typical). The comparator output is continuously checked during a conversion. If a fault is detected, the last valid measured temperature is used for the temperature measurement result, the OPEN bit (Status Register, bit 2) is set high, and, if the alert function is enabled, $\overline{\text{ALERT}}$ asserts low.

The D+ and D− inputs must be connected together to prevent meaningless fault warnings when the TMP411-Q1 and TMP411D-Q1 remote sensors are not in use.

7.3.6 Undervoltage Lockout (TMP411-Q1 Only)

Legacy Chip: The TMP411-Q1 senses when the power-supply voltage reaches a minimum voltage level for the ADC converter to function, as shown in Figure 7-3. The detection circuitry consists of a voltage comparator that enables the ADC converter after the power supply (V+) exceeds 2.45V (typical). The comparator output is checked during a conversion. The TMP411 does not perform a temperature conversion if the power supply is not valid. The last valid measured temperature remains as the temperature measurement result. Note that the device can still communicate with the Host when the power supply value is between the power-on-reset (POR) and Undervoltage Lockout voltages.

New Chip: This behavior is combined with the power-on-reset (POR), and the user must consider POR instead of the undervoltage lockout. The new chip can both communicate with the Host and do temperature conversion when the power supply value is above POR voltage, as shown in Figure 7-4. In addition, when there is no remote diode connected, the first remote conversion must be ignored with the power supply ramp rate less than 240V/s.

The differences of POR and Brownout detect voltages in both legacy chip and new chip are shown in Figure 6-22.

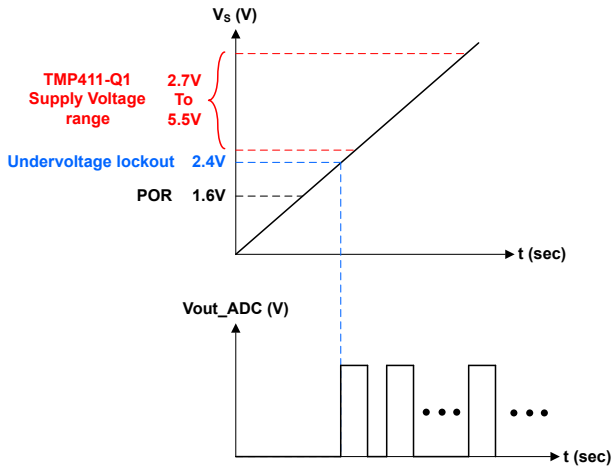


Figure 7-3. Undervoltage Lockout Behavior (Legacy Chip)

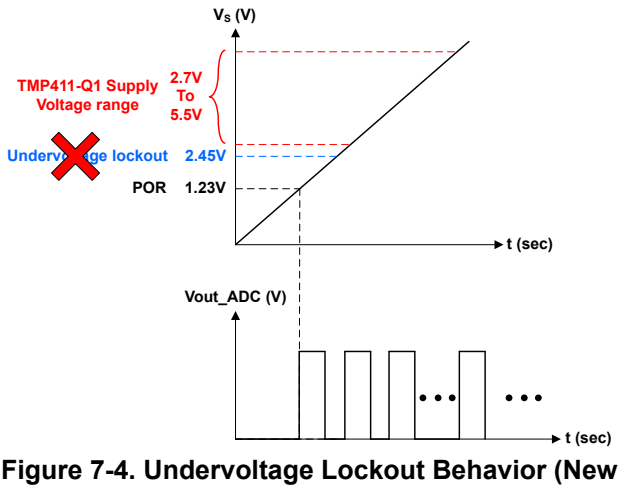


Figure 7-4. Undervoltage Lockout Behavior (New Chip)

7.3.7 Filtering

Remote junction temperature sensors are typically implemented in a noisy environment. Noise is most often created by fast digital signals, and it can corrupt measurements. The TMP411-Q1 and TMP411D-Q1 devices have a built-in 65kHz filter on the inputs of D+ and D− to minimize the effects of noise. However, a bypass capacitor placed differentially across the inputs of the remote temperature sensor is recommended to make the application more robust against unwanted coupled signals. The value of the capacitor must be between 100pF and 1nF. Some applications attain better overall accuracy with additional series resistance; however, this increased accuracy is setup-specific. When series resistance is added, the value must not be greater than 3kΩ.

If filtering is needed, the suggested component values are 100pF and 50Ω on each input. Exact values are specific to the application.

7.4 Device Functional Modes

7.4.1 Shutdown Mode (SD)

The TMP411-Q1 and TMP411D-Q1 Shutdown mode saves maximum power by shutting down all device circuitry other than the serial interface, which reduces current consumption to typically less than 3µA (0.6µA for the TMP411-Q1 new chip and TMP411D-Q1); see Figure 6-20 (Figure 6-21 for the new chip). Shutdown mode is enabled when the shutdown bit (SD) of the Configuration Register is configured 1’b. Once programmed, the device enters the Shutdown mode immediately and stops any current temperature conversion. If the Shutdown mode is entered during local temperature conversion, no update to the local/remote temperature result occurs. If the Shutdown mode is entered during remote temperature conversion, no update to the remote temperature result occurs, but the local temperature result is updated since the local temperature conversion is already completed. When the shutdown bit (SD) is configured to 0’b, the device remains in continuous conversion state.

7.4.2 One-Shot Conversion

When the TMP411-Q1 and TMP411D-Q1 devices are in Shutdown mode (SD = 1 in the Configuration Register), a single conversion on both channels is started by writing any value to the One-Shot Start Register, pointer address 0Fh. This write operation starts one conversion; the TMP411-Q1 and TMP411D-Q1 return to Shutdown mode when that conversion completes. The value of the data sent in the write command is irrelevant and is not stored by the TMP411-Q1 and TMP411D-Q1. When the TMP411-Q1 and TMP411D-Q1 devices are in Shutdown mode, an initial 200µs is required before a one-shot command can be given. (NOTE: When a shutdown command is issued, the TMP411-Q1 and TMP411D-Q1 complete the current conversion before shutting down.) This wait time only applies to the 200µs immediately following shutdown. One-shot commands can be issued without delay thereafter.

7.5 Programming

7.5.1 Serial Interface

The TMP411-Q1 and TMP411D-Q1 devices operate only as a target device on either the two-wire bus or the SMBus. Connections to either bus are made through the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP411-Q1 and TMP411D-Q1 support the transmission protocol for fast (1kHz to 400kHz) and high-speed (1kHz to 3.4MHz) modes. All data bytes are transmitted with the MSB first.

7.5.2 Bus Overview

The TMP411-Q1 and TMP411D-Q1 devices are SMBus interface-compatible. In the SMBus protocol, the device that initiates the transfer is called a controller, and the devices controlled by the controller are targets. The bus must be controlled by a controller device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated. START is indicated by pulling the data line (SDA) from a high to a low logic level while SCL is high. All targets on the bus shift are in the target address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the target being addressed responds to the controller by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses, followed by an Acknowledge bit. During data transfer, the SDA line must remain stable while SCL is high, because any change in SDA while SCL is high is interpreted as a control signal.

Once all data has been transferred, the controller generates a STOP condition. STOP is indicated by pulling the SDA line from low to high while the SCL line is high.

7.5.3 Timing Diagrams

The TMP411-Q and TMP411D-Q1 devices are two-wire and SMBus-compatible. Figure 7-5 to Figure 7-8 describe the various operations on the TMP411-Q1 and TMP411D-Q1. Bus definitions are given as follows:

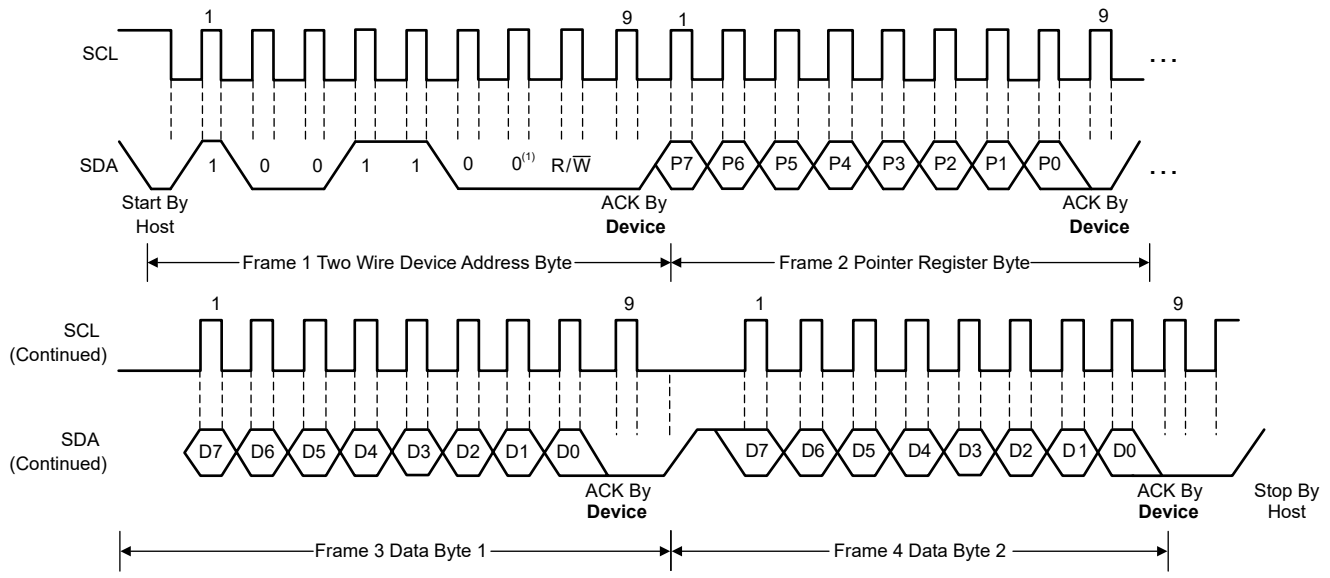
Bus Idle: Both SDA and SCL lines remain high.

Start Data Transfer: A change in the state of the SDA line, from high to low (while the SCL line is high), defines a START condition. A START condition initiates each data transfer.

Stop Data Transfer: A change in the state of the SDA line from low to high (while the SCL line is high) defines a STOP condition. A STOP or repeated START condition terminates each data transfer.

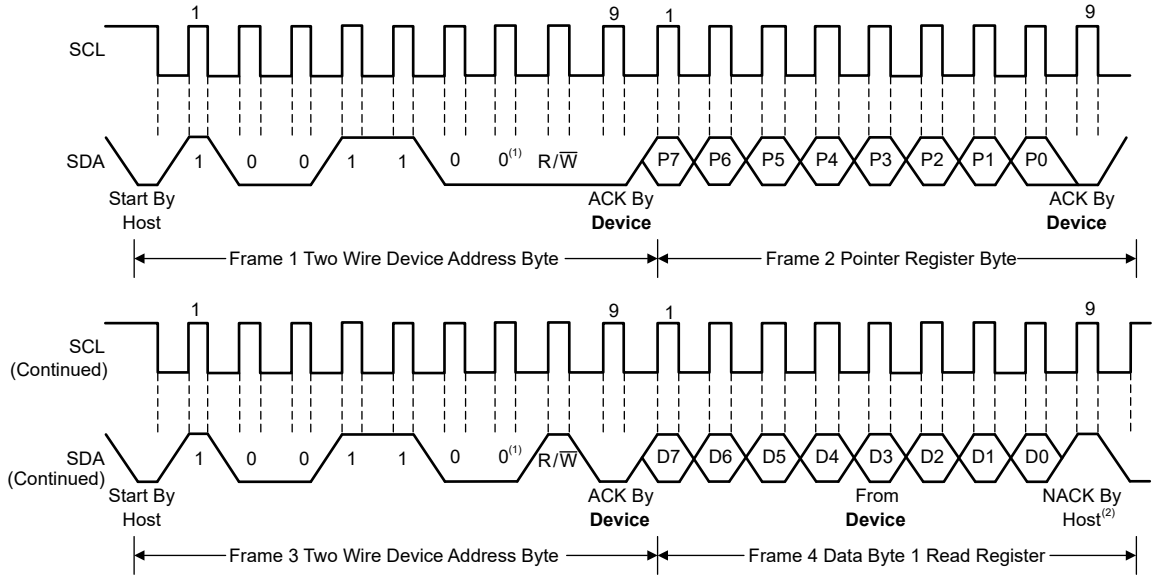
Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the controller device. The receiver acknowledges the data transfer.

Acknowledge: Each receiving device (when addressed) is required to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a controller receive, the controller signals data transfer termination by generating a not-acknowledge bit transmitted by the controller.



A. Target address 1001 100 (TMP411**A**-Q1/TMP411D**A**-Q1 and TMP411**D**-Q1/TMP411D**D**-Q1) shown. Target address changes for TMP411**B**-Q1/TMP411D**B**-Q1 and TMP411**C**-Q1/TMP411D**C**-Q1. See the *Ordering Information* table for more details.

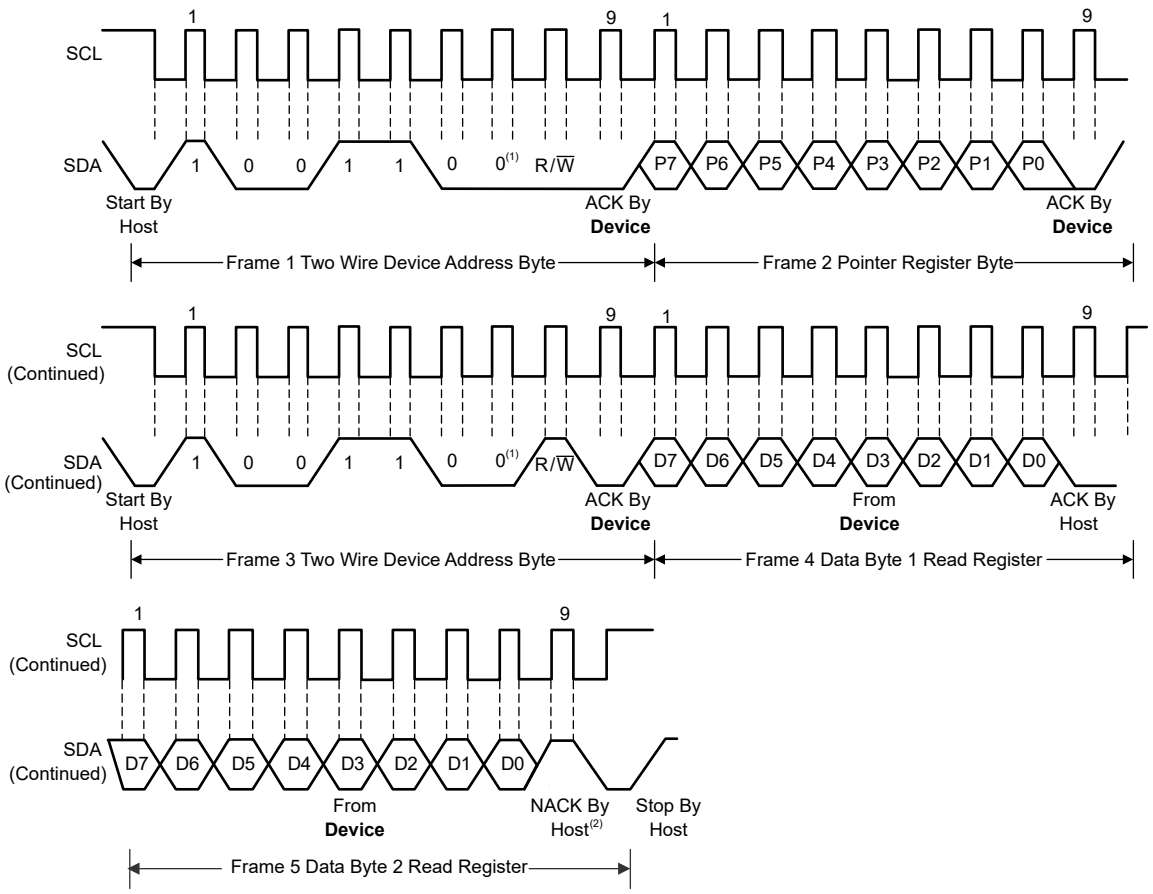
Figure 7-5. Two-Wire Timing Diagram for Write Word Format



A. Target address 1001 100 (TMP411**A**-Q1/TMP411D**A**-Q1 and TMP411**D**-Q1/TMP411D**D**-Q1) shown. Target address changes for TMP411**B**-Q1/TMP411D**B**-Q1 and TMP411**C**-Q1/TMP411D**C**-Q1. See the *Ordering Information* table for more details.

B. The host must leave SDA high to terminate a single-byte read operation.

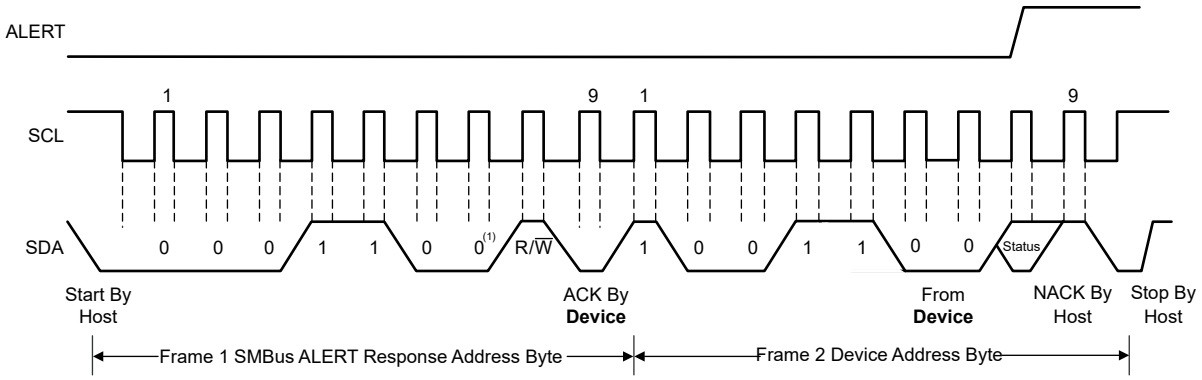
Figure 7-6. Two-Wire Timing Diagram for Single-Byte Read Format



A. Target address 1001 100 (TMP411**A**-Q1/TMP411D**A**-Q1 and TMP411**D**-Q1/TMP411D**D**-Q1) shown. Target address changes for TMP411**B**-Q1/TMP411D**B**-Q1 and TMP411**C**-Q1/TMP411D**C**-Q1. See the *Ordering Information* table for more details.

B. The host must leave SDA high to terminate a two−byte read operation.

Figure 7-7. Two-Wire Timing Diagram for Two-Byte Read Format



A. Target address 1001 100 (TMP411**A**-Q1/TMP411D**A**-Q1 and TMP411**D**-Q1/TMP411D**D**-Q1) shown. Target address changes for TMP411**B**-Q1/TMP411D**B**-Q1 and TMP411**C**-Q1/TMP411D**C**-Q1. See the *Ordering Information* table for more details.

Figure 7-8. Timing Diagram for SMBus $\overline{\text{ALERT}}$

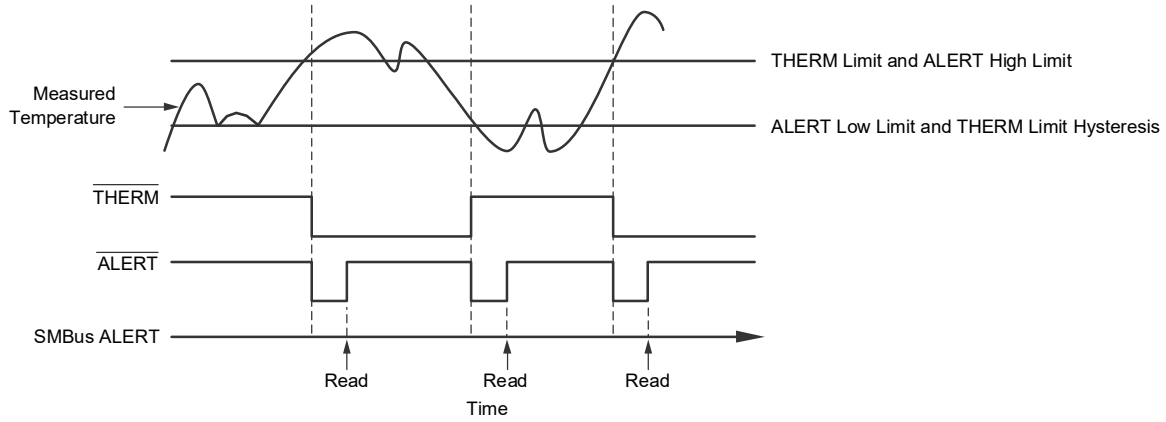


Figure 7-9. SMBus Alert Timing Diagram

7.5.4 Serial Bus Address

To communicate with the TMP411-Q1 and TMP411D-Q1, the controller must first address target devices through a target address byte. The target address byte consists of seven address bits and a direction bit that indicates whether the operation is read or write. The addresses of the TMP411A-Q1 and TMP411DA-Q1, and the TMP411D-Q1 and TMP411DD-Q1 devices are 4Ch (1001100b).

Table 7-5. TMP411-Q1 and TMP411D-Q1 Device Address Options

DEVICE NAME	PART NUMBER	I²C BINARY ADDRESS	I²C HEX ADDRESS	DEFAULT LOCAL/ REMOTE HIGH TEMPERATURE LIMIT
TMP411-Q1 (DGK package)	TMP411**A**QDGKRQ1	100 1100b	4Ch	+85°C
	TMP411**B**QDGKRQ1	100 1101b	4Dh	+85°C
	TMP411**C**QDGKRQ1	100 1110b	4Eh	+85°C
	TMP411**D**QDGKRQ1	100 1100b	4Ch	+110°C
TMP411D-Q1 (DDF package)	TMP411D**A**QDDFRQ1	100 1100b	4Ch	+85°C
	TMP411D**B**QDDFRQ1	100 1101b	4Dh	+85°C
	TMP411D**C**QDDFRQ1	100 1110b	4Eh	+85°C
	TMP411D**D**QDDFRQ1	100 1100b	4Ch	+110°C

7.5.5 Read/Write Operations

To access a particular register on the TMP411-Q1 and TMP411D-Q1, the appropriate value must be written to the Pointer Register. With the read and write bit low, the value for the Pointer Register is the first byte transferred after the target address byte. Every write operation to the TMP411-Q1 and TMP411D-Q1 requires a value for the Pointer Register, as shown in Figure 7-5.

When reading from the TMP411-Q1 and TMP411D-Q1 devices, the last value stored in the Pointer Register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer Register. This transaction is accomplished by issuing a target address byte with the R/W bit low, followed by the Pointer Register byte. No additional data is required. The controller then generates a START condition and sends the target address byte with the R/W bit high to initiate the read command. See Figure 7-6 for details of this sequence. Continually sending the Pointer Register bytes is not necessary if repeated reads from the same register are desired, because the TMP411-Q1 and TMP411D-Q1 devices retain the Pointer Register value until the value is changed by the next write operation. Note that the MSB sends the register bytes first, followed by the LSB.

7.5.6 Time-Out Function

When bit 7 of the Consecutive Alert Register is set high, the TMP411-Q1 and TMP411D-Q1 time-out function is enabled. The TMP411-Q1 and TMP411D-Q1 reset the serial interface if either SCL or SDA is held low for 30ms

(typical) between a START and STOP condition. If the TMP411-Q1 and TMP411D-Q1 devices are holding the bus low, the devices release the bus and wait for a START condition. Maintaining a communication speed of at least 1kHz for the SCL operating frequency is necessary to avoid activating the timeout function. The default state of the timeout function is enabled (bit 7 = high).

7.5.7 High-Speed Mode

For the two-wire bus to operate at frequencies above 400kHz, the controller device must issue a high-speed mode (Hs-mode) controller code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP411-Q1 and TMP411D-Q1 devices do not acknowledge this byte, but switch the input filters on SDA and SCL lines, switch the output filter on SDA to operate in Hs-mode, which allows transfers at up to 3.4MHz. After the Hs-mode controller code is issued, the controller transmits a two-wire target address to initiate a data transfer operation. The bus operates in Hs-mode until a STOP condition occurs on the bus. The TMP411-Q1 and TMP411D-Q1 devices switch the input and output filter after receiving the STOP condition.

7.5.8 General-Call Reset

The TMP411-Q1 and TMP411D-Q1 devices support a reset through the two-wire general-call address 00h (0000 0000b). The TMP411-Q1 and TMP411D-Q1 devices acknowledge the general-call address and respond to the second byte. If the second byte is 06h (0000 0110b), the TMP411-Q1 and TMP411D-Q1 execute a software reset. This software reset restores the power-on-reset state to all TMP411-Q1 and TMP411D-Q1 registers, aborts any conversion in progress, and clears the $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins. The TMP411-Q1 and TMP411D-Q1 do not respond to other values in the second byte.

7.5.9 Software Reset

The TMP411-Q1 and TMP411D-Q1 reset by writing any value to Pointer Register FCh. This restores the power-on-reset state to all of the TMP411-Q1 and TMP411D-Q1 registers, aborts any conversion in process, and clears the $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins.

7.5.10 SMBUS Alert Function

The TMP411-Q1 and TMP411D-Q1 support the SMBus alert function. When pin 6 is configured as an alert output, the $\overline{\text{ALERT}}$ pin of the TMP411-Q1 and TMP411D-Q1 can be connected as an SMBus alert signal. When a controller detects an alert condition on the ALERT line, the controller sends an SMBus alert command (0001 1001) on the bus. If the $\overline{\text{ALERT}}$ pin of the TMP411-Q1 and TMP411D-Q1 devices is active, the device acknowledges the SMBus alert command and returns the target address on the SDA line. The eighth bit (LSB) of the target address byte indicates whether the temperature exceeding one of the temperature high limit settings or falling below one of the temperature low limit settings caused the alert condition. The bit is high if the temperature is greater than one of the temperature high limit settings; the bit is low if the temperature is less than or equal to one of the temperature low limit settings. See Figure 7-9 for details of this sequence.

If multiple devices on the bus respond to the SMBus alert command, arbitration during the target address portion of the SMBus alert command determines which device clears the alert status. If the TMP411-Q1 and TMP411D-Q1 win the arbitration, the $\overline{\text{ALERT}}$ pin becomes inactive at the completion of the SMBus alert command. If the TMP411-Q1 and TMP411D-Q1 devices lose the arbitration, the $\overline{\text{ALERT}}$ pin remains active.

8 Register Map

Table 8-1. Register Map Summary

POINTER ADDRESS (HEX)		POWER-ON RESET (HEX) FOR A,B, AND C	POWER-ON RESET (HEX) FOR D	BIT DESCRIPTIONS								REGISTER DESCRIPTIONS
READ	WRITE			D7	D6	D5	D4	D3	D2	D1	D0	
00	NA[1]	00	00	LT11	LT10	LT9	LT8	LT7	LT6	LT5	LT4	Local Temperature (High Byte)
01	NA	00	00	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	Remote Temperature (High Byte)
02	NA	XX	XX	BUSY	LHIGH	LLOW	RHIGH	RLOW	OPEN	RTHRM	LTHRM	Status Register
03	09	00	00	MASK1	SD	AL/TH	0	0	RANGE	0	0	Configuration Register
04	0A	08	08	0	0	0	0	R3	R2	R1	R0	Conversion Rate Register
05	0B	55	6E	LTH11	LTH10	LTH9	LTH8	LTH7	LTH6	LTH5	LTH4	Local Temperature High Limit (High Byte)
06	0C	00	00	LTL11	LTL10	LTL9	LTL8	LTL7	LTL6	LTL5	LTL4	Local Temperature Low Limit (High Byte)
07	0D	55	6E	RTH11	RTH10	RTH9	RTH8	RTH7	RTH6	RTH5	RTH4	Remote Temperature High Limit (High Byte)
08	0E	00	00	RTL11	RTL10	RTL9	RTL8	RTL7	RTL6	RTL5	RTL4	Remote Temperature Low Limit (High Byte)
NA	0F	XX	XX	X[2]	X	X	X	X	X	X	X	One-Shot Start
10	NA	00	00	RT3	RT2	RT1	RT0	0	0	0	0	Remote Temperature (Low Byte)
13	13	00	00	RTH3	RTH2	RTH1	RTH0	0	0	0	0	Remote Temperature High Limit (Low Byte)
14	14	00	00	RTL3	RTL2	RTL1	RTL0	0	0	0	0	Remote Temperature Low Limit (Low Byte)
15	NA	00	00	LT3	LT2	LT1	LT0	0	0	0	0	Local Temperature (Low Byte)
16	16	00	00	LTH3	LTH2	LTH1	LTH0	0	0	0	0	Local Temperature High Limit (Low Byte)
17	17	00	00	LTL3	LTL2	LTL1	LTL0	0	0	0	0	Local Temperature Low Limit (Low Byte)
18	18	00	00	NC7	NC6	NC5	NC4	NC3	NC2	NC1	NC0	N-factor Correction
19	19	55	6E	RTHL11	RTHL10	RTHL9	RTHL8	RTHL7	RTHL6	RTHL5	RTHL4	Remote $\overline{\text{THERM}}$ Limit
1A	1A	1C	1C	0	0	0	1	1	1	RES1	RES0	Resolution Register
20	20	55	6E	LTHL11	LTHL10	LTHL9	LTHL8	LTHL7	LTHL6	LTHL5	LTHL4	Local $\overline{\text{THERM}}$ Limit
21	21	0A	0A	TH11	TH10	TH9	TH8	TH7	TH6	TH5	TH4	$\overline{\text{THERM}}$ Hysteresis
22	22	81	81	TO_EN	0	0	0	C2	C1	C0	1	Consecutive Alert Register
30	30	FF	FF	LMT11	LMT10	LMT9	LMT8	LMT7	LMT6	LMT5	LMT4	Local Temperature Minimum (High Byte)
31	31	F0	F0	LMT3	LMT2	LMT1	LMT0	0	0	0	0	Local Temperature Minimum (Low Byte)
32	32	00	00	LXT11	LXT10	LXT9	LXT8	LXT7	LXT6	LXT5	LXT4	Local Temperature Maximum (High Byte)
33	33	00	00	LXT3	LXT2	LXT1	LXT0	0	0	0	0	Local Temperature Maximum (Low Byte)
34	34	FF	FF	RMT11	RMT10	RMT9	RMT8	RMT7	RMT6	RMT5	RMT4	Remote Temperature Minimum (High Byte)

Table 8-1. Register Map Summary (continued)

POINTER ADDRESS (HEX)		POWER-ON RESET (HEX) FOR A,B, AND C	POWER-ON RESET (HEX) FOR D	BIT DESCRIPTIONS								REGISTER DESCRIPTIONS
READ	WRITE			D7	D6	D5	D4	D3	D2	D1	D0	
35	35	F0	F0	RMT3	RMT2	RMT1	RMT0	0	0	0	0	Remote Temperature Minimum (Low Byte)
36	36	00	00	RXT11	RXT10	RXT9	RXT8	RXT7	RXT6	RXT5	RXT4	Remote Temperature Maximum (High Byte)
37	37	00	00	RXT3	RXT2	RXT1	RXT0	0	0	0	0	Remote Temperature Maximum (Low Byte)
NA	FC	XX	XX	X(2)	X	X	X	X	X	X	X	Software Reset
FE	NA	55	55	0	1	0	1	0	1	0	1	Manufacturer ID
FF	NA	12	12	0	0	0	1	0	0	1	0	Device ID for TMP411**A**-Q1/TMP411D**A**-Q1
FF	NA	13	13	0	0	0	1	0	0	1	1	Device ID for TMP411**B**-Q1/TMP411D**B**-Q1
FF	NA	10	10	0	0	0	1	0	0	0	0	Device ID for TMP411**C**-Q1/TMP411D**C**-Q1

(1) NA = not applicable; register is write- or read-only
(2) X = indeterminate state

8.1 Register Information

The TMP411-Q1 and TMP411D-Q1 contains multiple registers for holding configuration information, temperature measurement results, temperature comparator maximum and minimum limits, and status information. These registers are described in Figure 8-1 and Table 8-1.

8.2 Pointer Register

Figure 8-1 shows the internal register structure of the TMP411-Q1 and TMP411D-Q1. The 8-bit Pointer Register is used to address a given data register. The Pointer Register identifies which of the data registers must respond to a read or write command on the two-wire bus. This register is set with every write command. A write command must be issued to set the proper value in the Pointer Register before executing a read command. Table 8-1 describes the pointer address of the registers available in the TMP411-Q1 and TMP411D-Q1. Please note the read pointer addresses 0x05, 0x07, 0x19, and 0x20 have different power-on-reset values for A, B, C vs D. The power-on-reset (POR) value of the Pointer Register is 00h (0000 0000b).

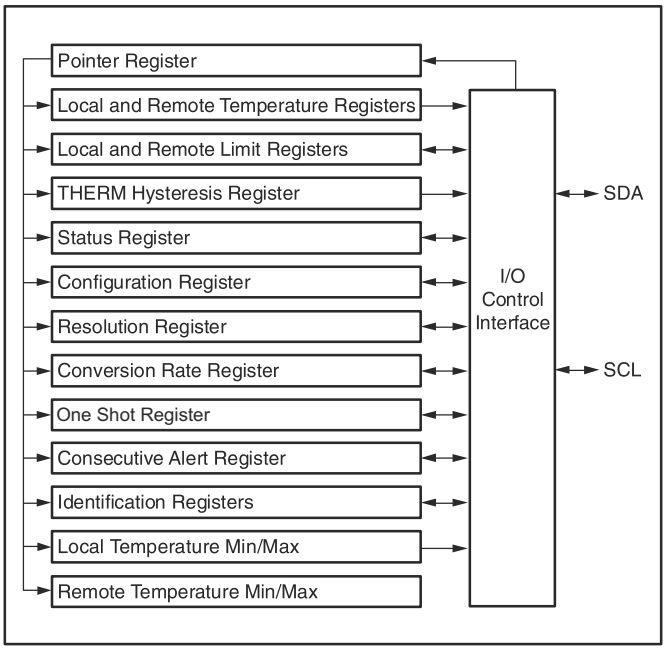


Figure 8-1. Internal Register Structure

8.3 Temperature Registers

The TMP411-Q1 and TMP411D-Q1 have four 8-bit registers that hold temperature measurement results. Both the local channel and the remote channel have a high byte register that contains the most significant bits (MSBs) of the temperature analog-to-digital converter (ADC) result and a low-byte register that contains the least significant bits (LSBs) of the temperature ADC result. The local channel high byte address is 00h; the local channel low byte address is 15h. The remote channel high byte is at address 01h; the remote channel low byte address is 10h. These registers are read-only and are updated by the ADC each time a temperature measurement is completed.

The TMP411-Q1 and TMP411D-Q1 contain circuitry to verify that a low byte register read command returns data from the same ADC conversion as the immediately preceding high byte read command. This verification remains valid only until another register is read. For proper operation, the high byte of a temperature register must be read first. The low byte register must be read in the next read command. The low byte register can be left unread if the LSBs are not needed. Alternatively, the temperature registers can be read as a 16-bit register by using a single two-byte read command from address 00h for the local channel result or from address 01h for the remote channel result. The high byte is read first, followed by the low byte. Both bytes of this read operation are from the same ADC conversion. The power-on-reset value of both temperature registers is 00h.

8.4 Limit Registers

The TMP411-Q1 and TMP411D-Q1 have 11 registers for setting comparator limits for both the local and remote measurement channels. These registers have read and write capability. The High and Low Limit Registers for both channels span two registers, as do the temperature registers. The local temperature high limit is set by writing the high byte to pointer address 0Bh and writing the low byte to pointer address 16h, or by using a single two-byte write command (high byte first) to pointer address 0Bh. The local temperature high limit is obtained by reading the high byte from pointer address 05h and the low byte from pointer address 16h or by using a two-byte read command from pointer address 05h. The power-on-reset value of the local temperature high limit is 55h/6Eh/00h (85°C in standard temperature mode for TMP411A-Q1/TMP411DA-Q1 to TMP411C-Q1/TMP411DC-Q1; 110°C in standard temperature mode for TMP411D-Q1/TMP411DD-Q1, 21°C in extended temperature range).

Similarly, the local-temperature low limit is set by writing the high byte to pointer address 0Ch and writing the low byte to pointer address 17h, or by using a single two-byte write command to pointer address 0Ch. The local temperature low limit is read by reading the high byte from pointer address 06h and the low byte from pointer address 17h, or by using a two-byte read from pointer address 06h. The power-on-reset value of the local temperature low limit register is 00h/00h (0°C in standard temperature mode; –64°C in extended mode).

The remote temperature high limit is set by writing the high byte to pointer address 0Dh and writing the low byte to pointer address 13h, or by using a two-byte write command to pointer address 0Dh. The remote temperature high limit is obtained by reading the high byte from pointer address 07h and the low byte from pointer address 13h, or by using a two-byte read command from pointer address 07h. The power-on-reset value of the Remote Temperature High Limit Register is 55h/6Eh/00h (85°C in standard temperature mode for TMP411A-Q1/TMP411DA-Q1 to TMP411C-Q1/TMP411DC-Q1; 110°C in standard temperature mode for TMP411D-Q1/TMP411DD-Q1, 21°C in extended temperature mode).

The remote temperature low limit is set by writing the high byte to pointer address 0Eh and writing the low byte to pointer address 14h, or by using a two-byte write to pointer address 0Eh. The remote temperature low limit is read by reading the high byte from pointer address 08h and the low byte from pointer address 14h, or by using a two-byte read from pointer address 08h. The power-on-reset value of the Remote Temperature Low Limit Register is 00h/00h (0°C in standard temperature mode, –64°C in extended mode).

The TMP411-Q1 and TMP411D-Q1 also have $\overline{\text{THERM}}$ limit registers for both the local and the remote channels. These registers are eight bits and allow for $\overline{\text{THERM}}$ limits set to 1°C resolution. The local channel $\overline{\text{THERM}}$ limit is set by writing to the pointer address 20h. The remote channel $\overline{\text{THERM}}$ limit is set by writing to the pointer address 19h. The local channel $\overline{\text{THERM}}$ limit is obtained by reading from pointer address 20h, and the remote channel $\overline{\text{THERM}}$ limit is read from pointer address 19h. The power-on-reset value of the $\overline{\text{THERM}}$ limit registers is 55h/6Eh/00h (85°C in standard temperature mode for TMP411A-Q1/TMP411DA-Q1 to TMP411C-Q1/TMP411DC-Q1; 110°C in standard temperature mode for TMP411D-Q1/TMP411DD-Q1; 21°C in extended temperature mode). The $\overline{\text{THERM}}$ limit comparators also have hysteresis. The hysteresis of both comparators is set by writing to the pointer address 21h. The hysteresis value is obtained by reading from pointer address 21h. The Hysteresis Register value is an unsigned number (always positive). The power-on-reset value of this register is 0Ah (10°C).

Whenever changing between standard and extended temperature ranges, note that the temperatures stored in the temperature limit registers are not automatically reformatted to correspond to the new temperature range format. These values must be reprogrammed in the appropriate binary or extended binary format.

8.5 Status Register

The TMP411-Q1 and TMP411D-Q1 have a Status Register to report the state of the temperature comparators. Table 8-2 shows the Status Register bits. The Status Register is read-only from pointer address 02h.

The BUSY bit reads as 1 if the ADC is making a conversion, and 0 if the ADC is not converting.

The OPEN bit reads as 1 if the remote transistor is detected as OPEN since the last read of the Status Register. The OPEN status is only detected when the ADC is attempting to convert a remote temperature.

The RTHRM bit reads as 1 if the remote temperature exceeds the remote $\overline{\text{THERM}}$ limit, remains greater than the remote $\overline{\text{THERM}}$ limit, and is less than the value in the shared Hysteresis Register; see Figure 7-9.

The LTHRM bit reads as 1 if the local temperature exceeds the local $\overline{\text{THERM}}$ limit, remains greater than the local $\overline{\text{THERM}}$ limit, and is less than the value in the shared Hysteresis Register; see Figure 7-9.

The LHIGH and RHIGH bit values depend on the state of the AL/TH bit in the Configuration Register. If the AL/TH bit is 0, the LHIGH bit reads as 1 if the local high limit is exceeded since the last clearing of the Status Register. The RHIGH bit reads as 1 if the remote high limit is exceeded since the last clearing of the Status Register. If the AL/TH bit is 1, the remote high limit and the local high limit are used to implement a $\overline{\text{THERM2}}$ function. LHIGH reads as 1 if the local temperature has exceeded the local high limit and remains greater than the local high limit, and less than the value in the Hysteresis Register.

The RHIGH bit reads as 1 if the remote temperature exceeds the remote high limit and remains greater than the remote high limit, and less than the value in the Hysteresis Register.

The LLOW and RLOW bits are not affected by the AL/TH bit. The LLOW bit reads as 1 if the local low limit is exceeded since the last clearing of the Status Register. The RLOW bit reads as 1 if the remote low limit is exceeded since the last clearing of the Status Register. When there is no remote diode connected and the power supply ramp rate is less than 240V/s, the RLOW flag is set, as well and must be ignored.

The values of the LLOW, RLOW, and OPEN (as well as LHIGH and RHIGH when AL/TH is 0) are latched and read as 1 until the Status Register is read or a device reset occurs. These bits are cleared by reading the Status Register, provided that the condition causing the flag to be set no longer exists. The values of BUSY, LTHRM, and RTHRM (as well as LHIGH and RHIGH when $\overline{\text{ALERT}}$/ $\overline{\text{THERM2}}$ is 1) are not latched and are not cleared by reading the Status Register. The values of BUSY, LTHRM, and RTHRM always indicate the current state, and are updated appropriately at the end of the corresponding ADC conversion. Clearing the Status Register bits does not clear the state of the $\overline{\text{ALERT}}$ pin; an SMBus alert response address command must be used to clear the $\overline{\text{ALERT}}$ pin.

The TMP411-Q1 and TMP411D-Q1 NORs LHIGH, LLOW, RHIGH, RLOW, and OPEN, so a status change for any of these flags from 0 to 1 automatically causes the $\overline{\text{ALERT}}$ pin to go low (This only applies when the $\overline{\text{ALERT}}$/ $\overline{\text{THERM2}}$ pin is configured for $\overline{\text{ALERT}}$ mode).

Table 8-2. Status Register Format

STATUS REGISTER (Read = 02h, Write = NA)								
BIT #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	BUSY	LHIGH	LLOW	RHIGH	RLOW	OPEN	RTHRM	LTHRM
POR VALUE	0(1)	0	0	0	0	0	0	0

(1) The BUSY bit changes to 1 almost immediately (<<100µs) following power up, as the TMP411-Q1 and TMP411D-Q1 begin the first temperature conversion. The BUSY bit is high whenever the TMP411-Q1 and TMP411D-Q1 devices are converting a temperature reading.

8.6 Configuration Register

The Configuration Register sets the temperature range, controls Shutdown mode, and determines how the $\overline{\text{ALERT}}$/ $\overline{\text{THERM2}}$ pin functions. The Configuration Register is set by writing to pointer address 09h and by reading from pointer address 03h.

The MASK bit (bit 7) enables or disables the $\overline{\text{ALERT}}$ pin output if AL/TH = 0. If AL/TH = 1, then the MASK bit has no effect. If MASK is set to 0, the $\overline{\text{ALERT}}$ pin goes low when one of the temperature measurement channels exceeds the high or low limits for the selected number of consecutive conversions. If the MASK bit is set to 1, the TMP411-Q1 and TMP411D-Q1 retain the $\overline{\text{ALERT}}$ pin status, but the $\overline{\text{ALERT}}$ pin does not go low.

The shutdown (SD) bit (bit 6) enables or disables the temperature measurement circuitry. If SD = 0, the TMP411-Q1 and TMP411D-Q1 convert continuously at the rate set in the conversion rate register. When SD is set to 1, the TMP411-Q1 and TMP411D-Q1 immediately stop converting and enter a Shutdown mode. When SD

is set to 0 again, the TMP411-Q1 and TMP411D-Q1 resume continuous conversions. A single conversion can be started by writing to the One-Shot Register when SD = 1.

The AL/TH bit (bit 5) controls whether the $\overline{\text{ALERT}}$ pin functions in $\overline{\text{ALERT}}$ mode or $\overline{\text{THERM2}}$ mode. If AL/TH = 0, the $\overline{\text{ALERT}}$ pin operates as an interrupt pin. In this mode, the $\overline{\text{ALERT}}$ pin goes low after the set number of consecutive out-of-limit temperature measurements occurs.

If AL/TH = 1, the $\overline{\text{ALERT}}$/ $\overline{\text{THERM2}}$ pin implements a THERM function ($\overline{\text{THERM2}}$). In this mode, $\overline{\text{THERM2}}$ functions similarly to the $\overline{\text{THERM}}$ pin except that the local high limit and remote high limit registers are used for the thresholds. $\overline{\text{THERM2}}$ goes low when either RHIGH or LHIGH is set.

The temperature range is set by configuring bit 2 of the Configuration Register. Setting this bit low configures the TMP411-Q1 and TMP411D-Q1 devices for the standard measurement range (0°C to 127°C). Temperature conversions are stored in the standard binary format. Setting bit 2 high configures the TMP411-Q1 and TMP411D-Q1 for the extended measurement range (–55°C to 150°C). Temperature conversions are stored in the extended binary format (see Table 7-1).

The remaining bits of the Configuration Register are reserved and must always be set to 0. The power-on-reset value for this register is 00h. Table 8-3 summarizes the bits of the Configuration Register.

Note

The TMP411**x**-Q1/TMP411D**x**-Q1 device family is set to the standard temperature range as the default. Therefore, the device always needs to be configured to the extended temperature range after power-up if this feature is used.

Table 8-3. Configuration Register Bit Descriptions

CONFIGURATION REGISTER (Read = 03h, Write = 09h, POR = 00h)			
BIT	**NAME**	**FUNCTION**	**POWER-ON RESET VALUE**
7	MASK	0 = $\overline{\text{ALERT}}$ enabled; 1 = $\overline{\text{ALERT}}$ masked	0
6	SD	0 = Run; 1 = Shut down	0
5	AL/TH	0 = $\overline{\text{ALERT}}$ mode; 1 = $\overline{\text{THERM}}$ mode	0
4, 3	Reserved	—	0
2	Temperature range	0 = 0°C to 127°C; 1 = –55°C to 150°C	0
1, 0	Reserved	—	0

8.7 Resolution Register

The RES1 and RES0 bits (resolution bits 1 and 0) of the Resolution Register set the resolution of the local temperature measurement channel. Remote temperature measurement channel resolution is not affected. Changing the local channel resolution also affects the conversion time and rate of the TMP411-Q1 only. The Resolution Register is set by writing to pointer address 1Ah and is read from pointer address 1Ah. Table 8-4 shows the resolution bits for the Resolution Register.

Table 8-4. Resolution Register: Local Channel Programmable Resolution

RESOLUTION REGISTER (Read = 1Ah, Write = 1Ah, POR = 1Ch)				
RES1	**RES0**	**RESOLUTION**	**CONVERSION TIME (TYPICAL) TMP411-Q1 (Legacy chip)**	**CONVERSION TIME (TYPICAL) TMP411-Q1 (New chip) TMP411D-Q1**
0	0	9 bits (0.5°C)	12.5ms	17.7ms
0	1	10 bits (0.25°C)	25ms	17.7ms
1	0	11 bits (0.125°C)	50ms	17.7ms
1	1	12 bits (0.0625°C)	100ms	17.7ms

Bits 2 through 4 of the Resolution Register must always be set to 1. Bits 5 through 7 of the Resolution Register must always be set to 0. The power-on-reset value of this register is 1Ch.

8.8 Conversion Rate Register

The Conversion Rate Register controls the rate at which temperature conversions are performed. This register adjusts the idle time between conversions but not the conversion timing, thereby allowing TMP411-Q1 and TMP411D-Q1 power dissipation to be balanced with the temperature register update rate. Table 8-5 shows the conversion rate options and corresponding current consumption.

Table 8-5. Conversion Rate Register

CONVERSION RATE REGISTER (Read = 04h, Write = 0Ah, POR = 08h)											
R7	R6	R5	R4	R3	R2	R1	R0	CONVERSIONS PER SECOND	AVERAGE IQ (TYPICAL) (µA) TMP411-Q1 (Legacy chip)		AVERAGE IQ (TYPICAL) (µA) TMP411-Q1 (New chip) TMP411D-Q1
									V+ = 2.7V	V+ = 5.5V	V+ = 2.7V and 5.5V
0	0	0	0	0	0	0	0	0.0625	11	32	1.5
0	0	0	0	0	0	0	1	0.125	17	38	1.8
0	0	0	0	0	0	1	0	0.25	28	49	2.5
0	0	0	0	0	0	1	1	0.5	47	69	3.8
0	0	0	0	0	1	0	0	1	80	103	6.5
0	0	0	0	0	1	0	1	2	128	155	12
0	0	0	0	0	1	1	0	4	190	220	23
07h to 0Fh								8	373	413	45

8.9 N-factor Correction Register

The TMP411-Q1 and TMP411D-Q1 allow for a different *n*-factor value to be used for converting remote channel measurements to temperature. The remote channel uses sequential current excitation to extract a differential V_{BE} voltage measurement to determine the temperature of the remote transistor. Equation 1 relates this voltage and temperature.

$$V_{BE2} - V_{BE1} = \frac{nkT}{q} \times \ln\left(\frac{I_2}{I_1}\right) \quad (1)$$

The value *n* is a characteristic of the particular transistor used for the remote channel. The default value for the TMP411-Q1 and TMP411D-Q1 devices is *n* = 1.008. The value in the N-Factor Correction Register can be used to adjust the effective n-factor according to Equation 2 and Equation 3.

$$n_{eff} = \frac{1.008 \times 300}{300 - N_{ADJUST}} \quad (2)$$

$$N_{ADJUST} = 300 - \frac{300 \times 1.008}{n_{eff}} \quad (3)$$

The *n*-correction value must be stored in two's-complement format, yielding an effective data range from −128 to 127, as shown in Table 8-6. The n-correction value can be written to and read from pointer address 18h. The register power-on-reset value is 00h, which is not affected unless the value is written to.

Table 8-6. N-Factor Range

N_{ADJUST}			N
BINARY	HEX	DECIMAL	
0111 1111	7F	127	1.747977
0000 1010	0A	10	1.042759
0000 1000	08	8	1.035616
0000 0110	06	6	1.028571

Table 8-6. N-Factor Range (continued)

N_{ADJUST}			N
BINARY	HEX	DECIMAL	
0000 0100	04	4	1.021622
0000 0010	02	2	1.014765
0000 0001	01	1	1.011371
0000 0000	00	0	1.008
1111 1111	FF	−1	1.004651
1111 1110	FE	−2	1.001325
1111 1100	FC	−4	0.994737
1111 1010	FA	−6	0.988235
1111 1000	F8	−8	0.981818
1111 0110	F6	−10	0.975484
1000 0000	80	−128	0.706542

8.10 Minimum and Maximum Registers

The TMP411-Q1 and TMP411D-Q1 stores the minimum and maximum temperature measured since power on, chip reset, or minimum and maximum register reset for both the local and remote channels. The Local Temperature Minimum Register is read with the high byte from pointer address 30h, and the low byte is read from pointer address 31h. The Local Temperature Minimum Register is read with a two-byte read command from pointer address 30h. The Local Temperature Minimum Register resets at power-on by executing the chip-reset command, or by writing any value to any of the pointer addresses 30h through 37h. The reset value for these registers is FFh/F0h.

The Local Temperature Maximum Register is read with the high byte from pointer address 32h and the low byte from pointer address 33h. The Local Temperature Maximum Register is read with a two-byte read command from pointer address 32h. The Local Temperature Maximum Register resets at power-on by executing the chip reset command, or by writing any value to any of the pointer addresses 30h through 37h. The reset value for these registers is 00h/00h.

The Remote Temperature Minimum Register is read with the high byte from pointer address 34h and the low byte from pointer address 35h. The Remote Temperature Minimum Register is read with a two-byte read command from pointer address 34h. The Remote Temperature Minimum Register resets at power-on by executing the chip reset command, or by writing any value to any of the pointer addresses 30h through 37h. The reset value for these registers is FFh/F0h.

The Remote Temperature Maximum Register is read with the high byte from pointer address 36h and the low byte from pointer address 37h. The Remote Temperature Maximum Register is read with a two-byte read command from pointer address 36h. The Remote Temperature Maximum Register resets at power-on by executing the chip reset command, or by writing any value to any of the pointer addresses 30h through 37h. The reset value for these registers is 00h/00h.

8.11 Consecutive Alert Register

The value in the Consecutive Alert Register (address 22h) determines how many consecutive out-of-limit measurements must occur on a measurement channel before the $\overline{\text{ALERT}}$ signal is activated. The value in this register does not affect bits in the Status Register. Values of one, two, three, or four consecutive conversions can be selected; one conversion is the default. This function allows additional filtering for the $\overline{\text{ALERT}}$ pin. The consecutive alert bits are shown in Table 8-7.

Table 8-7. Consecutive Alert Register

CONSECUTIVE ALERT REGISTER (READ = 22h, WRITE = 22h, POR = 01h)			
C2	C1	C0	NUMBER OF CONSECUTIVE OUT OF LIMIT MEASUREMENTS
0	0	0	1

Table 8-7. Consecutive Alert Register (continued)

CONSECUTIVE ALERT REGISTER (READ = 22h, WRITE = 22h, POR = 01h)			
C2	C1	C0	NUMBER OF CONSECUTIVE OUT OF LIMIT MEASUREMENTS
0	0	1	2
0	1	1	3
1	1	1	4

Note

Bit 7 of the Consecutive Alert Register controls the enable/disable of the timeout function. See the Timeout Function section for a description of this feature.

8.12 $\overline{\text{THERM}}$ Hysteresis Register

The $\overline{\text{THERM}}$ Hysteresis Register, shown in Table 8-9, stores the hysteresis value used for the $\overline{\text{THERM}}$ pin alarm function. This register must be programmed with a value that is less than the Local Temperature High Limit Register value, Remote Temperature High Limit Register value, Local THERM Limit Register value, or Remote THERM Limit Register value; otherwise, the respective temperature comparator does not trip on the measured temperature falling edges. Allowable hysteresis values are shown in Table 8-8. The default hysteresis value is 10°C, whether the device is operating in the standard or extended mode setting.

Table 8-8. Allowable $\overline{\text{THERM}}$ Hysteresis Values

TEMPERATURE (°C)	$\overline{\text{THERM}}$ HYSTERESIS VALUES	
	TH[11:4] (STANDARD BINARY)	(HEX)
0	0000 0000	00
1	0000 0001	01
5	0000 0101	05
10	0000 1010	0A
25	0001 1001	19
50	0011 0010	32
75	0100 1011	4B
100	0110 0100	64
125	0111 1101	7D
127	0111 1111	7F
150	1001 0110	96
175	1010 1111	AF
200	1100 1000	C8
225	1110 0001	E1
255	1111 1111	FF

Table 8-9. $\overline{\text{THERM}}$ Hysteresis Register Format

$\overline{\text{THERM}}$ HYSTERESIS REGISTER (Read = 21h, Write = 21h, POR = 0Ah)								
BIT #	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	TH11	TH10	TH9	TH8	TH7	TH6	TH5	TH4
POR VALUE	0	0	0	0	1	0	1	0

8.13 Identification Registers

The TMP411-Q1 and TMP411D-Q1 allow for the two-wire bus controller to query the device for manufacturer and device identification. This feature allows for software identification of the device at a particular two-wire

bus address. The manufacturer ID is obtained by reading from the pointer address FEh. The TMP411-Q1 and TMP411D-Q1 manufacturer code is 55h. The device ID depends on the specific model; see the Register Map (Table 8-1). These registers are read-only.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TMP411-Q1 and TMP411D-Q1 only require a transistor connected between the D+ and D– pins for remote temperature measurement. Tie the D+ pin to D- if the remote channel is not used and only the local temperature is measured. The SDA, $\overline{\text{ALERT}}$, and $\overline{\text{THERM}}$ pins (and SCL, if driven by an open-drain output) require pullup resistors as part of the communication bus. TI recommends using a 0.1µF power-supply decoupling capacitor for local bypassing. Figure 9-1 illustrates the typical configurations for the TMP411-Q1 and TMP411D-Q1. For V+ ≥ 2.7V as shown in Figure 9-1, TMP411-Q1 and TMP411D-Q1 digital pins (4, 6, 7, and 8) can be connected to a separate I^{2}C pullup and supply voltage due to fixed logic input voltages. However, for V+ < 2.7V as shown in Figure 9-2, TMP411D-Q1 digital pins (SCL, SDA) must be connected to an equal I^{2}C pullup and supply voltage due to ratiometric logic input voltages (30%/70% of V+ pin).

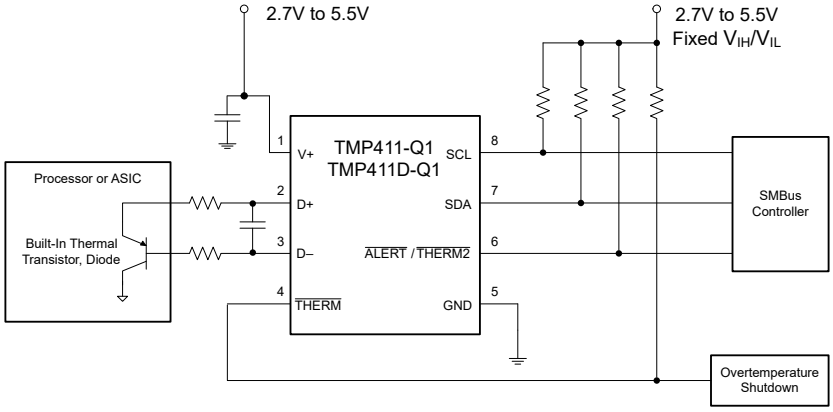


Figure 9-1. TMP411-Q1 and TMP411D-Q1 Simplified Block Diagram (Separate I^{2}C Pullup and Supply Voltage Application While V+ ≥ 2.7V)

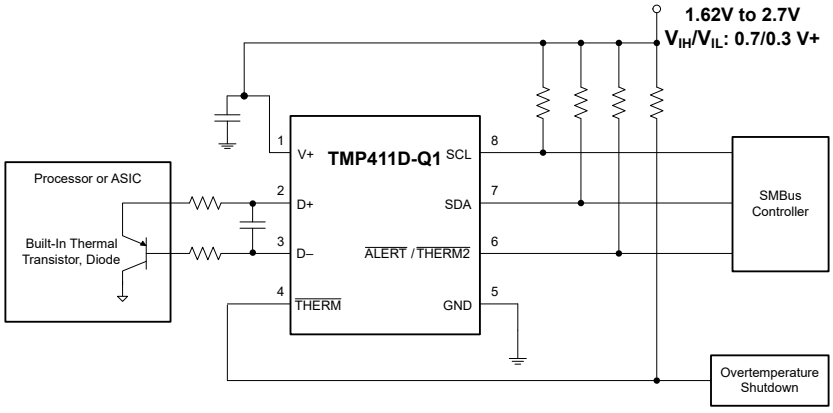


Figure 9-2. TMP411D-Q1 Simplified Block Diagram (Equal I^{2}C Pullup and Supply Voltage Application While V+ < 2.7V)

9.2 Typical Application

9.2.1 Design Requirements

The TMP411-Q1 and TMP411D-Q1 devices are designed to be used with discrete transistors or substrate transistors built into processor chips and ASICs. NPN or PNP transistors can be used, as long as the base-emitter junction is the remote temperature sensor. A transistor or diode connection can be used, as shown in Figure 7-1. The D+ pin waveform is shown in Figure 9-3 while a transistor is connected between the D+ and D– pins. Due to the three different source currents used in Section 7.2, the D+ waveform has three levels of voltage during temperature conversion.

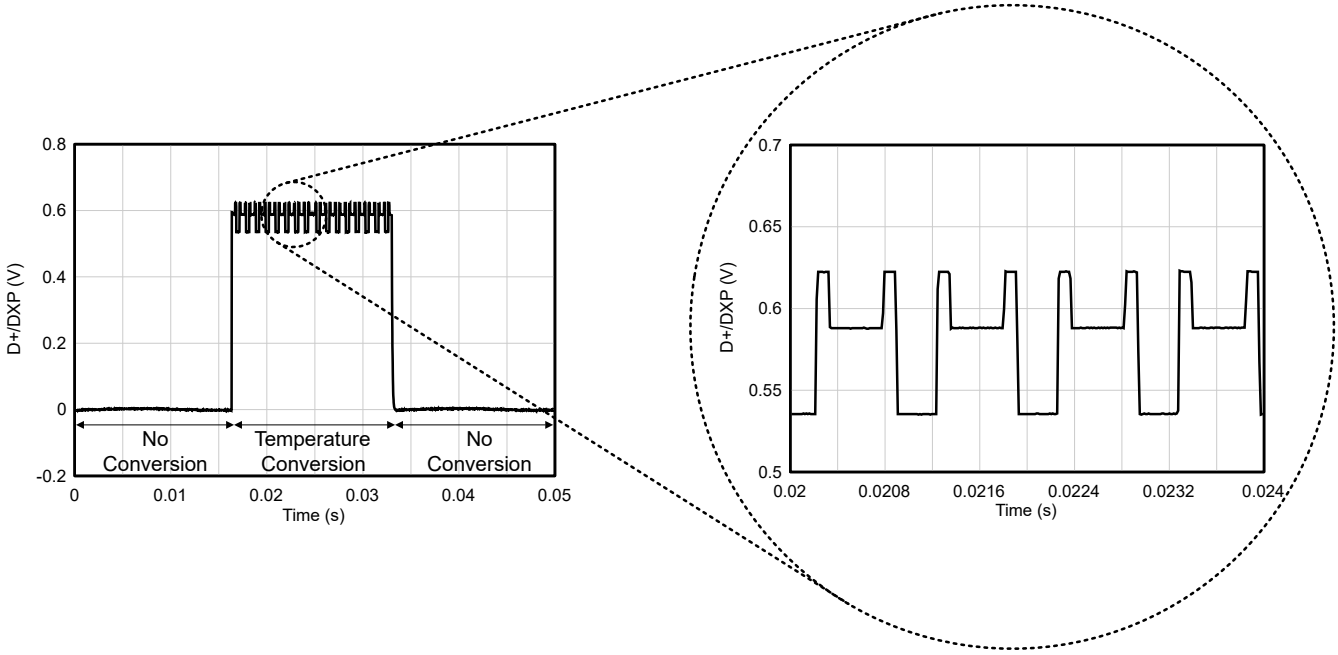


Figure 9-3. D+ Waveform

Errors in remote temperature sensor readings are the result of the ideality factor and current excitation from the TMP411-Q1 and TMP411D-Q1 versus the manufacturer-specified operating current for a given transistor. Some manufacturers specify a high-level and low-level current for the temperature-sensing substrate transistors. The TMP411-Q1 and TMP411D-Q1 have an I_{LOW} value of 6µA, and an I_{HIGH} value of 120µA. The TMP411-Q1 and TMP411D-Q1 allow for different *n*-factor values, as shown in Table 8-6.

The ideality factor (*n*) is a measured characteristic of a remote temperature sensor diode compared to an ideal diode. The ideality factor reduces to a value of 1.008. For transistors with an ideality factor that does not match the TMP411-Q1 and TMP411D-Q1, Equation 4 calculates the temperature error. Note that the actual temperature (°C) must be converted to Kelvin (K) for the equation to yield the correct results.

$$T_{ERR} = \left(\frac{n - 1.008}{1.008}\right) \times \left(273.15 + T(^{\circ}C)\right) \quad \text{or} \quad T_{ERR} = \left(\frac{n_{actual} - n_{expected}}{n_{expected}}\right) \times \left(273.15 + T_{actual}(^{\circ}C)\right) \tag{4}$$

where:

- n or n_{actual} = the ideality factor of the remote temperature sensor
- T(°C) or T_{actual}(°C) = actual temperature
- $T_{ERR} = T_{reported} - T_{actual}$= device reading error due to n or $n_{actual} \neq 1.008$
- Degree delta is the same for °C and K
- $n_{expected} = 1.008$

For n = 1.004 and T(°C) = 100°C, use Equation 5:

$$T_{ERR} = \left(\frac{1.004 - 1.008}{1.008}\right) \times (273.15 + 100^{\circ}C)$$
$$T_{ERR} = -1.48^{\circ}C \quad (5)$$

If a discrete transistor is used as the remote temperature sensor, please select the transistor according to the following criteria, which results in the best accuracy.

1. Base-emitter voltage > 0.25V at 6µA, at the highest sensed temperature.
2. Base-emitter voltage < 0.95V at 120µA, at the lowest sensed temperature.
3. Base resistance < 100Ω
4. Tight control of V_{BE} characteristics is indicated by small variations in h_{FE} (that is, 50 to 150).

Based on these criteria, use two small-signal transistors, such as the 2N3904 (NPN) or 2N3906 (PNP).

9.2.2 Detailed Design Procedure

The temperature measurement accuracy of the TMP411-Q1 and TMP411D-Q1 depends on the remote or local temperature sensor being at the same temperature as the monitored system point. If the temperature sensor is not in good thermal contact with the part of the system being monitored, then there is a delay in the response of the sensor to a temperature change in the system. For remote temperature sensing applications using a substrate transistor (or a small, SOT-23 transistor) placed close to the device, this delay is typically not a concern.

The local temperature sensor inside the TMP411-Q1 and TMP411D-Q1 monitors the ambient air around the device. The thermal time constant for the TMP411-Q1 and TMP411D-Q1 devices is approximately two seconds. This constant implies that if the ambient air changes quickly by 100°C, the TMP411-Q1 and TMP411D-Q1 take approximately 10 seconds (that is, five thermal time constants) to settle within 1°C of the final value. In most applications, the TMP411-Q1 and TMP411D-Q1 package is in electrical (and thermal contact) with the printed circuit board (PCB), and is subjected to forced airflow. The accuracy of the temperature measurement directly depends on how accurately the PCB and forced airflow temperatures represent the temperature measured by the device. Additionally, the internal power dissipation of the TMP411-Q1 and TMP411D-Q1 can cause the temperature to rise above the ambient or PCB temperature. The internal power dissipated as a result of exciting the remote temperature sensor is negligible because of the small currents used.

TMP411-Q1 (Legacy Chip): For a 5.5V supply and maximum conversion rate of eight conversions per second, the TMP411-Q1 dissipates 2.2mW (PD IQ = 5.5V × 400µA). If the $\overline{\text{ALERT}}$/ $\overline{\text{THERM2}}$ and THERM pins are each sinking 1mA, an additional power of 0.8mW is dissipated (PD OUT = 1mA × 0.4V + 1mA × 0.4V = 0.8mW). Total power dissipation equals 3mW (PD IQ + PD OUT) and (with a θ_{JA} value of 150°C/W) causes the junction temperature to rise approximately 0.45°C above the ambient.

TMP411-Q1 (New Chip): For a 5.5V supply and maximum conversion rate of eight conversions per second, the TMP411-Q1 dissipates 0.248mW (PD IQ = 5.5V × 45µA). If the $\overline{\text{ALERT}}$/ $\overline{\text{THERM2}}$ and THERM pins are each sinking 1mA, an additional power of 0.8mW is dissipated (PD OUT = 1mA × 0.4V + 1mA × 0.4V = 0.8mW). Total power dissipation equals 1.048mW (PD IQ + PD OUT) and (with a θ_{JA} value of 162°C/W) causes the junction temperature to rise approximately 0.170°C above the ambient.

TMP411D-Q1: For a 5.5V supply and maximum conversion rate of eight conversions per second, the TMP411D-Q1 dissipates 0.248mW (PD IQ = 5.5V × 45µA). If the $\overline{\text{ALERT}}$/ $\overline{\text{THERM2}}$ and THERM pins are each sinking 1mA, an additional power of 0.8mW is dissipated (PD OUT = 1mA × 0.4V + 1mA × 0.4V = 0.8mW). Total power dissipation equals 1.048mW (PD IQ + PD OUT) and (with a θ_{JA} value of 182°C/W) causes the junction temperature to rise approximately 0.191°C above the ambient.

9.2.3 Application Curves

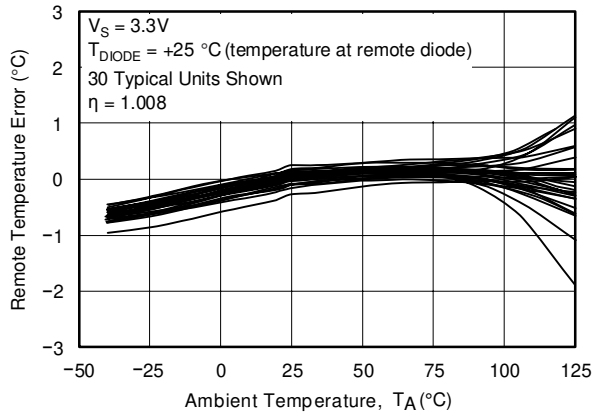


Figure 9-4. Remote Temperature Error vs TMP411-Q1 Ambient Temperature (Legacy chip)

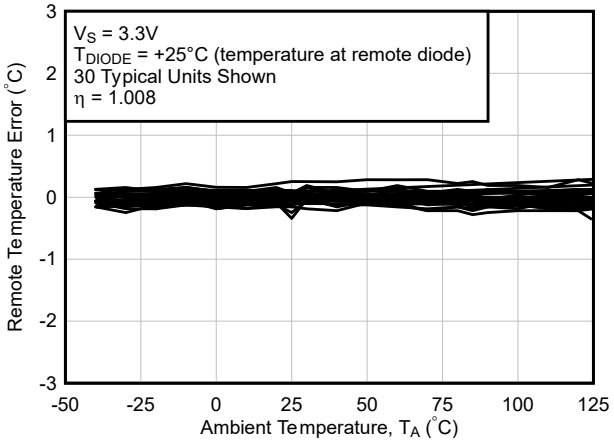


Figure 9-5. Remote Temperature Error vs TMP411-Q1 Ambient Temperature (New Chip)

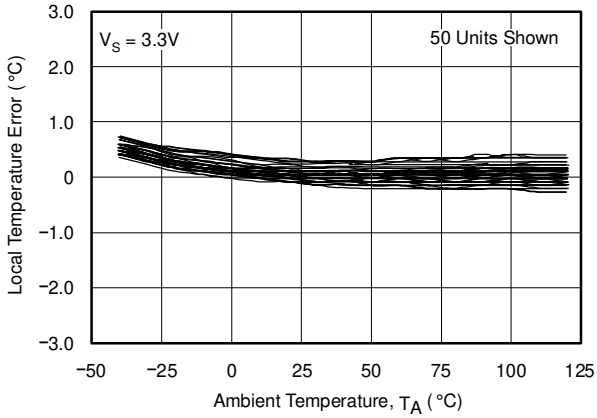


Figure 9-6. Local Temperature Error vs TMP411-Q1 Ambient Temperature (Legacy Chip)

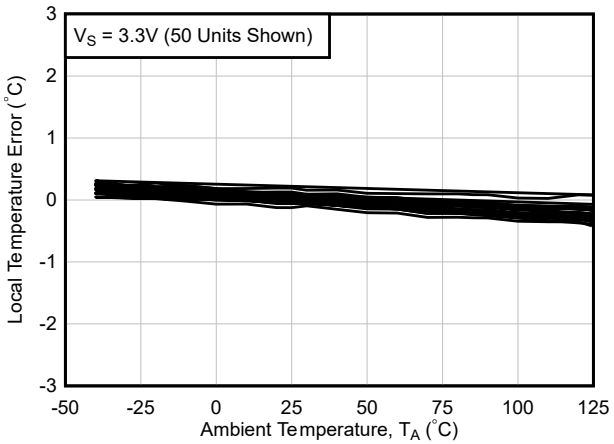


Figure 9-7. Local Temperature Error vs TMP411-Q1 Ambient Temperature (New Chip)

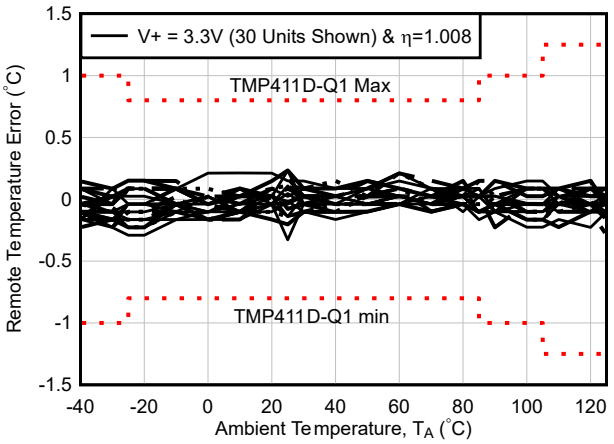


Figure 9-8. Remote Temperature Error vs TMP411D-Q1 Ambient Temperature

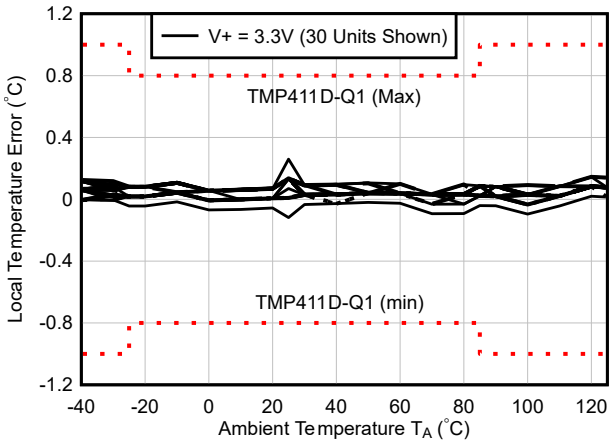


Figure 9-9. Local Temperature Error vs TMP411D-Q1 Ambient Temperature

9.3 Power Supply Recommendations

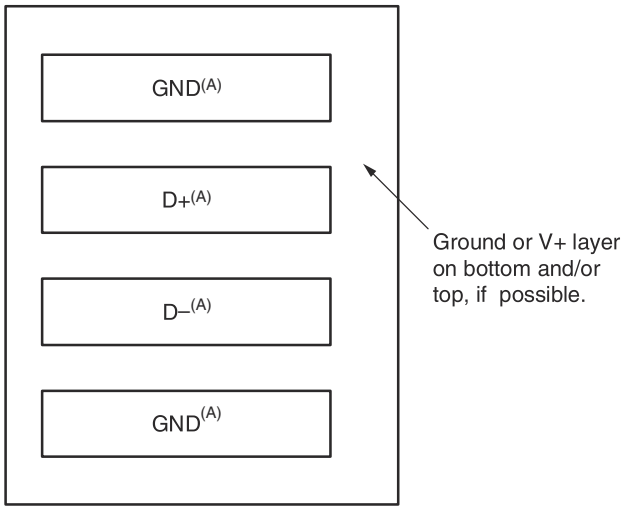
The TMP411-Q1 operates with a power supply range of 2.7V to 5.5V, while the TMP411D-Q1 power supply range of 1.62V to 5.5V. The device is optimized for operation at a 3.3V supply, but measures temperature accurately in the full supply range. TI recommends using a power supply bypass capacitor. Place the capacitor as close as possible to the supply and ground pins of the device. 0.1µF is a typical value for the supply bypass capacitor. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

9.4 Layout

9.4.1 Layout Guidelines

Remote temperature sensing on the TMP411-Q1 and TMP411D-Q1 devices measures small voltages using low currents, and therefore, noise at the device inputs must be minimized. Most applications using the TMP411-Q1 and TMP411D-Q1 devices have high digital content, with several clocks and logic-level transitions creating a noisy environment. The layout must adhere to the following guidelines:

1. Place the TMP411-Q1 and TMP411D-Q1 devices as close to the remote junction sensor as possible.
2. Route the D+ and D− traces next to each other and shield them from adjacent signals using ground guard traces, as shown in Figure 9-10. If a multilayer PCB is used, bury these traces between ground or VDD planes to shield them from extrinsic noise sources. Five-mil (0.127mm) PCB traces are recommended.
3. Minimize additional thermocouple junctions caused by copper-to-solder connections. If these junctions are used, make the same number and approximate locations of copper-to-solder connections in both the D+ and D− connections to cancel any thermocouple effects.
4. Use a 0.1µF local bypass capacitor directly between the V+ and GND of the TMP411-Q1 and TMP411D-Q1 devices, as shown in Figure 9-11. Minimize filter capacitance between D+ and D− to 1000pF or less for optimum measurement performance. This capacitance includes any cable capacitance between the remote temperature sensor and the TMP411-Q1 and TMP411D-Q1 devices.
5. If the connection between the remote temperature sensor and the TMP411-Q1 and TMP411D-Q1 devices is less than 8 inches (20cm), use a twisted-wire pair connection. Beyond 8 inches (20cm), use a twisted, shielded pair with the shield grounded as close to the TMP411-Q1 and TMP411D-Q1 devices as possible. Leave the remote sensor connection end of the shield wire open to avoid ground loops and 60Hz pickup.



A. 5mil (0.127mm) traces with 5mil (0.127mm) spacing

Figure 9-10. Example Signal Traces

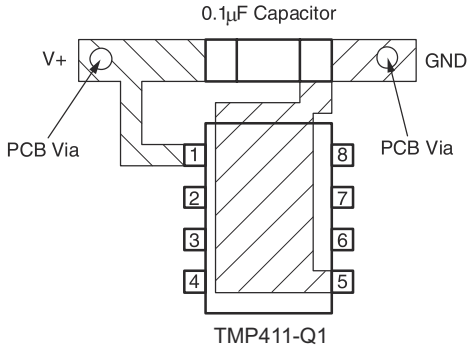


Figure 9-11. Suggested Bypass Capacitor Placement

9.4.2 Layout Example

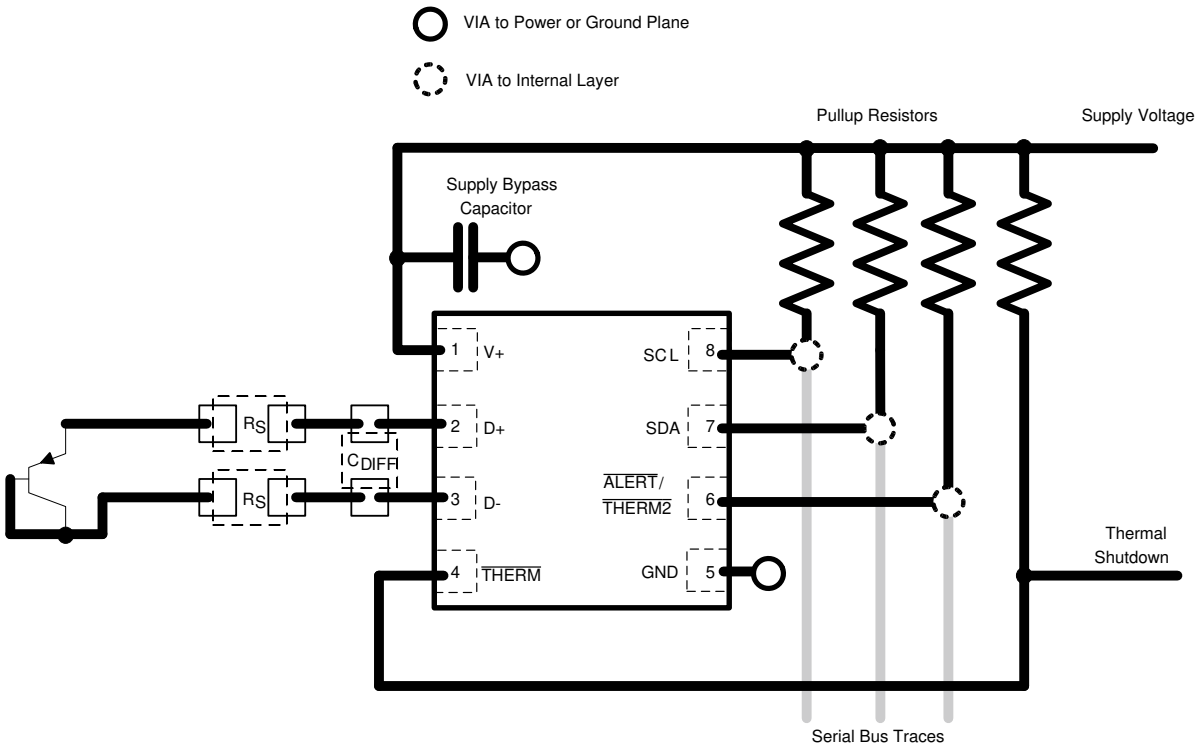


Figure 9-12. TMP411-Q1 and TMP411D-Q1 Device Layout (Equal I²C Pullup and Supply Voltage Application)

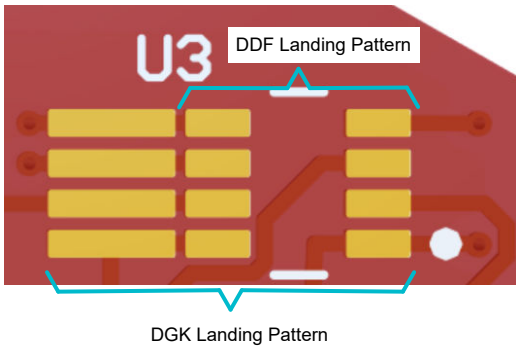


Figure 9-13. TMP411-Q1 (DGK) and TMP411D-Q1 (DDF) Devices Footprints

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

- Texas Instruments, *Optimizing Remote Temperature Sensor Design*, application note
- Texas Instruments, *TMP411-Q1 Functional Safety FIT Rate, FMD and Pin FMA*, functional safety information
- Texas Instruments, *TMP411 ±1°C and TMP411D ±0.8°C Remote and Local Temperature Sensor With N-Factor and Series Resistance Correction*, data sheet
- Texas Instruments, *TMP451-Q1 ±1°C Remote and Local Temperature Sensor With η-Factor and Offset Correction, Series-Resistance Cancellation, and Programmable Digital Filter*, data sheet
- Texas Instruments, *Remote Temperature Sensor Transistor Selection Guide*, application note
- Texas Instruments, *TMP411 Evaluation Module*, EVM

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (November 2013) to Revision G (September 2025) **Page**

- Added the TMP411D-Q1 device throughout the document; updated the data sheet title... 1
- Updated the look and feel of the document per the latest Texas Instruments and industry data sheet standards... 1
- Added "Package Information" table to the *Description* section... 1
- Added "Device Comparison" table, "Device Nomenclature" figure and description... 3
- Updated the "Conversion time" throughout the document... 3
- Changed the Average and Shutdown currents throughout the document... 3
- Added *Pin Configurations and Functions* section... 5
- Added "Type" column to *Pin Functions* table... 5
- Updated the maximum voltage ratings on D+/D- pins... 6
- Updated the maximum voltage rating on pins 4, 6, 7, 8... 6
- Updated the maximum voltage rating on V+ pin... 6
- Updated Human body model (HBM) and Charged device model (CDM) Electrostatic discharge for TMP411-Q1... 6
- Added DGK and DDF packages Thermal Information section... 6
- Updated the typo and moved "T_A = 15°C to 85°C, V+ = 3.3V" from Remote temperature error to Local temperature error... 7
- Added "T_{DIODE} = –40°C to 150°C" condition to temperature error power supply sensitivity... 7
- Added "Conversion time" for the New chip in Electrical Characteristics table... 7
- Updated the typo for Hysteresis typical value from 500mV to 170mV... 7
- Added "Logic input current" for the New chip in Electrical Characteristics table... 7
- Added "Output low voltage" for the New chip in Electrical Characteristics table... 7
- Added "High-level output leakage current" for the New chip in Electrical Characteristics table... 7
- Updated the typo and added 6mA min to "$\overline{\text{ALERT}}$ or $\overline{\text{THERM2}}$ output low sink current"... 7
- Added "Quiescent current" for the New chip and all test conditions in the Electrical Characteristics table... 7
- Removed limitation on Undervoltage lockout... 7
- Added "Power-on-reset threshold" for the new chip in the Electrical Characteristics table... 7
- Added Brownout detect value in the Electrical Characteristics table... 7
- Changed t(SUDAT) in High-Speed Mode from 10ns to 20ns... 11
- Added "Typical Characteristics (TMP411-Q1)" graphs for the New chip... 12
- Added an overview in the *Detailed Description* section... 19
- Updated the Basic Connections figure in the Overview section... 19
- Added *Functional Block Diagram* section... 20
- Added *Feature Description* section and relocated feature information to this section... 20
- Added "12-bit Q4 parameters and Bit values" tables along with its C code... 20
- Updated the *Undervoltage Lockout* section due to Undervoltage Lockout voltage removal by POR in the New chip... 23
- Added *Device Functional Modes* section... 24
- Clarified the Shutdown Mode (SD) section to match actual silicon behavior... 24
- Changed the terminology "Master" to "Controller" and "Slave" to "Target" throughout the document... 25
- Added *Timing Diagrams* to the *Specifications* section... 25
- Added "TMP411-Q1 and TMP411D-Q1 Device Address Options" table... 28
- Changed *REGISTER INFORMATION* section to *Register Maps* section and centralized register information in this section... 32
- Updated the Status Register section due to Undervoltage lockout voltage removal by POR in the New chip. 33
- Added "Application Information" section... 40
- Added D+ waveform in the Design Requirements section... 41
- Updated *Detailed Design Procedure* section... 42

- Added *Power Supply Recommendations* section....44
- Changed from *Layout Considerations* to *Layout Guidelines* 44
- Added "Layout Example" section....45
- Added the *Device and Documentation Support* section and subsections....46
- Added the *Mechanical, packaging, and Orderable Information* section....49

Changes from Revision E (December 2012) to Revision F (November 2013) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document....1
- Changed package throughout document from MSOP to VSSOP....1
- Changed device CDM ESD Classification Level from C3B to C4B in Section 1 list item and in the ABSOLUTE MAXIMUM RATINGS table....6

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMP411AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	125 to -40	411AQ
TMP411AQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	125 to -40	411AQ
TMP411BQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	411BQ
TMP411BQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	411BQ
TMP411CQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	411CQ
TMP411CQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	411CQ
TMP411DAQDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3O5F
TMP411DBQDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3O6F
TMP411DCQDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3O7F
TMP411DDQDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3O8F
TMP411DQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	411DQ
TMP411DQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	411DQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TMP411-Q1, TMP411D-Q1 :

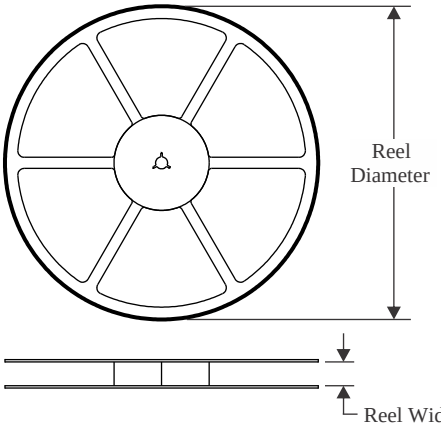
- Catalog : TMP411, TMP411D

NOTE: Qualified Version Definitions:

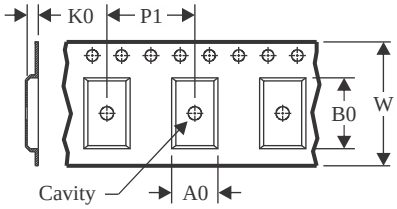
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

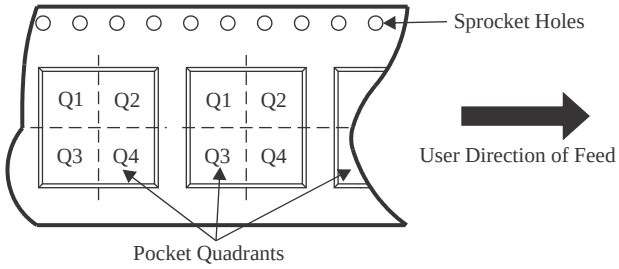


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

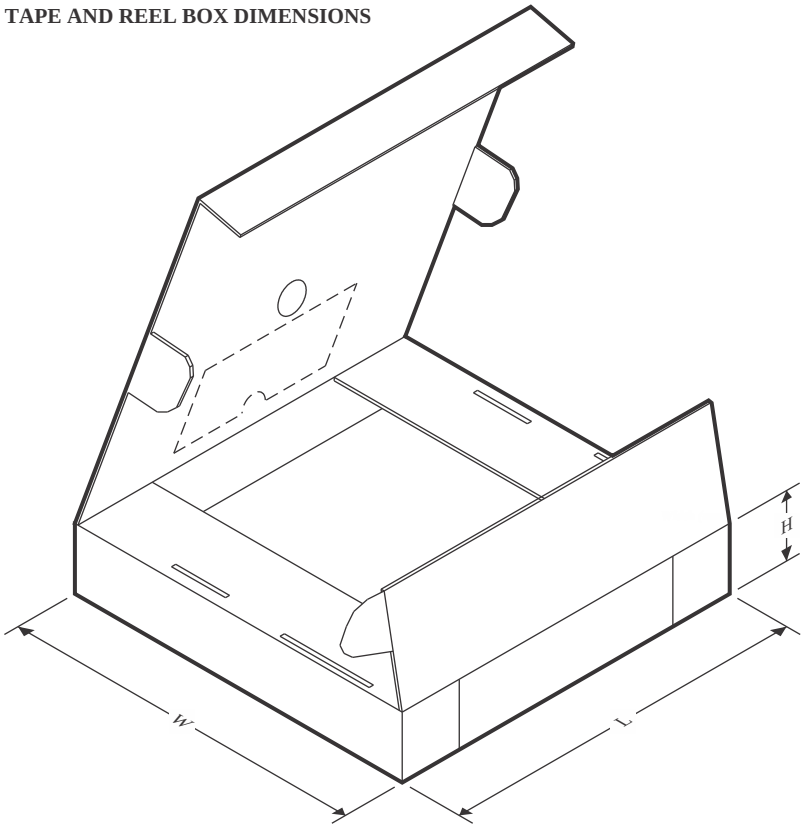
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP411AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TMP411BQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP411CQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP411DAQDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMP411DBQDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMP411DCQDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMP411DDQDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMP411DQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

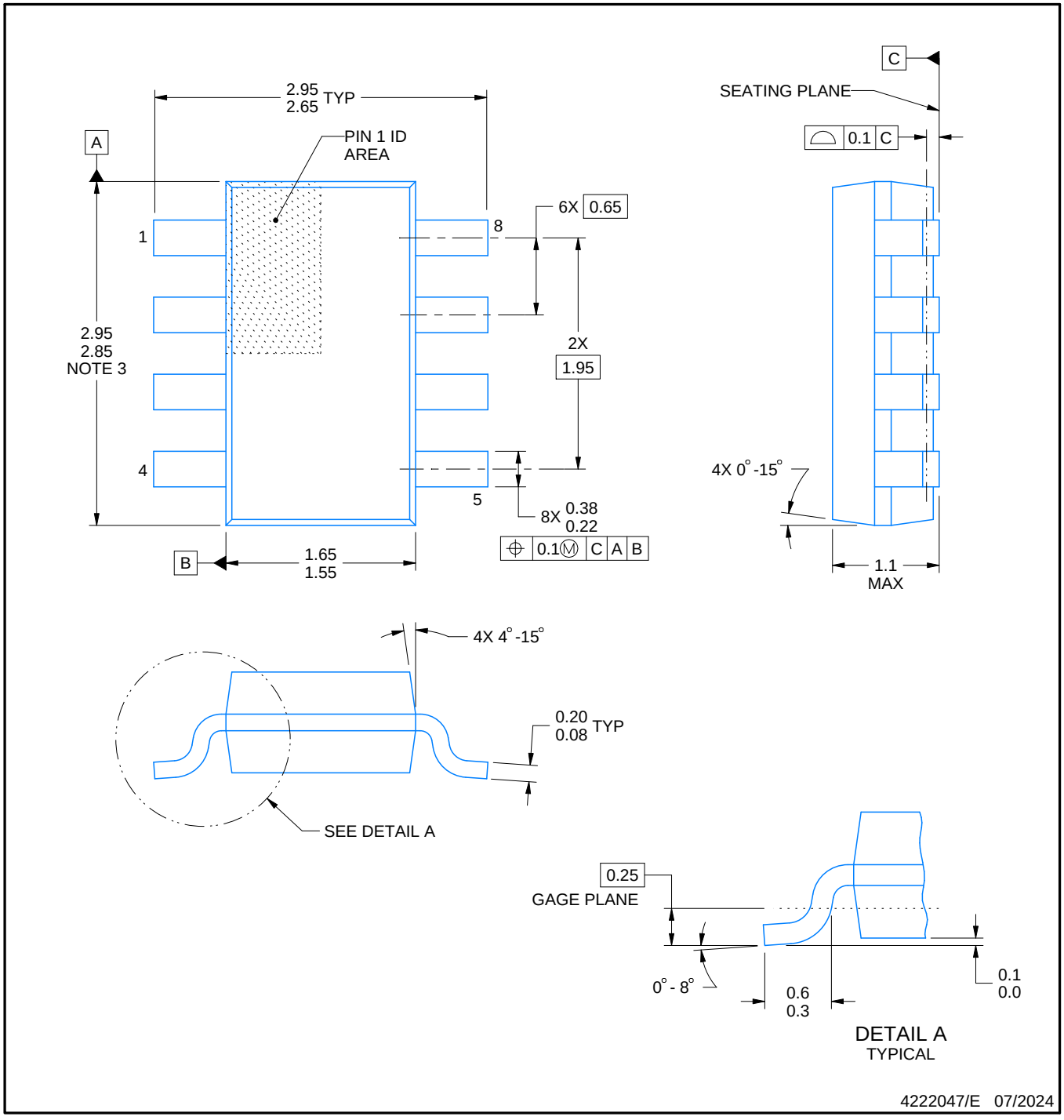
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP411AQDGKRQ1	VSSOP	DGK	8	2500	367.0	367.0	38.0
TMP411BQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP411CQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP411DAQDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TMP411DBQDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TMP411DCQDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TMP411DDQDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TMP411DQDGKRQ1	VSSOP	DGK	8	2500	367.0	367.0	38.0

PACKAGE OUTLINE

DDF0008A

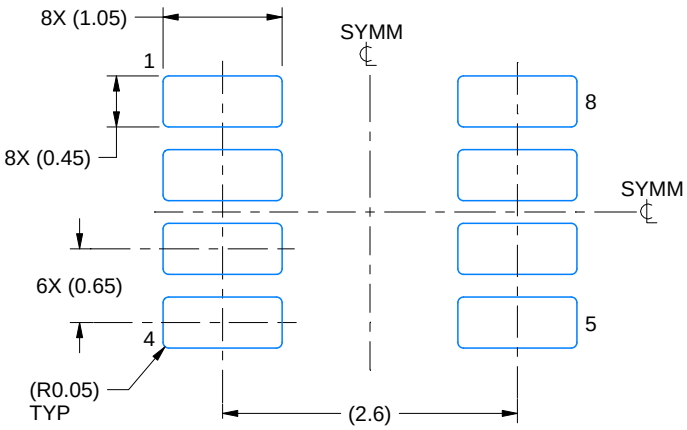
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

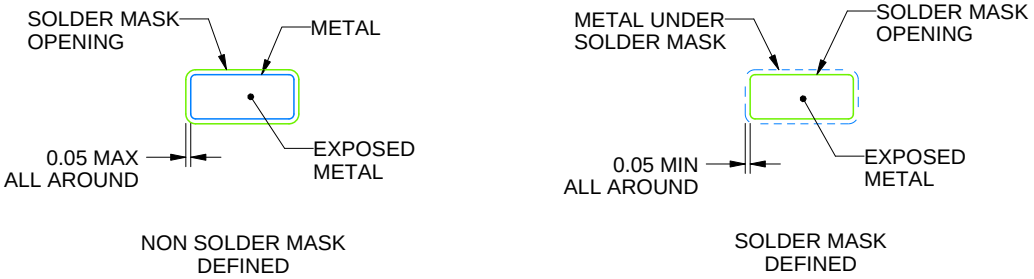


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

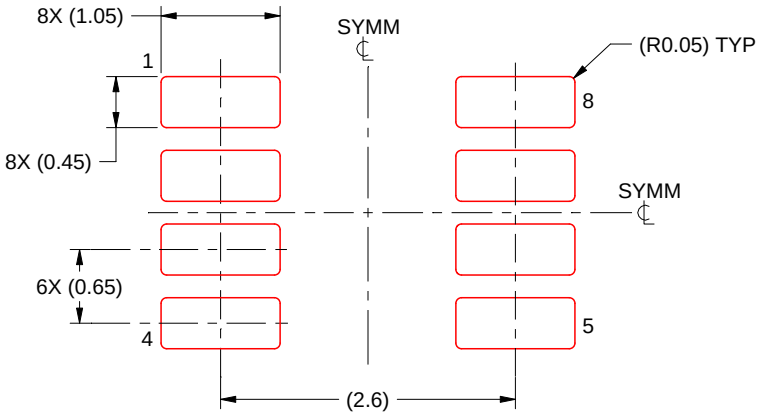
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

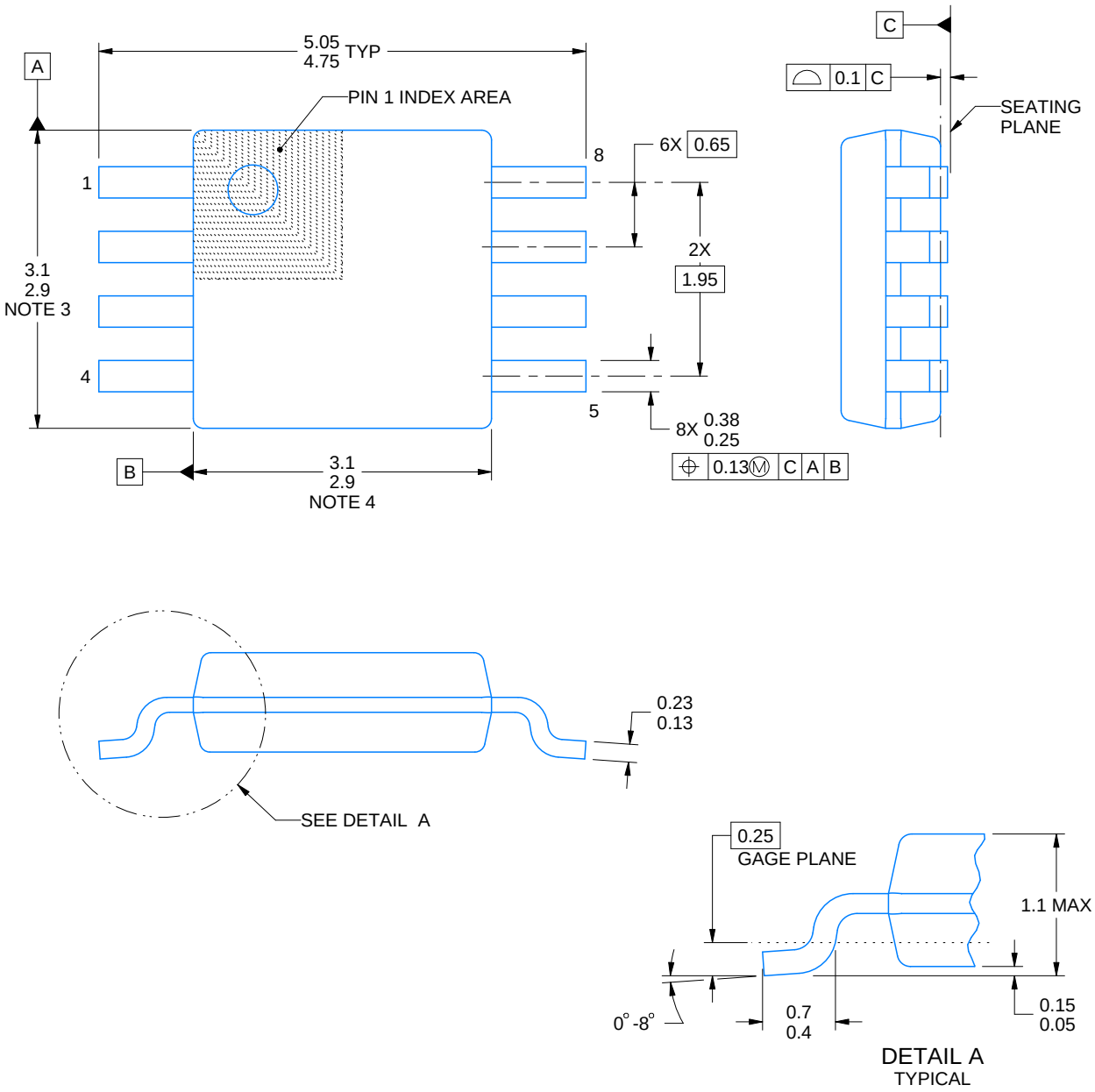
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

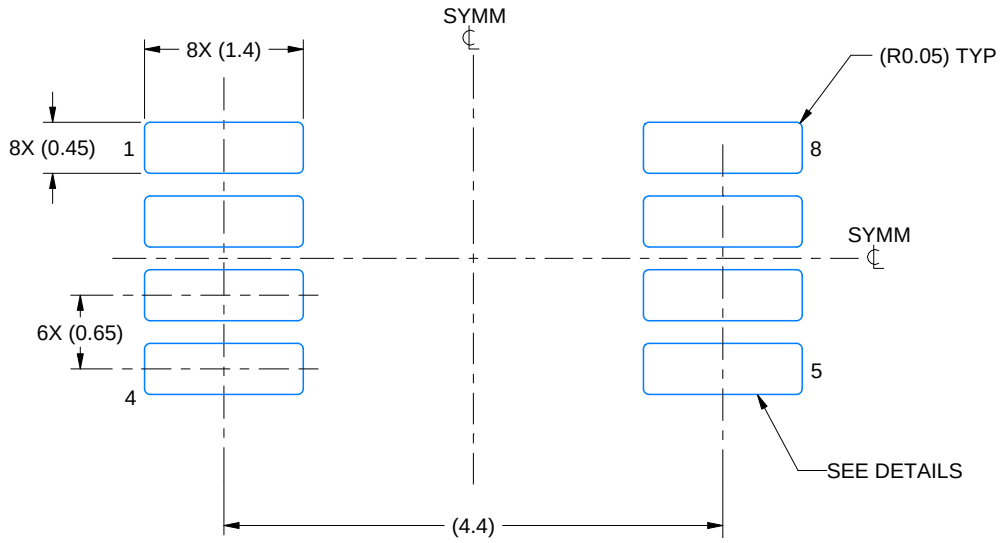
SMALL OUTLINE PACKAGE



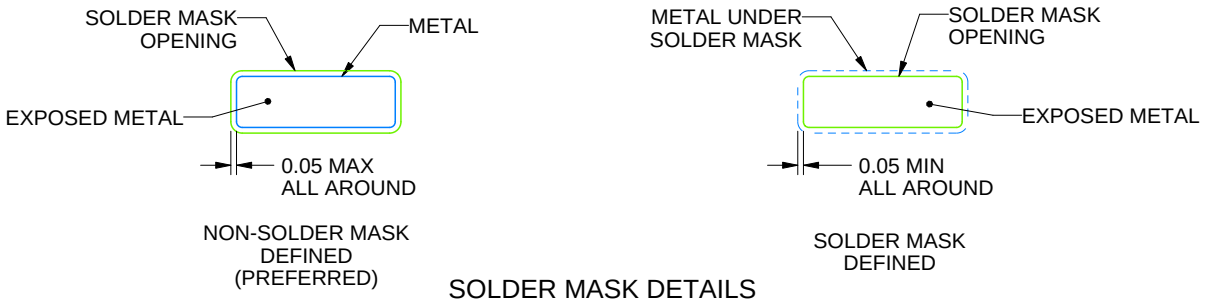
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

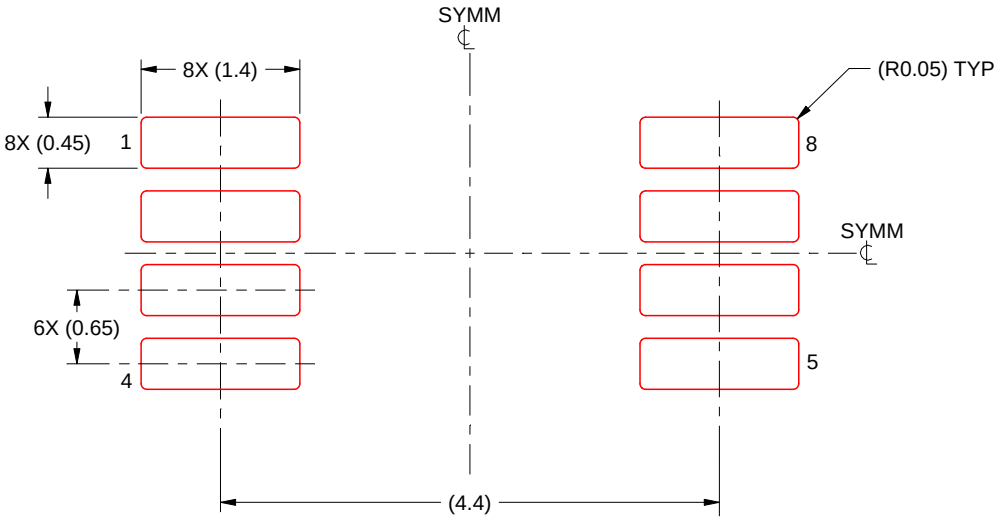


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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