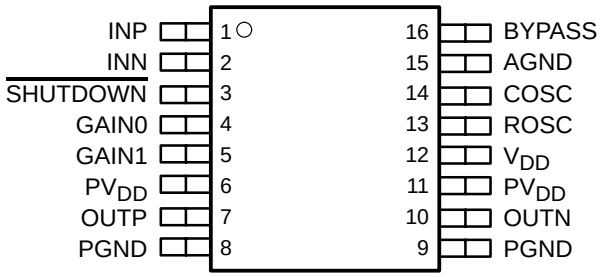
- **Modulation Scheme Optimized to Operate Without a Filter**
- **TSSOP Package Options**
- **1 W Into an 8-Ω Speaker (THD+N<1%)**
- **<0.2% THD+N at 1 W, 1 kHz, Into an 8-Ω Load**
- **Extremely Efficient Third Generation 5-V Class-D Technology:**
  - **Low-Supply Current (No Filter) . . . 4 mA**
  - **Low-Supply Current (Filter) . . . 7.5 mA**
  - **Low-Shutdown Current . . . 0.05 μA**
  - **Low-Noise Floor . . . 40 μV_{RMS} (No-Weighting Filter)**
  - **Maximum Efficiency Into 8 Ω, 75 – 85%**
  - **4 Internal Gain Settings . . . 6 – 23.5 dB**
  - **PSRR . . . –77 dB**
- **Integrated Depop Circuitry**
- **Short-Circuit Protection (Short to Battery, Ground, and Load)**

PW PACKAGE
(TOP VIEW)



description

The TPA2001D1 is a 1-W mono bridge-tied-load (BTL) class-D amplifier designed to drive a speaker with at least 8-Ω impedance. The amplifier uses TI's third generation modulation technique, which results in improved efficiency and SNR. It also allows the device to be connected directly to the speaker without the use of the LC output filter commonly associated with class-D amplifiers (this results in EMI which must be shielded at the system level). These features make the device ideal for use in devices where high-efficiency is needed to extend battery run time.

The gain of the amplifier is controlled by two input terminals, GAIN1, and GAIN0. This allows the amplifier to be configured for a gain of 6, 12, 18, and 23.5 dB. The differential input terminals are high-impedance CMOS inputs, and can be used as summing nodes.

The class-D BTL amplifier includes depop circuitry to reduce the amount of turnon pop at power up, and when cycling $\overline{\text{SHUTDOWN}}$.

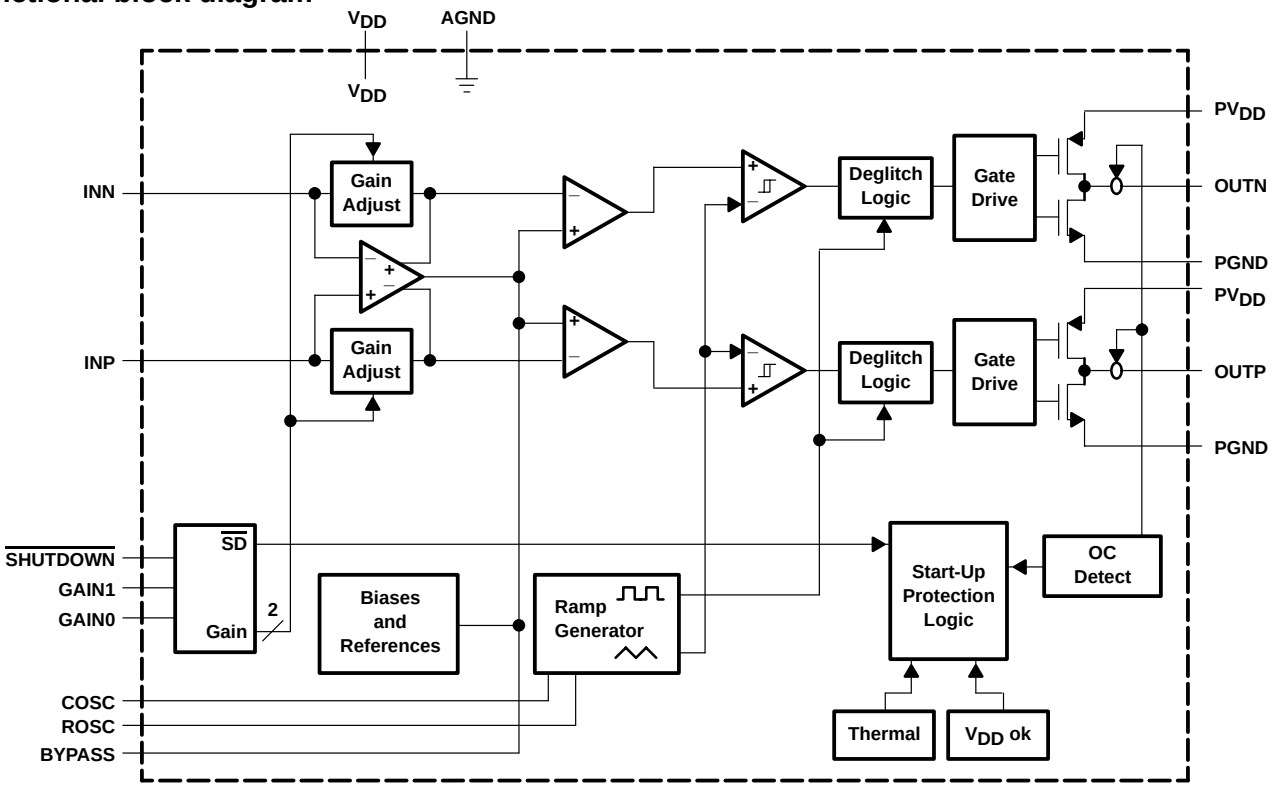
The TPA2001D1 is available in the 16-pin TSSOP package that drives 1 W of continuous output power into an 8-Ω load. TPA2001D1 operates over an ambient temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	TSSOP (PW)†
–40°C to 85°C	TPA2001D1PW

† The PW package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA2001D1PWR).

functional block diagram



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	GQC	PW		
AGND	A3 – A5, B2 – B6, C2 – C6, D2 – D4	15	I	Analog ground
BYPASS	A6	16	I	Connect capacitor to ground for BYPASS voltage filtering.
COSC	B7	14	I	Connect capacitor to ground to set oscillation frequency.
GAIN0	C1	4	I	Bit 0 of gain control (TTL logic level)
GAIN1	D1	5	I	Bit 1 of gain control (TTL logic level)
INN	A1	2	I	Negative differential input
INP	A2	1	I	Positive differential input
OUTN	G7	10	O	Negative BTL output
OUTP	G1	7	O	Positive BTL output
PGND	D5, D6 E2 – E6 F2 – F6 G2 – G6	8, 9	I	High-current grounds
PV_{DD}	E1, E7, F1, F7	6, 11	I	High-current power supplies
ROSC	C7	13	I	Connect resistor to ground to set oscillation frequency.
$\overline{SHUTDOWN}$	B1	3	I	Places the amplifier in shutdown mode if a TTL logic low is placed on this terminal, and normal operation if a TTL logic high is placed on this terminal.
V_{DD}	D7	12	I	Analog power supply

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD}, PV_{DD} . . . . . –0.3 V to 5.5 V
Input voltage, V_I . . . . . –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation . . . . . (see Dissipation Rating Table)
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Operating junction temperature range, T_J . . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PW	774 mW	6.19 mW/°C	495 mW	402 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}, PV_{DD}		2.7	5.5	V
High-level input voltage, V_{IH}	GAIN0, GAIN1, $\overline{\text{SHUTDOWN}}$	2		V
Low-level input voltage, V_{IL}	GAIN0, GAIN1, $\overline{\text{SHUTDOWN}}$		0.7	V
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics at specified free-air temperature, PV_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS}\rvert$	Output offset voltage (measured differentially)	V_I = 0 V,	A_V = any gain			25	mV
PSRR	Power supply rejection ratio	PV_{DD} = 4.9 V to 5.1 V			77		dB
$\lvert I_{IH}\rvert$	High-level input current	PV_{DD} = 5.5 V,	$V_I = PV_{DD}$			1	μA
$\lvert I_{IL}\rvert$	Low-level input current	PV_{DD} = 5.5 V,	V_I = 0 V			1	μA
I_{DD}	Supply current, no filter (with or without speaker load)				4	6	mA
$I_{DD(SD)}$	Supply current, shutdown mode	GAIN0, GAIN1, $\overline{\text{SHUTDOWN}}$ = 0 V			0.05	20	μA

operating characteristics, PV_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω, gain = 6 dB (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 1%,	f = 1 kHz		1		W
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 20 kHz		<0.1%		
B_{OM}	Maximum output power bandwidth	THD = 1%			20		kHz
k_{SVR}	Supply ripple rejection ratio	f = 1 kHz,	$C_{(BYP)}$ = 1 μF		71		dB
SNR	Signal-to-noise ratio				95		dB
V_n	Output noise voltage (no noise weighting filter)	$C_{(BYP)}$ = 1 μF,	f = <10 Hz to 22 kHz		40		μV(rms)
Z_I	Input impedance				>15		kΩ

electrical characteristics at specified free-air temperature, PV_{DD} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OS}\|$	Output offset voltage (measured differentially)	V_I = 0 V,	A_V = any gain			25	mV
PSRR	Power supply rejection ratio	PV_{DD} = 3.2 V to 3.4 V			61		dB
$\|I_{IH}\|$	High-level input current	PV_{DD} = 3.3 V,	$V_I = PV_{DD}$			1	μA
$\|I_{IL}\|$	Low-level input current	PV_{DD} = 3.3 V,	V_I = 0 V			1	μA
I_{DD}	Supply current, no filter (with or without speaker load)				4	6	mA
$I_{DD(SD)}$	Supply current, shutdown mode				0.05	20	μA

operating characteristics, PV_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω, gain = 6 dB (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 1%,	f = 1 kHz		400		mW
THD + N	Total harmonic distortion plus noise	P_O = 55 mW,	f = 20 Hz to 20 kHz		<0.1%		
B_{OM}	Maximum output power bandwidth	THD = 0.7%			20		kHz
k_{SVR}	Supply ripple rejection ratio	f = 1 kHz,	$C_{(BYP)}$ = 1 μF		61		dB
SNR	Signal-to-noise ratio				93		dB
V_n	Output noise voltage (no noise weighting filter)	$C_{(BYP)}$ = 1 μF,	f = <10 Hz to 22 kHz		40		μV(rms)
Z_I	Input impedance				>15		kΩ

APPLICATION INFORMATION

eliminating the output filter with the TPA2001D1

This section focuses on why the user can eliminate the output filter with the TPA2001D1.

effect on audio

The class-D amplifier outputs a pulse-width modulated (PWM) square wave, which is the sum of the switching waveform and the amplified input audio signal. The human ear acts as a band-pass filter such that only the frequencies between approximately 20 Hz and 20 kHz are passed. The switching frequency components are much greater than 20 kHz, so the only signal heard is the amplified input audio signal.

traditional class-D modulation scheme

The traditional class-D modulation scheme, which is used in the TPA005Dxx family, has a differential output where each output is 180 degrees out of phase and changes from ground to the supply voltage (V_{DD}). Therefore, the differential prefiltered output varies between positive and negative V_{DD}, where filtered 50% duty cycle yields 0 volts across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 1. Note that even at an average of 0 V across the load (50% duty cycle), the current to the load is high, causing high loss, thus causing a high supply current.

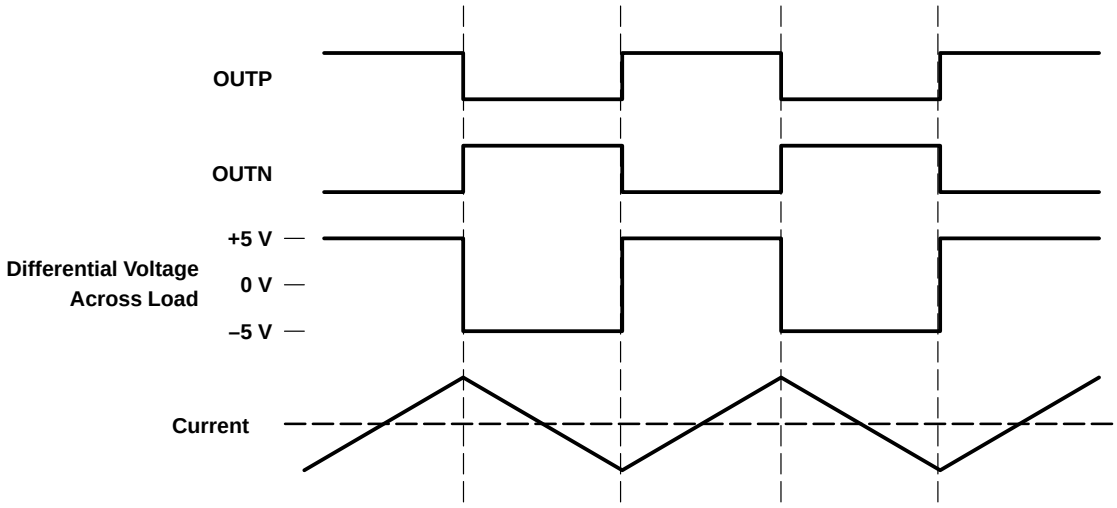


Figure 1. Traditional Class-D Modulation Scheme's Output Voltage and Current Waveforms Into an Inductive Load With No Input

TPA2001D1 modulation scheme

The TPA2001D1 uses a modulation scheme that still has each output switching from 0 to the supply voltage. However, OUTP and OUTN are now in phase with each other with no input. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative voltages. The voltage across the load sits at 0 V throughout most of the switching period greatly reducing the switching current, which reduces any I^2R losses in the load.

APPLICATION INFORMATION

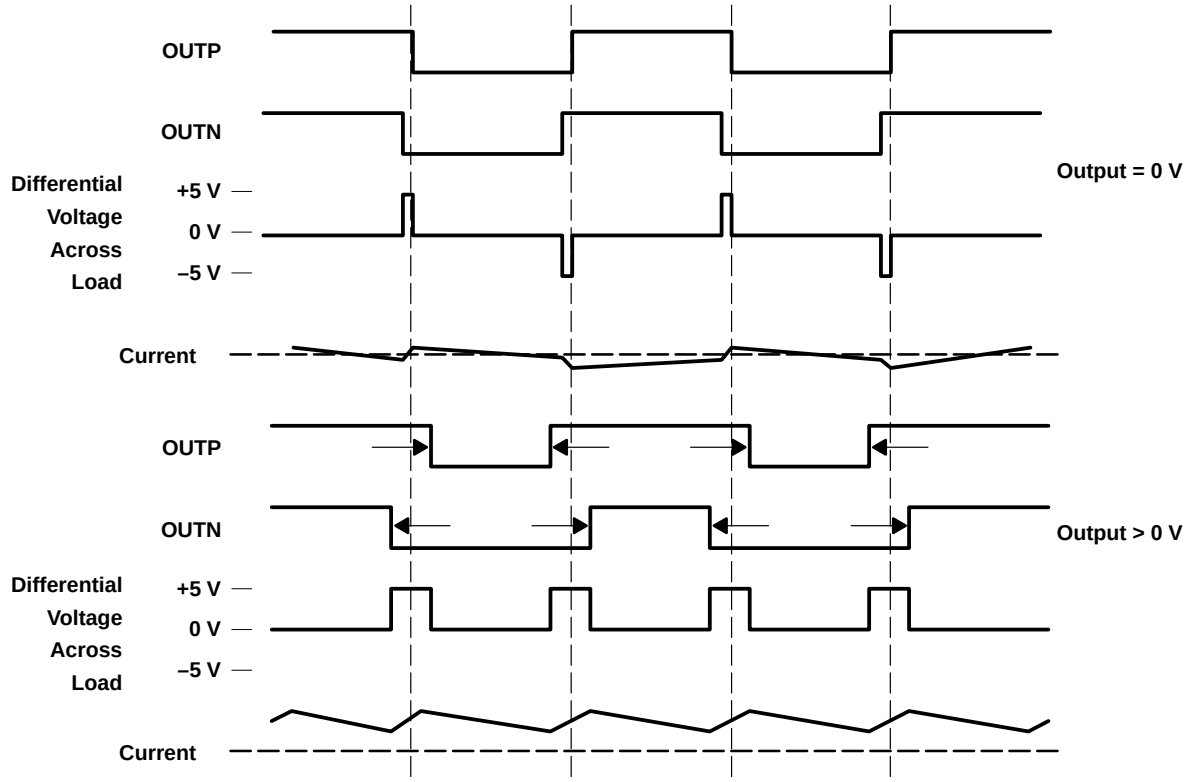


Figure 2. The TPA2001D1 Output Voltage and Current Waveforms Into an Inductive Load

efficiency: why you must use a filter with the traditional class-D modulation scheme

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is $2 \times V_{DD}$ and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA2001D1 modulation scheme has very little loss in the load without a filter because the pulses are very short and the change in voltage is V_{DD} instead of $2 \times V_{DD}$. As the output power increases, the pulses widen making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance than the speaker that results in less power dissipated, which increases efficiency.

APPLICATION INFORMATION

effects of applying a square wave into a speaker

Audio specialists advise not to apply a square wave to speakers. If the amplitude of the waveform is high enough and the frequency of the square wave is within the bandwidth of the speaker, the square wave could cause the voice coil to jump out of the air gap and/or scar the voice coil. A 250-kHz switching frequency, however, is not significant because the speaker cone movement is proportional to $1/f^2$ for frequencies beyond the audio band. Therefore, the amount of cone movement at the switching frequency is very small. However, damage could occur to the speaker if the voice coil is not designed to handle the additional power. To size the speaker for added power, the ripple current dissipated in the load needs to be calculated by subtracting the theoretical supplied power ($P_{SUP\ THEORETICAL}$) from the actual supply power (P_{SUP}) at maximum output power (P_O). The switching power dissipated in the speaker is the inverse of the measured efficiency ($\eta_{MEASURED}$) minus the theoretical efficiency ($\eta_{THEORETICAL}$) all multiplied by P_O.

$$P_{SPKR} = P_{SUP} - P_{SUP\ THEORETICAL} \text{ (at max output power)} \quad (1)$$

$$P_{SPKR} = P_O(P_{SUP} / P_O - P_{SUP\ THEORETICAL} / P_O) \text{ (at max output power)} \quad (2)$$

$$P_{SPKR} = P_O(1/\eta_{MEASURED} - 1/\eta_{THEORETICAL}) \text{ (at max output power)} \quad (3)$$

The maximum efficiency of the TPA2001D1 with an 8-Ω load is 85%. Using equation 3 with the efficiency at maximum power (78%), we see that there is an additional 106 mW dissipated in the speaker. The added power dissipated in the speaker is not an issue as long as it is taken into account when choosing the speaker.

when to use an output filter

Design the TPA2001D1 without the filter if the traces from amplifier to speaker are short. The TPA2001D1 passed FCC and CE radiated emissions with no shielding with speaker wires eight inches long or less. Notebook PCs and powered speakers where the speaker is in the same enclosure as the amplifier are good applications for class-D without a filter.

A ferrite bead filter can often be used if the design is failing radiated emissions without a filter, and the frequency sensitive circuit is greater than 1 MHz. This is good for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30 MHz. If choosing a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies.

Use an output filter if there are low frequency (<1 MHz) EMI sensitive circuits and/or there are long leads from amplifier to speaker.

gain setting via GAIN0 and GAIN1 inputs

The gain of the TPA2001D1 is set by two input terminals, GAIN0 and GAIN1.

The gains listed in Table 1 are realized by changing the taps on the input resistors inside the amplifier. This causes the input impedance, Z_I, to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the actual gain distribution from part-to-part is quite good. However, the input impedance may shift by 30% due to shifts in the actual resistance of the input resistors.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 20 kΩ, which is the absolute minimum input impedance of the TPA2001D1. At the higher gain settings, the input impedance could increase as high as 115 kΩ.

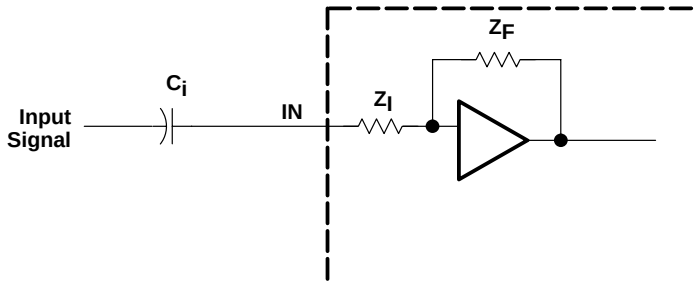
APPLICATION INFORMATION

Table 1. Gain Settings

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	6	104
0	1	12	74
1	0	18	44
1	1	23.5	24

input resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over six times that value. As a result, if a single capacitor is used in the input high-pass filter, the –3 dB or cutoff frequency also changes by over six times.



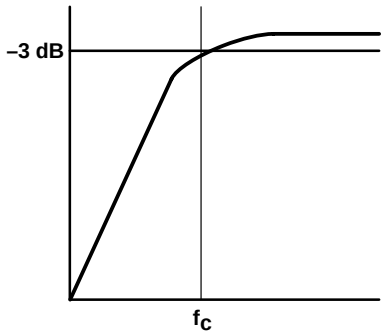
The –3 dB frequency can be calculated using equation 4.

$$f_c = \frac{1}{2\pi Z_I C_i} \quad (4)$$

input capacitor, C_i

In the typical application an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier (Z_I) form a high-pass filter with the corner frequency determined in equation 5.

$$f_c = \frac{1}{2\pi Z_I C_i} \quad (5)$$



APPLICATION INFORMATION

input capacitor, C_i (continued)

The value of C_i is important, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_I is 20 kΩ and the specification calls for a flat bass response down to 80 Hz. Equation 5 is reconfigured as equation 6.

$$C_i = \frac{1}{2\pi Z_I f_c} \quad (6)$$

In this example, C_i is 0.1 μF, so one would likely choose a value in the range of 0.1 μF to 1 μF. If the gain is known and will be constant, use Z_I from Table 1 to calculate C_i. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

C_i must be 10 times smaller than the bypass capacitor to reduce clicking and popping noise from power on/off and entering and leaving shutdown. After sizing C_i for a given cutoff frequency, size the bypass capacitor to 10 times that of the input capacitor.

$$C_i \leq C_{BYP} / 10 \quad (7)$$

power supply decoupling, C_S

The TPA2001D1 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, $C_{(BYP)}$

The midrail bypass capacitor ($C_{(BYP)}$) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, $C_{(BYP)}$ determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor ($C_{(BYP)}$) values of 0.47-μF to 1-μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

Increasing the bypass capacitor reduces clicking and popping noise from power on/off and entering and leaving shutdown. To have minimal pop, $C_{(BYP)}$ should be 10 times larger than C_i.

$$C_{(BYP)} \geq 10 \times C_i \quad (8)$$

APPLICATION INFORMATION

differential input

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA2001D1 EVM with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA2001D1 with a single-ended source, ac ground the INN input through a capacitor and apply the audio single to the input. In a single-ended input application, the INN input should be ac-grounded at the audio source instead of at the device input for best noise performance.

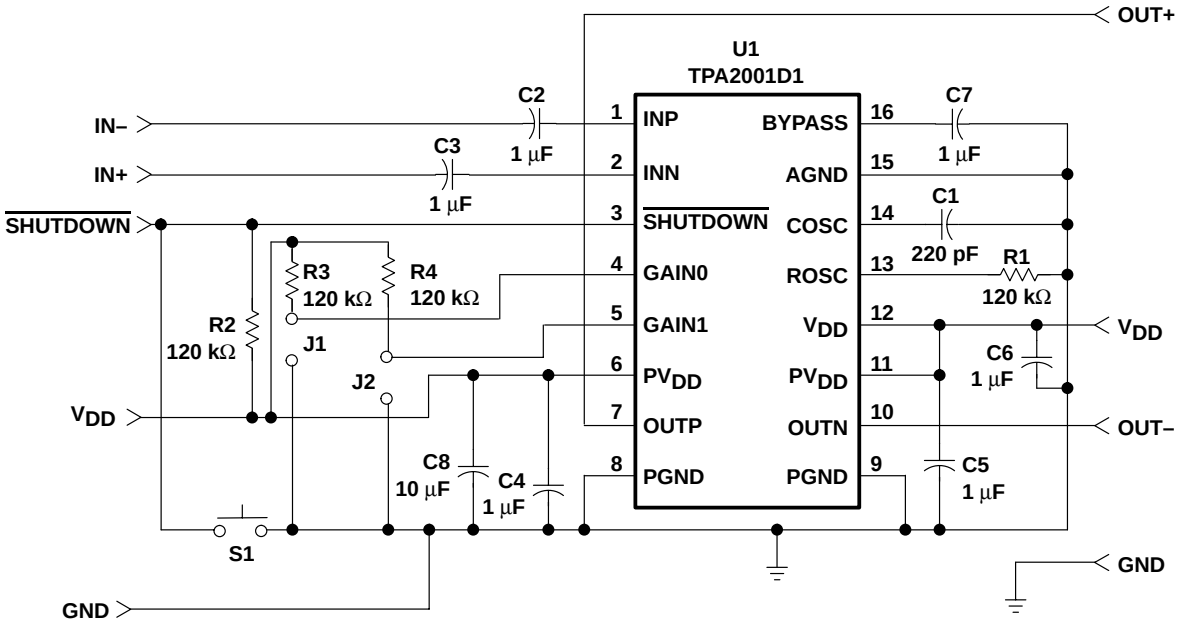
shutdown modes

The TPA2001D1 employs a shutdown mode of operation designed to reduce supply current (I_{DD}) to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, $I_{DD(SD)}$ = 1 μA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

evaluation circuit



NOTE: R1, R2, and R3 are used in the EVM but are not required for normal applications.

APPLICATION INFORMATION

Table 2. TPA2001D1 Evaluation Bill of Materials

REFERENCE	DESCRIPTION	SIZE	QUANTITY	MANUFACTURER	PART NUMBER
C1	Capacitor, ceramic, 220 pF, ±10%, XICON, 50 V	0805	1	Mouser	140-CC501B221K
C2 – C7	Capacitor, ceramic, 1 μF, +80%/–20%, Y5V, 16 V	0805	6	Murata	GRM40-Y5V105Z16
C8	Capacitor, ceramic, 10 μF, +80%/–20%, Y5V, 16 V	1210	1	Murata	GRM235-Y5V106Z16
R1, R2†, R3†, R4†	Resistor, chip, 120 kΩ, 1/10 W, 5%, XICON	0805	4	Mouser	260–120K
U1	IC, TPA2001D1, audio power amplifier, 1-W, single channel, class-D	24 pin TSSOP	1	TI	TPA2001D1PW

† These components are used in the EVM, but they are not required for normal applications.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA2001D1PW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2001D1
TPA2001D1PW.A	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2001D1
TPA2001D1PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2001D1
TPA2001D1PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2001D1
TPA2001D1PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2001D1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

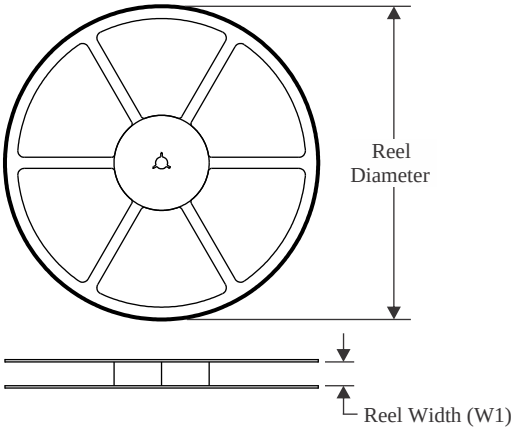
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

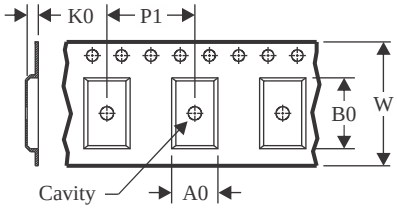
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

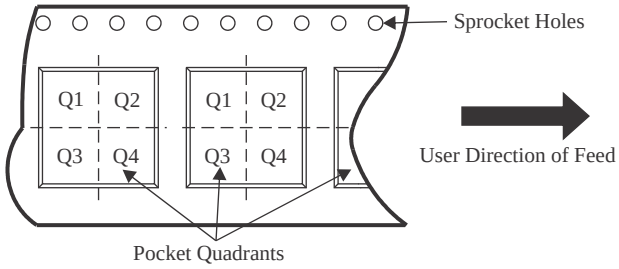


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

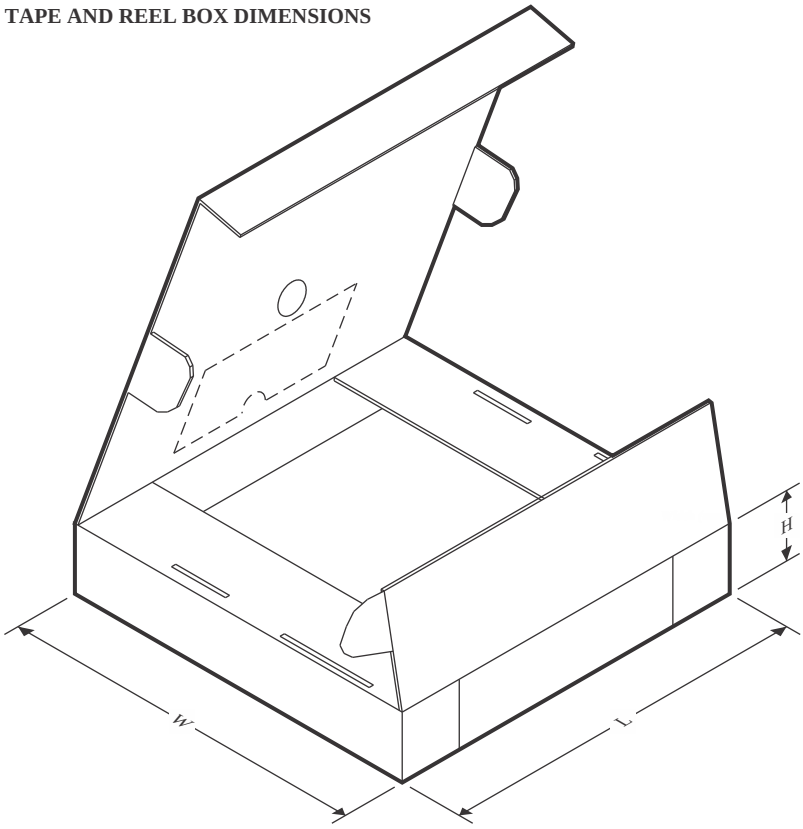
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA2001D1PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

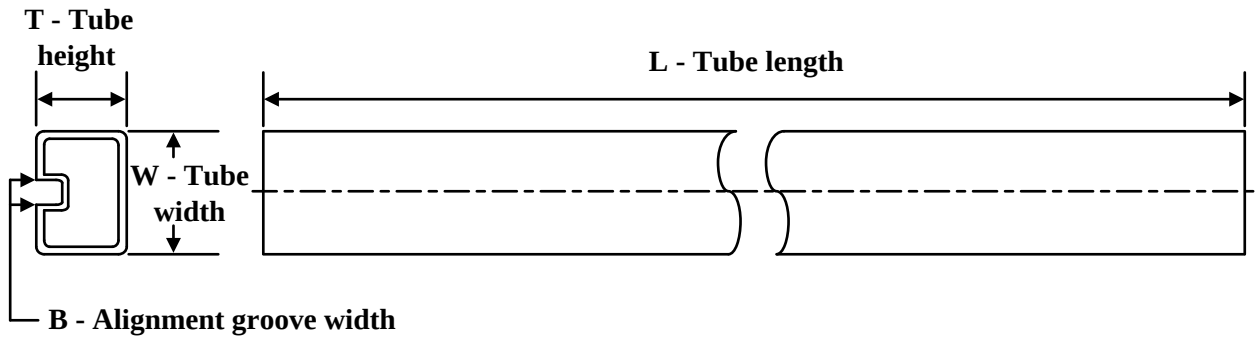
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA2001D1PWR	TSSOP	PW	16	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

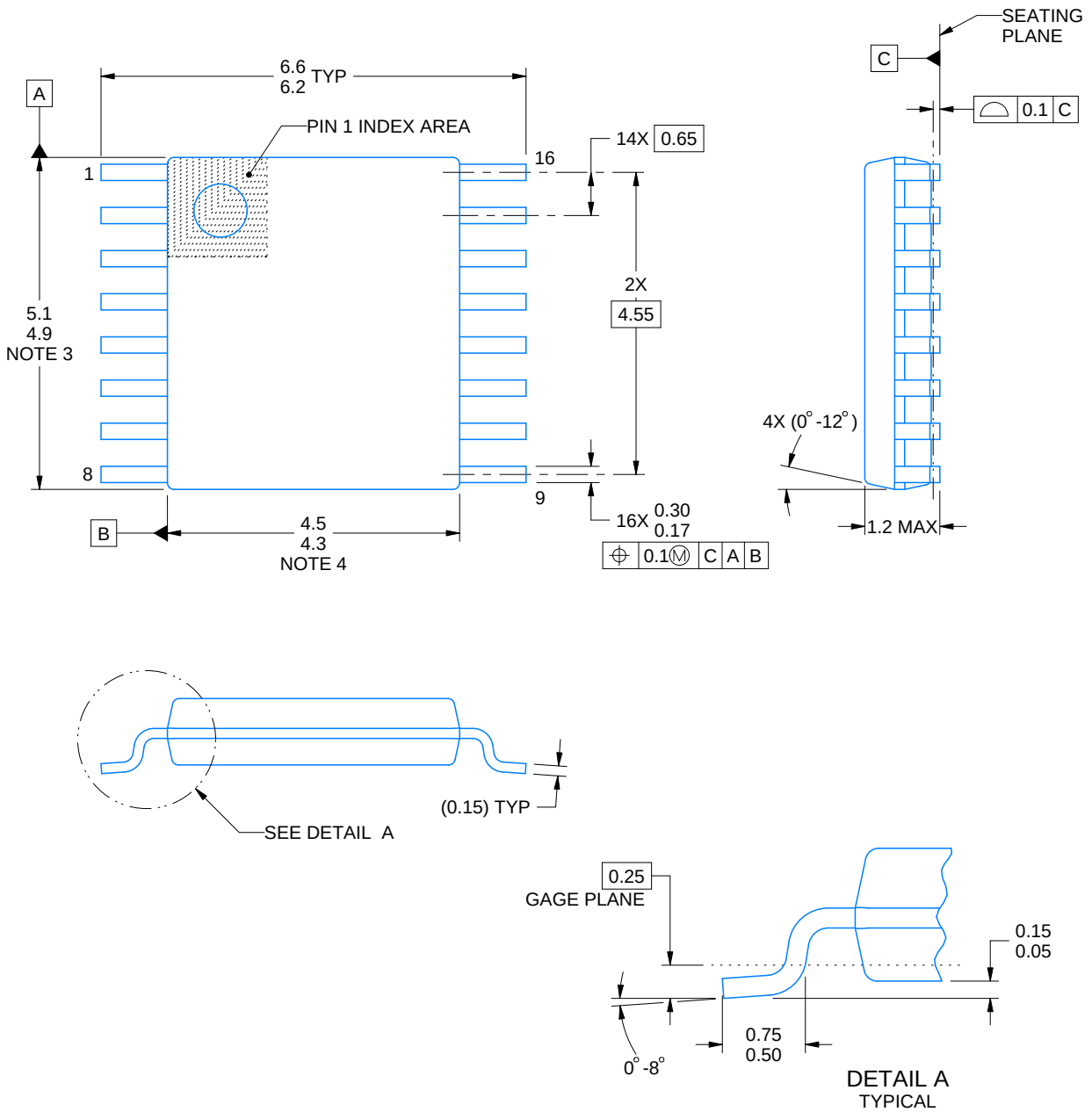
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA2001D1PW	PW	TSSOP	16	90	530	10.2	3600	3.5
TPA2001D1PW.A	PW	TSSOP	16	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0016A

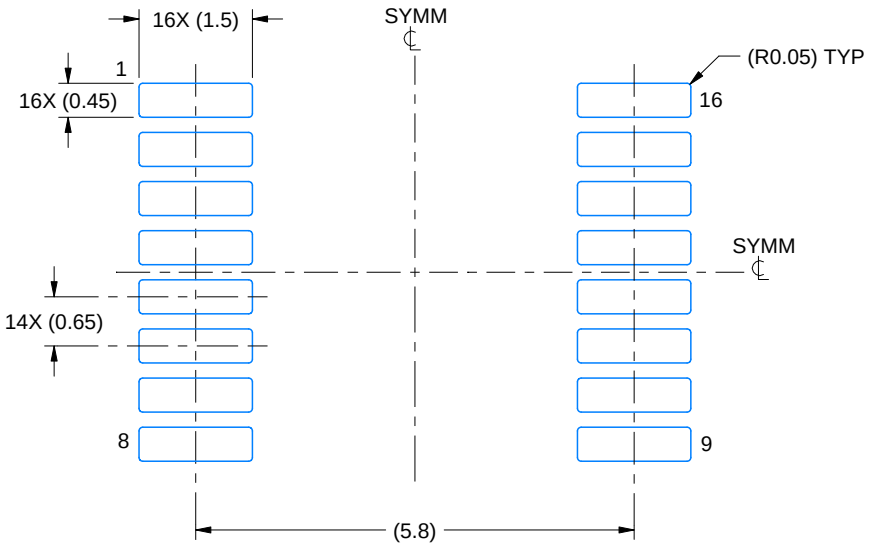
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

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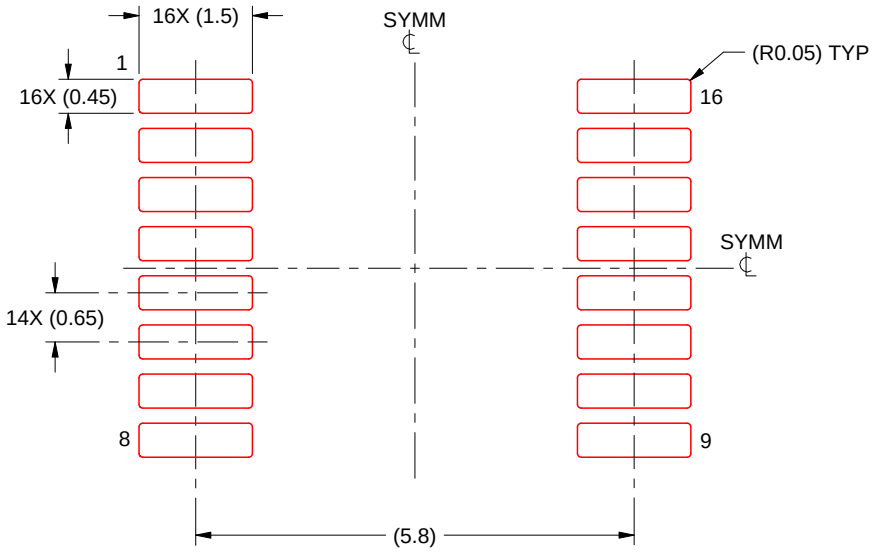
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025