

## TPS2HB16-Q1 40-V, 16-mΩ Dual-Channel Smart High-Side Switch

### 1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1:  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
  - Withstands 40-V load dump
- Dual-channel smart high-side switch with 16-mΩ  $R_{ON}$  ( $T_J = 25^\circ\text{C}$ )
- Improve system level reliability through [adjustable current limiting](#)
  - Current limit adjustable from 4.1 A to 48.5 A and internally fixed at 60 A
- Robust integrated output protection:
  - Integrated thermal protection
  - Protection against short to ground/battery
  - Protection against [reverse battery](#) events including automatic switch on with reverse voltage
  - Automatic shut off if loss of battery/ground occurs
  - Integrated output clamp to demagnetize inductive loads
  - Configurable fault handling
- Analog sense output can be configured to accurately measure:
  - Load current
  - Device temperature
- Provides fault indication through SNS pin
  - Detection of open load and short-to-battery

### 2 Applications

- [Automotive display module](#)
- [ADAS modules](#)
- [Seat comfort module](#)
- [Transmission control unit](#)
- [HVAC control module](#)
- [Body control modules](#)
- [LED lighting](#)
- [2x27W Bulbs](#)

### 3 Description

The TPS2HB16-Q1 device is a dual-channel smart high-side switch intended for use in 12-V automotive systems. The device integrates robust protection and diagnostic features to ensure output port protection even during harmful events like short circuits in automotive systems. The device protects against faults through a [reliable current limit](#), which, depending on device variant, is adjustable from 4.1 A to 48.5 A. The TPS2HB16F-Q1 device is designed to be able to drive 2x35W, 2x27W, and 2x21W bulbs due to its high fixed current limit of 60A.

The high current limit range allows for usage in loads that require large transient currents, while the low current limit range provides improved protection for loads that do not require high peak current. The device is capable of reliably driving various [load profiles](#).

The TPS2HB16-Q1 also provides a high accuracy analog current sense that allows for improved load diagnostics. By reporting load current and device temperature to a system MCU, the device enables predictive maintenance and load diagnostics that improves the system lifetime.

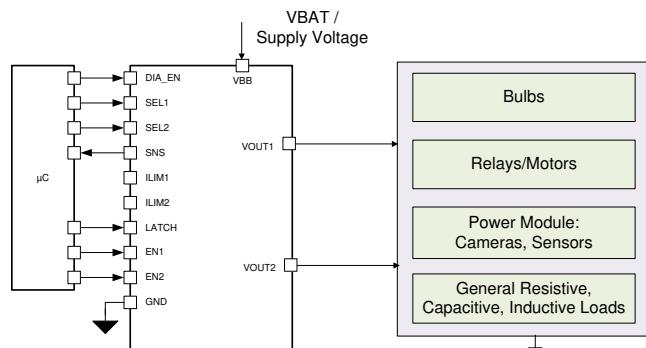
The TPS2HB16-Q1 is available in a HTSSOP package which allows for reduced PCB footprint.

#### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE     | BODY SIZE (NOM)   |
|-------------|-------------|-------------------|
| TPS2HB16-Q1 | HTSSOP (16) | 5.00 mm x 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Simplified Schematic



An **IMPORTANT NOTICE** at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. **PRODUCTION DATA**.

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## 4 Revision History

| Changes from Revision B (November 2019) to Revision C | Page |
|---|------|
| • Added Device Version F                              | 3    |

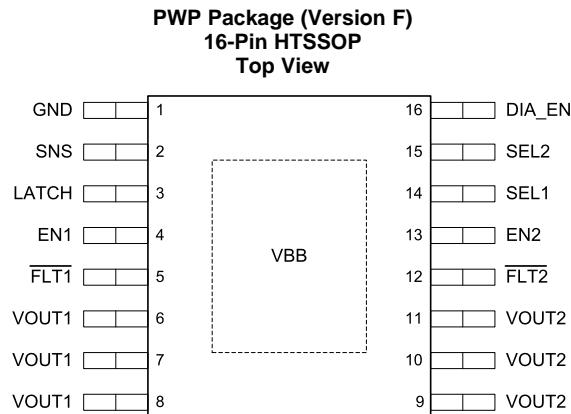
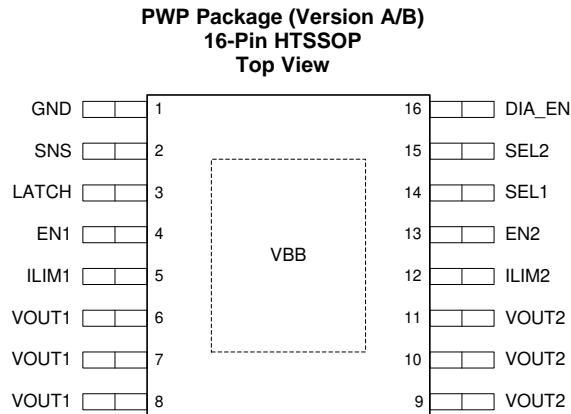
| Changes from Revision A (April 2019) to Revision B    | Page |
|---|------|
| • Changed from Advance Information to Production Data | 1    |

## 5 Device Comparison Table

**Table 1. TPS2HB16-Q1 Device Options**

| Device Version | Part Number  | Orderable Part Number | Current Limit         | Current Limit Range | Overcurrent Behavior       |
|----------------|--------------|-----------------------|-----------------------|---------------------|----------------------------|
| A              | TPS2HB16A-Q1 | TPS2HB16AQPWPR Q1     | Resistor Programmable | 4.1 A - 22 A        | Disable switch immediately |
| B              | TPS2HB16B-Q1 | TPS2HB16BQPWPR Q1     | Resistor Programmable | 10.3 A - 48.5 A     | Disable switch immediately |
| F              | TPS2HB16F-Q1 | TPS2HB16FQPWPR Q1     | Internally Set        | 60 A                | Disable switch immediately |

## 6 Pin Configuration and Functions



### Pin Functions

| PIN    |             |             | I/O | DESCRIPTION  |
|--------|-------------|-------------|-----|--|
| NO.    | Version A/B | Version F   |     |  |
| GND    | 1           | 1           | -   | Device ground  |
| SNS    | 2           | 2           | O   | Sense output   |
| LATCH  | 3           | 3           | I   | Sets fault handling behavior (latched or auto-retry)   |
| EN1    | 4           | 4           | I   | Channel 1 control input, active high   |
| ILIM1  | 5           | -           | O   | Connect pull-up resistor to V <sub>BB</sub> to set current-limit threshold on CH1                |
| FLT1   | -           | 5           | O   | Open drain fault indication  |
| VOUT1  | 6-8         | 6-8         | O   | Channel 1 output   |
| VOUT2  | 9-11        | 9-11        | O   | Channel 2 output   |
| ILIM2  | 12          | -           | O   | Connect pull-up resistor to V <sub>BB</sub> to set current-limit threshold on CH2                |
| FLT2   | -           | 12          | O   | Open drain fault indication  |
| EN2    | 13          | 13          | I   | Channel 2 control input, active high   |
| SEL1   | 14          | 14          | I   | Diagnostics select 1. No functionality on version F; tie to device ground through 10 kΩ resistor |
| SEL2   | 15          | 15          | I   | Diagnostics select 2   |
| DIA_EN | 16          | 16          | I   | Diagnostic enable, active high   |
| VBB    | Exposed Pad | Exposed Pad | I   | Power supply input   |

## 6.1 Recommended Connections for Unused Pins

The TPS2HB16-Q1 device is designed to provide an enhanced set of diagnostic and protection features. However, if the system design only allows for a limited number of I/O connections, some pins may be considered optional.

**Table 2. Connections for Optional Pins**

| PIN NAME               | CONNECTION IF NOT USED                             | IMPACT IF NOT USED   |
|------------------------|--|--|
| SNS                    | Ground through 1-k $\Omega$ resistor               | Analog sense is not available.   |
| LATCH                  | Float or ground through R <sub>PROT</sub> resistor | With LATCH unused, the device will auto-retry after a fault. If latched behavior is desired, but the system describes limited I/O, it is possible to use one microcontroller output to control the latch function of several high-side channels. |
| ILIM1, ILIM2           | Float  | If the ILIMx pin is left floating, the device will be set to the default internal current-limit threshold.   |
| SEL1                   | Float or ground through R <sub>PROT</sub> resistor | SEL1 selects the T <sub>J</sub> sensing feature. With SEL1 unused, only CH1 and CH2 current sensing and open load detection are available.   |
| SEL2                   | Ground through R <sub>PROT</sub> resistor          | With SEL2 = 0 V, CH2 current sensing and CH2 open load detection are not available.  |
| FLT1, FLT2 (Version F) | Float  | If the FLT pin is unused, the system cannot read faults from the output.   |
| DIA_EN                 | Float or ground through R <sub>PROT</sub> resistor | With DIA_EN unused, the analog sense, open-load, and short-to-battery diagnostics are not available.   |

R<sub>PROT</sub> is used to protect the pins from excess current flow during reverse battery conditions, for more information see the section on [Reverse Battery](#) protection.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|   |  | MIN | MAX               | UNIT |
|---|--|-----|-------------------|------|
| Maximum continuous supply voltage, $V_{BB}$             |  | 36  |                   | V    |
| Load dump voltage, $V_{LD}$                             | ISO16750-2:2010(E)   |     | 40                | V    |
| Reverse battery voltage, $V_{Rev}$ , $t \leq 3$ minutes |  | -18 |                   | V    |
| Enable pin voltage, $V_{EN1}$ and $V_{EN2}$             |  | -1  | 7                 | V    |
| LATCH pin voltage, $V_{LATCH}$                          |  | -1  | 7                 | V    |
| Diagnostic Enable pin voltage, $V_{DIA\_EN}$            |  | -1  | 7                 | V    |
| Sense pin voltage, $V_{SNS}$                            |  | -1  | 18                | V    |
| Select pin voltage, $V_{SEL1}$ and $V_{SEL2}$           |  | -1  | 7                 | V    |
| Reverse ground current, $I_{GND}$                       | $V_{BB} < 0$ V   |     | -50               | mA   |
| Energy dissipation during turnoff, $E_{TOFF}$           | Single pulse, one channel, $L_{OUT} = 5$ mH, $T_{J,start} = 125^\circ C$     |     | 50 <sup>(2)</sup> | mJ   |
| Energy dissipation during turnoff, $E_{TOFF}$           | Repetitive pulse, one channel, $L_{OUT} = 5$ mH, $T_{J,start} = 125^\circ C$ |     | 13 <sup>(2)</sup> | mJ   |
| Maximum junction temperature, $T_J$                     |  | 150 |                   | °C   |
| Storage temperature, $T_{stg}$                          |  | -65 | 150               | °C   |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

(2) For further details, see the section regarding switch-off of an inductive load.

### 7.2 ESD Ratings

|             |  |   | VALUE                                   | UNIT       |
|-------------|--|---|---|------------|
| $V_{(ESD)}$ | Electrostatic discharge                      | Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> | All pins except $V_{BB}$ and $V_{OUTx}$ | $\pm 2000$ |
|             |  |   | $V_{BB}$ and $V_{OUTx}$                 | $\pm 4000$ |
|             | Charged-device model (CDM), per AEC Q100-011 | All pins  | $\pm 750$                               | V          |

(1) AEC-Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specifications.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                            |  | MIN | MAX | UNIT |
|----------------------------|--|-----|-----|------|
| $V_{BB}$                   | Nominal supply voltage <sup>(1)</sup>  | 6   | 18  | V    |
| $V_{BB}$                   | Extended supply voltage <sup>(2)</sup> | 3   | 28  | V    |
| $V_{EN1}$ ,<br>$V_{EN2}$   | Enable voltage                         | -1  | 5.5 | V    |
| $V_{LATCH}$                | LATCH voltage                          | -1  | 5.5 | V    |
| $V_{DIA\_EN}$              | Diagnostic Enable voltage              | -1  | 5.5 | V    |
| $V_{SEL1}$ ,<br>$V_{SEL2}$ | Select voltage                         | -1  | 5.5 | V    |
| $V_{SNS}$                  | Sense voltage                          | -1  | 7   | V    |
| $T_A$                      | Operating free-air temperature         | -40 | 125 | °C   |

(1) All operating voltage conditions are measured with respect to device GND

(2) Device will function within extended operating range, however some parametric values might not apply

## 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> (2) |  | TPS2HB16-Q1  | UNIT |
|-----------------------------------|--|--------------|------|
|                                   |  | PWP (HTSSOP) |      |
|                                   |  | 16 PINS      |      |
| $R_{\theta JA}$                   | Junction-to-ambient thermal resistance       | 32.9         | °C/W |
| $R_{\theta JC(\text{top})}$       | Junction-to-case (top) thermal resistance    | 30.8         | °C/W |
| $R_{\theta JB}$                   | Junction-to-board thermal resistance         | 9.0          | °C/W |
| $\psi_{JT}$                       | Junction-to-top characterization parameter   | 1.8          | °C/W |
| $\psi_{JB}$                       | Junction-to-board characterization parameter | 9.2          | °C/W |
| $R_{\theta JC(\text{bot})}$       | Junction-to-case (bottom) thermal resistance | 2.0          | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

## 7.5 Electrical Characteristics

$V_{BB} = 6 \text{ V to } 18 \text{ V}$ ,  $T_J = -40^\circ\text{C to } 150^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                            | TEST CONDITIONS   | MIN   | TYP  | MAX | UNIT             |    |
|--------------------------------------|---|---|------|-----|------------------|----|
| <b>INPUT VOLTAGE AND CURRENT</b>     |   |   |      |     |                  |    |
| $V_{DSCLAMP}$                        | $V_{DS}$ clamp voltage  | 40  | 46   |     | V                |    |
| $V_{BBCLAMP}$                        | $V_{BB}$ clamp voltage  | 58  | 76   |     | V                |    |
| $V_{UVLOF}$                          | $V_{BB}$ undervoltage lockout falling                                 | Measured with respect to the GND pin of the device  | 2.0  | 3   | V                |    |
| $V_{UVLOR}$                          | $V_{BB}$ undervoltage lockout rising                                  | Measured with respect to the GND pin of the device  | 2.2  | 3   | V                |    |
| $I_{SB}$                             | Standby current (total device leakage including both MOSFET channels) | $V_{BB} = 13.5 \text{ V}$ , $T_J = 25^\circ\text{C}$<br>$V_{ENx} = V_{DIA\_EN} = 0 \text{ V}$ , $V_{OUT} = 0 \text{ V}$                 |      | 0.5 | $\mu\text{A}$    |    |
|                                      |   | $V_{BB} = 13.5 \text{ V}$ , $T_J = 125^\circ\text{C}$ ,<br>$V_{ENx} = V_{DIA\_EN} = 0 \text{ V}$ , $V_{OUT} = 0 \text{ V}$              |      | 4   | $\mu\text{A}$    |    |
| $I_{L_{NOM}}$                        | Continuous load current, per channel                                  | Two channels enabled, $T_{AMB} = 70^\circ\text{C}$  | 5    |     | A                |    |
|                                      |   | One channel enabled, $T_{AMB} = 70^\circ\text{C}$   | 7    |     | A                |    |
| $I_{OUT(\text{standby})}$            | Output leakage current (per channel)                                  | $V_{BB} = 13.5 \text{ V}$ , $T_J = 25^\circ\text{C}$<br>$V_{ENx} = V_{DIA\_EN} = 0 \text{ V}$ , $V_{OUT} = 0 \text{ V}$                 | 0.01 | 0.5 | $\mu\text{A}$    |    |
|                                      |   | $V_{BB} = 13.5 \text{ V}$ , $T_J = 125^\circ\text{C}$<br>$V_{ENx} = V_{DIA\_EN} = 0 \text{ V}$ , $V_{OUT} = 0 \text{ V}$                |      | 1.5 | $\mu\text{A}$    |    |
| $I_{DIA}$                            | Current consumption in diagnostic mode                                | $V_{BB} = 13.5 \text{ V}$ , $I_{SNS} = 0 \text{ mA}$<br>$V_{ENx} = 0 \text{ V}$ , $V_{DIA\_EN} = 5 \text{ V}$ , $V_{OUT} = 0 \text{ V}$ | 3    | 6   | mA               |    |
| $I_Q$                                | Quiescent current   | $V_{BB} = 13.5 \text{ V}$<br>$V_{ENx} = V_{DIA\_EN} = 5 \text{ V}$ , $I_{OUTx} = 0 \text{ A}$   | 3    | 6   | mA               |    |
| $t_{STBY}$                           | Standby mode delay time   | $V_{ENx} = V_{DIA\_EN} = 0 \text{ V}$ to standby  | 12   | 17  | 22               | ms |
| <b>RON CHARACTERISTICS</b>           |   |   |      |     |                  |    |
| $R_{ON}$                             | On-resistance (Includes MOSFET and package)                           | $T_J = 25^\circ\text{C}$ , $6 \text{ V} \leq V_{BB} \leq 28 \text{ V}$ , $I_{OUT1} = I_{OUT2} > 1 \text{ A}$                            | 16   |     | $\text{m}\Omega$ |    |
|                                      |   | $T_J = 150^\circ\text{C}$ , $6 \text{ V} \leq V_{BB} \leq 28 \text{ V}$ , $I_{OUT1} = I_{OUT2} > 1 \text{ A}$                           |      | 40  | $\text{m}\Omega$ |    |
|                                      |   | $T_J = 25^\circ\text{C}$ , $3 \text{ V} \leq V_{BB} \leq 6 \text{ V}$ , $I_{OUT1} = I_{OUT2} > 1 \text{ A}$                             |      | 30  | $\text{m}\Omega$ |    |
| $R_{ON(\text{REV})}$                 | On-resistance during reverse polarity                                 | $T_J = 25^\circ\text{C}$ , $-18 \text{ V} \leq V_{BB} \leq -8 \text{ V}$  | 16   |     | $\text{m}\Omega$ |    |
|                                      |   | $T_J = 105^\circ\text{C}$ , $-18 \text{ V} \leq V_{BB} \leq -8 \text{ V}$   |      | 40  | $\text{m}\Omega$ |    |
| <b>CURRENT SENSE CHARACTERISTICS</b> |   |   |      |     |                  |    |
| $K_{SNS}$                            | Current sense ratio $I_{OUTx} / I_{SNS}$                              | $I_{OUTx} = 1 \text{ A}$  | 3000 |     |                  |    |

## Electrical Characteristics (continued)

$V_{BB} = 6 \text{ V to } 18 \text{ V}$ ,  $T_J = -40^\circ\text{C to } 150^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                     |   | TEST CONDITIONS  | MIN  | TYP    | MAX   | UNIT  |        |
|-------------------------------|---|--|--|--------|-------|-------|--------|
| I <sub>SNSI</sub>             | Current sense current and accuracy                      | $V_{EN} = V_{DIA\_EN} = 5 \text{ V}$ ,<br>$V_{SEL1} = 0 \text{ V}$ , $V_{SEL2} = X$  | I <sub>OUT</sub> = 6 A                         | 2.000  |       | mA    |        |
|                               |   |  |  | -5     | 5.3   | %     |        |
|                               |   |  | I <sub>OUT</sub> = 3 A                         | 1.000  |       | mA    |        |
|                               |   |  |  | -5     | 5.3   | %     |        |
|                               |   |  | I <sub>OUT</sub> = 1 A                         | 0.333  |       | mA    |        |
|                               |   |  |  | -5     | 5.3   | %     |        |
|                               |   |  | I <sub>OUT</sub> = 300 mA                      | 0.1    |       | mA    |        |
|                               |   |  |  | -6     | 6.3   | %     |        |
|                               |   |  | I <sub>OUT</sub> = 100 mA                      | 0.0322 |       | mA    |        |
|                               |   |  |  | -9     | 9.6   | %     |        |
|                               |   |  | I <sub>OUT</sub> = 50 mA                       | 0.0154 |       | mA    |        |
|                               |   |  |  | -19.5  | 18.7  | %     |        |
|                               |   |  | I <sub>OUT</sub> = 20 mA                       | 0.0054 |       | mA    |        |
|                               |   |  |  | -59.3  | 53.1  | %     |        |
| TJ SENSE CHARACTERISTICS      |   |  |  |        |       |       |        |
| I <sub>SNST</sub>             | Temperature sense current<br>Device Version A/B         | $V_{DIA\_EN} = 5 \text{ V}$ , $V_{SEL1} = 5 \text{ V}$ , $V_{SEL2} = 0 \text{ V}$  | T <sub>J</sub> = -40°C                         | 0.00   | 0.12  | 0.29  | mA     |
|                               |   |  | T <sub>J</sub> = 25°C                          | 0.68   | 0.85  | 1.02  | mA     |
|                               |   |  | T <sub>J</sub> = 85°C                          | 1.25   | 1.52  | 1.79  | mA     |
|                               |   |  | T <sub>J</sub> = 125°C                         | 1.61   | 1.96  | 2.31  | mA     |
|                               |   |  | T <sub>J</sub> = 150°C                         | 1.80   | 2.25  | 2.70  | mA     |
| dI <sub>SNST</sub> /dT        | Coefficient   |  |  |        | 0.011 |       | mA/°C  |
| SNS CHARACTERISTICS           |   |  |  |        |       |       |        |
| I <sub>SNSFH</sub>            | I <sub>SNS</sub> fault high-level                       | $V_{DIA\_EN} = 5 \text{ V}$ , $V_{SEL1} = 0 \text{ V}$ , $V_{SEL2} = X$  |  | 4      | 4.5   | 5.3   | mA     |
| I <sub>SNSleak</sub>          | I <sub>SNS</sub> leakage                                | $V_{DIA\_EN} = 0 \text{ V}$  |  |        |       | 1     | µA     |
| CURRENT LIMIT CHARACTERISTICS |   |  |  |        |       |       |        |
| I <sub>CL</sub>               | Current Limit Threshold                                 | Device Version A, T <sub>J</sub> = -40°C to 150°C  | R <sub>ILIM</sub> = GND, open, or out of range |        | 29.1  |       | A      |
|                               |   |  | R <sub>ILIM</sub> = 5 kΩ                       | 17.4   | 22    | 29.3  | A      |
|                               |   |  | R <sub>ILIM</sub> = 25 kΩ                      | 2.66   | 4.1   | 5.46  | A      |
|                               |   |  | R <sub>ILIM</sub> = GND, open, or out of range |        | 67.5  |       | A      |
|                               |   | Device Version B, T <sub>J</sub> = -40°C to 150°C  | R <sub>ILIM</sub> = 5 kΩ                       | 38     | 48.5  | 65    | A      |
|                               |   |  | R <sub>ILIM</sub> = 25 kΩ                      | 8.1    | 10.3  | 13.7  | A      |
|                               |   |  | T <sub>J</sub> = -40°C to 60°C                 | 51.65  | 60    | 76.32 | A      |
|                               |   |  | T <sub>J</sub> = 150°C                         | 42.16  | 48.00 | 57.60 | A      |
|                               |   | Device Version F   | Version A                                      |        | 102   |       | A * kΩ |
|                               |   |  | Version B                                      |        | 258   |       | A * kΩ |
| FAULT CHARACTERISTICS         |   |  |  |        |       |       |        |
| V <sub>OL</sub>               | Open-load (OL) detection voltage                        | $V_{ENx} = 0 \text{ V}$ , $V_{DIA\_EN} = 5 \text{ V}$  |  | 2      | 3     | 4     | V      |
| t <sub>OL1</sub>              | OL and STB indication-time from ENx falling             | $V_{ENx} = 5 \text{ V to } 0 \text{ V}$ , $V_{DIA\_EN} = 5 \text{ V}$ , $V_{SEL1} = 0 \text{ V}^{(1)}$<br>I <sub>OUT</sub> = 0 mA, V <sub>OUTx</sub> = 4 V |  | 300    | 500   | 700   | µs     |
| t <sub>OL2</sub>              | OL and STB indication-time from DIA_EN rising           | $V_{ENx} = 0 \text{ V}$ , $V_{DIA\_EN} = 0 \text{ V to } 5 \text{ V}$ , $V_{SEL1} = 0 \text{ V}^{(1)}$<br>I <sub>OUT</sub> = 0 mA, V <sub>OUTx</sub> = 4 V |  |        |       | 50    | µs     |
| t <sub>OL3</sub>              | OL and STB indication-time from V <sub>OUT</sub> rising | $V_{ENx} = 0 \text{ V}$ , $V_{DIA\_EN} = 5 \text{ V}$ , $V_{SEL1} = 0 \text{ V}^{(1)}$<br>I <sub>OUT</sub> = 0 mA, V <sub>OUTx</sub> = 0 V to 4 V          |  |        |       | 50    | µs     |

(1) SELx must be set to select the relevant channel. Diagnostics are performed on Channel 1 when SELx = 00 and diagnostics are performed on channel 2 when SELx = 01

## Electrical Characteristics (continued)

$V_{BB} = 6 \text{ V to } 18 \text{ V}$ ,  $T_J = -40^\circ\text{C to } 150^\circ\text{C}$  (unless otherwise noted)

| PARAMETER  |                                | TEST CONDITIONS   | MIN | TYP | MAX | UNIT |
|--|--------------------------------|---|-----|-----|-----|------|
| $T_{ABS}$  | Thermal shutdown               |   |     | 150 |     | °C   |
| $T_{REL}$  | Relative thermal shutdown      |   |     | 50  |     | °C   |
| $T_{HYS}$  | Thermal shutdown hysteresis    |   |     | 28  |     | °C   |
| $t_{FAULT}$  | Fault shutdown indication-time | $V_{DIA\_EN} = 5 \text{ V}$<br>Time between switch shutdown and $I_{SNS}$ settling at $I_{SNSFH}$ |     |     | 50  | μs   |
| $t_{RETRY}$  | Retry time                     | Time from fault shutdown until switch re-enable (thermal shutdown or current limit).              | 1   | 2   | 3   | ms   |
| <b>EN1 AND EN2 PIN CHARACTERISTICS<sup>(2)</sup></b> |                                |   |     |     |     |      |
| $V_{IL, ENx}$  | Input voltage low-level        | No GND network diode  |     |     | 0.8 | V    |
| $V_{IH, ENx}$  | Input voltage high-level       | No GND network diode  | 2   |     |     | V    |
| $V_{IHYS, ENx}$                                      | Input voltage hysteresis       |   |     | 350 |     | mV   |
| $R_{ENx}$  | Internal pulldown resistor     |   | 0.5 | 1   | 2   | MΩ   |
| $I_{IL, EN}$   | Input current low-level        | $V_{EN} = 0.8 \text{ V}$  |     | 0.8 |     | μA   |
| $I_{IH, EN}$   | Input current high-level       | $V_{EN} = 5 \text{ V}$  |     | 5   |     | μA   |
| <b>DIA_EN PIN CHARACTERISTICS<sup>(2)</sup></b>      |                                |   |     |     |     |      |
| $V_{IL, DIA\_EN}$                                    | Input voltage low-level        | No GND network diode  |     |     | 0.8 | V    |
| $V_{IH, DIA\_EN}$                                    | Input voltage high-level       | No GND network diode  | 2.0 |     |     | V    |
| $V_{IHYS, DIA\_EN}$                                  | Input voltage hysteresis       |   |     | 350 |     | mV   |
| $R_{DIA\_EN}$  | Internal pulldown resistor     |   | 0.5 | 1   | 2   | MΩ   |
| $I_{IL, DIA\_EN}$                                    | Input current low-level        | $V_{DIA\_EN} = 0.8 \text{ V}$   |     | 0.8 |     | μA   |
| $I_{IH, DIA\_EN}$                                    | Input current high-level       | $V_{DIA\_EN} = 5 \text{ V}$   |     | 5.0 |     | μA   |
| <b>SEL1 AND SEL2 PIN Characteristics</b>             |                                |   |     |     |     |      |
| $V_{IL, SELx}$                                       | Input voltage low-level        | No GND network diode  |     |     | 0.8 | V    |
| $V_{IH, SELx}$                                       | Input voltage high-level       | No GND network diode  | 2   |     |     | V    |
| $V_{IHYS, SELx}$                                     | Input voltage hysteresis       |   |     | 350 |     | mV   |
| $R_{SELx}$   | Internal pulldown resistor     |   | 0.5 | 1   | 2   | MΩ   |
| $I_{IL, SELx}$                                       | Input current low-level        | $V_{SELx} = 0.8 \text{ V}$  |     | 0.8 |     | μA   |
| $I_{IH, SELx}$                                       | Input current high-level       | $V_{SELx} = 5 \text{ V}$  |     | 5   |     | μA   |
| <b>LATCH PIN CHARACTERISTICS<sup>(2)</sup></b>       |                                |   |     |     |     |      |
| $V_{IL, LATCH}$                                      | Input voltage low-level        | No GND network diode  |     |     | 0.8 | V    |
| $V_{IH, LATCH}$                                      | Input voltage high-level       | No GND network diode  | 2.0 |     |     | V    |
| $V_{IHYS, LATCH}$                                    | Input voltage hysteresis       |   |     | 350 |     | mV   |
| $R_{LATCH}$  | Internal pulldown resistor     |   | 0.5 | 1   | 2   | MΩ   |
| $I_{IL, LATCH}$                                      | Input current low-level        | $V_{LATCH} = 0.8 \text{ V}$   |     | 0.8 |     | μA   |
| $I_{IH, LATCH}$                                      | Input current high-level       | $V_{LATCH} = 5 \text{ V}$   |     | 5.0 |     | μA   |

(2)  $V_{BB} = 3 \text{ V to } 28 \text{ V}$

## 7.6 SNS Timing Characteristics

$V_{BB} = 6 \text{ V to } 18 \text{ V}$ ,  $T_J = -40^\circ\text{C to } +150^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                         |  | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|-----------------------------------|--|--|-----|-----|-----|------|
| <b>SNS TIMING - CURRENT SENSE</b> |  |  |     |     |     |      |
| $t_{SNSION1}$                     | Settling time from rising edge of DIA_EN | $V_{ENx} = 5 \text{ V}$ , $V_{DIA\_EN} = 0 \text{ V to } 5 \text{ V}$<br>$R_{SNS} = 1 \text{ k}\Omega$ , $R_L \leq 4 \Omega$ |     |     | 40  | μs   |

## SNS Timing Characteristics (continued)

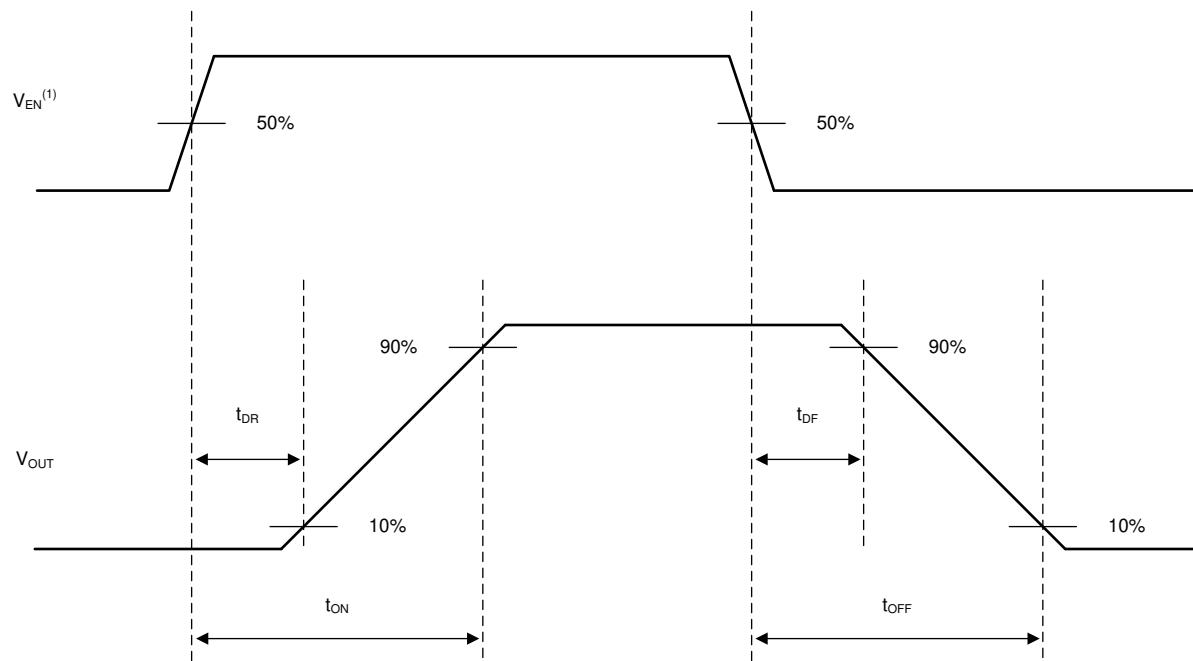
$V_{BB} = 6 \text{ V to } 18 \text{ V}$ ,  $T_J = -40^\circ\text{C to } +150^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                             |   | TEST CONDITIONS   | MIN | TYP | MAX | UNIT          |
|---------------------------------------|---|---|-----|-----|-----|---------------|
| $t_{SNSION2}$                         | Settling time from rising edge of ENx and DIA_EN      | $V_{ENx} = V_{DIA\_EN} = 0 \text{ V to } 5 \text{ V}$<br>$R_{SNS} = 1 \text{ k}\Omega$ , $R_L \leq 4 \Omega$  |     |     | 165 | $\mu\text{s}$ |
| $t_{SNSION3}$                         | Settling time from rising edge of ENx                 | $V_{ENx} = 0 \text{ V to } 5 \text{ V}$ , $V_{DIA\_EN} = 5 \text{ V}$<br>$R_{SNS} = 1 \text{ k}\Omega$ , $R_L \leq 4 \Omega$  |     |     | 165 | $\mu\text{s}$ |
| $t_{SNSIOFF1}$                        | Settling time from falling edge of DIA_EN             | $V_{ENx} = 5 \text{ V}$ , $V_{DIA\_EN} = 5 \text{ V to } 0 \text{ V}$<br>$R_{SNS} = 1 \text{ k}\Omega$ , $R_L \leq 4 \Omega$  |     |     | 20  | $\mu\text{s}$ |
| $t_{SETTLEH}$                         | Settling time from rising edge of load step           | $V_{ENx} = 5 \text{ V}$ , $V_{DIA\_EN} = 5 \text{ V}$<br>$R_{SNS} = 1 \text{ k}\Omega$ , $I_{OUT} = 5 \text{ A to } 1 \text{ A}$  |     |     | 20  | $\mu\text{s}$ |
| $t_{SETTLEL}$                         | Settling time from falling edge of load step          | $V_{ENx} = 5 \text{ V}$ , $V_{DIA\_EN} = 5 \text{ V}$<br>$R_{SNS} = 1 \text{ k}\Omega$ , $I_{OUT} = 5 \text{ A to } 1 \text{ A}$  |     |     | 20  | $\mu\text{s}$ |
| <b>SNS TIMING - TEMPERATURE SENSE</b> |   |   |     |     |     |               |
| $t_{SNSTON1}$                         | Settling time from rising edge of DIA_EN              | $V_{ENx} = 5 \text{ V}$ , $V_{DIA\_EN} = 0 \text{ V to } 5 \text{ V}$<br>$R_{SNS} = 1 \text{ k}\Omega$  |     |     | 40  | $\mu\text{s}$ |
| $t_{SNSTON2}$                         | Settling time from rising edge of DIA_EN              | $V_{ENx} = 0 \text{ V}$ , $V_{DIA\_EN} = 0 \text{ V to } 5 \text{ V}$<br>$R_{SNS} = 1 \text{ k}\Omega$  |     |     | 70  | $\mu\text{s}$ |
| $t_{SNSTOFF}$                         | Settling time from falling edge of DIA_EN             | $V_{ENx} = X$ , $V_{DIA\_EN} = 5 \text{ V to } 0 \text{ V}$<br>$R_{SNS} = 1 \text{ k}\Omega$  |     |     | 20  | $\mu\text{s}$ |
| <b>SNS TIMING - MULTIPLEXER</b>       |   |   |     |     |     |               |
| $t_{MUX}$                             | Settling time from temperature sense to current sense | $V_{ENx} = X$ , $V_{DIA\_EN} = 5 \text{ V}$<br>$V_{SEL1} = 5 \text{ V to } 0 \text{ V}$ , $V_{SEL2} = X$<br>$R_{SNS} = 1 \text{ k}\Omega$ , $R_L \leq 4 \Omega$   |     |     | 60  | $\mu\text{s}$ |
|                                       | Settling time from current sense on CHx to CHy        | $V_{ENx} = X$ , $V_{DIA\_EN} = 5 \text{ V}$<br>$V_{SEL1} = 0 \text{ V}$ , $V_{SEL2} = 0 \text{ V to } 5 \text{ V}$<br>$R_{SNS} = 1 \text{ k}\Omega$ , $I_{OUT1} = 2 \text{ A}$ , $I_{OUT2} = 4 \text{ A}$ |     |     | 20  | $\mu\text{s}$ |
|                                       | Settling time from current sense to temperature sense | $V_{ENx} = X$ , $V_{DIA\_EN} = 5 \text{ V}$<br>$V_{SEL1} = 0 \text{ V to } 5 \text{ V}$ , $V_{SEL2} = X$<br>$R_{SNS} = 1 \text{ k}\Omega$ , $R_L \leq 4 \Omega$   |     |     | 60  | $\mu\text{s}$ |

## 7.7 Switching Characteristics

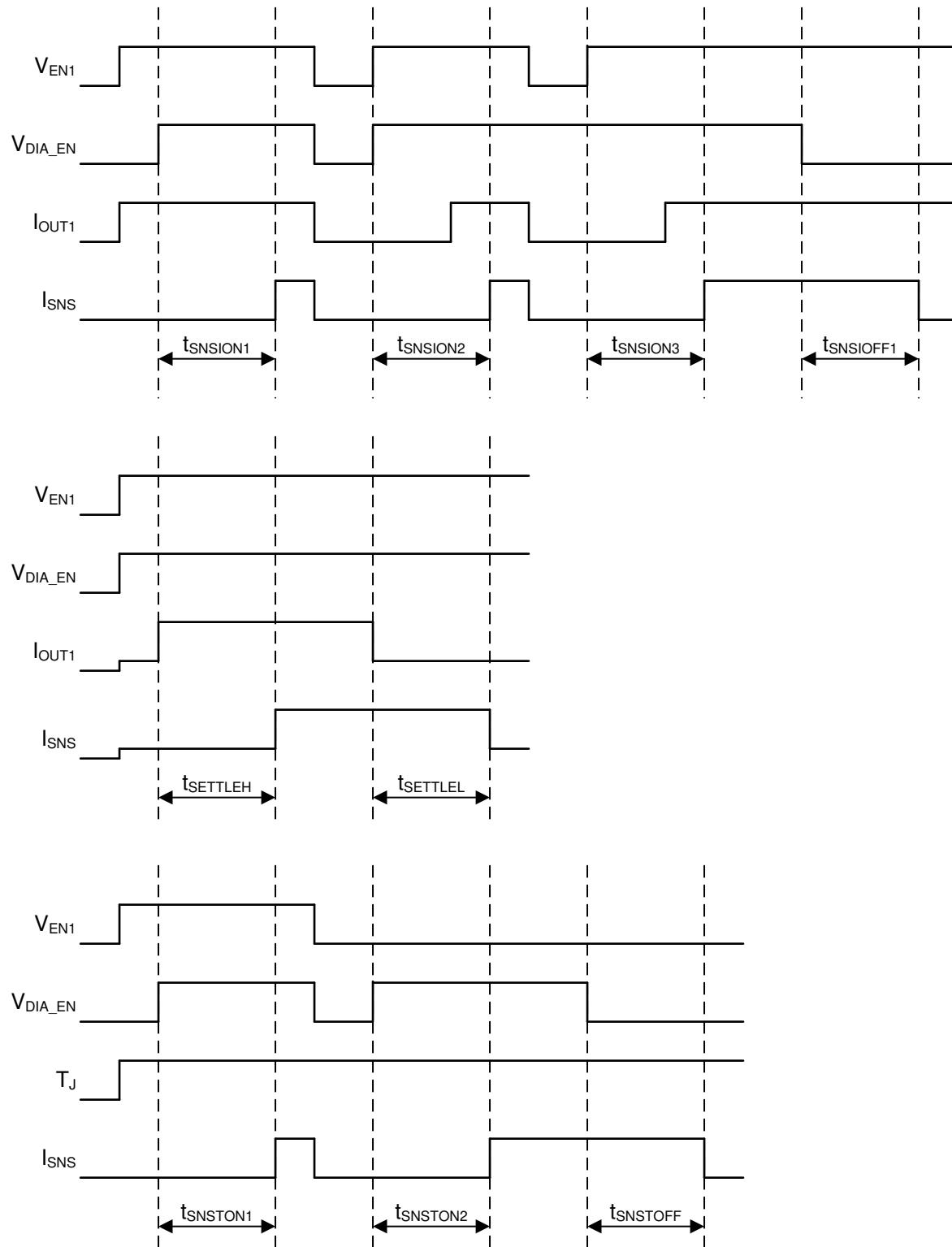
$V_{BB} = 13.5 \text{ V}$ ,  $T_J = -40^\circ\text{C to } +150^\circ\text{C}$  (unless otherwise noted)

| PARAMETER          |  | TEST CONDITIONS   | MIN | TYP | MAX | UNIT                   |
|--------------------|--|---|-----|-----|-----|------------------------|
| $t_{DR}$           | Turnon delay time                      | $V_{BB} = 13.5 \text{ V}$ , $R_L \leq 4 \Omega$ , 50% EN rising to 10% $V_{OUT}$ rising   | 20  | 60  | 100 | $\mu\text{s}$          |
| $t_{DF}$           | Turnoff delay time                     | $V_{BB} = 13.5 \text{ V}$ , $R_L \leq 4 \Omega$ , 50% EN falling to 90% $V_{OUT}$ Falling | 20  | 60  | 100 | $\mu\text{s}$          |
| $SR_R$             | $V_{OUTx}$ rising slew rate            | $V_{BB} = 13.5 \text{ V}$ , 20% to 80% of $V_{OUT}$ , $R_L \leq 4 \Omega$                 | 0.1 | 0.4 | 0.7 | $\text{V}/\mu\text{s}$ |
| $SR_F$             | $V_{OUTx}$ falling slew rate           | $V_{BB} = 13.5 \text{ V}$ , 80% to 20% of $V_{OUT}$ , $R_L \leq 4 \Omega$                 | 0.1 | 0.4 | 0.7 | $\text{V}/\mu\text{s}$ |
| $t_{ON}$           | Turnon time                            | $V_{BB} = 13.5 \text{ V}$ , $R_L \leq 4 \Omega$ , 50% EN rising to 80% $V_{OUT}$ rising   | 39  | 87  | 145 | $\mu\text{s}$          |
| $t_{OFF}$          | Turnoff time                           | $V_{BB} = 13.5 \text{ V}$ , $R_L \leq 4 \Omega$ , 50% EN rising to 80% $V_{OUT}$ rising   | 39  | 87  | 147 | $\mu\text{s}$          |
| $t_{ON} - t_{OFF}$ | Turnon and turnoff matching            | 200- $\mu\text{s}$ enable pulse   | -50 | 0   | 50  | $\mu\text{s}$          |
| $E_{ON}$           | Switching energy losses during turnon  | $V_{BB} = 13.5 \text{ V}$ , $R_L \leq 4 \Omega$   |     |     | 0.4 | $\text{mJ}$            |
| $E_{OFF}$          | Switching energy losses during turnoff | $V_{BB} = 13.5 \text{ V}$ , $R_L \leq 4 \Omega$   |     |     | 0.4 | $\text{mJ}$            |



Rise and fall time of  $V_{ENx}$  is 100 ns.

**Figure 1. Switching Characteristics Definitions**

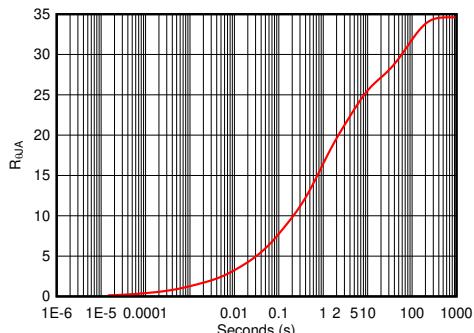


NOTE1: Rise and fall times of control signals are 100 ns. Control signals include: EN1, EN2, DIA\_EN, SEL1, SEL2.

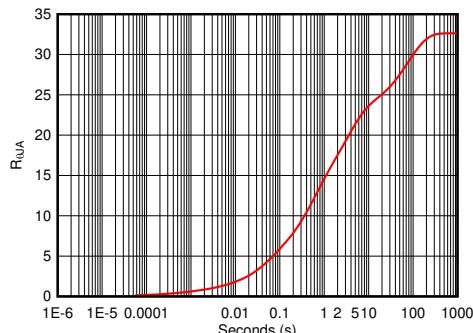
NOTE2: SEL1 and SEL2 must be set to the appropriate values.

**Figure 2. SNS Timing Characteristics Definitions**

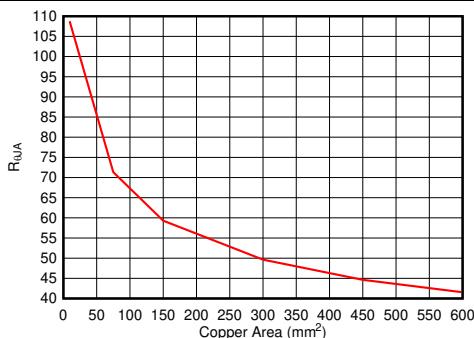
## 7.8 Typical Characteristics



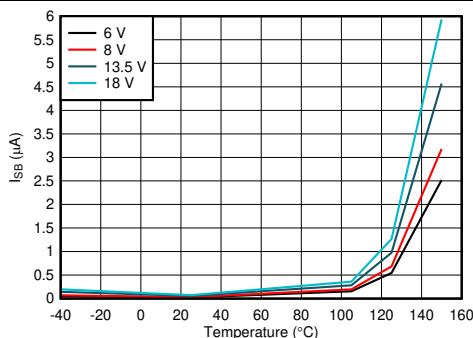
**Figure 3. Transient Thermal Impedance 1 Channel Enabled**



**Figure 4. Transient Thermal Impedance Both Channels Enabled**

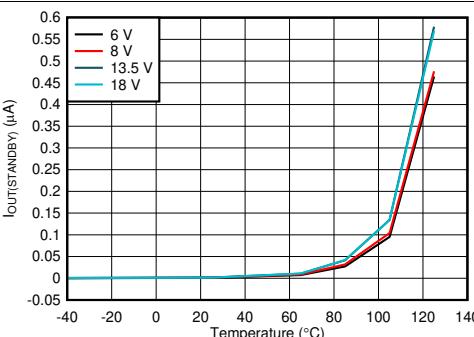


**Figure 5.  $R_{\theta JA}$  vs Copper Area**



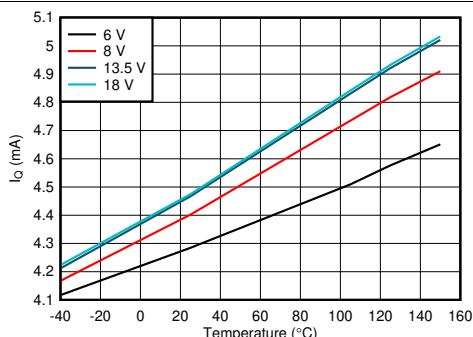
$V_{OUTX} = 0 \text{ V}$        $V_{ENX} = 0 \text{ V}$        $V_{DIAG\_EN} = 0 \text{ V}$

**Figure 6. Standby Current ( $I_{SB}$ ) vs Temperature**



$V_{OUTX} = 0 \text{ V}$        $V_{ENX} = 0 \text{ V}$        $V_{DIAG\_EN} = 0 \text{ V}$   
Both Channels

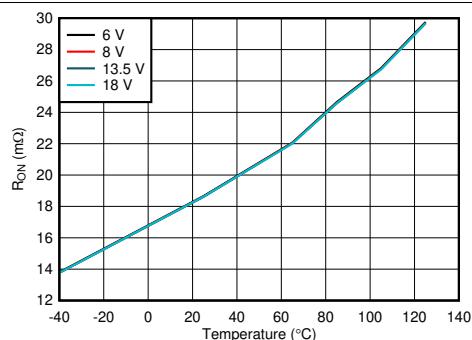
**Figure 7. Output Leakage Current ( $I_{OUT(standby)}$ ) vs Temperature**



$I_{OUTX} = 0 \text{ A}$        $V_{ENX} = 5 \text{ V}$        $V_{DIAG\_EN} = 5 \text{ V}$   
 $R_{SNS} = 1 \text{ k}\Omega$        $V_{SEL1} = V_{SEL2} = 0 \text{ V}$

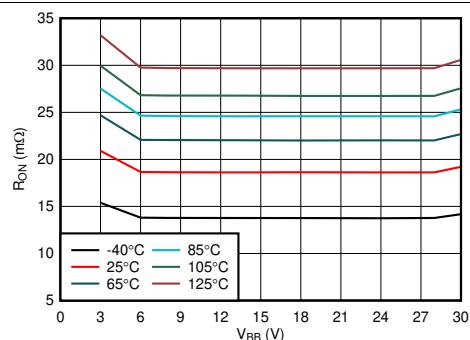
**Figure 8. Quiescent Current ( $I_Q$ ) vs Temperature**

## Typical Characteristics (continued)



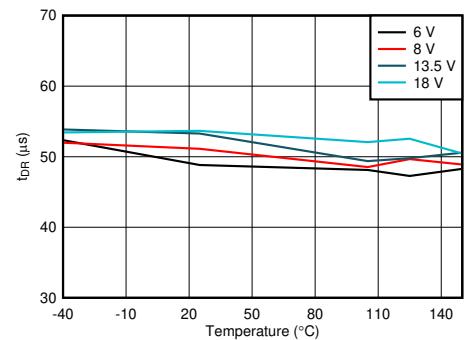
$I_{OUTX} = 200 \text{ mA}$        $V_{ENX} = 5 \text{ V}$        $V_{DIAG\_EN} = 0 \text{ V}$   
 $R_{SNS} = 1 \text{ k}\Omega$

**Figure 9. On Resistance ( $R_{ON}$ ) vs Temperature**



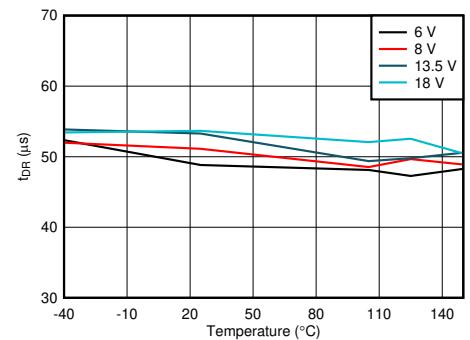
$I_{OUTX} = 200 \text{ mA}$        $V_{ENX} = 5 \text{ V}$        $V_{DIAG\_EN} = 0 \text{ V}$   
 $R_{SNS} = 1 \text{ k}\Omega$

**Figure 10. On Resistance ( $R_{ON}$ ) vs  $V_{BB}$**



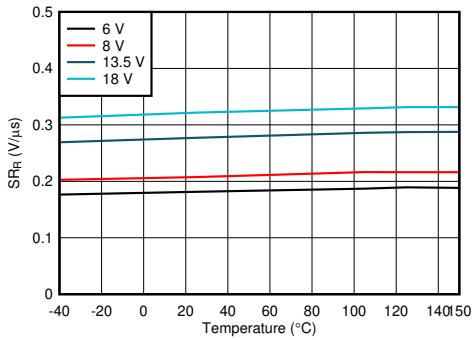
$R_{OUTX} = 2.6 \Omega$        $V_{ENX} = 0 \text{ V to } 5 \text{ V}$        $V_{DIAG\_EN} = 0 \text{ V}$   
 $R_{SNS} = 1 \text{ k}\Omega$

**Figure 11. Turn-on Delay Time ( $t_{DR}$ ) vs Temperature**



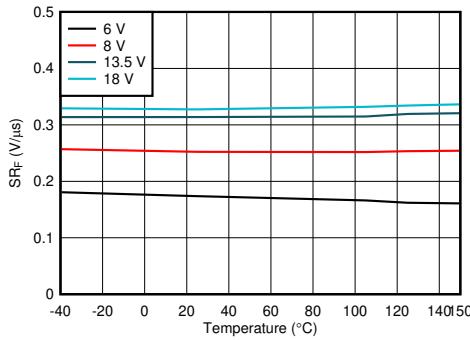
$R_{OUTX} = 2.6 \Omega$        $V_{ENX} = 5 \text{ V to } 0 \text{ V}$        $V_{DIAG\_EN} = 0 \text{ V}$   
 $R_{SNS} = 1 \text{ k}\Omega$

**Figure 12. Turn-off Delay Time ( $t_{DF}$ ) vs Temperature**



$R_{OUTX} = 2.6 \Omega$        $V_{ENX} = 0 \text{ V to } 5 \text{ V}$        $V_{DIAG\_EN} = 0 \text{ V}$   
 $R_{SNS} = 1 \text{ k}\Omega$

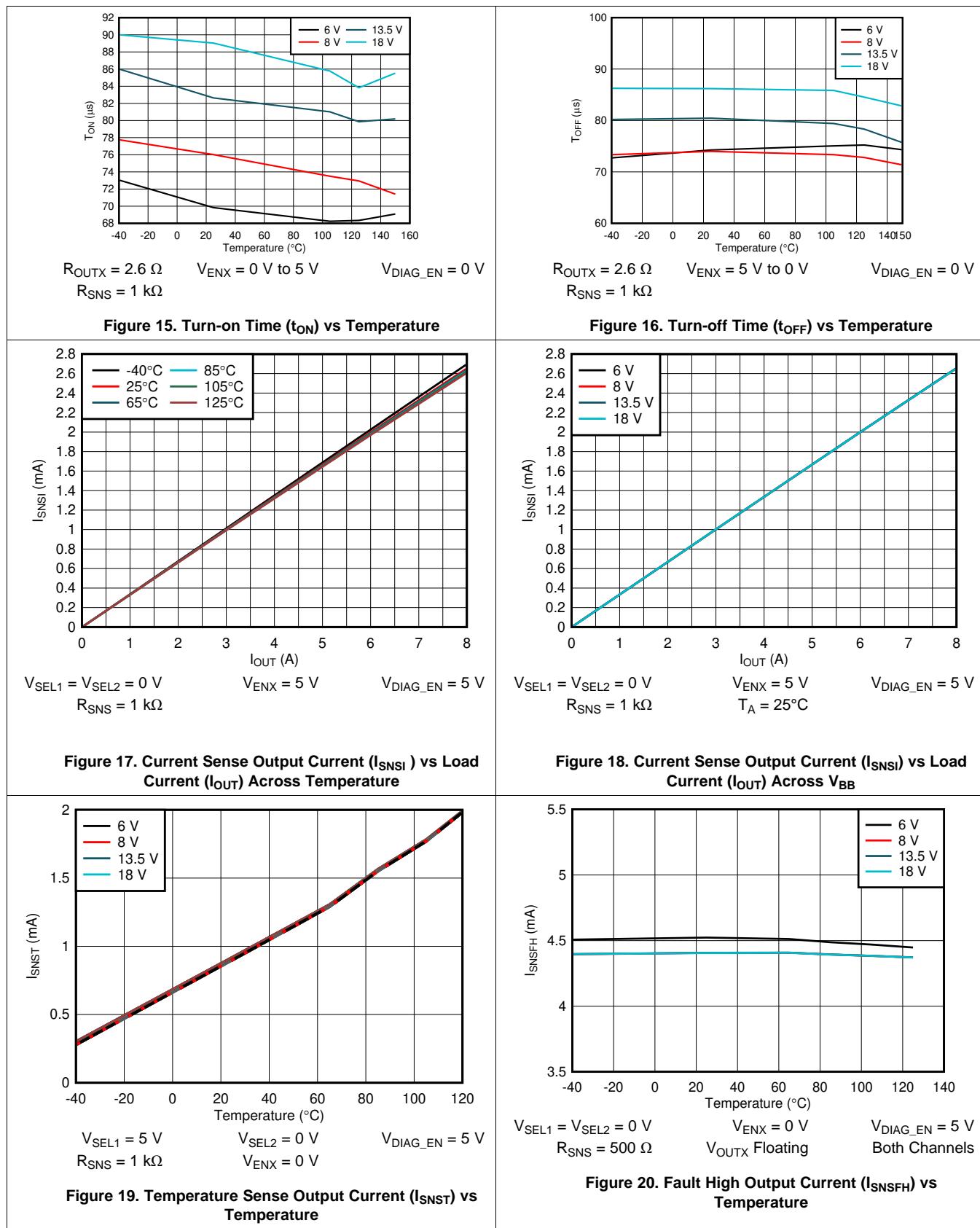
**Figure 13.  $V_{OUT}$  Slew Rate Rising (SR<sub>R</sub>) vs Temperature**



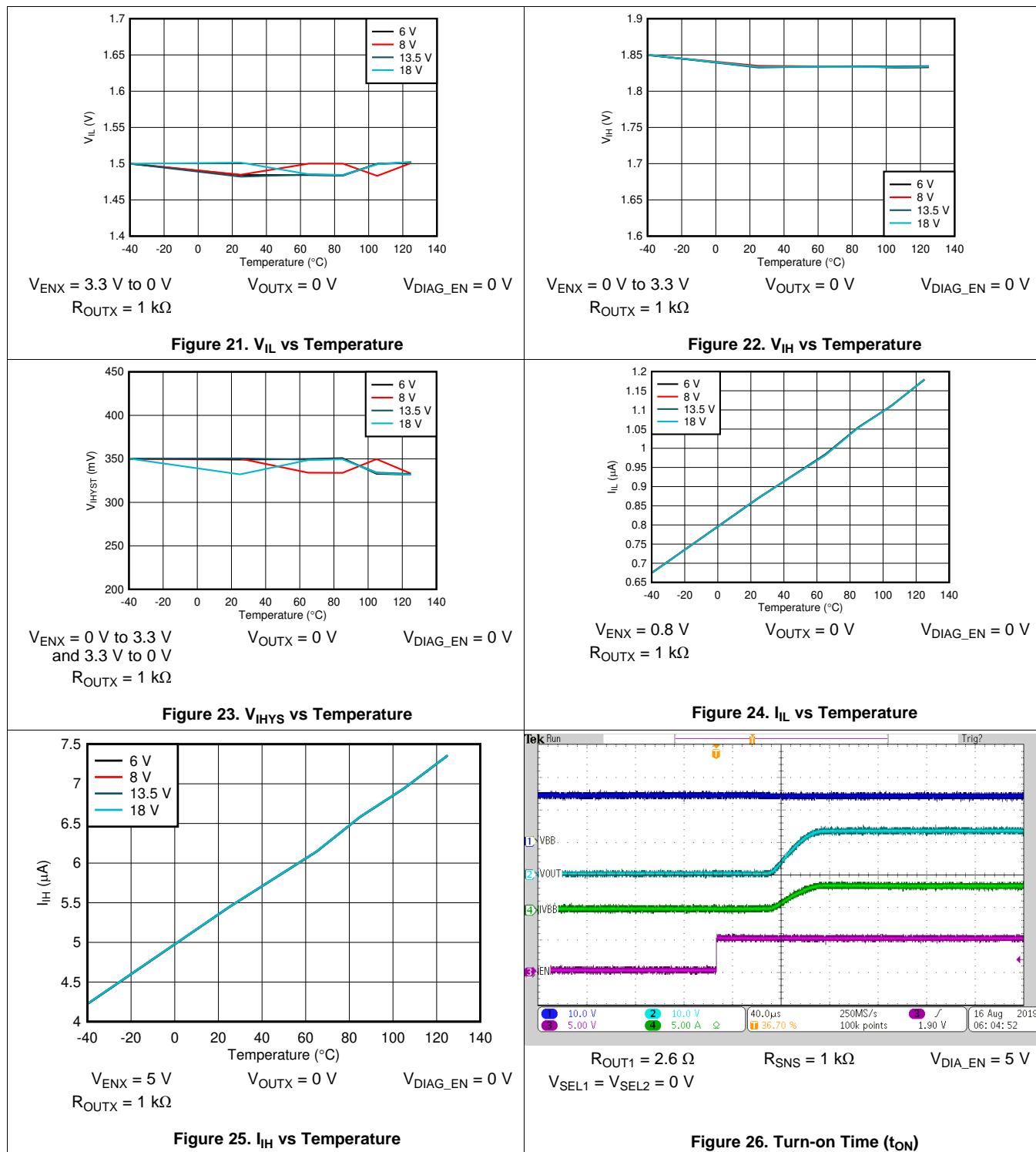
$R_{OUTX} = 2.6 \Omega$        $V_{ENX} = 5 \text{ V to } 0 \text{ V}$        $V_{DIAG\_EN} = 0 \text{ V}$   
 $R_{SNS} = 1 \text{ k}\Omega$

**Figure 14.  $V_{OUT}$  Slew Rate Falling (SR<sub>F</sub>) vs Temperature**

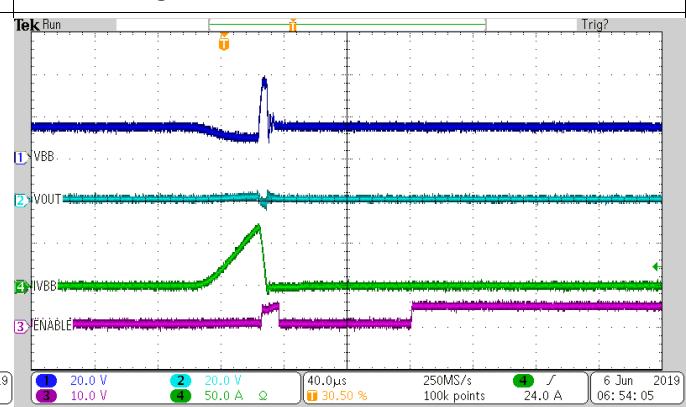
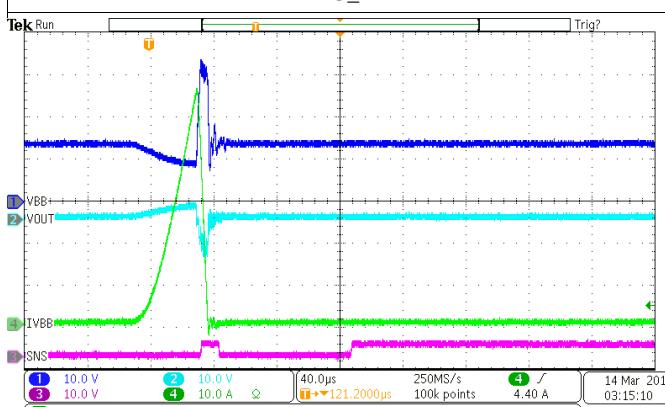
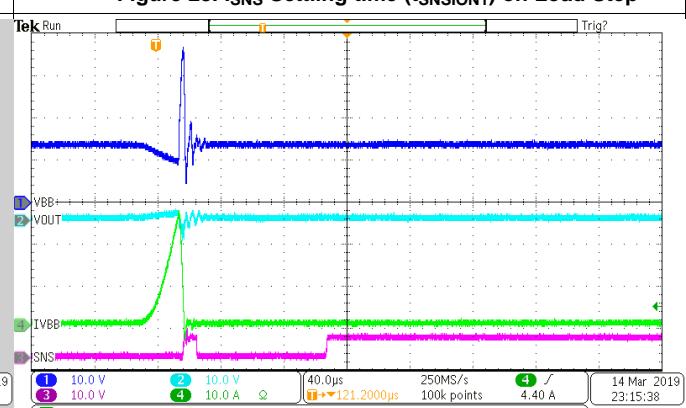
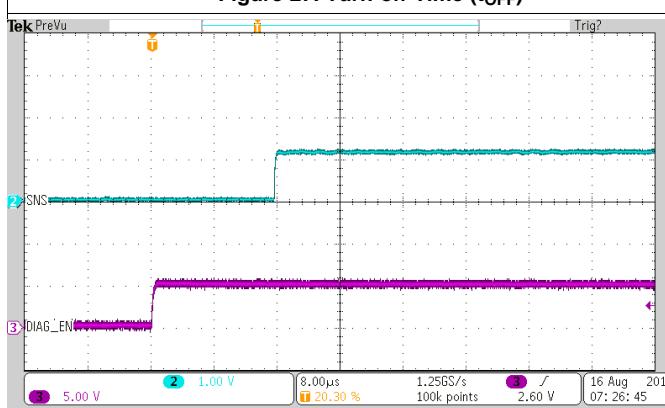
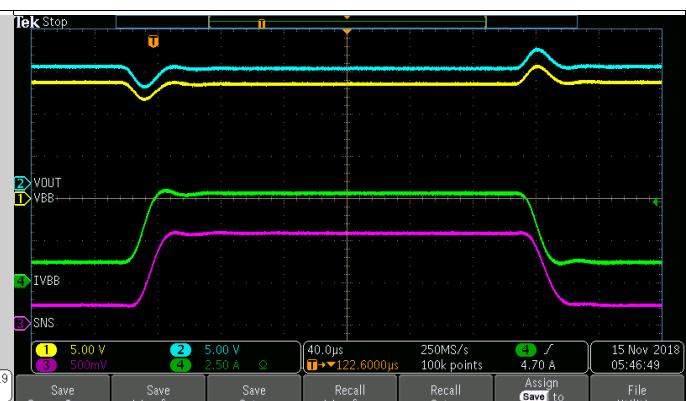
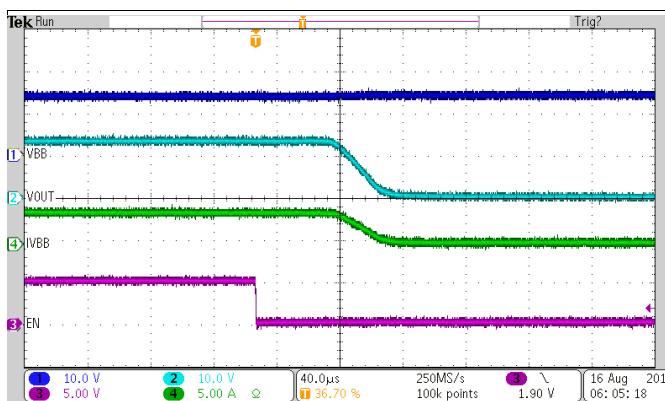
## Typical Characteristics (continued)



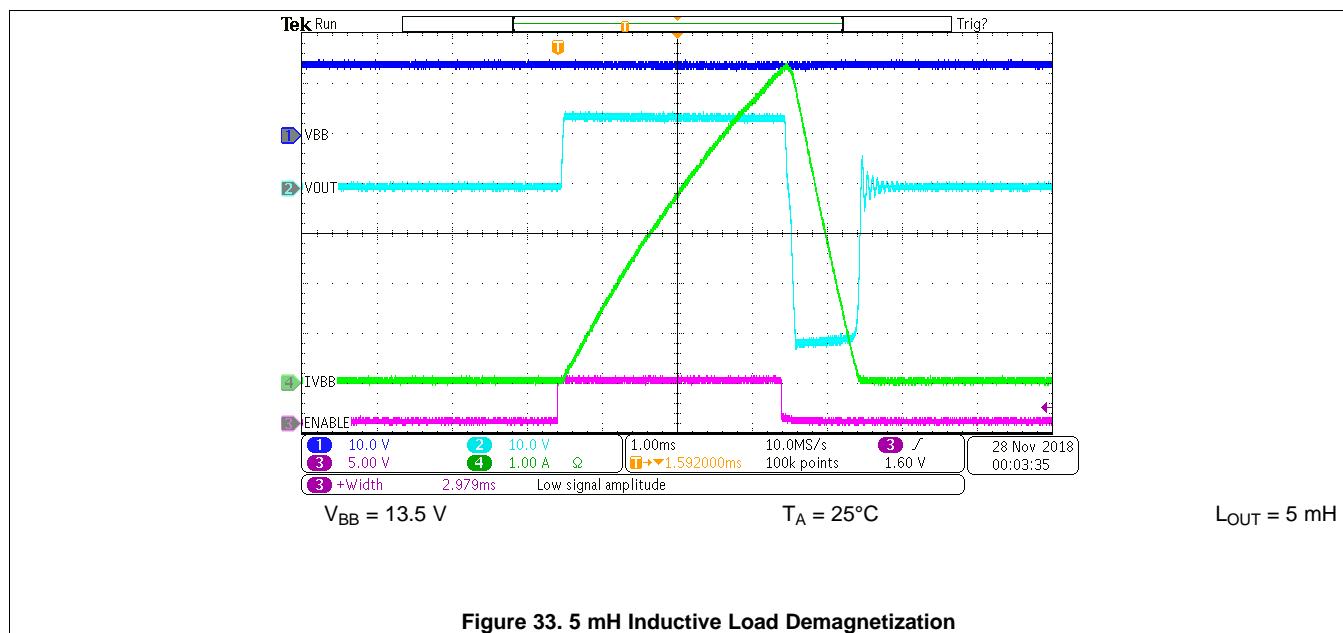
## Typical Characteristics (continued)



## Typical Characteristics (continued)



## Typical Characteristics (continued)



## 8 Parameter Measurement Information

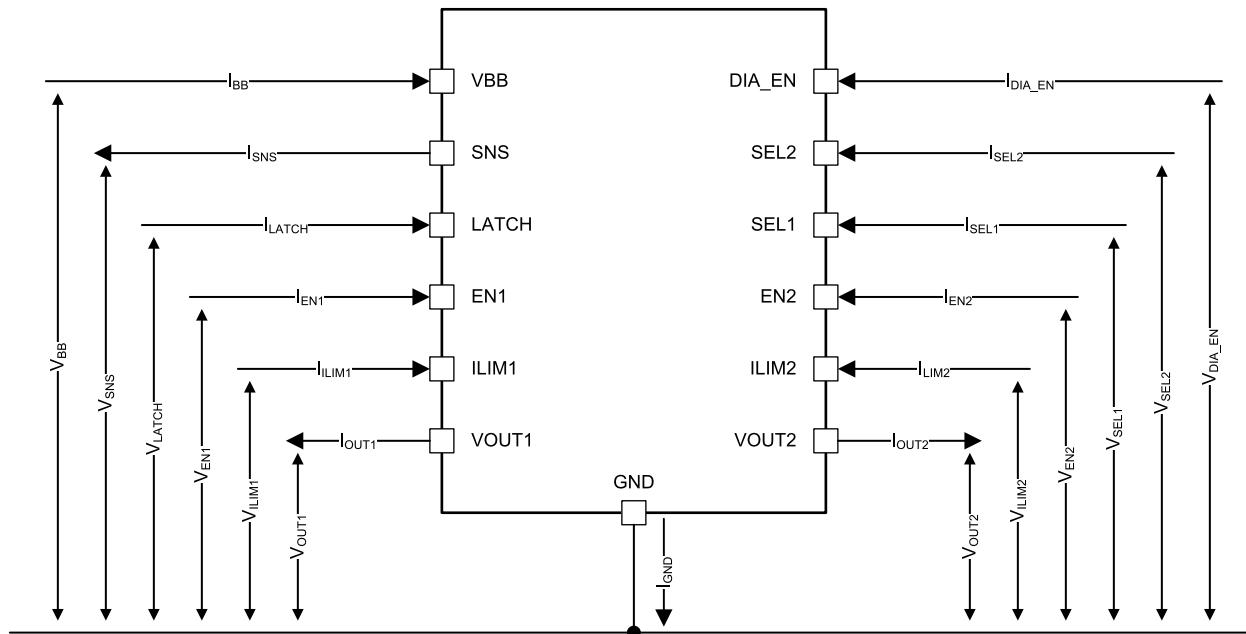


Figure 34. Parameter Definitions

## 9 Detailed Description

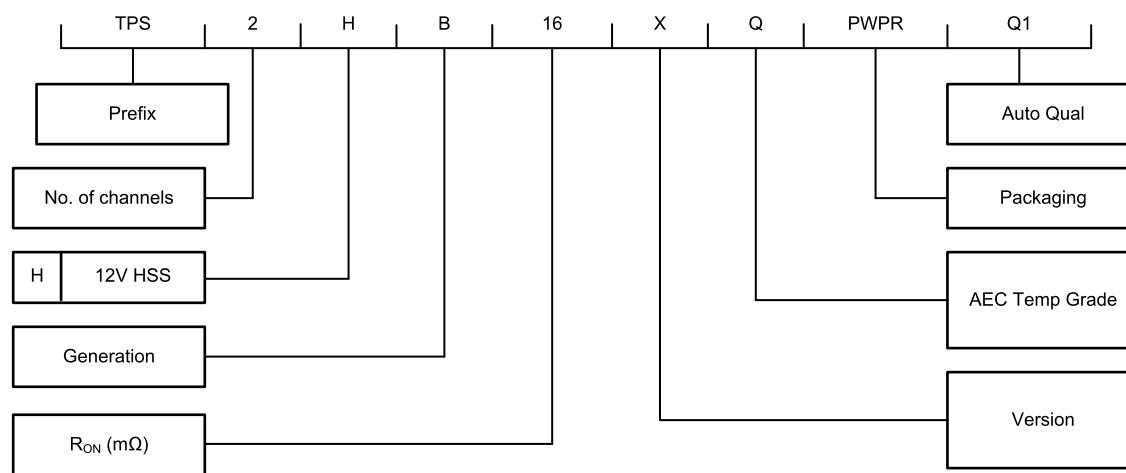
### 9.1 Overview

The TPS2HB16-Q1 device is a dual-channel smart high-side switch intended for use with 12-V automotive batteries. Many protection and diagnostic features are integrated in the device.

Diagnostics features include the analog SNS output that is capable of providing a signal that is proportional to load current or device temperature. The high-accuracy load current sense allows for diagnostics of complex loads. Version F of the device includes open drain FLT1 and FLT2 pins that indicates device fault states.

This device includes protection through thermal shutdown, current limiting, transient withstand, and reverse battery operation. For more details on the protection features, refer to the [Feature Description](#) and [Application Information](#) sections of the document.

The TPS2HB16-Q1 is one device in a family of TI high side switches. For each device, the part number indicates elements of the device behavior. [Figure 35](#) gives an example of the device nomenclature.

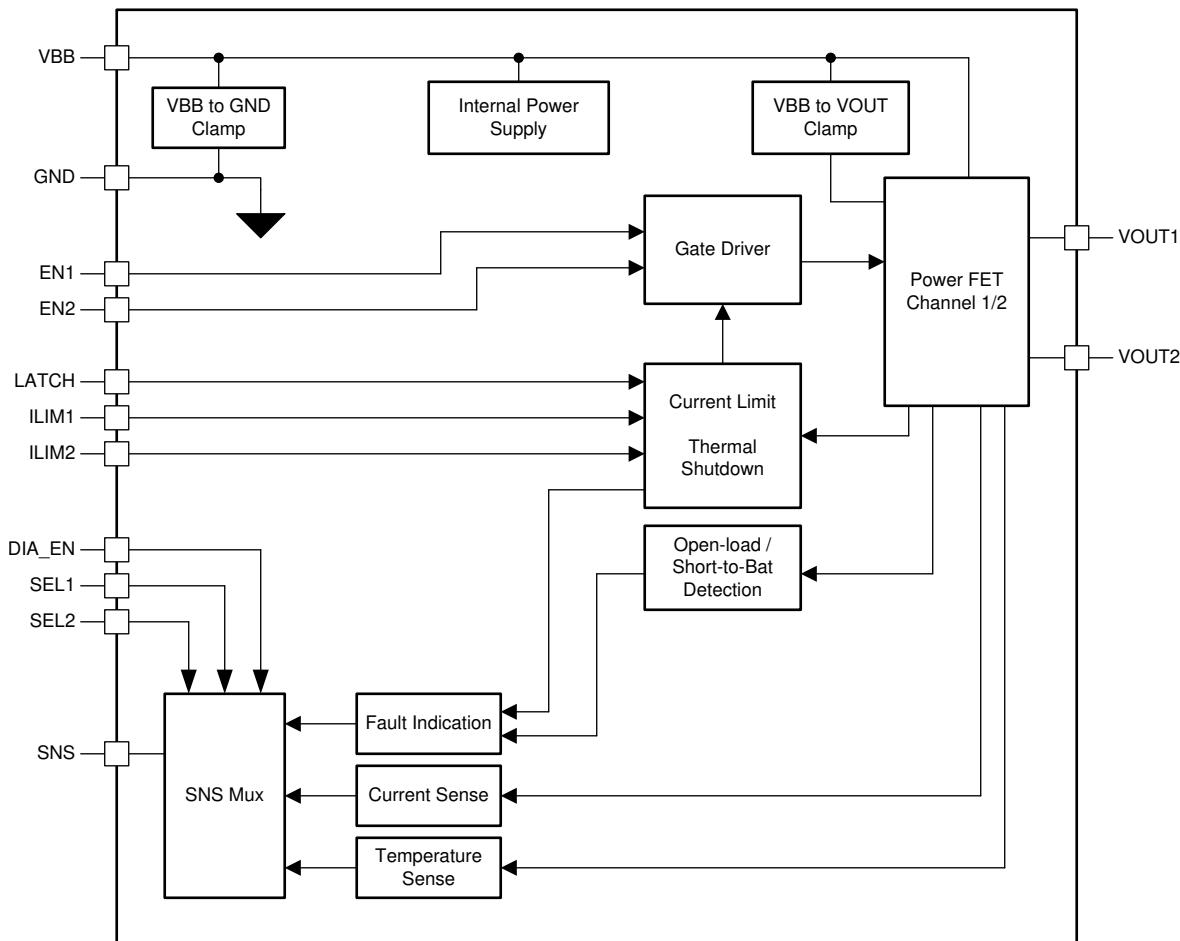


**Figure 35. Naming Convention**

## 9.2 Functional Block Diagram

The functional block diagram shown is for device versions A/B.

For version F, the ILIM1 and ILIM2 pins will be replaced by open drain outputs  $\overline{FLT1}$  and  $\overline{FLT2}$ .



## 9.3 Feature Description

### 9.3.1 Protection Mechanisms

The TPS2HB16-Q1 is designed to operate in the automotive environment. The protection mechanisms allow the device to be robust against many system-level events such as load dump, reverse battery, short-to-ground, and more.

There are two protection features which, if triggered, will cause the switch to automatically disable:

- Thermal Shutdown
- Current Limit

When any of these protections are triggered, the device will enter the FAULT state. In the FAULT state, the fault indication will be available on the SNS pin (see the [Diagnostic Mechanisms](#) section of the data sheet for more details). For version F of the device, the fault will also be indicated on the  $\overline{\text{FLT1}}$  or  $\overline{\text{FLT2}}$  pin, depending on the channel that recognizes the fault.

The switch is no longer held off and the fault indication is reset when all of the below conditions are met:

- LATCH pin is low
- $t_{\text{RETRY}}$  has expired
- All faults are cleared (thermal shutdown, current limit)

#### NOTE

CH1 and CH2 operate independently. If there is a fault on one channel, the other channel is not affected. On version F of the device,  $\overline{\text{FLT1}}$  and  $\overline{\text{FLT2}}$  each independently diagnose each channel output.

#### 9.3.1.1 Thermal Shutdown

The device includes a temperature sensor on each power FET and also within the controller portion of the device. There are two cases that the device will consider to be a thermal shutdown fault:

- $T_{\text{J,FET}} > T_{\text{ABS}}$
- $(T_{\text{J,FET}} - T_{\text{J,controller}}) > T_{\text{REL}}$

After the fault is detected, the relevant switch will turn off. Each channel is turned off based on the measurement of temperature sensor for that channel. Therefore, if the thermal fault is detected on only one channel, the other channel continues operation. If  $T_{\text{J,FET}}$  passes  $T_{\text{ABS}}$ , the fault is cleared when the switch temperature decreases by the hysteresis value,  $T_{\text{HYS}}$ . If instead the  $T_{\text{REL}}$  threshold is exceeded, the fault is cleared after  $T_{\text{RETRY}}$  passes.

#### 9.3.1.2 Current Limit

When  $I_{\text{OUT}}$  reaches the current limit threshold,  $I_{\text{CL}}$ , the channel will switch off immediately. The  $I_{\text{CL}}$  value will vary with slew rate and a fast current increase that occurs during a powered-on short circuit can temporarily go above the specified  $I_{\text{CL}}$  value. When the switch is in the FAULT state it will output an output current  $I_{\text{SNSFH}}$  on the SNS pin and on version F of the device, the fault will also be indicated on the corresponding  $\overline{\text{FLT}}$  pin.

During a short circuit event, the device will hit the  $I_{\text{CL}}$  value that is listed in the [Electrical Characteristics](#) table (for the given device version and  $R_{\text{ILIM}}$ ) and then turn the output off to protect the device. The device will register a short circuit event when the output current exceeds  $I_{\text{CL}}$ , however the measured maximum current may exceed the  $I_{\text{CL}}$  value due to the TPS2HB16-Q1 deglitch filter and turn-off time. The device is specified to protect itself during a short circuit event over the nominal supply voltage range (as defined in the [Electrical Characteristics](#) table) at 125°C.

The current limit specification in the datasheet is based on the part being enabled into a short circuit condition with 5- $\mu\text{H}$  inductor on the input and output and the input resistance being less than 10 m $\Omega$  and the output impedance less than 100 m $\Omega$ . When the part is enabled into this short circuit condition, the current will rise up to the threshold specified in the [Electrical Characteristics](#) table before it begins to shut off the current. The deglitch filter time for the device to react to the current threshold is 3  $\mu\text{s}$ . Therefore if you take Version A/B and subtract 3  $\mu\text{s}$  from the maximum current value, the current limit threshold will align with the value specified in the [Electrical Characteristics](#) table.

## Feature Description (continued)

### 9.3.1.2.1 Current Limit Foldback

Version B and F of the TPS2HB16-Q1 implement a current limit foldback feature that is designed to protect the device in the case of a long-term fault condition. If the device undergoes fault shutdown events (either of thermal shutdown or current limit) seven consecutive times, the current limit will be reduced to half of the original value. The device will revert back to the original current limit threshold if either of the following occurs:

- The device goes to standby mode.
- The switch turns on and turns off without any fault occurring.

Version A does not implement the current limit foldback due to the lower current limit causing less harm during repetitive long-term faults.

### 9.3.1.2.2 Programmable Current Limit

The TPS2HB16-Q1 includes an adjustable current limit. Some applications (for example, incandescent bulbs) will require a high current limit. Other applications can benefit from a lower current limit threshold. In general, wherever possible a lower current limit is recommended due to allowing system advantages through:

- Reduced size and cost in current carrying components such as PCB traces and module connectors
- Less disturbance at the power supply ( $V_{BB}$  pin) during a short circuit event
- Improved protection of the downstream load

To set the current limit threshold, connect a resistor from  $I_{LIM}$  to  $V_{BB}$ . The current limit threshold is determined by [Equation 1](#) ( $R_{ILIM}$  in  $k\Omega$ ):

$$I_{CL} = K_{CL} / R_{ILIM} \quad (1)$$

The  $R_{ILIM}$  range is between 5  $k\Omega$  and 25  $k\Omega$ . An  $R_{ILIM}$  resistor is required; however, in the fault case where the pin is floating, grounded, or outside of this range the current limit will default to an internal level that is defined in the [Specifications](#) section of this document.

#### NOTE

Capacitance on the  $I_{LIM}$  pin can cause  $I_{LIM}$  to go out of range during short circuit events. For accurate current limiting, place  $R_{ILIM}$  near to the device with short traces to ensure  $<5$  pF capacitance to GND on the  $I_{LIM}$  pin.

For device version F, there is no  $I_{LIMX}$  pin and the current limit is not adjustable. In this case, the device will current limit at the internal threshold  $I_{CL}$  as defined in the [Electrical Characteristics](#) section.

### 9.3.1.2.3 Undervoltage Lockout (UVLO)

The device monitors the supply voltage  $V_{BB}$  to prevent unpredicted behaviors in the event that the supply voltage is too low. When the supply voltage falls down to  $V_{UVLOF}$ , the output stage is shut down automatically. When the supply rises up to  $V_{UVLOR}$ , the device turns back on.

During an initial ramp of  $V_{BB}$  from 0 V at a ramp rate slower than 1 V/ms,  $V_{EN}$  pin will have to be  $V_{BB}$  held low until  $V_{BB}$  is above UVLO threshold (with respect to board ground) and the supply voltage to the device has reliably reached above the UVLO condition. For best operation, ensure that  $V_{BB}$  has risen above UVLO before setting the  $V_{EN}$  pin to high.

### 9.3.1.2.4 $V_{BB}$ During Short-to-Ground

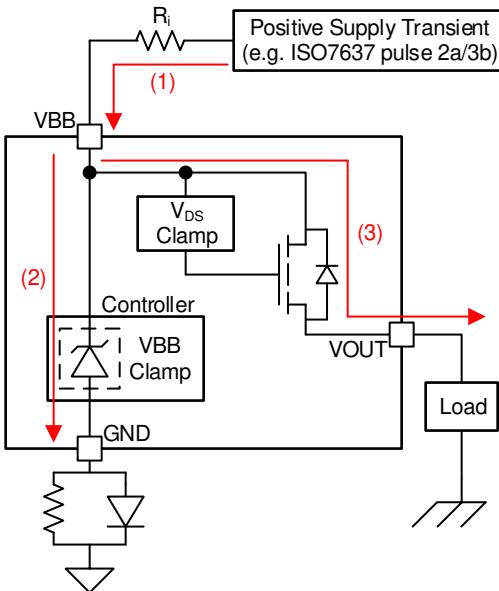
When  $V_{OUT}$  is shorted to ground, the module power supply ( $V_{BB}$ ) can have a transient decrease. This is caused by the sudden increase in current flowing through the wiring harness cables. To achieve ideal system behavior, it is recommended that the module maintain  $V_{BB} > 3$  V (above the maximum  $V_{UVLOF}$ ) during  $V_{OUT}$  short-to-ground. This is typically accomplished by placing bulk capacitance on the power supply node.

### 9.3.1.3 Voltage Transients

The TPS2HB16-Q1 device describes two types of voltage clamps which protect the FET against system-level voltage transients. The two different clamps are shown in [Figure 36](#).

## Feature Description (continued)

The clamp from  $V_{BB}$  to GND is primarily used to protect the controller from positive transients on the supply line (for example, ISO7637-2). The clamp from  $V_{BB}$  to  $V_{OUT}$  is primarily used to limit the voltage across the FET when switching off an inductive load. If the voltage potential from  $V_{BB}$  to GND exceeds the  $V_{BB}$  clamp level, the clamp will allow current to flow through the device from  $V_{BB}$  to GND (Path 2). If the voltage potential from  $V_{BB}$  to  $V_{OUT}$  exceeds the clamping voltage, the power FET will allow current to flow from  $V_{BB}$  to  $V_{OUT}$  (Path 3). Additional capacitance from  $V_{BB}$  to GND can increase the reliability of the system during ISO 7637 pulse 2-A testing.



**Figure 36. Current Path During Supply Voltage Transient**

### 9.3.1.3.1 Load Dump

The TPS2HB16-Q1 device is tested according to ISO 16750-2:2010(E) suppressed load dump pulse. The device supports up to 40-V load dump transient and will maintain normal operation during the load dump pulse. If the switch is enabled, it will stay enabled and if the switch is disabled, it will stay disabled.

### 9.3.1.4 Driving Inductive Loads

When switching off an inductive load, the inductor may impose a negative voltage on the output of the switch. The TPS2HB16-Q1 includes a voltage clamp to limit voltage across the FET. The maximum acceptable load inductance is a function of the device robustness.

For more information on driving inductive loads, refer to TI's [How To Drive Inductive, Capacitive, and Lighting Loads with Smart High Side Switches](#) application report.

### 9.3.1.5 Reverse Battery

In the reverse battery condition, the switch will automatically be enabled regardless of the state of EN1/EN2 to prevent excess power dissipation inside the MOSFET body diode. In many applications (for example, resistive loads), the full load current may be present during reverse battery. In order to activate the automatic switch on feature, the SEL2 pin must have a path to module ground. This may be path 1 as shown in [Figure 37](#), or if the SEL2 pin is unused, the path may be through  $R_{PROT}$  to module ground.

Protection features like thermal shutdown are not available during a reverse battery event. Care must be taken to ensure that excessive power is not dissipated in the switch during the reverse battery condition.

There are two options for blocking reverse current in the system. The first option is to place a blocking device (FET or diode) in series with the battery supply, blocking all current paths. The second option is to place a blocking diode in series with the GND node of the high-side switch. This method will protect the controller portion of the switch (path 2), but it will not prevent current from flowing through the load (path 3). The diode used for the second option may be shared amongst multiple high-side switches.

## Feature Description (continued)

Path 1 shown in Figure 37 is blocked inside of the device.

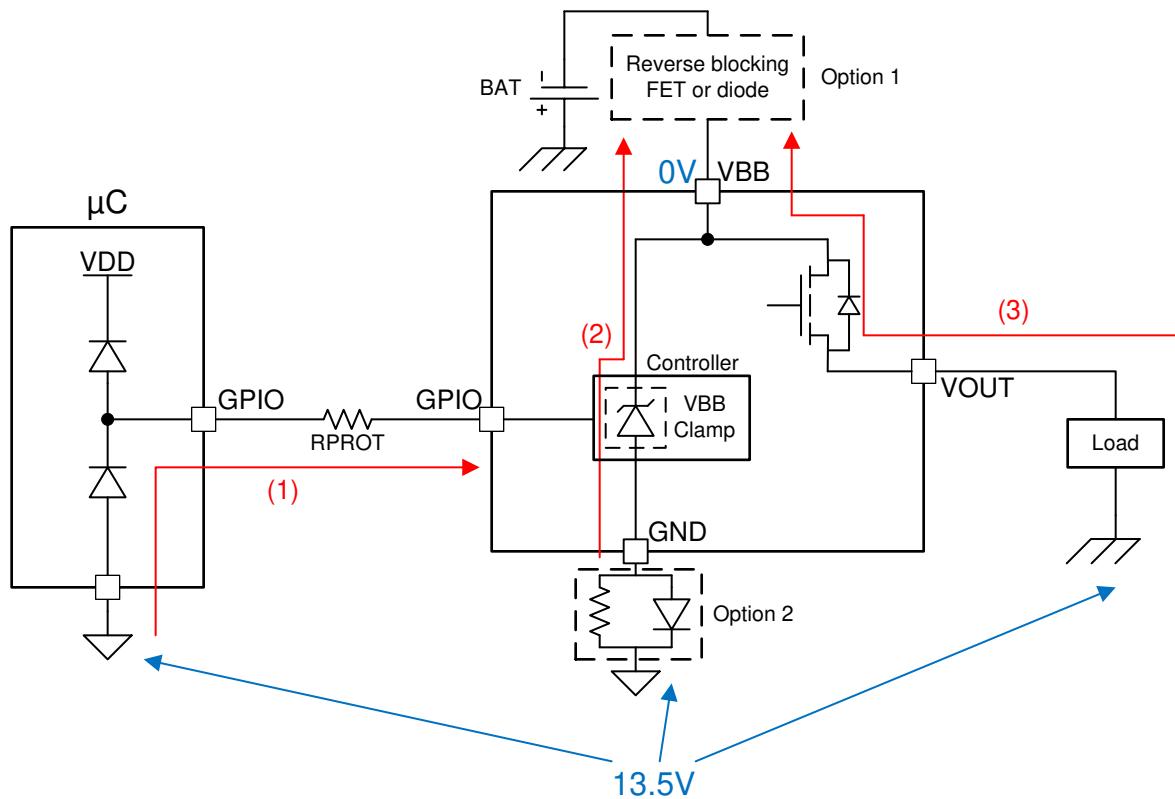


Figure 37. Current Path During Reverse Battery

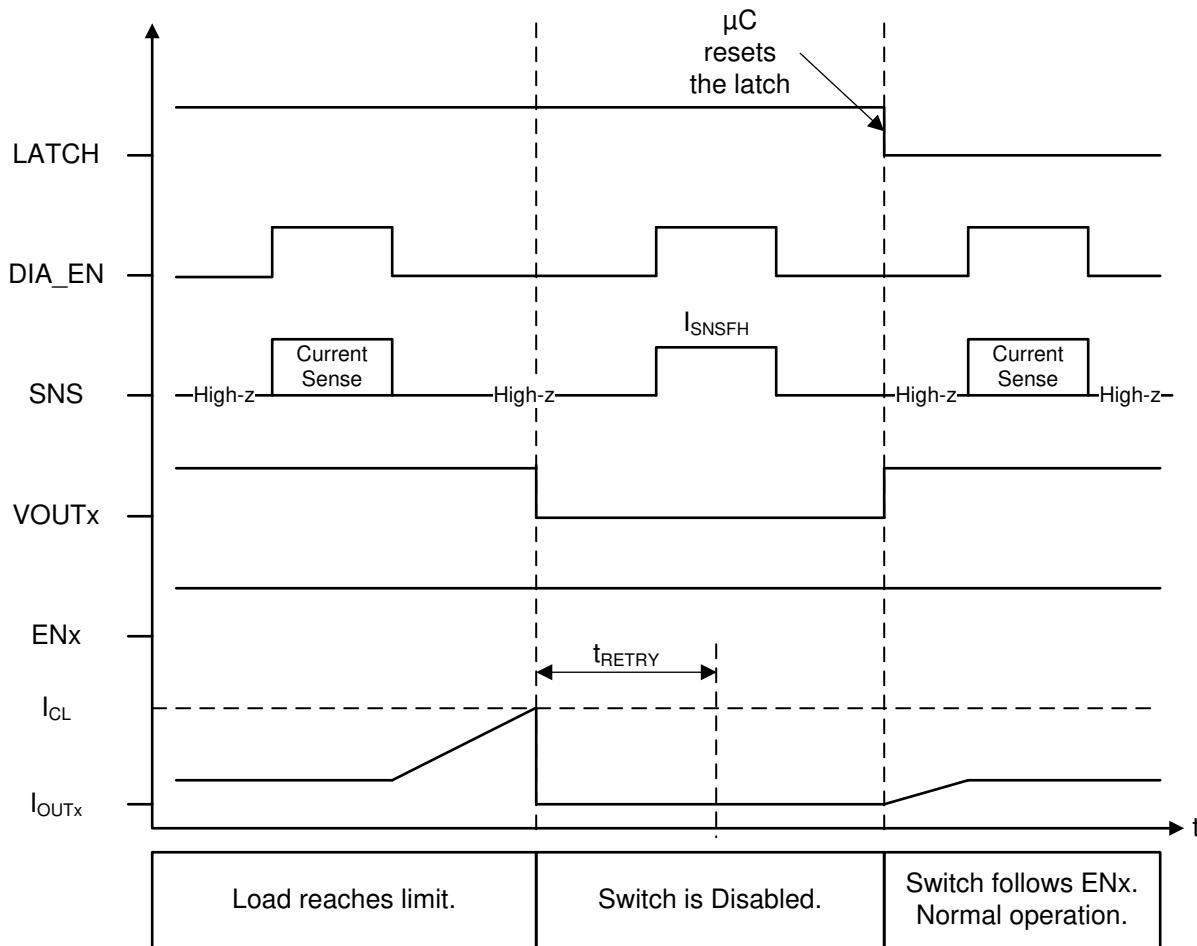
### 9.3.1.6 Fault Event – Timing Diagrams (Version A/B)

#### NOTE

All timing diagrams assume that the SELx pins are set to select the relevant channel.

The LATCH, DIA\_EN, and ENx pins are controlled by the user. The timing diagrams represent a possible use-case.

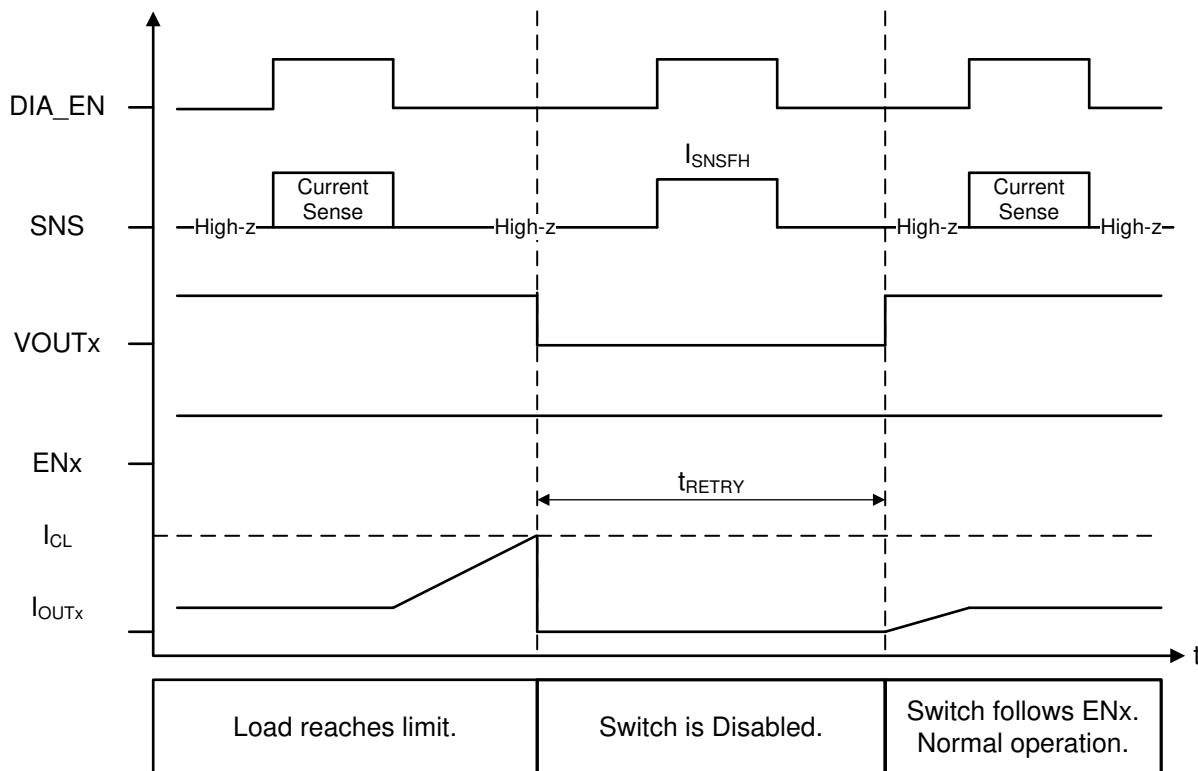
Figure 38 shows the immediate current limit switch off and the retry behavior of versions A and B of the device. As shown, the switch will remain latched off until the LATCH pin is low.

**Feature Description (continued)**


**Figure 38. Current Limit – Version A and B - Latched Behavior**

Figure 39 shows the immediate current limit switch off behavior of versions A and B. In this example, LATCH is tied to GND; hence, the switch will retry after the fault is cleared and  $t_{RETRY}$  has expired.

## Feature Description (continued)



**Figure 39. Current Limit – Version A and B - LATCH = 0**

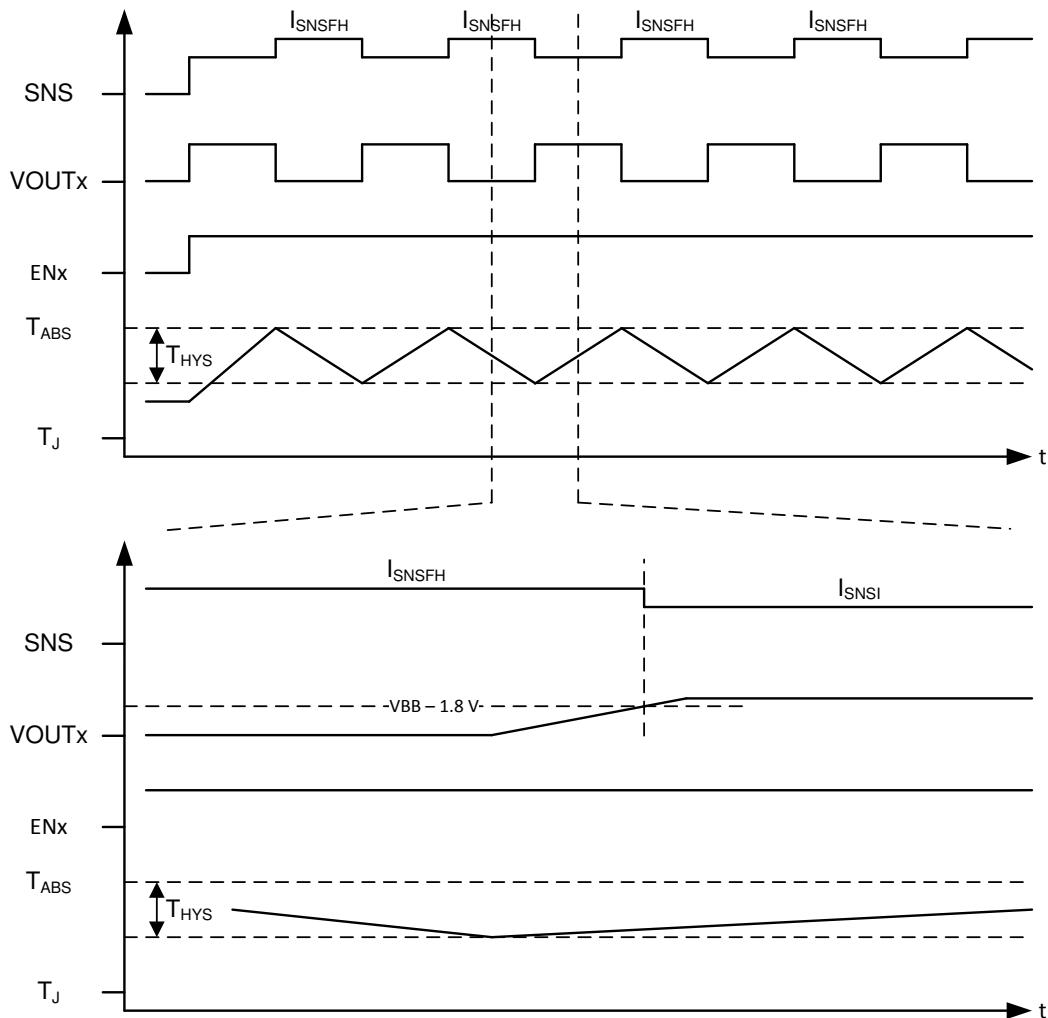
Figure 40 illustrates auto-retry behavior and provides a zoomed-in view of the fault indication during retry. When the switch retries after a shutdown event, the SNS fault indication will remain at the fault state until  $V_{OUT}$  has risen to  $V_{BB} - 1.8$  V. Once  $V_{OUT}$  has risen, the SNS fault indication is reset and current sensing is available. If there is a short-to-ground and  $V_{OUT}$  cannot rise, the SNS fault indication will remain indefinitely.

**NOTE**

Figure 40 assumes that  $t_{RETRY}$  has expired by the time that  $T_J$  reaches the hysteresis threshold.

LATCH = 0 V and DIA\_EN = 5 V

## Feature Description (continued)



**Figure 40. Fault Indication During Retry**

### 9.3.2 Fault Event – Timing Diagrams - Version F

TPS2HB16-Q1 device version F will follow the same timing and fault diagrams as described for versions A and B, with the only difference being the behavior of the FLT1 and FLT2 pins. For each diagram, the FLT1 or FLT2 pins will indicate over-current or over-temperature faults for the respective channel. The two pins are independent and will not indicate a fault that corresponds to the opposite channel.

### 9.3.3 Diagnostic Mechanisms

#### 9.3.3.1 VOUTx Short-to-Battery and Open-Load

The TPS2HB16-Q1 is capable of detecting short-to-battery and open-load events regardless of whether the switch is turned on or off, however the two conditions use different methods.

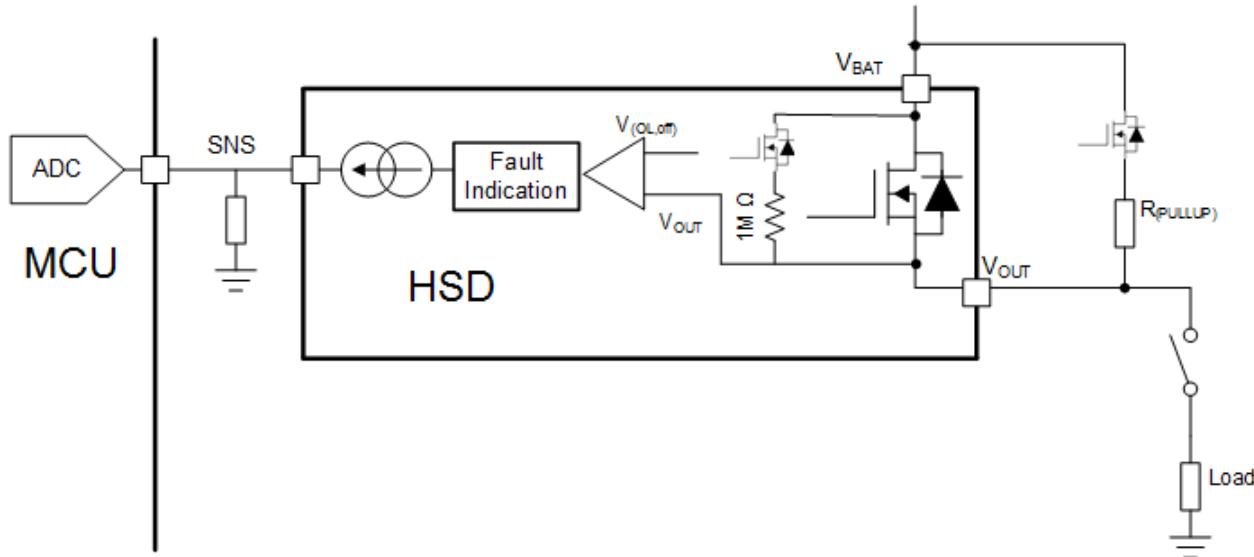
##### 9.3.3.1.1 Detection With Switch Enabled

When the switch is enabled, the VOUTx short-to-battery and open-load conditions can be detected by the current sense feature. In both cases, the load current will be measured through the SNS pin as below the expected value.

## Feature Description (continued)

### 9.3.3.1.2 Detection With Switch Disabled

While the switch is disabled, if DIA\_EN is high, an internal comparator will detect the condition of  $V_{OUT}$ . If the load is disconnected (open load condition) or there is a short to battery the  $V_{OUT}$  voltage will be higher than the open load threshold ( $V_{OL,off}$ ) and a fault is indicated on the SNS pin and the FLT1 or FLT2 pin on version F. An internal pull-up of 1 MΩ is in series with an internal MOSFET switch, so no external component is required if only a completely open load must be detected. However, if there is significant leakage or other current draw even when the load is disconnected, a lower value pull-up resistor and switch can be added externally to set the  $V_{OUT}$  voltage above the  $V_{OL,off}$  during open load conditions.



This figure assumes that the device ground and the load ground are at the same potential. In a real system, there may be a ground shift voltage of 1 V to 2 V.

**Figure 41. Short to Battery and Open Load Detection**

The detection circuitry is only enabled when DIA\_EN = HIGH and EN = LOW. If  $V_{OUT} > V_{OL}$ , the SNS pin will go to the fault level, but if  $V_{OUT} < V_{OL}$  there will be no fault indication. The fault indication will only occur if the SEL2 pin is set to diagnose the respective channel.

While the switch is disabled and DIA\_EN is high, the fault indication mechanisms will continuously represent the present status. For example, if  $V_{OUT}$  decreases from greater than  $V_{OL}$  to less than  $V_{OL}$ , the fault indication is reset. Additionally, the fault indication is reset upon the falling edge of DIA\_EN or the rising edge of EN.

## Feature Description (continued)

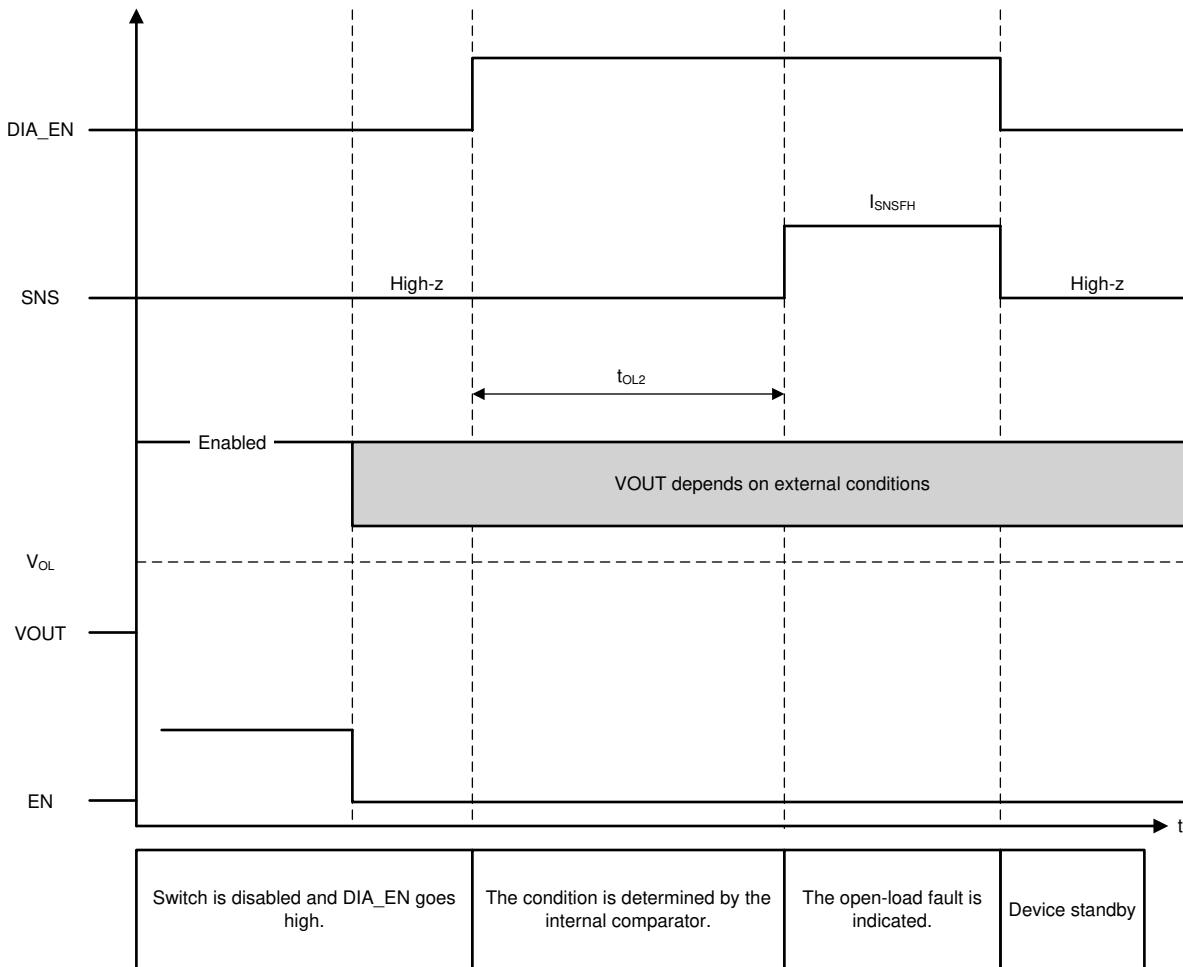


Figure 42. Open Load

## 9.3.3.2 SNS Output

The SNS output may be used to sense the load current or device temperature. The SELx pins will select the desired sense signal. The sense circuit will provide a current that is proportional to the selected parameter. This current will be sourced into an external resistor to create a voltage that is proportional to the selected parameter. This voltage may be measured by an ADC or comparator.

To ensure accurate sensing measurement, the sensing resistor should be connected to the same ground potential as the  $\mu$ C ADC.

Table 3. Analog Sense Transfer Function

| PARAMETER          | TRANSFER FUNCTION  |
|--------------------|--|
| Load current       | $I_{SNSI} = I_{OUT} / K_{SNS} (3000)$                              |
| Device temperature | $I_{SNST} = (T_J - 25^\circ\text{C}) \times dI_{SNST} / dT + 0.85$ |

The SNS output will also be used to indicate system faults.  $I_{SNS}$  will go to the predefined level,  $I_{SNSFH}$ , when there is a fault.  $I_{SNSFH}$ ,  $dI_{SNS}/dT$ , and  $K_{SNS}$  are defined in the [Specifications](#) section.

In device version F, device temperature measurement is not available so load current measurement is the only sense output.

#### 9.3.3.2.1 $R_{SNS}$ Value

The following factors should be considered when selecting the  $R_{SNS}$  value:

- Current sense ratio ( $K_{SNS}$ )
- Largest and smallest diagnosable load current required for application operation
- Full-scale voltage of the ADC
- Resolution of the ADC

For an example of selecting  $R_{SNS}$  value, reference [Selecting the  \$R\_{SNS}\$  Value](#) in the applications section of this datasheet.

##### 9.3.3.2.1.1 High Accuracy Load Current Sense

In many automotive modules, it is required that the high-side switch provide diagnostic information about the downstream load. With more complex loads, high accuracy sensing is required. A few examples follow:

- **LED lighting:** In many architectures, the body control module (BCM) must be compatible with both incandescent bulbs and also LED modules. The bulb may be relatively simple to diagnose. However, the LED module will consume less current and also can include multiple LED strings in parallel. The same BCM is used in both cases, so the high-side switch can accurately diagnose both load types.
- **Solenoid protection:** Often solenoids are precisely controlled by low-side switches. However, in a fault event, the low-side switch cannot disconnect the solenoid from the power supply. A high-side switch can be used to continuously monitor several solenoids. If the system current becomes higher than expected, the high-side switch can disable the module.

##### 9.3.3.2.1.2 SNS Output Filter

To achieve the most accurate current sense value, it is recommended to filter the SNS output. There are two methods of filtering:

- Low-Pass RC filter between the SNS pin and the ADC input. This filter is illustrated in [Figure 46](#) with typical values for the resistor and capacitor. The designer should select a  $C_{SNS}$  capacitor value based on system requirements. A larger value will provide improved filtering but a smaller value will allow for faster transient response.
- The ADC and microcontroller can also be used for filtering. It is recommended that the ADC collects several measurements of the SNS output. The median value of this data set should be considered as the most accurate result. By performing this median calculation, the microcontroller can filter out any noise or outlier data.

#### 9.3.3.3 Fault Indication and SNS Mux

The following faults will be communicated through the SNS output:

- Switch shutdown, due to:
  - Thermal Shutdown
  - Current limit
- Open-Load /  $V_{OUT}$  shorted-to-battery

Open-load and short-to-battery are not indicated while the switch is enabled, although these conditions can still be detected through the sense current. Hence, if there is a fault indication corresponding to an enabled channel, then it must be either due to an overcurrent or overtemperature event.

The SNS pin will only indicate the fault if the SELx pins are selecting the relevant channel. When the device is set to measure temperature, the pin will be measuring the temperature of whichever channel is at a higher temperature.

**Table 4. Version A/B SNS Mux**

| INPUTS |      |      |                             | OUTPUTS            |
|--------|------|------|-----------------------------|--------------------|
| DIA_EN | SEL1 | SEL2 | FAULT DETECT <sup>(1)</sup> | SNS                |
| 0      | X    | X    | X                           | High-Z             |
| 1      | 0    | 0    | 0                           | CH1 current        |
| 1      | 0    | 1    | 0                           | CH2 current        |
| 1      | 1    | 0    | 0                           | Device temperature |
| 1      | 1    | 1    | 0                           | N/A                |
| 1      | 0    | 0    | 1                           | $I_{SNSFH}$        |
| 1      | 0    | 1    | 1                           | $I_{SNSFH}$        |
| 1      | 1    | 0    | 1                           | Device temperature |
| 1      | 1    | 1    | 1                           | N/A                |

(1) Fault Detect encompasses multiple conditions:  
 (a) Switch shutdown and waiting for retry  
 (b) Open-load and short-to-battery

Version F of the device has a different fault table due to the lack of SEL1 pin functionality and the addition of the FLT1 and FLT2 pins. In all cases, SEL1 should be tied to ground for device version F. The table below shows the FLT mux for Version F of the device. The FLT1 and a FLT2 pin which will each trigger independently. If the fault detect flag corresponds to channel 1 over-current, over-temperature, or open load, FLT1 will trigger, while if the fault detect flag corresponds to channel 2 over-current, over-temperature, or open load, FLT2 will trigger.

**Table 5. Version F SNS Mux**

| INPUTS |      |                             |                   | OUTPUTS     |
|--------|------|-----------------------------|-------------------|-------------|
| DIA_EN | SEL2 | FAULT DETECT <sup>(1)</sup> | $\overline{FLTx}$ | SNS         |
| 0      | X    | X                           | High-Z            | High-Z      |
| 1      | 0    | 0                           | High-Z            | CH1 current |
| 1      | 1    | 0                           | High-Z            | CH2 current |
| 1      | 0    | 1                           | Open-Drain        | $I_{SNSFH}$ |
| 1      | 1    | 1                           | Open-Drain        | $I_{SNSFH}$ |

(1) Fault Detect encompasses multiple conditions:  
 (a) Switch shutdown and waiting for retry  
 (b) Open Load / Short To Battery

#### 9.3.3.4 Resistor Sharing

Multiple high-side channels may use the same SNS resistor as shown in [Figure 43](#). This reduces the total number of passive components in the system and the number of ADC terminals that are required of the microcontroller.

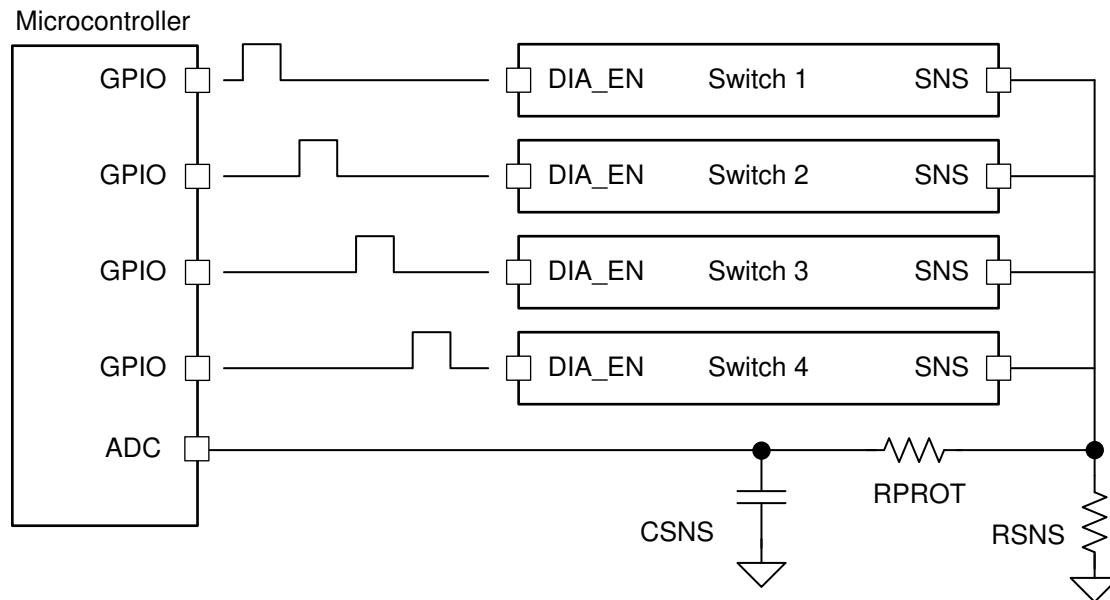


Figure 43. Sharing  $R_{SNS}$  Among Multiple Devices

#### 9.3.3.5 High-Frequency, Low Duty-Cycle Current Sensing

Some applications will operate with a high-frequency, low duty-cycle PWM or require fast settling of the SNS output. For example, a 250 Hz, 5% duty cycle PWM will have an on-time of only 200  $\mu$ s that must be accommodated. The micro-controller ADC may sample the SNS signal after the defined settling time  $t_{SNSION3}$ .

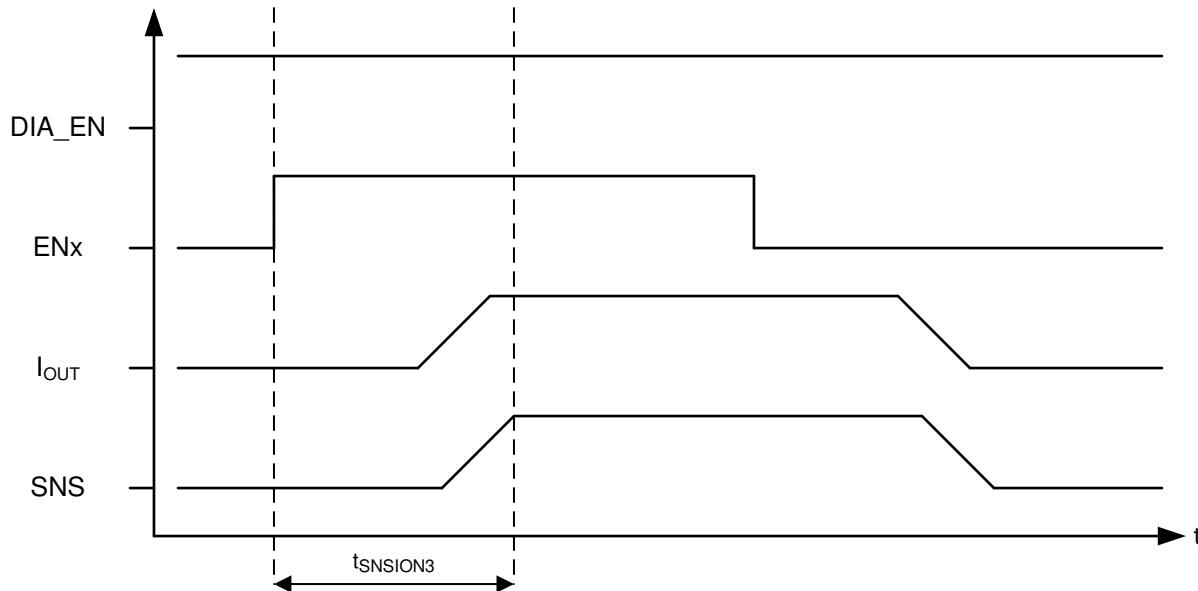


Figure 44. Current Sensing in Low-Duty Cycle Applications

## 9.4 Device Functional Modes

During typical operation, the TPS2HB16-Q1 can operate in a number of states that are described below and shown as a state diagram in [Figure 45](#).

## Device Functional Modes (continued)

### 9.4.1 Off

Off state occurs when the device is not powered.

### 9.4.2 Standby

Standby state is a low-power mode used to reduce power consumption to the lowest level. Diagnostic capabilities are not available in Standby mode.

### 9.4.3 Diagnostic

Diagnostic state may be used to perform diagnostics while the switches are disabled.

### 9.4.4 Standby Delay

The Standby Delay state is entered when EN1, EN2, and DIA\_EN are low. After  $t_{STBY}$ , if the ENx and DIA\_EN pins are still low, the device will go to Standby state.

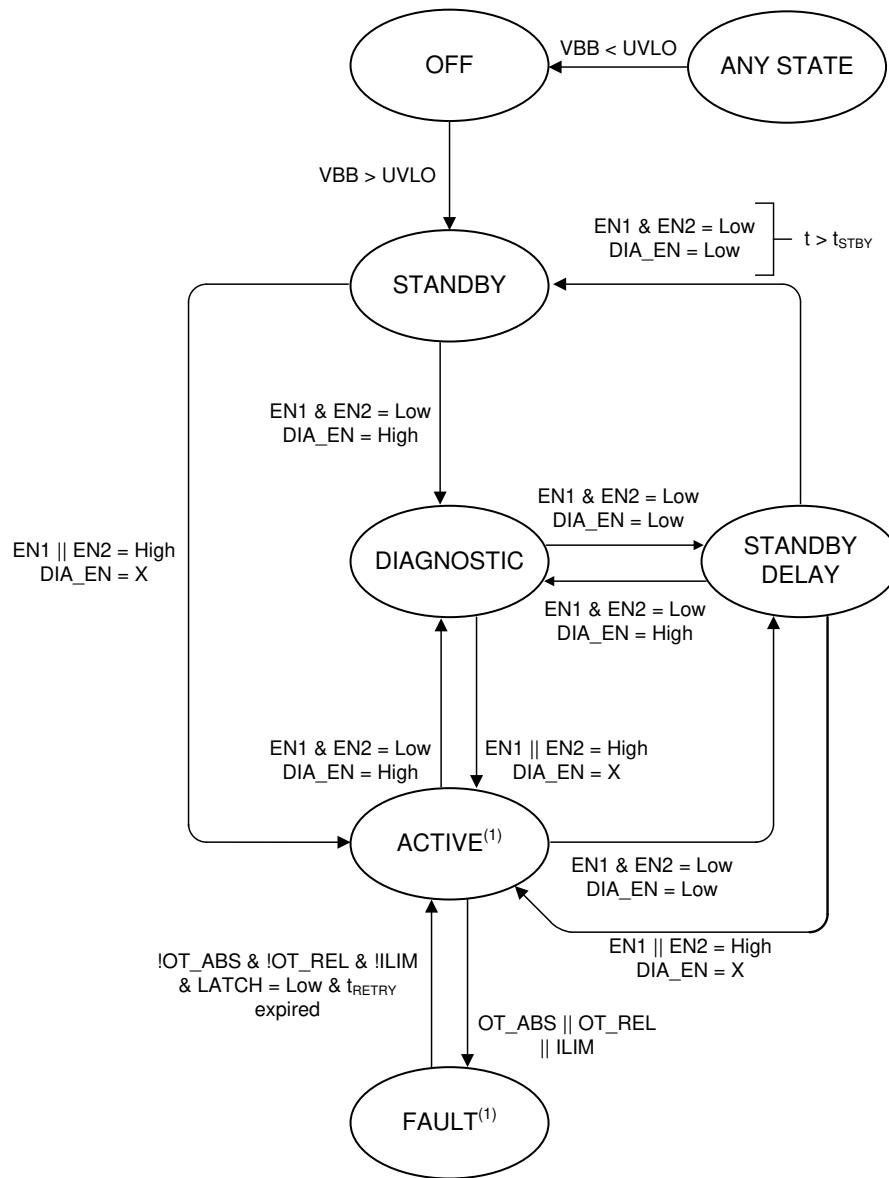
### 9.4.5 Active

In Active state, one or more of the switches are enabled. The diagnostic functions may be turned on or off during Active state.

### 9.4.6 Fault

The Fault state is entered if a fault shutdown occurs (thermal shutdown or current limit). After all faults are cleared, the LATCH pin is low, and the retry timer has expired, the device will transition out of Fault state. If the relevant ENx pin is high, the switch will re-enable. If the relevant ENx pin is low, the switch will remain off.

## Device Functional Modes (continued)



CH1 and CH2 operate independently. Each channel is enabled or disabled independently. Also, if there is a fault on one channel, the other channel is not affected.

**Figure 45. State Diagram**

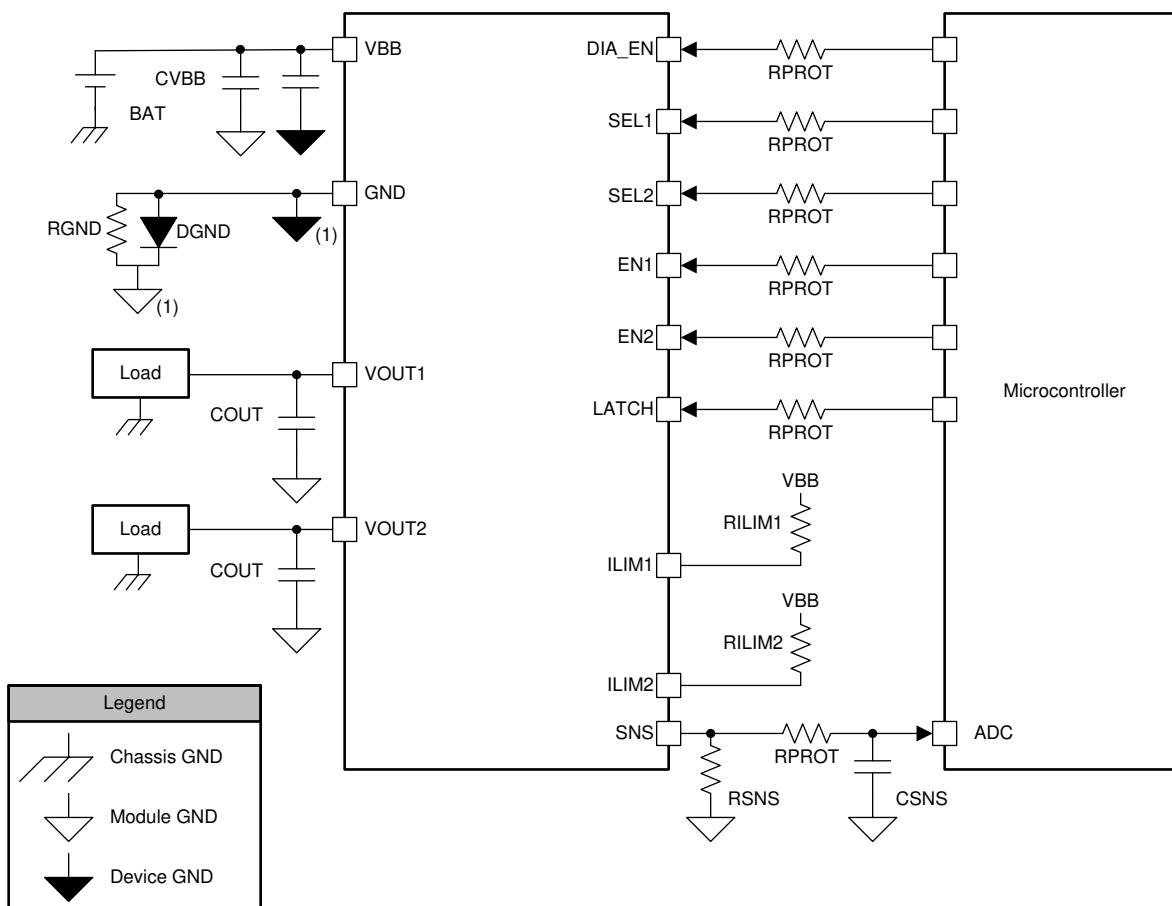
## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

Figure 46 shows the schematic of a typical application for the TPS2HB16-Q1. It includes all standard external components. This section of the datasheet discusses the considerations in implementing commonly required application functionality. This diagram corresponds to version A of the device. Version F will have minor differences due to the addition of the **FLTX** pins



With the ground protection network, the device ground will be offset relative to the microcontroller ground.

**Figure 46. System Diagram**

**Table 6. Recommended External Components**

| COMPONENT  | TYPICAL VALUE  | PURPOSE  |
|------------|----------------|--|
| $R_{PROT}$ | 15 k $\Omega$  | Protect the microcontroller and device I/O pins.           |
| $R_{SNS}$  | 1 k $\Omega$   | Translate the sense current into sense voltage.            |
| $C_{SNS}$  | 100 pF - 10 nF | Creates Low-pass filter for the ADC input                  |
| $R_{GND}$  | 4.7 k $\Omega$ | Stabilize GND potential during turn-off of inductive load. |

## Application Information (continued)

Table 6. Recommended External Components (continued)

| COMPONENT         | TYPICAL VALUE        | PURPOSE   |
|-------------------|----------------------|---|
| D <sub>GND</sub>  | BAS21 Diode          | Protect the device during reverse battery.                                      |
| R <sub>ILIM</sub> | 5 kΩ - 25 kΩ         | Set the current limit threshold.  |
| C <sub>VBB</sub>  | 4.7 nF to Device GND | Filters voltage transients (for example, ESD, ISO7637-2) and improves emissions |
|                   | 220 nF to Module GND | Stabilize the input supply and filter out low frequency noise.                  |
| C <sub>OUT</sub>  | 220 nF               | Filters voltage transients (for example, ESD, ISO7637-2)                        |

### 10.1.1 Ground Protection Network

As discussed in the [Reverse Battery](#) section, D<sub>GND</sub> may be used to prevent excessive reverse current from flowing into the device during a reverse battery event. Additionally, R<sub>GND</sub> is placed in parallel with D<sub>GND</sub> if the switch is used to drive an inductive load. The ground protection network (D<sub>GND</sub> and R<sub>GND</sub>) may be shared amongst multiple high-side switches.

A minimum value for R<sub>GND</sub> may be calculated by using the absolute maximum rating for I<sub>GND</sub>. During the reverse battery condition, I<sub>GND</sub> = V<sub>BB</sub> / R<sub>GND</sub>:

$$R_{GND} \geq V_{BB} / I_{GND}$$

- Set V<sub>BB</sub> = -13.5 V
- Set I<sub>GND</sub> = -50 mA (absolute maximum rating)

$$R_{GND} \geq -13.5 \text{ V} / -50 \text{ mA} = 270 \Omega \quad (2)$$

In this example, it is found that R<sub>GND</sub> must be at least 270 Ω. It is also necessary to consider the power dissipation in R<sub>GND</sub> during the reverse battery event:

$$P_{RGND} = V_{BB}^2 / R_{GND} \quad (3)$$

$$P_{RGND} = (13.5 \text{ V})^2 / 270 \Omega = 0.675 \text{ W}$$

In practice, R<sub>GND</sub> may not be rated for such a high power. In this case, a larger resistor value should be selected.

### 10.1.2 Interface With Microcontroller

The ground protection network will cause the device ground to be at a higher potential than the module ground (and microcontroller ground). This offset will impact the interface between the device and the microcontroller.

Logic pin voltage will be offset by the forward voltage of the diode. For input pins (for example, EN1), the designer must consider the V<sub>IH</sub> specification of the switch and the V<sub>OH</sub> specification of the microcontroller. For a system that *does not* include D<sub>GND</sub>, it is required that V<sub>OH</sub> > V<sub>IH</sub>. For a system that *does* include D<sub>GND</sub>, it is required that V<sub>OH</sub> > (V<sub>IH</sub> + V<sub>F</sub>). V<sub>F</sub> is the forward voltage of D<sub>GND</sub>.

The sense resistor, R<sub>SNS</sub>, should be terminated to the microcontroller ground. In this case, the ADC can accurately measure the SNS signal even if there is an offset between the microcontroller ground and the device ground.

### 10.1.3 I/O Protection

R<sub>PROT</sub> is used to protect the microcontroller I/O pins during system-level voltage transients such as ISO pulses or reverse battery. The SNS pin voltage can exceed the ADC input pin maximum voltage if the fault or saturation current causes a high enough voltage drop across the sense resistor. If that can occur in the design (for example, by switching to a high value R<sub>SNS</sub> to improve ADC input level), then an appropriate external clamp has to be designed to prevent a high voltage at the SNS output and the ADC input.

### 10.1.4 Inverse Current

Inverse current occurs when 0 V < V<sub>BB</sub> < V<sub>OUTx</sub>. In this case, current may flow from V<sub>OUTx</sub> to V<sub>BB</sub>. Inverse current cannot be caused by a purely resistive load. However, a capacitive or inductive load can cause inverse current. For example, if there is a significant amount of load capacitance and the V<sub>BB</sub> node has a transient droop, V<sub>OUTx</sub> may be greater than V<sub>BB</sub>.

The TPS2HB16-Q1 will not detect inverse current. When the switch is enabled, inverse current will pass through the switch. When the switch is disabled, inverse current may pass through the MOSFET body diode. The device will continue operating in the normal manner during an inverse current event.

### 10.1.5 Loss of GND

The ground connection may be lost either on the device level or on the module level. If the ground connection is lost, both switches will be disabled. If the switch was already disabled when the ground connection was lost, the switch will remain disabled. When the ground is reconnected, normal operation will resume.

### 10.1.6 Automotive Standards

The TPS2HB16-Q1 is designed to be protected against all relevant automotive standards to ensure reliable operations when connected to a 12-V automotive battery.

#### 10.1.6.1 ISO7637-2

The TPS2HB16-Q1 is tested according to the ISO7637-2:2011 (E) standard. The test pulses are applied both with the switches enabled and disabled. The test setup includes only the DUT and minimal external components:  $C_{VBB}$ ,  $C_{OUT}$ ,  $D_{GND}$ , and  $R_{GND}$ .

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as: *The function does not perform as designed during the test but returns automatically to normal operation after the test.* See [Table 7](#) for ISO7637-2:2011 (E) expected results.

**Table 7. ISO7637-2:2011 (E) Results**

| TEST PULSE        | TEST PULSE SEVERITY LEVEL WITH STATUS II FUNCTIONAL PERFORMANCE |        | MINIMUM NUMBER OF PULSES OR TEST TIME | BURST CYCLE / PULSE REPETITION TIME |        |
|-------------------|---|--------|---------------------------------------|-------------------------------------|--------|
|                   | LEVEL   | US     |                                       | MIN                                 | MAX    |
| 1                 | III   | -112 V | 500 pulses                            | 0.5 s                               | --     |
| 2a <sup>(1)</sup> | III   | +55 V  | 500 pulses                            | 0.20 s                              | 5 s    |
| 2b                | IV  | +10 V  | 10 pulses                             | 0.5 s                               | 5 s    |
| 3a                | IV  | -220 V | 1 hour                                | 90 ms                               | 100 ms |
| 3b                | IV  | +150 V | 1 hour                                | 90 ms                               | 100 ms |

(1) 1  $\mu$ F capacitance on  $C_{VBB}$  is required for passing level 3 ISO7637 pulse 2 A.

#### 10.1.6.2 AEC – Q100-012 Short Circuit Reliability

The TPS2HB16-Q1 is tested according to the AEC-Q100-012 Short Circuit Reliability standard. This test is performed to demonstrate the robustness of the device against  $V_{OUT}$  short-to-ground events. Test conditions and test procedures are summarized in [Table 8](#). For further details, refer to the AEC - Q100-012 standard document.

Test conditions:

- LATCH = 0 V
- $I_{LIM} = \text{N/A}$  (Version F)
- 10 units from 3 separate lots for a total of 30 units
- $L_{\text{supply}} = 5 \mu\text{H}$ ,  $R_{\text{supply}} = 10 \text{ m}\Omega$
- $V_{BB} = 14 \text{ V}$

Test procedure:

- Parametric data is collected on each unit pre-stress.
- Each unit is enabled into a short-circuit with the required short circuit cycles or duration as specified.
- Functional testing is performed on each unit post-stress to verify that the part still operates as expected.

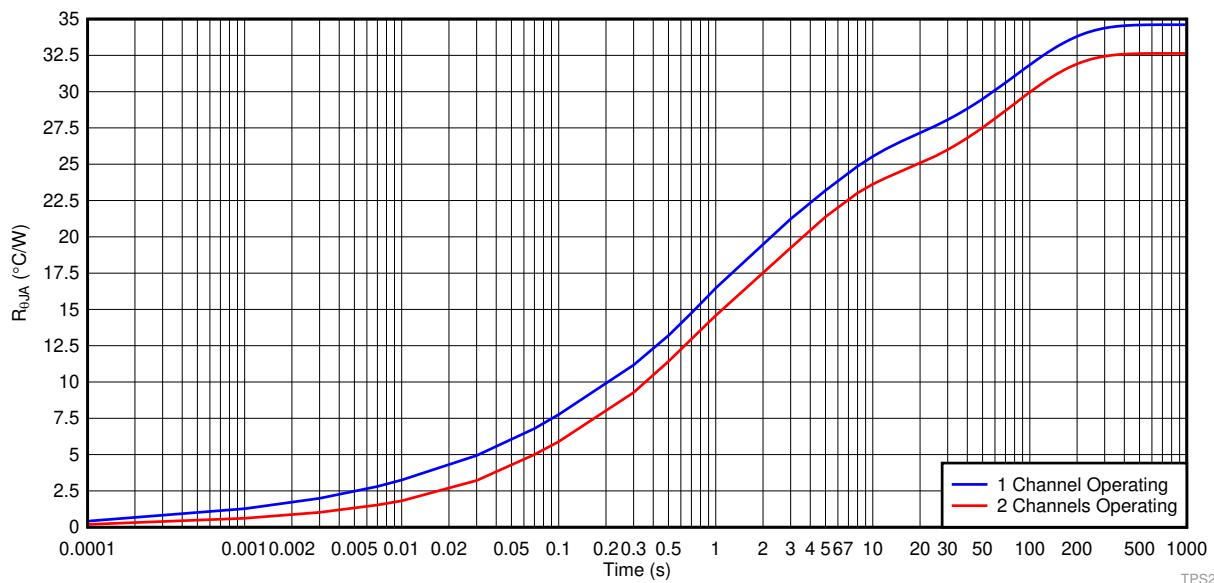
The cold repetitive test is run at 85°C which is the worst case condition for the device to sustain a short circuit. The cold repetitive test refers to the device being given time to cool down between pulses, rather than being run at a cold temperature. The load short circuit is the worst case situation, since the energy stored in the cable inductance can cause additional harm. The fast response of the device ensures current limiting occurs quickly and at a current close to the load short condition. In addition, the hot repetitive test is performed as well.

**Table 8. AEC - Q100-012 Test Results**

| TEST                         | LOCATION OF SHORT  | DEVICE VERSION | NO. OF CYCLES / DURATION | NO. OF UNITS | NO. OF FAILS |
|------------------------------|--|----------------|--------------------------|--------------|--------------|
| Cold Repetitive - Long Pulse | Load Short Circuit, $L_{short} = 5 \mu\text{H}$ , $R_{short} = 100 \text{ m}\Omega$ , $T_A = 85^\circ\text{C}$ | F              | 100 k cycles             | 30           | 0            |
| Hot Repetitive - Long Pulse  | Load Short Circuit, $L_{short} = 5 \mu\text{H}$ , $R_{short} = 100 \text{ m}\Omega$ , $T_A = 25^\circ\text{C}$ | F              | 100 hours                | 30           | 0            |

### 10.1.7 Thermal Information

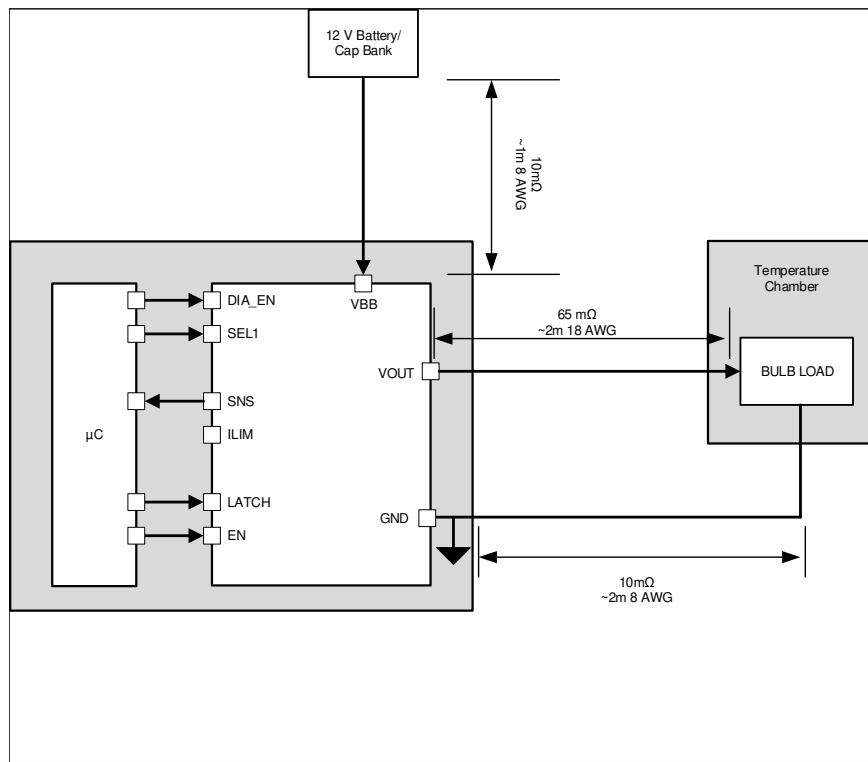
When outputting current, the TPS2HB16-Q1 will heat up due to the power dissipation. The transient thermal impedance curve can be used to determine the device temperature during a pulse of a given length. This  $R_{\theta JA}$  value corresponds to a JEDEC standard 2s2p thermal test PCB with thermal vias. The  $R_{\theta JA}$  will vary depending on whether the power dissipation is concentrated in a single channel or is distributed evenly between each channel.


**Figure 47. TPS2HB16-Q1 Transient Thermal Impedance**

### 10.2 Typical Application

This application example demonstrates how the TPS1HB16-Q1 device can be used to power bulb loads in automotive headlights. In this example, we consider a 27 W that is powered by the device. This is just one example of the many applications where this device can fit.

## Typical Application (continued)



**Figure 48. Block Diagram for Driving Bulb Load**

### 10.2.1 Design Requirements

For this design example, use the input parameters shown in [Table 9](#).

**Table 9. Design Parameters**

| DESIGN PARAMETER                    | EXAMPLE VALUE |
|-------------------------------------|---------------|
| $V_{BB}$                            | 16 V          |
| Load - Bulb                         | 2x27 W        |
| Fixed $I_{LIM}$                     | 60 A          |
| Ambient temperature                 | 25°C          |
| Bulb Temperature in Chamber         | -40°C         |
| Cable Impedance from Device to Bulb | 65 mΩ         |
| Device Version                      | F             |

### 10.2.2 Detailed Design Procedure

The typical bulb test setup is where the device is at 25°C and the bulb is in a temperature chamber at -40°C. The bulb needs to be kept at -40°C so that the impedance is very low and the inrush current will be the highest. The impedance of the cables is important because it will change the inrush current of the bulb as well. The F version of the TPS2HB16-Q1 has a very high fixed current limit so that the inrush current of the bulb can be passed without limitation.

### 10.2.3 Application Curves

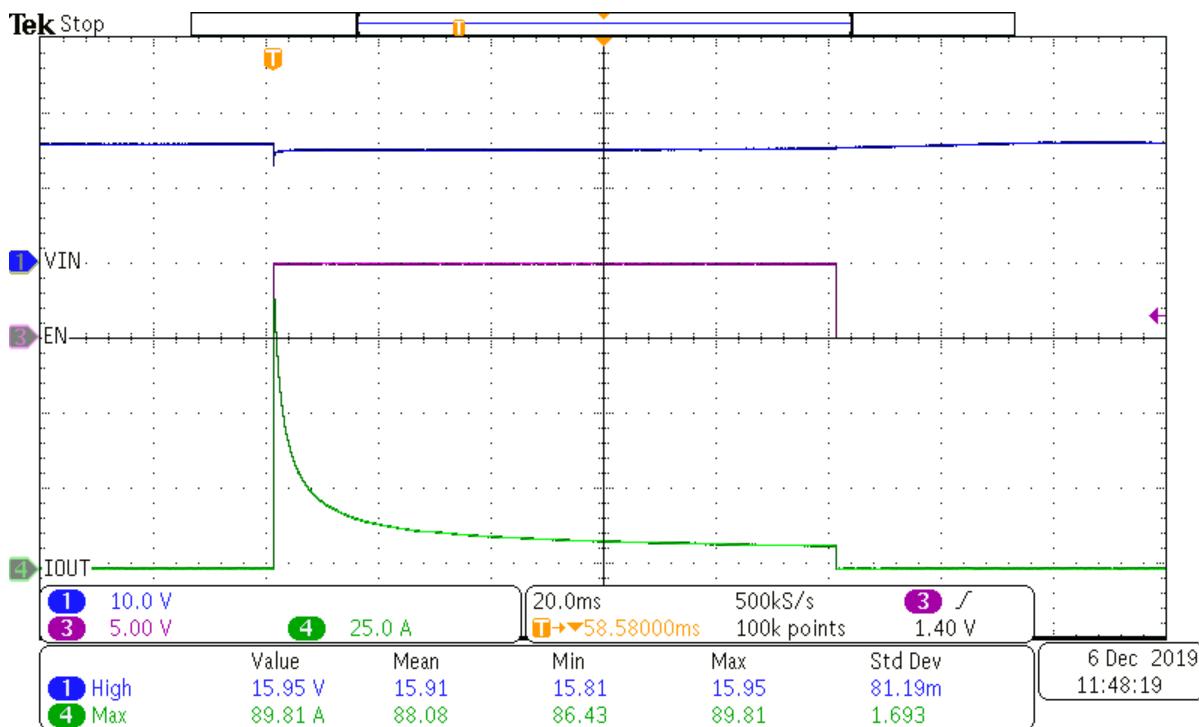


Figure 49. TPS2HB16-Q1 Version F Driving 2x27 W Bulb Inrush

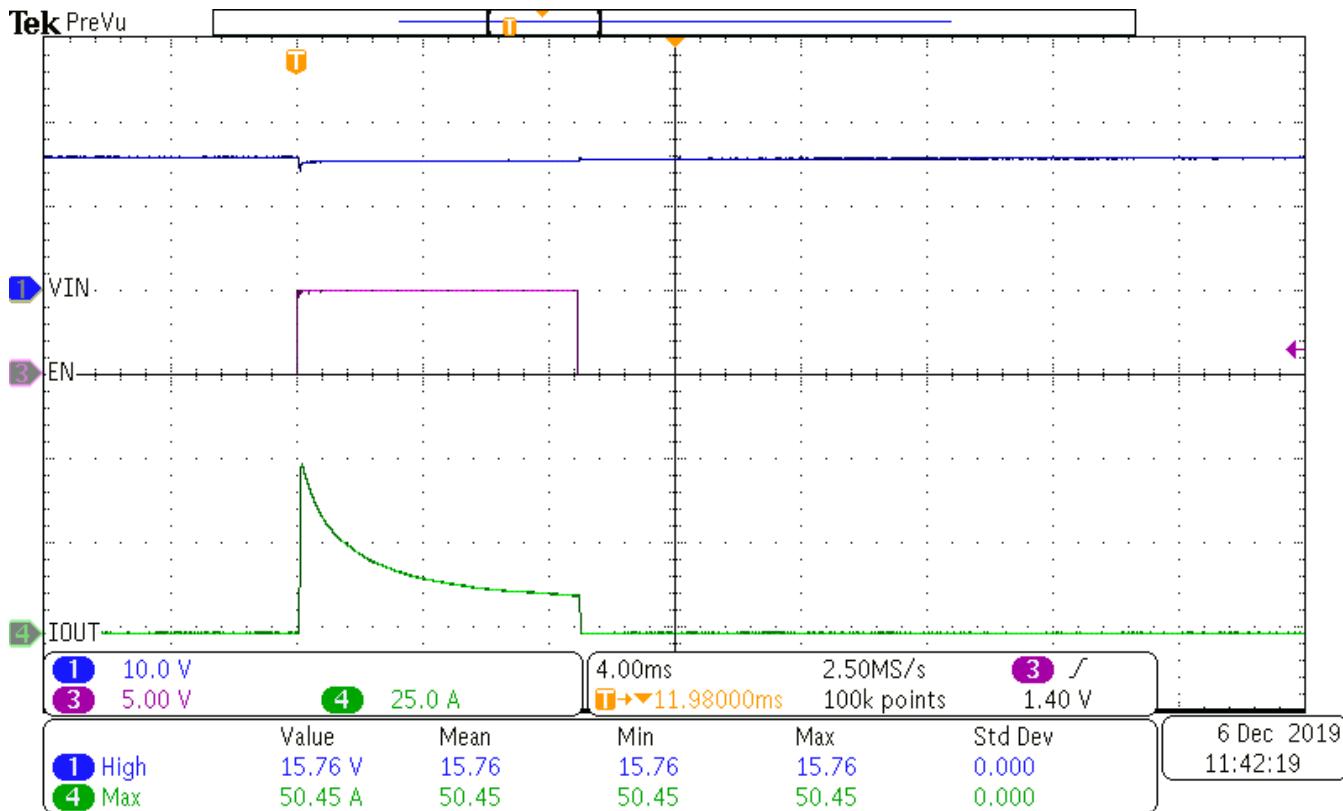


Figure 50. TPS2HB16-Q1 Version F Driving Single 27 W Bulb Inrush

## 10.2.4 Design Requirements

For this design example, use the input parameters shown in [Table 10](#).

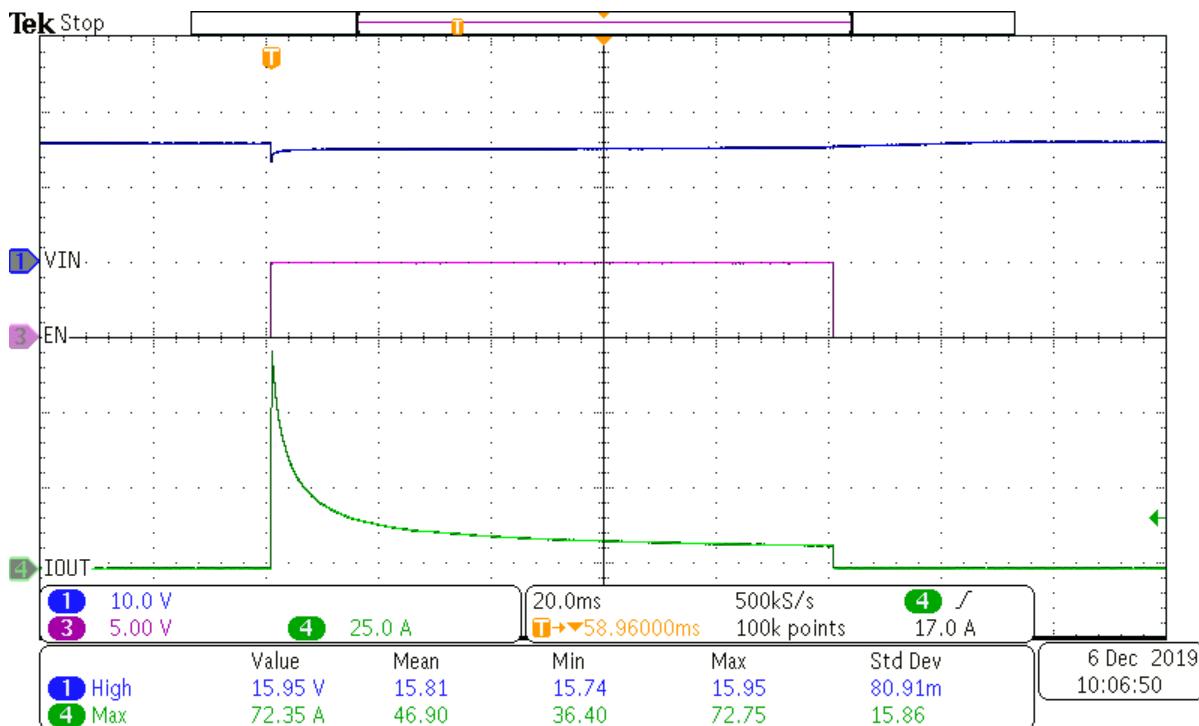
**Table 10. Design Parameters**

| DESIGN PARAMETER                    | EXAMPLE VALUE |
|-------------------------------------|---------------|
| $V_{BB}$                            | 16 V          |
| Load - Bulb                         | 2x27 W        |
| Fixed $I_{LIM}$                     | 60 A          |
| Ambient temperature                 | 105°C         |
| Bulb Temperature in Chamber         | 25°C          |
| Cable Impedance from Device to Bulb | 65 mΩ         |
| Device Version                      | F             |

## 10.2.5 Detailed Design Procedure

The another typical bulb test is to have the bulbs at room temperature (25°C) and the device heated up to 105°C. This test is designed see if the device can drive the bulbs without hitting thermal shutdown due to the current draw of the bulbs. The passing criteria is that the bulb illuminates when the device enables the channels and the device does not go into thermal shutdown. [Figure 51](#) shows the current waveform of this test and as it can be seen the bulb comes on and stays on without hitting thermal shutdown. Notice that the current is lower in this condition than the inrush condition. This is due to the bulbs effective capacitance being lower at higher temperatures as expected.

## 10.2.6 Application Curves



**Figure 51. TPS2HB16-Q1 Version F 2x27W Bulb Turn On**

## 10.3 Typical Application

This application example demonstrates how the TPS2HB16-Q1 device can be used to power resistive heater loads in automotive seats. In this example, we consider dual heater loads that are powered independently by the two channels of the device. A dual-channel device is the ideal solution as it will yield a smaller solution size relative to two single-channel devices.

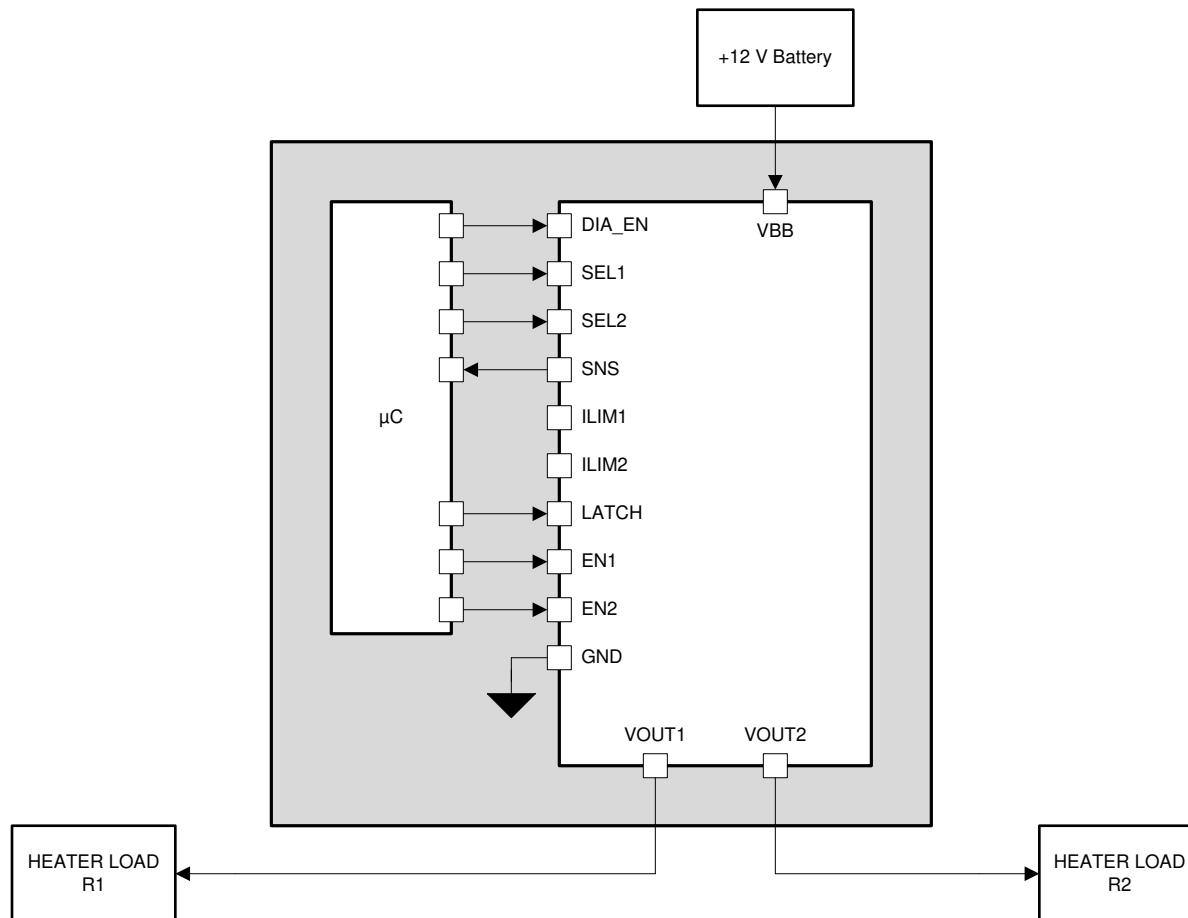


Figure 52. Block Diagram for Powering Dual Heater Loads

### 10.3.1 Design Requirements

For this design example, use the input parameters shown in Table 11.

Table 11. Design Parameters

| DESIGN PARAMETER    | EXAMPLE VALUE               |
|---------------------|-----------------------------|
| V <sub>BB</sub>     | 13.5 V                      |
| Load Ch1 - Heater 1 | 55 W max                    |
| Load Ch2 - Heater 2 | 55 W max                    |
| Load Current Sense  | 60 mA to 12 A               |
| I <sub>LIM</sub>    | 6 A                         |
| Ambient temperature | 70°C                        |
| R <sub>θJA</sub>    | 32.5°C/W (depending on PCB) |
| Device Version      | A                           |

## 10.3.2 Detailed Design Procedure

### 10.3.2.1 Thermal Considerations

The DC current in each channel under maximum load power condition will be around 4.1 A. Both heater loads can be ON at the same time, so the case where both channels are enabled simultaneously is considered to assume worst case heating.

Power dissipation in the switch is calculated in [Equation 4](#).  $R_{ON}$  is assumed to be 40 mΩ because this is the maximum specification at high temperature. In practice,  $R_{ON}$  will almost always be lower.

$$P_{FET} = I^2 \times R_{ON} \quad (4)$$

$$P_{FET} = (4.1 \text{ A})^2 \times 40 \text{ m}\Omega = 0.67 \text{ W} \quad (5)$$

If both channels are enabled, then the total power dissipation is 1.34 W. The junction temperature of the device can be calculated using [Equation 6](#) and the  $R_{0JA}$  value from the [Specifications](#) section.

$$T_J = T_A + R_{0JA} \times P_{FET} \quad (6)$$

$$T_J = 70^\circ\text{C} + 32.5^\circ\text{C/W} \times 1.34 \text{ W} = 113.5^\circ\text{C}$$

The maximum junction temperature rating for the TPS2HB16-Q1 device is  $T_J = 150^\circ\text{C}$ . Based on the above example calculation, the device temperature will stay below the maximum rating.

### 10.3.2.2 $R_{ILIM}$ Calculation

In this application, the TPS2HB16-Q1 must allow for the maximum 4.1-A current with margin but minimize the energy in the switch during a fault condition by minimizing the current limit. For this application, the best  $I_{LIM}$  set point is approximately 6 A. [Equation 7](#) allows you to calculate the  $R_{ILIM}$  value that is placed from the  $I_{LIMX}$  pins to  $V_{BB}$ .  $R_{ILIM}$  is calculated in kΩ.

$$R_{ILIM} = K_{CL} / I_{CL} \quad (7)$$

Because this device is version A, the  $K_{CL}$  value in the [Specifications](#) section is 102 A × kΩ.

$$R_{ILIM} = 102 \text{ A} \times \text{k}\Omega / 6 \text{ A} = 17 \text{ k}\Omega \quad (8)$$

For a  $I_{LIM}$  of 6 A, the  $R_{ILIM}$  value should be set at approximately 17 kΩ.

### 10.3.2.3 Diagnostics

If the resistive heating load is disconnected (heater malfunction), an alert is desired. Open-load detection can be performed in the switch-enabled state with the current sense feature of the TPS2HB16-Q1 device. Under open load condition, the current in the SNS pin will be the fault current and this can be detected from the sense voltage measurement.

#### 10.3.2.3.1 Selecting the $R_{SNS}$ Value

[Table 12](#) shows the requirements for the load current sense in this application. The  $K_{SNS}$  value is specified for the device and can be found in the [Specifications](#) section.

**Table 12.  $R_{SNS}$  Calculation Parameters**

| PARAMETER                         | EXAMPLE VALUE |
|-----------------------------------|---------------|
| Current Sense Ratio ( $K_{SNS}$ ) | 3000          |
| Largest diagnosable load current  | 12 A          |
| Smallest diagnosable load current | 60 mA         |
| Full-scale ADC voltage            | 5-V           |
| ADC resolution                    | 10-bit        |

The load current measurement requirements of 12 A ensures that even in the event of a overcurrent surpassing the device internal 6-A limit, the MCU can register and react by shutting down the TPS2HB16-Q1, while the low level of 60 mA allows for accurate measurement of low load currents.

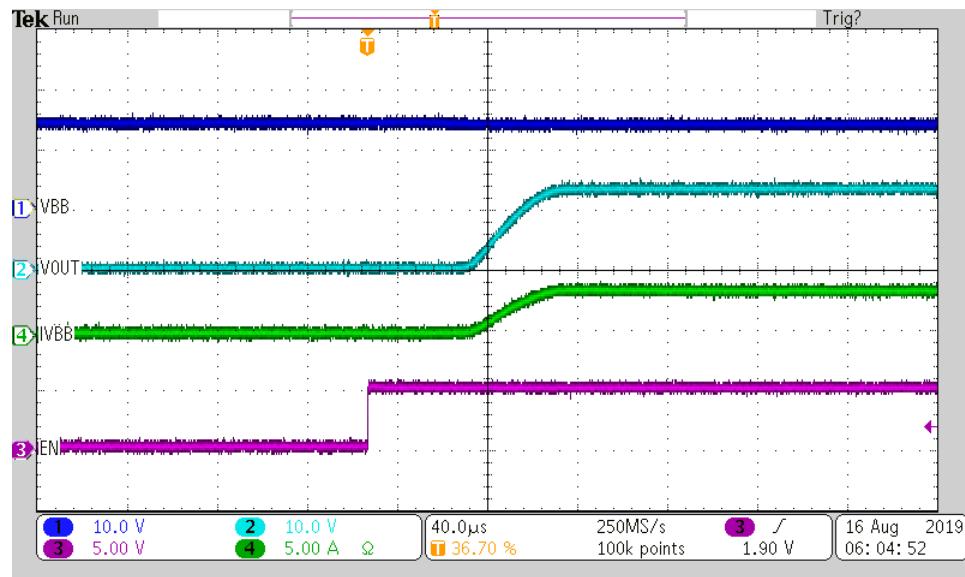
The  $R_{SNS}$  resistor value should be selected such that the largest diagnosable load current puts  $V_{SNS}$  at about 95% of the ADC full-scale. With this design, any ADC value above 95% can be considered a fault. Additionally, the  $R_{SNS}$  resistor value should ensure that the smallest diagnosable load current does not cause  $V_{SNS}$  to fall below 1 LSB of the ADC. With the given example values, a 1.2-k $\Omega$  sense resistor satisfies both requirements shown in Table 13.

**Table 13.  $V_{SNS}$  Calculation**

| LOAD (A) | SENSE RATIO | $I_{SNS}$ (mA) | $R_{SNS}$ ( $\Omega$ ) | $V_{SNS}$ (V) | % of 5-V ADC |
|----------|-------------|----------------|------------------------|---------------|--------------|
| 0.060    | 3000        | 0.02           | 1200                   | 0.024         | 0.5%         |
| 12       | 3000        | 4              | 1200                   | 4.800         | 96.0%        |

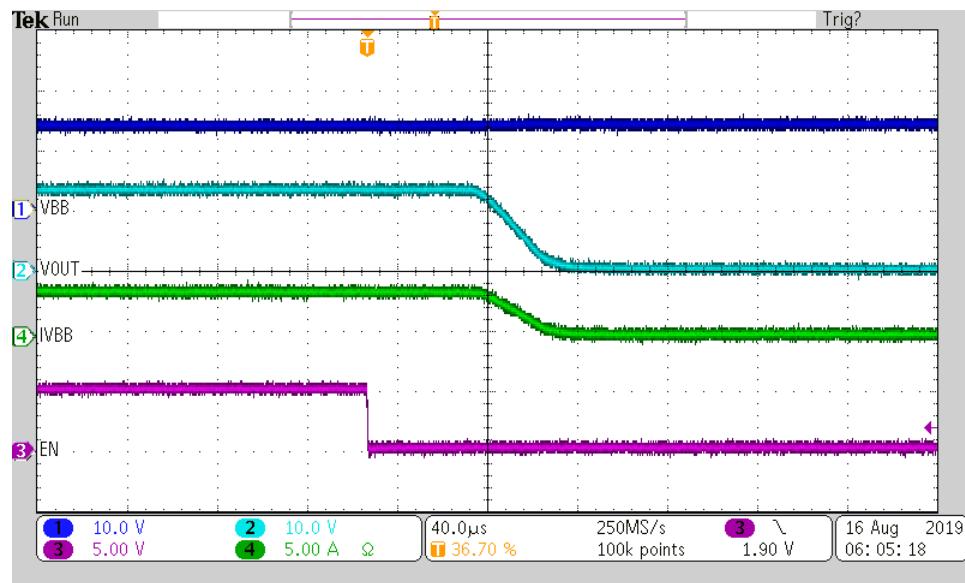
### 10.3.3 Application Curves

When the device receives a rising edge on the ENx pulse the output will turn on as shown in Figure 53. After the turn-on delay time, the device  $V_{OUT}$  goes to the  $V_{BB}$  supply and begins outputting the steady state resistive current.



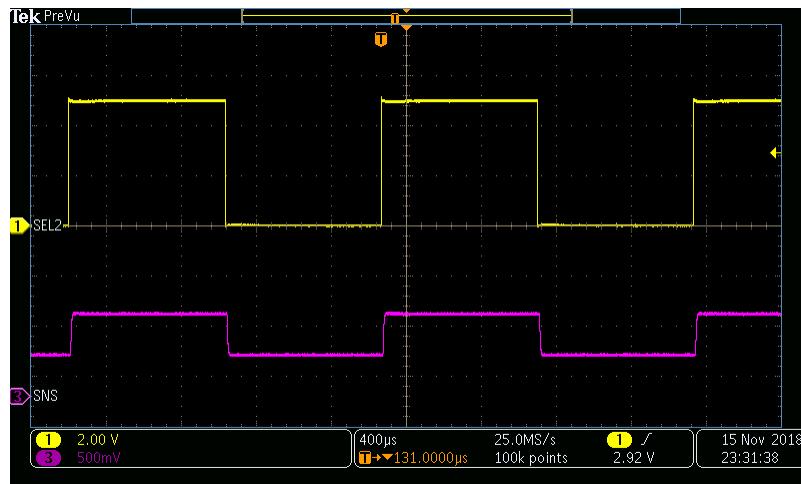
**Figure 53. Turn On Waveform**

When the device turns off on a falling edge of ENx, the channel  $I_{OUT}$  will go to zero and the  $V_{OUT}$  will drop to zero as well as shown in Figure 54.



**Figure 54. Turn-Off Waveform**

While enabled, it is important to measure the output current through both channels. Figure 55 shows this behavior when toggling the SELx pins. The image shows that when SEL2 toggles high to low, the SNS pin toggles between representing  $I_{OUT1}$  and  $I_{OUT2}$ . When SEL2 is low SNS represents  $I_{OUT1}$  and when SEL2 is high SNS represents  $I_{OUT2}$ . This image shows that channel 2 is currently outputting twice the output current as channel 1.



**Figure 55. Toggling Between CH1 and CH2 Current Measurement**

Figure 56 shows the SNS current behavior when there is a load step. The image shows the output current temporarily increase from 1 A to 5 A and then return to 1 A. In this situation, the output current is accurately modeled throughout the pulse by the voltage on the SNS pin allowing for accurate diagnostics.

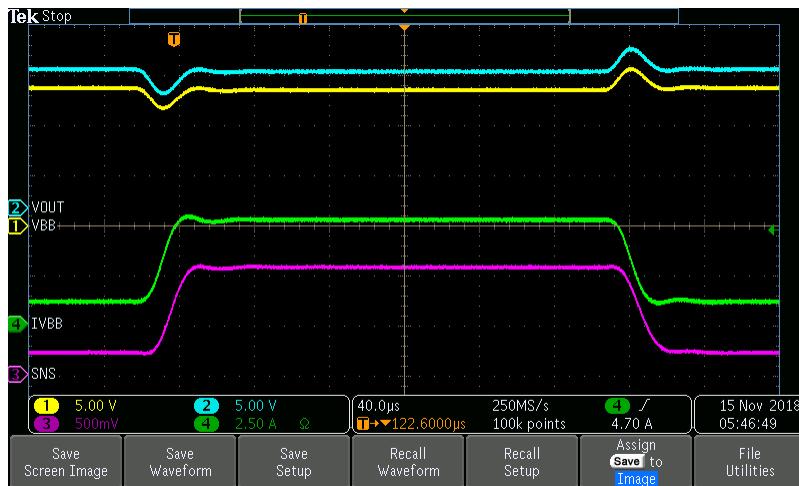


Figure 56. SNS Settling Time

If the output of the TPS2HB16-Q1 is short-circuited, the device will protect the system from failure. shows the device turning off the output at a set current limit when the output is short circuited. (Note: shows a case with a higher  $R_{ILIM}$  than calculated in this example, so the current limit is higher than ).

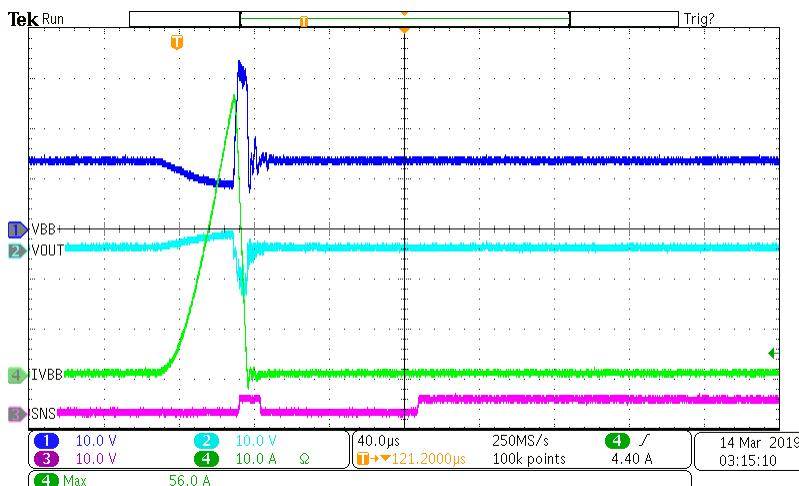


Figure 57. TPS2HB16B-Q1 Short Circuit Waveform

## 11 Power Supply Recommendations

The TPS2HB16-Q1 device is designed to operate in a 12-V automotive system. The nominal supply voltage range is 6 V to 18 V as measured at the  $V_{BB}$  pin with respect to the GND pin of the device. In this range the device meets full parametric specifications as listed in the [Electrical Characteristics](#) table. The device is also designed to withstand voltage transients beyond this range. When operating outside of the nominal voltage range but within the operating voltage range, the device will exhibit normal functional behavior. However, parametric specifications may not be specified outside the nominal supply voltage range.

Table 14. Operating Voltage Range

| $V_{BB}$ Voltage Range | Note   |
|------------------------|--|
| 3 V to 6 V             | Transients such as cold crank and start-stop, functional operation are specified but some parametric specifications may not apply. The device is completely short-circuit protected up to 125°C. |

**Table 14. Operating Voltage Range (continued)**

| <b>V<sub>BB</sub> Voltage Range</b> | <b>Note</b>   |
|-------------------------------------|---|
| 6 V to 18 V                         | Nominal supply voltage, all parametric specifications apply. The device is completely short-circuit protected up to 125°C.    |
| 18 V to 40 V                        | Transients such as jump-start and load-dump, functional operation specified but some parametric specifications may not apply. |

## 12 Layout

### 12.1 Layout Guidelines

To achieve optimal thermal performance, connect the exposed pad to a large copper pour. On the top PCB layer, the pour may extend beyond the package dimensions as shown in the example below. In addition to this, it is recommended to have a  $V_{BB}$  plane either on one of the internal PCB layers or on the bottom layer.

Vias should connect this plane to the top  $V_{BB}$  pour.

Ensure that all external components are placed close to the pins. Device current limiting performance can be harmed if the  $R_{ILIM}$  is far from the pins and extra parasitics are introduced.

### 12.2 Layout Example

The layout example shown below is for device versions A/B.

For version F, there will be minor differences due to the open-drain  $\overline{FLT1}$  and  $\overline{FLT2}$  pins and the removal of the  $ILIM1$  and  $ILIM2$  pins.

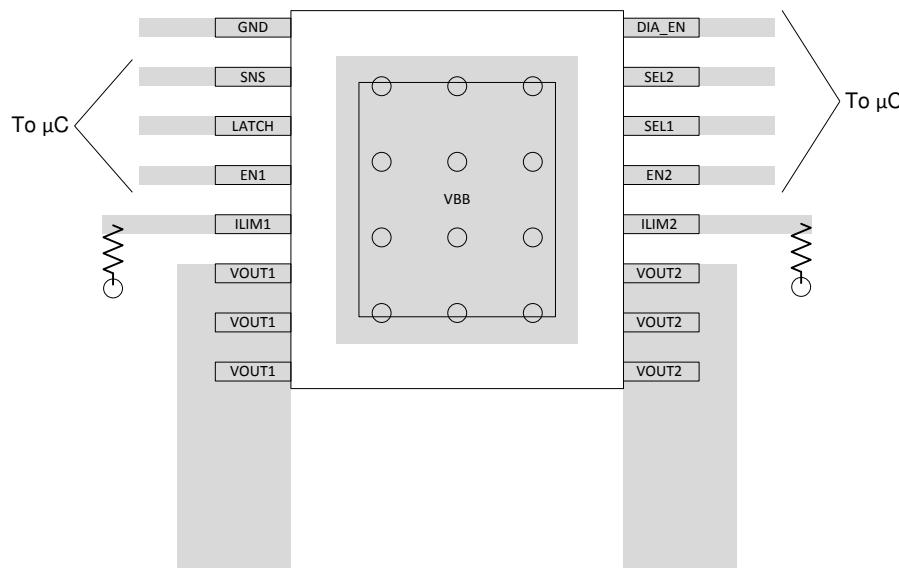


Figure 58. PWP Layout Example

## 13 Device and Documentation Support

### 13.1 Documentation Support

#### 13.1.1 Related Documentation

For related documentation see the following:

- TI's [How To Drive Inductive, Capacitive, and Lighting Loads with Smart High Side Switches](#)
- TI's [Short Circuit Reliability Test for Smart Power Switch](#)
- TI's [Adjustable Current Limit of Smart Power Switches](#)
- TI's [TPS2HB35-Q1 40-V, 35-mΩ Dual-Channel Smart High-Side Switch](#)
- TI's [Improved Automotive Short Circuit Reliability with Adjustable Current Limiting](#)

### 13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 13.3 Support Resources

[TI E2ETM support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 13.4 Trademarks

E2E is a trademark of Texas Instruments.

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### 13.5 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

 ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 13.6 Glossary

[SLYZ022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TPS2HB16AQPWPRQ1      | Active        | Production           | HTSSOP (PWP)   16 | 3000   LARGE T&R      | ROHS Exempt | NIPDAU                               | Level-3-260C-168HRS               | -40 to 125   | 2HB16AQ             |
| TPS2HB16AQPWPRQ1.A    | Active        | Production           | HTSSOP (PWP)   16 | 3000   LARGE T&R      | ROHS Exempt | NIPDAU                               | Level-3-260C-168HRS               | -40 to 125   | 2HB16AQ             |
| TPS2HB16BQPWPRQ1      | Active        | Production           | HTSSOP (PWP)   16 | 3000   LARGE T&R      | ROHS Exempt | NIPDAU                               | Level-3-260C-168HRS               | -40 to 125   | 2HB16BQ             |
| TPS2HB16BQPWPRQ1.A    | Active        | Production           | HTSSOP (PWP)   16 | 3000   LARGE T&R      | ROHS Exempt | NIPDAU                               | Level-3-260C-168HRS               | -40 to 125   | 2HB16BQ             |
| TPS2HB16FQPWPRQ1      | Active        | Production           | HTSSOP (PWP)   16 | 3000   LARGE T&R      | ROHS Exempt | NIPDAU                               | Level-3-260C-168HRS               | -40 to 125   | 2HB16FQ             |
| TPS2HB16FQPWPRQ1.A    | Active        | Production           | HTSSOP (PWP)   16 | 3000   LARGE T&R      | ROHS Exempt | NIPDAU                               | Level-3-260C-168HRS               | -40 to 125   | 2HB16FQ             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

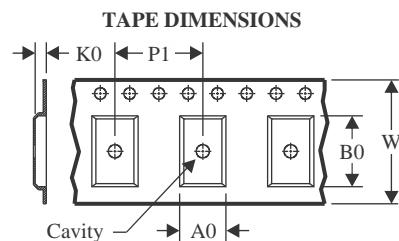
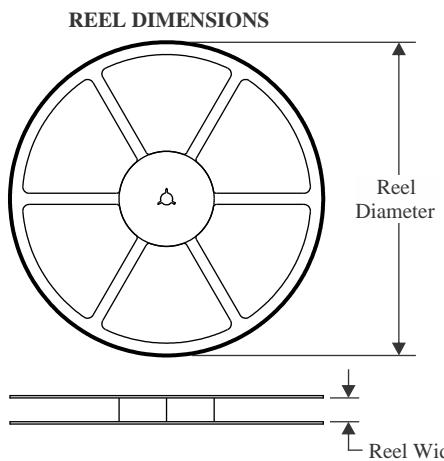
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

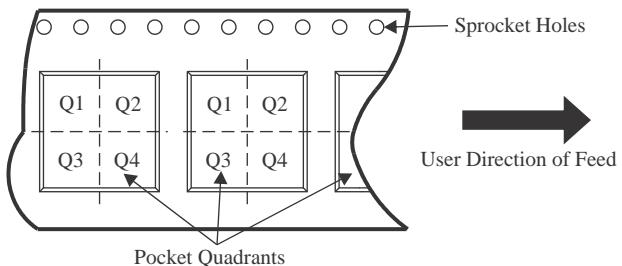
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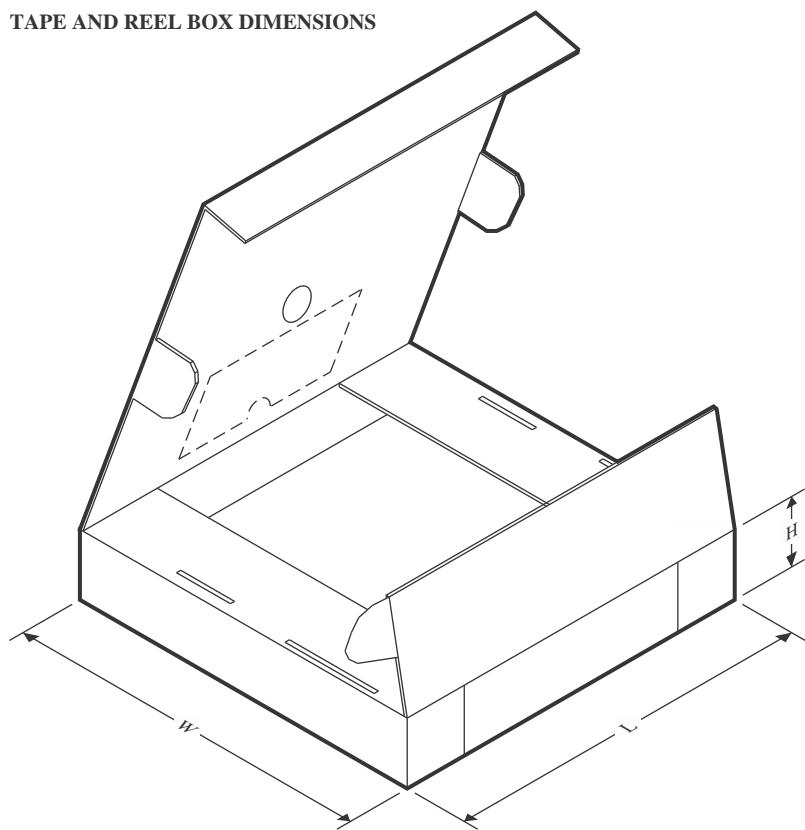
**TAPE AND REEL INFORMATION**


|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS2HB16AQPWPRQ1 | HTSSOP       | PWP             | 16   | 3000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TPS2HB16BQPWPRQ1 | HTSSOP       | PWP             | 16   | 3000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TPS2HB16FQPWPRQ1 | HTSSOP       | PWP             | 16   | 3000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

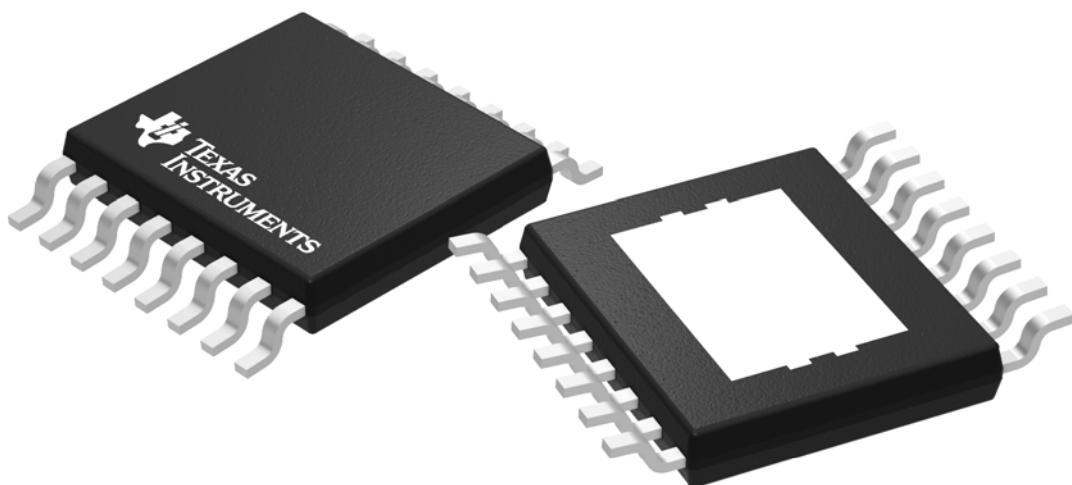
| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS2HB16AQPWPRQ1 | HTSSOP       | PWP             | 16   | 3000 | 350.0       | 350.0      | 43.0        |
| TPS2HB16BQPWPRQ1 | HTSSOP       | PWP             | 16   | 3000 | 350.0       | 350.0      | 43.0        |
| TPS2HB16FQPWPRQ1 | HTSSOP       | PWP             | 16   | 3000 | 350.0       | 350.0      | 43.0        |

## GENERIC PACKAGE VIEW

PWP 16

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4073225-3/J

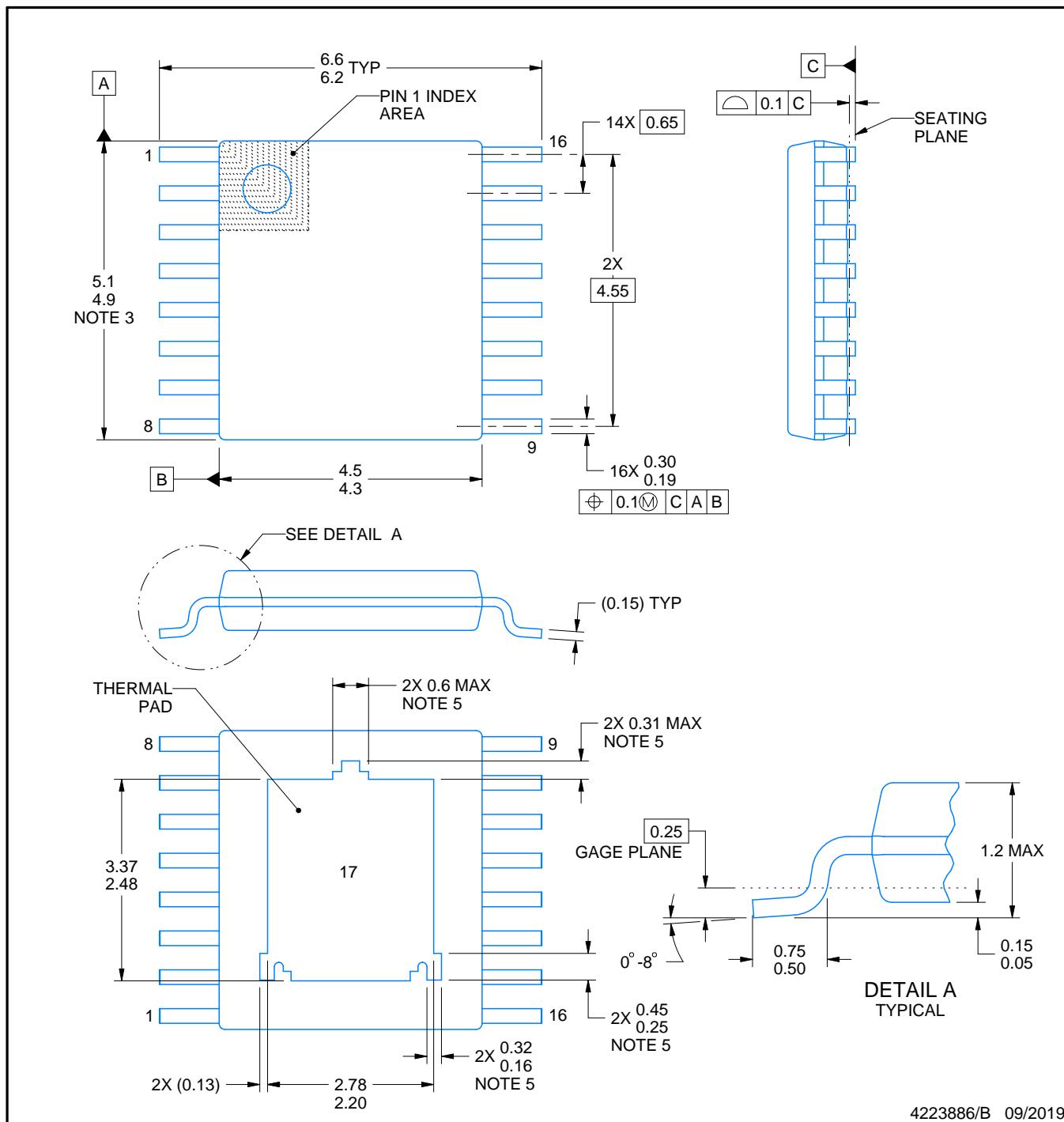
# PACKAGE OUTLINE

PWP0016M



PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

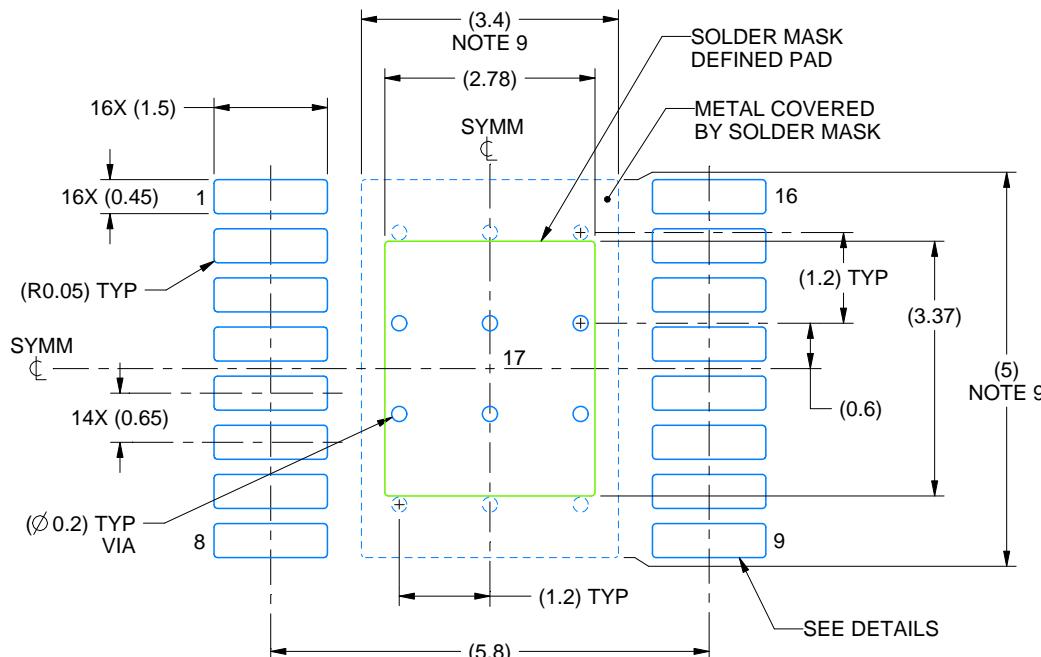
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

# EXAMPLE BOARD LAYOUT

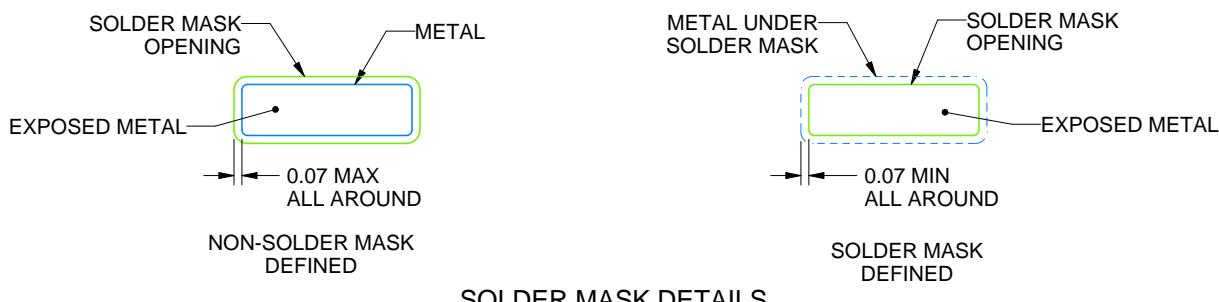
PWP0016M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

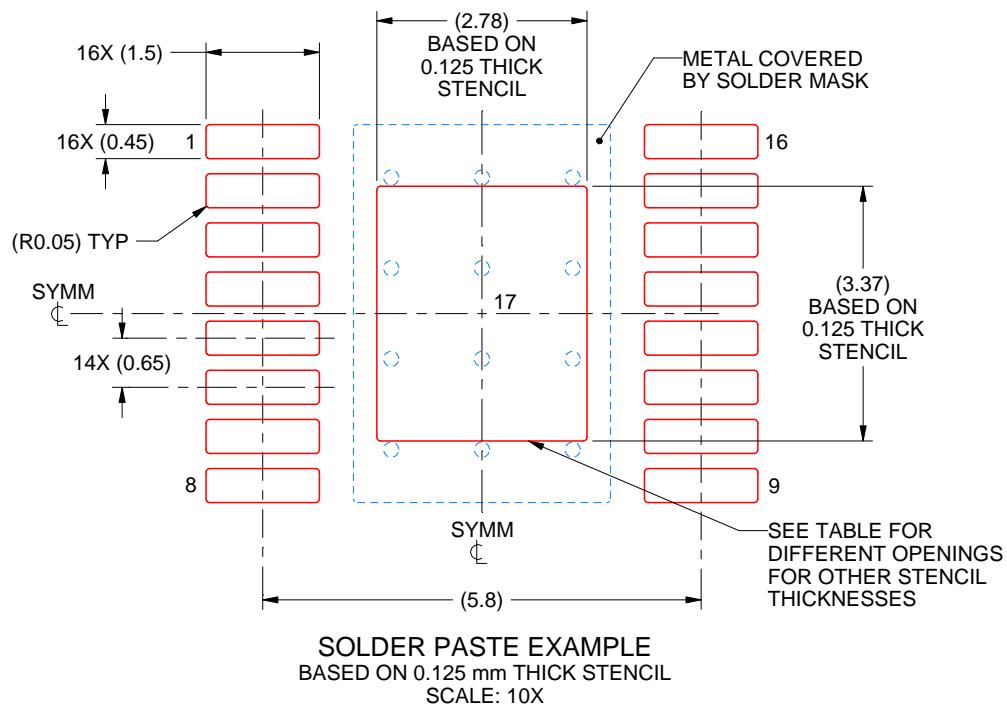
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

PWP0016M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1               | 3.11 X 3.77            |
| 0.125             | 2.78 X 3.37 (SHOWN)    |
| 0.15              | 2.54 X 3.08            |
| 0.175             | 2.35 X 2.85            |

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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