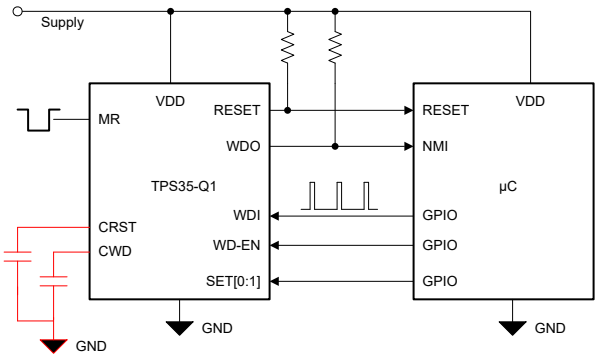
TPS35-Q1 Automotive Nano IQ Precision Voltage Supervisor with Precision Timeout Watchdog Timer

1 Features

- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
- Factory programmed or user-programmable watchdog timeout
  - ±10% Accurate timer (maximum)
  - Factory programmed: 1ms to 100s
- Factory programmed or user-programmable reset delay
  - ±10% Accurate timer (maximum)
  - Factory programmed option: 2ms to 10s
- Input voltage range: V_{DD} = 1.04V to 6.0V
- Fixed threshold voltage (V_{IT-}): 1.05V to 5.4V
  - Threshold voltage available in 50mV steps
  - 1.2% Voltage threshold accuracy (maximum)
  - Built-in hysteresis (V_{HYS}): 5% (typical)
- Ultra low supply current: I_{DD} = 250nA (typical)
- Open-drain, push-pull; active-low outputs
- Various programmability options:
  - Watchdog enable-disable
  - Watchdog startup delay: no delay to 10s
  - On the fly timer extension: 1X to 256X
  - Latched output option
- $\overline{MR}$ functionality support

2 Applications

- On-board (OBC) and wireless charger
- Driver monitoring
- Battery Management System (BMS)
- Front camera
- Surround view system ECU



TPS35-Q1 offers various pinout options to support different features. Choose suitable pinout based on application needs

Typical Application Circuit

3 Description

The TPS35-Q1 is an ultra-low power consumption (250nA typical) device offering a precision voltage supervisor with a programmable timeout watchdog timer. The TPS35-Q1 supports wide threshold levels for undervoltage supervision with 1.2% accuracy across the specified temperature range.

The TPS35-Q1 offers a high accuracy timeout watchdog timer with a host of features for a wide variety of applications. The timeout watchdog timer can be factory programmed or user programmed using an external capacitor. The timer value can be changed on-the-fly using a combination of logic pins. The watchdog also offers unique features such as enable-disable, start-up delay, independent WDO pin option.

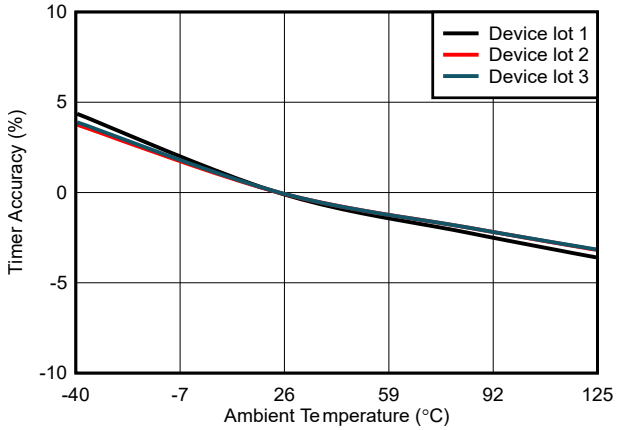
The $\overline{RESET}$ or $\overline{WDO}$ delay can be set by factory-programmed default delay settings or programmed by an external capacitor. The device also offers a latched output operation where the output is latched until the supervisor or watchdog fault is cleared.

The TPS35-Q1 provides a performance upgrade alternative to TPS3851-Q1 device family. The TPS35-Q1 is available in a small 8-pin SOT-23 package.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM) (2)
TPS35-Q1	DDF (8)	2.90mm × 1.60mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



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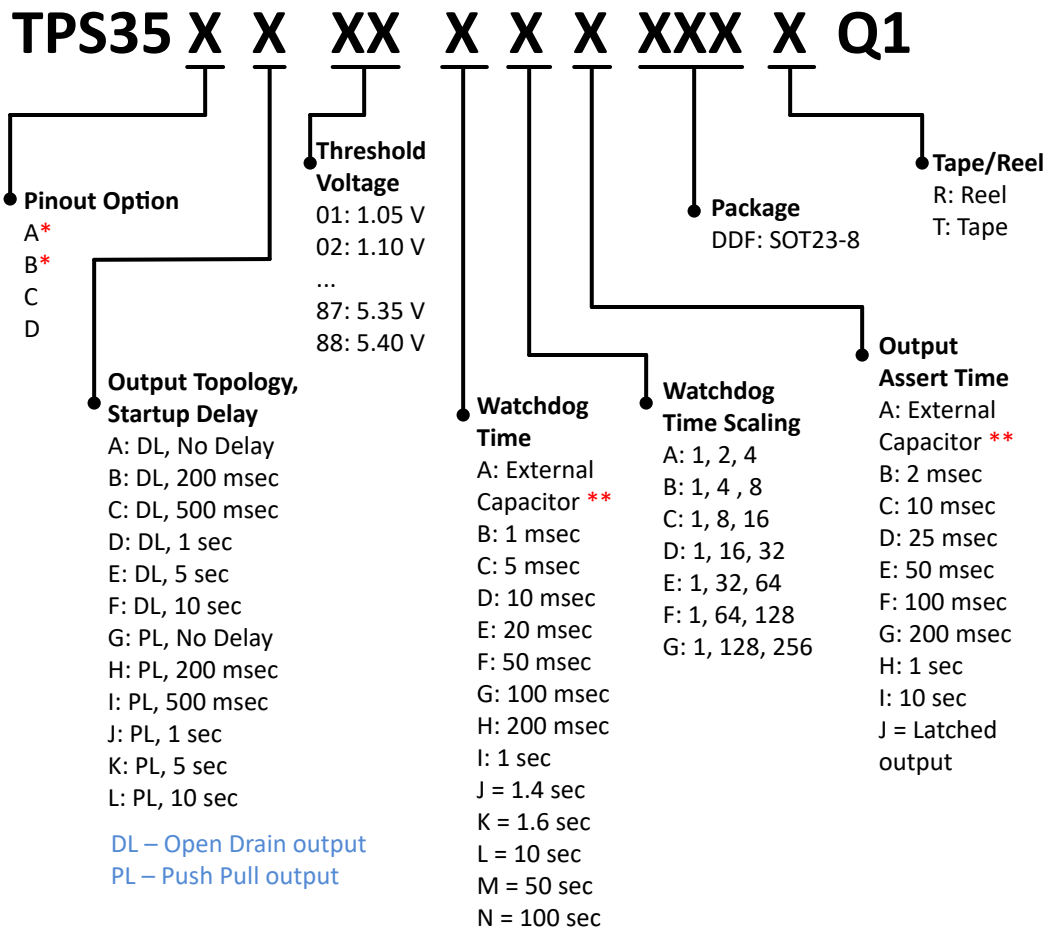
4 Device Comparison

Figure 4-1 shows the device naming nomenclature of the TPS35-Q1. For all possible output types, threshold voltage options, watchdog time options and output assert delay options, see Section 7 or Table 4-1 for more details. Contact TI sales representatives or on TI's E2E forum for detail and availability of other options.

Table 4-1. Available devices

Device	Function [2]	Pinout [3]	WD Timeout	Startup-Delay	Time Scaling	Output Pulse	Output Topology	Vit-
TPS3435CAEBJDDFR [1]	WD	C	20ms	0	1, 4, 8	Latched	open-drain	N/A
TPS3435CAGBJDDFRQ1 [1]	WD	C	100ms	0	1, 4, 8	Latched	open-drain	N/A
TPS3435CBHAJDDFR [1]	WD	C	200ms	200ms	1, 2, 4	Latched	open-drain	N/A
TPS3435CCGAJDDFR [1]	WD	C	100ms	500ms	1, 2, 4	Latched	open-drain	N/A
TPS3435CECAJDDFRQ1 [1]	WD	C	5ms	5s	1, 2, 4	Latched	open-drain	N/A
TPS3435CGLEFDDFR [1]	WD	C	10s	0	1, 32, 64	100ms	push-pull	N/A
TPS3435CAKAGDDFR	WD	C	1.6s	0	1, 2, 4	200ms	open-drain	N/A
TPS3435AFACADDFRQ1	WD	A	Adjustable	10s	1, 8	Adjustable	open-drain	N/A
TPS3435CAKAGDDFRQ1	WD	C	1.6s	0	1, 2, 4	200ms	open-drain	N/A
TPS3435CAIEGDDFR	WD	C	1s	0	1, 32, 64	200ms	open-drain	N/A
TPS3435JAJAJDSER [1]	WD	J	1.4s	0	1, 2	Latched	open-drain	N/A
TPS3435JFMAFDSER [1]	WD	J	50s	10s	1, 2	100ms	open-drain	N/A
TPS35CA38GACDDFRQ1 [1]	WD + SVS	C	100ms	0	1, 2, 4	10ms	open-drain	2.9V
TPS35DA40GCJDDFR [1]	WD + SVS	D	100ms	0	1, 8, 16	Latched	open-drain	3V
TPS35DA69GADDDFRQ1 [1]	WD + SVS	D	100ms	0	1, 2, 4	25ms	open-drain	4.45V
TPS35JE42IADDSER [1]	WD + SVS	J	1s	20ms	1, 2	25ms	open-drain	3.1V
TPS35AA17AGADDFR	WD + SVS	A	Adjustable	0	1, 128	Adjustable	open-drain	1.85V
TPS35JE35JADDSER	WD + SVS	J	1.4s	5s	1, 2	25ms	open-drain	2.75V
TPS35AA38AGADDFRQ1	WD + SVS	A	Adjustable	0	1, 128	Adjustable	open-drain	2.9V
TPS35CA43DACDDFRQ1	WD + SVS	C	10ms	0	1, 2, 4	10ms	open-drain	3.15V
TPS35CA38IAGDDFRQ1 [1]	WD + SVS	C	1s	0	1, 2, 4	200ms	open-drain	2.9V

(1) Product preview. Please check with a Texas Instruments representative for availability.
(2) WD = Watchdog , SVS = Voltage Supervisor
(3) Please refer to Section 5 for pinout information



* Pinout option supports Start up Delay settings of “No Delay” and “10 sec” only.
** Capacitor programmable time feature available with pinout options A & B. For fixed time and latched output features use pinout options C & D.
Refer ‘Mechanical, Packaging and Orderable Information’ section for list of released orderable. For any other orderable, contact local TI support.

Figure 4-1. Device Naming Nomenclature

TPS35-Q1 belongs to family of pin compatible devices offering different feature sets as highlighted in Table 4-2.

Table 4-2. Pin Compatible Device Families

DEVICE	VOLTAGE SUPERVISOR	TYPE OF WATCHDOG
TPS35-Q1	Yes	Timeout
TPS36-Q1	Yes	Window
TPS3435-Q1	No	Timeout
TPS3436-Q1	No	Window

5 Pin Configuration and Functions

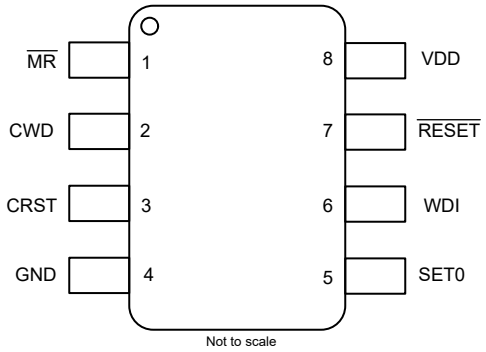


Figure 5-1. Pin Configuration Option A DDF Package, 8-Pin SOT-23, TPS35-Q1 Top View

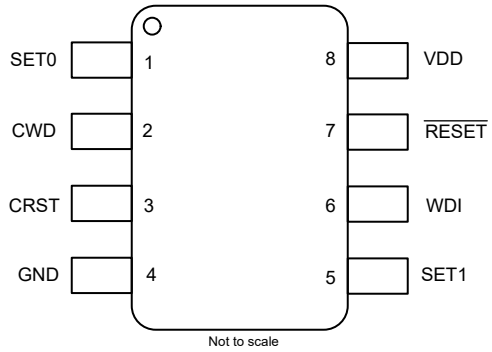


Figure 5-2. Pin Configuration Option B DDF Package, 8-Pin SOT-23, TPS35-Q1 Top View

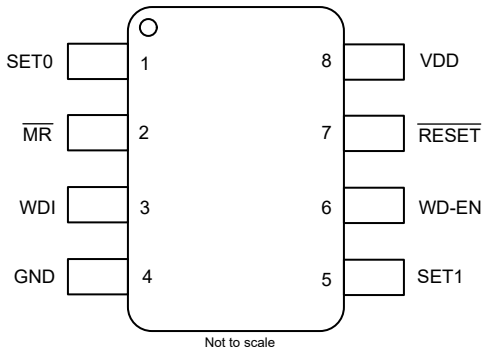


Figure 5-3. Pin Configuration Option C DDF Package, 8-Pin SOT-23, TPS35-Q1 Top View

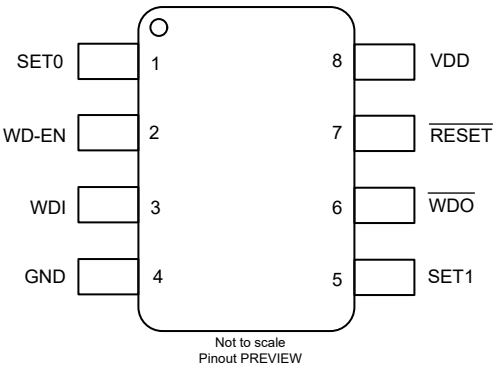


Figure 5-4. Pin Configuration Option D DDF Package, 8-Pin SOT-23, TPS35-Q1 Top View

Table 5-1. Pin Functions

PIN NAME	PIN NUMBER				I/O	DESCRIPTION
	PINOUT A	PINOUT B	PINOUT C	PINOUT D		
CRST	3	3	—	—	I	Programmable reset timeout pin. Connect a capacitor between this pin and GND to program the reset timeout period. See *Section 7.3.4* for more details.
CWD	2	2	—	—	I	Programmable watchdog timeout input. Watchdog timeout is set by connecting a capacitor between this pin and ground. See *Section 7.3.2.1* for more details.
GND	4	4	4	4	—	Ground pin
$\overline{MR}$	1	—	2	—	I	Manual reset pin. A logic low on this pin asserts the $\overline{RESET}$. See *Section 7.3.3* for more details.
$\overline{RESET}$	7	7	7	7	O	Reset output. Connect $\overline{RESET}$ to VDD using a pull up resistance when using open drain output. $\overline{RESET}$ is asserted when the voltage at the VDD pin goes below the undervoltage threshold (V_{IT-}) or $\overline{MR}$ pin is driven LOW. For pinout options which do not support independent $\overline{WDO}$ pin, $\overline{RESET}$ is also asserted for watchdog error. See *Section 7.3.4* for more details.
SET0	5	1	1	1	I	Logic input. SET0, SET1, and WD-EN pins select the watchdog timer scaling and enable-disable the watchdog; see *Section 7.3.2.4* for more details.
SET1	—	5	5	5	I	Logic input. SET0, SET1, and WD-EN pins select the watchdog timer scaling and enable-disable the watchdog; see *Section 7.3.2.4* for more details.
VDD	8	8	8	8	I	Supply voltage pin. For noisy systems, connecting a 0.1µF bypass capacitor is recommended.
WD-EN	—	—	6	2	I	Logic input. Logic high input enables the watchdog monitoring feature. See *Section 7.3.2.2* for more details.
WDI	6	6	3	3	I	Watchdog input. A falling transition (edge) must occur at this pin before the timeout expires in order for $\overline{RESET}$ / $\overline{WDO}$ to not assert. See *Section 7.3.2* for more details.
$\overline{WDO}$	—	—	—	6	O	Watchdog output. Connect $\overline{WDO}$ to VDD using pull up resistance when using open drain output. $\overline{WDO}$ asserts when a watchdog error occurs. $\overline{WDO}$ only asserts when $\overline{RESET}$ is high. When a watchdog error occurs, $\overline{WDO}$ asserts for the set $\overline{RESET}$ timeout delay (t_D). When $\overline{RESET}$ is asserted, $\overline{WDO}$ is deasserted and watchdog functionality is disabled. See *Section 7.3.4* for more details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted(1)

		MIN	MAX	UNIT
Voltage	VDD	–0.3	6.5	V
Voltage	C_{WD}, C_{RST}, WD–EN, SETx, WDI, $\overline{MR}$ (2), $\overline{RESET}$ (Push Pull), $\overline{WDO}$ (Push Pull)	–0.3	V_{DD}+0.3 (3)	V
	$\overline{RESET}$ (Open Drain), $\overline{WDO}$ (Open Drain)	–0.3	6.5	
Current	$\overline{RESET}$, $\overline{WDO}$ pin	–20	20	mA
Temperature (4)	Operating ambient temperature, T_A	–40	125	℃
Temperature	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If the logic signal driving $\overline{MR}$ is less than V_{DD}, then additional current flows into V_{DD} and out of $\overline{MR}$.
(3) The absolute maximum rating is (VDD + 0.3)V or 6.5V, whichever is smaller
(4) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	VDD (Active Low output)	0.9		6	V
	C_{WD}, C_{RST}, WD–EN, SETx, WDI, $\overline{MR}$ (1)	0		VDD	
	$\overline{RESET}$ (Open Drain) , $\overline{WDO}$ (Open Drain)	0		6	
	$\overline{RESET}$ (Open Drain) , $\overline{WDO}$ (Push Pull)	0		VDD	
Current	$\overline{RESET}$, $\overline{WDO}$ pin current	–5		5	mA
C_{RST}	C_{RST} pin capacitor range	1.5		1800	nF
C_{WD}	C_{WD} pin capacitor range	1.5		1000	nF
T_A	Operating ambient temperature	–40		125	℃

(1) If the logic signal driving $\overline{MR}$ is less than V_{DD}, then additional current flows into V_{DD} and out of $\overline{MR}$. V_{MR} should not be higher than V_{DD}.

6.4 Thermal Information

THERMAL METRIC[1]		TPS35-Q1 DDF (SOT23-8) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	175.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	94.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	92.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	91.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

At 1.04V ≤ V_{DD} ≤ 6V, $\overline{MR}$ = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100kΩ to VDD, $\overline{WDO}$ pull-up resistor ($R_{pull-up}$) = 100kΩ to VDD, output load (C_{LOAD}) = 10pF and over operating free-air temperature range –40°C to 125°C, unless otherwise noted. VDD ramp rate ≤ 1V/µs. Typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
COMMON PARAMETERS							
V_{DD}	Input supply voltage	Active LOW output		1.04		6	V
$V_{IT–}$	Negative-going input threshold accuracy (1)	$V_{IT–}$ = 1.05V to 1.95V		–1.4	±0.5	1.4	%
		$V_{IT–}$ = 2.0V to 5.4V		–1.2	±0.5	1.2	
V_{HYS}	Hysteresis $V_{IT–}$ pin	$V_{IT–}$ = 1.05V to 5.4V		3	5	7	%
I_{DD}	Supply current into VDD pin (2)	V_{DD} = 2V $V_{IT–}$ = 1.05V to 1.9V	T_A = –40°C to 85°C		0.25	0.8	µA
					0.25	3	
		V_{DD} = 6V $V_{IT–}$ = 1.05V to 5.4V	T_A = –40°C to 85°C		0.25	0.8	
					0.25	3	
V_{IL}	Low level input voltage WD–EN, WDI, SETx, $\overline{MR}$ (2)					$0.3V_{DD}$	V
V_{IH}	High level input voltage WD–EN, WDI, SETx, $\overline{MR}$ (2)			$0.7V_{DD}$			V
$R_{\overline{MR}}$	Manual reset internal pull-up resistance				100		kΩ
$\overline{RESET}$ / $\overline{WDO}$ (Open-drain active-low)							
V_{OL}	Low level output voltage	V_{DD} =1.5V, 1.55V ≤ $V_{IT–}$ ≤ 3.35V $I_{OUT(Sink)}$ = 500µA				300	mV
		V_{DD} = 3.3V, 3.4V ≤ $V_{IT–}$ ≤ 5.4V $I_{OUT(Sink)}$ = 2mA				300	mV
$I_{lkg(OD)}$	Open-Drain output leakage current	V_{DD} = V_{PULLUP} = 6V T_A = –40°C to 85°C			10	30	nA
		V_{DD} = V_{PULLUP} = 6V			10	120	nA
$\overline{RESET}$ / $\overline{WDO}$ (Push-pull active-low)							
V_{POR}	Power on $\overline{RESET}$ voltage (3)	$V_{OL(max)}$ = 300mV $I_{OUT(Sink)}$ = 15µA				900	mV
V_{OL}	Low level output voltage	V_{DD} = 0.9V, 1.05V ≤ $V_{IT–}$ ≤ 1.5V $I_{OUT(Sink)}$ = 15µA				300	mV
		V_{DD} = 1.5V, 1.55V ≤ $V_{IT–}$ ≤ 3.35V $I_{OUT(Sink)}$ = 500µA				300	
		V_{DD} = 3.3V, 3.4V ≤ $V_{IT–}$ ≤ 5.4V $I_{OUT(Sink)}$ = 2mA				300	
V_{OH}	High level output voltage	V_{DD} = 1.8V, 1.05V ≤ $V_{IT–}$ ≤ 1.4V $I_{OUT(Source)}$ = 500µA		$0.8V_{DD}$			V
		V_{DD} = 3.3V, 1.45V ≤ $V_{IT–}$ ≤ 3.0V $I_{OUT(Source)}$ = 500µA		$0.8V_{DD}$			
		V_{DD} = 6V, 3.05V ≤ $V_{IT–}$ ≤ 5.4V $I_{OUT(Source)}$ = 2mA		$0.8V_{DD}$			

(1) $V_{IT–}$ threshold voltage range from 1.05V to 5.4V in 50mV steps.
(2) If the logic signal driving $\overline{MR}$ is less than V_{DD}, then additional current flows into V_{DD} and out of $\overline{MR}$.
(3) V_{POR} is the minimum V_{DD} voltage level for a controlled output state

6.6 Timing Requirements

At 1.04V ≤ V_{DD} ≤ 6V, $\overline{MR}$ = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100kΩ to VDD, $\overline{WDO}$ pull-up resistor ($R_{pull-up}$) = 100kΩ to VDD, output RESET / WDO load (C_{LOAD}) = 10pF and over operating free-air temperature range –40℃ to 125℃, unless otherwise noted. VDD ramp rate ≤ 1V/µs. Typical values are at T_A = 25℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{GI_VIT-}	Glitch immunity V_{IT-}	5% V_{IT-} overdrive(1)		15		µs
$t_{\overline{MR}\_PW}$	$\overline{MR}$ pin pulse duration to assert reset			100		ns
t_{P-WD}	WDI pulse duration to start next frame (2)	V_{DD} > V_{IT-}	500			ns
$t_{HD-WDEN}$	WD-EN hold time to enable or disable WD operation (2)	V_{DD} > V_{IT-}	200			µs
$t_{HD-SETx}$	SETx hold time to change WD timer setting (2)	V_{DD} > V_{IT-}	150			µs
t_{WD}	Watchdog timeout period	Orderable Option TPS35xxxxB	0.8	1	1.2	ms
		Orderable Option TPS35xxxxC	4	5	6	
		Orderable Option TPS35xxxxD	9	10	11	
		Orderable Option TPS35xxxxE	18	20	22	
		Orderable Option TPS35xxxxF	45	50	55	
		Orderable Option TPS35xxxxG	90	100	110	
		Orderable Option TPS35xxxxH	180	200	220	
		Orderable Option TPS35xxxxI	0.9	1	1.1	s
		Orderable Option TPS35xxxxJ	1.26	1.4	1.54	
		Orderable Option TPS35xxxxK	1.44	1.6	1.76	
		Orderable Option TPS35xxxxL	9	10	11	
		Orderable Option TPS35xxxxM	45	50	55	
		Orderable Option TPS35xxxxN	90	100	110	

(1) Overdrive % = [(V_{DD}/ V_{IT-}) – 1] × 100%
(2) Not production tested

6.7 Switching Characteristics

At 1.04V ≤ V_{DD} ≤ 6V, $\overline{MR}$ = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100kΩ to VDD, $\overline{WDO}$ pull-up resistor ($R_{pull-up}$) = 100kΩ to VDD, output RESET / WDO load (C_{LOAD}) = 10pF and over operating free-air temperature range –40℃ to 125℃, unless otherwise noted. VDD ramp rate ≤ 1V/µs. Typical values are at T_A = 25℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STRT}	Startup delay(2)				500	µs
t_{P_HL}	RESET detect delay for VDD falling below V_{IT-}	V_{DD}: (V_{IT+} + 10%) to (V_{IT-} – 10%) (1)		30	50	µs
t_{SD}	Watchdog startup delay	Orderable part number TPS35xA, TPS35xG		0		ms
		Orderable part number TPS35xB, TPS35xH	180	200	220	
		Orderable part number TPS35xC, TPS35xI	450	500	550	
		Orderable part number TPS35xD, TPS35xJ	0.9	1	1.1	s
		Orderable part number TPS35xE, TPS35xK	4.5	5	5.5	
		Orderable part number TPS35xF, TPS35xL	9	10	11	
t_D	Reset time delay (3)	Orderable part number TPS35xxxxxxB	1.6	2	2.4	ms
		Orderable part number TPS35xxxxxxC	9	10	11	ms
		Orderable part number TPS35xxxxxxD	22.5	25	27.5	ms
		Orderable part number TPS35xxxxxxE	45	50	55	ms
		Orderable part number TPS35xxxxxxF	90	100	110	ms
		Orderable part number TPS35xxxxxxG	180	200	220	ms
		Orderable part number TPS35xxxxxxH	0.9	1	1.1	s
		Orderable part number TPS35xxxxxxI	9	10	11	s
t_{WDO}	Watchdog timeout delay			t_D		s
$t_{\overline{MR}\_RES}$	Propagation delay from $\overline{MR}$ low to reset assertion	V_{DD} ≥ V_{IT-} + 0.2V, $\overline{MR}$ = $V_{\overline{MR}\_H}$ to $V_{\overline{MR}\_L}$		100		ns
$t_{\overline{MR}\_tD}$	Delay from $\overline{MR}$ release to reset deassert	V_{DD} = 3.3V, $\overline{MR}$ = $V_{\overline{MR}\_L}$ to $V_{\overline{MR}\_H}$		t_D		s

(1) t_{P_HL} measured from threshold trip point (V_{IT-}) to RESET assert. V_{IT+} = V_{IT-} + V_{HYS}
(2) Specified by design parameter. When VDD starts from less than the specified minimum V_{DD} and then exceeds V_{IT+}, reset is deasserted after the startup delay (t_{STRT}) + t_D delay.
(3) VDD voltage transitions from (V_{IT-} - 10%) to (V_{IT-} + 10%)

6.8 Timing Diagrams

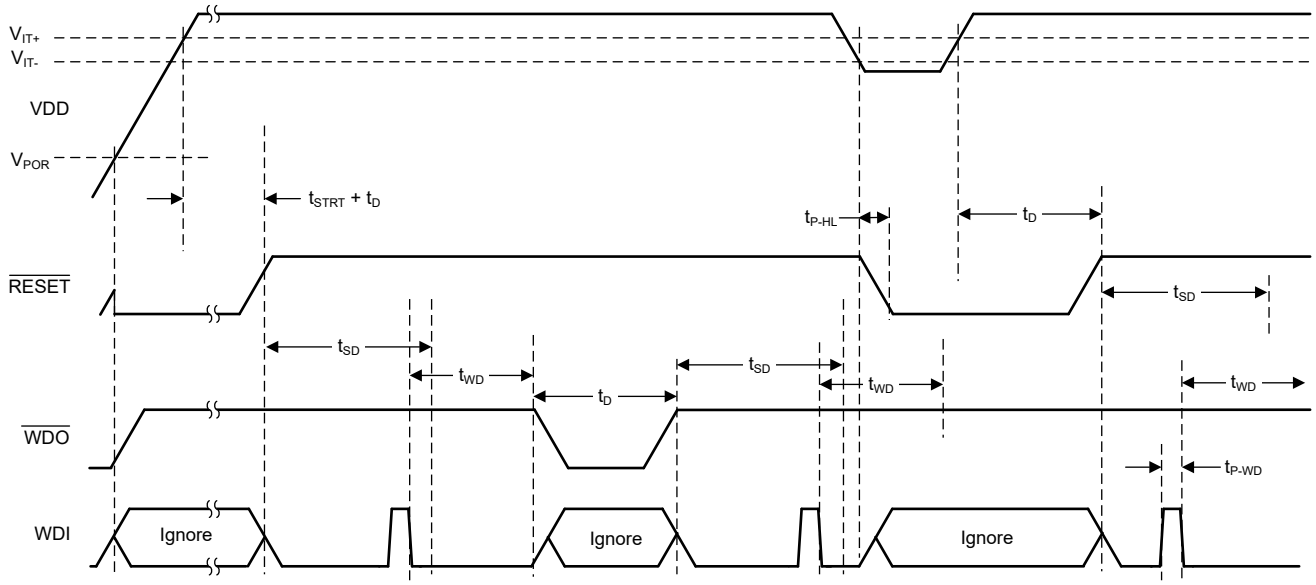


Figure 6-1. Functional Timing Diagram

6.9 Typical Characteristics

all curves are taken at T_A = 25°C (unless otherwise noted)

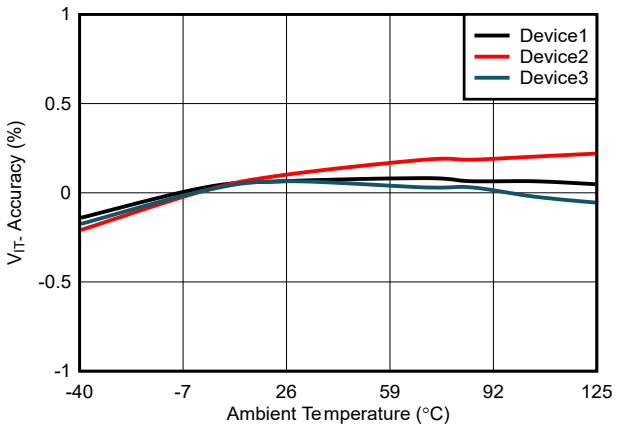


Figure 6-2. V_{IT-} Accuracy vs Temperature

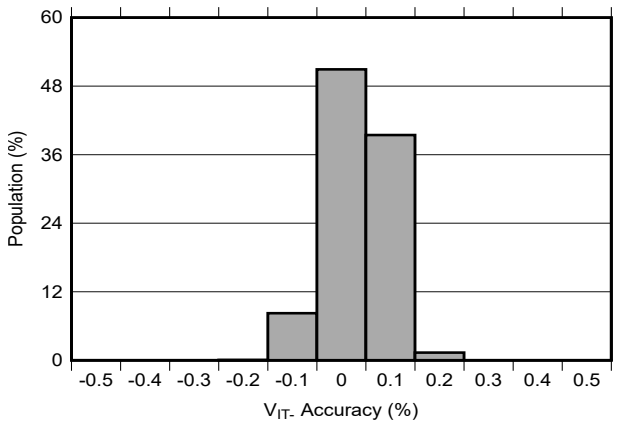


Figure 6-3. V_{IT-} Accuracy Histogram

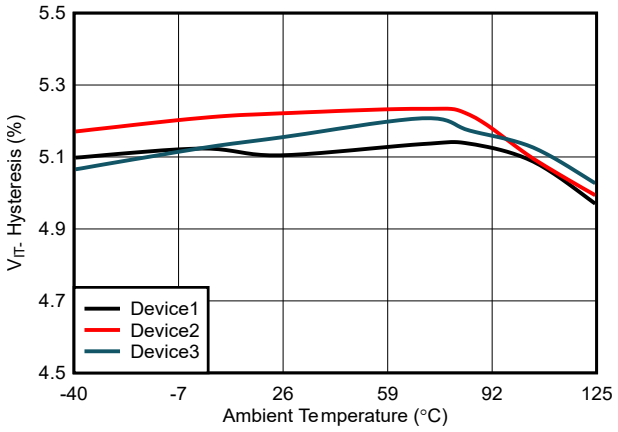


Figure 6-4. V_{IT-} Hysteresis Vs Temperature

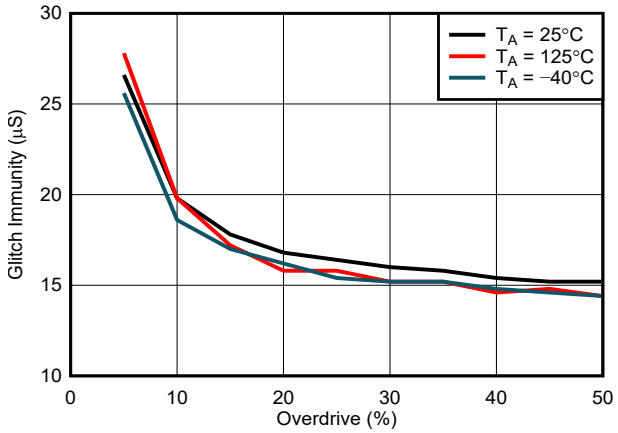


Figure 6-5. Supply Glitch Immunity vs Overdrive

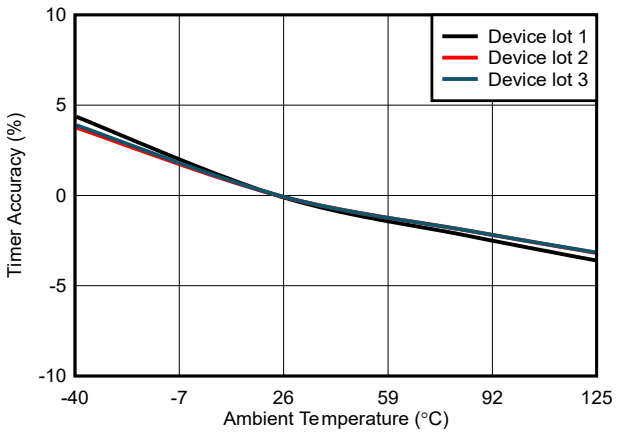


Figure 6-6. Timer Accuracy vs Temperature

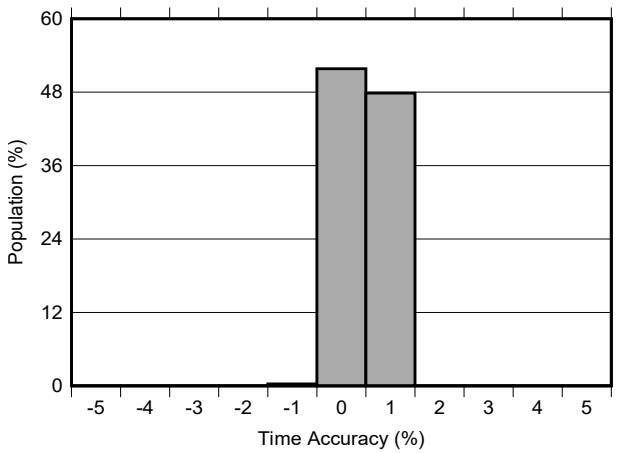


Figure 6-7. Timer Accuracy Histogram

6.9 Typical Characteristics (continued)

all curves are taken at T_A = 25°C (unless otherwise noted)

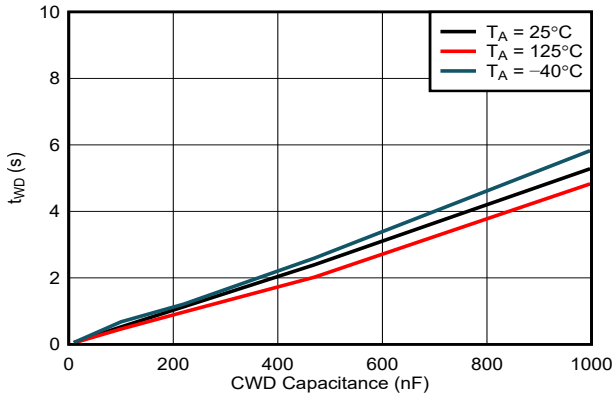


Figure 6-8. t_{WD} vs Capacitance

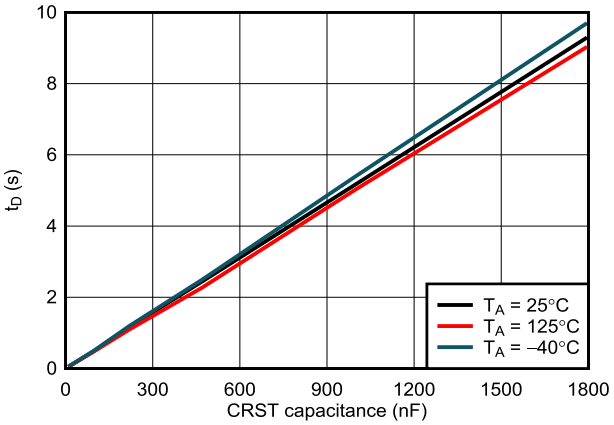


Figure 6-9. t_D vs Capacitance

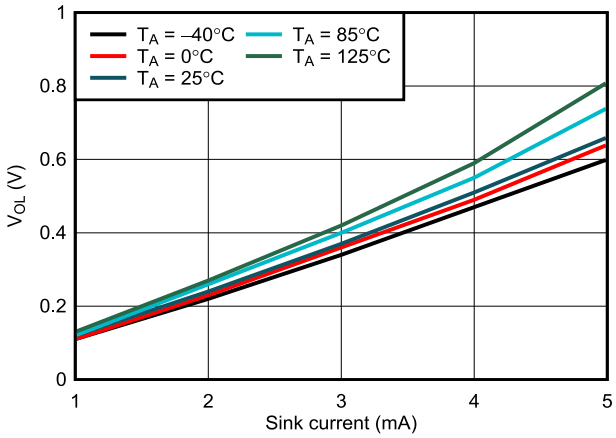


Figure 6-10. RESET V_{OL} vs I_{sink}, V_{DD} = 1.5V

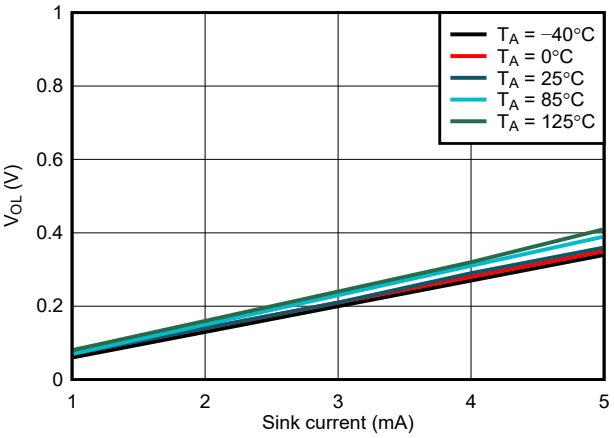


Figure 6-11. WDO V_{OL} vs I_{sink}, V_{DD} = 1.5V

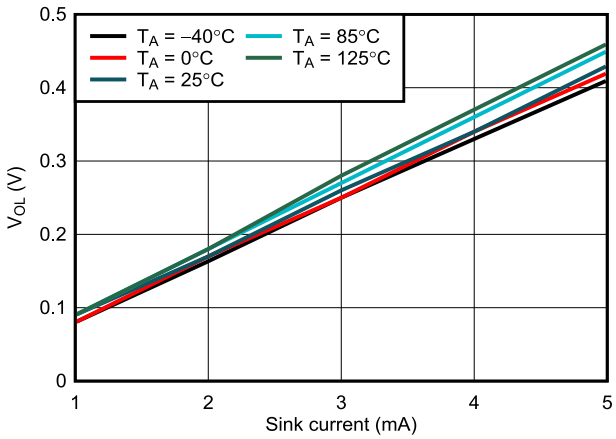


Figure 6-12. RESET V_{OL} vs I_{sink}, V_{DD} = 3.3V

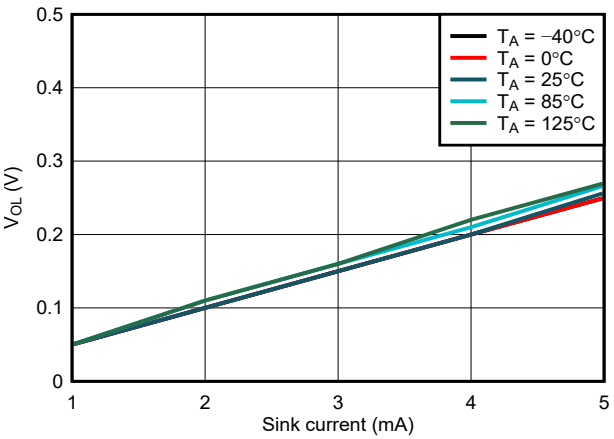


Figure 6-13. WDO V_{OL} vs I_{sink}, V_{DD} = 3.3V

6.9 Typical Characteristics (continued)

all curves are taken at T_A = 25°C (unless otherwise noted)

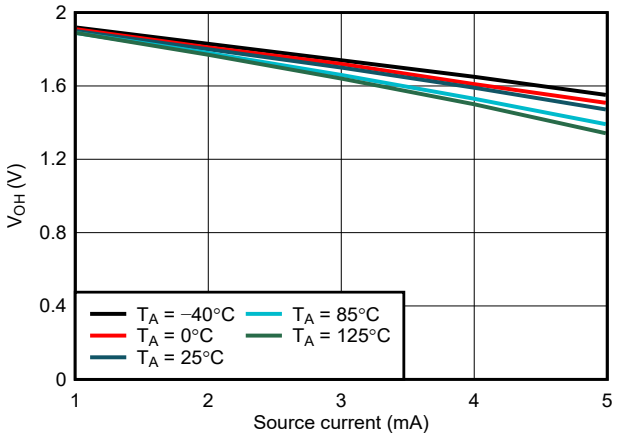


Figure 6-14. RESET V_{OH} vs I_{source}, V_{DD} = 2.0V

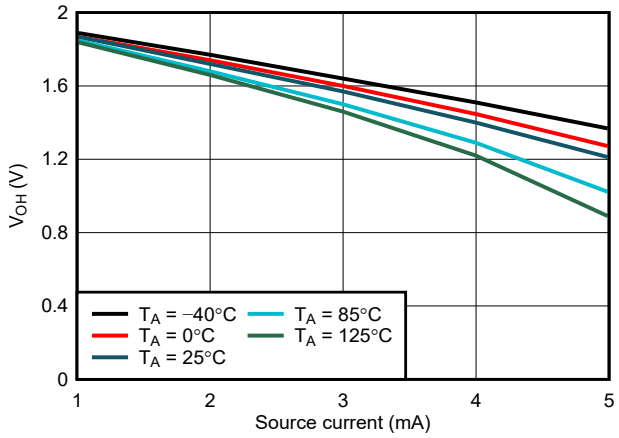


Figure 6-15. WDO V_{OH} vs I_{source}, V_{DD} = 2.0V

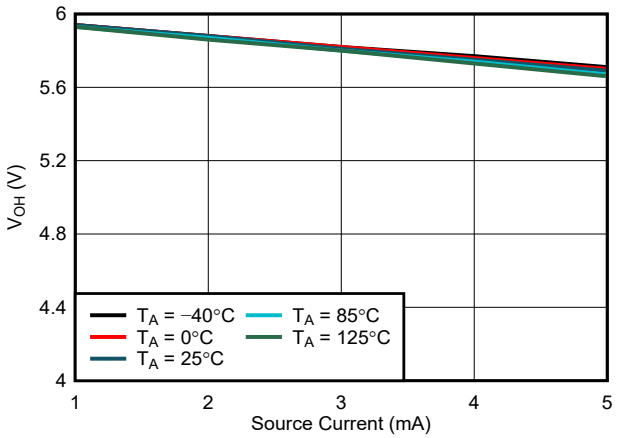


Figure 6-16. RESET V_{OH} vs I_{source}, V_{DD} = 6.0V

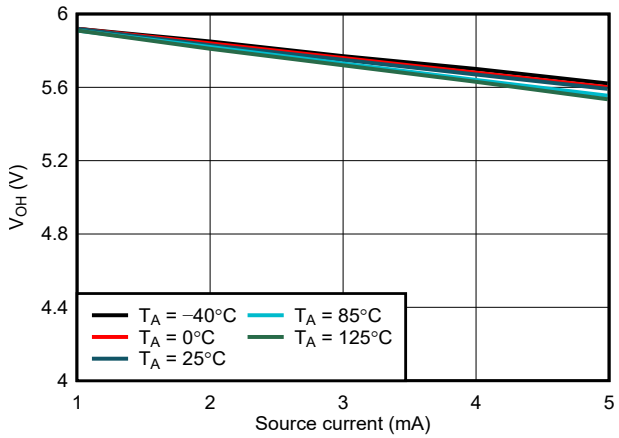


Figure 6-17. WDO V_{OH} vs I_{source}, V_{DD} = 6.0V

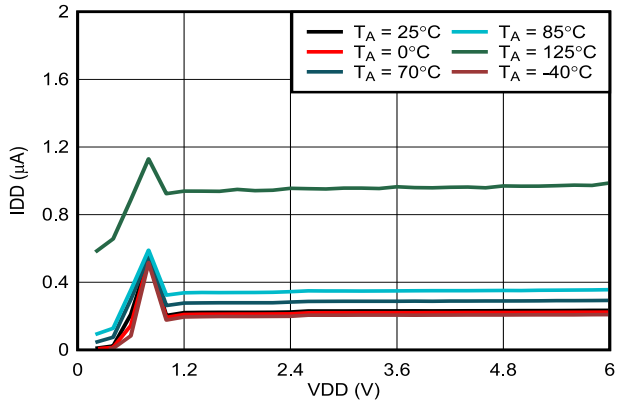


Figure 6-18. Supply Current vs Power-Supply Voltage

7 Detailed Description

7.1 Overview

The TPS35-Q1 is a high-accuracy under voltage supervisor with an integrated timeout watchdog timer device. The device family supports multiple features related to watchdog operation in a compact 8 pin SOT23 package. The devices are available in 4 different pinout configurations. Each pinout offers access to different features to meet the various application requirements. The device family is rated for AEC-Q100 applications.

7.2 Functional Block Diagrams

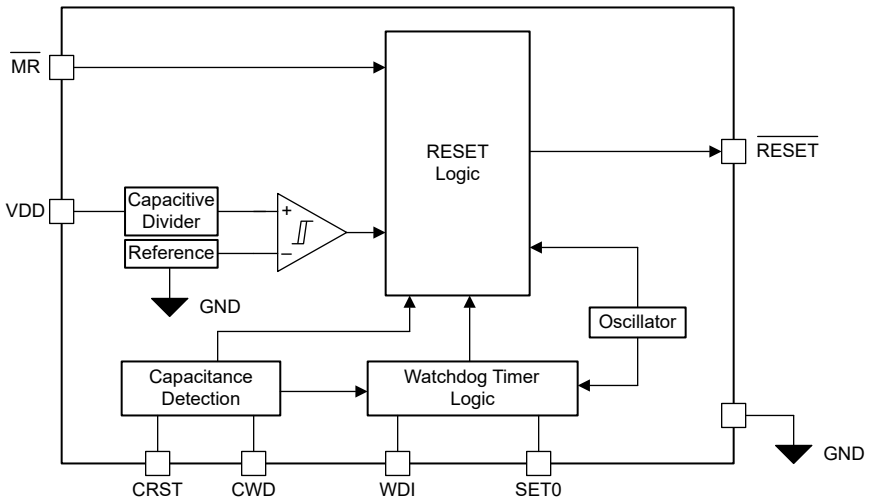


Figure 7-1. Pinout Option A

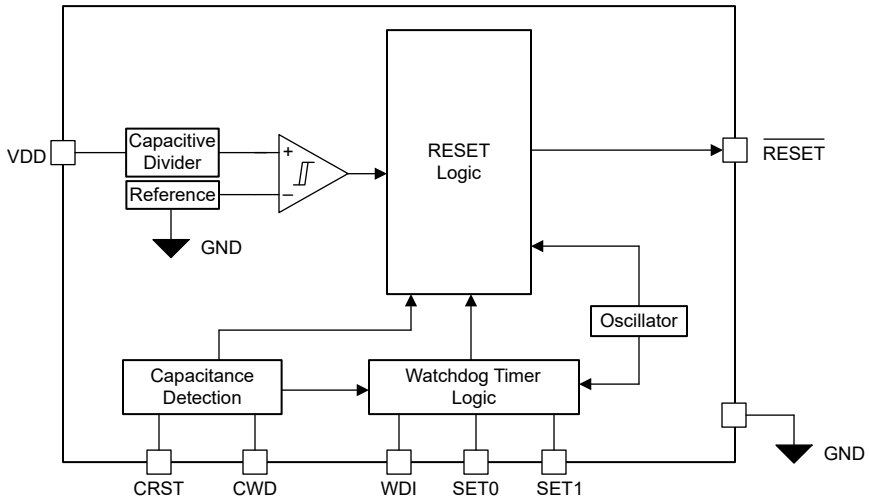


Figure 7-2. Pinout Option B

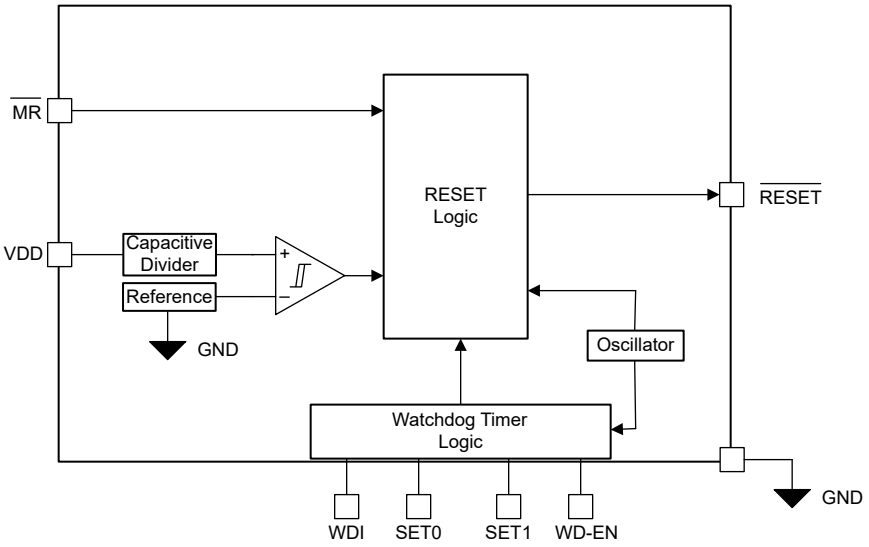


Figure 7-3. Pinout Option C

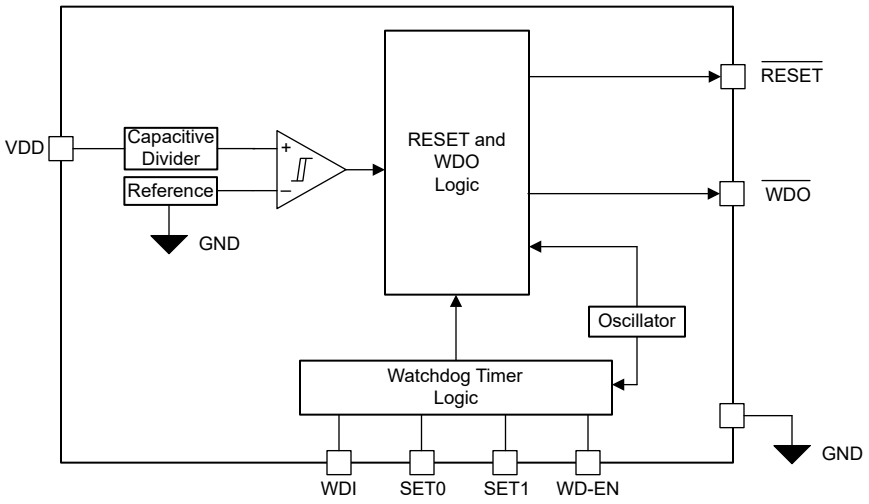


Figure 7-4. Pinout Option D

7.3 Feature Description

7.3.1 Voltage Supervisor

The TPS35-Q1 offers high accuracy under voltage supervisor function at very low quiescent current. The voltage supervisor function is always active. After the device powers up from VDD < V_{POR}, the RESET and WDO outputs are actively driven when VDD is greater than V_{POR}. The device starts monitoring the supply level when the VDD voltage is greater than 1.04V. The device holds the RESET pin asserted for t_{STRT} + t_D time after the VDD > V_{IT+} (V_{IT-} + V_{HYS}). Refer *Section 7.3.4* for the t_D value computation. For a capacitor based t_D delay option, the RESET is asserted for t_{STRT} + 2ms time if the CRST pin is open.

Device pinout options A to C offer only RESET output. In these devices the internal RESET output from supervisor and WDO output from watchdog timer are ANDed together to drive the external RESET output.

The supervisor offers wide range of fixed monitoring thresholds (V_{IT-}) from 1.05V to 5.40V in steps of 50mV. The device asserts the RESET output when the VDD signal falls below V_{IT-} threshold. The device offers hysteresis functionality for voltage supervision. This makes sure the supply has recovered above the monitoring threshold before the RESET output is deasserted. The TPS35-Q1 typical voltage hysteresis (V_{HYS}) is 5%. Along with the voltage hysteresis, the device keeps the RESET output asserted for time duration t_D after the supply has risen

above V_{IT+}. The RESET output assert duration changes from t_D to t_{STRT} + t_D if the VDD signal is ramping from voltage < V_{POR}. The t_D time duration can be programmable using an external capacitor or fixed time options offered by the device.

The typical timing behavior for a voltage supervisor and the RESET output is showcased in Figure 7-5. The voltage supervisor monitoring output has higher priority over watchdog functionality. If the device voltage supervisor output is asserted, the watchdog functionality is disabled including WDO assert control. The device resumes watchdog related functionality only after the supply is stable and the t_D time duration has elapsed.

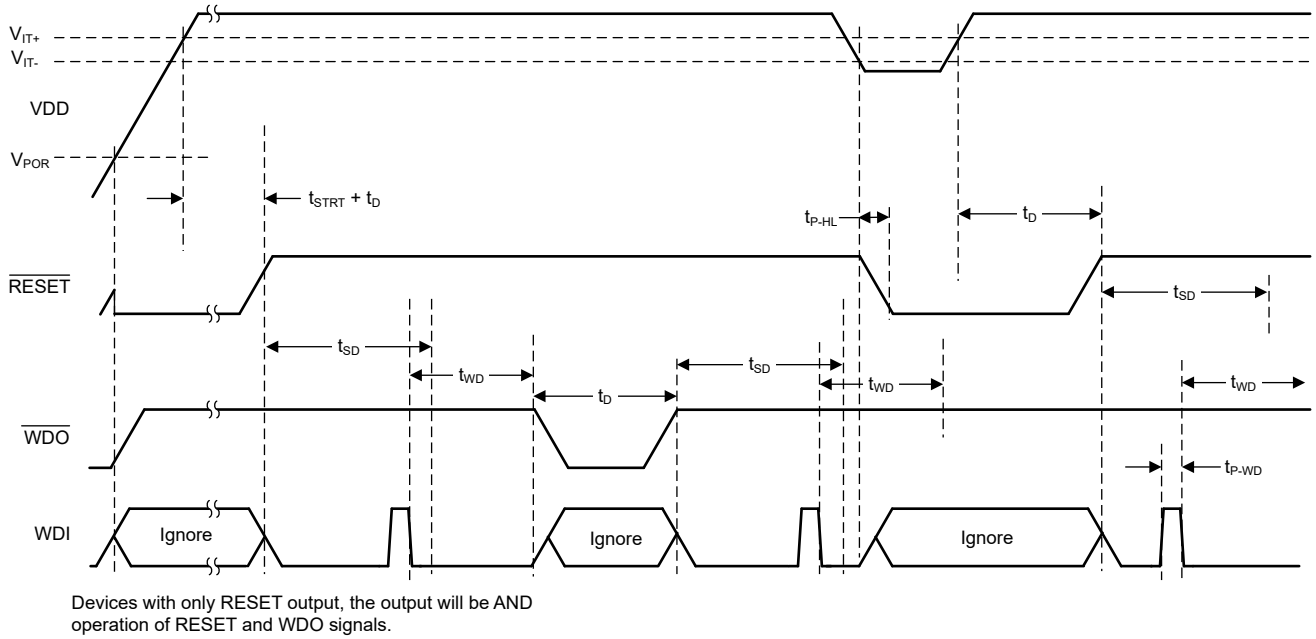


Figure 7-5. Voltage Supervisor Timing Diagram

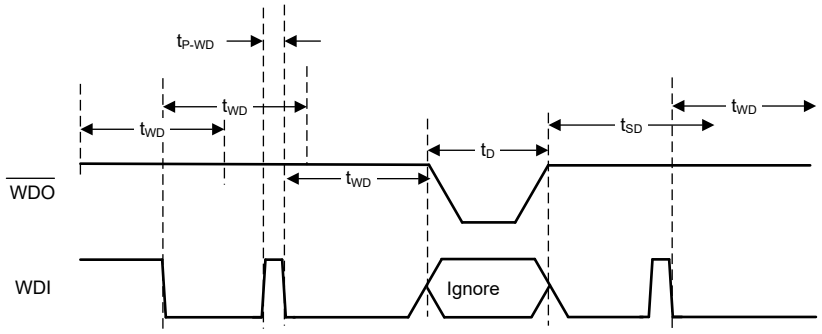
7.3.2 Timeout Watchdog Timer

The TPS35-Q1 offers high precision timeout watchdog timer monitoring. The device is available in multiple pinout options A to D which support multiple features to meet ever expanding needs of various applications. Make sure a correct pinout is selected to meet the application needs.

The timeout watchdog is active when the VDD voltage is higher than the V_{IT-} + V_{HYS} and the RESET is deasserted after the t_D time. The watchdog stays active as long as VDD > V_{IT-} and watchdog is enabled. TPS35-Q1 family offers various startup time delay options to make sure enough time is available for the host to complete boot operation. Please refer *Section 7.3.2.3* for additional details.

The timeout watchdog timer monitors the WDI pin for falling edge in the time frame defined by t_{WD} time period. Refer *Section 7.3.2.1* section to arrive at the relevant t_{WD} value needed for application. The timer value is reset when a valid falling edge is detected on WDI pin in the t_{WD} time duration. When a valid WDI transition is not detected in t_{WD} time, the device asserts RESET output for pinout options A, B and C or WDO output for pinout D. The RESET or WDO is asserted for time t_D . Refer *Section 7.3.4* to arrive at the relevant t_D value needed for application.

Figure 7-6 shows the basic operation for timeout watchdog timer operation. The TPS35-Q1 watchdog functionality supports multiple features. Details are available in following sub sections.



Devices with only RESET output, the RESET output will be asserted when watchdog error occurs.

Figure 7-6. Timeout Watchdog Timer Operation

7.3.2.1 t_{WD} Timer

The t_{WD} timer for TPS35-Q1 can be set using an external capacitor connected between CWD pin and GND pin. This feature is available with pinout options A or B. Applications which are space constrained or need timer values which meet offered timer options, can benefit when using pinout options C or D. The TPS35-Q1 offers multiple fixed timer options ranging from 1ms up-to 100s.

The TPS35-Q1, when using capacitance based timer, senses the capacitance value during the power up or after a RESET event. The capacitor is charged and discharged with known internal current source for one cycle to sense the capacitance value. The sensed value is used to arrive at t_{WD} timer for the watchdog operation. This unique implementation helps reduce the continuous charge and discharge current for the capacitor, thus reducing overall current consumption. Continuous charge and discharge of capacitance creates wider dead time (no watchdog monitor functionality) when capacitor is discharging. The dead time is higher for high value of capacitance. The unique implementation of TPS35-Q1 helps avoid the dead time as the capacitance is not continuously charging or discharging under normal operation. Make sure C_{CWD} is < 200 x C_{CRST} for accurate calibration of capacitance. Equation 1 highlights the relationship between t_{WD} in second and CWD capacitance in farad. The t_{WD} timer is 20% accurate for an ideal capacitor. Accuracy of the capacitance has additional impact on the t_{WD} time. Make sure the capacitance meets the recommended operating range. Capacitance outside the recommended range can lead to incorrect operation of the device.

$$t_{WD}\ (sec) = 4.95 \times 10^{6} \times C_{CWD}\ (F) \quad (1)$$

The TPS35-Q1 also offers wide selection of high accuracy fixed timer options starting from 1ms to 100sec including various industry standard values. The TPS35-Q1 fixed time options are ±10% accurate for t_{WD} ≥ 10ms. For t_{WD} < 10ms, the accuracy is ±20%. t_{WD} value relevant to application can be identified from the orderable part number. Refer *Section 4* section to identify mapping of orderable part number to t_{WD} value.

The TPS35-Q1 offers flexibility to change the t_{WD} value on the fly by controlling the logic levels on the SETx pins. *Section 7.3.2.4* section explains the advantages offered by this feature and the device behavior with various SETx pin combinations.

7.3.2.2 Watchdog Enable Disable Operation

The TPS35-Q1 supports watchdog enable or disable functionality. This functionality is critical for different use cases as listed below.

- Disable watchdog during firmware update to avoid host RESET.
- Disable watchdog during software step-by-step debug operation.
- Disable watchdog when performing critical task to avoid watchdog error interrupt.
- Keep watchdog disabled until host boots up.

The TPS35-Q1 supports watchdog enable or disable functionality through either WD-EN pin (pin configuration C) or SET[1:0] = 0b'01 (pin configuration B) logic combination. For a given pinout only one of these two methods is available for the user to disable watchdog operation.

For a pinout which offers a WD-EN pin, the watchdog enable disable functionality is controlled by the logic state of WD-EN pin. Drive WD-EN = 1 to enable the watchdog operation or drive WD-EN = 0 to disable the watchdog operation. The WD-EN pin can be toggled any time during the device operation. The Figure 7-7 diagram shows timing behavior with WD-EN pin control.

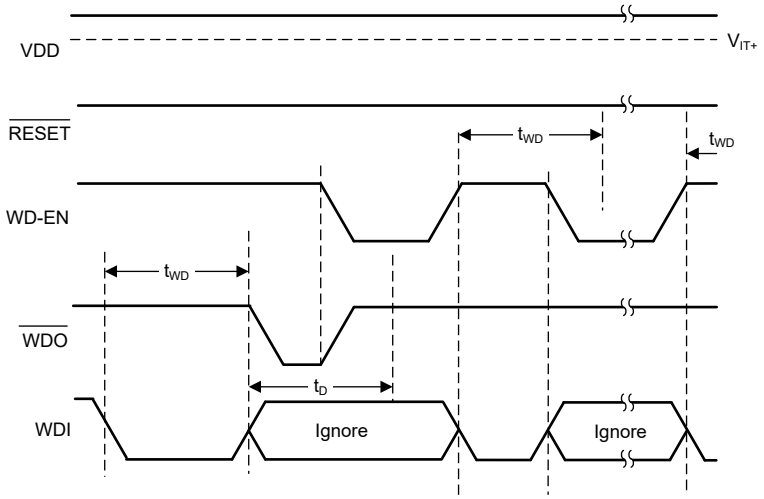


Figure 7-7. Watchdog Enable: WD-EN Pin Control

SET[1:0] = 0b'01 combination can be used to disable watchdog operation with a pinout which offers SET1 and SET0 pins, but does not include WD-EN pin. The SET pin logic states can be changed at any time during watchdog operation. Refer *Section 7.3.2.4* section for additional details regarding SET[1:0] pin behavior.

Pinout options A, B offer watchdog timer control using a capacitance connected between CWD and GND pin. A capacitance value higher than recommended or connect to GND leads to watchdog functionality getting disabled. Capacitance based disable operation overrides the other two options mentioned above. Changing capacitance on the fly does not enable or disable watchdog operation. A power supply recycle or device recovery after UV fault, $\overline{MR}$ low event is needed to detect change in capacitance.

Ongoing watchdog frame is terminated when watchdog is disabled. WDO stays deasserted when watchdog operation is disabled. For a pinout with only RESET output, the RESET can assert if supply supervisor error occurs. When enabled the device immediately enters t_{WD} frame and start watchdog monitoring operation.

7.3.2.3 t_{SD} Watchdog Start Up Delay

The TPS35-Q1 supports watchdog startup delay feature. This feature is activated after power up or after a RESET assert event or after WDO assert event. When t_{SD} frame is active, the device monitors the WDI pin but the WDO output is not asserted. This feature allows time for the host complete boot process before watchdog monitoring can take over. The start up delay helps avoid unexpected WDO or RESET assert events during boot. The t_{SD} time is predetermined based on the device part number selected. Refer *Section 4* section for details to map the part number to t_{SD} time. Pinout option A, B are available only in no delay or 10 sec start up delay options.

To exit t_{SD} frame, one of the following event must occur:

- The host provides a valid pulse transition on the WDI pin.
- Change in logic state of SET[1:0].
- Toggling of the WD_EN pin.

The device enters watchdog monitoring phase after the device exits the t_{SD} frame.

Failure to provide one of the exit condition within t_{SD} triggers the watchdog error by asserting the WDO output pin for t_D, this is observed in Figure 7-8. For devices with only RESET output, the RESET pin is asserted.

The t_{SD} frame is not initiated when the watchdog functionality is enabled using WD-EN pin or SET[1:0] pin combination as described in *Section 7.3.2.2* section.

Figure 7-8 shows the operation for t_{SD} time frame.

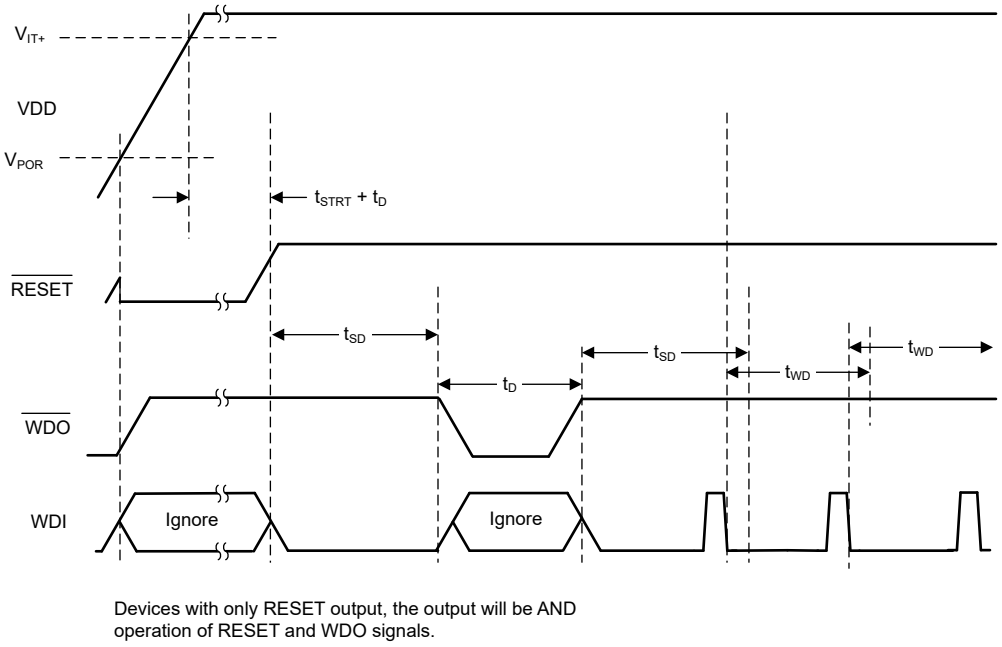


Figure 7-8. t_{SD} Frame Behavior

7.3.2.4 SET Pin Behavior

The TPS35-Q1 offers one or two SET pins based on the pinout option selected. SET pins offer flexibility to the user to program the t_{WD} timer on the fly to meet various application requirements. Typical use cases where SET pin can be used are:

- Use wide timeout timer when host is in sleep mode, change to small timeout operation when host is operational. Watchdog can be used to wake up the host after long duration to perform the application related activities before going back to sleep.
- Change to wide timeout timer when performing system critical tasks to make sure the watchdog does not interrupt the critical task. Change timer to application specified interval after the critical task is complete.

The t_{WD} timer value for the device is combination of timer selection based on the CWD pin or fixed timer value along with SET pin logic level. The base t_{WD} timer value is decided based on the Watchdog Time selector in the *Section 4* section. The SET pin logic level is decoded during the device power up. The SET pin value can be changed any time during the operation. SETx pin change which leads to change of watchdog timer value or enable disable state, terminates the ongoing watchdog frame immediately. SETx pins can be updated when WDO or RESET output is asserted as well. The updated t_{WD} timer value is going be applied after output is deasserted and the t_{SD} timer is over or terminated.

For a pinout which offers only SET0 pin to the user, the t_{WD} multiplier value is decided based on the Watchdog Time Scaling selector in the *Section 4* section. Table 7-1 showcases an example of the t_{WD} values for different SET0 logic levels when using Watchdog Time setting as option D = 10ms.

Table 7-1. t_{WD} Scaling with SET0 Pin Only (Pin Configuration A)

WATCHDOG TIME SCALING SELECTION	t_{WD}	
	SET0 = 0	SET0 = 1
A	10ms	20ms
B	10ms	40ms
C	10ms	80ms
D	10ms	160ms
E	10ms	320ms
F	10ms	640ms
G	10ms	1280ms

For pinouts which offer both SET0 & SET1 pins to the user, the t_{WD} multiplier value is decided based on the Watchdog Time Scaling selector in the *Section 4* section. Two SETx pins offer 3 different time scaling options. The SET[1:0] = 0b'01 combination disables the watchdog operation. Table 7-2 showcases an example of the t_{WD} values for different SET[1:0] logic levels when using Watchdog Time setting as option G = 100ms. The package pin out selected does not offer WD-EN pin.

Table 7-2. t_{WD} Scaling with SET0 & SET1 Pins, WD-EN Pin Not Available (Pin Configuration B)

WATCHDOG TIME SCALING SELECTION	t_{WD}			
	SET[1:0] = 0b'00	SET[1:0] = 0b'01	SET[1:0] = 0b'10	SET[1:0] = 0b'11
A	100ms	Watchdog disable	200ms	400ms
B	100ms	Watchdog disable	400ms	800ms
C	100ms	Watchdog disable	800ms	1600ms
D	100ms	Watchdog disable	1600ms	3200ms
E	100ms	Watchdog disable	3200ms	6400ms
F	100ms	Watchdog disable	6400ms	12800ms
G	100ms	Watchdog disable	12800ms	25600ms

Selected pinout option can offer WD-EN pin along with SET[1:0] pins (Pin Configuration C, D). With this pinout, the WD-EN pin controls watchdog enable and disable operation. The SET[1:0] = 0b'01 combination operates as SET[1:0] = 0b'00.

Make sure the t_{WD} value with SETx multiplier does not exceed 640s. If a selection of timer and multiplier results in t_{WD} > 640s, the timer value is restricted to 640s.

Figure 7-9 to Figure 7-11 diagrams show the timing behavior with respect to SETx status changes.

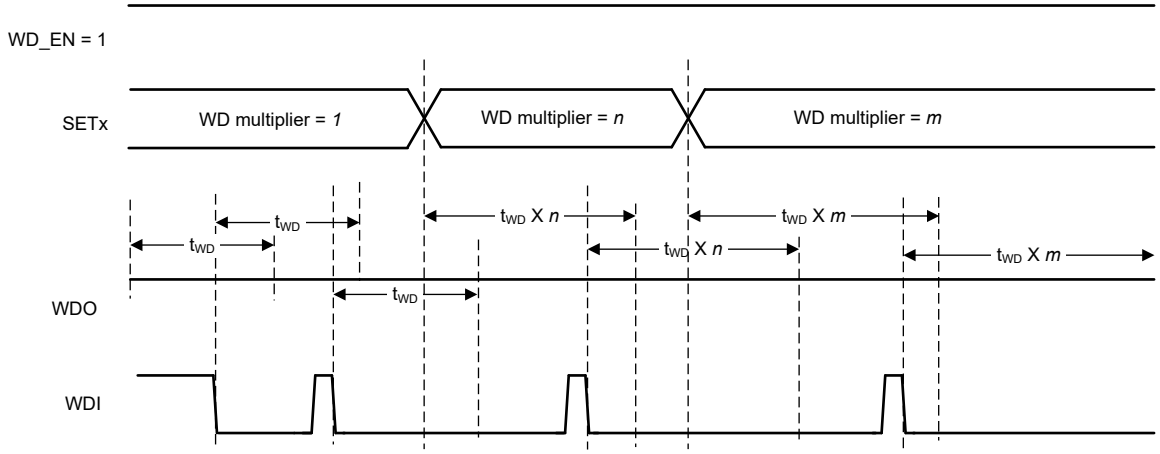
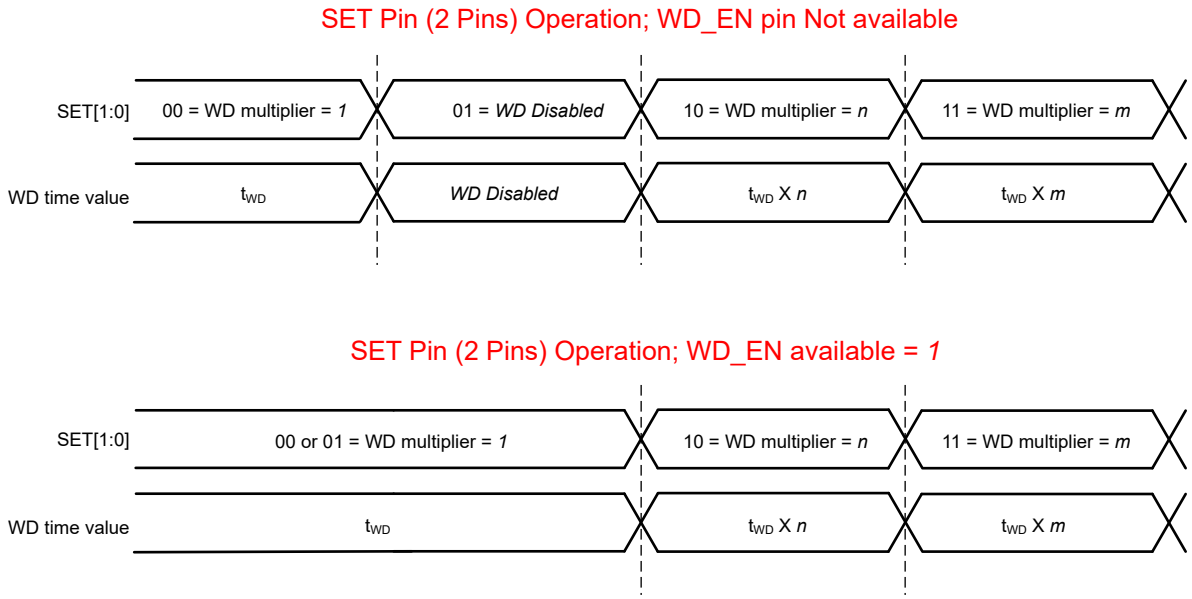
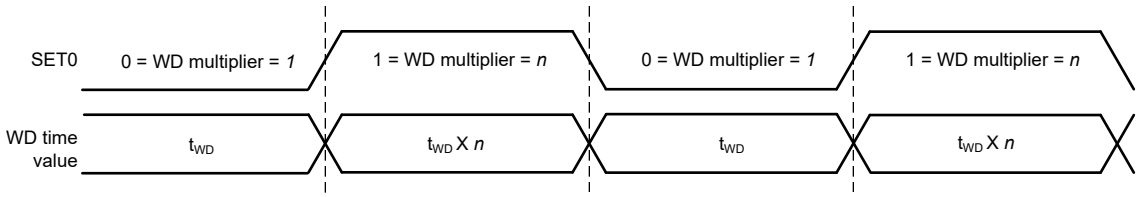


Figure 7-9. Watchdog Behavior with SETx Pin Status



t_{WD} = Fixed based on OPN or programmable using capacitor
n,m = Fixed based on timeset multiplier chosen

Figure 7-10. Watchdog Operation with 2 SET Pins



t_{WD} = Fixed based on OPN or programmable using capacitor
n = Fixed based on timeset multiplier chosen

Figure 7-11. Watchdog Operation with 1 SET Pin

7.3.3 Manual RESET

The TPS35-Q1 supports manual reset functionality using $\overline{MR}$ pin. $\overline{MR}$ pin when driven with voltage lower than 0.3 x VDD, asserts the RESET output. The $\overline{MR}$ pin has 100kΩ pull up to VDD. The $\overline{MR}$ pin can be left floating. The internal pull up makes sure the output is not asserted due to $\overline{MR}$ pin trigger.

The output is deasserted after $\overline{MR}$ pin voltage rises above 0.7 x VDD voltage and time t_D is elapsed. Refer Figure 7-12 for more details.

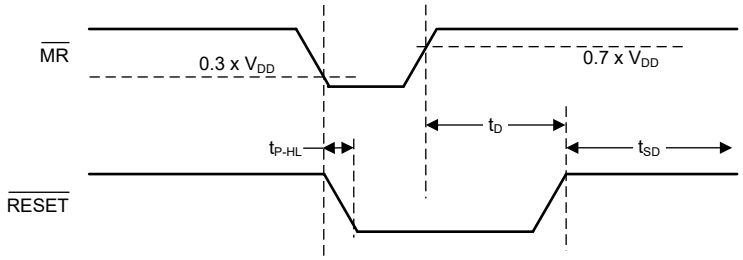


Figure 7-12. $\overline{MR}$ Pin Response

7.3.4 RESET and WDO Output

The TPS35-Q1 device can offer RESET or RESET with independent WDO output pin. The output configuration is dependent on the pinout variant selected. For a pinout which has only RESET output, the RESET output is asserted when VDD voltage is below the monitored threshold or $\overline{MR}$ pin voltage is lower than threshold or watchdog timer error is detected. For a pinout which has independent RESET and WDO output pins, the RESET output is asserted when VDD voltage is below the monitored threshold or $\overline{MR}$ pin voltage is lower than threshold. WDO output is asserted only when watchdog timer error is detected. RESET error has higher priority than WDO error. If RESET is asserted when WDO is asserted, the device deasserts the WDO pin and watchdog is disabled until RESET pin is deasserted and startup delay frame is terminated.

The output is asserted for t_D time when any relevant events described above are detected. The time t_D can be programmed by connecting a capacitor between CRST pin and GND or the device asserts t_D for fixed time duration as selected by orderable part number. Refer *Section 4* section for all available options.

Equation 2 describes the relationship between capacitor value and the time t_D . Make sure the capacitance meets the recommended operating range. Capacitance outside the recommended range can lead to incorrect operation of the device.

$$t_D\,(\text{sec}) = 4.95 \times 10^6 \times C_{CRST}\,(\text{F}) \quad (2)$$

TPS35-Q1 also offers a unique option of latched output. An orderable with latched output holds the output in asserted state indefinitely until the device is power cycled or the error condition is addressed. If the output is latched due to voltage supervisor undervoltage detection, the output latch is released when VDD voltage rises above the $V_{IT-} + V_{HYS}$ level. If the output is latched due to $\overline{MR}$ pin low voltage, the output latch is released when $\overline{MR}$ pin voltage rises above 0.7 x V_{DD} level. If the output is latched due to watchdog timer error, the output latch is be released when a WDI negative edge is detected or the device is shutdown and powered up again. Figure 7-13 shows timing behavior of the device with latched output configuration.

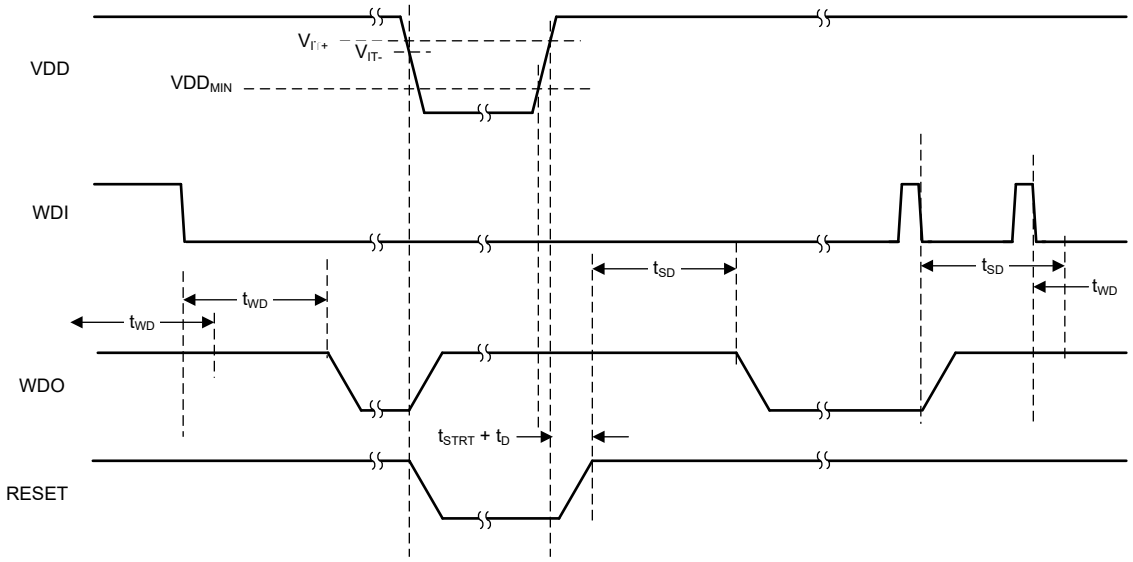


Figure 7-13. Output Latch Timing Behavior

7.4 Device Functional Modes

Table 7-3 summarizes the functional modes of the TPS35-Q1.

Table 7-3. Device Functional Modes

VDD	WATCHDOG STATUS	WDI	$\overline{\text{WDO}}$	$\overline{\text{RESET}}$
$V_{DD} < V_{POR}$	Not Applicable	—	Undefined	Undefined
$V_{POR} \le V_{DD} < V_{IT-}$	Not Applicable	Ignored	High	Low
$V_{DD} \ge V_{IT+}$	Disabled	Ignored	High	High
	Enabled	t_{pulse} [1] < $t_{WD(min)}$	High	High
	Enabled	t_{pulse} [1] > $t_{WD(max)}$	Low	High

(1) Where t_{pulse} is the time between falling edges on WDI.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following sections describe in detail proper device implementation, depending on the final application requirements.

8.1.1 CRST Delay

The TPS35-Q1 features two options for setting the reset delay (t_D): using a fixed timing and programming the timing through an external capacitor.

8.1.1.1 Factory-Programmed watchdog Timing

Fixed watchdog timings are available using pinout C and D. Using these timings enables a high-precision, 10% accurate watchdog timer t_{WD}.

8.1.1.2 Adjustable Capacitor Timing

The TPS35-Q1 also offers programmable reset delay option when using pinout A and B. The TPS35-Q1 can be programmed to have a desired reset delay by connecting a capacitor between CRST pin and GND. The typical delay time resulting from a given external capacitance on the CRST pin can be calculated by Equation 3 , where t_D is the reset delay time in seconds and C_{CRST} is the capacitance in farads.

$$t_D \text{ (sec)} = 4.95 \times 10^6 \times C_{CRST} \text{ (F)} \quad (3)$$

To minimize the difference between the calculated reset delay time and the actual reset delay time, use a use a high-quality ceramic dielectric COG capacitor and minimize parasitic board capacitance around this pin. Table 8-1 lists the reset delay time ideal capacitor values for C_{CRST}.

Table 8-1. Reset Delay Time for Common Ideal Capacitor Values

C_{CRST}	RESET DELAY TIME (t_D)			UNIT
	MIN (1)	TYP	MAX (1)	
10nF	39.6	49.5	59.4	ms
100nF	396	495	594	ms
1µF	3960	4950	5940	ms

(1) Minimum and maximum values are calculated using ideal capacitors.

8.1.2 Watchdog Timer Functionality

The TPS35-Q1 features two options for setting the watchdog timer (t_{WD}): using a fixed timing and programming the timing through an external capacitor.

8.1.2.1 Factory-Programmed watchdog Timing

Fixed watchdog timings are available using pinout C and D. Using these timings enables a high-precision, 10% accurate watchdog timer t_{WD}.

8.1.2.2 Adjustable Capacitor Timings

Adjustable t_{WD} timing is achievable by connecting a capacitor to the CWD pin. If this method is used, please consult Equation 1 for calculating typical t_{WD} values using ideal capacitors. Capacitor tolerances cause the

actual device timing to vary such that the minimum of t_{WD} can decrease and the maximum of t_{WD} can increase by the capacitor tolerance. For the most accurate timing, use ceramic capacitors with COG dielectric material.

8.2 Typical Applications

8.2.1 Design 1: Monitoring a Microcontroller Supply Voltage and Watchdog Timer

The TPS35-Q1 features high-accuracy (1.2% maximum) voltage supervising along with on-the-fly adjustable watchdog timing to monitor critical processing elements in systems.

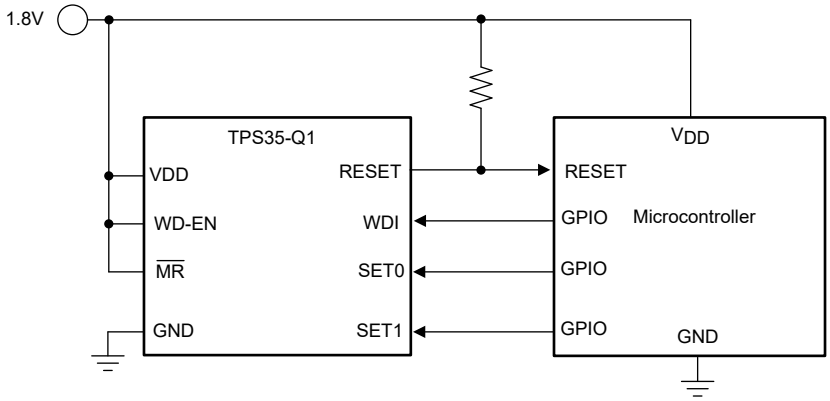


Figure 8-1. Microcontroller Supply and Watchdog Monitoring Circuit

8.2.1.1 Design Requirements

Table 8-2. Design Parameters

PARAMETER	DESIRED REQUIREMENT	DESIGN RESULT
Threshold Voltage	Typical threshold voltage of 1.65V	Typical threshold voltage of 1.65V
Watchdog Timeout Period	Typical timeout period of 1.6s	Typical timeout period of 1.6s
RESET Delay	Typical reset delay of 200ms	Typical reset delay of 200ms
Startup Delay	Minimum startup delay of 700ms	Minimum startup delay of 900ms
Output Logic	Open-drain	Open-drain
Maximum Device Current Consumption	20µA	250nA typical, 3µA maximum

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Setting the Voltage Threshold

The negative-going threshold voltage, V_{IT-}, is set by the device variant. Equation 4 shows how to calculate the "Threshold Voltage" section of the orderable part number.

$$\text{OPN "Threshold Voltage" number} = (V_{IT-} - 1) / 0.05 \quad (4)$$

In this example, the nominal supply voltage for the microcontroller is 1.8V. The minimum supply voltage is 10% lower than the nominal supply voltage, or 1.62V. Setting a 1.65V threshold makes sure that the device resets just before the supply voltage reaches the minimum allowed. Thus a 1.65V threshold is chosen and, using Equation 4, the part number is reduced to TPS35xx13xxxxxxxQ1. Since the hysteresis is 5% typical, the positive-going threshold voltage, V_{IT+}, is 1.73V.

8.2.1.2.2 Meeting the Watchdog Timeout Period

The watchdog timeout design requirement can be met either by using a fixed-timeout version of the TPS35-Q1 or by connecting a capacitor between the CWD pin and GND. The typical values can be met with preprogrammed fixed time options, hence a pinout offering fixed time options is selected. Please see the Timing Requirements for a list of fixed timeouts. If using the CWD feature, pinout A or B must be used; please refer to t_{WD} Timer for instructions on how to program the timout period. The design requirement in this example is t_{WD} = 1.6s. This is one of the fixed timeout options offered by pinout C or D. Thus the possible variant option is narrowed down to TPS35Cx13KAxDDFRQ1.

8.2.1.2.3 Setting the Reset Delay

The reset delay requirement can be met either by using a fixed-timeout version of the TPS35-Q1 or by connecting a capacitor between the CRST pin and GND. The typical values can be met with preprogrammed fixed time options, hence a pinout offering fixed time options is selected. Please see the Timing Requirements for a list of fixed timeouts. If using the CRST feature, pinout A or B must be used; please refer to the Timing Specifications for instructions on how to program the timout period. The design requirement in this example is t_D = 200ms. Thus the possible variant option is narrowed down to TPS35Cx13KAGDDFRQ1.

8.2.1.2.4 Setting the Startup Delay and Output Topology

The startup delay and output topology are set by the device variant. Please refer to Device Comparison for the possible options. A minimum startup delay of 700ms and open-drain output are desired, thus Option D, 1s typical startup delay and open-drain active-low, is selected. Thus the option suitable to meet design requirements is TPS35CD13KAGDDFRQ1.

8.2.1.2.5 Calculating the RESET Pullup Resistor

The TPS35-Q1 uses an open-drain configuration for the $\overline{\text{RESET}}$ output, as shown in Figure 8-2. When the FET is off, the resistor pulls the drain of the transistor to VDD and when the FET is turned on, the FET pulls the output to ground, thus creating an effective resistor divider. The resistors in this divider must be chosen to make sure that V_{OL} is below the maximum value. To choose the proper pullup resistor, there are three key specifications to keep in mind: the pullup voltage (V_{PU}), the recommended maximum $\overline{\text{RESET}}$ pin current (I_{RST}), and V_{OL}. The maximum V_{OL} is 0.3V, meaning that the effective resistor divider created must be able to bring the voltage on the reset pin below 0.3V with I_{RST} kept below 2mA for V_{DD} ≥ 3V and 500µA for V_{DD} = 1.5V. For this example, with a V_{PU} =V_{DD} = 1.5V, a resistor must be chosen to keep I_{RST} below 500µA because this value is the maximum consumption current allowed. To make sure this specification is met, a pullup resistor value of 10kΩ was selected, which sinks a maximum of 180µA when $\overline{\text{RESET}}$ is asserted.

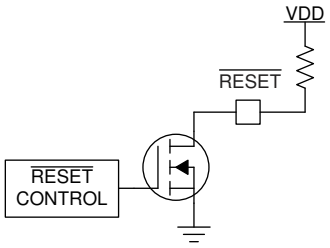


Figure 8-2. Open-Drain $\overline{\text{RESET}}$ Configuration

8.2.1.3 Application Curves

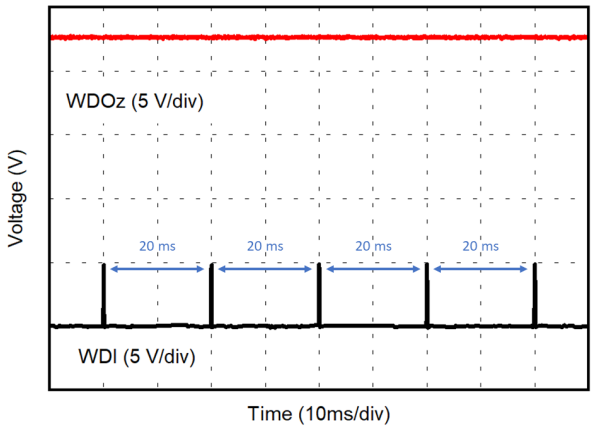


Figure 8-3. Typical WDI Pulse

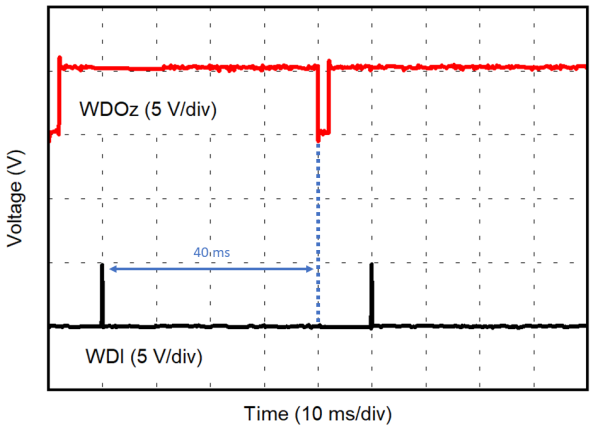


Figure 8-4. Watchdog Timeout Fault

8.3 Power Supply Recommendations

This device is designed to operate from an input supply with a voltage range between 1.04V and 6V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1µF capacitor between the VDD pin and the GND pin.

8.4 Layout

8.4.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a 0.1µF ceramic capacitor as near as possible to the VDD pin. If a capacitor is not connected to the CRST pin, then minimize parasitic capacitance on this pin so the $\overline{\text{RESET}}$ delay time is not adversely affected.

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1µF ceramic capacitor as near as possible to the VDD pin.
- Place C_{CRST} capacitor as close as possible to the CRST pin.
- Place C_{CWD} capacitor as close as possible to the CWD pin.
- Place the pullup resistor on the $\overline{\text{RESET}}$ pin as close to the pin as possible.

8.4.2 Layout Example

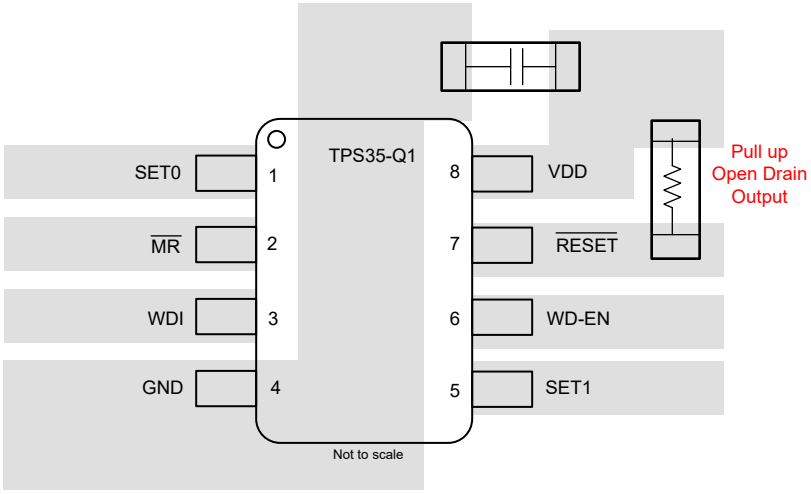


Figure 8-5. Typical Layout for the Pinout C of TPS35-Q1

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

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All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2023) to Revision B (August 2024)	Page
• Added available device part table	3
• Added t_{SD} exit condition	20

Changes from Revision * (November 2022) to Revision A (June 2023)	Page
• Advance Information to Production Data release	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS35AA38AGADDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NLHOE
TPS35AA38AGADDFRQ1.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NLHOE
TPS35AA39AGADDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NLHOW
TPS35AA39AGADDFRQ1.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NLHOW
TPS35BA38AAADDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NLHOX
TPS35CA38GACDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NLHON
TPS35CA38GACDDFRQ1.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NLHON
TPS35CA38IABDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ANLHO
TPS35CA38IAGDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NLHO6
TPS35CA43DACDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NLHOC
TPS35CA43DACDDFRQ1.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NLHOC
TPS35DA69GADDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NLHOT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS35-Q1 :

- Catalog : TPS35

NOTE: Qualified Version Definitions:

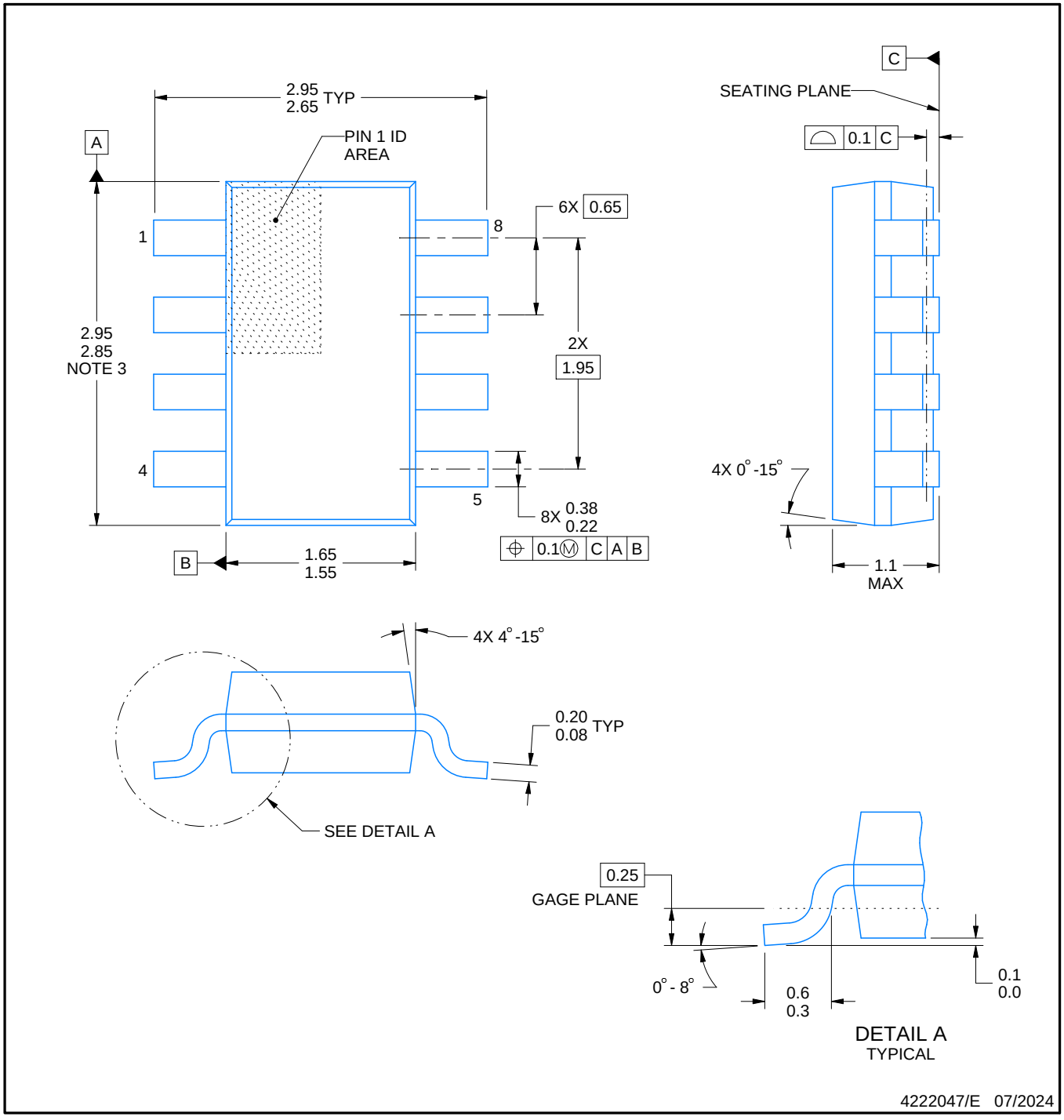
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

DDF0008A

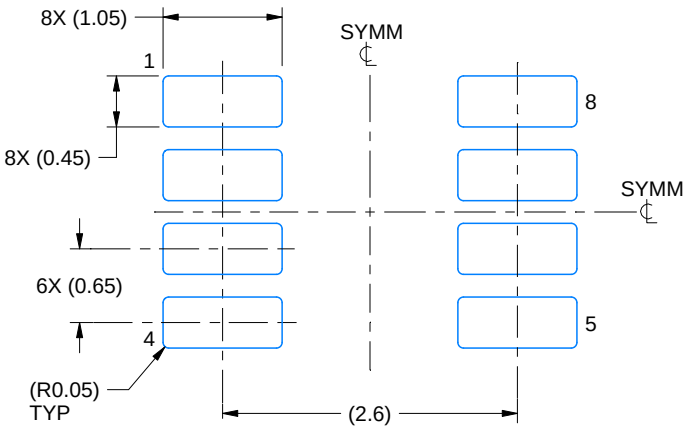
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

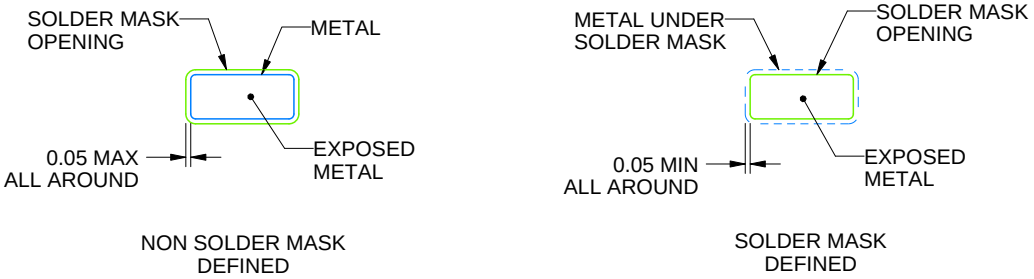


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

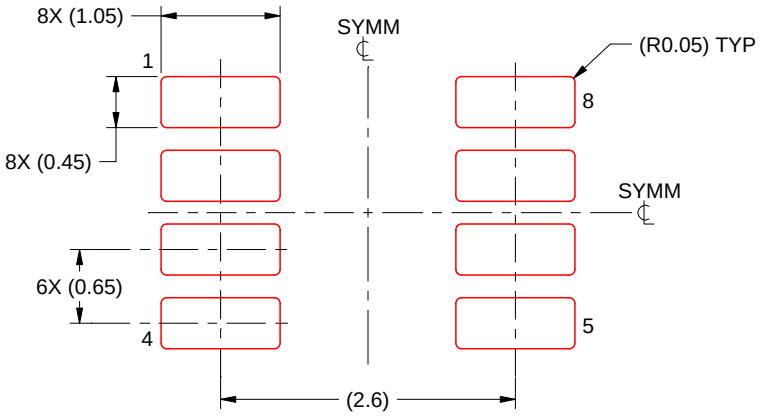
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025