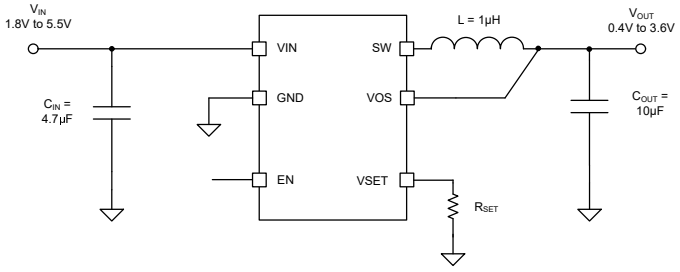
TPS62843 1.8V to 5.5V, 600mA, 275nA I_Q, Small-Size Step-Down Converters

1 Features

- 1.8V to 5.5V input voltage range
- 0.4V to 3.6V output voltage range
- 275nA typical quiescent current
- 600mA output current
- 1% output voltage accuracy
- 4nA typical shutdown current
- Output discharge
- VSET pin-selectable output voltage through a single resistor
  - TPS628436: 0.4V to 0.8V
  - TPS628437: 0.8V to 1.8V
  - TPS628438: 1.8V to 3.6V
- Designed for small passive components
  - 1µH inductor
  - Down to effective capacitance of 4µF C_{OUT}
- High PSRR (up to 83dB)
- Low output voltage ripple in power save mode
- RF-friendly and fast transient DCS-Control
- Automatic transition to no ripple 100% mode
- 0603-inductor and 0402-capacitor size supported
- Tiny 6-pin, 0.35mm pitch WCSP package with 0.84mm² size
- Pin-to-pin compatible to the TPS6280x family (1A) in WCSP package
- Available in a 1.60mm × 1.60mm SOT563 package

2 Applications

- Wearable electronics
- Headsets, headphones, and earbuds
- Mobile phones
- Medical sensor patches
- Hearing aid



Typical Application

3 Description

The TPS62843 is a high-efficiency, step-down converter family with ultra-low operating quiescent current of typically 275nA. The device features a 4nA shutdown (typical) current when disabled.

The device uses DCS-Control with a low and RF-friendly output voltage ripple to power radios.

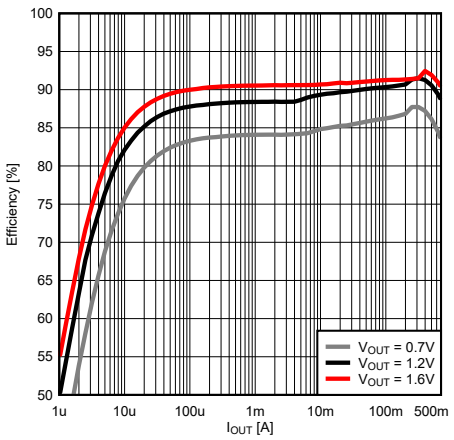
The device operates with a typical switching frequency of 1.5MHz and extends a high efficiency at light-load down to 100µA load current and below.

3 × 18 pre-defined output voltages can be selected by connecting a resistor to the VSET pin, making the family usable across various applications with a minimum set of passive components.

Device Information

PART NUMBER(2)	V_{OUT} RANGE	PACKAGE(1)	BODY SIZE (NOM)
TPS628436	0.4V – 0.8V	YKA (DSBGA, 6)	0.80mm × 1.05mm × 0.40mm
TPS628437	0.8V – 1.8V		
TPS628438	1.8V – 3.6V		
TPS628436	0.4V – 0.8V	DRL (SOT563, 6)	1.6mm × 1.6mm × 0.6mm
TPS628437	0.8V – 1.8V		
TPS628438	1.8V – 3.6V		

(1) For more information, see Section 11.
(2) See the *Device Comparison Table*.



Efficiency vs Output Current at 3.6V_{IN}

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4 Device Comparison Table

Device	Fixed V_{OUT} VSET = GND	Selectable Output Voltages	f_{SW} [MHz]	Soft Start t_{SS}	Inductor
TPS628436	1.0V	0.4V – 0.8V in 25mV steps	1.5	400µs	1µH
TPS628437	1.8V	0.8V – 1.6V in 50mV steps	1.5	800µs	1µH
TPS628438	3.6V	1.8V – 3.4V in 100mV steps	1.5	800µs	1µH

5 Pin Configuration and Functions

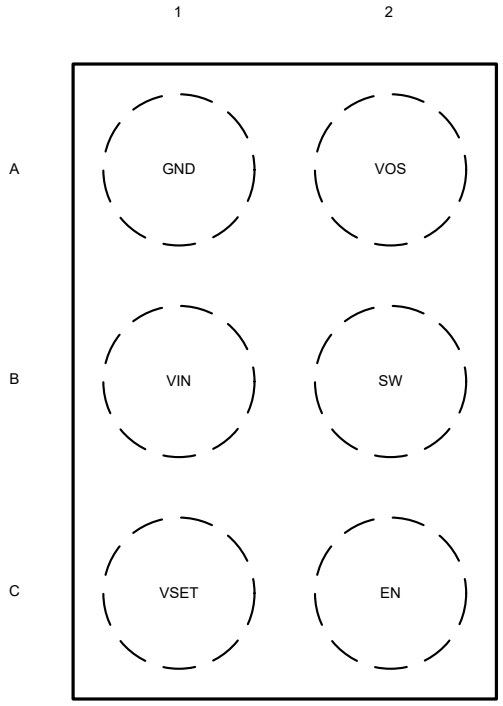


Figure 5-1. 6-Pin DSBGA YKA Package (Top View)

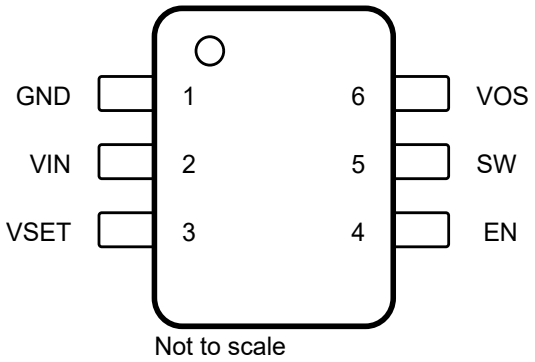


Figure 5-2. 6-Pin DRL SOT563 Package (Top View)

Table 5-1. Pin Functions

PIN NUMBER			TYPE	DESCRIPTION
NAME	SOT563	DSBGA		
GND	1	A1	PWR	GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor.
VIN	2	B1	PWR	V_{IN} power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A ceramic capacitor is required.
VSET	3	C1	I	Connecting a resistor to GND selects a pre-defined output voltage.
VOS	6	A2	I	Output voltage sense pin for the internal feedback divider network and regulation loop. This pin also discharges V_{OUT} by an internal MOSFET when the converter is disabled. Connect this pin directly to the output capacitor with a short trace.
SW	5	B2	O	The switch pin is connected to the internal MOSFET switches. Connect the inductor to this terminal.
EN	4	C2	I	A high level enables the devices and a low level turns the device off. The pin features an internal pulldown resistor, which is disabled once the device has started up.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	VIN	-0.3	6	V
Pin voltage	SW, DC	-0.3	V_{IN}+0.3V	V
Pin voltage	SW, transient < 10 ns, while switching	-2.5	9	V
Pin voltage	VSET	-0.3	6	V
Pin voltage	EN	-0.3	6	V
Pin voltage	VOS	-0.3	5	V
T_J	Operating junction temperature	-40	150	°C
T_{stg}	Storage temperature	-55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage V_{IN}	1.8		5.5	V
I_{OUT}	Output current			0.6	A
L	Effective inductance	0.7	1.0	1.2	µH
C_{OUT}	Effective output capacitance	4		25	µF
C_{IN}	Effective input capacitance	0.5	4.7		µF
C_{VSET}	External parasitic capacitance at VSET pin			30	pF
R_{SET}	Resistance range for external resistor at VSET pin (E96 1% resistor values)	10		249	kΩ
	External resistor tolerance E96 series at VSET pin			1%	
	E96 resistor series temperature coefficient (TCR)	-200		+200	ppm/°C
T_J	Operating junction temperature range	-40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		YKA (DSBGA) 6 PINS	DRL (SOT563) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	147.7	138.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.7	57.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.5	24.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.6	24.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

T_J = –40°C to +125°C, V_{IN} = 1.8V to 5.5V. Typical values are at T_J = 25°C, V_{IN} = 3.6V and V_{OUT} = 0.7V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Operating Quiescent Current (Power Save Mode)	Non-switching, V_{EN} = V_{IN}, I_{OUT} = 0µA, T_J = -40°C to 85°C		275	1500	nA
		Switching, V_{EN} = V_{IN}, I_{OUT} = 0µA, V_{OUT} = 0.7V		350		nA
I_{SD}	Shutdown Current	V_{EN} = 0V, VSET = GND, T_J = -40°C to 85°C		4	850	nA
UVLO						
$V_{UVLO(R)}$	Undervoltage Lockout Rising Threshold	V_{IN} rising, I_{OUT} = 0µA		1.75	1.8	V
$V_{UVLO(F)}$	Undervoltage Lockout Falling Threshold	V_{IN} falling, I_{OUT} = 0µA		1.65	1.7	V
$V_{UVLO(H)}$	Undervoltage Lockout Hysteresis			100		mV
VSET PIN						
$V_{SET(LKG)}$	VSET Input leakage current	T_J = -40°C to 85°C		10	800	nA
$V_{SET(H)}$	VSET High-level detection	Voltage at VSET during startup	1.0			V
R_{SET}	RSET accuracy	T_J = -20°C to 125°C	-4		4	%
R_{SET}	RSET accuracy	T_J = -40°C to 125°C	-3.5		3.5	%
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	0.8			V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching			0.4	V
$V_{EN(LKG)}$	EN Input leakage current	V_{EN} > 0.8V, T_J = -40°C to 85°C		1	25	nA
$R_{EN;PD}$	EN internal pull-down resistance	EN pin to GND	425	500		kΩ
VOUT VOLTAGE						
V_{OUT}	DC Output voltage accuracy	PWM operation, T_J = -20°C to 125°C	-1		+1	%
V_{OUT}	DC Output voltage accuracy	PWM operation, T_J = -40°C to 125°C	-1.5		+1.5	%
V_{OUT}	TPS628436		0.4		0.8	V
	TPS628437		0.8		1.8	V
	TPS628438		1.8		3.6	V
$I_{VOS(LKG)}$	VOS input leakage current	TPS628436, V_{EN} = V_{IN}, V_{VOS} = 0.7V, T_J = -40°C to 85°C			100	nA
		TPS628437, V_{EN} = V_{IN}, V_{VOS} = 1.2V, T_J = -40°C to 85°C		100	250	nA
		TPS628438, V_{EN} = V_{IN}, V_{VOS} = 3.3V, T_J = -40°C to 85°C		275	450	nA
f_{SW}		I_{OUT} = 400mA		1.5		MHz
STARTUP						

6.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C, V_{IN} = 1.8V to 5.5V. Typical values are at T_J = 25°C, V_{IN} = 3.6V and V_{OUT} = 0.7V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SS}	TPS628436 soft-start time	From V_{OUT}= 0% to V_{OUT}= 95% of V_{OUT} nominal		0.45	0.6	ms
	TPS628438 soft-start time			1.0	1.4	
	TPS628437 soft-start time			0.7	1.0	
$t_{Startup\_delay}$	EN HIGH to start of switching delay	R2D = GND		330	560	µs
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	V_{IN} = 3.6V, I_{OUT} = 300mA		170	260	mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	V_{IN} = 3.6V, I_{OUT} = 300mA		70	115	mΩ
I_{LKG_SW}	Leakage Current into SW-Pin	V_{SW} = 0.7V, T_J = -40°C to 85°C		0	35	nA
I_{LKG_SW}	Leakage Current into SW-Pin	V_{SW} = 1.2V, T_J = -40°C to 85°C		0	45	nA
I_{LKG_SW}	Leakage Current into SW-Pin	$V_{VIN} > V_{SW}$, V_{SW} = 3.3V, T_J = -40°C to 85°C		0	45	nA
OVERCURRENT PROTECTION						
$I_{HS(OC)}$	High-side peak current limit	$V_{IN} \geqq$ 2.2V	0.9	1.1	1.3	A
$I_{LS(OC)}$	Low-side valley current limit	$V_{IN} \geqq$ 2.2V	0.79	1.0	1.11	A
OUTPUT DISCHARGE						
R_{DSCH_VOS}	Output discharge resistor on VOS pin	V_{EN} = GND, I(VOS) = -10mA		7	22	Ω
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold	Temperature rising		160		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis			20		°C

6.6 Typical Characteristics

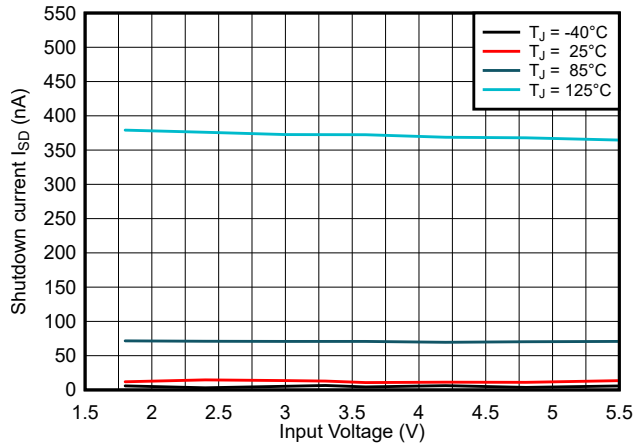


Figure 6-1. Shutdown Current I_{SD}

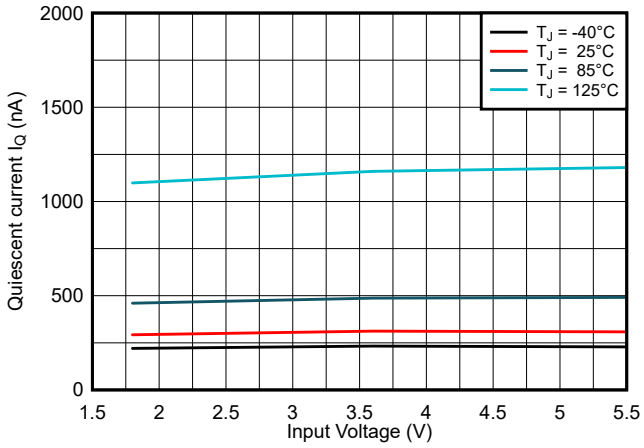


Figure 6-2. Quiescent Current I_Q

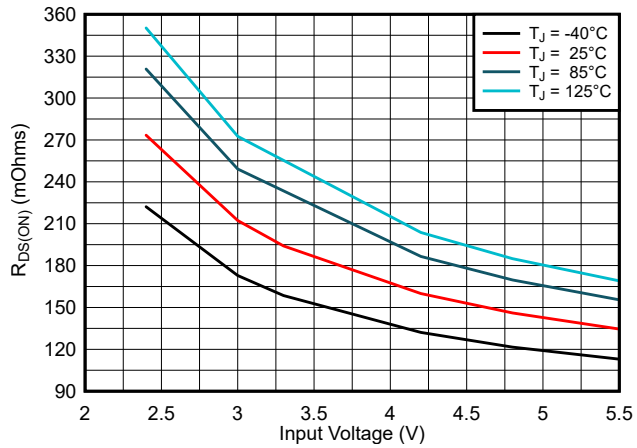


Figure 6-3. High Side Switch Drain Source Resistance $R_{DS(ON)}$

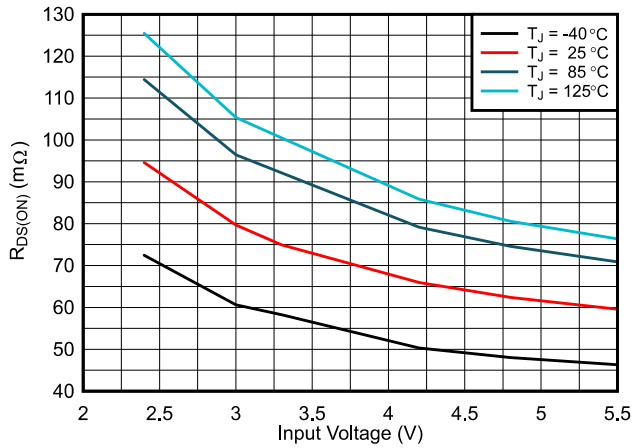


Figure 6-4. Low Side Switch Drain Source Resistance $R_{DS(ON)}$

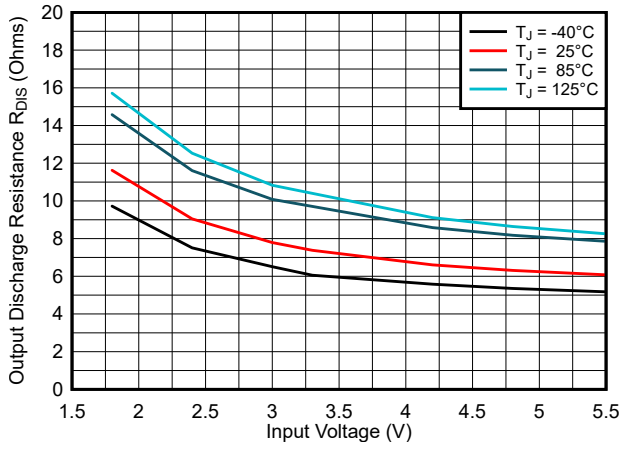


Figure 6-5. VOS Discharge Switch Drain Source Resistance R_{DIS}

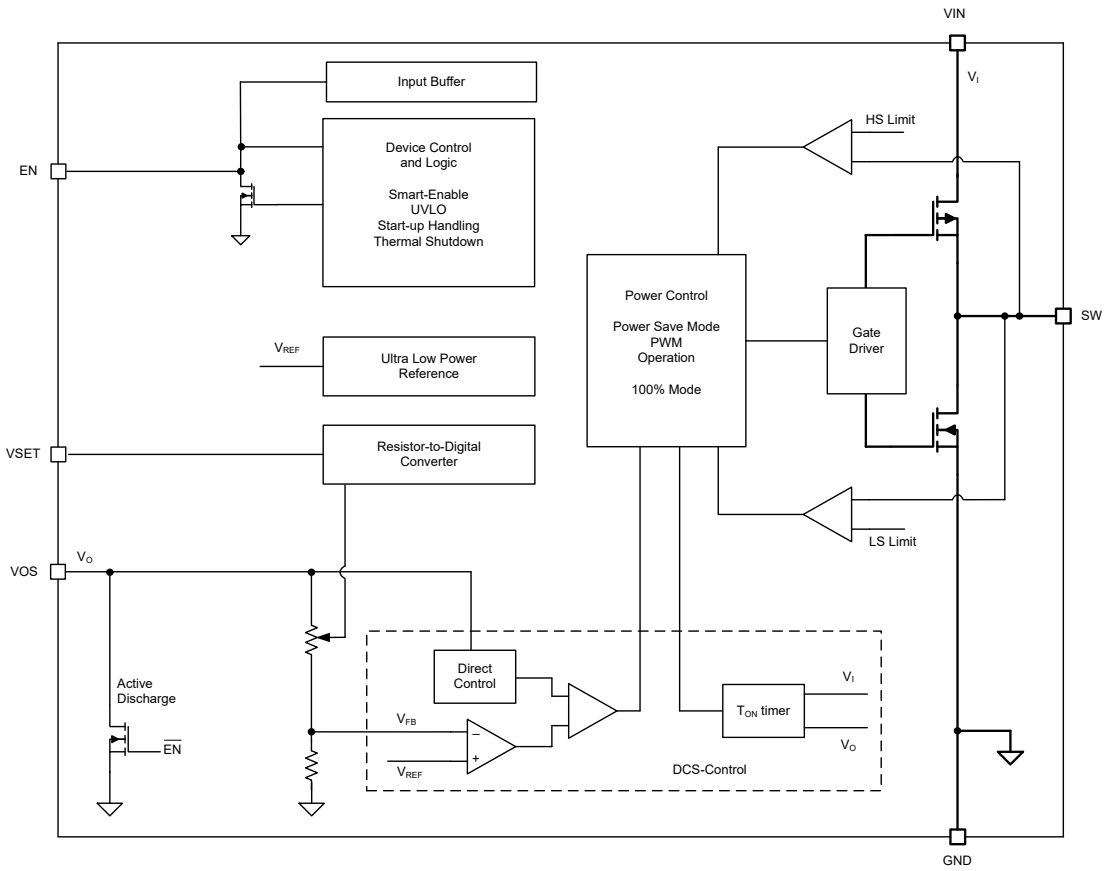
7 Detailed Description

7.1 Overview

The TPS62843 is a high-frequency, synchronous step-down converter with ultra-low quiescent current of typically 275nA in a 0.84-mm² chip size. The device operates with a tiny 1-µH inductor and 10-µF output capacitor over the entire recommended operation range to provide one of the industry's smallest chip and solution size.

Using TI's DCS-Control topology, the device extends the high efficiency operation area down to microamperes of load current during power save mode operation. TI's DCS-Control (Direct Control with Seamless Transition into power save mode) is an advanced regulation topology that combines the advantages of hysteretic and voltage mode control. Characteristics of DCS-Control are excellent AC load regulation and transient response, low output ripple voltage, and a seamless transition between PFM and PWM mode operation. DCS-Control includes an AC loop that senses the output voltage (VOS pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Smart Enable and Shutdown (EN)

An internal 500kΩ resistor pulls the EN pin to GND and avoids floating the pin. This action prevents an uncontrolled start-up of the device in case the EN pin cannot be driven to low level safely. With EN low, the device is in shutdown mode. The device is turned on with EN set to a high level. The pulldown control circuit disconnects the pulldown resistor on the EN pin after the internal control logic and the reference have been powered up. With EN set to a low level, the device enters shutdown mode and the pulldown resistor is activated again. The high level of the EN pin must not exceed VIN voltage level.

7.3.2 Soft Start

After the device has been enabled with EN high, the device initializes and powers up the internal circuits. This action occurs during the regulator start-up delay time, $t_{Startup\_delay}$. After $t_{Startup\_delay}$ expires, the internal soft-start circuitry ramps up the output voltage within the soft-start time, t_{ss}. See Figure 7-1.

The start-up delay time, $t_{Startup\_delay}$, varies depending on the selected VSET value. The start-up delay is shortest with VSET = 0 and longest with VSET = 16.

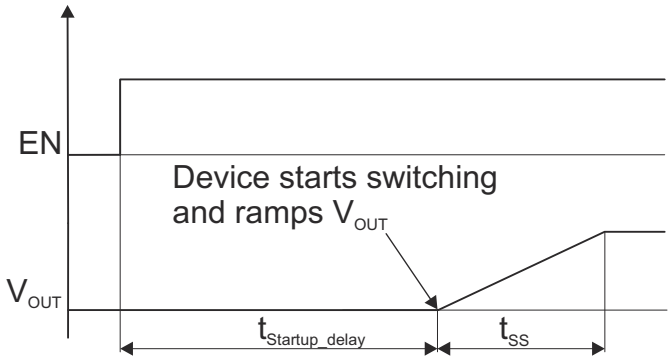


Figure 7-1. Device Start-Up

7.3.3 VSET Pin: Output Voltage Selection

The output voltage is set with a single external resistor connected between the VSET pin and GND. After the device has been enabled and the control logic as well as the internal reference have been powered up, a R2D (resistor-to-digital) conversion is started to detect the external resistor, R_{SET}, within the regulator start-up delay time, $t_{Startup\_delay}$. An internal current source applies current through the external resistor and an internal ADC reads back the resulting voltage level. Depending on the level, an internal feedback divider network is selected to set the correct output voltage. After this R2D conversion is finished, the current source is turned off to avoid current flow through the external resistor. The circuit can detect resistive values, high-level, low-level, and a pin-open.

For a proper reading, ensure that there is no additional current path or capacitance greater than 30pF total to GND during R2D conversion. Otherwise, the additional current to GND is interpreted as a lower resistor value and a false output voltage is set. Table 7-1 lists the correct resistor values for R_{SET} to set the appropriate output voltages. The R2D converter is designed to operate with resistor values out of the E96 table and requires 1% resistor value accuracy. The external resistor R_{SET} is not a part of the regulator feedback loop and has therefore no impact on the output voltage accuracy. Ensure that there is no other leakage path than the R_{SET} resistor at the VSET pin during an undervoltage lockout event. Otherwise, a false output voltage is set.

Table 7-1. Output Voltage Setting

VSET	Output Voltage Setting [V]			R_{SET} [Ω]
	TPS628436	TPS628437	TPS628438	
1	0.400	0.80	1.8	10.0k
2	0.425	0.85	1.9	12.1k
3	0.450	0.90	2.0	15.4k
4	0.475	0.95	2.1	18.7k
5	0.500	1.00	2.2	23.7k
6	0.525	1.05	2.3	28.7k
7	0.550	1.10	2.4	36.5k
8	0.575	1.15	2.5	44.2k
9	0.600	1.20	2.6	56.2k
10	0.625	1.25	2.7	68.1k
11	0.650	1.30	2.8	86.6k
12	0.675	1.35	2.9	105.0k
13	0.700	1.40	3.0	133.0k
14	0.725	1.45	3.1	162.0k
15	0.750	1.50	3.2	205.0k
16	0.775	1.55	3.3	249.0k or larger
17	0.8	1.6	3.4	VIN
0	1.0	1.8	3.6	GND

7.3.4 Undervoltage Lockout (UVLO)

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) comparator monitors the supply voltage. The UVLO comparator shuts down the device at an input voltage of 1.7V (maximum) with falling V_{IN}. The device starts at an input voltage of 1.8V (maximum) rising V_{IN}. After the device re-enters operation out of an undervoltage lockout condition, the device behaves like it does being enabled. The internal control logic is powered up and the external resistor at the VSET pin is read out.

7.3.5 Switch Current Limit, Short-Circuit Protection

The TPS62843 integrates a current limit on the high-side and low-side MOSFETs to protect the device against overload or short circuit conditions. The current in the switches is monitored cycle by cycle. If the high-side MOSFET current limit, $I_{HS(OC)}$ trips, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. After the inductor current through the low-side switch decreases beneath the low-side MOSFET current limit, $I_{LS(OC)}$, the low-side MOSFET is turned off and the high-side MOSFET turns on again.

7.3.6 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds the thermal shutdown temperature, $T_{J(SD)}$, of 160°C (typical), the device enters thermal shutdown. Both the high-side and low-side power FETs are turned off. When T_J decreases below the hysteresis amount of typically 20°C, the converter resumes operation, beginning with a soft start to the originally set V_{OUT} (there is no R2D conversion of R_{SET}). The thermal shutdown is not active in power save mode.

7.3.7 Output Voltage Discharge

The purpose of the output discharge function is to ensure a defined down-ramp of the output voltage when the device is disabled and to keep the output voltage close to 0V.

The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled. The minimum supply voltage required to keep the discharge function active is $V_{IN} > V_{TH\_UVLO(R)}$.

7.4 Device Functional Modes

7.4.1 Power Save Mode Operation

The DCS-Control topology supports power save mode operation. At light loads, the device operates in PFM (pulse frequency modulation) mode that generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shut down to achieve the lowest operating quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current. During the sleep periods, the current consumption is reduced to typically 275nA. This low quiescent current consumption is achieved by an ultra-low power voltage reference, an integrated high impedance feedback divider network, and an optimized power save mode operation.

In PFM mode, the switching frequency varies linearly with the load current. At medium and high load conditions, the device enters automatically PWM (pulse width modulation) mode and operates in continuous conduction mode with a nominal switch frequency f_{sw} of typically 1.5MHz. The switching frequency in PWM mode is controlled and depends on V_{IN} and V_{OUT}. The boundary between PWM and PFM mode is when the inductor current becomes discontinuous.

If the load current decreases, the converter seamlessly enters PFM mode to maintain high efficiency down to very light loads. Because DCS-Control supports both operation modes within one single building block, the transition from PWM to PFM mode is seamless with minimum output voltage ripple.

7.4.2 100% Mode Operation

The duty cycle of the buck converter operating in PWM mode is given as $D = V_{OUT}/V_{IN}$. The duty cycle increases as the input voltage comes close to the output voltage. In 100% duty cycle mode, the device keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the internal set point. This allows the conversion of small input to output voltage differences.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following sections discuss the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

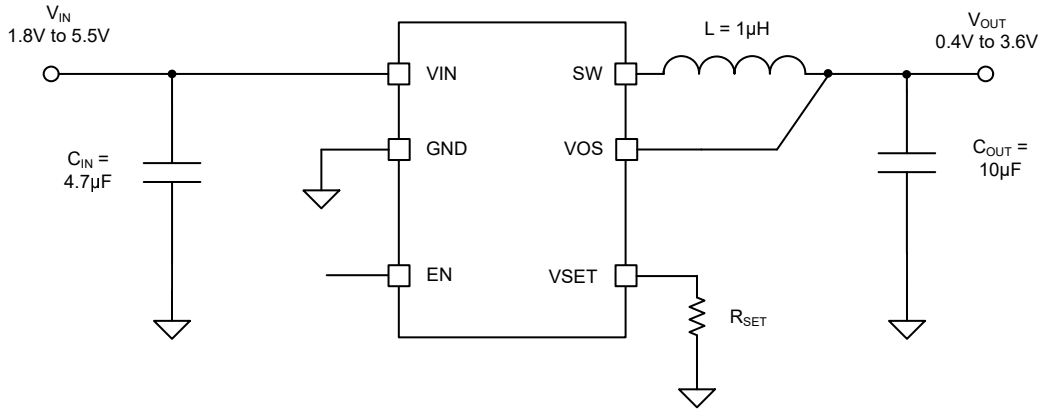


Figure 8-1. TPS62843 Typical Application Circuit

8.2.1 Design Requirements

Table 8-1 shows the list of components for the application circuit and the characteristic application curves.

Table 8-1. Components for Application Characteristic Curves

Reference	Description	Value	Size Code Inch [metric L × W × T]	Manufacturer
TPS628436, TPS628437, TPS628438	275nA-I_Q buck converter		[1.05mm × 0.8mm × 0.4mm]	TI
C_{IN}	Ceramic capacitor GRM155R60J475ME47D	4.7µF	0402 [1.0mm × 0.5mm × 0.5mm]	Murata
L	Inductor DFE201610-1R0M	1µH	0806 [2.0mm × 1.6mm × 1.0mm]	Murata
C_{OUT}	Ceramic capacitor GRM155R60J106ME15D	10µF	0402 [1.0mm × 0.5mm × 0.5mm]	Murata
R_{SET}	See voltage setting table		0402 [1.0mm × 0.5mm × 0.5mm]	

8.2.2 Detailed Design Procedure

Follow the passive component selection per the typical application circuit.

8.2.3 Application Curves

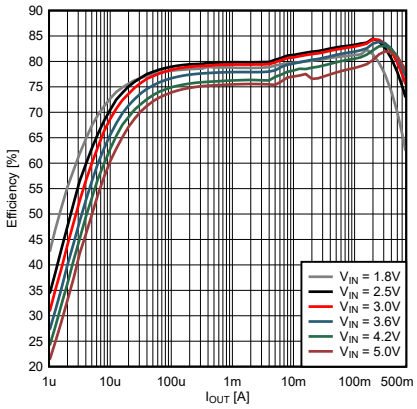


Figure 8-2. Efficiency at V_{OUT} = 0.4V

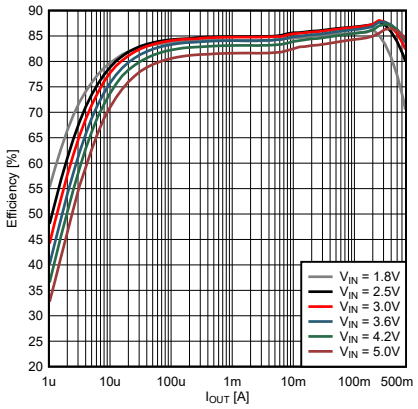


Figure 8-3. Efficiency at V_{OUT} = 0.7V

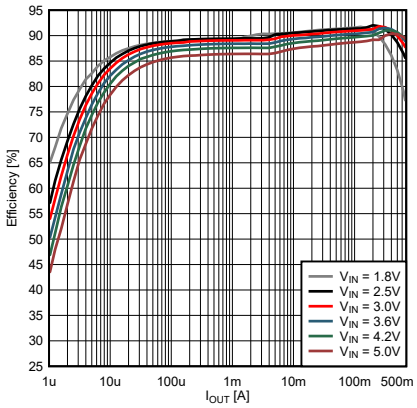


Figure 8-4. Efficiency at V_{OUT} = 1.2V

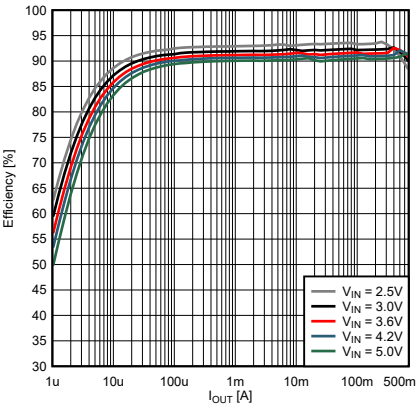


Figure 8-5. Efficiency at V_{OUT} = 1.8V

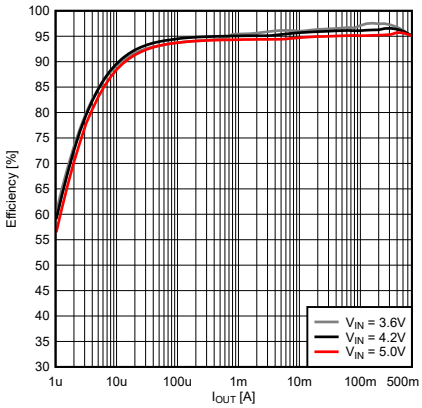


Figure 8-6. Efficiency at V_{OUT} = 3.3V

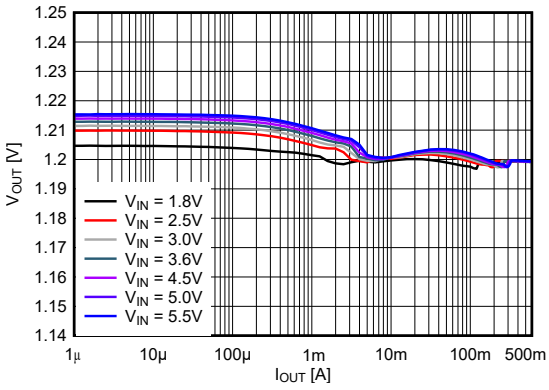


Figure 8-7. Output Voltage vs Output Current at V_{OUT} = 1.2V

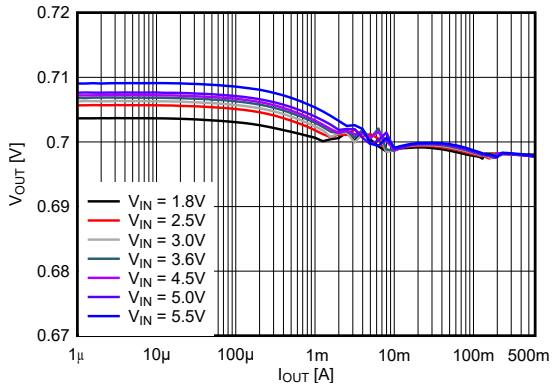


Figure 8-8. Output Voltage vs Output Current at V_{OUT} = 0.7V

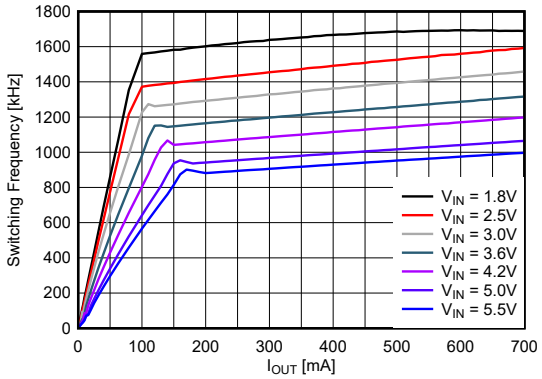


Figure 8-9. Switching Frequency vs Output Current at V_{OUT} = 0.4V

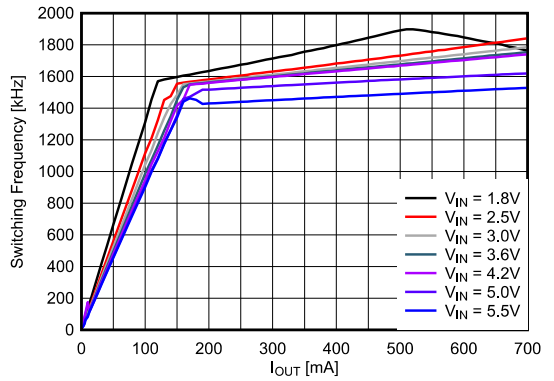


Figure 8-10. Switching Frequency vs Output Current at V_{OUT} = 0.7V

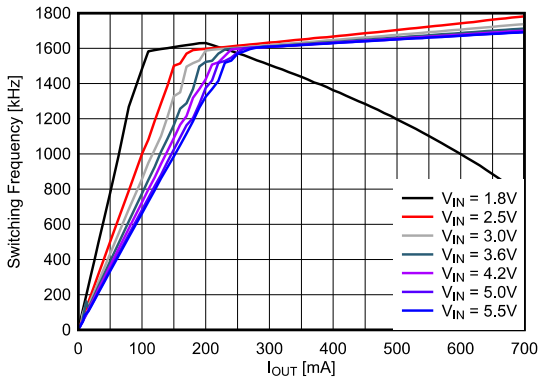


Figure 8-11. Switching Frequency vs Output Current at V_{OUT}= 1.2V

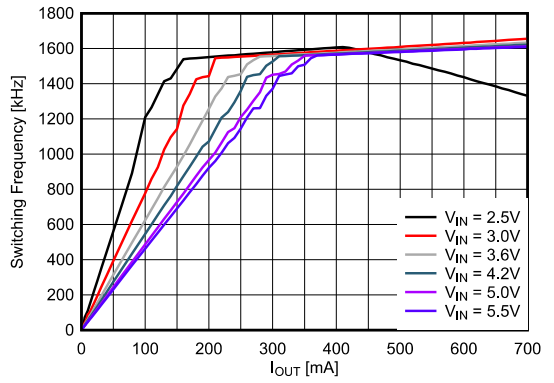


Figure 8-12. Switching Frequency vs Output Current at V_{OUT}= 1.8V

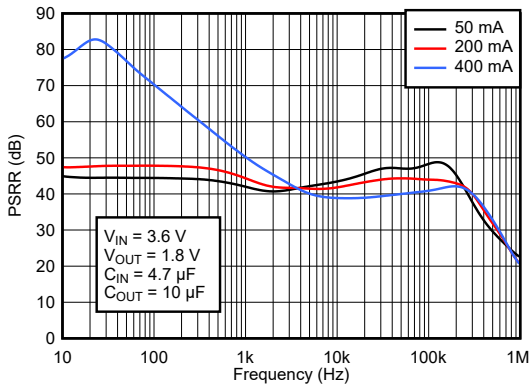


Figure 8-13. Power Supply Rejection Ratio (PSRR) at V_{OUT} = 1.8V

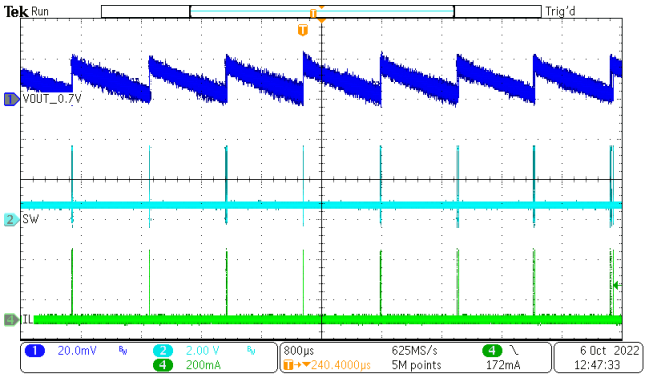


Figure 8-14. Typical Operation at V_{OUT} = 0.7V, I_{OUT} = 100µA

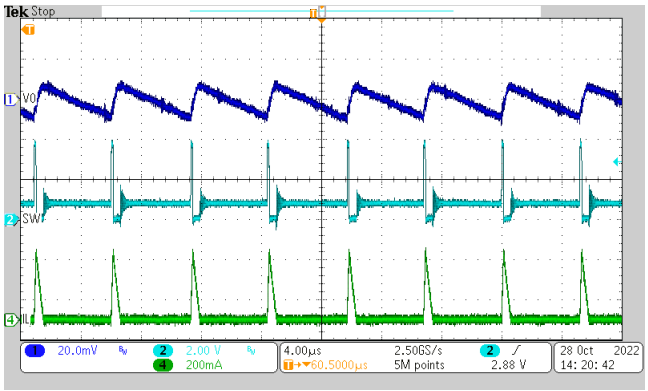


Figure 8-15. Typical Operation at V_{OUT} = 0.7V, I_{OUT} = 20mA

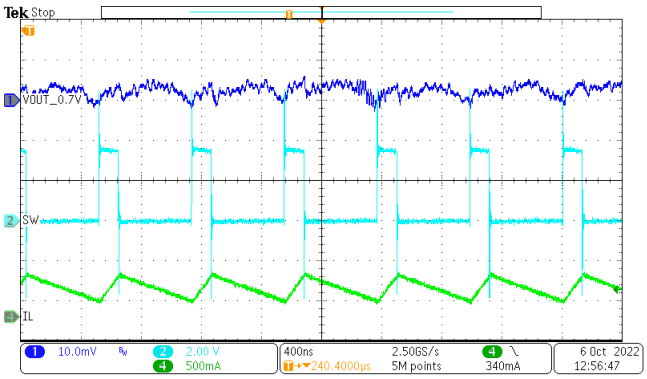


Figure 8-16. Typical Operation at V_{OUT} = 0.7V, I_{OUT} = 400mA

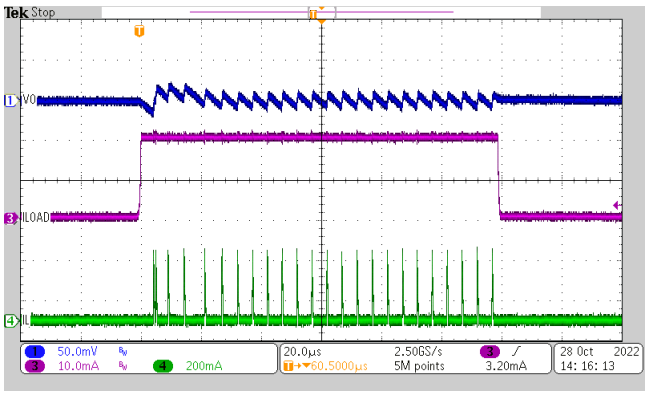


Figure 8-17. Load Transient at V_{OUT} = 0.7V, I_{OUT} = 100 µA to 20 mA

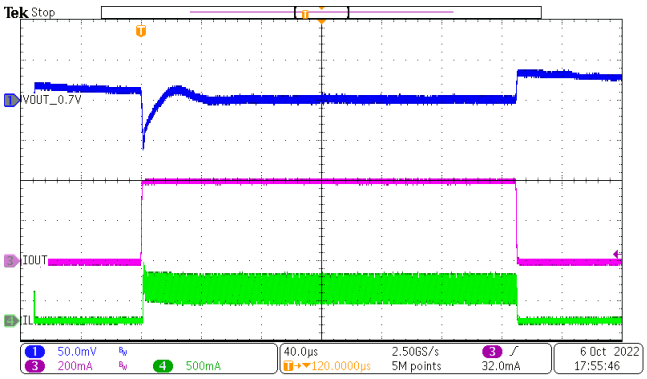


Figure 8-18. Load Transient at V_{OUT} = 0.7V, I_{OUT} = 100µA to 400mA

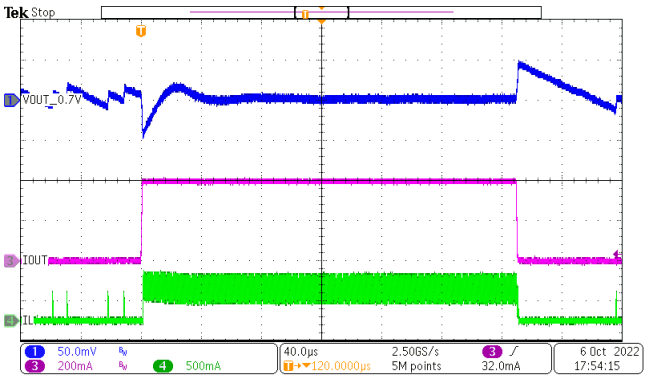


Figure 8-19. Load Transient at V_{OUT} = 0.7V, I_{OUT} = 5mA to 400mA

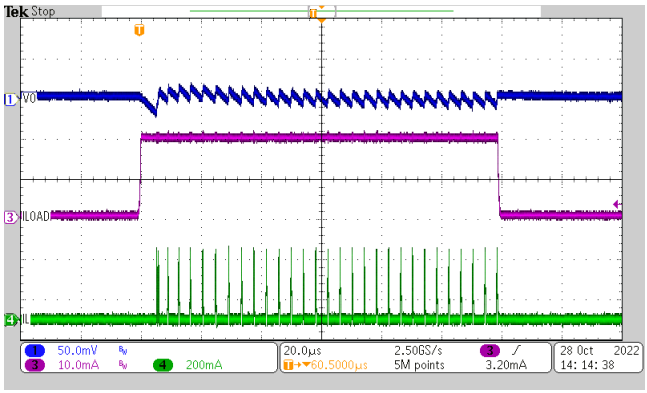


Figure 8-20. Load Transient at V_{OUT} = 1.2V, I_{OUT} = 100µA to 20mA

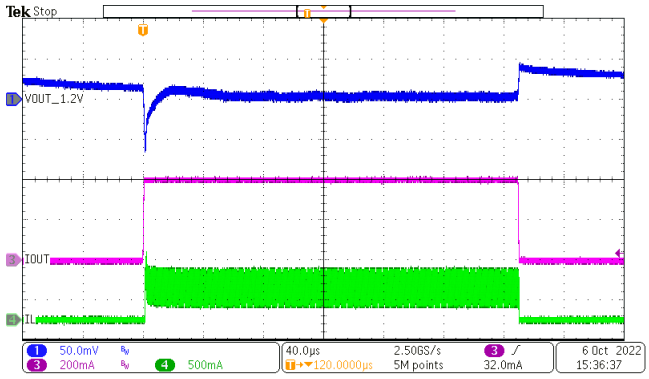


Figure 8-21. Load Transient at V_{OUT} = 1.2V, I_{OUT} = 100µA to 400mA

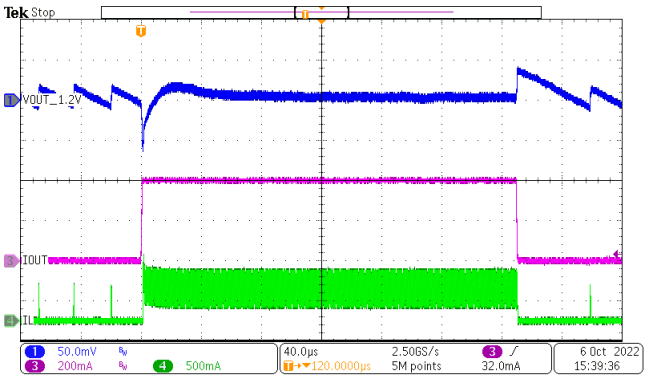


Figure 8-22. Load Transient at V_{OUT} = 1.2V, I_{OUT} = 5mA to 400mA

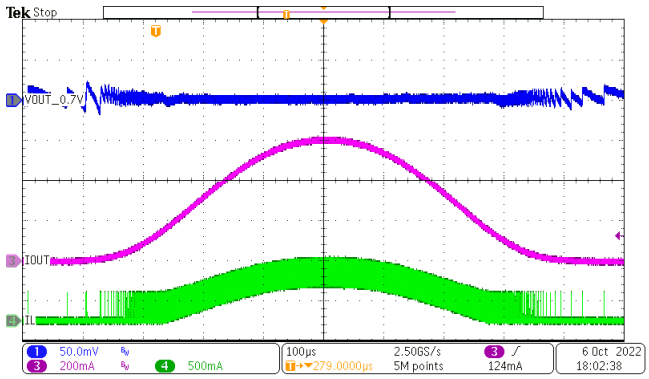


Figure 8-23. AC Load Sweep at V_{OUT} = 0.7V, I_{OUT} = 1mA to 600mA

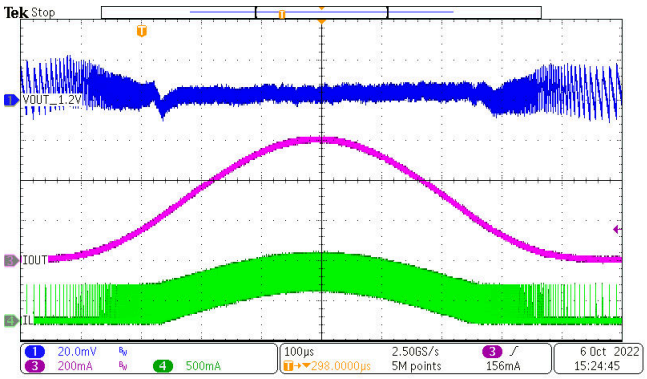


Figure 8-24. AC Load Sweep at V_{OUT} = 1.2V, I_{OUT} = 1mA to 600mA

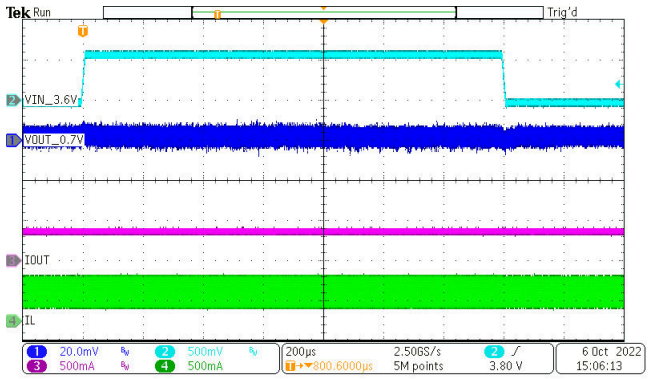


Figure 8-25. Line Transient at V_{OUT} = 0.7V, I_{OUT} = 400mA, V_{IN} = 3.6V to 4.2V

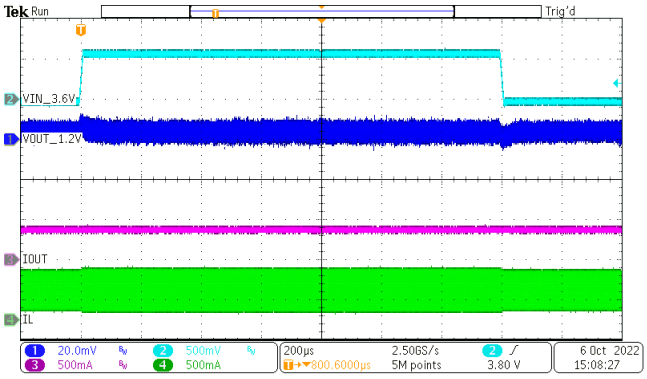


Figure 8-26. Line Transient at V_{OUT} = 1.2V, I_{OUT} = 400mA, V_{IN} = 3.6V to 4.2V

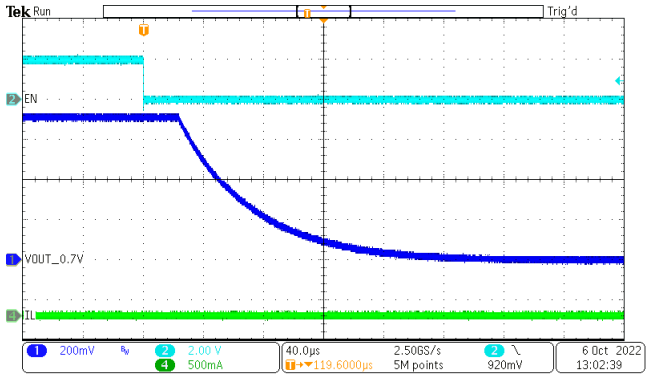


Figure 8-27. Shutdown, Output Discharge at V_{OUT} = 0.7V

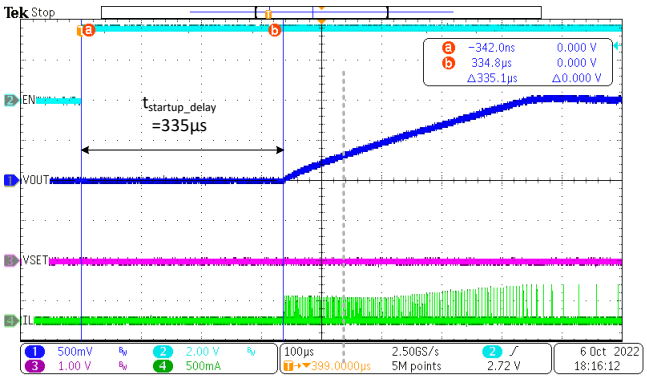


Figure 8-28. Start-Up Delay Time, VSET = GND

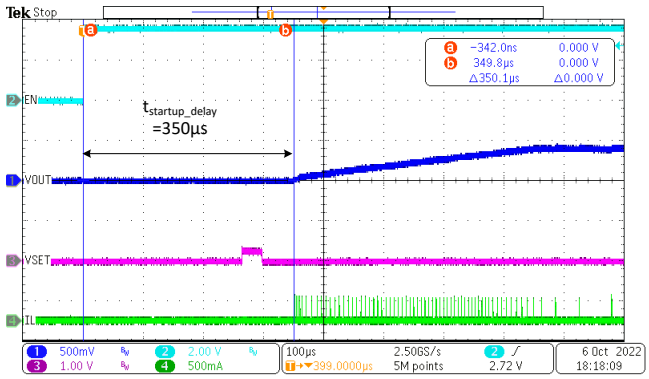


Figure 8-29. Start-Up Delay Time, VSET = 10kohms

8.3 Power Supply Recommendations

The power supply must provide a current rating according to the supply voltage, output voltage, and output current of the TPS62843.

8.4 Layout

8.4.1 Layout Guidelines

The pinout of the TPS62843 has been optimized to enable a single top layer PCB routing of the IC and its critical passive components such as CIN, COUT, and L. Furthermore, this pinout allows the user to connect tiny components such as 0201 (0603 Metric) size capacitors and 0402 (1005 Metric) size inductors. A solution size smaller than 5mm^2 can be achieved with a fixed output voltage. As for all switching power supplies, the layout is an important step in the design. Care must be taken in board layout to get the specified performance. Providing a low inductance, low impedance ground path is critical. Therefore, use wide and short traces for the main current paths. Place the input capacitor as close as possible to the VIN of the IC and GND pins. This placement is the most critical component placement. The VOS line is a sensitive, high impedance line and must be connected to the output capacitor and routed away from noisy components and traces (for example, the SW line) or other noise sources.

8.4.2 Layout Example

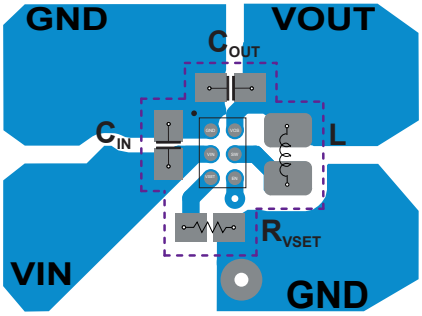


Figure 8-30. Layout Example (YKA Package)

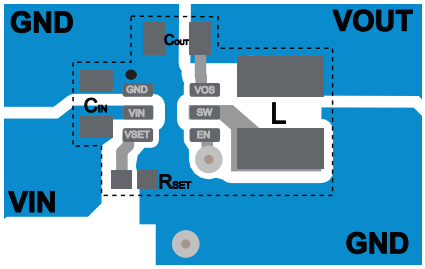


Figure 8-31. Layout Example (DRL Package)

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2023) to Revision C (June 2024)	Page
• Added a clarification that the minimum effective output capacitance is 4µF	1
• Deleted the preview note from the SOT563 package	1
• Added a column for the SOT563 package to add the pin numbers for the SOT563 package	4
• Added an Input Buffer block to the EN pin in the functional block diagram	9
• Added a statement in the description saying " The high level of the EN pin must not exceed VIN voltage level" to clarify correct pin usage	10
• Deleted the term I_{LIMF} and replaced with $I_{HS(OC)}$ for the high side FET and replaced with $I_{LS(OC)}$for the low side FET	11
• Deleted the erroneous load transient plot (Output Voltage vs Output Current for V_{OUT} 1.2V, and I_{OUT} step = 100uA to 400mA) and replaced with the correct plot	14

Changes from Revision A (May 2023) to Revision B (September 2023)	Page
• Added SOT563 package to the document	1

Changes from Revision * (January 2022) to Revision A (May 2023)	Page
• Changed document status from Advance Information to Production Data	1

11 Mechanical, Packaging, and Orderable Information

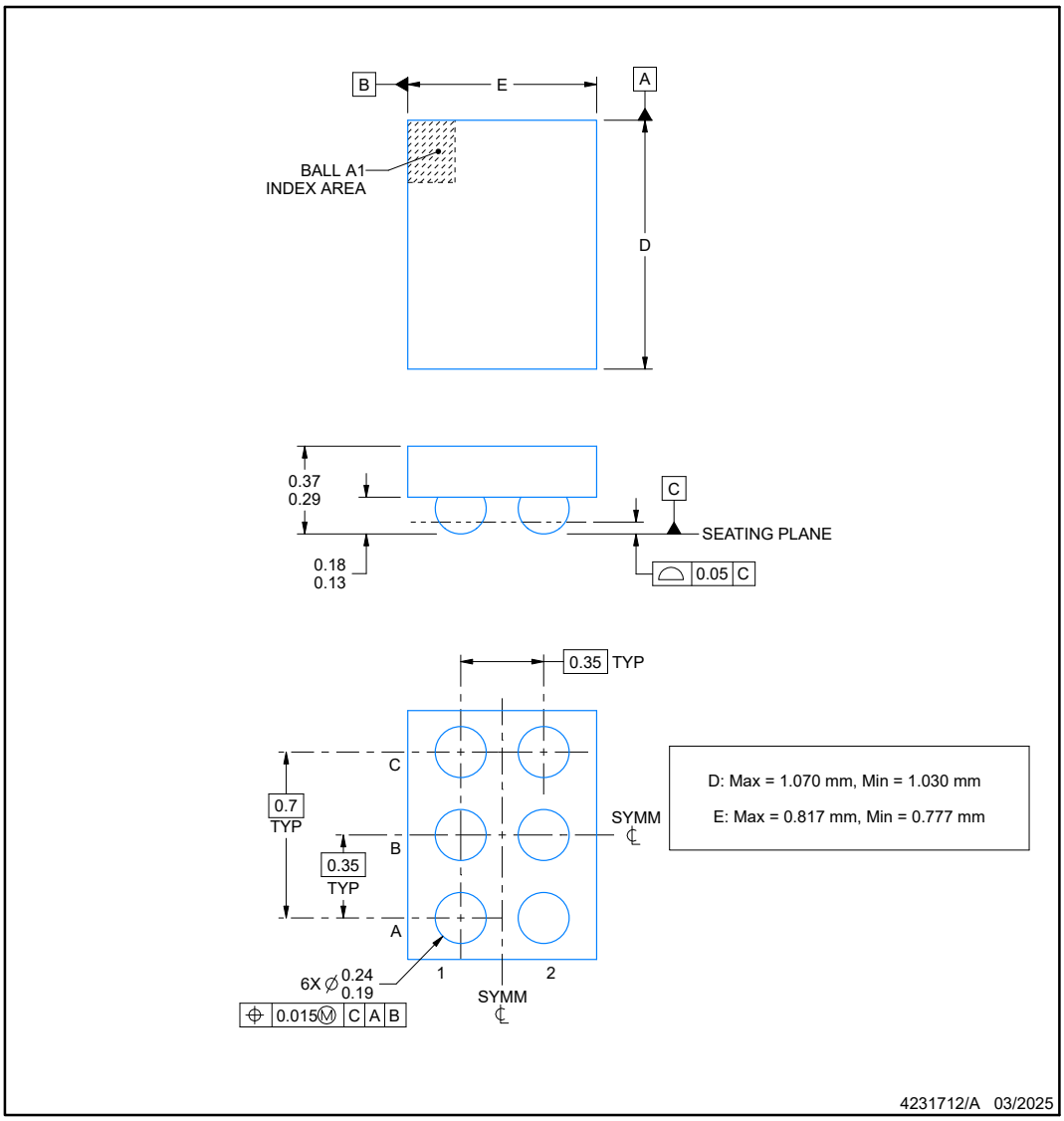
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

YKA0006-C02

DSBGA - 0.37 mm max height

DIE SIZE BALL GRID ARRAY



NanoFree Is a trademark of Texas Instruments.

NOTES:

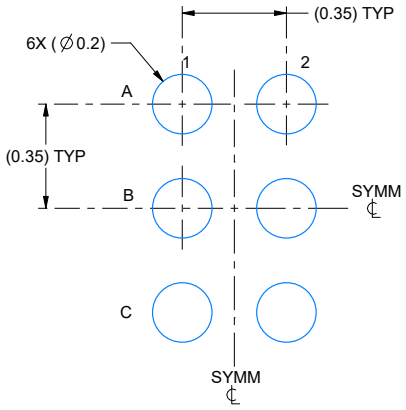
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT

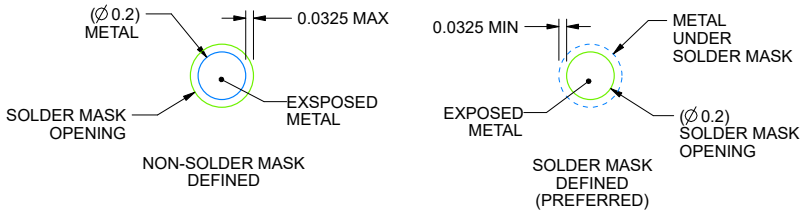
YKA0006-C02

DSBGA - 0.37 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4231712/A 03/2025

NOTES: (continued)

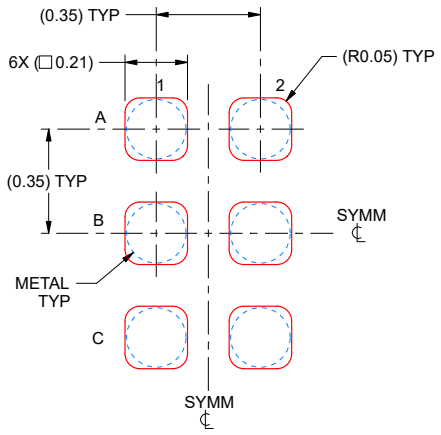
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YKA0006-C02

DSBGA - 0.37 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm - 0.1 mm THICK STENCIL
SCALE:50X

4231712/A 03/2025

NOTES: (continued)

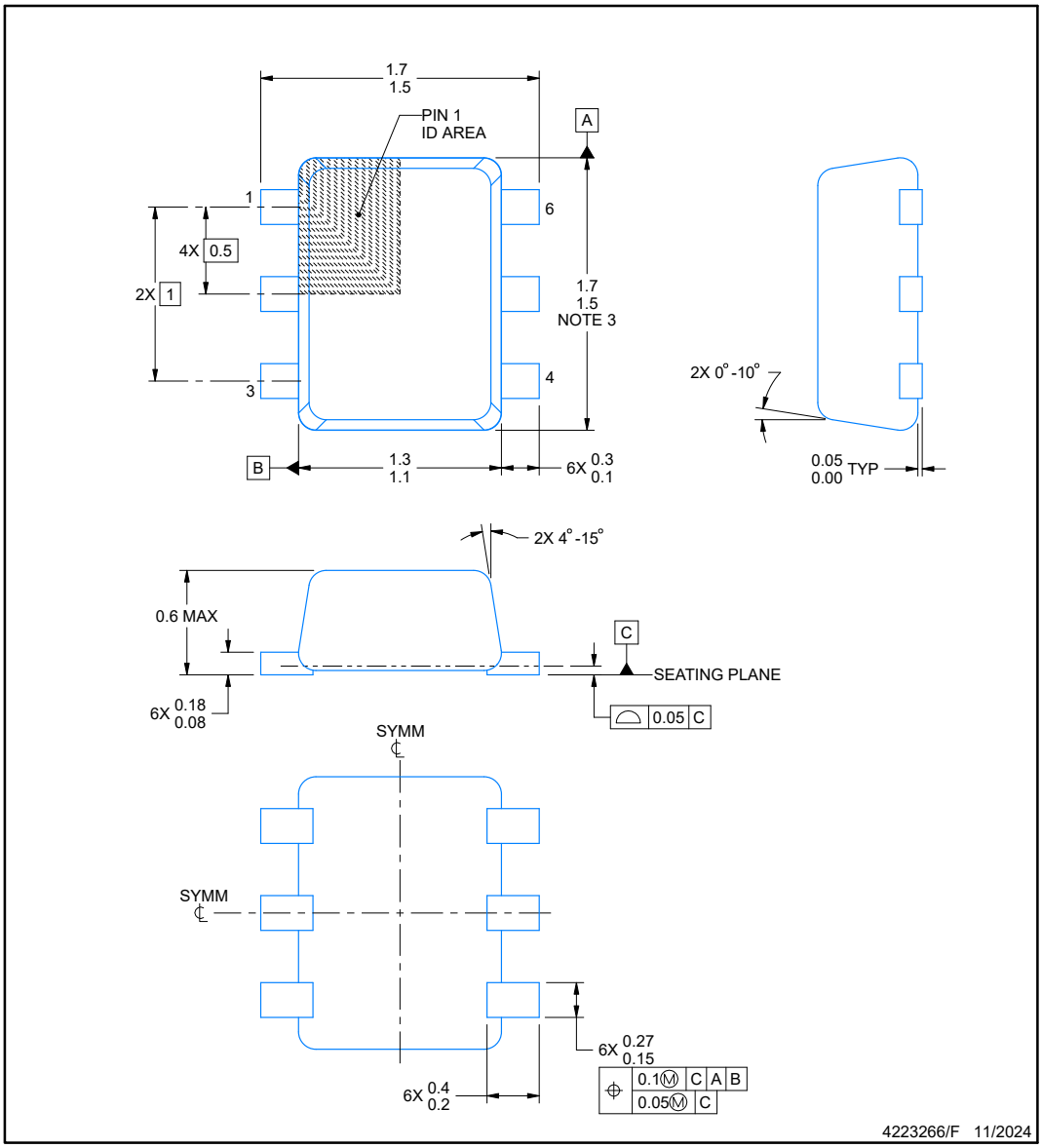
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

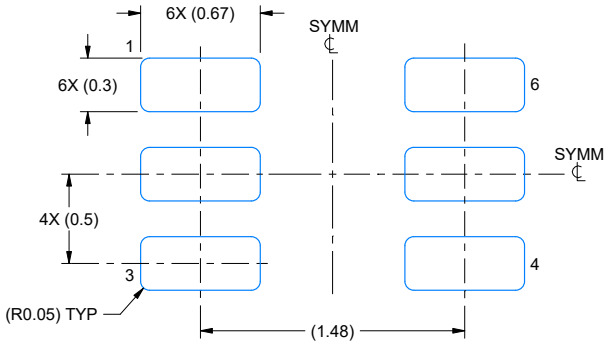
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

www.ti.com

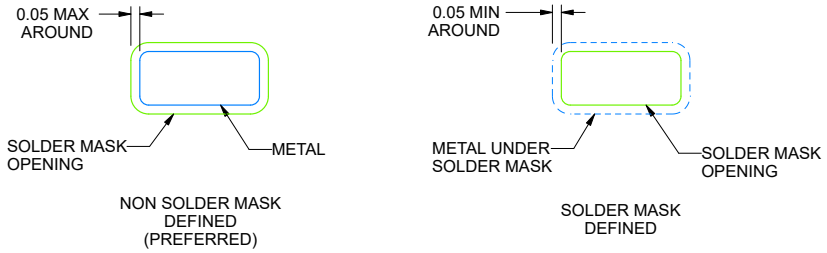
EXAMPLE BOARD LAYOUT

DRL0006A — **SOT - 0.6 mm max height**

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/F 11/2024

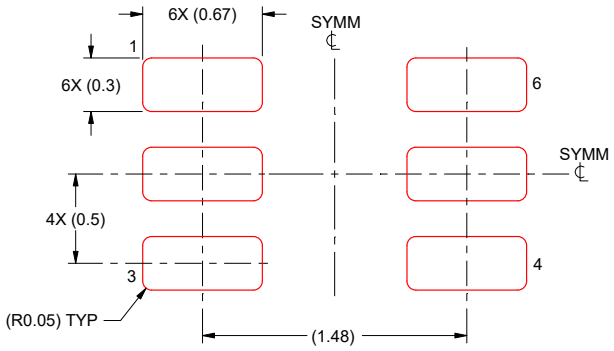
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A — **SOT - 0.6 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS628436DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	436
TPS628436DRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	436
TPS628436YKAR	Active	Production	DSBGA (YKA) | 6	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	J
TPS628436YKAR.A	Active	Production	DSBGA (YKA) | 6	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	J
TPS628437DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	437
TPS628437DRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	437
TPS628437YKAR	Active	Production	DSBGA (YKA) | 6	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	K
TPS628437YKAR.A	Active	Production	DSBGA (YKA) | 6	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	K
TPS628438DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	438
TPS628438DRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	438
TPS628438YKAR	Active	Production	DSBGA (YKA) | 6	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	L
TPS628438YKAR.A	Active	Production	DSBGA (YKA) | 6	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	L

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

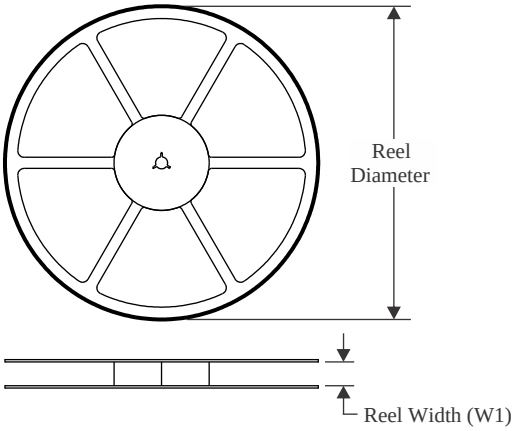
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

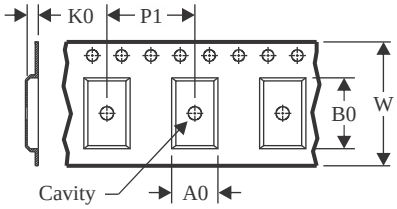
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

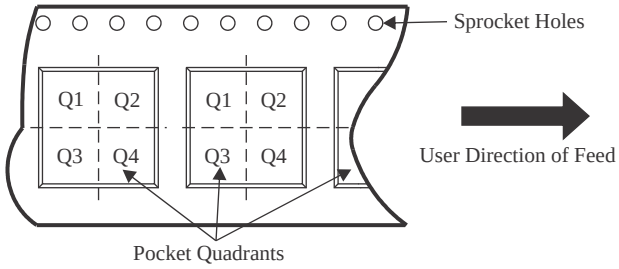


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

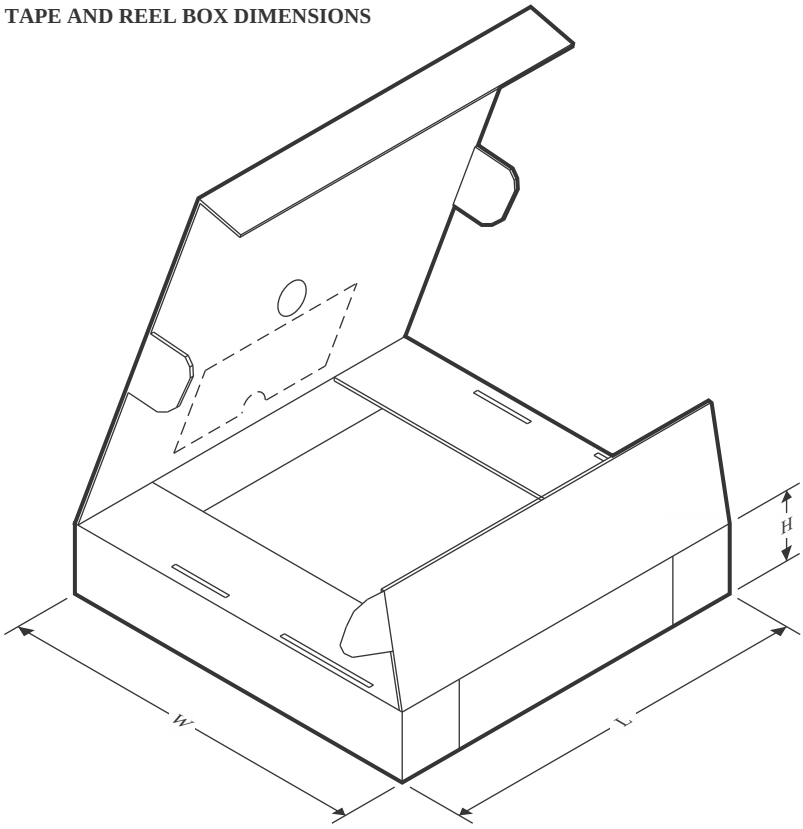
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS628436DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS628436YKAR	DSBGA	YKA	6	12000	180.0	8.4	0.9	1.16	0.47	2.0	8.0	Q1
TPS628437DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS628437YKAR	DSBGA	YKA	6	12000	180.0	8.4	0.9	1.16	0.47	2.0	8.0	Q1
TPS628438DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS628438YKAR	DSBGA	YKA	6	12000	180.0	8.4	0.9	1.16	0.47	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

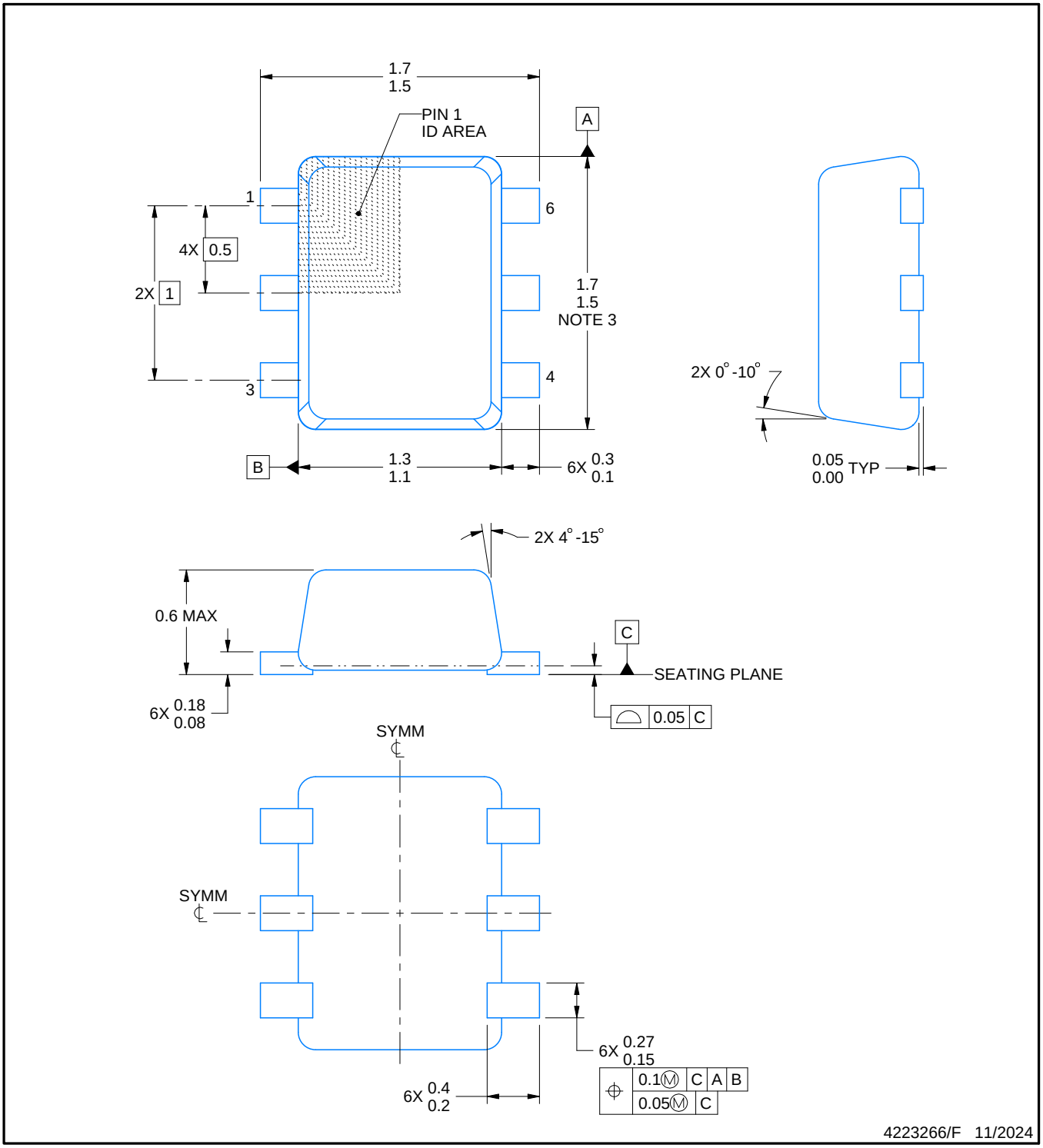
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS628436DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS628436YKAR	DSBGA	YKA	6	12000	182.0	182.0	20.0
TPS628437DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS628437YKAR	DSBGA	YKA	6	12000	182.0	182.0	20.0
TPS628438DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS628438YKAR	DSBGA	YKA	6	12000	182.0	182.0	20.0

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

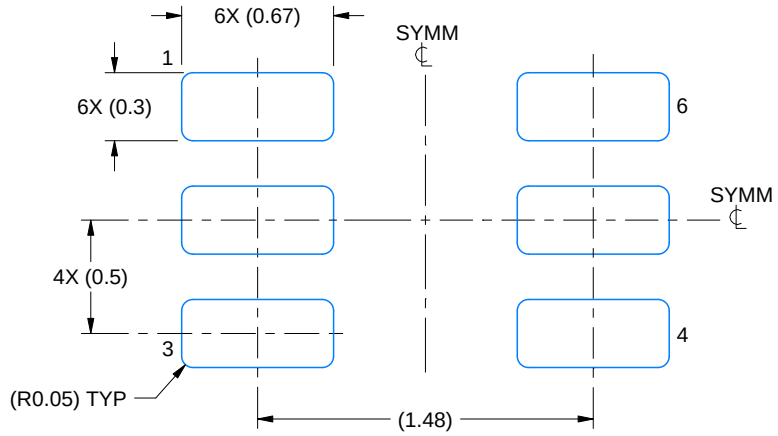
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

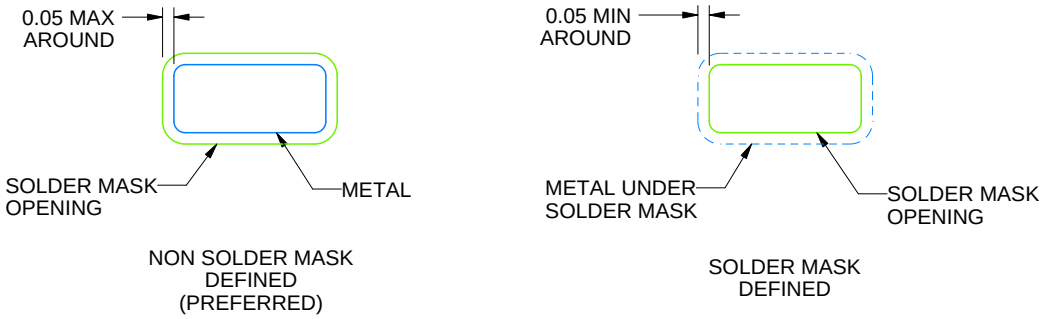
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

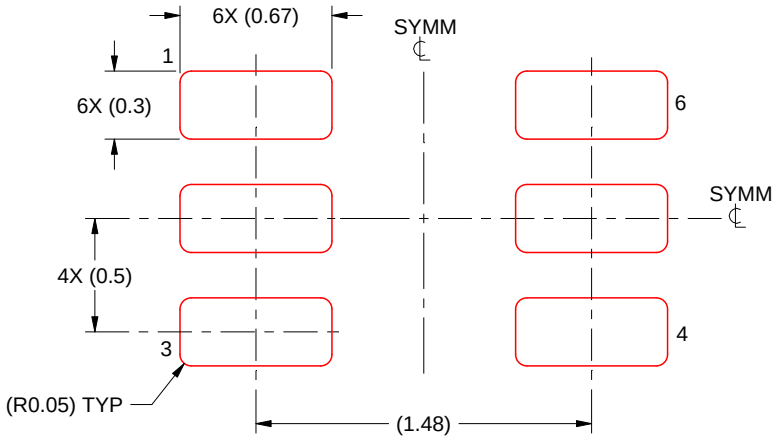
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

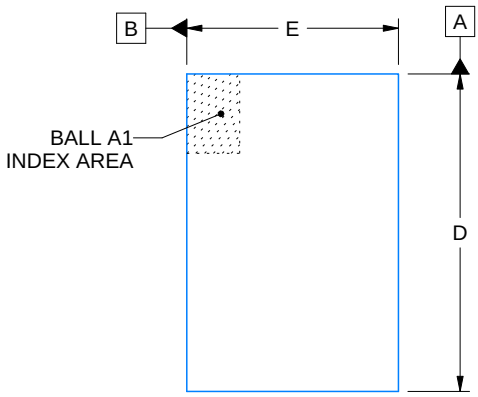
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

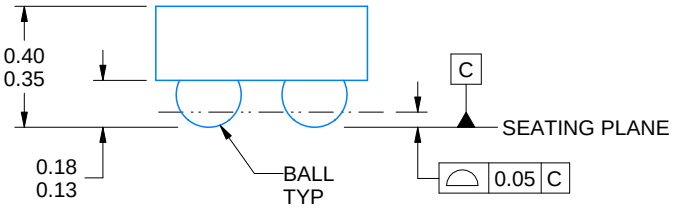
PACKAGE OUTLINE

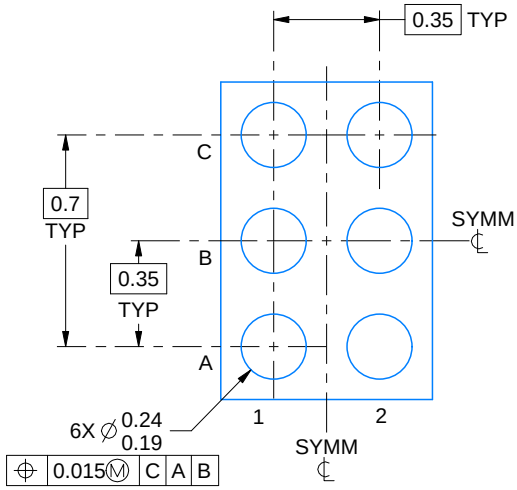
YKA0006

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY







D: Max = 1.04 mm, Min = 0.98 mm

E: Max = 0.787 mm, Min =0.727 mm

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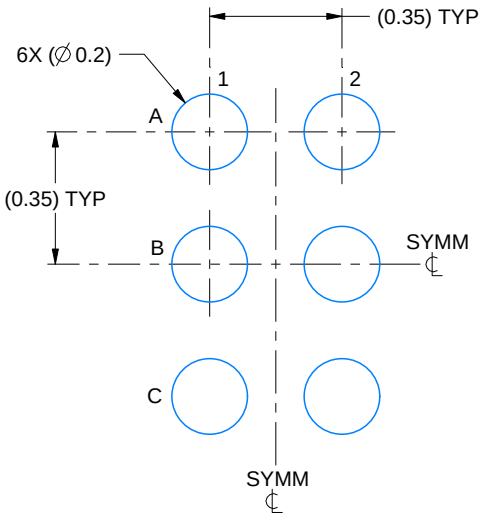
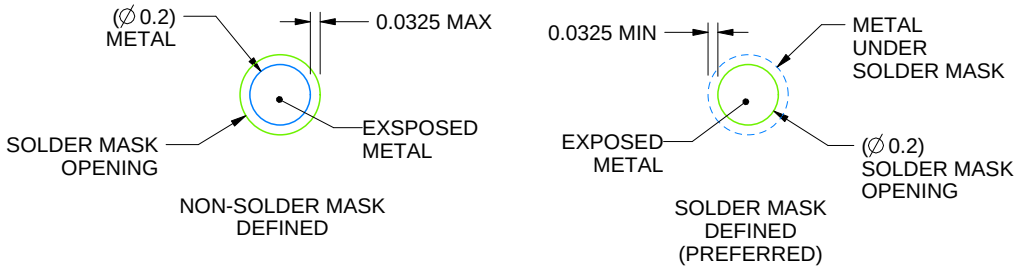
NanoFree Is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

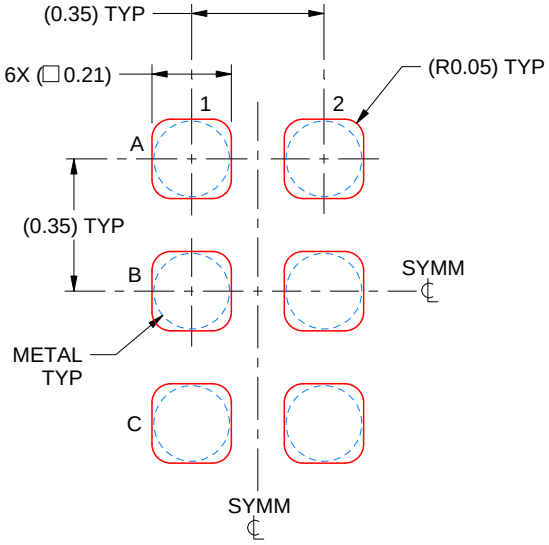
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YKA0006

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm - 0.1 mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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