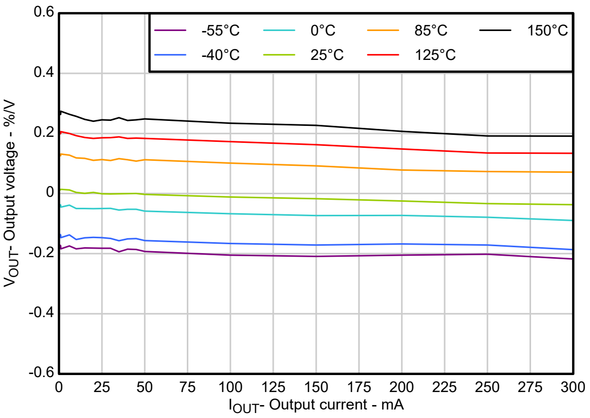
TPS7E72 300mA, 30V, Ultra-Low I_Q Low-Dropout Regulator

1 Features

- Input voltage range: 3.0V to 30V (32V max)
- Available output voltage options:
  - Fixed: 1.8V to 12V
  - Adjustable: 1.2V to 28V
- Output current: Up to 300mA
- ±1.2% accuracy across line, load and temperature
- Ultra-low I_Q: 2.8μA at I_{OUT} = 0mA
- Stable with 4.7μF or larger ceramic capacitors
  - ESR range: 0Ω to 1Ω
- Dropout voltage: 900mV (typical) at 300mA
- High PSRR:
  - 70dB at 1kHz
  - 45dB at 100kHz
- Over-current, over-power and over-temperature limiting
- Package:
  - 5-pin SOT-23 (DBV) [$R_{\theta JA}$: 190.9°C/W]
  - 6-pin WSON (DRV) [$R_{\theta JA}$: 90.2°C/W]
- Operating junction temperature: –40°C to +125°C
  - Extended range, M version: –40°C to +150°C

2 Applications

- Appliances
- Home and building automation
- Retail automation and payment
- Grid infrastructure
- Medical applications
- Lighting applications



V_{IN} = 5.3V, V_{OUT} = 3.3V

V_{OUT} Accuracy vs I_{OUT}

3 Description

The TPS7E72 low-dropout (LDO) linear voltage regulator is a low quiescent current device and supports wide input voltage range from 3V to 30V. The wide output range is from 1.2V to 28V for the adjustable configuration, 1.8V to 12V for the fixed configuration, and a load current of up to 300mA is supported. With only a 2.8μA quiescent current at no-load, the device is designed to power microcontrollers and other low-power loads for battery-powered applications.

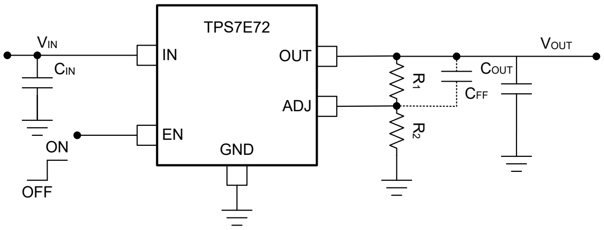
The TPS7E72 supports very tight DC accuracy of ±1.2% over line, load and temperature range. The device responds quickly to line and load transients. The low quiescent current (2.8μA typically) during regulation and controlled I_Q even in dropout operation (12μA typically in no-load dropout) makes this device designed for battery-powered or always-on systems that require very little idle-state power dissipation.

The TPS7E72 supports a low dropout of typically 900mV at 300mA of load current. The device has built-in protection mechanism for over-current, over-temperature and over-power delivery for reliable operation of the LDO. The TPS7E72 is stable with an output capacitor range of 4.7μF to 100μF.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS7E72	DBV (SOT-23, 5)	2.9mm × 2.8mm
	DRV (WSON, 6)	2.0mm × 2.0mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information* section.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application

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4 Pin Configuration and Functions

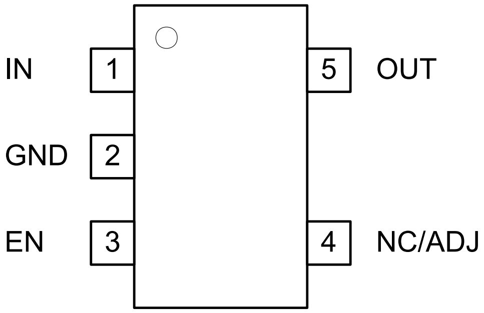


Figure 4-1. DBV Package, (Fixed/ADJ), 5-Pin SOT-23 (Top View)

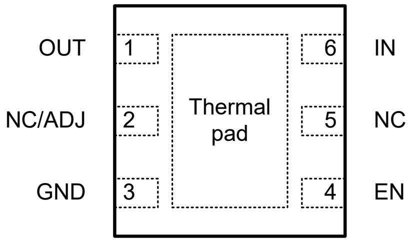


Figure 4-2. DRV Package (Fixed/ADJ), 6-Pin WSON (Top View)

Table 4-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	No.			
	DBV	DRV		
GND	2	3	—	Ground pin.
IN	1	1	Input	Input supply pin. See the *Recommended Operating Conditions* table and the *Input and Output Capacitor Selection* section for more information.
OUT	5	6	Output	Output of the regulator. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the *Recommended Operating Conditions* table and the *Input and Output Capacitor Selection* section. Place the output capacitor as close to output of the device as possible.
EN	3	2	Input	Enable pin. Driving the enable pin high enables the device. Driving this pin low disables the device. High and low thresholds are listed in the *Electrical Characteristics* table. This pin has a weak internal pullup and can be left floating to enable the device or the pin can be connected to the input pin. Refer to the *Enable (EN)* section for more details.
NC/ADJ	4	4	Input	When using the adjustable device, this pin sets the output voltage with the help of a feedback divider. In the adjustable configuration, this pin must be connected through a resistor divider to the output for the device to function. If using a fixed output device, this pin is not internally connected and can either be left floating or connected to GND.
NC	—	5	—	Not internally connected. Leave this pin open or connected to any potential. Tie this pin to ground for improved thermal performance.
Thermal pad				Thermal pad. Connect the pad to GND for the best possible thermal performance. See the *Layout* section for more information.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	32.0	V
	V_{OUT} (for fixed device only)	–0.3	2 × $V_{OUT(nom)}$ or V_{IN} + 0.3 or 15.0 (whichever is lower)	
	V_{OUT} (for adjustable device only)	–0.3	V_{IN} + 0.3 [2]	
	V_{ADJ} (Feedback voltage)	–0.3	3.6	
	V_{EN} (Enable voltage)	–0.3	32.0	
Current	I_{OUT} (Output current)	Internally limited		mA
Temperature	T_J, Operating junction	–55	150	°C
	T_{stg}, Storage	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The absolute maximum rating is V_{IN} + 0.3V or 32.0V, whichever is smaller.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22C101, all pins[2]	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range	3.0		30	V
V_{OUT}	Output voltage range (Fixed only)[1]	1.8		12	V
V_{OUT}	Output voltage range (Adjustable only)[1]	1.2		28	V
V_{EN}	Enable voltage range	0		30	V
I_{OUT}	Output current	0		300	mA
C_{IN}	Input capacitor[2]		0.47		µF
C_{OUT}	Output capacitor [3]	4.7		100	µF
C_{ADJ}	ADJ to GND (feedback) capacitor[4]			15	pF
C_{FF}	Feed-forward capacitor [5]		10		nF
T_J	Operating junction temperature	–40		125	°C
	Operating junction temperature (M version only)	–40		150	°C

(1) This output voltage range does not include device accuracy or accuracy of the feedback resistors.
(2) An input capacitor is not required for LDO stability. However, an input capacitance with an effective value of 0.1µF minimum is recommended to counteract the effect of source resistance and inductance, which can in some cases cause symptoms of system level instability such as ringing or oscillation, especially in the presence of load transients.
(3) All capacitor values listed are the nominal value and the effective capacitance is assumed to derate up-to 50% of the nominal capacitor value.

(4) The upper limit for the capacitor on the ADJ pin with respect to GND impacts the stable operation of the voltage regulator in adjustable configuration. For C_{ADJ} capacitor higher than limits mentioned in *Recommended Operating Conditions* table, use C_{FF} capacitor.

(5) The C_{FF} capacitor improves transient, noise, and PSRR performance, but is not required for regulator stability. Using a higher capacitance C_{FF} is permissible but start-up time increases.

5.4 Thermal Information

THERMAL METRIC (1)		TPS7E72		UNIT
		DRV (WSON) (2)	DBV (SOT-23) (2)	
		6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.2	190.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	113.5	89.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.7	60.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.0	28.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	55.3	59.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	30.6	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

(2) Thermal performance results are based on the JEDEC standard of 2s2p PCB configuration. These thermal metric parameters are further improved by 35-55% based on thermally optimized PCB layout designs. See the analysis of the Impact of board layout on LDO thermal performance application note.

5.5 Electrical Characteristics

Over operating junction temperature range (T_J = –40°C to +125°C, extended range for M version: T_J = –40°C to +150°C), V_{IN} = 3.0V or $V_{IN} = V_{OUT(nom)}$ + 0.5V (whichever is greater), I_{OUT} = 1mA, V_{EN} = 2.0V, C_{IN} = 1.0µF, C_{OUT} = 4.7µF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ADJ}	Feedback voltage			1.2		V
V_{UVLO+}	Rising input supply UVLO	V_{IN} rising		2.8	2.91	V
V_{UVLO-}	Falling input supply UVLO	V_{IN} falling	2.6	2.7		V
$V_{UVLO(HYST)}$	V_{UVLO} hysteresis			100		mV
V_{OUT}	Output voltage	$V_{IN} = V_{OUT}$ + 0.5V, I_{OUT} = 1mA, T_J = 25℃	–0.3		0.3	%
V_{OUT}	Output voltage	V_{OUT} + 2.0V ≤ V_{IN} ≤ 30V, I_{OUT} = 35mA, T_J = 25℃	–0.7		0.7	%
		V_{OUT} + 2.0V ≤ V_{IN} ≤ 30V, I_{OUT} = 35mA	–1.2		1.2	
		1mA ≤ I_{OUT} ≤ 300mA, 2.0V ≤ $V_{IN} - V_{OUT}$ ≤ 15V	–1.2		1.2	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	I_{OUT} = 1mA, V_{OUT} + 0.5V ≤ V_{IN} ≤ 30V			10	mV
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	1mA ≤ I_{OUT} ≤ 300mA, $V_{IN} = V_{OUT}$ + 2.0V, 1.2V ≤ V_{OUT} < 5.0V			11	mV
		1mA ≤ I_{OUT} ≤ 300mA, $V_{IN} = V_{OUT}$ + 2.0V, 5.0V ≤ V_{OUT} < 12.0V			22	mV
$\Delta\%V_{OUT}/\Delta I_{OUT}$	Load regulation	1mA ≤ I_{OUT} ≤ 300mA, $V_{IN} = V_{OUT}$ + 2.0V, 12.0V ≤ V_{OUT}			0.65	%/A
V_{DO}	Dropout voltage	I_{OUT} = 300mA		0.95	1.8	V
		I_{OUT} = 300mA, for adjustable		0.96	1.8	
V_{DO}	Dropout voltage	I_{OUT} = 100mA		0.3	0.55	V
		I_{OUT} = 100mA, for adjustable		0.32	0.56	
I_{LIM}	Output current limit	V_{OUT} forced at 0.9 × $V_{OUT(nom)}$, $V_{IN} = V_{OUT(nom)}$ + 2.0V	350	500	625	mA
I_{SC}	Short-circuit current limit	R_{LOAD} = 20mΩ	30	55	80	mA
I_{PLIMIT}	Current limit at max headroom	V_{IN} = 30V, V_{OUT} = 1.2V			35	mA
$V_{HEADROOM}$	Max headroom at full load	V_{OUT} = 1.2V			15	V
I_{ADJ}	Feedback current	V_{IN} = 30V			25	nA

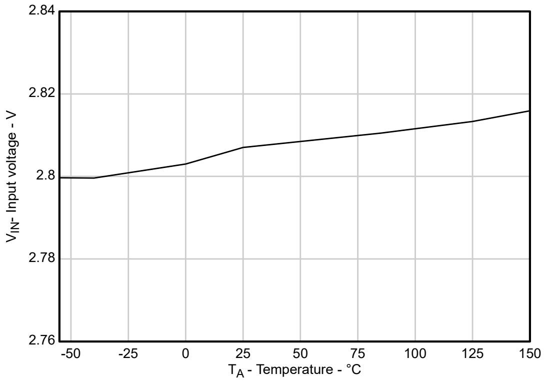
5.5 Electrical Characteristics (continued)

Over operating junction temperature range (T_J = –40°C to +125°C, extended range for M version: T_J = –40°C to +150°C), V_{IN} = 3.0V or V_{IN} = $V_{OUT(nom)}$ + 0.5V (whichever is greater), I_{OUT} = 1mA, V_{EN} = 2.0V, C_{IN} = 1.0µF, C_{OUT} = 4.7µF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Quiescent current	3.0V ≤ V_{IN} ≤ V_{OUT} – 0.2V , I_{OUT} = 0mA		12.5	25	µA
		I_{OUT} = 0mA		2.8	6.0	
		V_{OUT} + 0.5V ≤ V_{IN} ≤ 30V , I_{OUT} = 0mA			7.6	
I_{GND}	Ground current	I_{OUT} = 1mA		16.5	25	µA
I_{GND}	Ground current	V_{IN} = V_{OUT} + 2.0V, I_{OUT} = 300mA			600	µA
$I_{SHUTDOWN}$	Shutdown current	V_{EN} = 0V, T_J = 25℃		0.45		µA
		V_{OUT} + 0.5V ≤ V_{IN} ≤ 30V , V_{EN} = 0V			1.5	
$T_{start\text{-}up}$	Start-up time	V_{IN}, V_{EN} tied together, V_{IN} ramped to $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 0mA		500		µs
I_{EN}	EN pin current	0V ≤ V_{EN} ≤ 30V, V_{IN} and V_{EN} tied together			0.3	µA
		0V ≤ V_{IN} ≤ 30V, V_{EN} = 0V	–0.5			
$V_{IL(EN)}$	EN pin low-level input voltage (disable device)				0.46	V
$V_{IH(EN)}$	EN pin high-level input voltage (enable device)		1.1			
$V_{HYST(EN)}$	EN pin hysteresis (enable device)			0.13		V
PSRR	Power-supply ripple rejection	V_{IN} – V_{OUT} = 3.0V, I_{OUT} = 300mA, f = 100kHz		45		dB
V_n	Output noise voltage	Bandwidth = 10Hz to 100kHz, V_{IN} – V_{OUT} = 3.0V, I_{OUT} = 300mA		650		μV_{RMS}
T_{sd+}	Thermal shutdown temperature increasing	Shutdown, temperature increasing	163			°C
T_{sd-}	Thermal shutdown temperature decreasing	Reset, temperature decreasing	150			°C
$R_{Discharge}$	Output discharge resistance	V_{IN} = 3.0V, V_{EN} = 0V, T_J = 25℃, I_{OUT} = 1mA		780		Ω
I_{SINK}	Sink current on output	V_{OUT} = V_{OUT} × 1.05, T_J = 25℃		3.3		mA

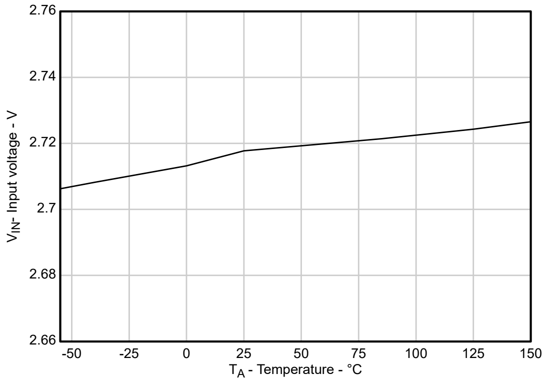
5.6 Typical Characteristics

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 4.7µF, V_{EN} = 2V, and I_{OUT} = 1mA (unless otherwise noted)



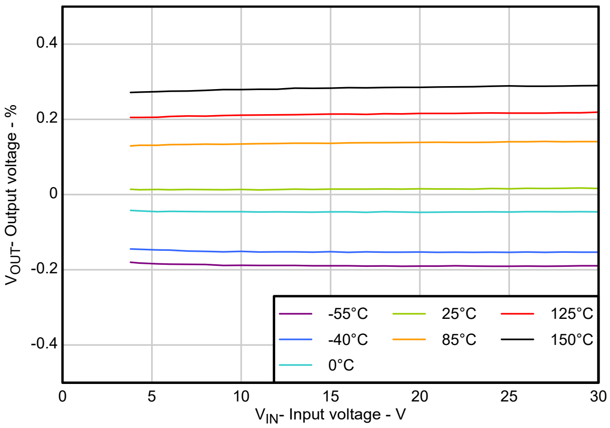
V_{OUT} = 3.3V

Figure 5-1. Rising Input Supply UVLO vs Temperature



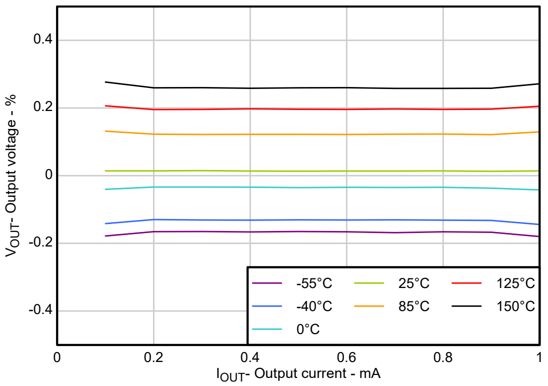
V_{OUT} = 3.3V

Figure 5-2. Falling Input Supply UVLO vs Temperature



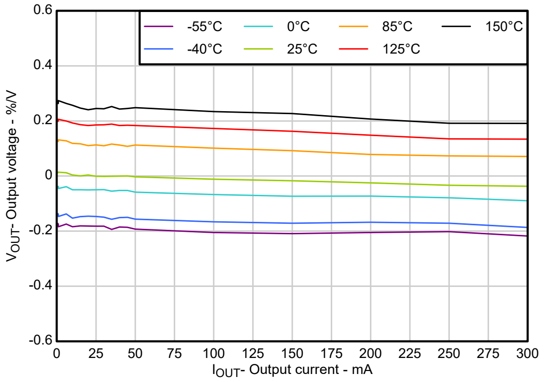
V_{OUT} = 3.3V

Figure 5-3. Accuracy vs Input Voltage



V_{IN} = 3.8V

Figure 5-4. Accuracy vs Output Current



V_{IN} = 5.3V

Figure 5-5. Accuracy vs Output Current

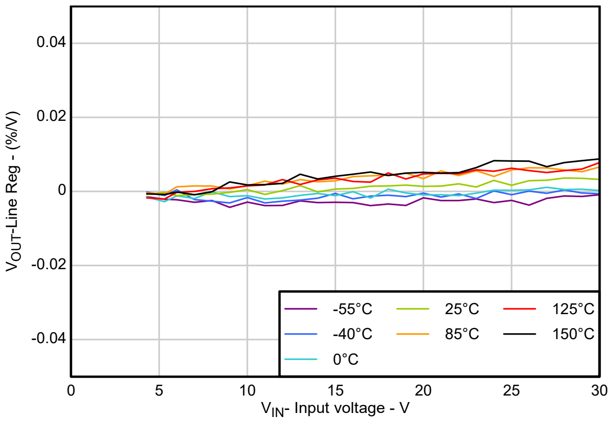


Figure 5-6. Line Regulation vs Input Voltage

5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 4.7µF, V_{EN} = 2V, and I_{OUT} = 1mA (unless otherwise noted)

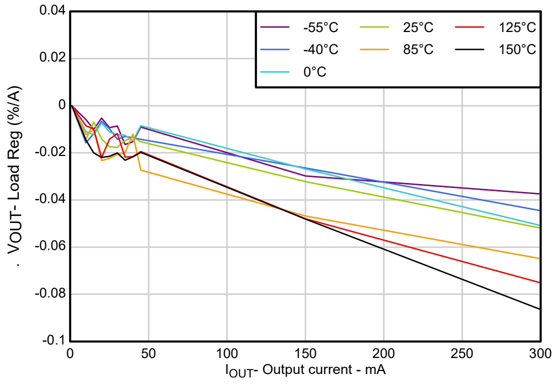


Figure 5-7. Load Regulation vs Output Current

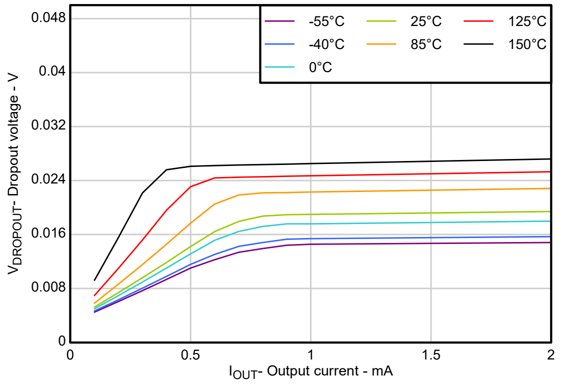


Figure 5-8. Dropout Voltage vs Output Current, Light Loads

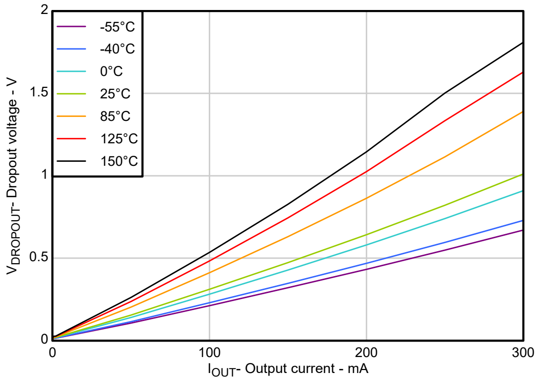
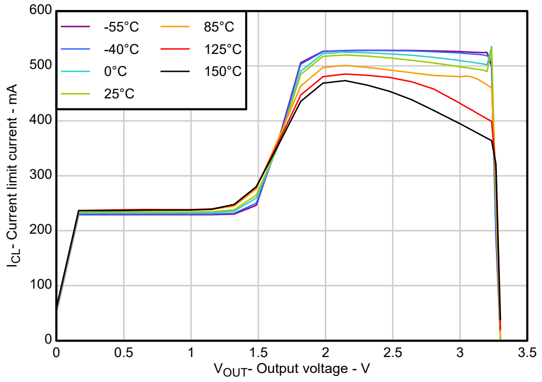
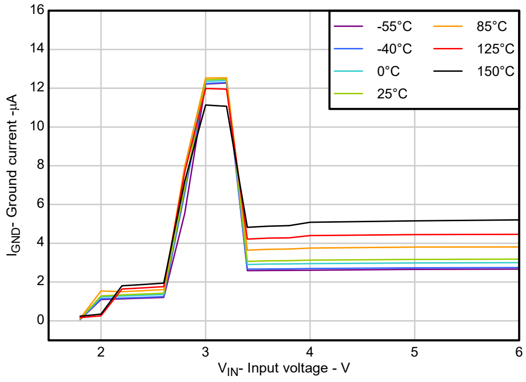


Figure 5-9. Dropout vs Output Current



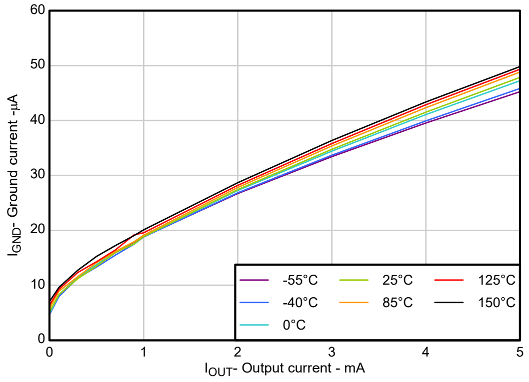
V_{IN} = 5.3V

Figure 5-10. Current Limit vs Output Voltage



I_{OUT} = 0mA

Figure 5-11. Ground Current vs Input Voltage

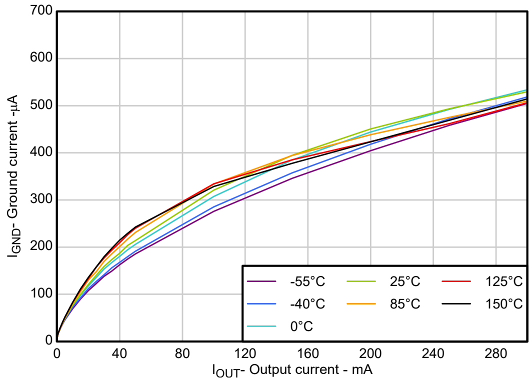


V_{IN} = 3.8V, V_{OUT} = 3.3V

Figure 5-12. Ground Current vs Output Current

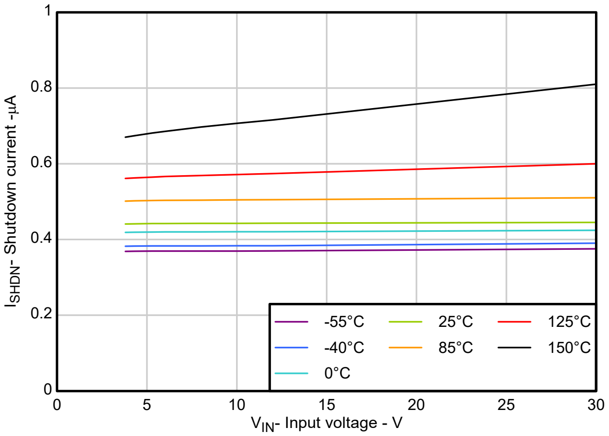
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 4.7µF, V_{EN} = 2V, and I_{OUT} = 1mA (unless otherwise noted)



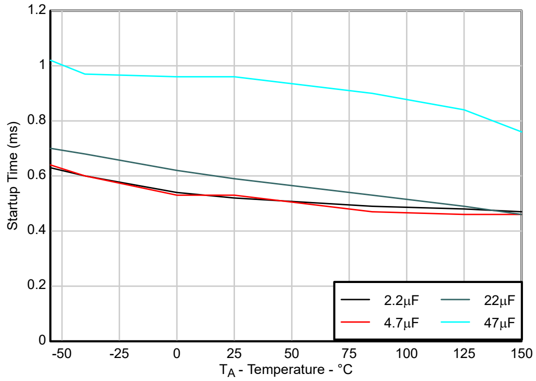
V_{IN} = 5.3V, V_{OUT} = 3.3V

Figure 5-13. Ground Current vs Output Current



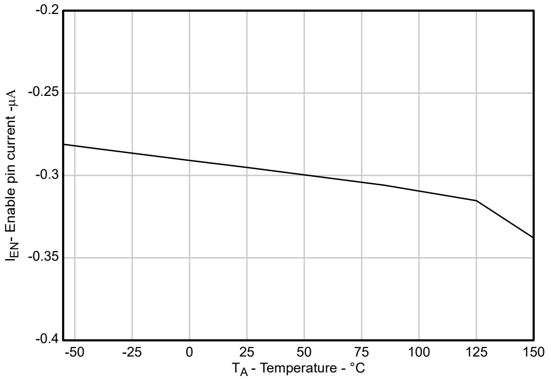
V_{EN} = 0V, I_{OUT} = 0mA

Figure 5-14. Shutdown Current vs Input Voltage



V_{OUT} = 3.3V, I_{OUT} = 0mA

Figure 5-15. Start-up Time vs Temperature, C_{OUT}



I_{OUT} = 0mA

Figure 5-16. Enable Pin Leakage Current vs Temperature

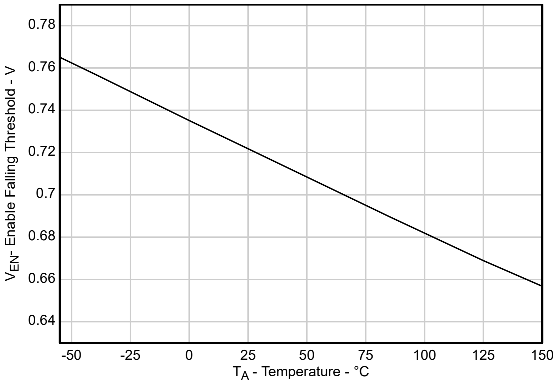


Figure 5-17. Enable Pin Low-Level Input Voltage vs Temperature

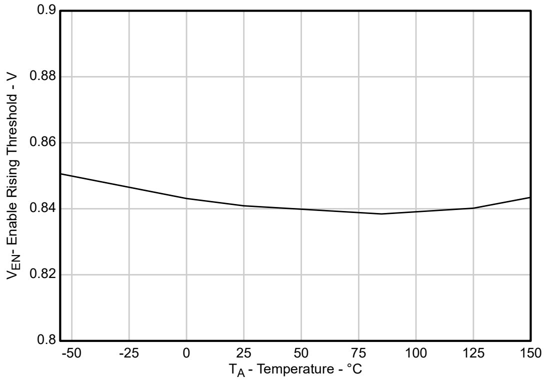
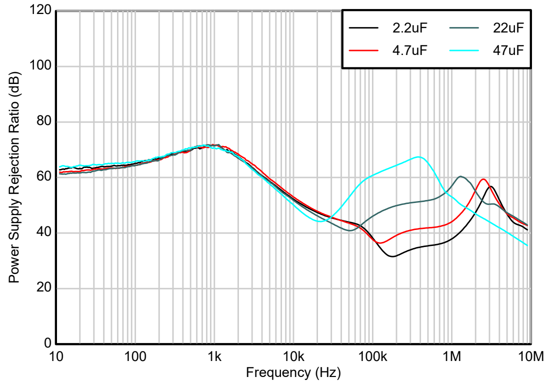


Figure 5-18. Enable Pin High-Level Input Voltage vs Temperature

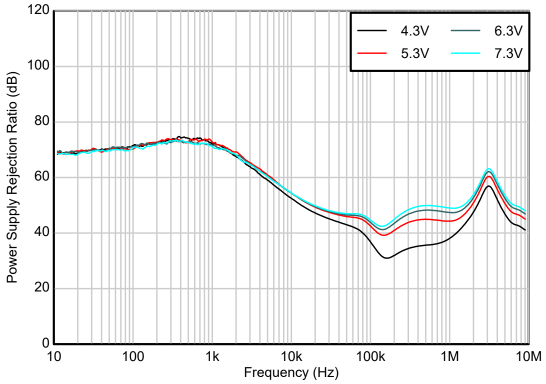
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 4.7µF, V_{EN} = 2V, and I_{OUT} = 1mA (unless otherwise noted)



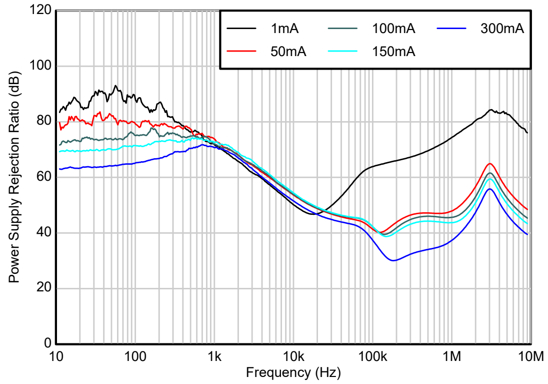
V_{IN} = 5.3V, V_{OUT} = 3.3V, I_{OUT} = 300mA

Figure 5-19. Ripple Rejection vs Frequency, C_{OUT}



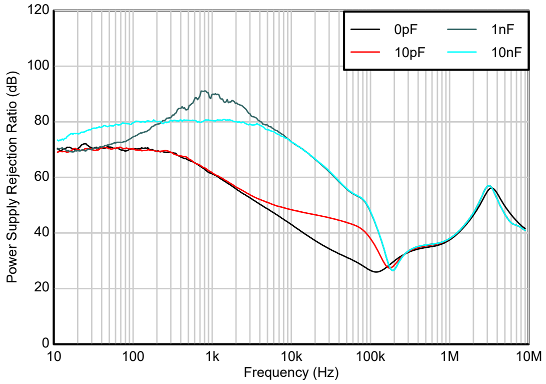
V_{OUT} = 3.3V, I_{OUT} = 150mA

Figure 5-20. Ripple Rejection vs Frequency, Input Voltage



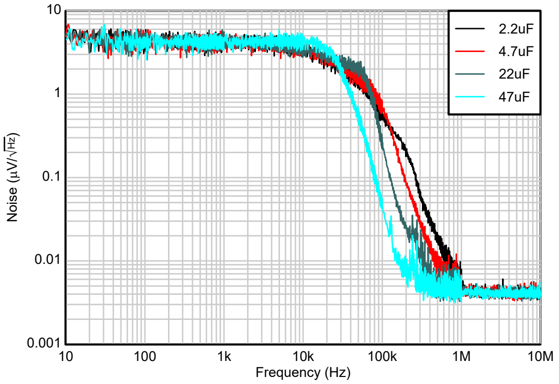
V_{IN} = 5.3V, V_{OUT} = 3.3V

Figure 5-21. Ripple Rejection vs Frequency, Output Current



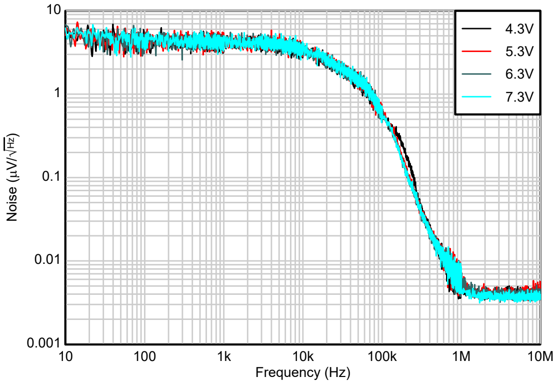
V_{OUT} = 3.3V, I_{OUT} = 150mA

Figure 5-22. Ripple Rejection vs Frequency, C_{FF}



V_{IN} = 5.3V, V_{OUT} = 3.3V, I_{OUT} = 300mA

Figure 5-23. Output Noise vs Frequency, C_{OUT}

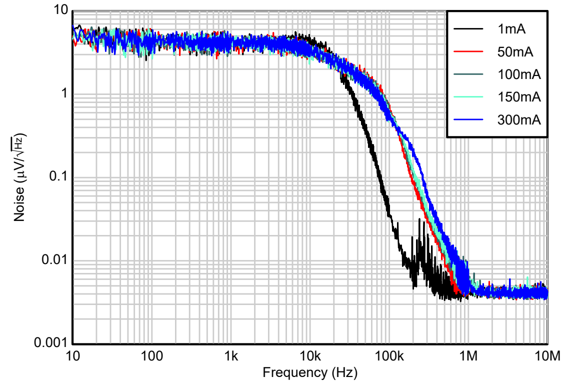


V_{OUT} = 3.3V, I_{OUT} = 150mA

Figure 5-24. Output Noise vs Frequency, Input Voltage

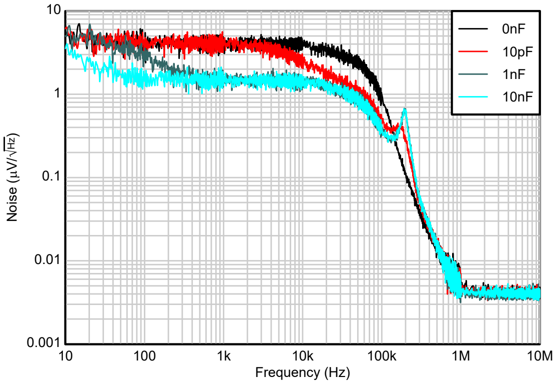
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 4.7µF, V_{EN} = 2V, and I_{OUT} = 1mA (unless otherwise noted)



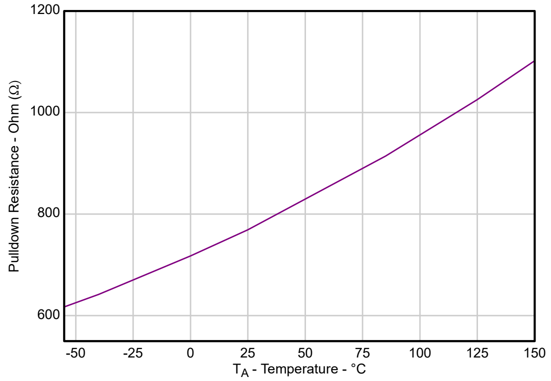
V_{IN} = 5.3V, V_{OUT} = 3.3V

Figure 5-25. Output Noise vs Frequency, Output Current



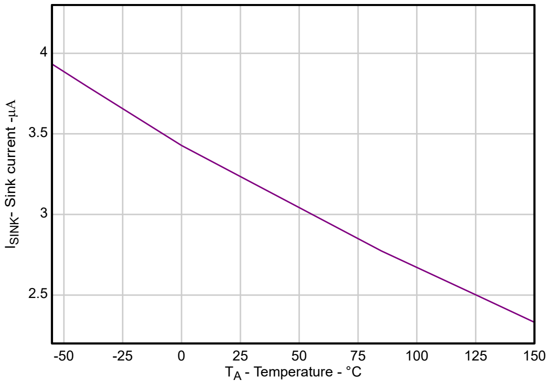
V_{OUT} = 3.3V, I_{OUT} = 150mA

Figure 5-26. Output Noise vs Frequency, C_{FF}



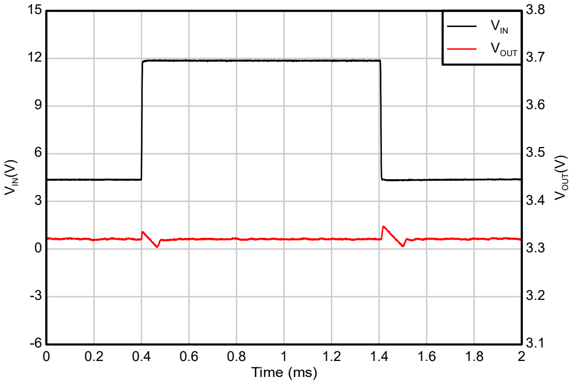
V_{EN} = 0V

Figure 5-27. Output Discharge Resistance vs Temperature



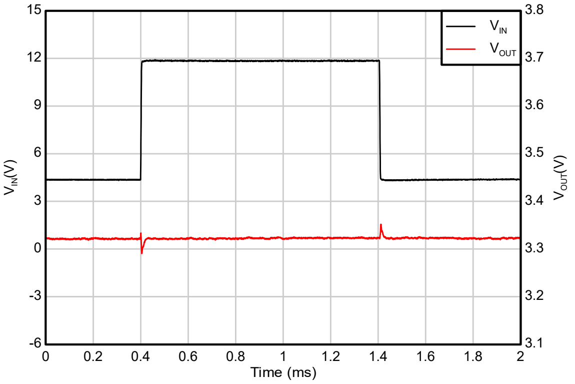
V_{EN} = V_{IN}, V_{OUT} = 1.05 × $V_{OUT(nom)}$

Figure 5-28. Output Sink Current vs Temperature



V_{IN} = 4.3V to 12V, V_{OUT} = 3.3V, slew rate = 2V/µs

Figure 5-29. Line Transient

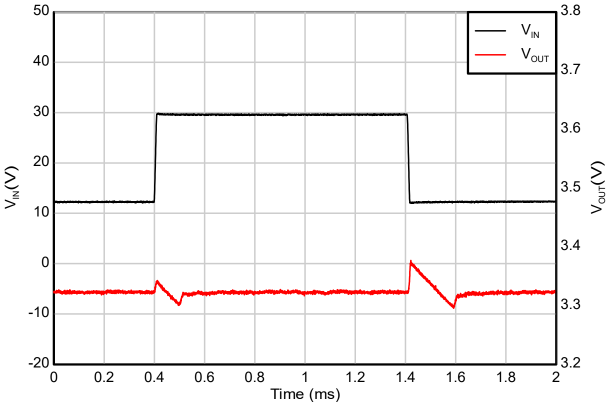


V_{IN} = 4.3V to 12V, V_{OUT} = 3.3V, I_{OUT} = 150mA, slew rate = 2V/µs

Figure 5-30. Line Transient

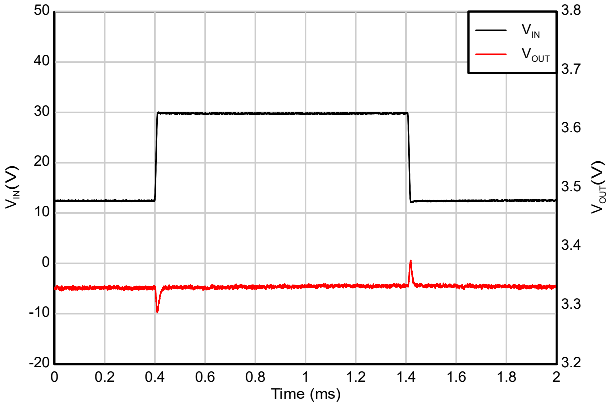
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 4.7µF, V_{EN} = 2V, and I_{OUT} = 1mA (unless otherwise noted)



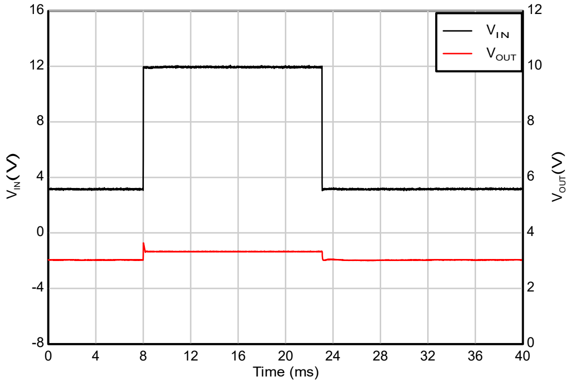
V_{IN} = 12V to 30V, V_{OUT} = 3.3V, slew rate = 2V/µs

Figure 5-31. Line Transient



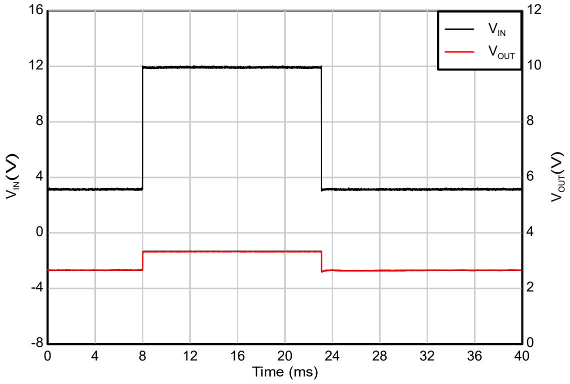
V_{IN} = 12V to 30V, V_{OUT} = 3.3V, I_{OUT} = 150mA, slew rate = 2V/µs

Figure 5-32. Line Transient



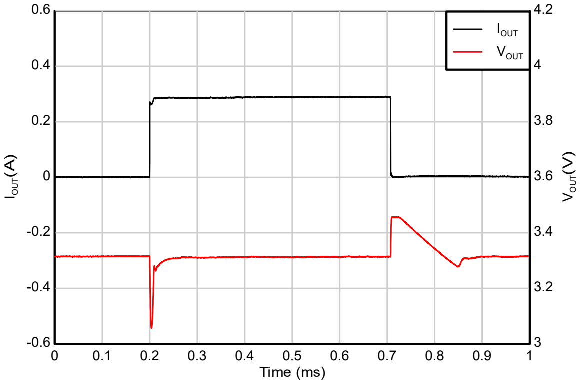
V_{IN} = 3V to 12V, V_{OUT} = 3.3V, slew rate = 2V/µs

Figure 5-33. Cold Crank Recovery



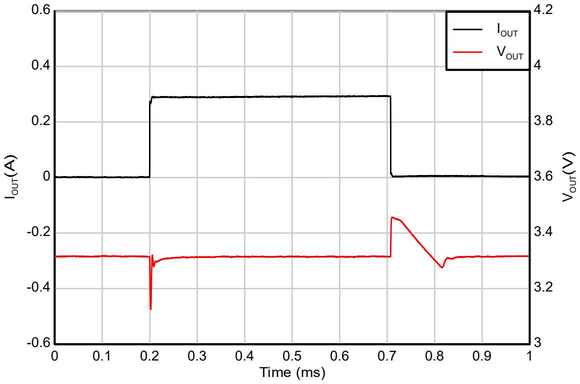
V_{IN} = 3V to 12V, V_{OUT} = 3.3V, I_{OUT} = 150mA, slew rate = 2V/µs

Figure 5-34. Cold Crank Recovery



I_{OUT} = 0mA to 300mA, V_{IN} = 5.3V, V_{OUT} = 3.3V, slew rate = 2A/µs

Figure 5-35. Load Transient

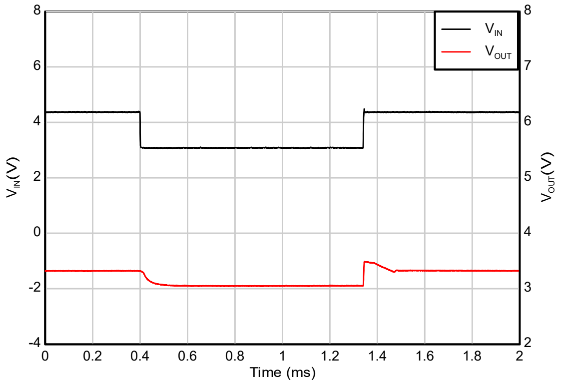


I_{OUT} = 1mA to 300mA, V_{IN} = 5.3V, V_{OUT} = 3.3V, slew rate = 2A/µs

Figure 5-36. Load Transient

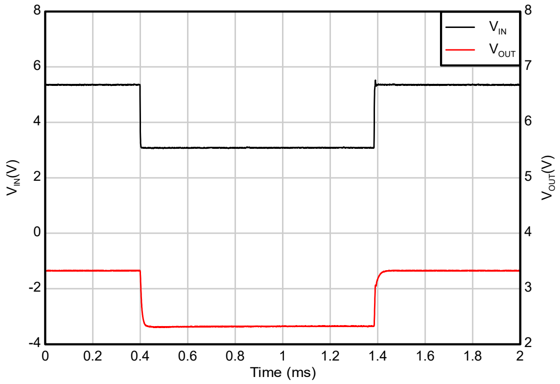
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 4.7µF, V_{EN} = 2V, and I_{OUT} = 1mA (unless otherwise noted)



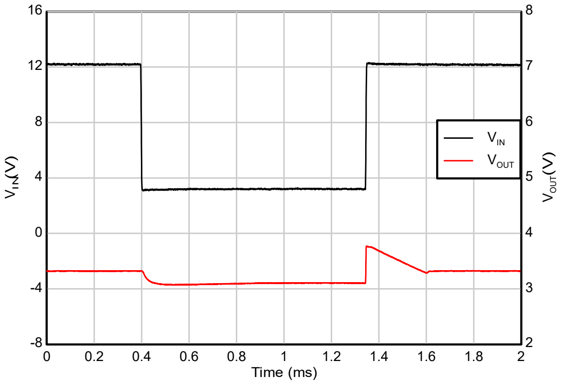
V_{IN} = 4.3V to 3V, V_{OUT} = 3.3V, slew rate = 2V/µs

Figure 5-37. Dropout Recovery



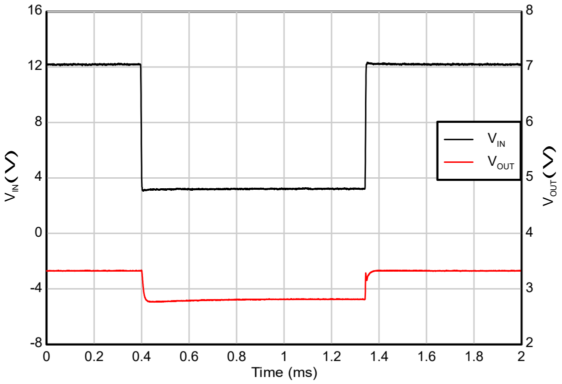
V_{IN} = 5.3V to 3V, V_{OUT} = 3.3V, I_{OUT}= 300mA, slew rate = 2V/µs

Figure 5-38. Dropout Recovery



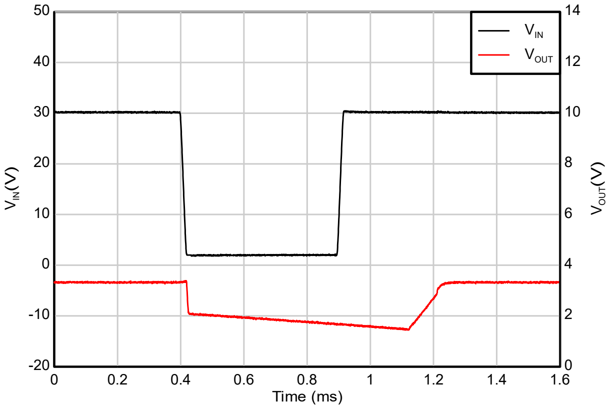
V_{IN} = 12V to 3V, V_{OUT} = 3.3V, slew rate = 2V/µs

Figure 5-39. Dropout Recovery



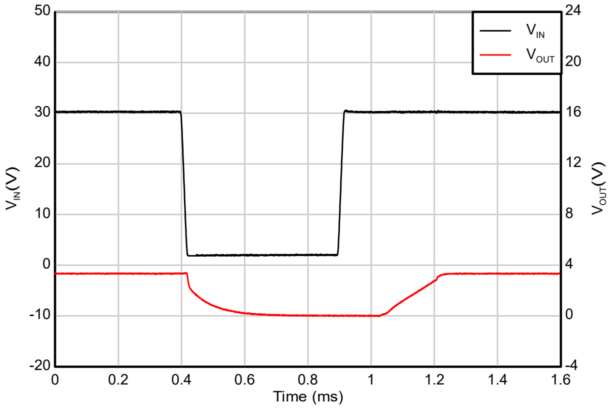
V_{IN} = 12V to 3V, V_{OUT} = 3.3V, I_{OUT}= 100mA, slew rate = 2V/µs

Figure 5-40. Dropout Recovery



V_{IN} = 30V to 2V, V_{OUT} = 3.3V, slew rate = 2V/µs

Figure 5-41. Brownout Recovery

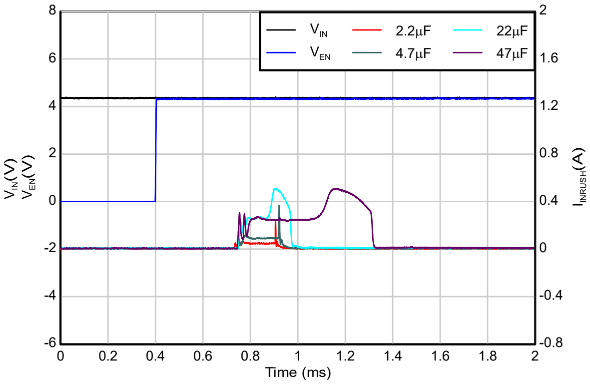


V_{IN} = 30V to 2V, V_{OUT} = 3.3V, I_{OUT}= 50mA, slew rate = 2V/µs

Figure 5-42. Brownout Recovery

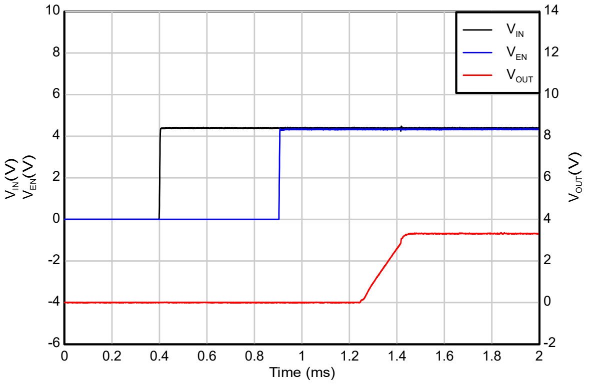
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 4.7µF, V_{EN} = 2V, and I_{OUT} = 1mA (unless otherwise noted)



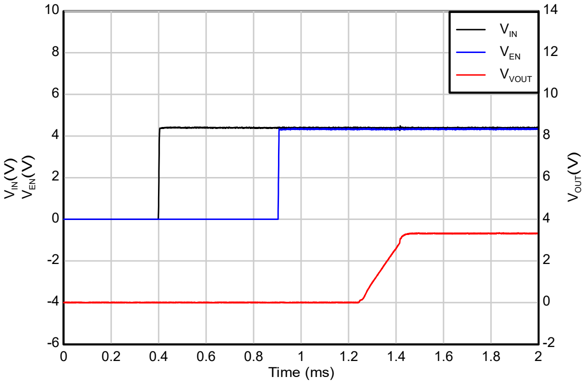
V_{OUT} = 3.3V, I_{OUT} = 0mA, slew rate = 1V/µs

Figure 5-43. Start-up Inrush Current



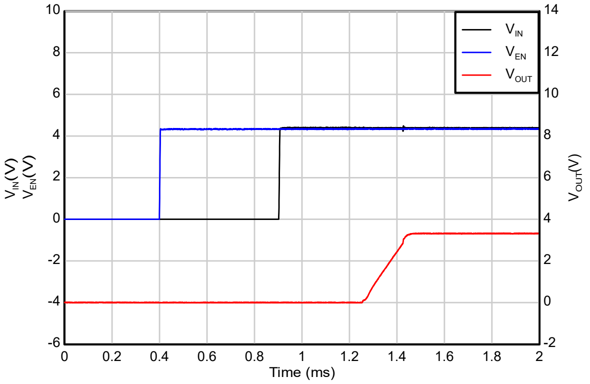
V_{OUT} = 3.3V, slew rate = 1V/µs

Figure 5-44. Start-up With Sequencing (EN after IN)



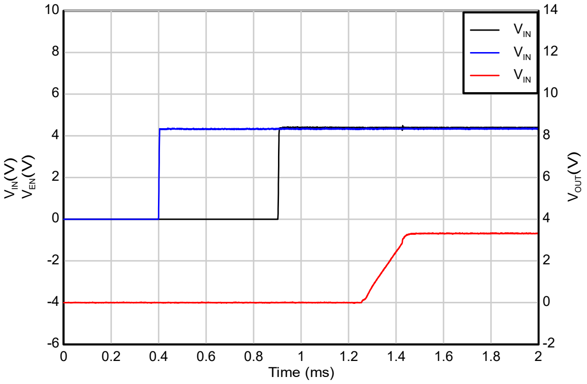
V_{OUT} = 3.3V, I_{OUT} = 50mA, slew rate = 1V/µs

Figure 5-45. Start-up With Sequencing (EN after IN)



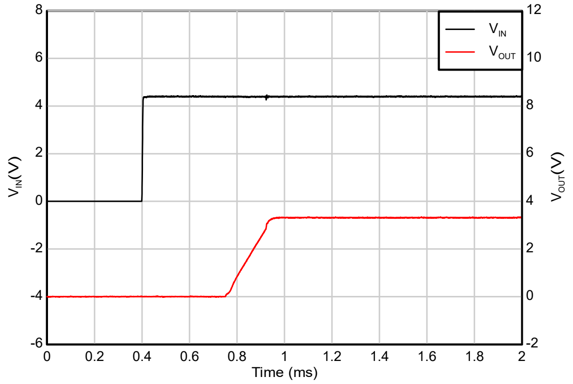
V_{OUT} = 3.3V, slew rate = 1V/µs

Figure 5-46. Start-up With Sequencing (IN after EN)



V_{OUT} = 3.3V, I_{OUT} = 50mA, slew rate = 1V/µs

Figure 5-47. Start-up With Sequencing (IN after EN)

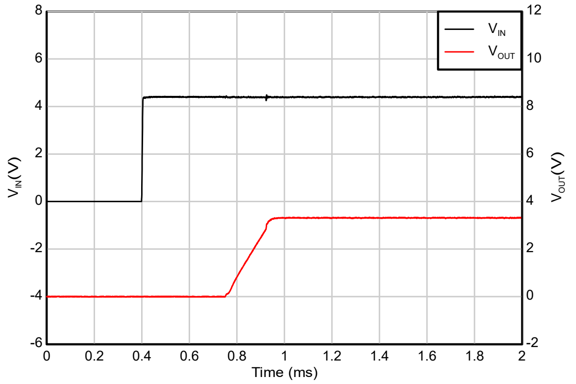


V_{EN} = V_{IN}, V_{OUT} = 3.3V, slew rate = 1V/µs

Figure 5-48. Start-up With IN and EN Tied Together

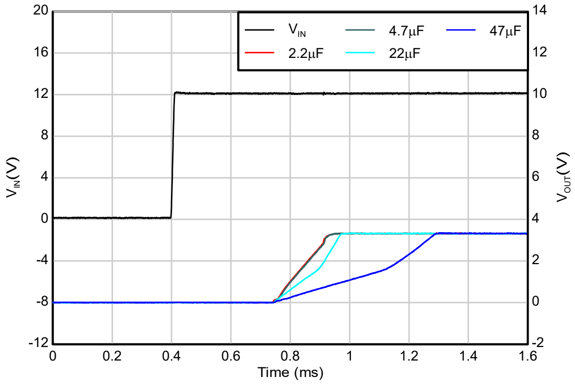
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or $V_{IN} = V_{OUT}(nom)$ + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 4.7µF, V_{EN} = 2V, and I_{OUT} = 1mA (unless otherwise noted)



$V_{EN} = V_{IN}$, V_{OUT} = 3.3V, I_{OUT} = 50mA, slew rate = 1V/µs

Figure 5-49. Start-up With IN and EN Tied Together



$V_{EN} = V_{IN}$, V_{OUT} = 3.3V, slew rate = 1V/µs

Figure 5-50. Start-up With IN and EN Tied Together, C_{OUT}

6 Detailed Description

6.1 Overview

The TPS7E72 low-dropout regulator (LDO) consumes ultra-low quiescent current (2.8µA (typ)) at no-load current. The device offers a wide input voltage range (3.0V to 30V) and wide output range (1.2V to 28V, in adjustable configuration) and supports up to 300mA of load current. The device is stable with the output capacitor range of 4.7µF to 100µF.

The low quiescent current across the complete load current range and controlled I_Q in no-load dropout situations makes the TPS7E72 designed for powering battery-operated applications. The TPS7E72 has an internal soft-start mechanism that provides a uniform start-up with controlled inrush current. This LDO also has over-current (fold-back), over-power and thermal protection during a load-short or fault condition on the output for better reliability.

6.2 Functional Block Diagrams

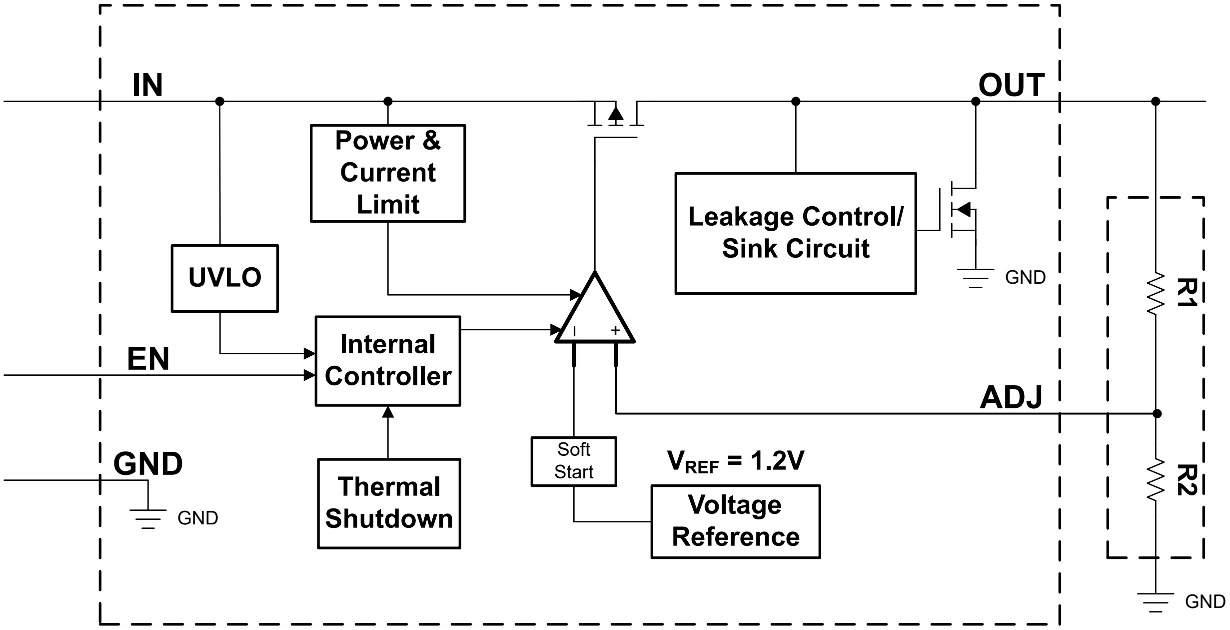


Figure 6-1. Functional Block Diagram: Adjustable Version

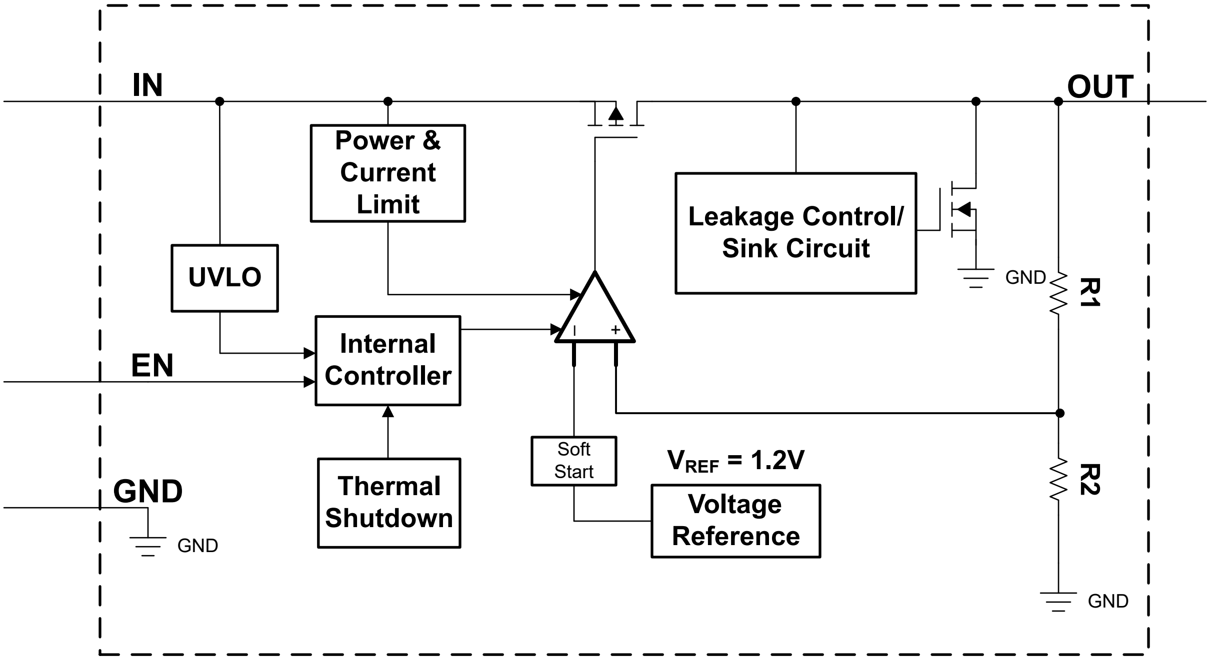


Figure 6-2. Functional Block Diagram: Fixed Version

6.3 Feature Description

6.3.1 Enable (EN)

The enable pin for the device is an active-high pin. The output voltage is enabled when the voltage of the enable pin is greater than the high-level input voltage (V_{IH}) of the EN pin and disabled with the enable pin voltage is less than the low-level input voltage (V_{IL}) of the EN pin. High and low thresholds are listed in *Electrical Characteristics*. If independent control of the output voltage is not needed, connect the enable pin to the input of the device.

The EN pin also has a weak internal pull-up and the EN pin can be left floating to enable the device. The internal pull-up current on the EN pin is captured in then *Electrical Characteristics* table as Enable pull-up current. However, care must be taken to verify that pin leakage (from board pollution or some other source) does not inadvertently pull this pin low. Leakage must be restricted to 25nA or less to avoid unintentional disabling of the device.

6.3.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage (V_{IN} – V_{OUT}) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

6.3.3 Undervoltage Lockout

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has in-built hysteresis. The UVLO limits are specified in the *Electrical Characteristics* table.

6.3.4 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to T_{SD+} (typical). Thermal shutdown hysteresis verifies that the device resets (turns on) when the temperature falls to T_{SD-} (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed the operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.3.5 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Section 5.5* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{CL}$]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{SC}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-3 shows a diagram of the foldback current limit.

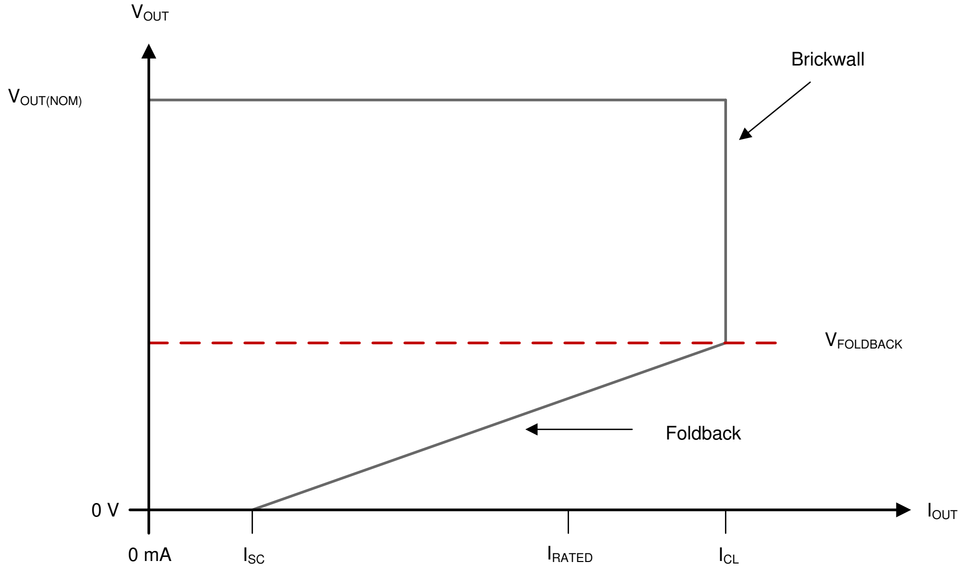


Figure 6-3. Foldback Current Limit

6.3.6 Power Limit

The device has an internal over-power limit circuit that limits the power dissipated across the LDO within the internal SOA (safe operating area) limits. The SOA limits for the LDO factor in safe operation for both silicon components and bondwires used in packaging. These limits verify reliable operation of the device and prevent the device failure from overheating, breakdown, or other damaging effects.

The power dissipated (P_{Dissip}) across the LDO is defined by voltage drop across LDO (V_{IN} - V_{OUT}) and load current (I_{OUT}) flowing through.

$$P_{Dissip} = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{2}$$

The power limiting circuit monitors both the voltage drop (headroom, V_{IN} - V_{OUT}) across LDO and output load current (I_{OUT}) flowing through. If P_{Dissip} crosses the defined SOA limits, the power limiting circuit limits the load current (I_{OUT}) flowing through. The output voltage is not regulated when the device is in power limit operation. The maximum supported current (I_{PLIMIT}) at full headroom (V_{IN} - V_{OUT} = 30V) and maximum supported headroom ($V_{HEADROOM}$) at full load current are captured in Section 5.5.

Figure 6-4 shows a diagram of the power limiting.

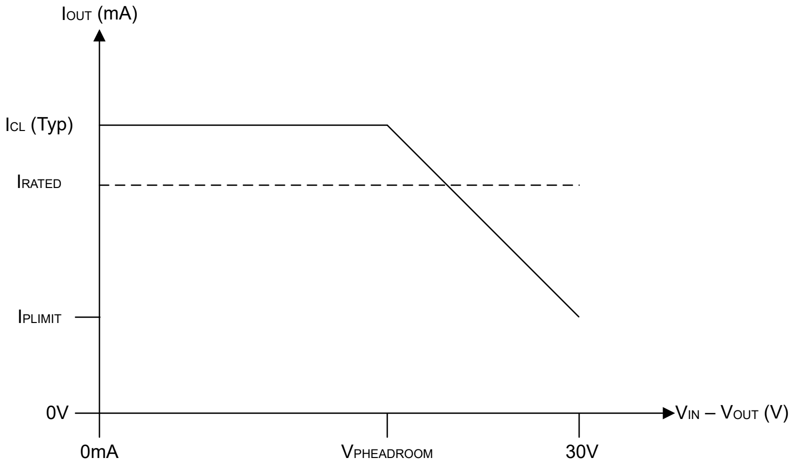


Figure 6-4. Power Limiting

6.3.7 Output Pulldown

The device has an output pulldown circuit. V_{OUT} pulldown sink to ground capability is listed in the *Electrical Characteristics* table. The output pulldown activates under the following conditions:

- $V_{EN} < V_{IL(EN)}$
- $1.0V < V_{IN} < V_{UVLO}$

The output pulldown resistance for this device is 780Ω typical, listed as $R_{Discharge}$ in the *Electrical Characteristics* table.

Do not rely on the output pulldown circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input. This reverse current flow can cause damage to the device. See the *Reverse Current* section for more details.

6.4 Device Functional Modes

6.4.1 Device Functional Mode Comparison

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Section 5.5* table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.2 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The headroom across the LDO (V_{IN} - V_{OUT}) is less than $V_{HEADROOM}$ for required I_{OUT}, such that power limit is not engaged
- The output current is less than the current limit ($I_{OUT} < I_{LIM}$)
- The device junction temperature is within the range given in the *Recommended Operating Conditions* table.
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

6.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

The TPS7E72 keeps the I_Q controlled in dropout operation to much lower values (12μA (typ) in no-load dropout) compared to conventional linear voltage regulators. This avoids battery drainage in cases which the battery level falls below the input voltage level required for the TPS7E72 to regulate.

6.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage, $V_{IL(EN)}$ (see *Electrical Characteristics*). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Adjustable Device Feedback Resistor Selection

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2, according to the following equation:

$$V_{OUT} = V_{ADJ} \times (1 + R_1 / R_2) \tag{3}$$

V_{ADJ} (or V_{FB}) is the feedback voltage and refers to the voltage on the ADJ pin. During normal operation of the adjustable device, the device regulates such that that V_{ADJ} is equal to the internal reference voltage of the device.

To ignore the feedback pin current error term in the V_{OUT} equation, set the feedback divider current to 100x the feedback pin current (I_{ADJ}) listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \le V_{OUT} / (I_{ADJ} \times 100) \tag{4}$$

7.1.2 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a general rule, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

7.1.3 Input and Output Capacitor Selection

The TPS7E72 requires an output capacitor of 4.7μF or larger (2.2μF or larger capacitance) for stability and an equivalent series resistance (ESR) between 0.0Ω and 1.0Ω. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitor is 100μF.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

7.1.4 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3V$.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

Figure 7-1 shows one approach for protecting the device.

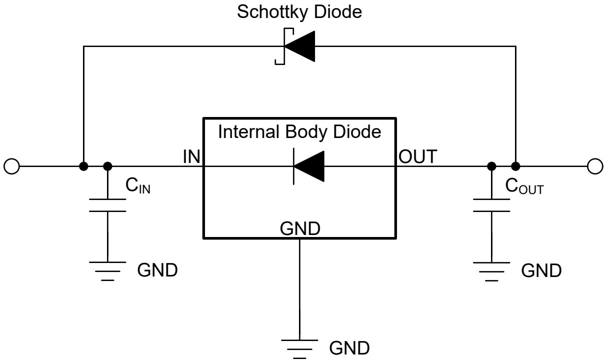


Figure 7-1. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.1.5 Feed-Forward Capacitor

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the ADJ pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. A higher capacitance C_{FF} can be used; however, the start-up time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

C_{FF} and R_1 form a zero in the loop gain at frequency f_Z, while C_{FF}, R_1, and R_2 form a pole in the loop gain at frequency f_P. C_{FF} zero and pole frequencies can be calculated from the following equations:

$$f_Z = 1 / (2 \times \pi \times C_{FF} \times R_1) \quad (5)$$

$$f_P = 1 / (2 \times \pi \times C_{FF} \times (R_1 \parallel R_2)) \quad (6)$$

7.1.6 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (7)$$

7.1.7 Estimating Junction Temperature

The JEDEC standard now recommends using psi (Ψ) thermal metrics to estimate the LDO junction temperatures when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with Equation 8 and are given in the *Section 5.5* table.

$$\begin{aligned}&\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D\\&\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D\end{aligned} \quad (8)$$

where:

- P_D is the power dissipated as explained in Equation 11
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

The JEDEC standard now recommends using psi (Ψ) thermal metrics to estimate the linear regulator junction temperatures when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the printed circuit board (PCB) surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (9)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (10)$$

where:

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use the metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

7.1.8 Power Dissipation (P_D)

Circuit reliability requires proper consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. Verify the PCB area around the regulator has few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (11)$$

Note

Power dissipation is minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. Power dissipation and junction temperature are most often related by the $R_{\theta JA}$ of the combined PCB and device package and the T_A. $R_{\theta JA}$ is the junction-to-ambient thermal resistance and T_A is the temperature of the ambient air. The following equation describes this relationship.

$$T_J = T_A + (R_{\theta JA} \times P_D) \tag{12}$$

The following equation rearranges this relationship for output current.

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \tag{13}$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design. This resistance therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area. $R_{\theta JA}$ is used as a relative measure of package thermal performance. For packages with thermal pad and a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package's $R_{\theta JCbot}$ plus the thermal resistance contribution by the PCB copper. $R_{\theta JCbot}$ is the junction-to-case (bottom) thermal resistance, as given in the *Thermal Information* table.

7.1.9 Power Dissipation Versus Ambient Temperature

Figure 7-2 and Figure 7-3 are based off of a JESD51-7 4-layer, high-K board. The allowable power dissipation is estimated using the following equation. As discussed in the *An empirical analysis of the impact of board layout on LDO thermal performance* application note, thermal dissipation can be improved in the JEDEC high-K layout by adding top layer copper and increasing the number of thermal vias. If a good thermal layout is used, the allowable thermal dissipation can be improved by up to 50%. Maintain the junction temperature of the device within recommended operating temperature range to maximize device lifetime and reliability, see the *Recommended Operating Conditions*.

$$T_A + R_{\theta JA} \times P_D \le T_J(\text{max}) \tag{14}$$

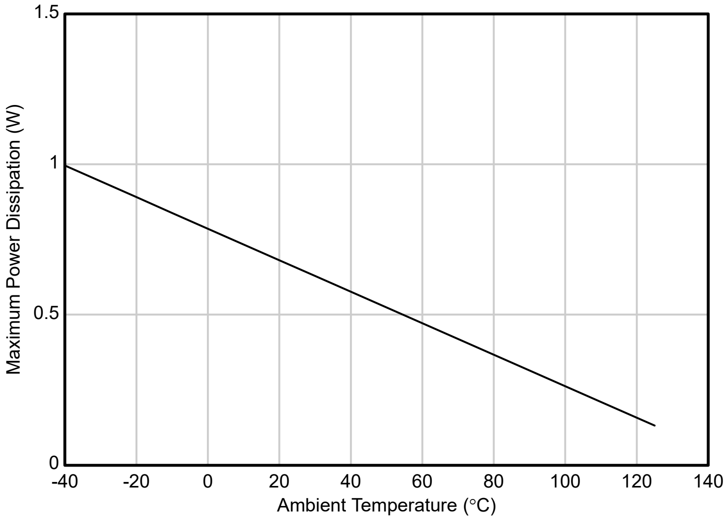


Figure 7-2. TPS7E72 (DBV) Allowable Power Dissipation

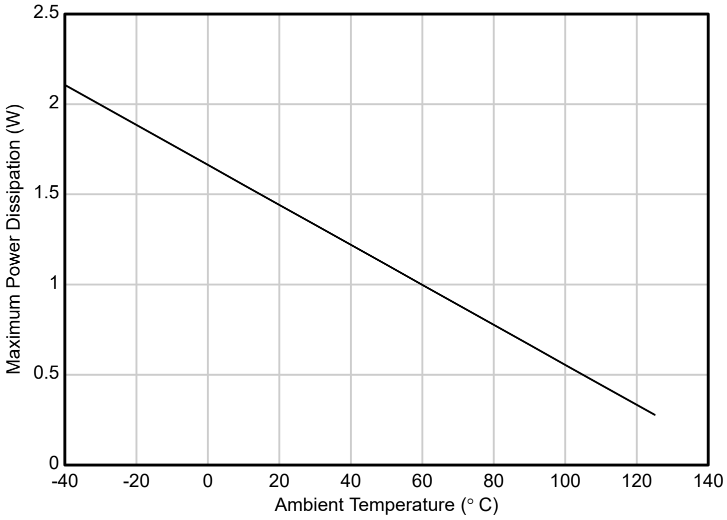


Figure 7-3. TPS7E72 (DRV) Allowable Power Dissipation

7.2 Typical Application

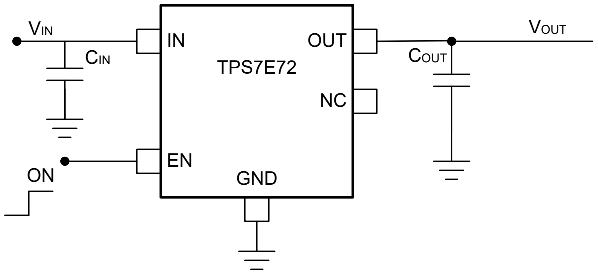


Figure 7-4. TPS7E72 Typical Application Circuit (Fixed-Voltage Version)

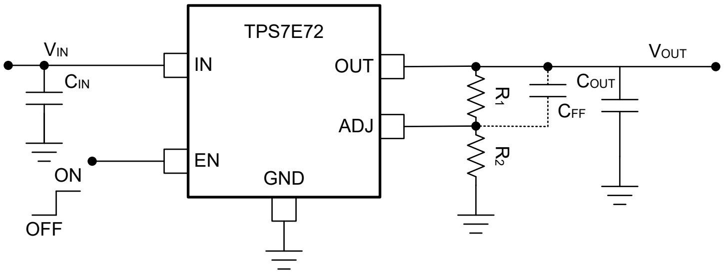


Figure 7-5. TPS7E72 Adjustable LDO Regulator Programming

NOTE: Dotted lines indicate an optional input capacitor and feed-forward capacitor. See the *Input and Output Capacitor Selection* and *Feed-Forward Capacitor* sections and the *Recommended Operating Conditions* table.

Table 7-1. Adjustable Output Voltage for Resistors R_1 and R_2

OUTPUT VOLTAGE (V)	R_1 (MΩ)	R_2 (MΩ)
1.8	0.499	1
2.8	1.33	1
5.0	3.16	1

7.2.1 Design Requirements

For this design example, use the parameters listed in Table 7-2 as the input parameters.

Table 7-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	6V to 30V
Output voltage	3.3V
Output current	150mA
Output capacitor	4.7µF

7.2.2 Detailed Design Procedure

For this design example, a nominal 6.0V input supply is assumed, with line transients up to 30V expected. Use a nominal 0.47µF input capacitor to minimize the effect of resistance and inductance between the 6.0V source and LDO input. Use a nominal 4.7µF output capacitor (minimum 2.2µF output capacitance) for stability and good load transient response.

If using the adjustable version of the device, refer to the *Choose Feedback Resistors* section and Design Parameters for guidance setting the output voltage.

Operating at a 3.3V output voltage and 150mA output current, the dropout voltage (V_{DO}) of the device is 900mV maximum. Given that the 6.0V input voltage source is >4.2V, there is no concern maintaining headroom.

The expected line transients of up to 30V are within the rated input voltage of the device.

7.2.2.1 Choose Feedback Resistors

For this design example, V_{OUT} is set to 3.3V. The following equations set the feedback divider resistors for the desired output voltage:

$$V_{OUT} = V_{ADJ} \times (1 + R_1 / R_2) \quad (15)$$

$$R_1 + R_2 \leq V_{OUT} / (I_{ADJ} \times 100) \quad (16)$$

For improved output accuracy, use Equation 16 and I_{ADJ} = 10nA as listed in the *Section 5.5* table to calculate the upper limit for series feedback resistance ($R_1 + R_2 \leq 3.3M\Omega$).

The control-loop error amplifier drives the ADJ pin to the same voltage as the internal reference (V_{ADJ} = 1.2V, as listed in the *Section 5.5* table). Use Equation 15 to determine the ratio of R_1 / R_2 = 1.75 Use this ratio and solve Equation 16 for R_1. Now calculate the upper limit for $R_1 \leq 2.1M\Omega$. Select a standard value resistor for R_1 = 1.75MΩ.

Reference Equation 17 and solve for R_2:

$$R_2 = R_1 / [(V_{OUT} / V_{ADJ}) - 1] \tag{17}$$

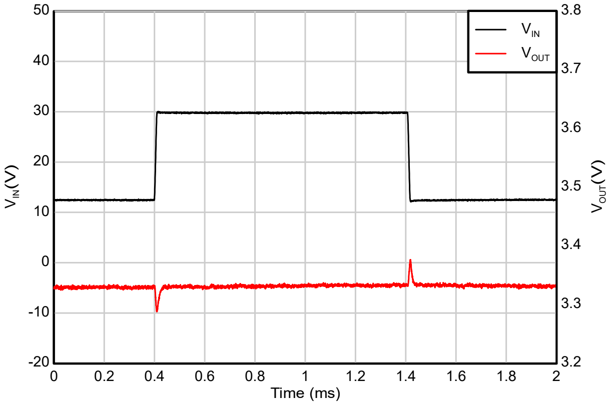
From Equation 17, R_2 = 1MΩ is determined. Select a standard value resistor for R_2 = 1MΩ. Verify that the feedback divider current is greater than the minimum value in the *Recommended Operating Conditions* table.

The following equation calculates the feedback divider current.

$$I_{FB\_Divider} = V_{OUT} / (R_1 + R_2) \tag{18}$$

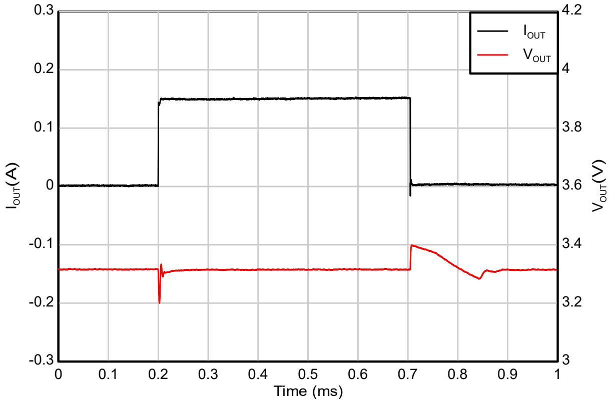
7.2.2.2 Application Curves

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 4.7µF, V_{EN} = 2V, and I_{OUT} = 1mA (unless otherwise noted)



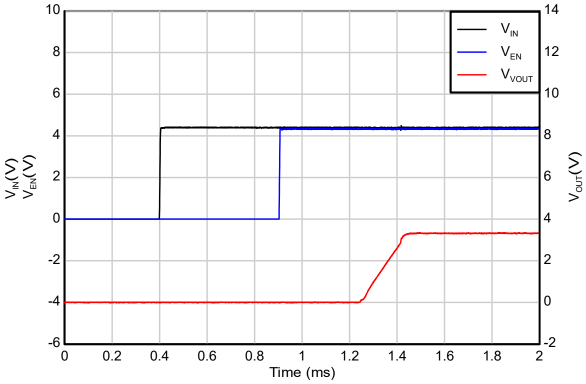
V_{IN} = 12V to 30V, V_{OUT} = 3.3V, I_{OUT} = 150mA, slew rate = 2V/µs

Figure 7-6. Line Transient



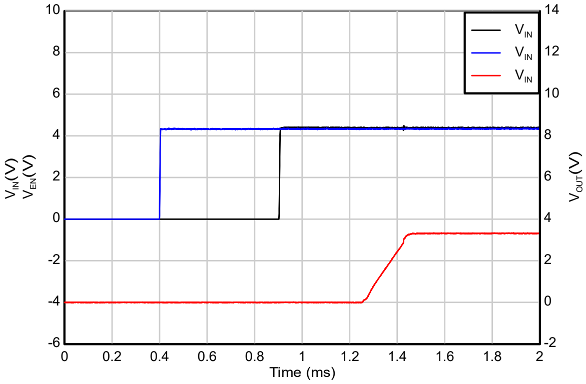
I_{OUT} = 1mA to 150mA, V_{OUT} = 3.3V, slew rate = 2A/µs

Figure 7-7. Load Transient



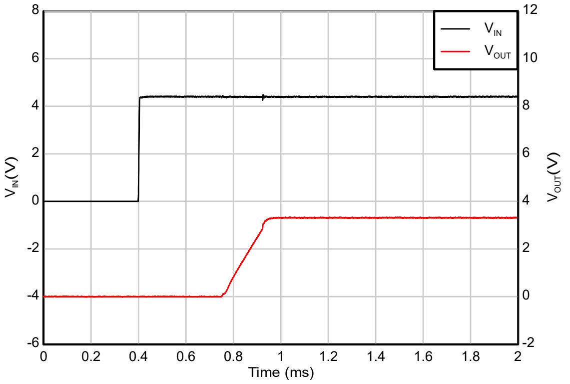
V_{OUT} = 3.3V, I_{OUT} = 50mA, slew rate = 1V/µs

Figure 7-8. Start-up With Sequencing (EN after IN)



V_{OUT} = 3.3V, I_{OUT} = 50mA, slew rate = 1V/µs

Figure 7-9. Start-up With Sequencing (IN after EN)



V_{EN} = V_{IN}, V_{OUT} = 3.3V, I_{OUT} = 50mA, slew rate = 1V/µs

Figure 7-10. Start-up With IN and EN Tied Together

7.2.3 Power Supply Recommendations

The TPS7E72 is designed to operate from an input voltage supply range between 3.0V and 30V. The input voltage range provides adequate headroom for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR help improve output noise performance.

7.2.4 Layout

7.2.4.1 Layout Guidelines

For best overall performance, follow the guidelines in this section. Place all circuit components on the same side of the printed circuit board (PCB) and as near as practical to the respective LDO pin connections. Place ground return connections for the input and output capacitors as close to the GND pin as possible, using wide, component-side, copper planes. Do not use vias and long traces to create LDO circuit connections to the input capacitor, output capacitor, or resistor divider. This practice negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is embedded in the PCB or located on the bottom side of the PCB opposite the components. This reference plane serves to provide accuracy of the output voltage and shield the LDO from noise. To improve the thermal performance of the device, and to maximize the current output at high ambient temperature, spread the copper under the thermal pad as far as possible and place enough thermal vias on the copper under the thermal pad.

7.2.4.2 Layout Example

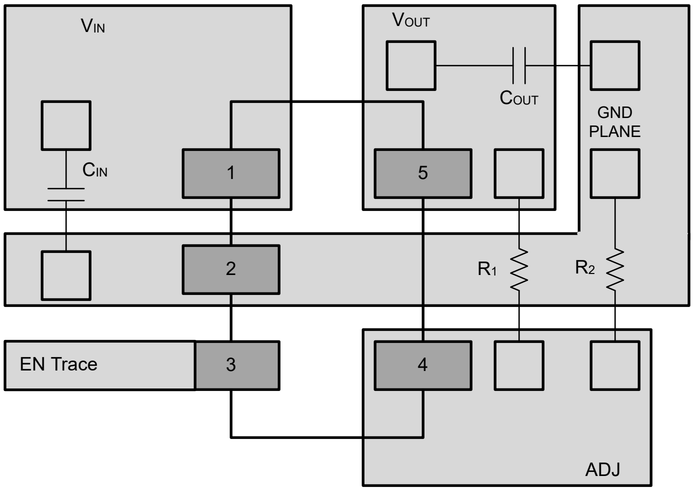


Figure 7-11. Example Layout for TPS7E72 DBV Package

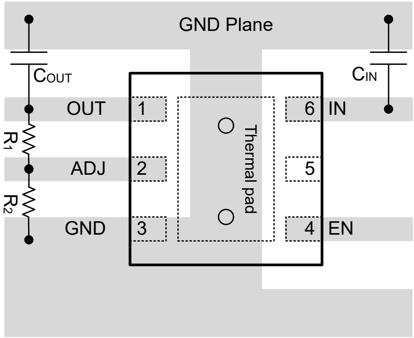


Figure 7-12. Example Layout for TPS7E72 DRV Package

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed in this section.

8.1 Device Support

8.1.1 Development Support

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS7E72. The Universal EVM (and related user's guide) can be requested at the TI website through the product folders or purchased directly from the TI eStore.

8.1.2 Device Nomenclature

Table 8-1. Device Nomenclature

PRODUCT[1]	DESCRIPTION
TPS7E72 **xx (M) yyy z**	**xx** is the nominal output voltage. For example, 33 = 3.3V, 50 = 5.0V, 01 = Adjustable. **yyy** is the package designator. For example, DBV = SOT-23, DRV = WSON. **(M)** indicates that a device is qualified to extended temperature range. See the *Recommended Operating Conditions*. **z** indicates the package quantity. R is for large reel (3000 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *An empirical analysis of the impact of board layout on LDO thermal performance* application note
- Texas Instruments, *Know Your Limits* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2026	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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