

# TPSM852892 36V, 6A, Fully Integrated Buck-boost Power Module with ZEN 2 Switcher Technology

## 1 Features

- **ZEN 2 Switcher**
  - Facilitates CISPR 32 class B compliance
  - Integrated VIN, VOUT, BOOT1 and BOOT2 bypass capacitors to reduce EMI
  - Optimized pinout for minimal loop inductance
  - Optional programmable spread spectrum
  - Fix-frequency control with programmable switching frequency
- Wide input and output voltage range
  - Wide input voltage range: 3.0V to 36V
  - Programmable output voltage range: 0.8V to 22V
  - $\pm 1\%$  reference voltage accuracy
  - Adjustable output voltage compensation for voltage droop over the cable
  - $\pm 5\%$  accurate output current monitoring
- High efficiency over entire load range
  - 96% efficiency at  $V_{IN} = 12V$ ,  $V_{OUT} = 20V$  and  $I_{OUT} = 2.5A$
  - Programmable PFM and FPWM mode at light load
- Avoid frequency interference and crosstalk
  - Optional clock synchronization
  - Programmable switching frequency from 400kHz to 1MHz
- Rich protection features
  - Output overvoltage protection
  - Hiccup mode for output short-circuit protection
  - Thermal shutdown protection
  - 6A average inductor current limit
- Small solution size
  - 7.5mm  $\times$  7.7mm  $\times$  3.8mm QFN package

## 2 Applications

- **Laser distance meter**
- **Powered surgical tools**
- **Parametric measurement unit (PMU)**

## 3 Description

The TPSM852892 is a buck-boost module that is optimized for converting battery voltage or adapter voltage into power supply rails. The TPSM852892 integrates four MOSFET switches and one power inductor providing a compact solution for a variety of applications. The TPSM852892 has up to 36V input voltage capability. When working in boost mode, the TPSM852892 can deliver 50W from a 12V input.

The TPSM852892 employs an average current-mode control scheme. The switching frequency is programmable from 400kHz to 1MHz by an external resistor and can be synchronized to an external clock. The TPSM852892 also provides optional spread spectrum to minimize peak EMI.

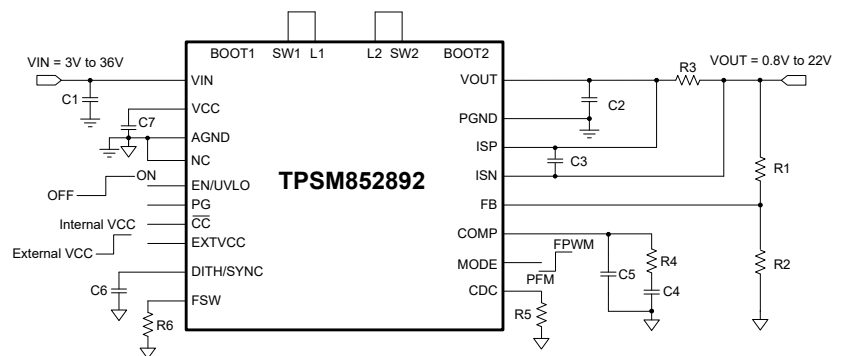
The TPSM852892 offers output over-voltage protection, average inductor current limit, cycle-by-cycle peak current limit, output short circuit protection. The TPSM852892 also specifies safe operating with optional output current limit and hiccup-mode protection in sustained overload conditions.

The TPSM852892 is designed with ZEN 2 switcher technology to quickly and easily implement a low-EMI design and offers a small solution size with 7.5mm  $\times$  7.7mm QFN package.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE
TPSM852892	RCM (QFN-FCMOD, 71)	7.5mm $\times$ 7.7mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



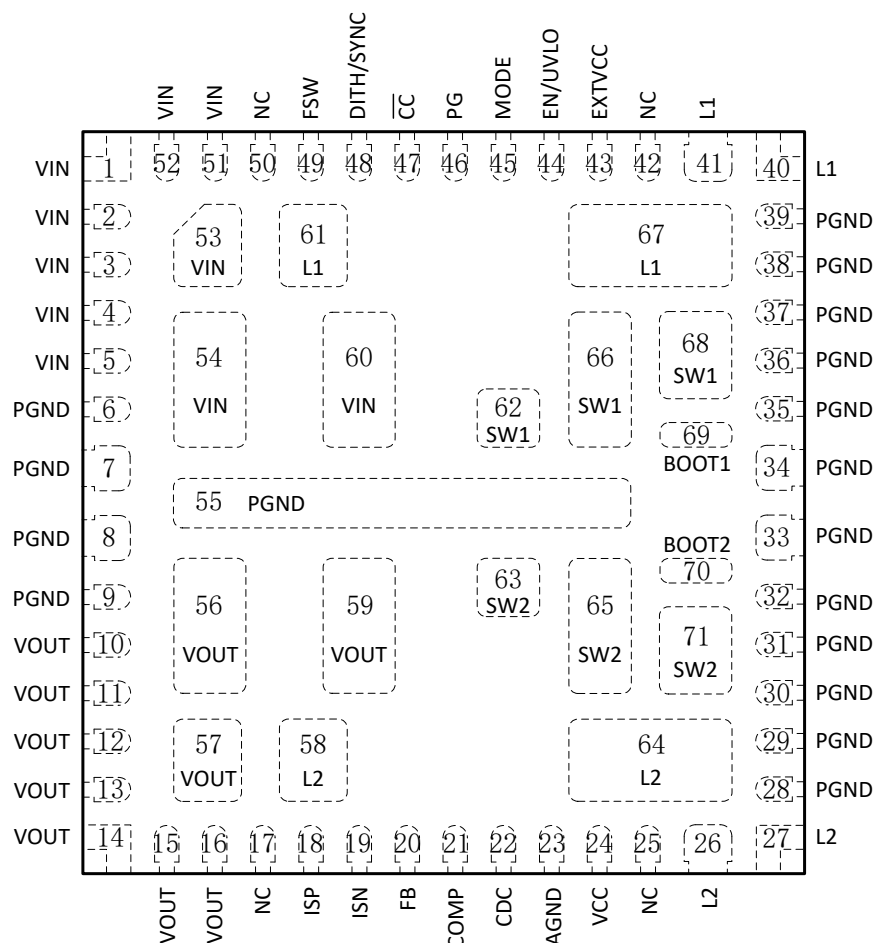
**Typical Application Circuit**



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>7 Application and Implementation</b> .....	<b>21</b>
<b>2 Applications</b> .....	<b>1</b>	7.1 Application Information.....	21
<b>3 Description</b> .....	<b>1</b>	7.2 Typical Application.....	21
<b>4 Pin Configuration and Functions</b> .....	<b>3</b>	7.3 Power Supply Recommendations.....	29
<b>5 Specifications</b> .....	<b>5</b>	7.4 Layout.....	29
5.1 Absolute Maximum Ratings.....	5	<b>8 Device and Documentation Support</b> .....	<b>31</b>
5.2 ESD Ratings.....	5	8.1 Device Support.....	31
5.3 Recommended Operating Conditions.....	5	8.2 Receiving Notification of Documentation Updates....	31
5.4 Thermal Information.....	6	8.3 Support Resources.....	31
5.5 Electrical Characteristics.....	6	8.4 Trademarks.....	31
5.6 Typical Characteristics.....	9	8.5 Electrostatic Discharge Caution.....	31
<b>6 Detailed Description</b> .....	<b>12</b>	8.6 Glossary.....	31
6.1 Overview.....	12	<b>9 Revision History</b> .....	<b>31</b>
6.2 Functional Block Diagram.....	13	<b>10 Mechanical, Packaging, and Orderable</b>	
6.3 Feature Description.....	14	<b>Information</b> .....	<b>31</b>
6.4 Device Functional Modes.....	20		

## 4 Pin Configuration and Functions



**Figure 4-1. TPSM852892 RYQ Package, 71-Pin VQFN-HR (Transparent Top View)**

**Table 4-1. Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	23	-	Signal ground of the IC.
BOOT1	69	O	Power supply for high-side MOSFET gate driver in buck side. A ceramic capacitor of 0.1µF is integrated between this pin and the SW1 pin. Leave this pin floating.
BOOT2	70	O	Power supply for high-side MOSFET gate driver in boost side. A ceramic capacitor of 0.1µF is integrated between this pin and the SW2 pin. Leave this pin floating.
CC	47	O	Constant current output indication open drain output. When output current limit is triggered, this pin outputs low level.
CDC	22	O	Voltage output proportional to the sensed voltage between the ISP pin and the ISN pin. Use a resistor between this pin and AGND to increase the output voltage to compensate voltage droop across the cable caused by the cable resistance.
COMP	21	O	Output of the internal error amplifier. Connect the loop compensation network between this pin and the AGND pin.
DITH/SYNC	48	I	Dithering frequency setting and synchronous clock input. Use a capacitor between this pin and ground to set the dithering frequency. When this pin is short to ground or pulled above 1.2V, there is no dithering function. An external clock can be applied at this pin to synchronize the switching frequency.

**Table 4-1. Pin Functions (continued)**

PIN		I/O	DESCRIPTION
NAME	NO.		
EN/UVLO	44	I	Enable logic input and programmable input voltage undervoltage lockout (UVLO) input. Logic high level enables the device. Logic low level disables the device and turns it into shutdown mode. After the voltage at the EN/UVLO pin is above the logic high voltage of 1.15V, this pin acts as programmable UVLO input with 1.23V internal reference.
EXTVCC	43	I	Select the internal LDO or external 5V for VCC. When it is connected to logic high voltage or is left floating, select the internal LDO. When it is connected to logic low voltage, select the external 5V for VCC.
FB	20	I	Connect to the center of a resistor divider to program the output voltage
FSW	49	I	The switching frequency is programmed by a resistor between this pin and the AGND pin.
ISN	19	I	Negative input of the current sense amplifier. An optional current sense resistor connected between the ISP pin and the ISN pin can limit the output current. If the sensed voltage reaches the current limit, a slow constant current control loop becomes active and starts to regulate the voltage between the ISP pin and the ISN pin. Connecting the ISP pin and the ISN pin together with the VOUT pin can disable the output current limit function. Do not leave floating.
ISP	18	I	Positive input of the current sense amplifier. An optional current sense resistor connected between the ISP pin and the ISN pin can limit the output current. If the sensed voltage reaches the current limit, a slow constant current control loop becomes active and starts to regulate the voltage between the ISP pin and the ISN pin. Connecting the ISP pin and the ISN pin together with the VOUT pin can disable the output current limit function. Do not leave floating.
L1	40-41, 61, 67	PWR	The terminal of the internal integrated inductor, connect this pin with SW1.
L2	26-27, 58, 64	PWR	The terminal of the internal integrated inductor, connect this pin with SW2.
MODE	45	I	Mode selection pin in light load condition. When it is connected to logic high voltage, the device works in forced PWM mode. When it is connected to logic low voltage, the device works in auto PFM mode. This pin can not be float in application.
NC	17, 25, 42, 50	-	Not connected internally, connect NC with AGND.
PG	46	O	Power good indication open drain output. When the output voltage is above 95% of the setting output voltage, this pin outputs high impedance. When the output voltage is below 90% of the setting output voltage, this pin outputs low level
PGND	6-9, 28-39, 55	PWR	IC power ground.
SW1	62, 66, 68	PWR	Buck side switching node pin. It is connected to the drain of the internal buck low-side power MOSFET and the source of internal buck high-side power MOSFET.
SW2	63, 65, 71	PWR	Boost side switching node pin. It is connected to the drain of the internal boost low-side power MOSFET and the source of internal boost high-side power MOSFET.
VCC	24	O	Internal regulator output. A ceramic capacitor of more than 4.7µF is required between this pin and the AGND pin.
VIN	1-5, 51-54, 60	PWR	Buck-boost module input.
VOUT	10-16, 56-57, 59	PWR	Buck-boost module output.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage range at terminals <sup>(2)</sup>	VIN, SW1, L1	−0.3	42	V
	BOOT1	SW1−0.3	SW1+6	V
	VCC, PG, $\overline{CC}$ , FSW, COMP, FB, MODE, CDC, DITH/SYNC, EXTVCC	−0.3	6	V
	VOUT, SW2, L2, ISP, ISN	−0.3	25	V
	EN/UVLO	−0.3	20	V
	BOOT2	SW2−0.3	SW2+6	V
	PG, $\overline{CC}$ , FSW, COMP, FB, MODE, CDC, DITH/SYNC, EXTVCC	−0.3	VCC+0.3	V
T <sub>J</sub>	Operating Junction, T <sub>J</sub> <sup>(3)</sup>	−40	150	°C
T <sub>stg</sub>	Storage temperature	−65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to network ground terminal.
- (3) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002 <sup>(2)</sup>	±500	

- (1) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Input voltage range	3.0		36	V
V <sub>OUT</sub>	Output voltage range	0.8		22	V
C <sub>IN</sub>	Effective input capacitance range	4.7	22		μF
C <sub>OUT</sub>	Effective output capacitance range	10	100	1000	μF
T <sub>J</sub>	Operating junction temperature	−40		125	°C

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPSM852892	UNIT
		RCM (QFN-FCMOD)	
		71 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	20.8 <sup>(2)</sup>	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	N/A <sup>(3)</sup>	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	N/A <sup>(3)</sup>	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) Measured on TPSM852892EVM-136, 4-layer, 2-oz/1-oz/1-oz/2-oz copper 91-mm x 66-mm PCB.

(3) Not applicable to an EVM.

## 5.5 Electrical Characteristics

T<sub>J</sub> = -40°C to 125°C, V<sub>IN</sub> = 12 V and V<sub>OUT</sub> = 20 V. Typical values are at T<sub>J</sub> = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLY</b>						
V <sub>IN</sub>	Input voltage range		3.0		36	V
V <sub>VIN_UVLO</sub>	Under voltage lockout threshold	V <sub>IN</sub> rising	2.8	2.9	3.0	V
		V <sub>IN</sub> falling	2.6	2.65	2.7	V
I <sub>Q</sub>	Quiescent current into VIN pin	IC enabled, no load, no switching. V <sub>IN</sub> = 3.0V to 24V, V <sub>OUT</sub> = 0.8V, V <sub>FB</sub> = V <sub>REF</sub> + 0.1V, R <sub>FSW</sub> = 49.9kΩ, T <sub>J</sub> up to 125°C		760	860	μA
	Quiescent current into VOUT pin	IC enabled, no load, no switching, V <sub>IN</sub> = 3.0V, V <sub>OUT</sub> = 3V to 20V, V <sub>FB</sub> = V <sub>REF</sub> + 0.1V, R <sub>FSW</sub> = 49.9kΩ, T <sub>J</sub> up to 125°C		760	860	μA
I <sub>SD</sub>	Shutdown current into VIN pin	IC disabled, V <sub>IN</sub> = 3.0V to 14V, T <sub>J</sub> up to 125°C, EXT <sub>VCC</sub> pin floating		0.8	3	μA
V <sub>CC</sub>	Internal regulator output	I <sub>VCC</sub> = 50mA, V <sub>IN</sub> = 8V, V <sub>OUT</sub> = 20V	5.05	5.2	5.45	V
<b>EN/UVLO</b>						
V <sub>EN_H</sub>	EN Logic high threshold	V <sub>CC</sub> = 3.0V to 5.5V			1.15	V
V <sub>EN_L</sub>	EN Logic low threshold	V <sub>CC</sub> = 3.0V to 5.5V	0.4			V
V <sub>EN_HYS</sub>	Enable threshold hysteresis	V <sub>CC</sub> = 3.0V to 5.5V	0.04			V
V <sub>UVLO</sub>	UVLO rising threshold at the EN/UVLO pin	V <sub>CC</sub> = 3.0V to 5.5V	1.20	1.23	1.26	V
V <sub>UVLO_HYS</sub>	UVLO threshold hysteresis	V <sub>CC</sub> = 3.0V to 5.5V		10		mV
I <sub>UVLO</sub>	Sourcing current at the EN/UVLO pin	V <sub>UVLO</sub> = 1.3V	4.4	5	5.6	μA
<b>OUTPUT</b>						
V <sub>OUT</sub>	Output voltage range		0.8		22	V
V <sub>OVP</sub>	Output overvoltage protection threshold		22.5	23.5	24.5	V
V <sub>OVP_HYS</sub>	Over voltage protection hysteresis			1		V
I <sub>FB_LKG</sub>	Leakage current at FB pin	T <sub>J</sub> up to 125°C			100	nA
I <sub>VOUT_LKG</sub>	Leakage current into VOUT pin	IC disabled, V <sub>OUT</sub> = 20V, V <sub>SW2</sub> = 0V, T <sub>J</sub> up to 125°C		1	20	μA
<b>REFERENCE VOLTAGE</b>						
V <sub>REF</sub>	Reference voltage at the FB pin		1.188	1.2	1.212	V
<b>POWER SWITCH</b>						

## 5.5 Electrical Characteristics (continued)

$T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{IN} = 12\text{ V}$  and  $V_{OUT} = 20\text{ V}$ . Typical values are at  $T_J = 25^{\circ}\text{C}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R <sub>DS(on)</sub>	Low-side MOSFET on resistance on buck side	V <sub>OUT</sub> = 20V, V <sub>CC</sub> =5.2V		22		mΩ
	High-side MOSFET on resistance on buck side	V <sub>OUT</sub> = 20V, V <sub>CC</sub> =5.2V		14		mΩ
	Low-side MOSFET on resistance on boost side	V <sub>OUT</sub> = 20V, V <sub>CC</sub> =5.2V		11		mΩ
	High-side MOSFET on resistance on boost side	V <sub>OUT</sub> = 20V, V <sub>CC</sub> =5.2V		11		mΩ
INTERNAL CLOCK						
f <sub>SW</sub>	Switching frequency	R <sub>FSW</sub> =49.9k	360	400	440	kHz
		R <sub>FSW</sub> =20k	900	1000	1100	kHz
t <sub>OFF_min</sub>	Min. off time	Boost mode		90	145	ns
t <sub>ON_min</sub>	Min. on time	Buck mode		90	130	ns
V <sub>FSW</sub>	Voltage at FSW pin			1		V
CURRENT LIMIT						
I <sub>LIM_AVG</sub>	Average inductor current limit	TPSM852892, V <sub>IN</sub> = 12V, V <sub>OUT</sub> = 9V, F <sub>SW</sub> = 400kHz, V <sub>CC</sub> = 5.2V	5	6	7	A
I <sub>LIM_PK_H</sub>	Peak inductor current limit at high side	TPSM852892, V <sub>IN</sub> = 12V, V <sub>OUT</sub> = 9V, F <sub>SW</sub> = 400kHz		9		A
I <sub>LIM_PK_L</sub>	Peak inductor current limit at low side	TPSM852892, V <sub>IN</sub> = 12V, V <sub>OUT</sub> = 9V, F <sub>SW</sub> = 400kHz		9		A
V <sub>SNS</sub>	Current loop regulation voltage between ISP and ISN pin		48	50	52	mV
CABLE VOLTAGE DROP COMPENSATION						
V <sub>CDC</sub>	Voltage at the CDC pin	R <sub>CDC</sub> = 20kΩ or floating, V <sub>ISP</sub> – V <sub>ISN</sub> = 50mV	0.95	1	1.05	V
		R <sub>CDC</sub> = 20kΩ or floating, V <sub>ISP</sub> – V <sub>ISN</sub> = 2mV		40	75	mV
I <sub>FB_CDC</sub>	FB pin sinking current	External output feedback, R <sub>CDC</sub> = 20kΩ, V <sub>ISP</sub> – V <sub>ISN</sub> = 50mV	7.23	7.5	7.87	μA
		External output feedback, R <sub>CDC</sub> = 20kΩ, V <sub>ISP</sub> – V <sub>ISN</sub> = 0mV		0	0.3	μA
		External output feedback, R <sub>CDC</sub> = floating, V <sub>ISP</sub> – V <sub>ISN</sub> = 50mV		0	0.3	μA
ERROR AMPLIFIER						
I <sub>SINK</sub>	COMP pin sink current	V <sub>FB</sub> = V <sub>REF</sub> + 400mV, V <sub>COMP</sub> =1.5V, V <sub>CC</sub> =5V		20		μA
I <sub>SOURCE</sub>	COMP pin source current	V <sub>FB</sub> = V <sub>REF</sub> - 400mV, V <sub>COMP</sub> =1.5V, V <sub>CC</sub> =5V		60		μA
V <sub>CCLPH</sub>	High clamp voltage at the COMP pin	FPWM mode, V <sub>OUT</sub> = 1.8V to 22V		1.23		V
V <sub>CCLPL</sub>	Low clamp voltage at the COMP pin	FPWM mode		0.7		V
G <sub>EA</sub>	Error amplifier transconductance			190		μA/V
SOFT START						
t <sub>SS</sub>	Soft-start time		2.4	3.6	5.0	ms
SPREAD SPECTRUM						
I <sub>DITH_CHG</sub>	Dithering charge current	V <sub>DITH/SYNC</sub> = 1.0V; R <sub>FSW</sub> =49.9kΩ; voltage rising from 0.9V		2		μA
I <sub>DITH_DIS</sub>	Dithering discharge current	V <sub>DITH/SYNC</sub> = 1.0V; R <sub>FSW</sub> =49.9kΩ; voltage falling from 1.1V		2		μA

## 5.5 Electrical Characteristics (continued)

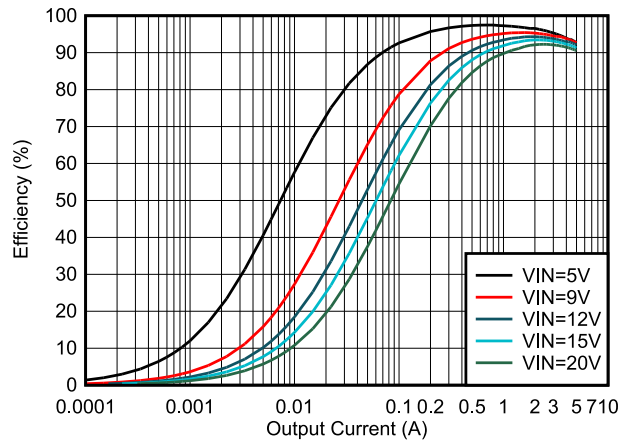
$T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{IN} = 12\text{ V}$  and  $V_{OUT} = 20\text{ V}$ . Typical values are at  $T_J = 25^{\circ}\text{C}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DITH\_H}$	Dither high threshold			1.07		V
$V_{DITH\_L}$	Dither low threshold			0.93		V
<b>SYNCHRONOUS CLOCK</b>						
$V_{SYNC\_H}$	Sync clock high voltage threshold				1.2	V
$V_{SYNC\_L}$	Sync clock low voltage threshold		0.4			V
$t_{SYNC\_MIN}$	Minimum sync clock pulse width		50			ns
<b>HICCUP</b>						
$t_{HICCUP}$	Hiccup off time			76		ms
<b>MODE</b>						
$V_{MODE}$	MODE logic high threshold	$V_{CC} = 3\text{V to } 5.5\text{V}$			1.2	V
$V_{MODE}$	MODE logic low threshold	$V_{CC} = 3\text{V to } 5.5\text{V}$	0.4			V
<b>EXTVCC</b>						
$V_{EXTVCC}$	EXTVCC Logic high threshold	$V_{CC} = 3\text{V to } 5.5\text{V}$			1.2	V
$V_{EXTVCC}$	EXTVCC Logic Low threshold	$V_{CC} = 3\text{V to } 5.5\text{V}$	0.4			V
<b>Power Good</b>						
$I_{PG\_H}$	Leakage current into PG pin when outputting high impedance	$V_{PG} = 5\text{V}$			100	nA
$V_{PG\_L}$	Output low voltage range of the PG pin	Sinking 4mA current		0.1	0.2	V
<b>Current Limit Indication</b>						
$I_{\overline{CC\_H}}$	Leakage current into $\overline{CC}$ pin when outputting high impedance	$V_{\overline{CC}} = 5\text{ V}$			100	nA
$V_{\overline{CC\_L}}$	Output low voltage range of the $\overline{CC}$ pin	Sinking 4-mA current		0.1	0.2	V
<b>PROTECTION</b>						
$T_{SD}$	Thermal shutdown threshold	$T_J$ rising		175		$^{\circ}\text{C}$
$T_{SD\_HYS}$	Thermal shutdown hysteresis	$T_J$ falling below $T_{sd}$		20		$^{\circ}\text{C}$

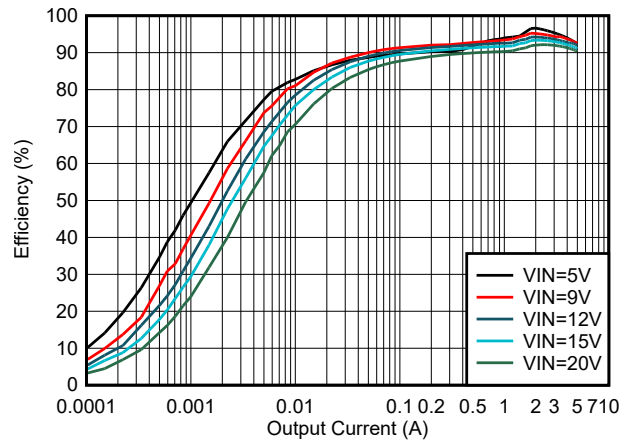


## 5.6 Typical Characteristics

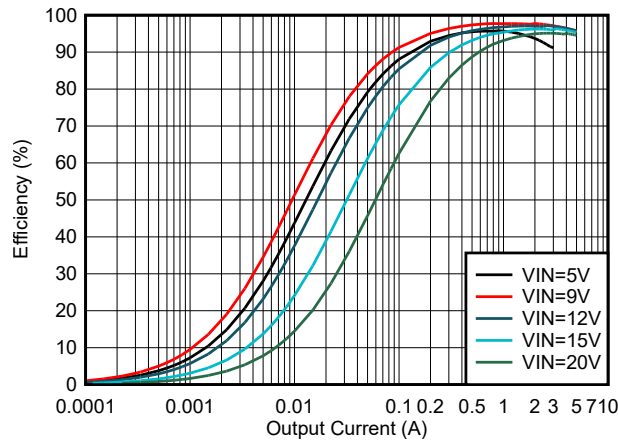
$V_{IN} = 12V$ ,  $T_A = 25^\circ C$ ,  $f_{SW} = 400kHz$ , unless otherwise noted



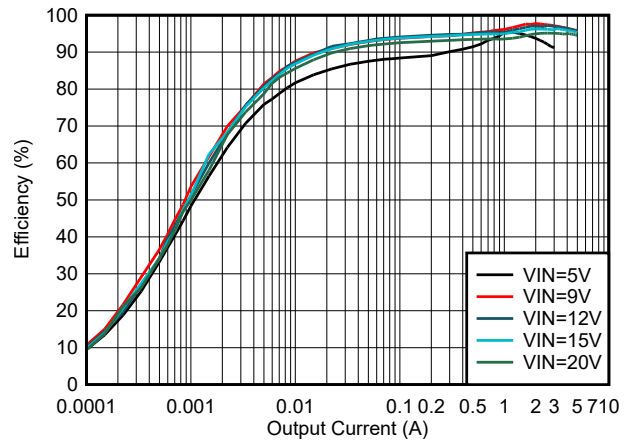
**Figure 5-1. Efficiency vs Output Current,  
 $V_{OUT} = 5V$ , FPWM**



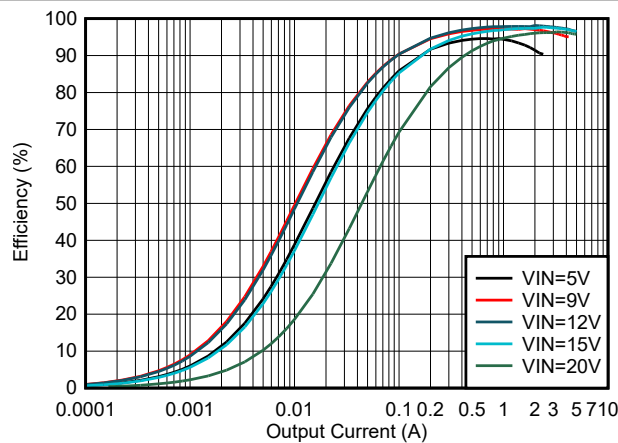
**Figure 5-2. Efficiency vs Output Current,  
 $V_{OUT} = 5V$ , PFM**



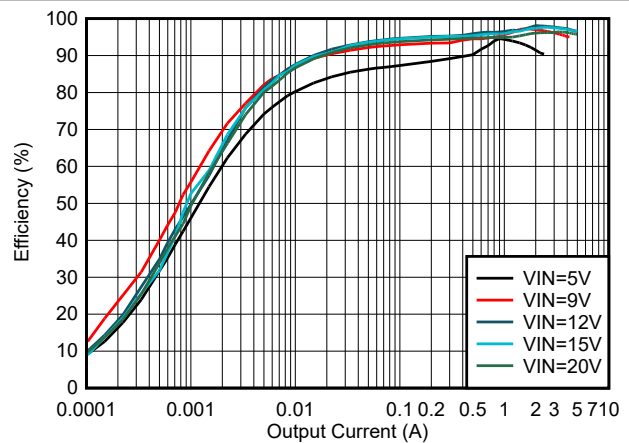
**Figure 5-3. Efficiency vs Output Current,  
 $V_{OUT} = 9V$ , FPWM**



**Figure 5-4. Efficiency vs Output Current,  
 $V_{OUT} = 9V$ , PFM**

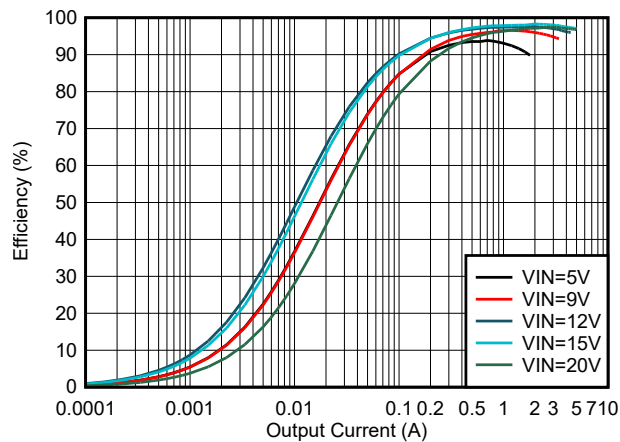


**Figure 5-5. Efficiency vs Output Current,  
 $V_{OUT} = 12V$ , FPWM**

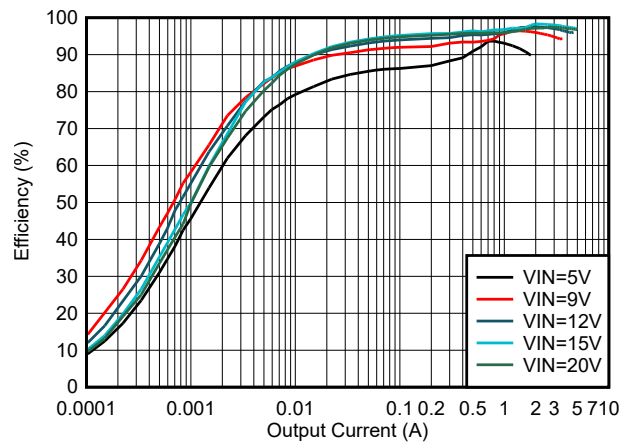


**Figure 5-6. Efficiency vs Output Current,  
 $V_{OUT} = 12V$ , PFM**

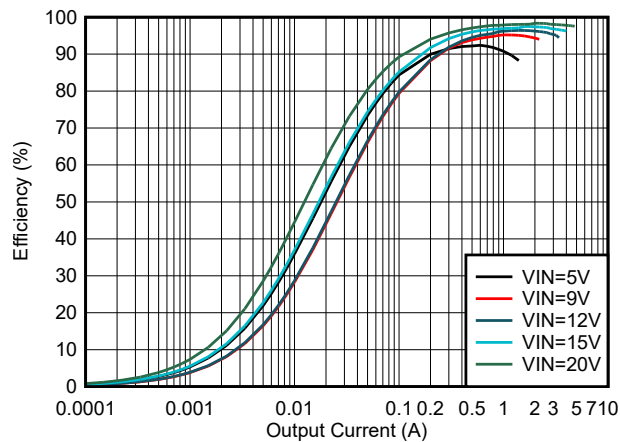
## 5.6 Typical Characteristics (continued)



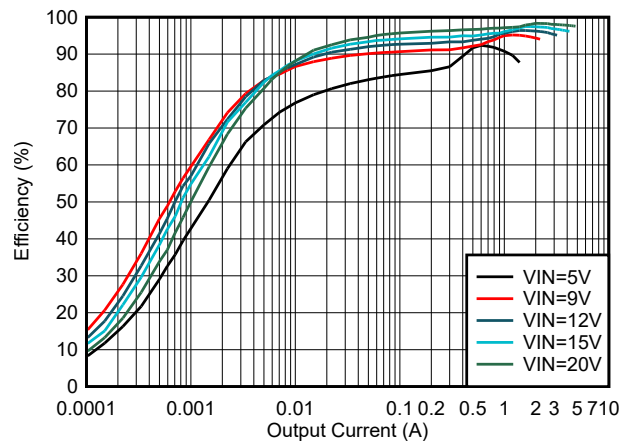
**Figure 5-7. Efficiency vs Output Current,  
 $V_{OUT} = 15V$ , FPWM**



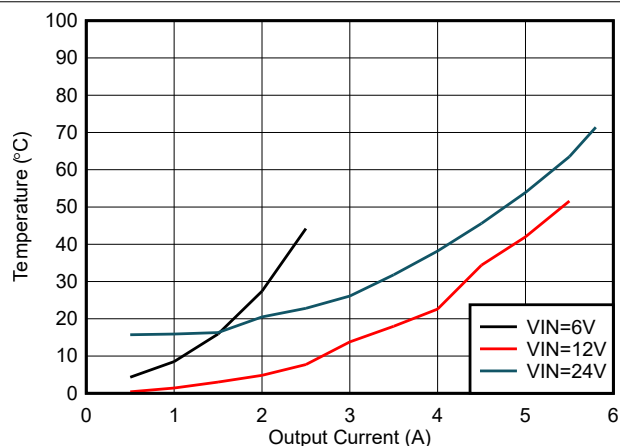
**Figure 5-8. Efficiency vs Output Current,  
 $V_{OUT} = 15V$ , PFM**



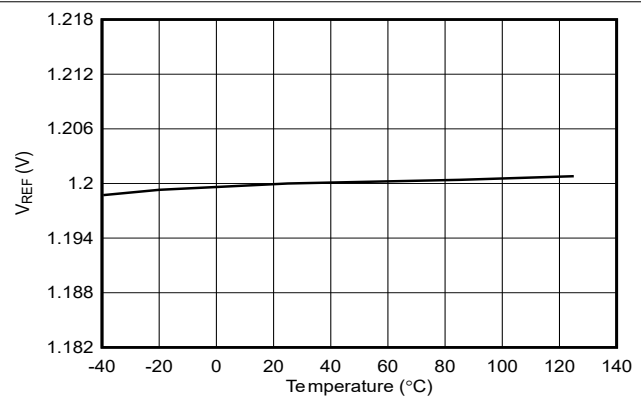
**Figure 5-9. Efficiency vs Output Current,  
 $V_{OUT} = 20V$ , FPWM**



**Figure 5-10. Efficiency vs Output Current,  
 $V_{OUT} = 20V$ , PFM**

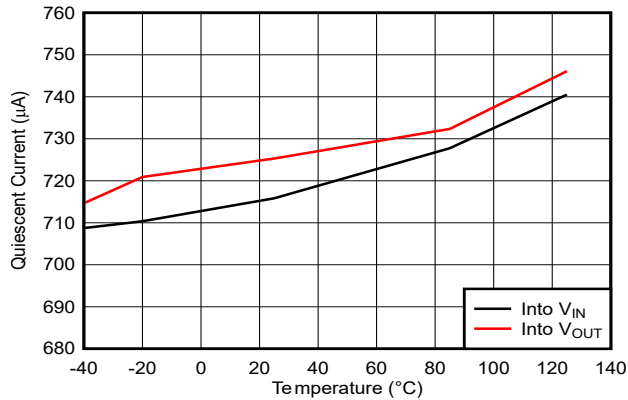


**Figure 5-11. Device Temperature Rise vs Output Current  
(12V<sub>OUT</sub>), FPWM**

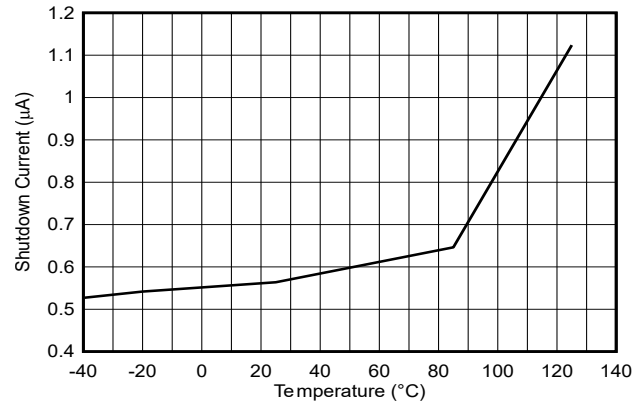


**Figure 5-12. Reference Voltage vs Temperature ( $V_{REF} = 1.2V$ )**

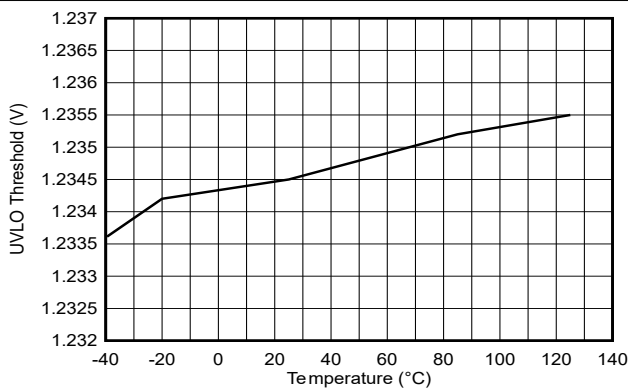
## 5.6 Typical Characteristics (continued)



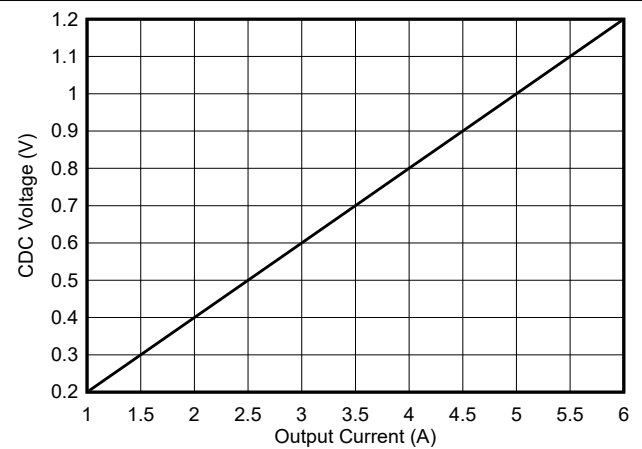
**Figure 5-13. Quiescent Current vs Temperature**



**Figure 5-14. Shutdown Current vs Temperature**



**Figure 5-15. ENABLE/UVLO Rising Threshold vs Temperature**



**Figure 5-16. CDC Voltage vs Output Current with  $R_{SENSE} = 10m\Omega$**

## 6 Detailed Description

### 6.1 Overview

The TPSM852892 is a 6A buck-boost DC-to-DC module with the four MOSFETs and power inductor integrated. The TPSM852892 can operate over a wide range of 3.0V to 36V input voltage and an output voltage of 0.8V to 22V. According to the input voltage and the set output voltage, the operation of device can transit among buck mode, buck-boost mode, and boost mode smoothly. The TPSM852892 operates in buck mode when the input voltage is greater than the output voltage and in boost mode when the input voltage is less than the output voltage. When the input voltage is close to the output voltage, the TPSM852892 operates in one-cycle buck and one-cycle boost mode alternately.

The TPSM852892 uses an average current mode control scheme. Current mode control provides simplified loop compensation, rapid response to the load transients, and inherent line voltage rejection. An error amplifier compares the feedback voltage with the internal reference voltage. The output of the error amplifier determines the average inductor current.

An internal oscillator can be configured to operate over a wide range of frequency from 400kHz to 1MHz. The internal oscillator can also synchronize to an external clock applied to the DITH/SYNC pin. To minimize EMI, the TPSM852892 can dither the switching frequency at  $\pm 7\%$  of the set frequency.

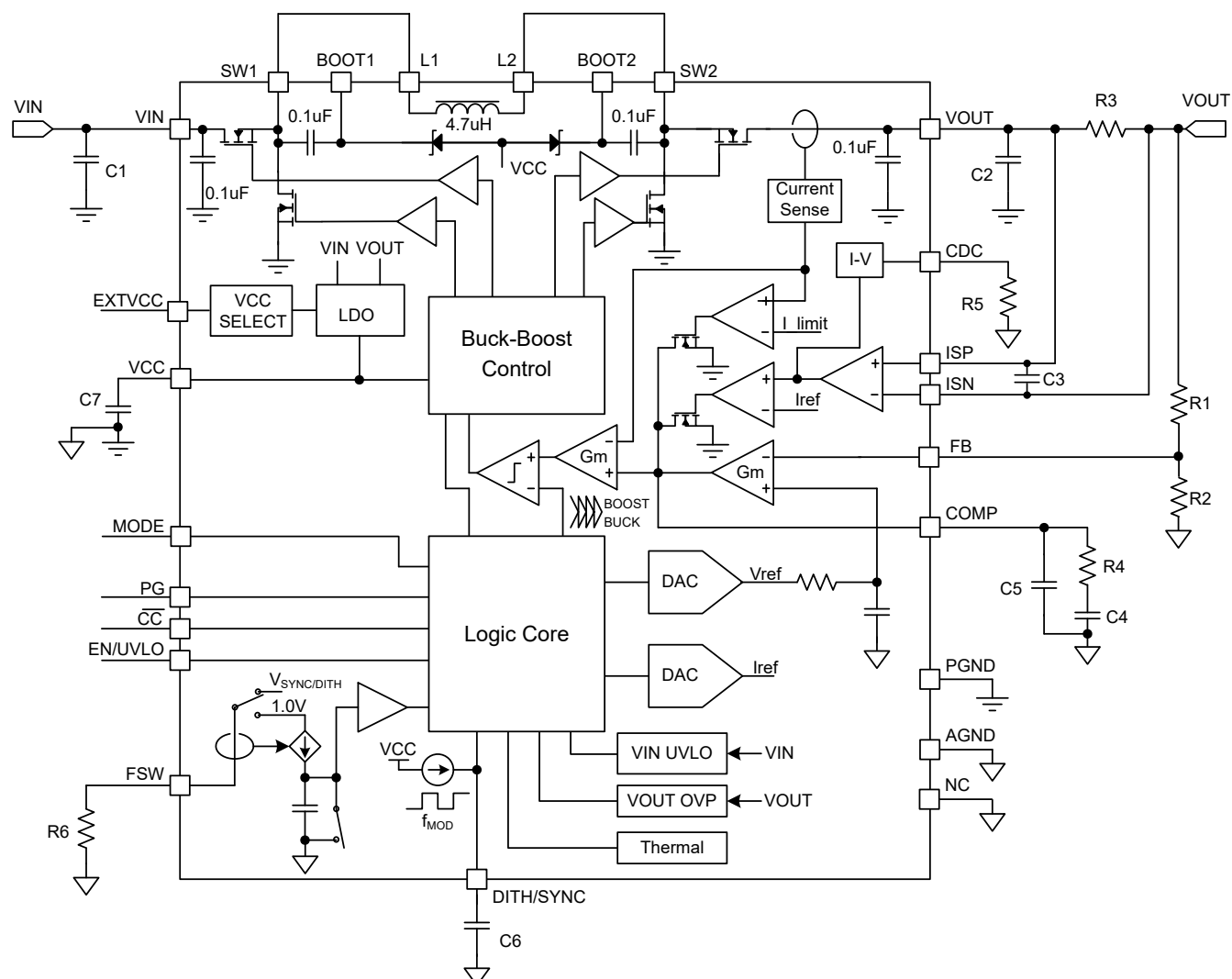
The TPSM852892 works in fixed-frequency PWM mode at moderate to heavy load currents. In light load condition, the TPSM852892 can be configured to automatically transition to PFM mode or be forced in PWM mode.

The TPSM852892 provides average inductor current limit of 6A typically. In addition, it provides cycle-by-cycle peak inductor current limit during transient to protect the device against overcurrent condition beyond the capability of the device.

A precision voltage threshold of 1.23V with 5 $\mu$ A sourcing current at the EN/UVLO pin supports programmable input undervoltage lockout (UVLO) with hysteresis. The output overvoltage protection (OVP) feature turns off the high-side FETs to prevent damage to the devices powered by the TPSM852892.

The device provides hiccup mode option to reduce the heating in the power components when output short circuit happens. The TPSM852892 turns off for 76ms and restarts at soft start-up.

## 6.2 Functional Block Diagram



## 6.3 Feature Description

### 6.3.1 VCC Power Supply

An internal LDO to supply the TPSM852892 outputs regulated 5.2V voltage at the VCC pin. When  $V_{IN}$  is less than  $V_{OUT}$ , the internal LDO selects the power supply source by comparing  $V_{IN}$  to a rising threshold of 6.2V with 0.3V hysteresis. When  $V_{IN}$  is higher than 6.2V, the supply for LDO is  $V_{IN}$ . When  $V_{IN}$  is lower than 5.9V, the supply for LDO is  $V_{OUT}$ . When  $V_{OUT}$  is less than  $V_{IN}$ , the internal LDO selects the power supply source by comparing  $V_{OUT}$  to a rising threshold of 6.2V with 0.3V hysteresis. When  $V_{OUT}$  is higher than 6.2V, the supply for LDO is  $V_{OUT}$ . When  $V_{OUT}$  is lower than 5.9V, the supply for LDO is  $V_{IN}$ . [Table 6-1](#) shows the supply source selection for the internal LDO.

**Table 6-1. VCC Power Supply Logic**

$V_{IN}$	$V_{OUT}$	INPUT for VCC LDO
$V_{IN} > 6.2V$	$V_{OUT} > V_{IN}$	$V_{IN}$
$V_{IN} < 5.9V$	$V_{OUT} > V_{IN}$	$V_{OUT}$
$V_{IN} > V_{OUT}$	$V_{OUT} > 6.2V$	$V_{OUT}$
$V_{IN} > V_{OUT}$	$V_{OUT} < 5.9V$	$V_{IN}$

### 6.3.2 EXTVCC Power Supply

To minimize the power dissipation of the internal LDO when both input voltage and output voltage are high, an external 5V power source can be applied at the VCC pin to supply the TPSM852892. The external 5V power supply must have at least 100mA output current capability and must be within the 4.75V to 5.5V regulation range. When the EXTVCC pin is connected to logic low, the device selects the external power supply to supply the device through VCC pin. When the EXTVCC pin is connected to logic high or is left floating, the device selects internal LDO.

### 6.3.3 Input Undervoltage Lockout

When the input voltage is below 2.6V, the TPSM852892 is disabled. When the input voltage is above 3V, the TPSM852892 can be enabled by pulling the EN pin to a high voltage above 1.3V.

### 6.3.4 Enable and Programmable UVLO

The TPSM852892 has a dual function enable and undervoltage lockout (UVLO) circuit. When the input voltage at the VIN pin is above the input UVLO rising threshold of 3V and the EN/UVLO pin is pulled above 1.15V but less than the enable UVLO threshold of 1.23V, the TPSM852892 is enabled but still in standby mode. The TPSM852892 starts to detect the MODE pin logic status.

The EN/UVLO pin has an accurate UVLO voltage threshold to support programmable input undervoltage lockout with hysteresis. When the EN/UVLO pin voltage is greater than the UVLO threshold of 1.23V, the TPSM852892 is enabled and switching operation. A hysteresis current  $I_{UVLO\_HYS}$  is sourced out of the EN/UVLO pin to provide hysteresis that prevents on/off chattering in the presence of noise with a slowly changing input voltage.

By using resistor divider as shown in [Figure 6-1](#), the turn on threshold is calculated using [Equation 1](#).

$$V_{IN(UVLO\_ON)} = V_{UVLO} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

where

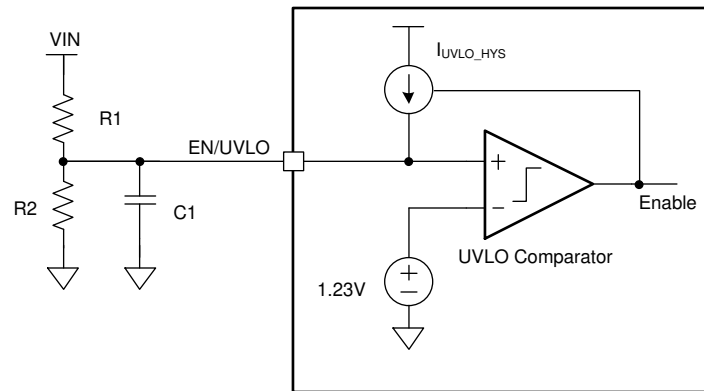
- $V_{UVLO}$  is the UVLO threshold of 1.23V at the EN/UVLO pin

The hysteresis between the UVLO turn on threshold and turnoff threshold is set by the upper resistor in the EN/UVLO resistor divider and is given by the [Equation 2](#).

$$\Delta V_{IN(UVLO)} = I_{UVLO\_HYS} \times R1 \quad (2)$$

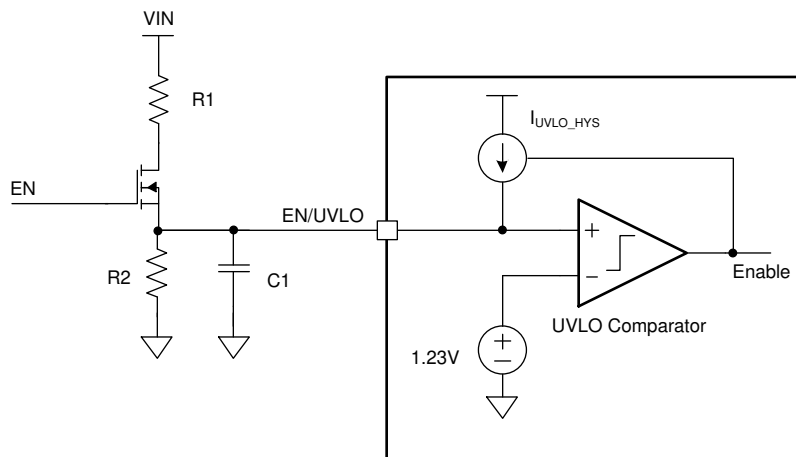
where

- $I_{UVLO\_HYS}$  is the sourcing current from the EN/UVLO pin when the voltage at the EN/UVLO pin is above  $V_{UVLO}$



**Figure 6-1. Programmable UVLO With Resistor Divider at the EN/UVLO Pin**

Using an NMOSFET together with a resistor divider can implement both logic enable and programmable UVLO as shown in Figure 6-2. The EN logic high level must be greater than enable threshold plus the  $V_{th}$  of the NMOSFET Q1. The Q1 also eliminates the leakage current from VIN to ground through the UVLO resistor divider during shutdown mode.



**Figure 6-2. Logic Enable and Programmable UVLO**

### 6.3.5 Soft Start

When the input voltage is above the UVLO threshold and the voltage at the EN/UVLO pin is above the enable UVLO threshold, the TPSM852892 starts to ramp up the output voltage by ramping an internal reference voltage from 0V to 1.2V within 3.6ms.

### 6.3.6 Shutdown

When the EN/UVLO pin voltage is pulled below 0.4V, the TPSM852892 is in shutdown mode, and all functions are disabled.

### 6.3.7 Switching Frequency

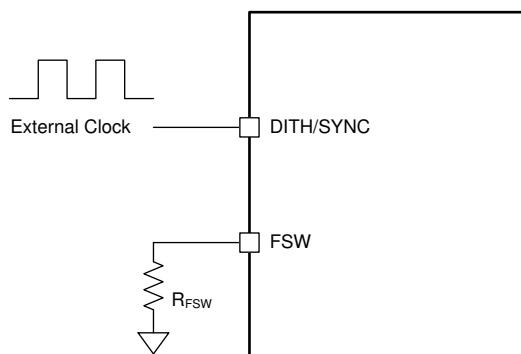
The TPSM852892 uses a fixed frequency average current control scheme. The switching frequency is between 400kHz and 1MHz set by placing a resistor at the FSW pin. An internal amplifier holds this pin at a fixed voltage of 1V. The setting resistance is between a maximum of 49.9kΩ and a minimum of 20kΩ. Use [Equation 3](#) to calculate the resistance by a given switching frequency.

$$f_{SW} = \frac{1000}{0.05 \times R_{FSW} + 35} \text{ (MHz)} \quad (3)$$

where

- $R_{FSW}$  is the resistance at the FSW pin (Ω)

For noise-sensitive applications, the TPSM852892 can be synchronized to an external clock signal applied to the DITH/SYNC pin. The duty cycle of the external clock is recommended in the range of 30% to 70%. A resistor also must be connected to the FSW pin when the TPSM852892 is switching by the external clock. The external clock frequency at the DITH/SYNC pin must have lower than 0.4V low level voltage and must be within  $\pm 30\%$  of the corresponding frequency set by the resistor. [Figure 6-3](#) is a recommended configuration.



**Figure 6-3. External Clock Configuration**



### 6.3.8 Switching Frequency Dithering

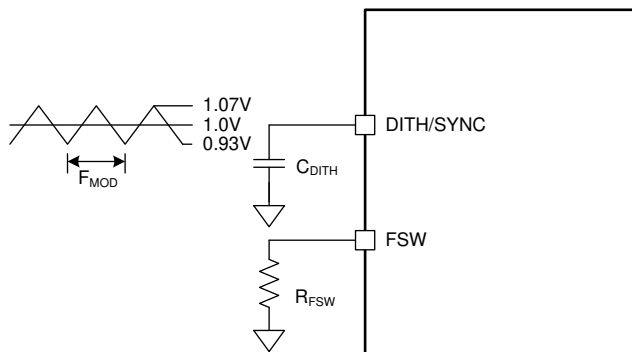
The TPSM852892 provides an optional switching frequency dithering that is enabled by connecting a capacitor from the DITH/SYNC pin to ground. Figure 6-4 illustrates the dithering circuit. By charging and discharging the capacitor, a triangular waveform centered at 1V is generated at the DITH/SYNC pin. The triangular waveform modulates the oscillator frequency by  $\pm 7\%$  of the nominal frequency set by the resistance at the FSW pin. The capacitance at the DITH/SYNC pin sets the modulation frequency. A small capacitance modulates the oscillator frequency at a faster rate than a large capacitance. For the dithering circuit to effectively reduce peak EMI, the modulation rate normally is below 1kHz. Equation 4 calculates the capacitance required to set the modulation frequency,  $F_{MOD}$ .

$$C_{DITH} = \frac{1}{2.8 \times R_{FSW} \times F_{MOD}} (F) \quad (4)$$

where

- $R_{FSW}$  is the switching frequency setting resistance ( $\Omega$ ) at the FSW pin
- $F_{MOD}$  is the modulation frequency (Hz) of the dithering

Connecting the DITH/SYNC pin below 0.4V or above 1.2V disables switching frequency dithering. The dithering function also is disabled when an external synchronous clock is used.



**Figure 6-4. Switching Frequency Dithering**

### 6.3.9 Inductor Current Limit

The TPSM852892 implements both peak current and average inductor current limit. The average current mode control loop uses the current sense information at the high-side MOSFET of the boost leg to clamp the maximum average inductor current to 6A (typical).

Besides the average current limit, a peak current limit protection is implemented during transient to protect the device against over current condition beyond the capability of the device.

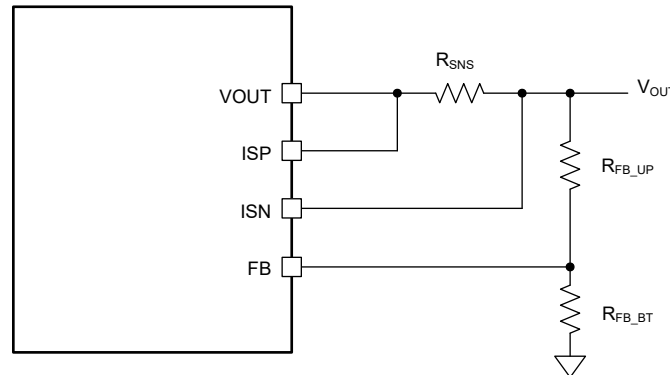
### 6.3.10 Internal Charge Path

Each of the two high-side MOSFET drivers is biased from its floating bootstrap capacitor, which is normally re-charged by  $V_{CC}$  through both the external and internal bootstrap diodes when the low-side MOSFET is turned on. When the TPSM852892 operates exclusively in the buck or boost regions, one of the high-side MOSFETs is constantly on. An internal charge path, from VOUT and BOOT2 to BOOT1 or from VIN and BOOT1 to BOOT2, charges the bootstrap capacitor to  $V_{CC}$  so that the high-side MOSFET remains on.

### 6.3.11 Output Voltage Setting

TPSM852892 output voltage is configured with feedback resistors as shown in Figure 6-5. Use Equation 5 to calculate the output voltage with the reference voltage at the FB pin.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB\_UP}}{R_{FB\_BT}}\right) \quad (5)$$



**Figure 6-5. Output Voltage Setting**

TI recommends using 100kΩ for the up resistor  $R_{FB\_UP}$ . The reference voltage  $V_{REF}$  is 1.2V.

### 6.3.12 Output Current Monitoring and Cable Voltage Droop Compensation

The TPSM852892 outputs a voltage at the CDC pin proportional to the sensed voltage across a output current sensing resistor between the ISP pin and the ISN pin. Equation 6 shows the exact voltage at the CDC pin related to the sensed output current.

$$V_{CDC} = 20 \times (V_{ISP} - V_{ISN}) \quad (6)$$

To compensate the voltage droop across a cable from the output of the USB port to its powered device, the TPSM852892 can lift its output voltage in proportion to the load current by placing a resistor between the CDC pin and AGND pin.

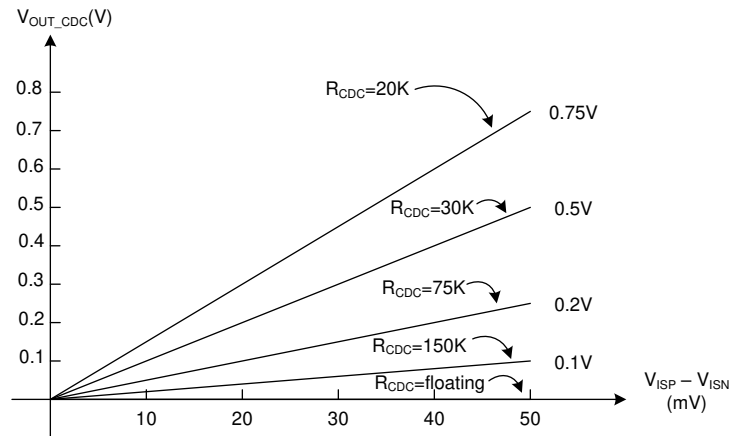
The output voltage rises in proportion to the current sourcing from the CDC pin through the resistor at the CDC pin. It is recommended to use 100kΩ resistance for the up resistor of the feedback resistor divider. Equation 7 shows the output voltage rise related to the sensed output current, the resistance at the CDC pin, and the up resistor of the output voltage feedback resistor divider.

$$V_{OUT\_CDC} = 3 \times R_{FB\_UP} \times \left(\frac{V_{ISP} - V_{ISN}}{R_{CDC}}\right) \quad (7)$$

where

- $R_{FB\_UP}$  is the up resistor of the resistor divider between the output and the FB pin
- $R_{CDC}$  is the resistor at the CDC pin

When  $R_{FB\_UP}$  is 100kΩ, the output voltage rise versus the sensed output current and the resistor at the CDC pin is shown in Figure 6-6.



**Figure 6-6. Output Voltage Rise versus Output Current**

### 6.3.13 Output Current Limit

The output current limit is programmable by placing a current sensing resistor between the ISP pin and ISN pin. The voltage limit between the ISP pin and the ISN pin is set to 50mV. Thus a smaller resistance gets higher current limit and a larger resistance gets lower current limit.

Connecting the ISP and the ISN pin together to the VOUT pin disables the output current limit because the sensed voltage is always zero.

### 6.3.14 Overvoltage Protection

The TPSM852892 has output overvoltage protection. When the output voltage at the VOUT pin is detected above 23.5V typically, the TPSM852892 turns off two high-side FETs and turns on two low-side FETs until its output voltage drops the hysteresis value lower than the output overvoltage protection threshold. This function prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

### 6.3.15 Output Short Circuit Protection

In addition to the average inductor current limit, the TPSM852892 implements the output short-circuit protection by entering hiccup mode. After soft start-up time of 3.6ms, the TPSM852892 monitors the average inductor current and output voltage. Whenever the output short circuit happens, causing the average inductor current hitting the current limit and the output voltage below 0.8V for 2ms, the TPSM852892 shuts down the switching for 76ms (typical) and then repeats the soft start for 3.6ms. The hiccup mode helps reduce the total power dissipation on the TPSM852892 in the output short-circuit or overcurrent condition.

### 6.3.16 Power Good

The TPSM852892 integrates a power-good function. The power-good output consists of an open-drain NMOS, requiring an external pullup resistor connect to a suitable voltage supply like VCC. The PG pin goes high after VOUT reaches 95% of the target output voltage. When the output voltage drops below 90% of the target output voltage, the PG pin goes low.

### 6.3.17 Constant Current Output Indication

The TPSM852892 integrates a constant current output indication function. The output of  $\overline{CC}$  pin consists of an open-drain NMOS, requiring an external pullup resistor connect to a suitable voltage supply like VCC. The  $\overline{CC}$  pin goes low with a 128us delay time after the voltage between the ISP pin and the ISN pin reaches to 50mV.

### 6.3.18 Thermal Shutdown

The TPSM852892 is protected by a thermal shutdown circuit that shuts down the device when the internal junction temperature exceeds 175°C (typical). The internal soft-start circuit is reset when thermal shutdown is triggered. The converter automatically restarts when the junction temperature drops below the thermal shutdown hysteresis of 20°C below the thermal shutdown threshold.

## 6.4 Device Functional Modes

In light load condition, the TPSM852892 can work in PFM or forced PWM mode to meet different application requirements. PFM mode decreases switching frequency to reduce the switching loss thus it gets high efficiency at light load condition. The FPWM mode keeps the switching frequency unchanged to avoid undesired low switching frequency but the efficiency becomes lower than that of PFM mode.

### 6.4.1 PWM Mode

When the MODE pin is connected to logic high, the TPSM852892 works in FPWM mode and the switching frequency is unchanged in light load condition. When the load current decreases, the output of the internal error amplifier decreases as well to reduce the average inductor current down to deliver less power from input to output. When the output current further reduces, the current through the inductor decreases to zero during the switch-off time. The high-side N-MOSFET is not turned off even if the current through the MOSFET is zero. Thus, the inductor current changes its direction after it runs to zero. The power flow is from output side to input side. The efficiency is low in this condition. However, with the fixed switching frequency, there is no audible noise or other problems that are caused by low switching frequency in light load condition.

### 6.4.2 Power Save Mode

The TPSM852892 improves the efficiency at light load condition with PFM mode. When the MODE pin is connected to logic low, the TPSM852892 can work in PFM mode at light load condition. When the TPSM852892 operates at light load condition, the output of the internal error amplifier decreases to make the inductor peak current down to deliver less power to the load. When the output current further reduces, the current through the inductor decreases to zero during the switch-off time. When the TPSM852892 works in buck mode, once the inductor current becomes zero, the low-side switch of the buck side is turned off to prevent the reverse current from output to ground. When the TPSM852892 works in boost mode, once the inductor current becomes zero, the high side-switch of the boost side is turned off to prevent the reverse current from output to input. The TPSM852892 resumes switching until the output voltage drops. Thus PFM mode reduces switching cycles and eliminates the power loss by the reverse inductor current to get high efficiency in light load condition.

## 7 Application and Implementation

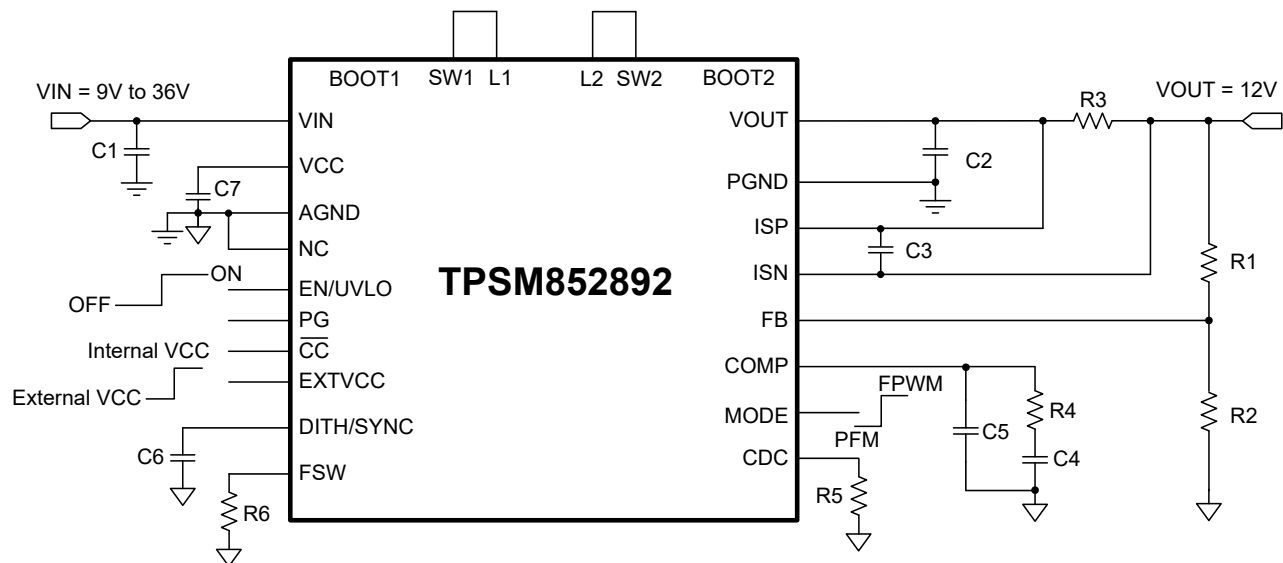
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Application Information

The TPSM852892 can operate over a wide range of 3.0V to 36V input voltage and output 0.8V to 22V. The TPSM852892 can transition among buck mode, buck-boost mode, and boost mode smoothly according to the input voltage and the setting output voltage. The TPSM852892 operates in buck mode when the input voltage is greater than the output voltage and in boost mode when the input voltage is less than the output voltage. When the input voltage is close to the output voltage, the TPSM852892 operates in one-cycle buck and one-cycle boost mode alternately. The switching frequency is set by an external resistor. To reduce the switching power loss in high power conditions, it is recommended to set the switching frequency below 600kHz.

### 7.2 Typical Application



**Figure 7-1. 12V Power Supply With 9V to 36V Input Voltage**

### 7.2.1 Design Requirements

The design parameters are listed in [Table 7-1](#):

**Table 7-1. Design Parameters**

PARAMETERS	VALUES
Input voltage	9V to 36V
Output voltage	12V
Output current limit	3A
Output voltage ripple	±50mV
Operating mode at light load	FPWM

### 7.2.2 Detailed Design Procedure

#### 7.2.2.1 Switching Frequency

The switching frequency of the TPSM852892 is set by a resistor at the FSW pin. Use [Equation 3](#) to calculate the resistance for the desired frequency. To reduce the switching power loss with such a high current application, a 1% standard resistor of 49.9kΩ is selected for 400kHz switching frequency for this application.

#### 7.2.2.2 Output Voltage Setting

The output voltage is set by an external resistor divider (R1, R2 in the [Figure 7-1](#) circuit diagram). When the output voltage is regulated, the typical voltage at the FB pin is  $V_{REF}$ . The value of R2 is then calculated as [Equation 8](#):

$$R2 = \frac{R1}{\left(\frac{V_{OUT}}{V_{REF}} - 1\right)} \quad (8)$$

#### 7.2.2.3 Input Capacitor

In buck mode, the input capacitor supplies high ripple current. The RMS current in the input capacitors is given by [Equation 14](#).

$$I_{CIN(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times V_{IN}}} \quad (9)$$

where

- $I_{CIN(RMS)}$  is the RMS current through the input capacitor
- $I_{OUT}$  is the output current

The maximum RMS current occurs at the output voltage is half of the input voltage, which gives  $I_{CIN(RMS)} = I_{OUT} / 2$ . Ceramic capacitors are recommended for their low ESR and high ripple current capability. A total of 20μF effective capacitance is a good starting point for this application. Add a 0.1μF/0402 package ceramic capacitor and place it close to VIN pin and GND pin to suppress high frequency noise which helps improve EMI performance. Add one aluminum electrolytic capacitor with a typical value of 100μF for stabilized input DC voltage during transient occasions.

#### 7.2.2.4 Output Capacitor

In boost mode, the output capacitor conducts high ripple current. The output capacitor RMS ripple current is given by [Equation 15](#), where the minimum input voltage and the maximum output voltage correspond to the maximum capacitor current.

$$I_{COUT(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \quad (10)$$

where

- $I_{\text{COUT(RMS)}}$  is the RMS current through the output capacitor
- $I_{\text{OUT}}$  is the output current

In this example, the maximum output ripple RMS current is 1.7A.

The ESR of the output capacitor causes an output voltage ripple given by [Equation 16](#) in boost mode.

$$V_{\text{RIPPLE(ESR)}} = \frac{I_{\text{OUT}} \times V_{\text{OUT}}}{V_{\text{IN}}} \times R_{\text{COUT}} \quad (11)$$

where

- $R_{\text{COUT}}$  is the ESR of the output capacitance

The capacitance also causes a capacitive output voltage ripple given by [Equation 17](#) in boost mode. When input voltage reaches the minimum value and the output voltage reaches the maximum value, there is the largest output voltage ripple caused by the capacitance.

$$V_{\text{RIPPLE(CAP)}} = \frac{I_{\text{OUT}} \times \left(1 - \frac{V_{\text{IN}}}{V_{\text{OUT}}}\right)}{C_{\text{OUT}} \times f_{\text{SW}}} \quad (12)$$

Typically, a combination of ceramic capacitors and bulk electrolytic capacitors is needed to provide low ESR, high ripple current, and small output voltage ripple. From the required output voltage ripple, use [Equation 16](#) and [Equation 17](#) to calculate the minimum required effective capacitance of the  $C_{\text{OUT}}$ .

Add a 0.1µF/0402 package ceramic capacitor and place it close to VOUT pin and GND pin to suppress high frequency noise which helps improve EMI performance.

#### 7.2.2.5 Output Current Limit

The output current limit is implemented by putting a current sense resistor between the ISP and ISN pins. The value of the limit voltage between the ISP and ISN pins is 50mV. The current sense resistor between the ISP and ISN pins is selected to specify that the output current limit is set high enough for output. The output current limit setting resistor is given by [Equation 18](#).

$$R_{\text{SNS}} = \frac{V_{\text{SNS}}}{I_{\text{OUT\_LIMIT}}} \quad (13)$$

where

- $V_{\text{SNS}}$  is the current limit setting voltage between the ISP and ISN pins
- $I_{\text{OUT\_LIMIT}}$  is the desired output current limit

Because the power dissipation is large, make sure the current sense resistor has enough power dissipation capability with large package.

#### 7.2.2.6 Loop Stability

The TPSM852892 uses average current control scheme. The inner current loop uses internal compensation. The outer voltage loop requires an external compensation. The COMP pin is the output of the internal voltage error amplifier. An external compensation network comprised of resistor and ceramic capacitors is connected to the COMP pin.

The TPSM852892 operates in buck mode or boost mode. Therefore, both buck and boost operating modes require loop compensations. The restrictive one of both compensations is selected as the overall compensation from a loop stability point of view. Typically for a converter designed either work in buck mode or boost mode, the boost mode compensation design is more restrictive due to the presence of a right half plane zero (RHPZ).

The power stage in boost mode can be modeled by [Equation 19](#).

$$G_{PS}(s) = \frac{R_{LOAD} \times (1-D)}{2 \times R_{SENSE}} \times \frac{\left(1 + \frac{s}{2\pi \times f_{ESRZ}}\right) \times \left(1 - \frac{s}{2\pi \times f_{RHPZ}}\right)}{1 + \frac{s}{2\pi \times f_P}} \quad (14)$$

where

- $R_{LOAD}$  is the output load resistance
- $D$  is the switching duty cycle in boost mode
- $R_{SENSE}$  is the equivalent internal current sense resistor, which is  $0.055\Omega$

The power stage has two zeros and one pole generated by the output capacitor and load resistance. Use [Equation 15](#) to [Equation 22](#) to calculate them.

$$f_P = \frac{2}{2\pi \times R_{LOAD} \times C_{OUT}} \quad (15)$$

$$f_{ESRZ} = \frac{1}{2\pi \times R_{COUT} \times C_{OUT}} \quad (16)$$

$$f_{RHPZ} = \frac{R_{LOAD} \times (1-D)^2}{2\pi \times L} \quad (17)$$

The internal transconductance amplifier together with the compensation network at the COMP pin constitutes the control portion of the loop. The transfer function of the control portion is shown by [Equation 23](#).

$$G_C(s) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{\left(1 + \frac{s}{2\pi \times f_{COMZ}}\right)}{\left(1 + \frac{s}{2\pi \times f_{COMP1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{COMP2}}\right)} \quad (18)$$

where

- $G_{EA}$  is the transconductance of the error amplifier
- $R_{EA}$  is the output resistance of the error amplifier
- $V_{REF}$  is the reference voltage input to the error amplifier
- $V_{OUT}$  is the output voltage
- $f_{COMP1}$  and  $f_{COMP2}$  are frequency of the pole of the compensation network
- $f_{COMZ}$  is the zero's frequency of the compensation network

The total open-loop gain is the product of  $G_{PS}(s)$  and  $G_C(s)$ . The next step is to choose the loop crossover frequency,  $f_C$ , at which the total open-loop gain is 1, namely 0dB. The higher in frequency that the loop gain stays above 0dB before crossing over, the faster the loop response. It is generally accepted that the loop gain cross over 0dB at the frequency no higher than the lower of either 1/10 of the switching frequency,  $f_{SW}$  or 1/5 of the RHPZ frequency,  $f_{RHPZ}$ .

Then, set the value of  $R_C$ ,  $C_C$ , and  $C_P$  by [Equation 24](#) to [Equation 26](#).

$$R_C = \frac{2\pi \times V_{OUT} \times R_{SENSE} \times C_{OUT} \times f_C}{(1-D) \times V_{REF} \times G_{EA}} \quad (19)$$

where

- $f_C$  is the selected crossover frequency



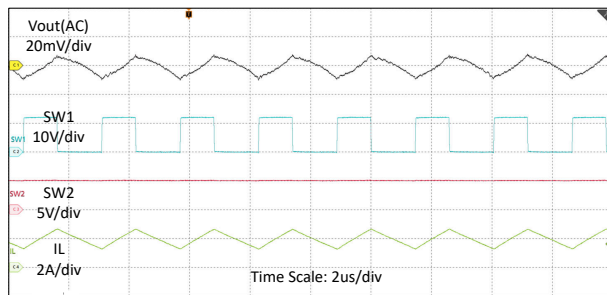
$$C_C = \frac{R_{LOAD} \times C_{OUT}}{2 \times R_C} \quad (20)$$

$$C_P = \frac{R_{COUT} \times C_{OUT}}{R_C} \quad (21)$$

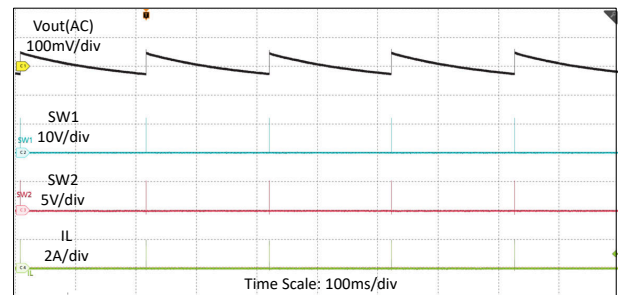
If the calculated  $C_P$  is less than 10pF, it can be left open.

Designing the loop for greater than 45° of phase margin and greater than 10dB gain margin eliminates output voltage ringing during the line and load transient.

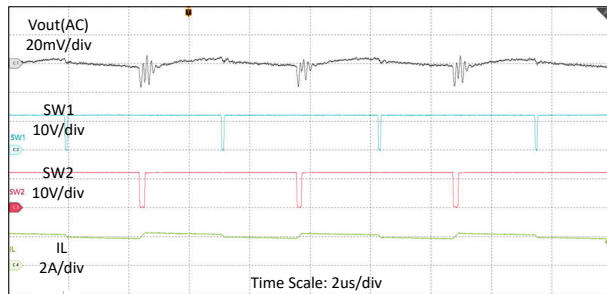
### 7.2.3 Application Curves



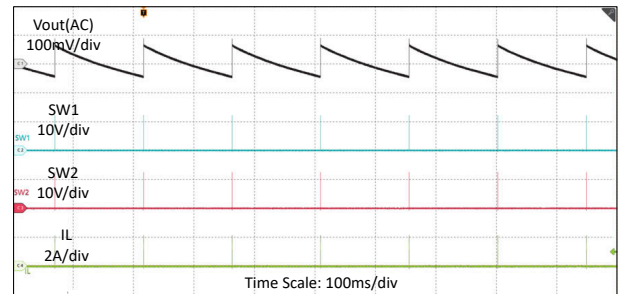
**Figure 7-2. Switching Waveforms in  $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $I_O = 2A$ , FPWM**



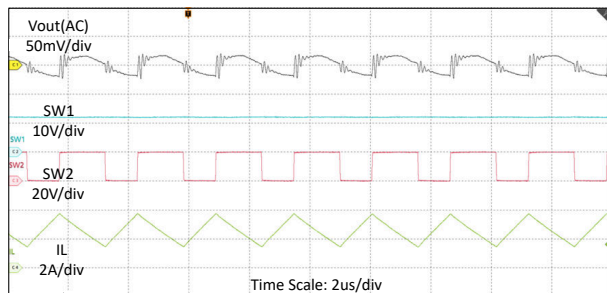
**Figure 7-3. Switching Waveforms in  $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $I_O = 0A$ , PFM**



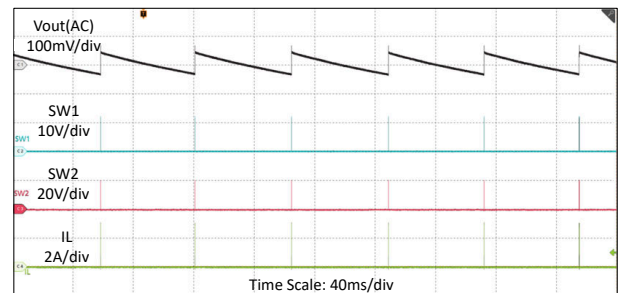
**Figure 7-4. Switching Waveforms in  $V_{IN} = 12V$ ,  $V_{OUT} = 12V$ ,  $I_O = 2A$ , FPWM**



**Figure 7-5. Switching Waveforms in  $V_{IN} = 12V$ ,  $V_{OUT} = 12V$ ,  $I_O = 0A$ , PFM**

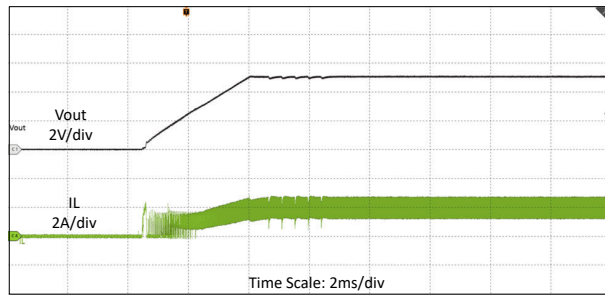


**Figure 7-6. Switching Waveforms in  $V_{IN} = 12V$ ,  $V_{OUT} = 20V$ ,  $I_O = 1.5A$ , FPWM**

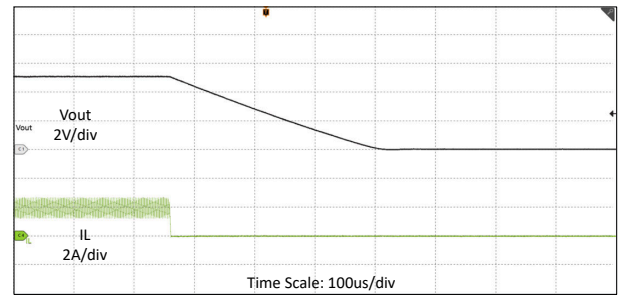


**Figure 7-7. Switching Waveforms in  $V_{IN} = 12V$ ,  $V_{OUT} = 20V$ ,  $I_O = 0A$ , PFM**

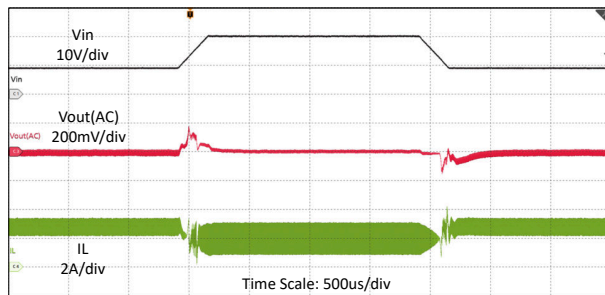
### 7.2.3 Application Curves (continued)



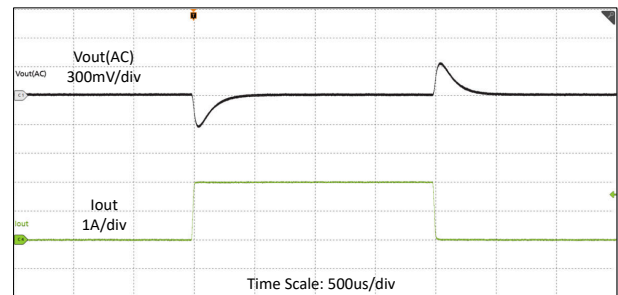
**Figure 7-8. Start-up Waveforms in  $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $R_{LOAD} = 2.5\Omega$ , FPWM**



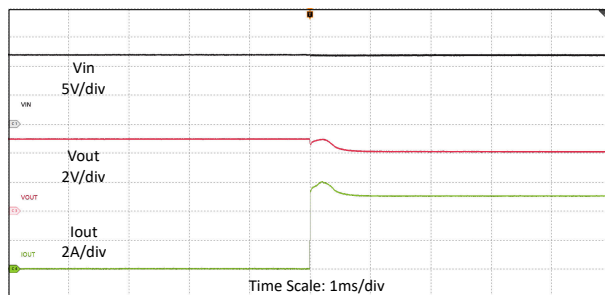
**Figure 7-9. Shutdown Waveforms in  $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $R_{LOAD} = 2.5\Omega$ , FPWM**



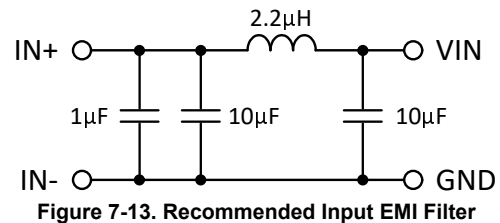
**Figure 7-10. Line Transient Waveforms in  $V_{IN} = 9V$  to  $20V$ ,  $V_{OUT} = 12V$ ,  $I_O = 2A$  with  $200\mu s$  Slew Rate, FPWM**



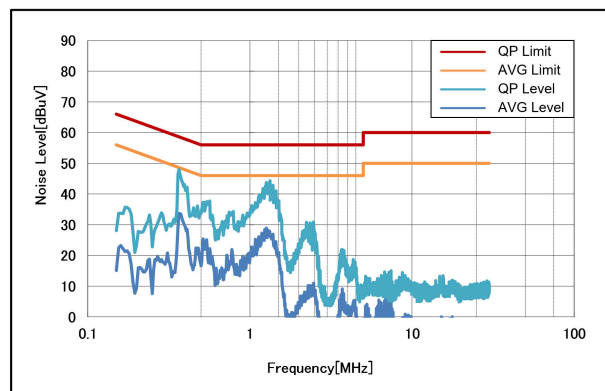
**Figure 7-11. Load Transient Waveforms in  $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $I_O = 0A$  to  $2A$  with  $20\mu s$  Slew Rate, FPWM**



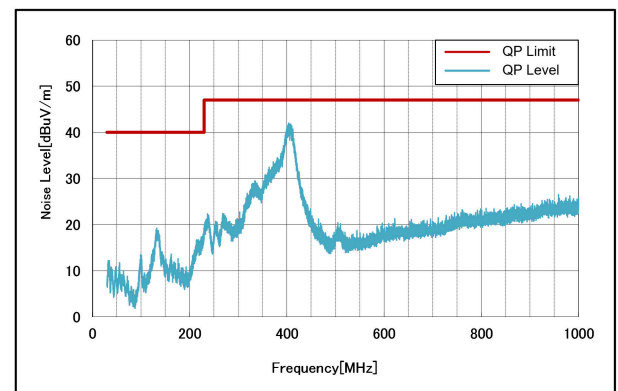
**Figure 7-12. Output Current Limit Waveforms in  $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $R_{LOAD} = 0.8\Omega$ ,  $R_{SNS} = 10m\Omega$ , FPWM**



**Figure 7-13. Recommended Input EMI Filter**

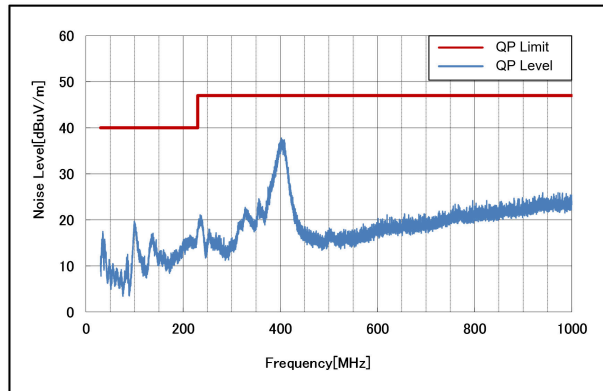


**Figure 7-14. CISPR 32 Class B Conducted Emissions in  $V_{IN} = 12V$ ,  $V_{OUT} = 9V$ ,  $R_{LOAD} = 3\Omega$ , FPWM, Spread Spectrum enabled**

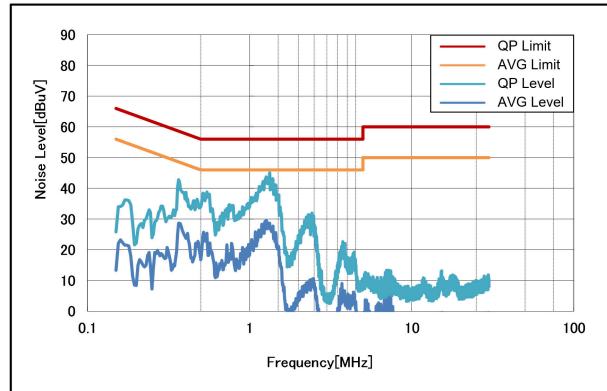


**Figure 7-15. CISPR 32 Class B Radiated Emissions - Horizontal in  $V_{IN} = 12V$ ,  $V_{OUT} = 9V$ ,  $R_{LOAD} = 3\Omega$ , FPWM, Spread Spectrum enabled**

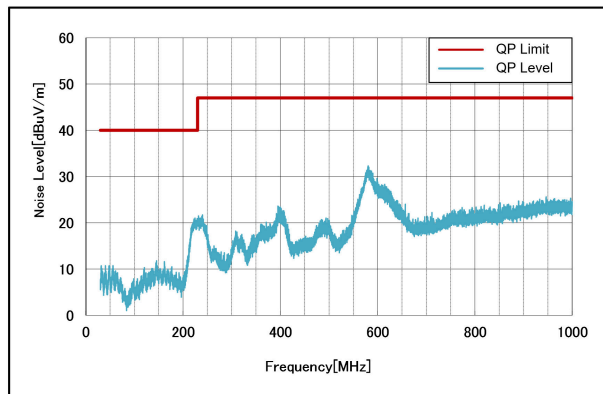
### 7.2.3 Application Curves (continued)



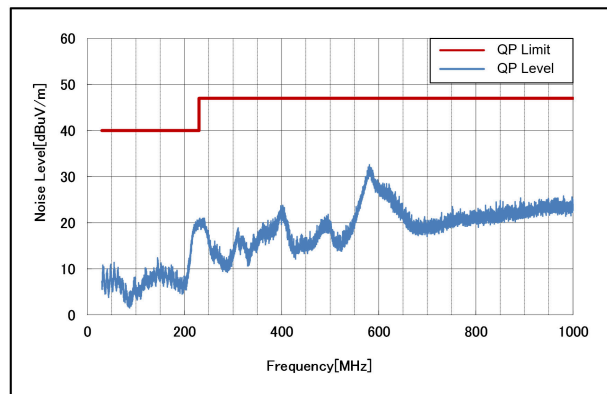
**Figure 7-16. CISPR 32 Class B Radiated Emissions - Vertical**  
in  $V_{IN} = 12V$ ,  $V_{OUT} = 9V$ ,  $R_{LOAD} = 3\Omega$ , FPWM, Spread Spectrum enabled



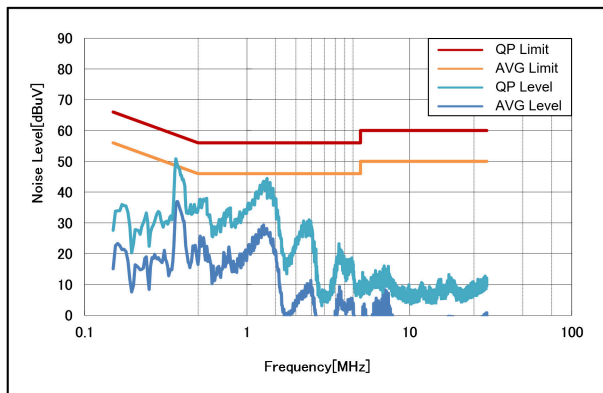
**Figure 7-17. CISPR 32 Class B Conducted Emissions in  $V_{IN} = 12V$ ,  $V_{OUT} = 12V$ ,  $R_{LOAD} = 6\Omega$ , FPWM, Spread Spectrum enabled**



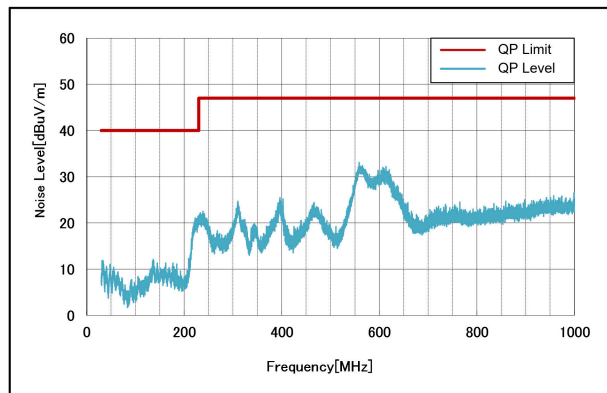
**Figure 7-18. CISPR 32 Class B Radiated Emissions - Horizontal**  
in  $V_{IN} = 12V$ ,  $V_{OUT} = 12V$ ,  $R_{LOAD} = 6\Omega$ , FPWM, Spread Spectrum enabled



**Figure 7-19. CISPR 32 Class B Radiated Emissions - Vertical**  
in  $V_{IN} = 12V$ ,  $V_{OUT} = 12V$ ,  $R_{LOAD} = 6\Omega$ , FPWM, Spread Spectrum enabled



**Figure 7-20. CISPR 32 Class B Conducted Emissions in  $V_{IN} = 12V$ ,  $V_{OUT} = 15V$ ,  $R_{LOAD} = 10\Omega$ , FPWM, Spread Spectrum enabled**



**Figure 7-21. CISPR 32 Class B Radiated Emissions - Horizontal**  
in  $V_{IN} = 12V$ ,  $V_{OUT} = 15V$ ,  $R_{LOAD} = 10\Omega$ , FPWM, Spread Spectrum enabled

### 7.2.3 Application Curves (continued)

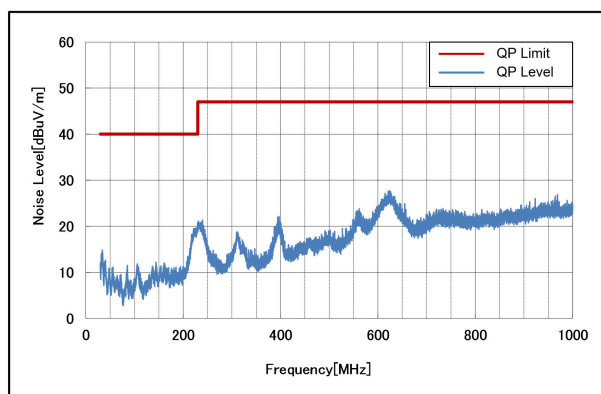


Figure 7-22. CISPR 32 Class B Radiated Emissions - Vertical in  $V_{IN} = 12V$ ,  $V_{OUT} = 15V$ ,  $R_{LOAD} = 10\Omega$ , FPWM, Spread Spectrum enabled

## 7.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 3.0V to 36V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. A typical choice is an aluminum electrolytic capacitor with a value of 100 $\mu$ F.

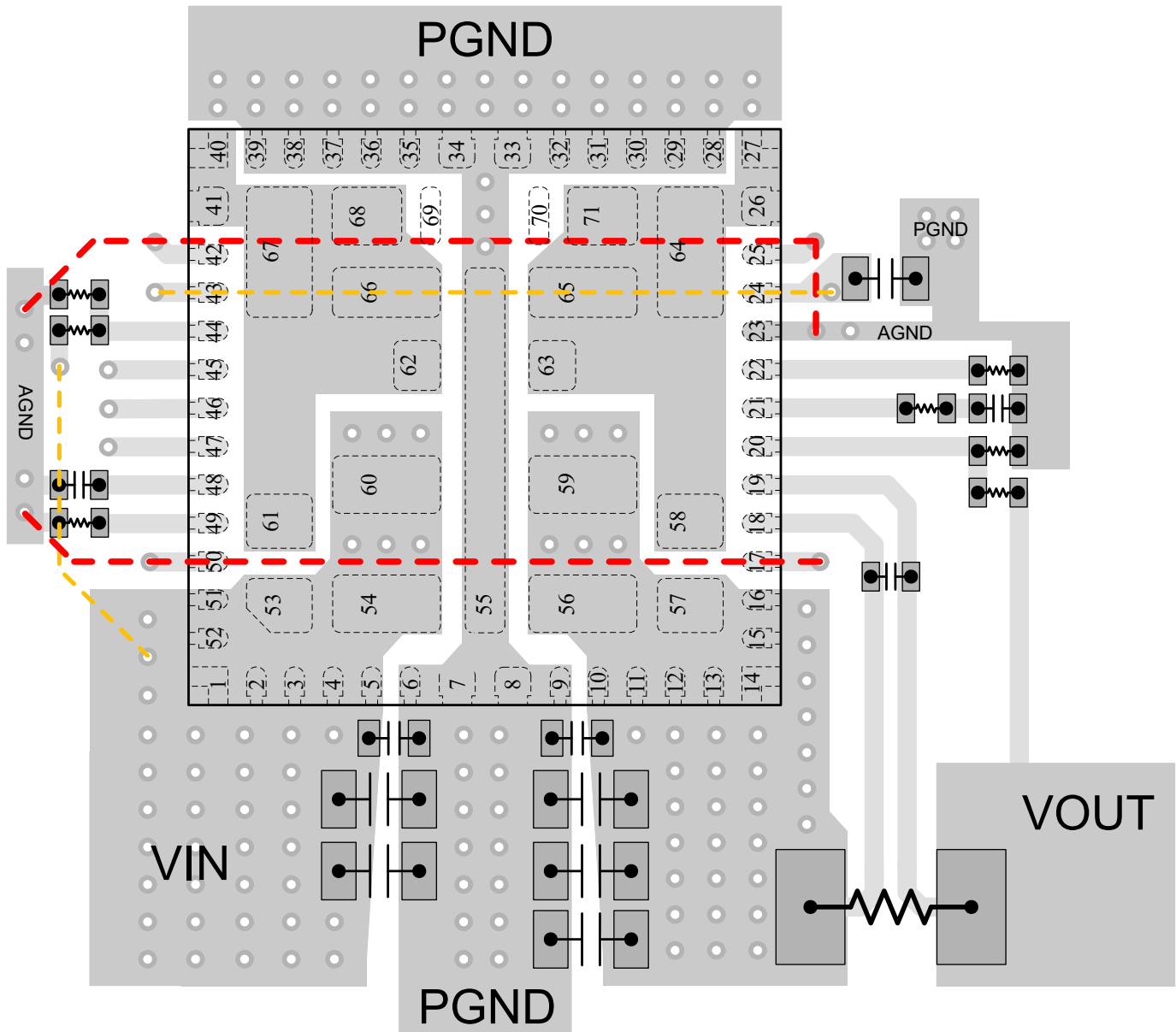
## 7.4 Layout

### 7.4.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator can suffer from instability and noise problems.

1. Place the 0.1 $\mu$ F small package (0402) ceramic capacitors close to the VIN/VOUT pins to minimize high frequency current loops, which improves the radiation of high-frequency noise (EMI) and efficiency.
2. Use multiple GND vias near PGND pin to connect the PGND to the internal ground plane, which also improves thermal performance.
3. Minimize the SW1 and L1, SW2 and L2 loop areas as these are high dv/dt nodes. Use a ground plane under the switching regulator to minimize interplane coupling.
4. Use Kelvin connections to RSENSE for the current sense signals ISP and ISN and run lines in parallel from the RSENSE terminals to the IC pins. Place the filter capacitor for the current sense signal as close to the IC pins as possible.
5. Place the VCC capacitor close to the IC with wide and short trace. The GND terminal of the VCC capacitor is directly connected with PGND plane through three to four vias.
6. Isolate the power ground from the analog ground. The PGND plane and AGND plane are connected at the terminal of the VCC capacitor. Thus the noise caused by the MOSFET driver and parasitic inductance does not interface with the AGND and internal control circuit.
7. Place the compensation components as close to the COMP pin as possible. Keep the compensation components, feedback components, and other sensitive analog circuitry far away from the power components and high-current trace to prevent noise coupling into the analog signals.
8. To improve thermal performance, it is recommended to use thermal vias beneath the TPSM852892 connecting the VIN pin to a large VIN area, and the VOUT pin to a large VOUT area separately.

## 7.4.2 Layout Example



- trace on bottom layer
- AGND plane on an inner layer

The first inner layer is the PGND plane

Figure 7-23. Layout Example

## 8 Device and Documentation Support

### 8.1 Device Support

#### 8.1.1 Third-Party Products Disclaimer

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### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 8.4 Trademarks

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All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

DATE	REVISION	NOTES
December 2025	*	Initial Release

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM852892RCMR	Active	Production	QFN-FCMOD (RCM)   71	750   LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 125	T852892

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

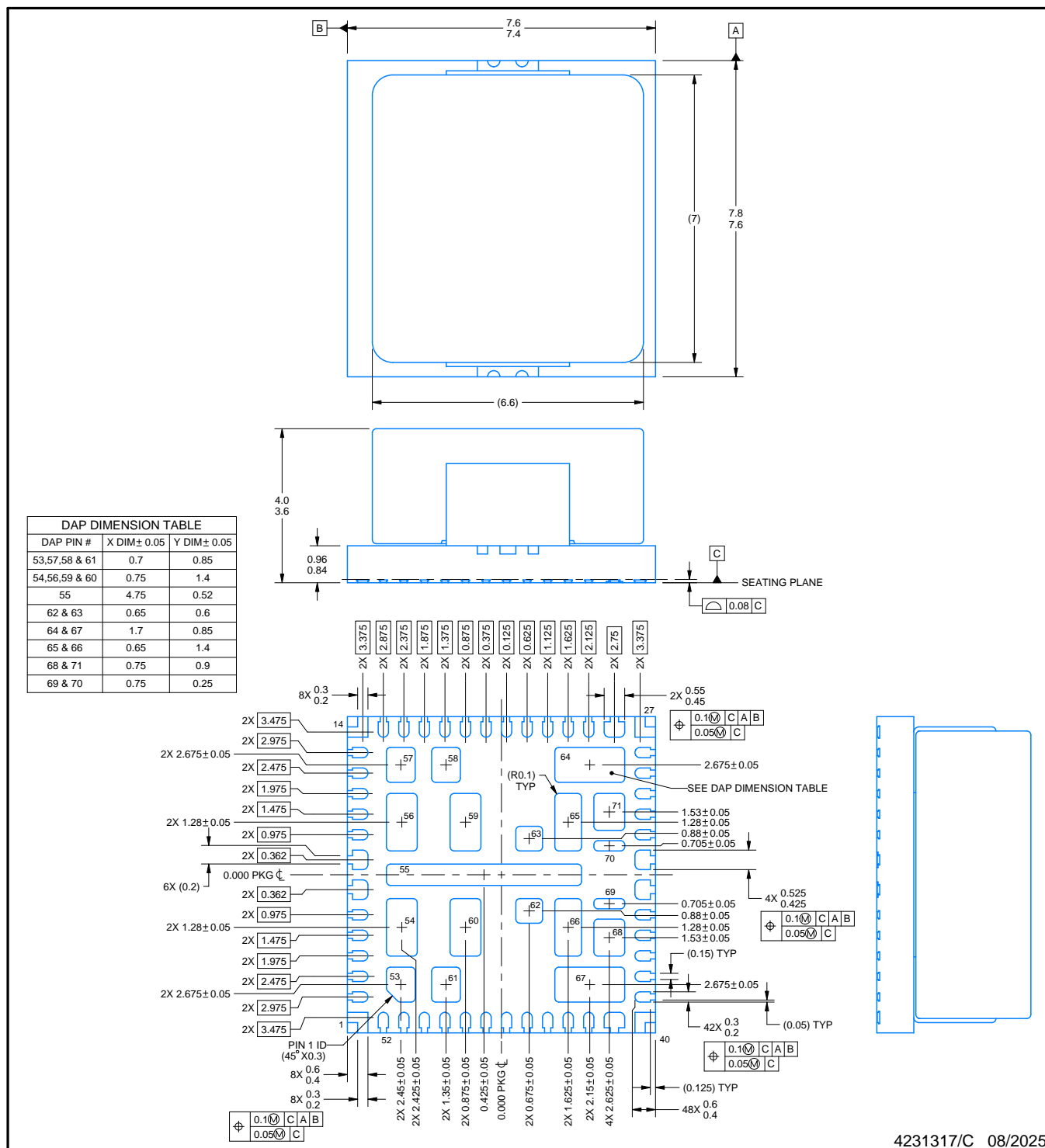
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.





## QFN-FCMOD - 4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

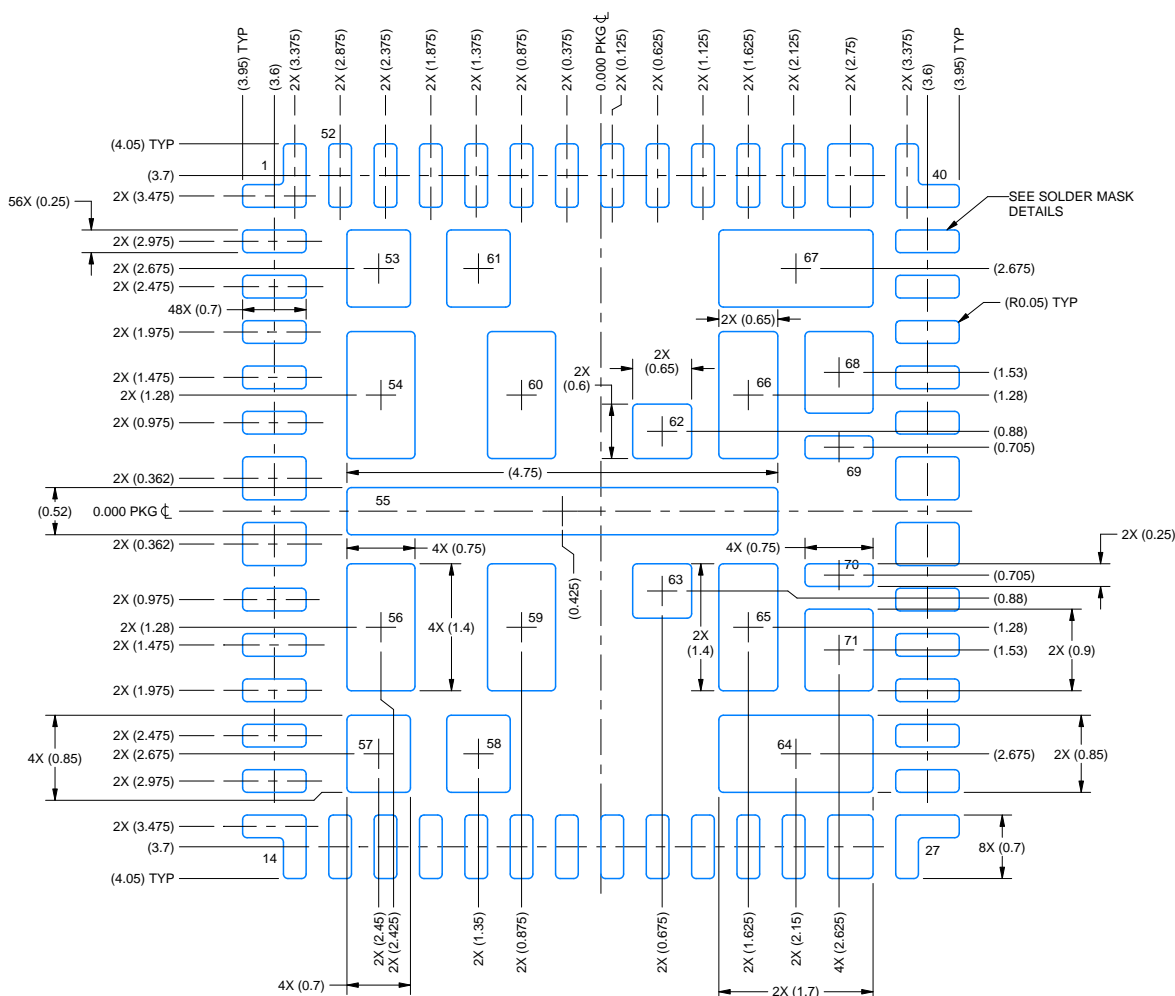
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

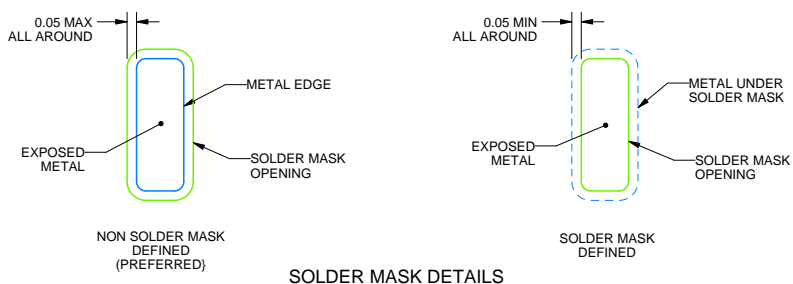
RCM0071A

QFN-FCMOD - 4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 12X



SOLDER MASK DETAILS

4231317/C 08/2025

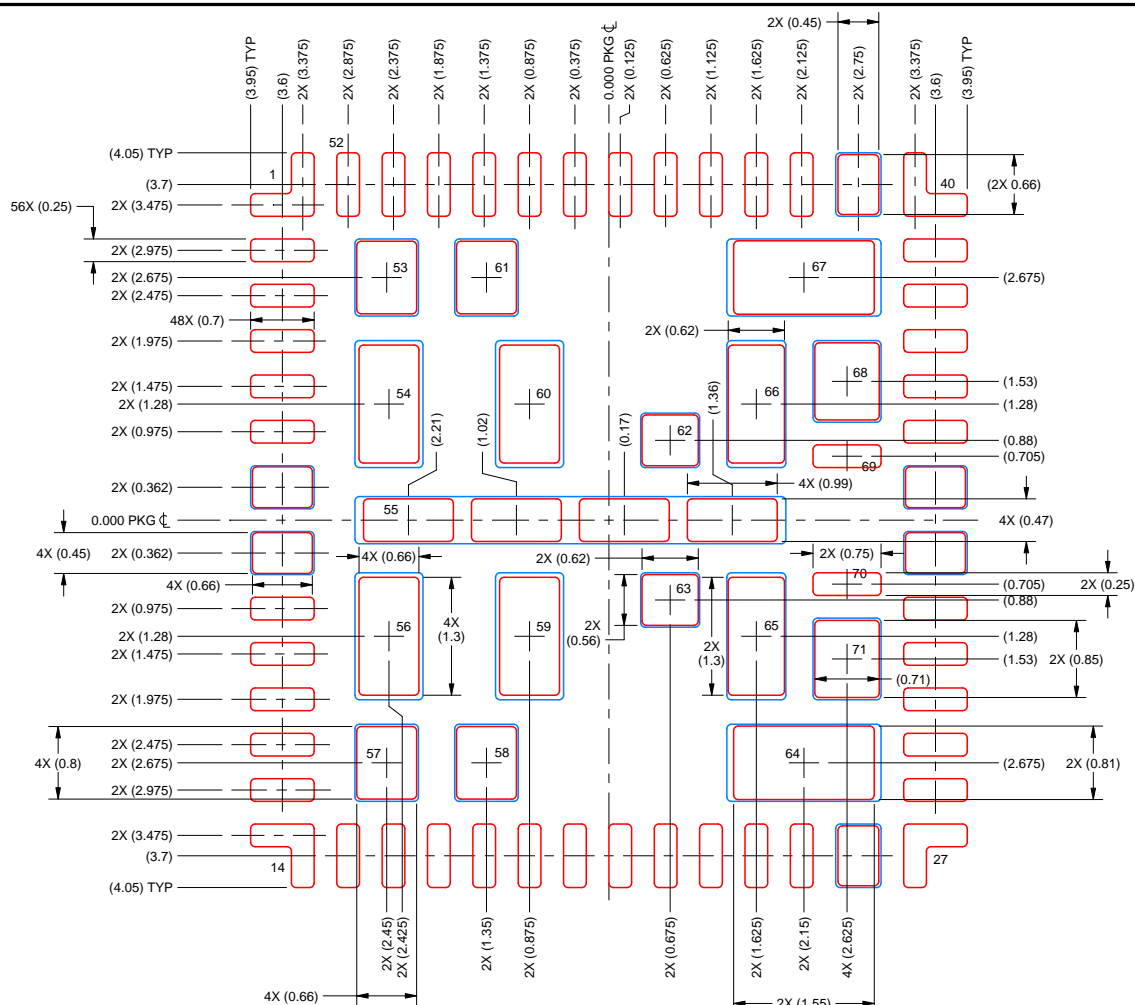
NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**RCM0071A**

## QFN-FCMOD - 4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
**BASED ON 0.125 mm THICK STENCIL**  
**SCALE: 12X**

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
PADS 53, 57, 58, 61, 62, 63, 65, 66, 68 & 71: 89%  
PADS: 54, 56, 59 & 60: 82%  
PAD 55: 75%  
PADS 64 & 67: 87%

4231317/C 08/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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