

## TS5A3166 0.9-Ω SPST Analog Switch

### 1 Features

- Low ON-State Resistance (0.9 Ω)
- Control Inputs Are 5.5-V Tolerant
- Low Charge Injection
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals
- Microphone Switching – Notebook Docking

### 3 Description

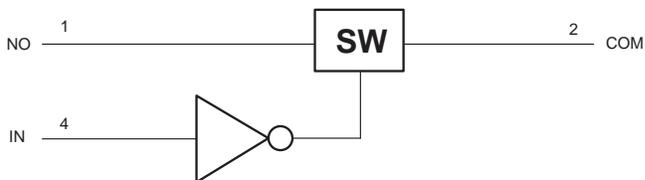
The TS5A3166 device is a single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A3166	SOT-23 (5)	2.90 mm × 1.60 mm
	SC70 (5)	2.00 mm × 1.25 mm
	DSBGA (5)	1.388 mm × 0.888 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Simplified Schematic



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (February 2016) to Revision E	Page
• Changed the YZP package pin numbers .....	3

Changes from Revision C (May 2015) to Revision D	Page
• Added "port" to COM description in <i>Pin Functions</i> table .....	3
• Deleted "digital" from GND description in <i>Pin Functions</i> table .....	3

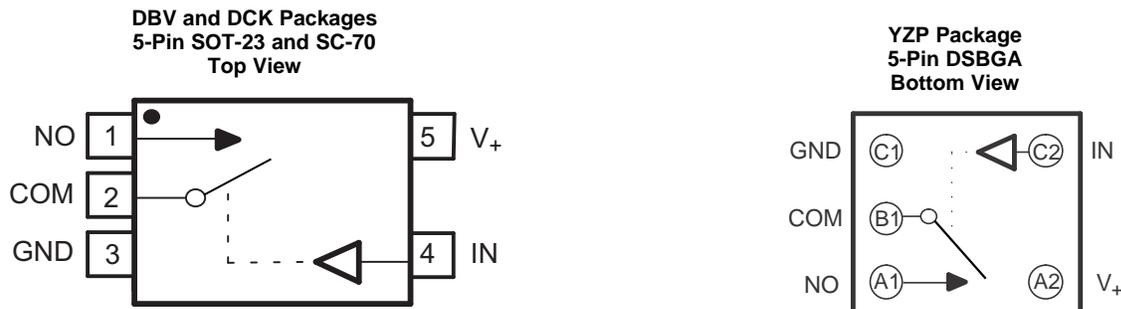
  

Changes from Revision B (September 2013) to Revision C	Page
• Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> , <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. ....	1
• Deleted <i>Ordering Information</i> table. ....	1

Changes from Revision A (October 2012) to Revision B	Page
• Removed 'Isolation in Powered-Off Mode, $V_+ = 0$ ' bullet from <i>Features</i> .....	1
• Changed pin name from NC to NO throughout the datasheet. ....	1

## 5 Pin Configuration and Functions



Pin Functions

PIN		NAME	TYPE	DESCRIPTION
DBC, DCK NO.	YZP NO.			
1	A1	NO	I/O	Normally opened port
2	B1	COM	I/O	Common port
3	C1	GND	GND	Ground
4	C2	IN	I	Digital control pin to connect COM to NO
5	A2	V <sub>+</sub>	Power	Power Supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

		MIN	MAX	UNIT
V <sub>+</sub>	Supply voltage <sup>(3)</sup>	-0.5	6.5	V
V <sub>NO</sub> V <sub>COM</sub>	Analog voltage <sup>(3)(4)(5)</sup>	-0.5	V <sub>+</sub> + 0.5	V
I <sub>K</sub>	Analog port diode current	V <sub>NO</sub> , V <sub>COM</sub> < 0		mA
I <sub>NO</sub> I <sub>COM</sub>	ON-state switch current ON-state peak switch current <sup>(6)</sup>	V <sub>NO</sub> , V <sub>COM</sub> = 0 to V <sub>+</sub>		mA
V <sub>I</sub>	Digital input voltage <sup>(3)(4)</sup>	-0.5	6.5	V
I <sub>IK</sub>	Digital clamp current	V <sub>I</sub> < 0		mA
I <sub>+</sub>	Continuous current through V <sub>+</sub>			100 mA
I <sub>GND</sub>	Continuous current through GND			-100 mA
T <sub>stg</sub>	Storage temperature	-65	150	°C
T <sub>j</sub>	Junction temperature			150 °C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Pulse at 1-ms duration < 10% duty cycle.

## 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	$V_+$	V
$V_+$	Supply voltage	1.65	5.5	V
$V_I$	Control Input Voltage	0	5.5	V
$T_A$	Operating free-air temperature	−40	85	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	TS5A3166			UNIT
	DBV (SOT)	DCK (SC-70)	YZP (DSBGA)	
	5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	206	252	132	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics for 5-V Supply

$V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT		
<b>Analog Switch</b>									
$V_{COM}, V_{NO}$	Analog signal range			0		$V_+$	V		
$r_{peak}$	Peak ON resistance	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -100\text{ mA}$	Switch ON, see <a href="#">Figure 13</a>	25°C	4.5 V	0.8	1.1	$\Omega$	
				Full		1.2			
$r_{on}$	ON-state resistance	$V_{NO} = 2.5\text{ V}$ , $I_{COM} = -100\text{ mA}$	Switch ON, see <a href="#">Figure 13</a>	25°C	4.5 V	0.7	0.9	$\Omega$	
				Full		1			
$r_{on(flat)}$	ON-state resistance flatness	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -100\text{ mA}$	Switch ON, see <a href="#">Figure 13</a>	25°C	4.5 V	0.15		$\Omega$	
				25°C		0.09	0.15		
				Full			0.15		
$I_{NO(OFF)}$	NO OFF leakage current	$V_{NO} = 1\text{ V}$ , $V_{COM} = 4.5\text{ V}$ , or $V_{NO} = 4.5\text{ V}$ , $V_{COM} = 1\text{ V}$	Switch OFF, see <a href="#">Figure 14</a>	25°C	5.5 V	−20	4	20	nA
				Full		−100		100	
$I_{NO(PWROFF)}$		$V_{NO} = 0\text{ to }5.5\text{ V}$ , $V_{COM} = 5.5\text{ V to }0$		25°C	0 V	−5	0.4	5	$\mu\text{A}$
				Full		−15		15	
$I_{COM(OFF)}$	COM OFF leakage current	$V_{COM} = 1\text{ V}$ , $V_{NO} = 4.5\text{ V}$ , or $V_{COM} = 4.5\text{ V}$ , $V_{NO} = 1\text{ V}$	Switch OFF, see <a href="#">Figure 14</a>	25°C	5.5 V	−20	4	20	nA
				Full		−100		100	
$I_{COM(PWROFF)}$		$V_{COM} = 5.5\text{ V to }0$ , $V_{NO} = 0\text{ to }5.5\text{ V}$		25°C	0 V	−5	0.4	5	$\mu\text{A}$
				Full		−15		15	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

**Electrical Characteristics for 5-V Supply (continued)**
 $V_+ = 4.5 \text{ V to } 5.5 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT
$I_{\text{NO(ON)}}$	NO ON leakage current	$V_{\text{NO}} = 1 \text{ V}$ , $V_{\text{COM}} = \text{Open}$ , or $V_{\text{NO}} = 4.5 \text{ V}$ , $V_{\text{COM}} = \text{Open}$ ,	Switch ON, see <a href="#">Figure 15</a>	25°C	5.5 V	-2	0.3	2	nA
				Full		-20		20	
$I_{\text{COM(ON)}}$	COM ON leakage current	$V_{\text{COM}} = 1 \text{ V}$ , $V_{\text{NO}} = \text{Open}$ , or $V_{\text{COM}} = 4.5 \text{ V}$ , $V_{\text{NO}} = \text{Open}$ ,	Switch ON, see <a href="#">Figure 15</a>	25°C	5.5 V	-2	0.3	2	nA
				Full		-20		20	
<b>Digital Control Inputs (IN)</b>									
$V_{\text{IH}}$	Input logic high			Full		2.4		5.5	V
$V_{\text{IL}}$	Input logic low			Full		0		0.8	V
$I_{\text{IH}}, I_{\text{IL}}$	Input leakage current	$V_{\text{I}} = 5.5 \text{ V or } 0$		25°C	5.5 V	-2	0.3	2	nA
				Full		-20		20	
<b>Dynamic</b>									
$t_{\text{ON}}$	Turnon time	$V_{\text{COM}} = V_+$ , $R_{\text{L}} = 50 \Omega$ ,	$C_{\text{L}} = 35 \text{ pF}$ , see <a href="#">Figure 17</a>	25°C	5 V	2.5	4.5	7	ns
				Full	4.5 V to 5.5 V	1.5		7.5	
$t_{\text{OFF}}$	Turnoff time	$V_{\text{COM}} = V_+$ , $R_{\text{L}} = 50 \Omega$ ,	$C_{\text{L}} = 35 \text{ pF}$ , see <a href="#">Figure 17</a>	25°C	5 V	6	9	11.5	ns
				Full	4.5 V to 5.5 V	4		12.5	
$Q_{\text{C}}$	Charge injection	$V_{\text{GEN}} = 0$ , $R_{\text{GEN}} = 0$ ,	$C_{\text{L}} = 1 \text{ nF}$ , see <a href="#">Figure 20</a>	25°C	5 V		1		pC
$C_{\text{NO(OFF)}}$	NO OFF capacitance	$V_{\text{NO}} = V_+$ or GND, Switch OFF,	See <a href="#">Figure 16</a>	25°C	5 V		19		pF
$C_{\text{COM(OFF)}}$	COM OFF capacitance	$V_{\text{COM}} = V_+$ or GND, Switch OFF,	See <a href="#">Figure 16</a>	25°C	5 V		18		pF
$C_{\text{NO(ON)}}$	NO ON capacitance	$V_{\text{NO}} = V_+$ or GND, Switch ON,	See <a href="#">Figure 16</a>	25°C	5 V		35.5		pF
$C_{\text{COM(ON)}}$	COM ON capacitance	$V_{\text{COM}} = V_+$ or GND, Switch ON,	See <a href="#">Figure 16</a>	25°C	5 V		35.5		pF
$C_{\text{I}}$	Digital input capacitance	$V_{\text{I}} = V_+$ or GND,	See <a href="#">Figure 16</a>	25°C	5 V		2		pF
BW	Bandwidth	$R_{\text{L}} = 50 \Omega$ , Switch ON,	See <a href="#">Figure 18</a>	25°C	5 V		200		MHz
$O_{\text{ISO}}$	OFF isolation	$R_{\text{L}} = 50 \Omega$ , $f = 1 \text{ MHz}$ ,	Switch OFF, see <a href="#">Figure 19</a>	25°C	5 V		-64		dB
THD	Total harmonic distortion	$R_{\text{L}} = 600 \Omega$ , $C_{\text{L}} = 50 \text{ pF}$ ,	$f = 20 \text{ Hz to } 20 \text{ kHz}$ , see <a href="#">Figure 21</a>	25°C	5 V		0.005%		
<b>Supply</b>									
$I_+$	Positive supply current	$V_{\text{I}} = V_+$ or GND,	Switch ON or OFF	25°C	5.5 V		0.01	0.1	$\mu\text{A}$
				Full				0.5	

## 6.6 Electrical Characteristics for 3.3-V Supply

 $V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>										
$V_{COM}, V_{NO}$	Analog signal range					0		$V_+$	V	
$r_{peak}$	Peak ON resistance	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, see <a href="#">Figure 13</a>	25°C	3 V		1.1	1.5	$\Omega$	
				Full			1.7			
$r_{on}$	ON-state resistance	$V_{NO} = 2\text{ V}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, see <a href="#">Figure 13</a>	25°C	3 V		1	1.4	$\Omega$	
				Full			1.5			
$r_{on(Flat)}$	ON-state resistance flatness	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, see <a href="#">Figure 13</a>	25°C	3 V		0.3		$\Omega$	
				25°C			0.09	0.15		
				Full			0.15			
$I_{NO(OFF)}$	NO OFF leakage current	$V_{NO} = 1\text{ V}$ , $V_{COM} = 3\text{ V}$ , or $V_{NO} = 3\text{ V}$ , $V_{COM} = 1\text{ V}$ ,	Switch OFF, see <a href="#">Figure 14</a>	25°C	3.6 V		-2	0.5	2	nA
				Full			-20	20		
$I_{NO(PWROFF)}$		$V_{NO} = 0\text{ to }3.6\text{ V}$ , $V_{COM} = 3.6\text{ V to }0$ ,		25°C	0 V		-1	0.1	1	$\mu\text{A}$
				Full			-5	5		
$I_{COM(OFF)}$	COM OFF leakage current	$V_{COM} = 1\text{ V}$ , $V_{NO} = 3\text{ V}$ , or $V_{COM} = 3\text{ V}$ , $V_{NO} = 1\text{ V}$ ,	Switch OFF, see <a href="#">Figure 14</a>	25°C	3.6 V		-2	0.5	2	nA
				Full			-20	20		
$I_{COM(PWROFF)}$		$V_{COM} = 3.6\text{ V to }0$ , $V_{NO} = 0\text{ to }3.6\text{ V}$ ,		25°C	0 V		-1	0.1	1	$\mu\text{A}$
				Full			-5	5		
$I_{NO(ON)}$	NO ON leakage current	$V_{NO} = 1\text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NO} = 3\text{ V}$ , $V_{COM} = \text{Open}$ ,	Switch ON, see <a href="#">Figure 15</a>	25°C	3.6 V		-2	0.2	2	nA
				Full			-20	20		
$I_{COM(ON)}$	COM ON leakage current	$V_{COM} = 1\text{ V}$ , $V_{NO} = \text{Open}$ , or $V_{COM} = 3\text{ V}$ , $V_{NO} = \text{Open}$ ,	Switch ON, see <a href="#">Figure 15</a>	25°C	3.6 V		-2	0.2	2	nA
				Full			-20	20		
<b>Digital Control Inputs (IN)</b>										
$V_{IH}$	Input logic high			Full		2		5.5	V	
$V_{IL}$	Input logic low			Full		0		0.8	V	
$I_{IH}, I_{IL}$	Input leakage current	$V_I = 5.5\text{ V or }0$		25°C	3.6 V		-2	0.3	2	nA
				Full			-20	20		
<b>Dynamic</b>										
$t_{ON}$	Turnon time	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , see <a href="#">Figure 17</a>	25°C	3.3 V	2	5	10	ns	
				Full	3 V to 3.6 V	1.5		11		
$t_{OFF}$	Turnoff time	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , see <a href="#">Figure 17</a>	25°C	3.3 V	6.5	9	12	ns	
				Full	3 V to 3.6 V	4		13		
$Q_C$	Charge injection	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1\text{ nF}$ , see <a href="#">Figure 21</a>	25°C	3.3 V		1		pC	
$C_{NO(OFF)}$	NO OFF capacitance	$V_{NO} = V_+$ or GND, Switch OFF,	See <a href="#">Figure 16</a>	25°C	3.3 V		19		pF	
$C_{COM(OFF)}$	COM OFF capacitance	$V_{COM} = V_+$ or GND, Switch OFF,	See <a href="#">Figure 16</a>	25°C	3.3 V		18		pF	
$C_{NO(ON)}$	NO ON capacitance	$V_{NO} = V_+$ or GND, Switch ON,	See <a href="#">Figure 16</a>	25°C	3.3 V		36		pF	
$C_{COM(ON)}$	COM ON capacitance	$V_{COM} = V_+$ or GND, Switch ON,	See <a href="#">Figure 16</a>	25°C	3.3 V		36		pF	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## Electrical Characteristics for 3.3-V Supply (continued)

 $V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT
$C_I$	Digital input capacitance	$V_I = V_+$ or GND,	See Figure 16	25°C	3.3 V		2		pF
BW	Bandwidth	$R_L = 50\ \Omega$ , Switch ON,	See Figure 18	25°C	3.3 V		200		MHz
$O_{ISO}$	OFF isolation	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch OFF, see Figure 19	25°C	3.3 V		-64		dB
THD	Total harmonic distortion	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ , see Figure 21	25°C	3.3 V		0.01%		
<b>Supply</b>									
$I_+$	Positive supply current	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	3.6 V		0.01	0.1	$\mu\text{A}$
				Full			0.25		

## 6.7 Electrical Characteristics for 2.5-V Supply

 $V_+ = 2.3\text{ V to }2.7\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>									
$V_{COM}$ , $V_{NO}$	Analog signal range				2.3 V	0		$V_+$	V
$r_{peak}$	Peak ON resistance	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, see Figure 13	25°C	2.3 V		1.8	2.4	$\Omega$
				Full				2.6	
$r_{on}$	ON-state resistance	$V_{NO} = 2\text{ V}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, see Figure 13	25°C	2.3 V		1.2	2.1	$\Omega$
				Full				2.4	
$r_{on(Flat)}$	ON-state resistance flatness	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -100\text{ mA}$ , $V_{NO} = 2\text{ V}, 0.8\text{ V}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, see Figure 13	25°C	2.3 V		0.7		$\Omega$
				25°C			0.4	0.6	
				Full				0.6	
$I_{NO(OFF)}$	NO OFF leakage current	$V_{NO} = 1\text{ V}$ , $V_{COM} = 3\text{ V}$ , or $V_{NO} = 3\text{ V}$ , $V_{COM} = 1\text{ V}$ ,	Switch OFF, see Figure 14	25°C	2.7 V	-5	0.3	5	nA
				Full			-50		
$I_{NO(PWROFF)}$		$V_{NO} = 0\text{ to }3.6\text{ V}$ , $V_{COM} = 3.6\text{ V to }0$ ,		25°C	0 V	-2	0.05	2	$\mu\text{A}$
				Full			-15		
$I_{COM(OFF)}$	COM OFF leakage current	$V_{COM} = 1\text{ V}$ , $V_{NO} = 3\text{ V}$ , or $V_{COM} = 3\text{ V}$ , $V_{NO} = 1\text{ V}$ ,	Switch OFF, see Figure 14	25°C	2.7 V	-5	0.3	5	nA
				Full			-50		
$I_{COM(PWROFF)}$		$V_{COM} = 3.6\text{ V to }0$ , $V_{NO} = 0\text{ to }3.6\text{ V}$ ,		25°C	0 V	-2	0.05	2	$\mu\text{A}$
				Full			-15		
$I_{NO(ON)}$	NO ON leakage current	$V_{NO} = 1\text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NO} = 3\text{ V}$ , $V_{COM} = \text{Open}$ ,	Switch ON, see Figure 15	25°C	2.7 V	-2	0.3	2	nA
				Full			-20		
$I_{COM(ON)}$	COM ON leakage current	$V_{COM} = 1\text{ V}$ , $V_{NO} = \text{Open}$ , or $V_{COM} = 3\text{ V}$ , $V_{NO} = \text{Open}$ ,	Switch ON, see Figure 15	25°C	2.7 V	-2	0.3	2	nA
				Full			-20		
<b>Digital Control Inputs (IN1, IN2)</b>									
$V_{IH}$	Input logic high			Full		1.8		5.5	V
$V_{IL}$	Input logic low			Full		0		0.6	V

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

**Electrical Characteristics for 2.5-V Supply (continued)**
 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT
$I_{IH}$ , $I_{IL}$	Input leakage current	$V_I = 5.5 \text{ V or } 0$		25°C	2.7 V	-2	0.3	2	nA
				Full		-20		20	
<b>Dynamic</b>									
$t_{ON}$	Turnon time	$V_{COM} = V_+$ , $R_L = 50 \Omega$ ,	$C_L = 35 \text{ pF}$ , see <a href="#">Figure 17</a>	25°C	2.5 V	2	6	10	ns
				Full	2.3 V to 2.7 V	1		12	
$t_{OFF}$	Turnoff time	$V_{COM} = V_+$ , $R_L = 50 \Omega$ ,	$C_L = 35 \text{ pF}$ , see <a href="#">Figure 17</a>	25°C	2.5 V	4.5	8	10.5	ns
				Full	2.3 V to 2.7 V	3		15	
$Q_C$	Charge injection	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1 \text{ nF}$ , see <a href="#">Figure 21</a>	25°C	2.5 V		4		pC
$C_{NO(OFF)}$	NO OFF capacitance	$V_{NO} = V_+$ or GND, Switch OFF,	See <a href="#">Figure 16</a>	25°C	2.5 V		19.5		pF
$C_{COM(OFF)}$	COM OFF capacitance	$V_{COM} = V_+$ or GND, Switch OFF,	See <a href="#">Figure 16</a>	25°C	2.5 V		18.5		pF
$C_{NO(ON)}$	NO ON capacitance	$V_{NO} = V_+$ or GND, Switch ON,	See <a href="#">Figure 16</a>	25°C	2.5 V		36.5		pF
$C_{COM(ON)}$	COM ON capacitance	$V_{COM} = V_+$ or GND, Switch ON,	See <a href="#">Figure 16</a>	25°C	2.5 V		36.5		pF
$C_I$	Digital input capacitance	$V_I = V_+$ or GND,	See <a href="#">Figure 16</a>	25°C	2.5 V		2		pF
BW	Bandwidth	$R_L = 50 \Omega$ , Switch ON,	See <a href="#">Figure 18</a>	25°C	2.5 V		150		MHz
$O_{ISO}$	OFF isolation	$R_L = 50 \Omega$ , $f = 1 \text{ MHz}$ ,	Switch OFF, see <a href="#">Figure 19</a>	25°C	2.5 V		-62		dB
THD	Total harmonic distortion	$R_L = 600 \Omega$ , $C_L = 50 \text{ pF}$ ,	$f = 20 \text{ Hz to } 20 \text{ kHz}$ , see <a href="#">Figure 21</a>	25°C	2.5 V		0.02%		
<b>Supply</b>									
$I_+$	Positive supply current	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	2.7 V		0.001	0.02	$\mu\text{A}$
				Full				0.25	

## 6.8 Electrical Characteristics for 1.8-V Supply<sup>(1)</sup>

 $V_+ = 1.65 \text{ V to } 1.95 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>										
$V_{COM}, V_{NO}$	Analog signal range					0		$V_+$	V	
$r_{peak}$	Peak ON resistance	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -100 \text{ mA}$ ,	Switch ON, see <a href="#">Figure 13</a>	25°C	1.65 V		4.2	25	$\Omega$	
				Full			30			
$r_{on}$	ON-state resistance	$V_{NO} = 2 \text{ V}$ , $I_{COM} = -100 \text{ mA}$ ,	Switch ON, see <a href="#">Figure 13</a>	25°C	1.65 V		1.6	3.9	$\Omega$	
				Full			4.0			
$r_{on(Flat)}$	ON-state resistance flatness	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -100 \text{ mA}$ ,	Switch ON, see <a href="#">Figure 13</a>	25°C	1.65 V		2.8		$\Omega$	
				25°C			4.1	22		
				Full				27		
$I_{NO(OFF)}$	NO OFF leakage current	$V_{NO} = 1 \text{ V}$ , $V_{COM} = 3 \text{ V}$ , or $V_{NO} = 3 \text{ V}$ , $V_{COM} = 1 \text{ V}$ ,	Switch OFF, see <a href="#">Figure 14</a>	25°C	1.95 V		-5	5	nA	
				Full			-50	50		
$I_{NO(PWROFF)}$		$V_{NO} = 0 \text{ to } 3.6 \text{ V}$ , $V_{COM} = 3.6 \text{ V to } 0$ ,		25°C	0 V		-2	2	$\mu\text{A}$	
				Full			-10	10		
$I_{COM(OFF)}$	COM OFF leakage current	$V_{COM} = 1 \text{ V}$ , $V_{NO} = 3 \text{ V}$ , or $V_{COM} = 3 \text{ V}$ , $V_{NO} = 1 \text{ V}$ ,	Switch OFF, see <a href="#">Figure 14</a>	25°C	1.95 V		-5	5	nA	
				Full			-50	50		
$I_{COM(PWROFF)}$		$V_{COM} = 0 \text{ to } 3.6 \text{ V}$ , $V_{NO} = 3.6 \text{ V to } 0$ ,		25°C	0 V		-2	2	$\mu\text{A}$	
				Full			-10	10		
$I_{NO(ON)}$	NO ON leakage current	$V_{NO} = 1 \text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NO} = 3 \text{ V}$ , $V_{COM} = \text{Open}$ ,	Switch ON, see <a href="#">Figure 15</a>	25°C	1.95 V		-2	2	nA	
				Full			-20	20		
$I_{COM(ON)}$	COM ON leakage current	$V_{COM} = 1 \text{ V}$ , $V_{NO} = \text{Open}$ , or $V_{COM} = 3 \text{ V}$ , $V_{NO} = \text{Open}$ ,	Switch ON, see <a href="#">Figure 15</a>	25°C	1.95 V		-2	2	nA	
				Full			-20	20		
<b>Digital Control Inputs (IN1, IN2)</b>										
$V_{IH}$	Input logic high			Full		1.5		5.5	V	
$V_{IL}$	Input logic low			Full		0		0.6	V	
$I_{IH}, I_{IL}$	Input leakage current	$V_I = 5.5 \text{ V or } 0$		25°C	1.95 V		-2	0.3	2	nA
				Full			-20	20		
<b>Dynamic</b>										
$t_{ON}$	Turnon time	$V_{COM} = V_+$ , $R_L = 50 \Omega$ ,	$C_L = 35 \text{ pF}$ , see <a href="#">Figure 17</a>	25°C	1.8 V		3	9	18	ns
				Full	1.65 V to 1.95 V		1		20	
$t_{OFF}$	Turnoff time	$V_{COM} = V_+$ , $R_L = 50 \Omega$ ,	$C_L = 35 \text{ pF}$ , see <a href="#">Figure 17</a>	25°C	1.8 V		5	10	15.5	ns
				Full	1.65 V to 1.95 V		4		18.5	
$Q_C$	Charge injection	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1 \text{ nF}$ , see <a href="#">Figure 21</a>	25°C	1.8 V		2		pC	
$C_{NO(OFF)}$	NO OFF capacitance	$V_{NO} = V_+ \text{ or GND}$ , Switch OFF,	See <a href="#">Figure 16</a>	25°C	1.8 V		19.5		pF	
$C_{COM(OFF)}$	COM OFF capacitance	$V_{COM} = V_+ \text{ or GND}$ , Switch OFF,	See <a href="#">Figure 16</a>	25°C	1.8 V		18.5		pF	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

**Electrical Characteristics for 1.8-V Supply<sup>(1)</sup> (continued)**
 $V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT
$C_{NO(ON)}$	NO ON capacitance	$V_{NO} = V_+$ or GND, Switch ON,	See <a href="#">Figure 16</a>	25°C	1.8 V		36.5		pF
$C_{COM(ON)}$	COM ON capacitance	$V_{COM} = V_+$ or GND, Switch ON,	See <a href="#">Figure 16</a>	25°C	1.8 V		36.5		pF
$C_I$	Digital input capacitance	$V_I = V_+$ or GND,	See <a href="#">Figure 16</a>	25°C	1.8 V		2		pF
BW	Bandwidth	$R_L = 50\ \Omega$ , Switch ON,	See <a href="#">Figure 18</a>	25°C	1.8 V		150		MHz
$O_{ISO}$	OFF isolation	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch OFF, see <a href="#">Figure 19</a>	25°C	1.8 V		-62		dB
THD	Total harmonic distortion	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ see <a href="#">Figure 21</a>	25°C	1.8 V		0.055 %		
<b>Supply</b>									
$I_+$	Positive supply current	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	1.95 V	0.001	0.01	0.15	$\mu\text{A}$
				Full					

## 6.9 Typical Characteristics

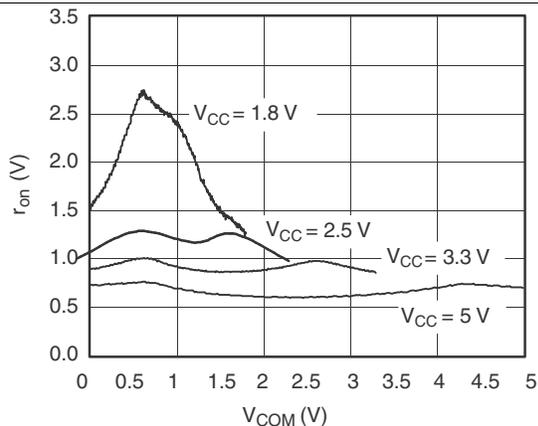


Figure 1.  $r_{on}$  vs  $V_{COM}$

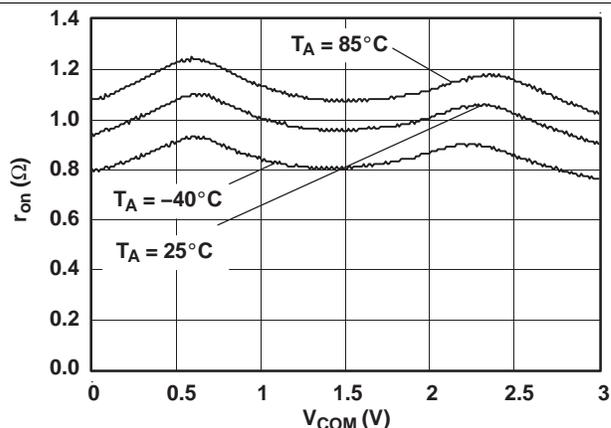


Figure 2.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 3$  V)

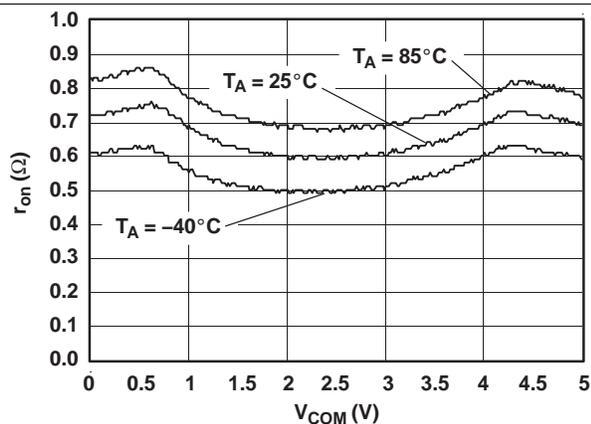


Figure 3.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 5$  V)

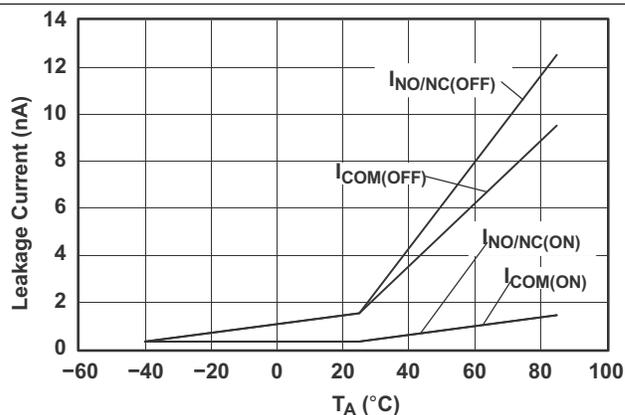


Figure 4. Leakage Current vs Temperature ( $V_+ = 5.5$  V)

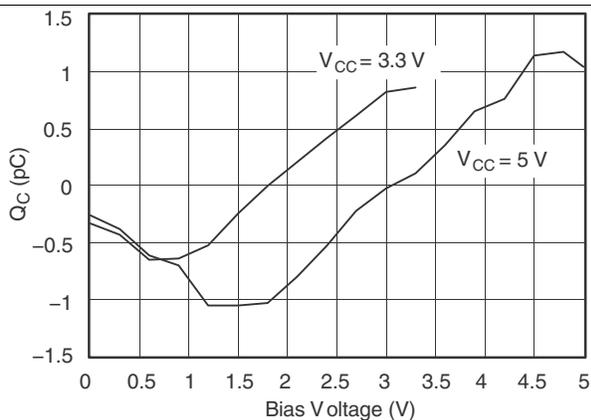


Figure 5. Charge Injection ( $Q_C$ ) vs  $V_{COM}$

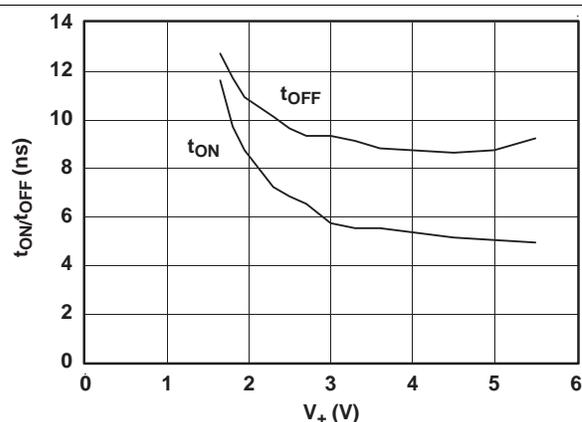
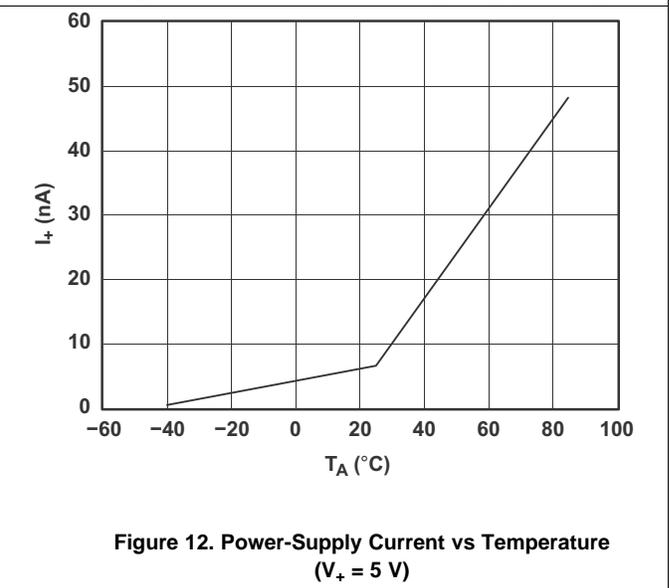
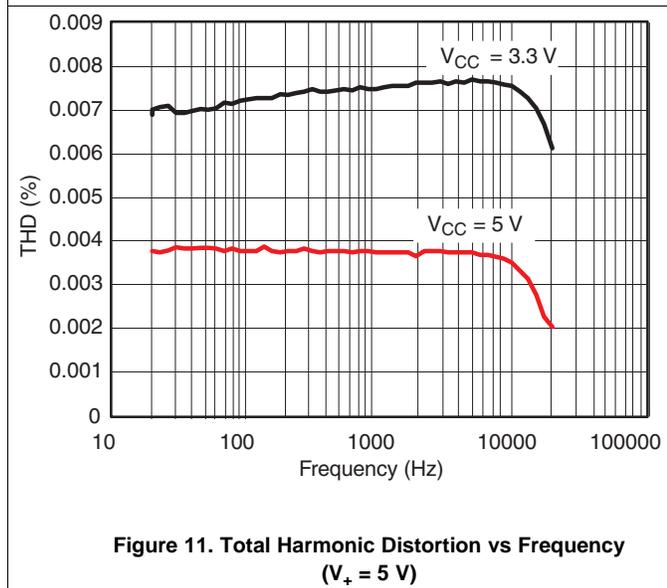
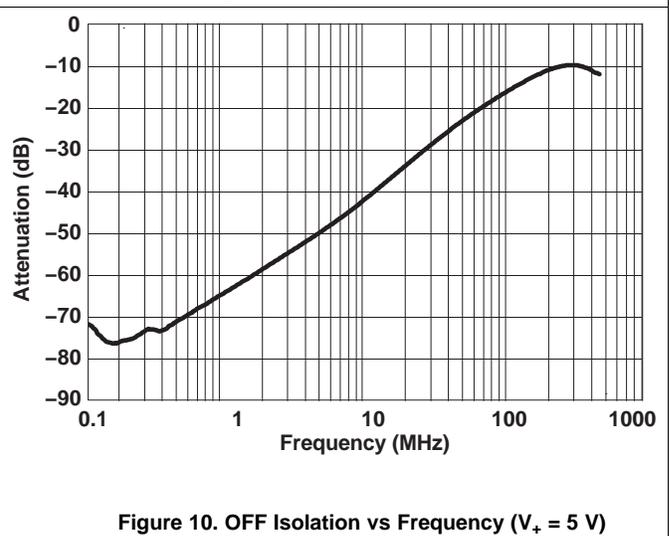
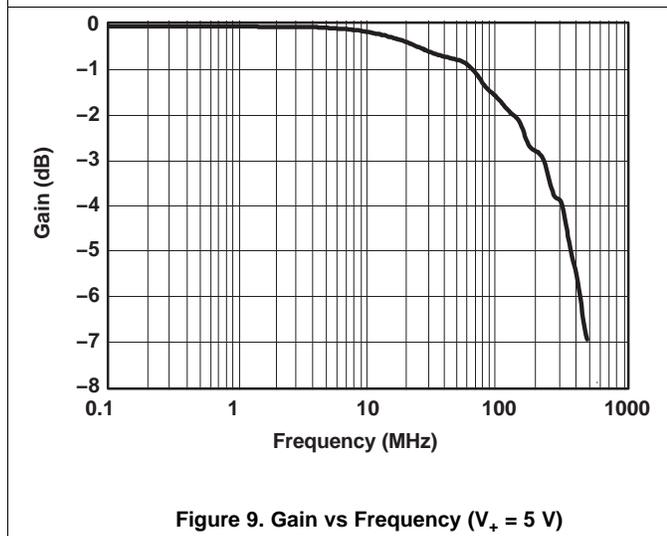
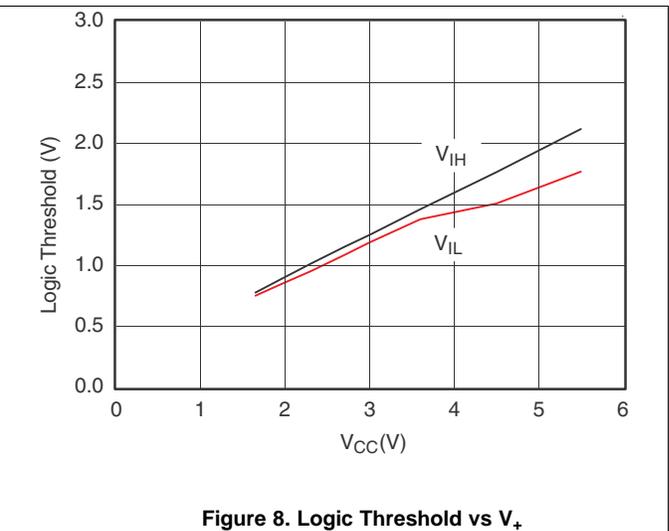
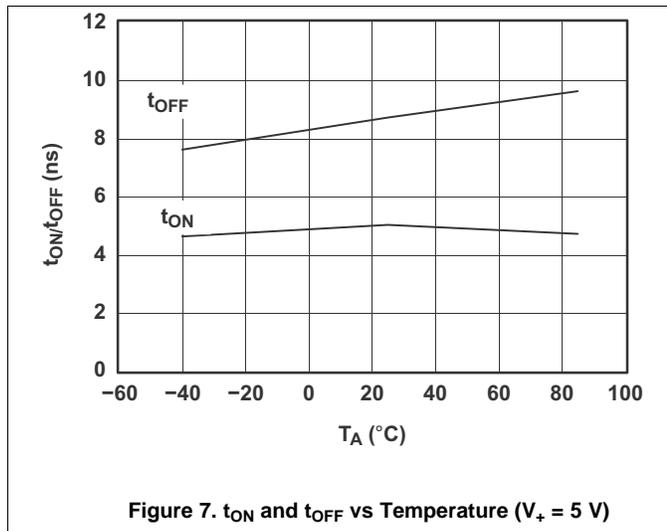


Figure 6.  $t_{ON}$  and  $t_{OFF}$  vs Supply Voltage

**Typical Characteristics (continued)**


## 7 Parameter Measurement Information

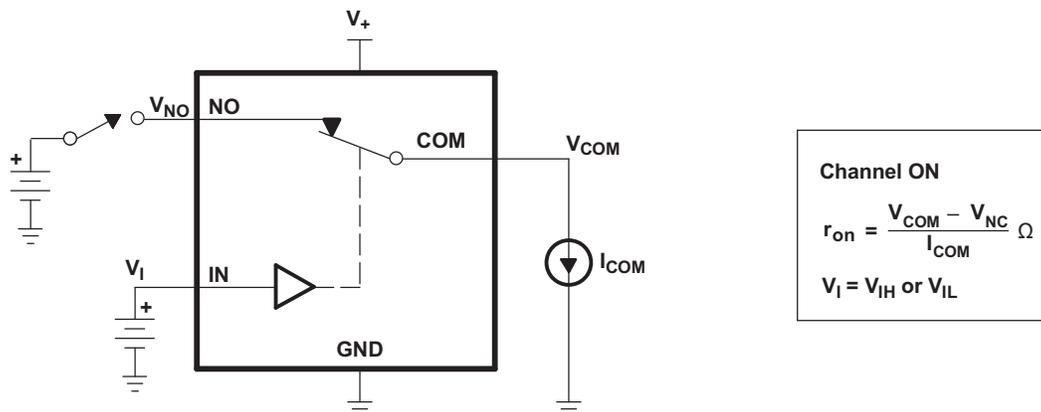


Figure 13. ON-State Resistance ( $r_{on}$ )

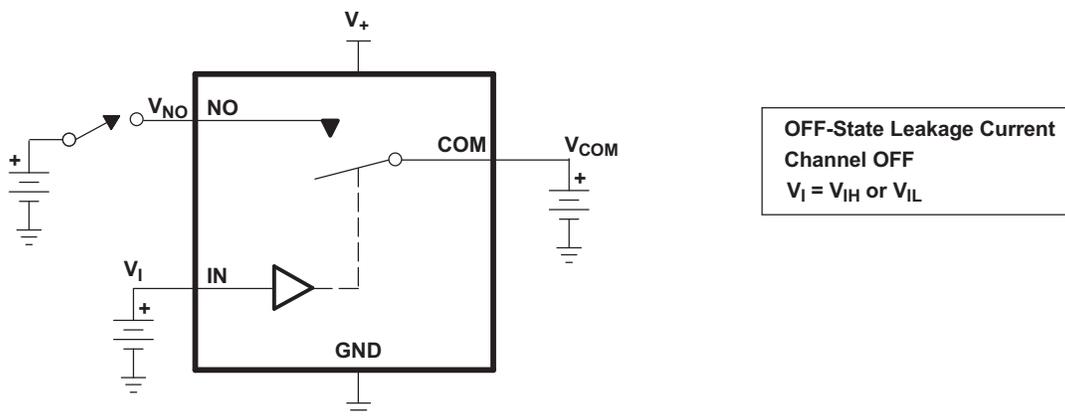


Figure 14. OFF-State Leakage Current ( $I_{COM(OFF)}$ ,  $I_{NO(OFF)}$ ,  $I_{COM(PWROFF)}$ ,  $I_{NO(PWROFF)}$ )

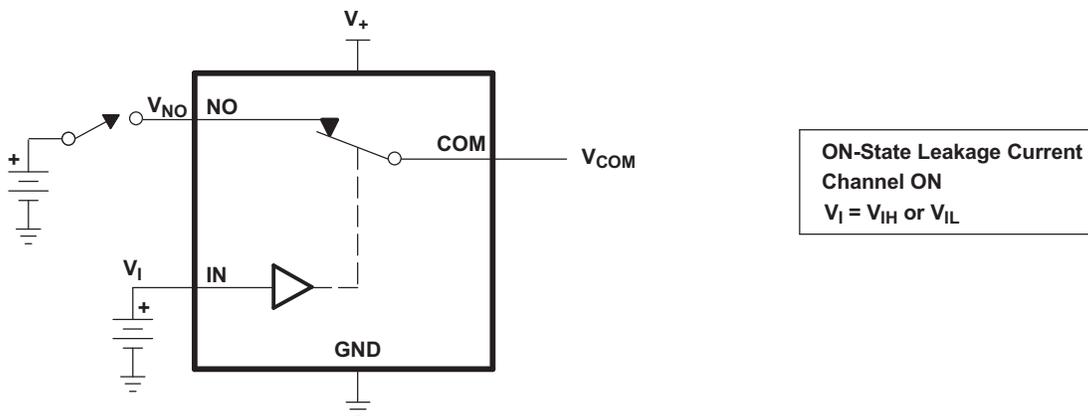


Figure 15. ON-State Leakage Current ( $I_{COM(ON)}$ ,  $I_{NO(ON)}$ )

Parameter Measurement Information (continued)

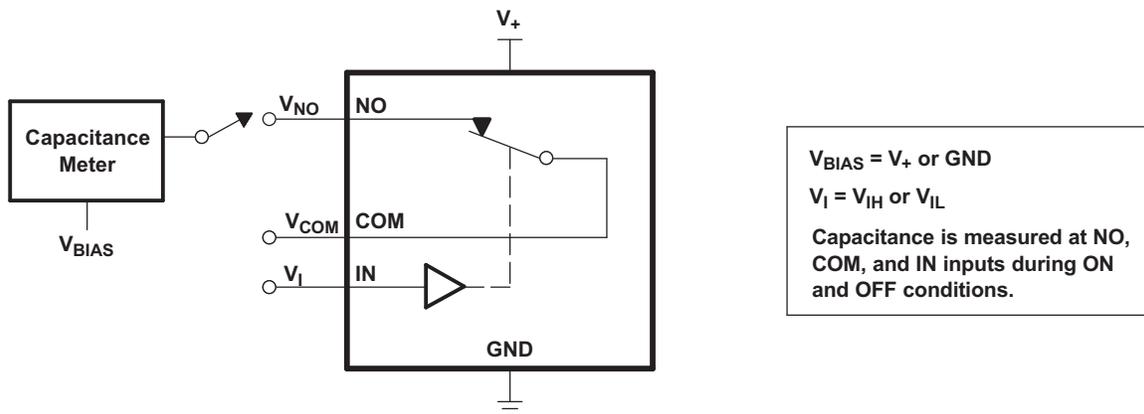
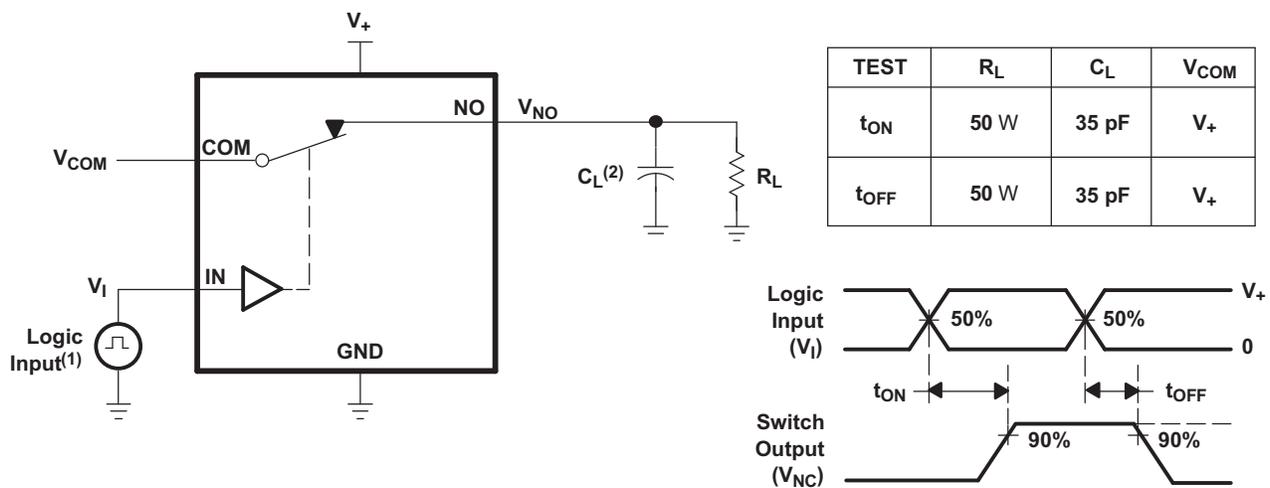


Figure 16. Capacitance ( $C_I$ ,  $C_{COM(OFF)}$ ,  $C_{COM(ON)}$ ,  $C_{NO(OFF)}$ ,  $C_{NO(ON)}$ )



- (1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> < 5 ns, t<sub>f</sub> < 5 ns.
- (2) C<sub>L</sub> includes probe and jig capacitance.

Figure 17. Turnon (t<sub>ON</sub>) and Turnoff Time (t<sub>OFF</sub>)

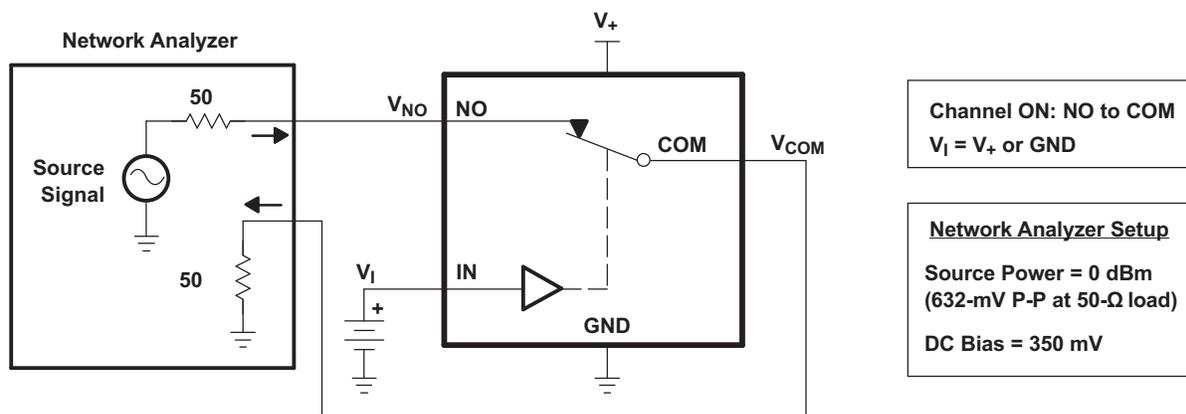


Figure 18. Bandwidth (BW)

Parameter Measurement Information (continued)

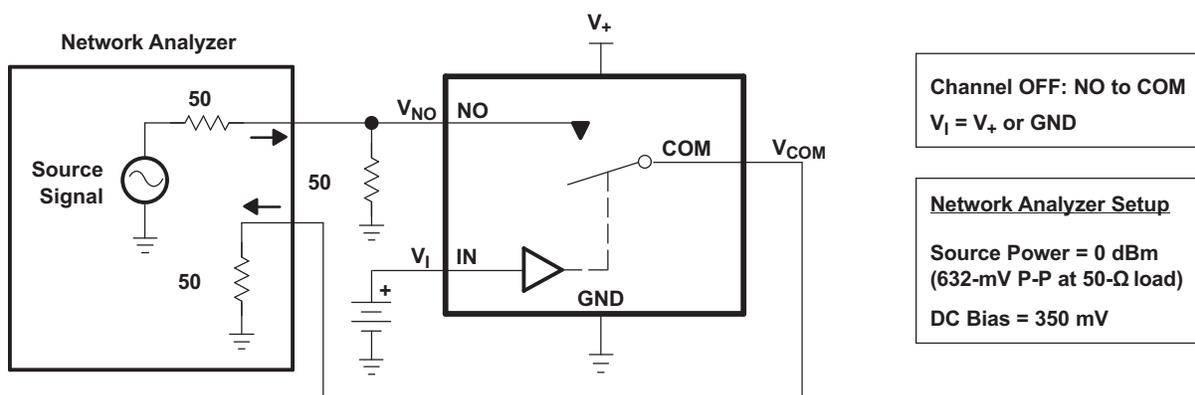
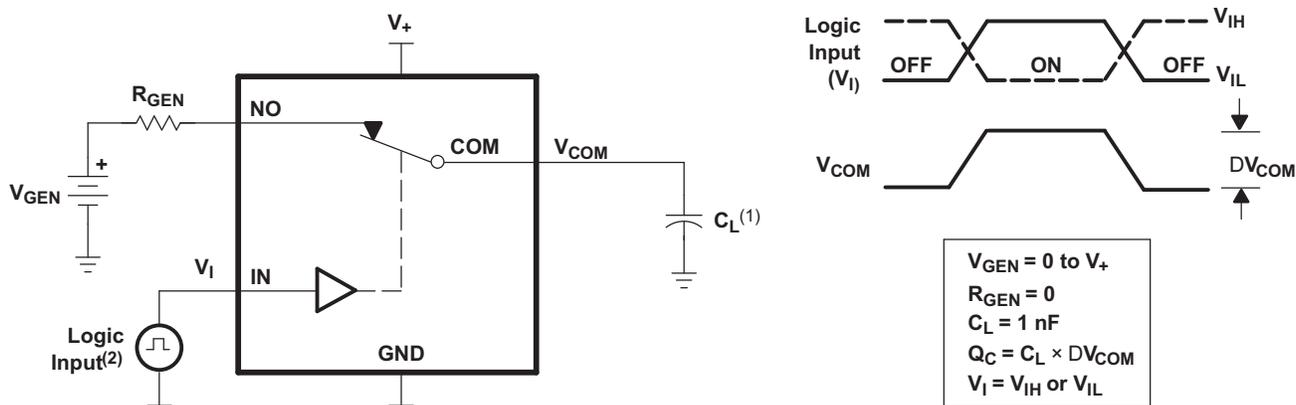
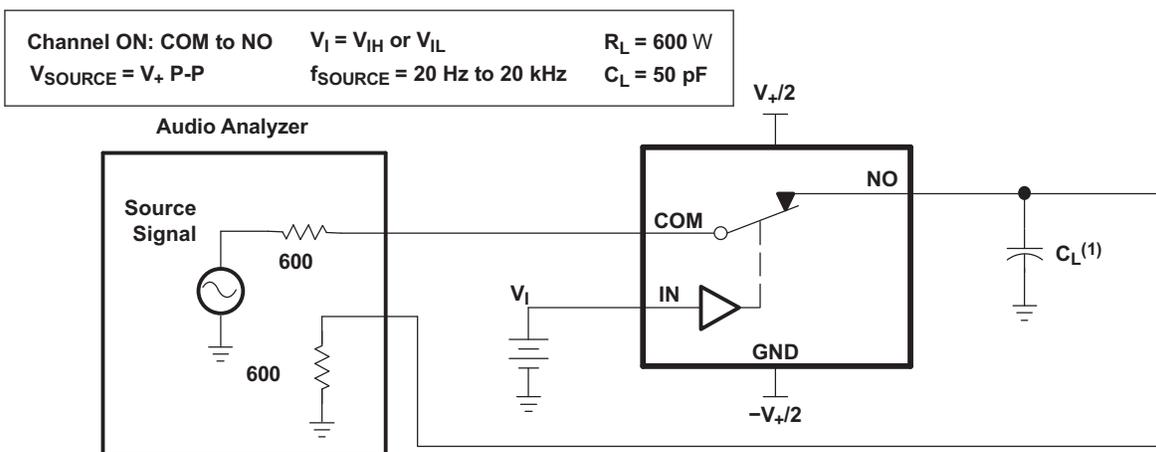


Figure 19. OFF Isolation ( $O_{ISO}$ )



- (1)  $C_L$  includes probe and jig capacitance.
- (2) All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.

Figure 20. Charge Injection ( $Q_C$ )



- (1)  $C_L$  includes probe and jig capacitance.

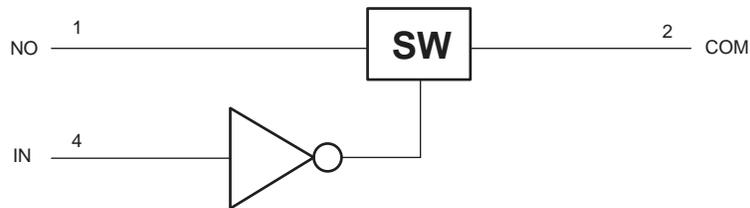
Figure 21. Total Harmonic Distortion (THD)

## 8 Detailed Description

### 8.1 Overview

The TS5A3166 is a single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

### 8.2 Functional Block Diagram



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### 8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A3166 make this switch an excellent choice for analog signals that require minimal distortion. In addition, the low THD allows audio signals to be preserved more clearly as they pass through the device.

The 1.65-V to 5.5-V operation allows compatibility with more logic levels, and the bidirectional I/Os can pass analog signals from 0 V to  $V_+$  with low distortion.

### 8.4 Device Functional Modes

**Table 1. Function Table**

IN	NO TO COM, COM TO NO
L	OFF
H	ON

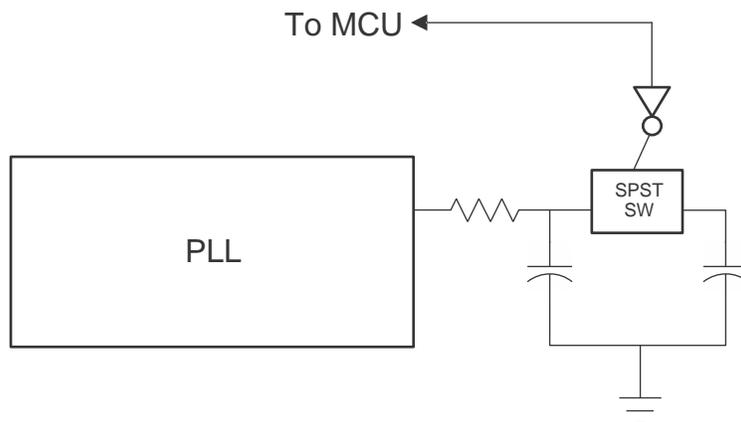
## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

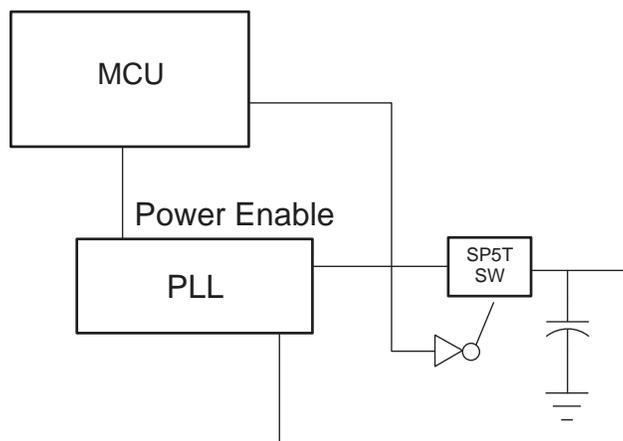
### 9.1 Application Information

SPST analog switch is a basic component that could be used in any electrical system design. [Figure 22](#) and [Figure 23](#) are some basic applications that utilize the TS5A3166.



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**Figure 22. Improved Lock Time Circuit Simplified Block Diagram**



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**Figure 23. PLL Improved Power Consumption Simplified Block Diagram**

## 9.2 Typical Application

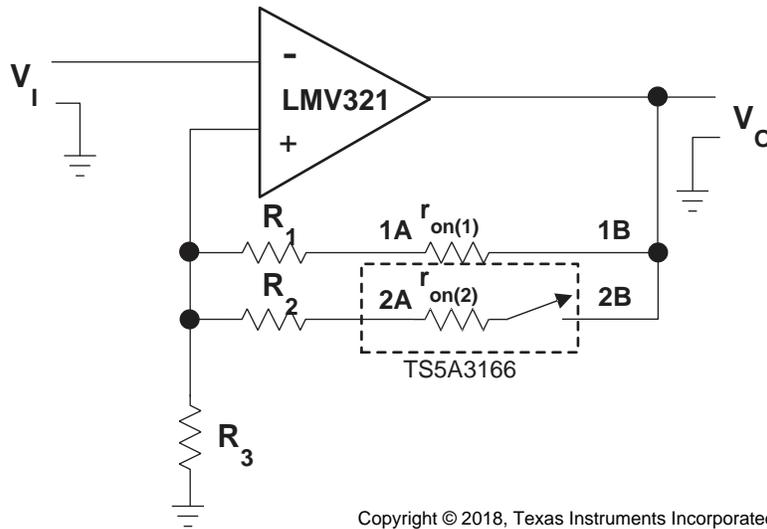


Figure 24. Gain-Control Circuit for Operational Amplifier

### 9.2.1 Design Requirements

By choosing values of R1 and R2, such that  $R_x \gg r_{on(x)}$ ,  $r_{on}$  of TS5A3166 can be ignored. The gain of operational amplifier can be calculated as follow:

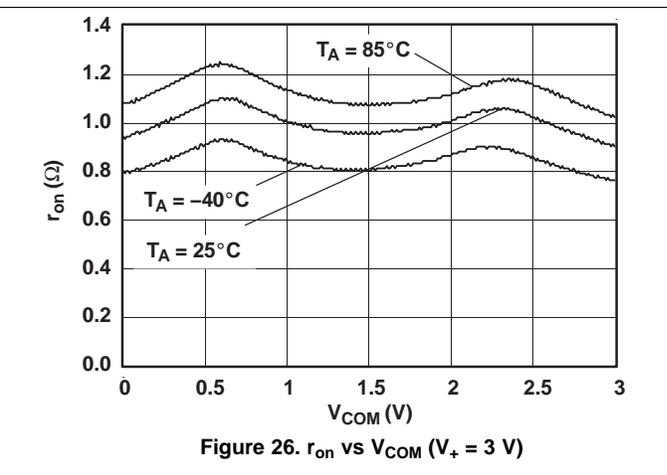
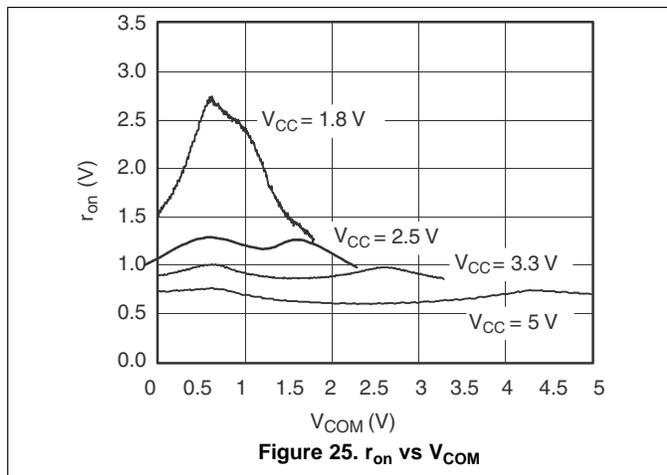
$$V_o / V_i = 1 + R_{||} / R_3 \tag{1}$$

$$R_{||} = (R_1 + r_{on(1)}) || (R_2 + r_{on(2)}) \tag{2}$$

### 9.2.2 Detailed Design Procedure

Place a switch in series with the input of the operational amplifier. Since the operational amplifier input impedance is very large, a switch on  $r_{on(1)}$  is irrelevant.

### 9.2.3 Application Curves



Typical Application (continued)

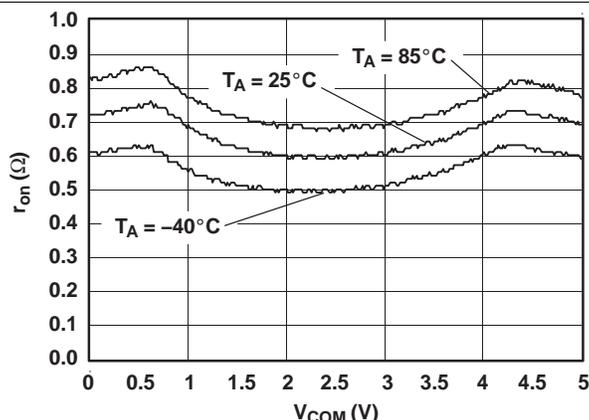


Figure 27. r<sub>on</sub> vs V<sub>COM</sub> (V<sub>+</sub> = 5 V)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#).

Each V<sub>CC</sub> terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If there are multiple pins labeled V<sub>CC</sub>, then a 0.01-μF or 0.022-μF capacitor is recommended for each V<sub>CC</sub> because the V<sub>CC</sub> pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V<sub>CC</sub> and V<sub>DD</sub>, a 0.1-μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. [Figure 28](#) shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

### 11.2 Layout Example

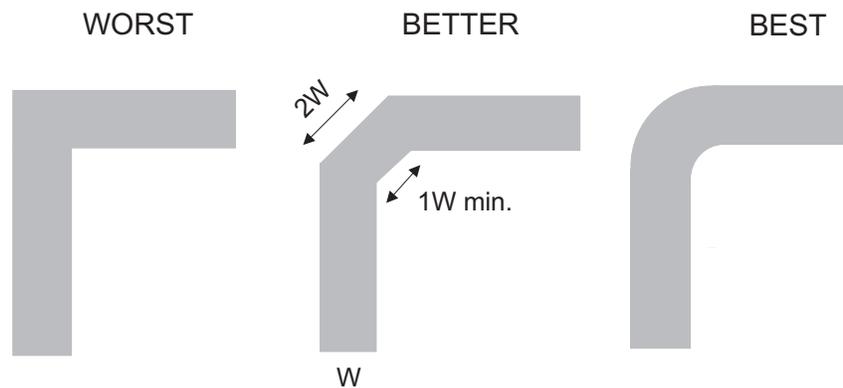


Figure 28. Trace Example

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Device Nomenclature

**Table 2. Parameter Description**

SYMBOL	DESCRIPTION
$V_{COM}$	Voltage at COM
$V_{NO}$	Voltage at NO
$r_{on}$	Resistance between COM and NO ports when the channel is ON
$r_{peak}$	Peak ON-state resistance over a specified voltage range
$r_{on(Flat)}$	Difference between the maximum and minimum value of $r_{on}$ in a channel over the specified range of conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
$I_{NO(PWROFF)}$	Leakage current measured at the NO port during the power-down condition, $V_+ = 0$
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the OFF state under worst-case input and output conditions
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, $V_+ = 0$
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the ON state and the output (NO) open
$V_{IH}$	Minimum input voltage for logic high for the control input (IN)
$V_{IL}$	Maximum input voltage for logic low for the control input (IN)
$V_I$	Voltage at the control input (IN)
$I_{IH}, I_{IL}$	Leakage current measured at the control input (IN)
$t_{ON}$	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
$t_{OFF}$	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
$Q_C$	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$ . $C_L$ is the load capacitance, and $\Delta V_{COM}$ is the change in analog output voltage.
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
$C_I$	Capacitance of control input (IN)
$O_{ISO}$	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NO to COM) in the OFF state.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
$I_+$	Static power-supply current with the control (IN) pin at $V_+$ or GND

## 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

## 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TS5A3166DBVR</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(JASF, JASR)
TS5A3166DBVR.B	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(JASF, JASR)
<a href="#">TS5A3166DBVRG4</a>	Obsolete	Production	SOT-23 (DBV)   5	-	-	Call TI	Call TI	-40 to 85	JASF
<a href="#">TS5A3166DCKR</a>	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JF5, JFF, JFR)
TS5A3166DCKR.B	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JF5, JFF, JFR)
<a href="#">TS5A3166YZPR</a>	Active	Production	DSBGA (YZP)   5	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JFN
TS5A3166YZPR.B	Active	Production	DSBGA (YZP)   5	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JFN

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

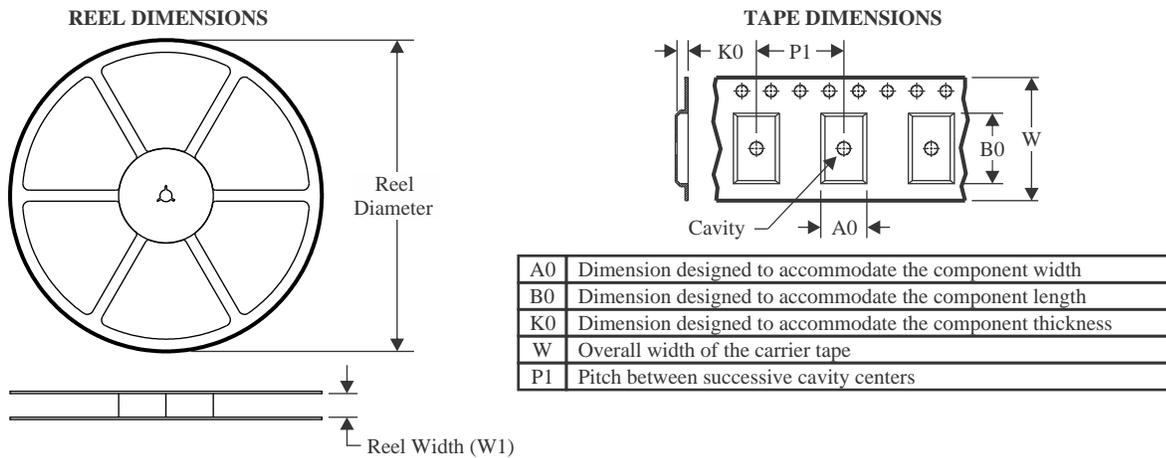
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TS5A3166 :**

- Automotive : [TS5A3166-Q1](#)

## NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3166DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TS5A3166DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3166DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3166DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TS5A3166DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
TS5A3166YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3166DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TS5A3166DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TS5A3166DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TS5A3166DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TS5A3166DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TS5A3166YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

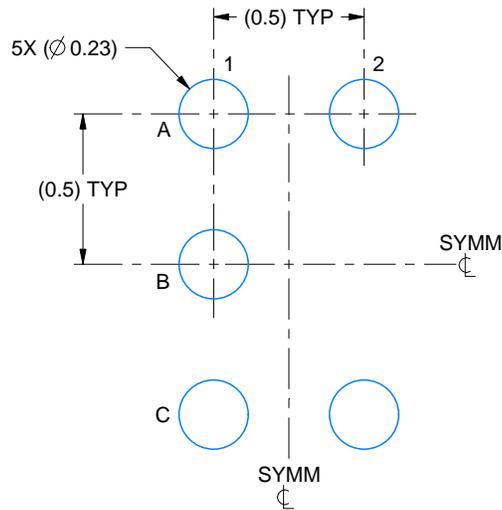


# EXAMPLE BOARD LAYOUT

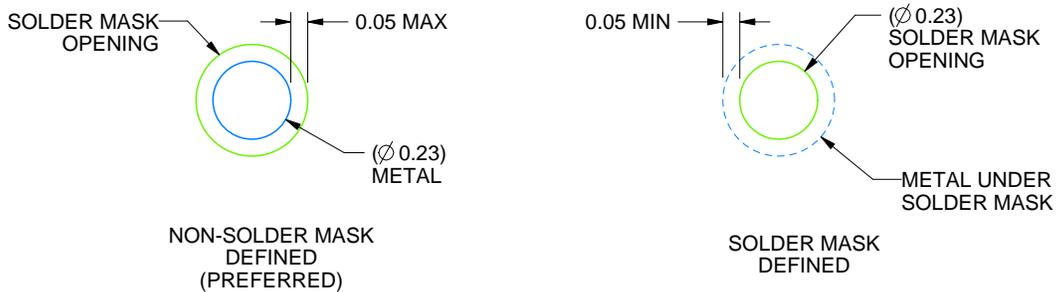
YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

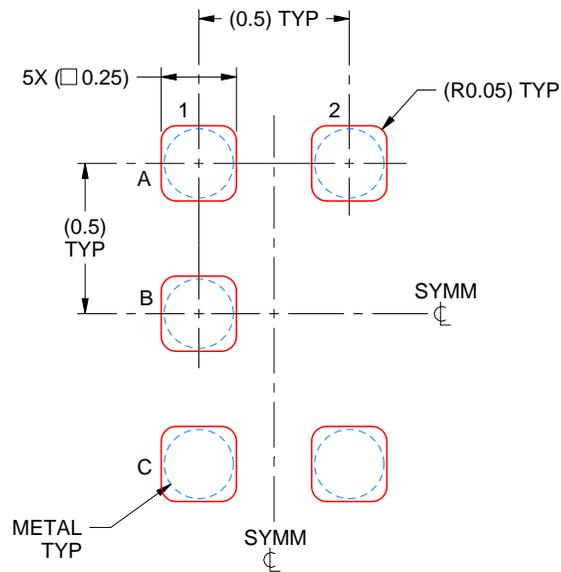
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

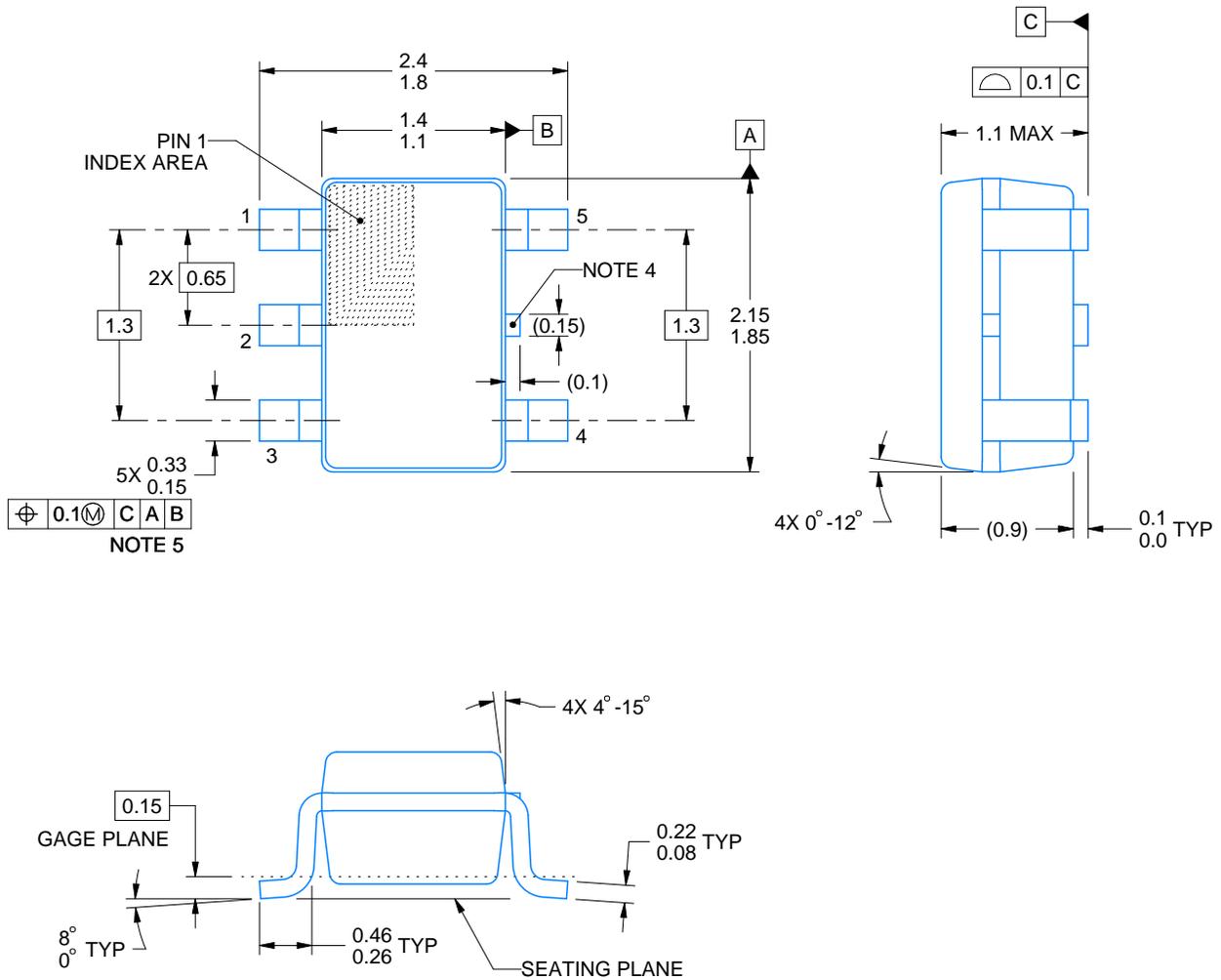
# DCK0005A



## PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

### NOTES:

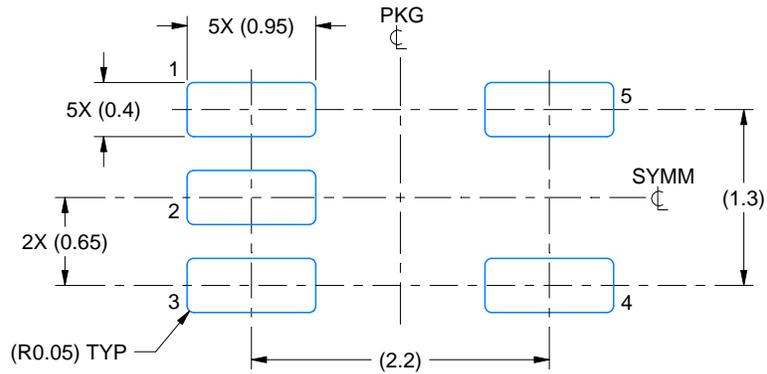
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

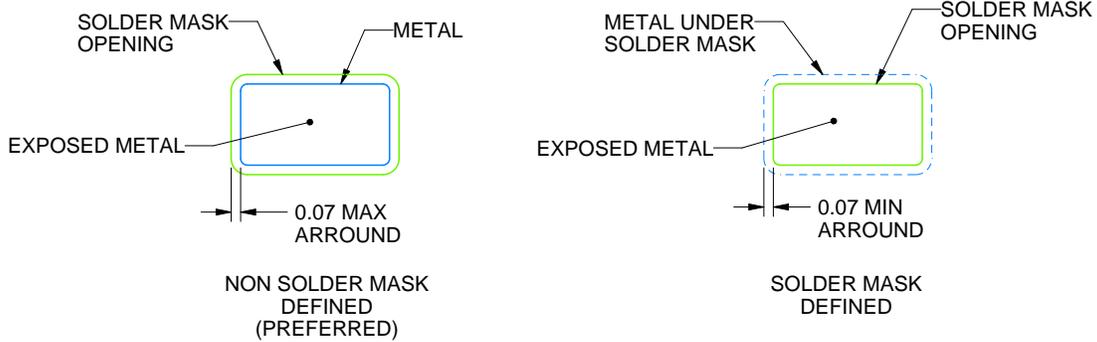
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

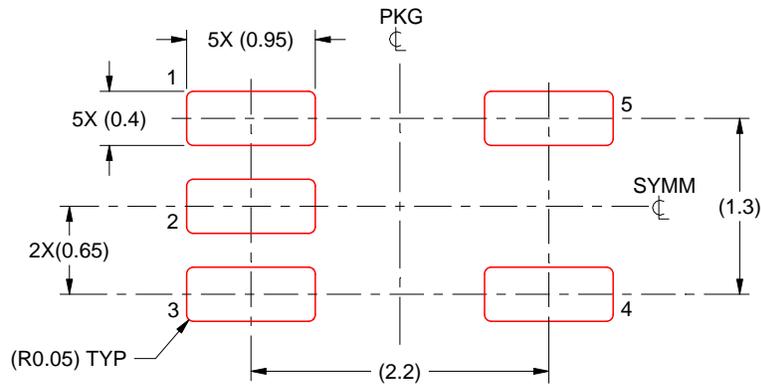
- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

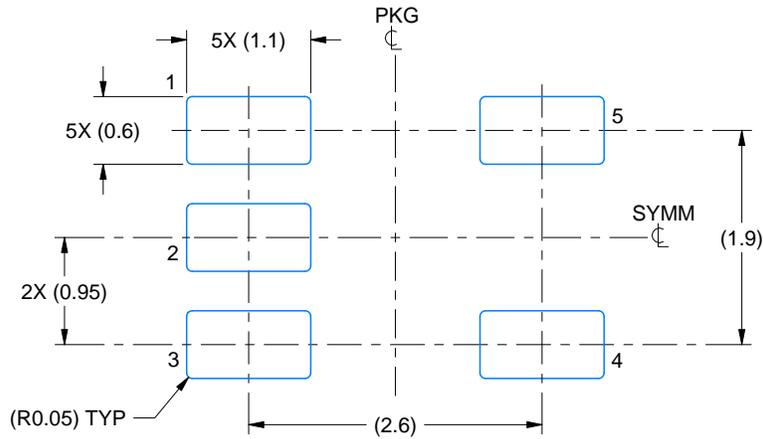


# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

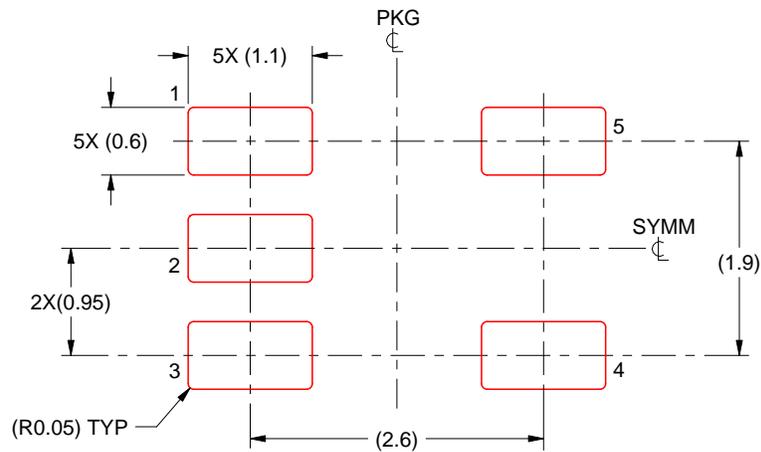
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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