TEXAS INSTRUMENTS

TSB42AC3

Data Manual

January 2006

CS Peripheral

SLLS593A

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1 Overview

1.1 TSB42AC3 Description

The TSB42AC3 is a 1394-1995 general purpose link layer ideal for a wide-range of applications, including motion control, motor control, video, and process control. The TSB42AC3 provides a high-performance interface with the capability of transferring data between the 32-bit host controller and the 1394 PHY-link interface. The 1394 PHY-link interface provides the connection to the 1394 physical layer device (PHY) and is supported by the link-layer controller (LLC). The LLC provides the control for transmitting and receiving 1394 packet data between the FIFO and PHY-link interface at rates of 50 (backplane only), 100, 200, and 400 Mbit/s.

The TSB42AC3 has a 32-bit, 50-MHz host interface, which makes connection to most 32-bit hosts fairly easy. The LLC also provides the capability to receive status from the PHY and to access the PHY control and status registers by the application software.

An internal 10K-byte memory is provided that can be configured as multiple variable-size FIFOs and eliminates the need for external FIFOs. Separate FIFOs can be user configured to support asynchronous transmit, isochronous transmit, and general 1394 receive transfer operations. These functions are accomplished by appropriately sizing the asynchronous transmit FIFO (ATF) and isochronous transmit FIFO (ITF). Once the ATF and ITF size are programmed, the remaining memory space is assigned to the general receive FIFO (GRF).

The TSB42AC3 has a separate ACK FIFO register that is capable of retaining up to six acknowledges returned by external nodes in response to the asynchronous packets transmitted from the TSB42AC3. This allows host software to load multiple asynchronous packets in the ATF, then return at a later time to retrieve and process the acknowledges returned from the receiving destination nodes.

New status bits were added to the programmable output status pins. The start/end of packet bit (*cd* bit) and the packet complete (*paccom* bit) may now be brought out to a pin for control of external hardware.

1.2 TSB42AC3 Features

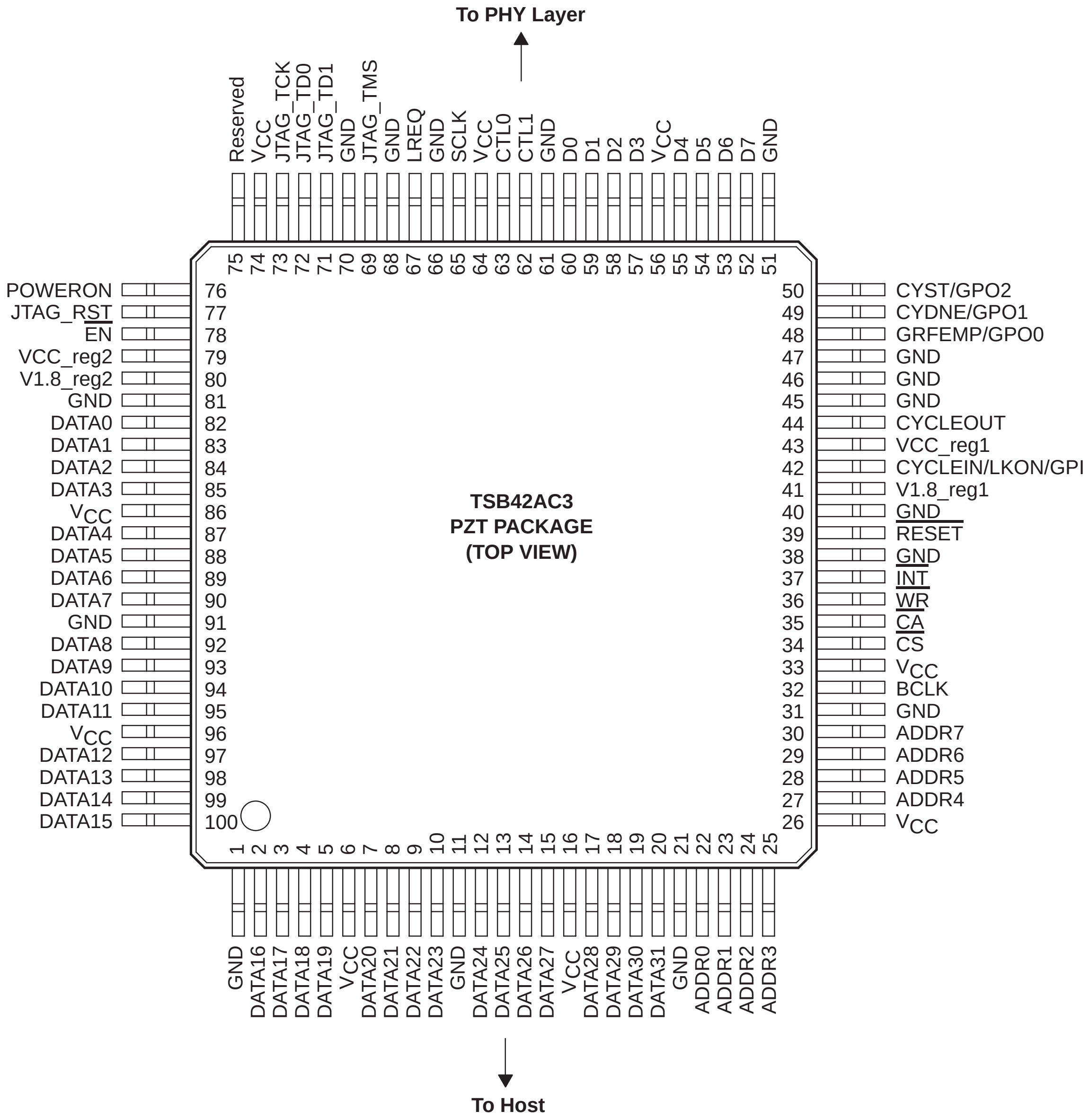
- 50-MHz Host Interface Frequency Allows Direct Connection to Host With Bus Speeds up to 50 MHz
- Programmable 10K Byte Total for Asynchronous, Isochronous, and General Receive FIFO
- Separate ACK FIFO Register Decreases ACK-tracking Burden on the Host
- Additional Programmable Status Output to Pins, Including *cd* and *paccom* Bits to Aid External DMA
- Supports 1394 Transfer Rates of 100, 200, and 400 Mbit/s in Cable Environment
- Supports 1394 Transfer Rates of 50 and 100 Mbit/s in Backplane Environment
- Generic 32-Bit Host Bus Interface
- Completely Software Compatible With the TSB12LV01B
- IEEE 1149.1 JTAG Interface to Support Board Level Scan Testing
- Operates from a 3.3-V Power Supply
- Support Provisions of IEEE 1394−1995 (1394) Standard for High-Performance Serial Bus
- High Performance 100-Pin TQFP Package

1.3 Ordering Information

AVAILABLE OPTIONS

ORDERING NUMBER	VOLTAGE	T_A	PACKAGE
TSB42AC3PZT	3.3 V	0°C to 70°C	100 PQFP
TSB42AC3IPZT	3.3 V	−40°C to 85°C	100 PQFP

1.4 Terminal Assignments



1.5 Terminal Functions

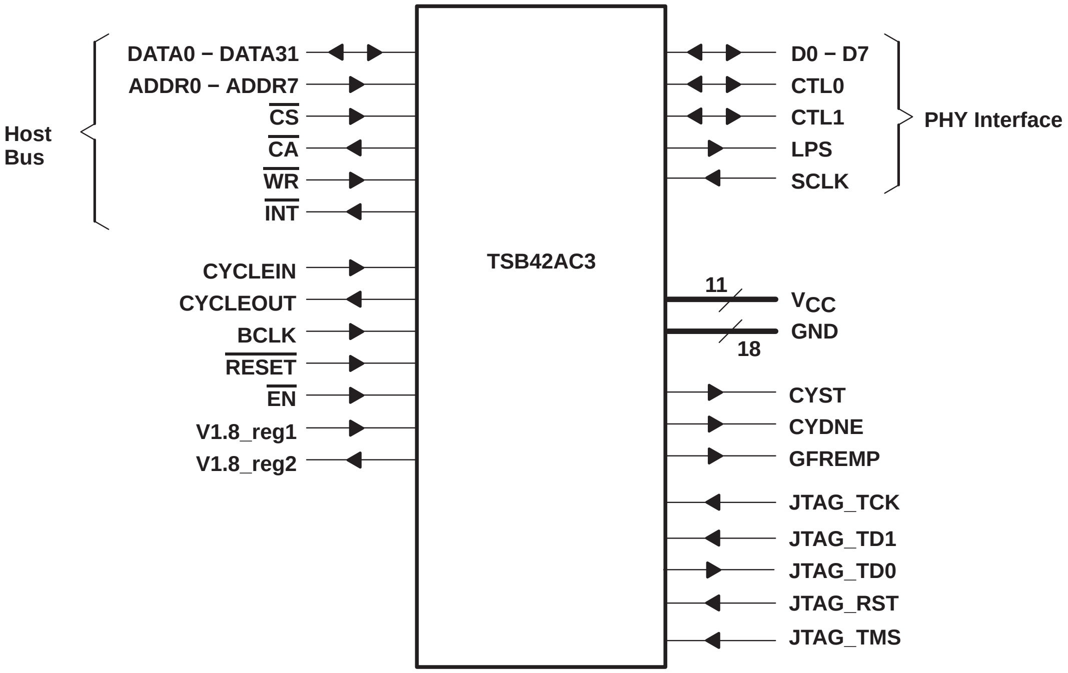


Figure 1−1. TSB42AC3 Terminal Functions

Table 1−1. Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
HOST BUS INTERFACE			
ADDR0−ADDR7	22−25, 27−30	I	Host address bus ADDR0 is the most significant bit (MSB). ADDR6 and 7 should be grounded. (Note: FIFO space and configuration registers are quadlet-aligned)
$\overline{\text{CA}}$	35	O	Cycle acknowledge (active low). $\overline{\text{CA}}$ is a TSB42AC3 control signal to the host bus. When asserted (low), access to the configuration registers or FIFO is complete.
$\overline{\text{CS}}$	34	I	Cycle start (active low). $\overline{\text{CS}}$ is a host bus control signal to indicate the beginning of an access to the TSB42AC3 configuration registers or FIFO space.
DATA0−DATA31	82−85, 87−90, 92−95, 97−100, 2−5, 7−10, 12−15, 17−20	I/O	Host data bus DATA0 is the most significant bit (MSB). Byte0 (DATA0−DATA7) is the most significant byte.
$\overline{\text{INT}}$	37	O	Interrupt (active low). When $\overline{\text{INT}}$ is asserted (low), the TSB42AC3 notifies the host bus that an interrupt has occurred.
$\overline{\text{WR}}$	36	I	Read/write enable. When $\overline{\text{CS}}$ is asserted (low) and $\overline{\text{WR}}$ is deasserted (high), a read from the TSB42AC3 is requested by the host bus controller. To request a write access, $\overline{\text{WR}}$ must be asserted (low).
BCLK	32	I	Host bus clock. BCLK is the clock input supplied by the host to the TSB42AC3. BCLK is asynchronous to the PHY SCLK and supports a maximum frequency of 50 MHz.
PHY INTERFACE			
CTL0, CTL1	63, 62	I/O	PHY-link interface control bus. CTL0 and CTL1 indicate the four operations that can occur on this interface (see Section 7 of this document or Annex J of the IEEE 1394−1995 standard for more information about the four operations).
D0−D7	60−57, 55−52	I/O	PHY-link interface data bus. Data is expected on D0 – D1 for 50/100 Mbits/s packets, D0 – D3 for 200 Mbits/s, and D0 – D7 for 400 Mbits/s.

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
LREQ	67	O	Link request to PHY. LREQ is a TSB42AC3 output that makes bus requests and register access requests to the PHY.
POWERON	76	O	Link power status to PHY interface. When active, LPS has a clock output with 1/32 of the BCLK frequency and indicates to the PHY interface that the link is powered up. This terminal can be connected to the LPS terminal on the TI PHY devices to provide an indication of the Link power condition.
SCLK	65	I	System clock. SCLK is a 49.152-MHz clock from the PHY at S100, S200, and S400. SCLK is a 24.576-MHz clock from the backplane PHY at S50.
JTAG INTERFACE			
JTAG_TCK	73	I	Test clock. TCLK provides the clock input for the TSB42AC3's JTAG controller
JTAG_TMS	69	I	Test mode select. TMS controls the state of the TSB42AC3's JTAG controller
JTAG_TDI	71	I	Test data in. TIN is the data input to the TSB42AC3's JTAG controller
JTAG_TDO	72	O	Test data out. TOUT is the data output from the TSB42AC3's JTAG controller
JTAG_RST	77	I	Test reset. This is the reset input to the TSB1201C's JTAG controller.
MISCELLANEOUS SIGNALS			
CYCLEIN/LKON/GPI	42	I	Cycle in/link on/general purpose program input.
CYCLEOUT	44	O	Cycle out. CYCLEOUT is the TSB42AC3 version of the cycle clock. It is based on the timer controls and received cycle-start messages.
GRFEMP/GPO0	48	O	GRF empty bit / general-purpose output 0. The power up default function for this terminal is GRFEMP. GRFEMP is asserted (high) for as long as the GRFEMP bit (bit 0 @ 3Ch) is set. After power up, this terminal may be programmed as a general-purpose output.
CYDNE/GPO1	49	O	CYDNE status bit / general purpose output 1. The power up default function for this terminal is CYDNE. CYDNE indicates the value of the cycle done (CyDne) bit of the interrupt register. It remains asserted (high) for as long as the interrupt bit is assigned. After power up, this terminal may be programmed as a general-purpose output.
CYST/GPO2	50	O	CYST status bit / general-purpose output 2. The power up default function for this terminal is CYST. CYST indicates the value of the cycle start (CySt) bit of the interrupt register. It remains asserted (high) for as long as the interrupt bit is assigned. After power up, this terminal may be programmed as a general-purpose output.
$\overline{\text{RESET}}$	39	I	System reset (active low). $\overline{\text{RESET}}$ is the asynchronous reset to the TSB42AC3. It must be held low for a minimum of 2 BCLK cycles.
$\overline{\text{EN}}$	78	Supply	Enable on-chip regulator. This active low pin enables the 1.8-V on-chip regulator and should be tied to GND.
V1.8_reg1, V1.8_reg2	41, 80	O	1.8-V regulator output. These pins are the output of the on-chip 1.8-V voltage regulator. In normal conditions these should be decoupled to the GND through a 0.1-µF capacitor.
VCC, VCC_reg1, VCC_reg2	6, 16, 26, 33, 43, 56, 64, 74, 79, 86, 96	Supply	3.3-V supply voltage
GND	1, 11, 21, 31, 38, 40, 45, 46, 47, 51, 61, 66, 68, 70, 81, 91	Supply	Ground reference
Reserved	75		Reserved pin. Must be tied to GND.

2 Architecture

2.1 Function Block Diagram

The functional block diagram of the TSB42AC3 is shown in Figure 2−1.

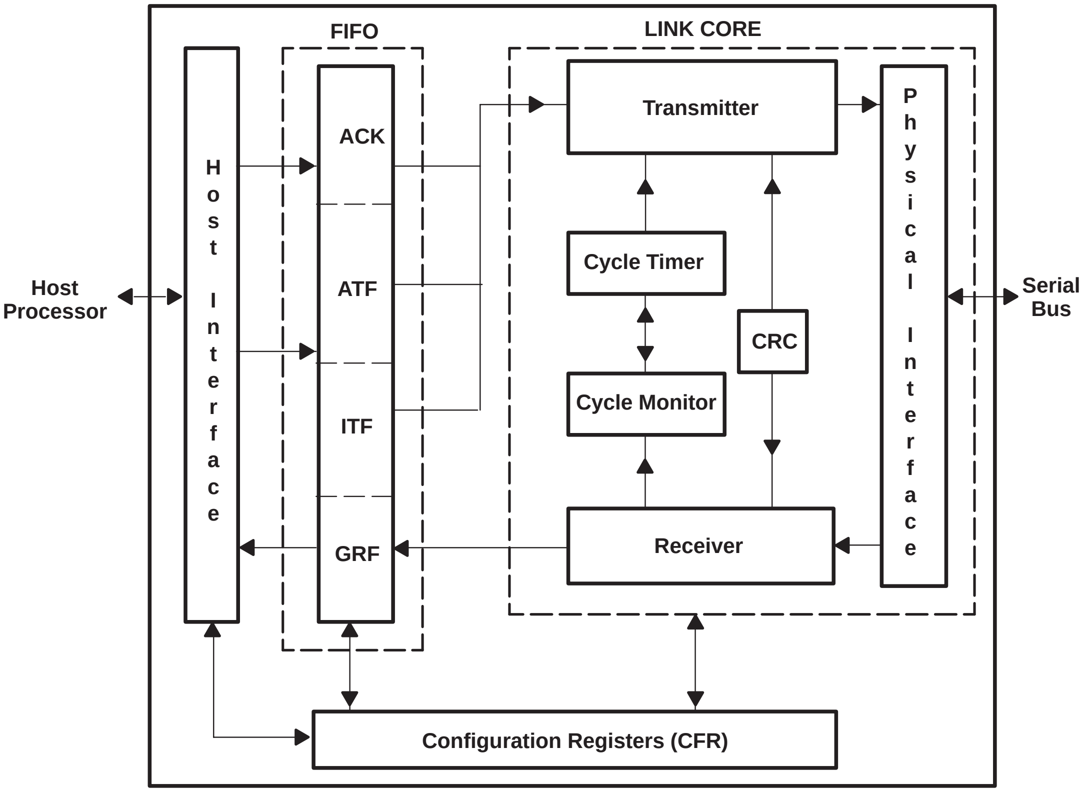


Figure 2−1. Function Block Diagram

2.1.1 *Physical Interface*

The physical (PHY) interface provides PHY-level services to the transmitter and receiver. This includes gaining access to the serial bus, sending packets, receiving packets, sending and receiving acknowledge packets, and reading and writing PHY registers.

The PHY interface module also interfaces to the PHY chip and conforms to the PHY-link interface specification described in Annex J of the IEEE 1394−1995 standard (see Section 7 of this document for more information).

2.1.2 *Transmitter*

The transmitter retrieves data from either the ATF or the ITF and creates correctly formatted serial-bus packets to be transmitted through the PHY interface. When data is present at the ATF interface to the transmitter, the TSB42AC3 PHY interface arbitrates for the serial bus immediately. When the data is present at the ITF interface to the transmitter, the TSB42AC3 arbitrates for the serial bus during the next isochronous cycle. The transmitter autonomously sends the cycle-start packets when the chip is a cycle master. The PHY interface provides PHY-level services to the transmitter and receiver. This included gaining access to the serial bus, sending packets, receiving packets, and sending and receiving acknowledge packets.

2.1.3 Receiver

The receiver takes incoming data from the PHY interface and determines if the incoming data is addressed to this node. If the incoming packet is addressed to this node, the CRC of the packet is checked. If the header CRC is good, the header is confirmed in the GRF. For block and isochronous transmit, the remainder of the packet is confirmed one quadlet at a time. The receiver places a status quadlet in the GRF after the last quadlet of the packet is confirmed in the GRF. The status quadlet contains the error code for the packet. The error code is the acknowledge code that is sent for that packet. For broadcast packets that do not need acknowledge packets, the error code is the acknowledge code that would have been sent. This acknowledge code tells the transition layer whether or not the data CRC is good or bad. When the header CRC is bad, the header is flushed and the rest of the packet is ignored. Bad packets are automatically flushed by the receiver.

When a cycle-start message is received, it is detected and the cycle-start message data is sent to the cycle timer. The cycle-start messages can be placed in the GRF like other quadlet packets.

2.1.4 Transmit and Receive FIFO Memories

The TSB42AC3 contains two transmit FIFOs (ATF and ITF) and one receive FIFO (GRF). Each of these FIFOs is one quadlet wide and their length is software-selectable. These software-selectable FIFOs allow customization of the size of each FIFO for individual applications. The sum of all FIFOs cannot be larger than 2560 quadlets. The transmit FIFO is write only from the host bus interface and the receiver FIFO is read only from the host bus interface. FIFO sizes must not be changed on the fly. All transition must be ignored and FIFOs cleared before changing the FIFO sizes.

An example of how to use software-adjustable FIFO follows.

In applications where isochronous packets are large and asynchronous packets are small, the user can get the ITF to a large size (2000 quadlets each) and set the ATF to a smaller size (300 quadlets). This means 200 quadlets are allocated to the GRF. Notice that the sum of all FIFOs is equal to 2560 quadlets. Only the ATF size and the ITF size can be programmed, the remaining space is assigned to the GRF.

2.1.5 Cycle Timer

The cycle timer is used by nodes that support isochronous data transfer. The cycle timer is a 32-bit cycle-timer register. Each node with isochronous data-transfer capability has a cycle-timer register as defined in the IEEE1394−1995 standard. In the TSB42AC3, the cycle-timer register is implemented in the cycle timer and is located in the IEEE−1212 initial register space at location 200h and can also be accessed through the local bus at address 14h.

The cycle timer contains the cycle-timer register. The cycle-timer register consists of three fields: cycle offset, cycle count, and seconds count. The low-order 12 bits of the timer are a modulo 3072 counter, which increments once every 24.576-MHz clock period (or 40.69 ns). The next 13 higher-order bits are a count of 8,000-Hz (or 125 µs) cycles and the highest 7 bits count seconds.

The cycle timer has two possible sources. First, if the cycle source (CySrc) bit in the configuration register is set, then the CYCLEIN input pin causes the cycle count field to increment for each positive transition of the CYCLEIN input (8 kHz) and the cycle offset resets to all zeros. CYCLEIN should only be the source when the node is cycle master. When the cycle-count field increments, CYCLEOUT is generated. The timer can also be disabled using the cycle-timer-enable bit in the control register.

The second cycle-source option is when the CySrc bit is cleared. In this state, the cycle-offset field of the cycle-timer register is incremented by the internal 24.576-MHz clock. The cycle timer is updated by the reception of the cycle-start packet for the noncycle master nodes. Each time the cycle-offset field rolls over, the cycle-count field is incremented and the CYCLEOUT signal is generated. The cycle-offset field in the isochronous cycle of 125 µs. The cycle-start bit is set when the cycle-start packet is sent from the cycle-master node or received by a noncycle master node.

2.1.6 Cycle Monitor

The cycle monitor is only used by nodes that support isochronous data transfer. The cycle monitor observes chip activity and handles scheduling of isochronous activity. When a cycle-start message is received or sent, the cycle monitor sets the cycle-started interrupt bit. It also detects missing cycle-start packets and sets the cycle-lost interrupt bit when this occurs. When the isochronous cycle is complete, the cycle monitor sets the cycle-done interrupt bit. The cycle monitor instructs the transmitter to send a cycle-start message when the cycle-master bit is set in the control register.

2.1.7 Cycle Redundancy Check (CRC)

The CRC module generates a 32-bit CRC for error detection. This is done for both the header and data. The CRC module generates the header and data CRC for transmitting packets and checks the header and data CRC for received data. See the IEEE 1394−1995 standard for details on the generation of the CRC.

2.1.8 Internal Register

The internal registers control the operation of the TSB42AC3.

2.1.9 Host Bus Interface

The host bus interface allows the TSB42AC3 to be easily connected to most host processors. This host bus interface consists of a 32-bit data bus and an 8-bit address bus. The TSB42AC3 utilize cycle-start and cycle-acknowledge handshake signals to allow the local bus clock and the 1394 clock to be asynchronous to one another. The host bus interface is capable of running at speeds up to 50 MHz. All bus signal labeling on the TSB42AC3 host interface use bit 0 to denote the most significant bit (MSB). The TSB42AC3 is interrupt driven to reduce polling.

3 Internal Registers

3.1 General

The host bus processor directs the operation of the TSB42AC3 through a set of registers internal to the TSB42AC3. These registers are read or written by asserting $\overline{\text{CS}}$ with the proper address on ADDR0−ADDR7 and asserting or deasserting $\overline{\text{WR}}$ depending on whether a read or write is needed. Figure 3−1 lists the register address; subsequent sections describe the function of the various registers.

3.2 Internal Register Definitions

The TSB42AC3 internal registers control the operation of the TSB42AC3. The bit definitions of the internal registers are shown in Figure 3−1 and are described in subsection 3.2.1 through 3.2.15.

There are three modes to access the internal link registers: normal mode, quick mode, and burst mode. The registers from address 00h to 2Ch are accessed using normal mode as shown in Figure 6−2 and Figure 6−3.

The registers 30h, 34h, 3Ch, 40h, 44h, 48h, and C0h may be accessed using quick mode reads as shown in Figure 6−5.

The register 30h and FIFO location 80h through 9Ch may be accessed using quick mode writes as shown in Figure 6−4.

NOTE:

The protocols for normal mode and quick mode are exactly the same. The only difference is that quick mode simply returns $\overline{\text{CA}}$ quicker.

FIFO locations 84h, 8Ch, 94h, 9Ch, A0h, and B0h may be accessed using burst mode writes as shown in Figure 6−6.

The register C0h may be access using burst mode read as shown in Figure 6−7.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
00h	Version (3031h)																Revision (3044h)																Version
04h	Bus Number										Node Number						Root	Reserved						ATAck					Reserved			AckV	Node Address
08h	IdVal	RxStd	BsyCtrl	RAI	RcvCvst	TxAEn	RxAEn	TxIEn	RxIEn	AckCEn	RstTx	RstRx	Reserved			11bitLREQ	Reserved				CyMas	CySrc	CyTEn	TrgEn	IRP1En	IRP2En	Reserved				FlshAckFIFO	FhBad	Control
0Ch	Int	PhInt	PhRRx	PhRst	SIDCom	TxRdy	RxDta	CmdRst	AckRcv	AckDisc	Reserved	ITBadF	ATBadF	Reserved	SntRj	HdrErr	TCErr	Reserved		CyTmo	CySec	CySt	CyDne	CyPnd	CyLst	CyArbFl	Reserved			ArbGap	FrGap	IsoArbFl	Interrupt
10h	Int	PhInt	PhRRx	PhRst	SIDCom	TxRdy	RxDta	CmdRst	AckRcv	AckDisc	Reserved	ITBadF	ATBadF	Reserved	SntRj	HdrErr	TCErr	Reserved		CyTmo	CySec	CySt	CyDne	CyPnd	CyLst	CyArbFl	Reserved			ArbGap	FrGap	IsoArbFl	Interrupt Mask
14h	7 Bits Seconds Count							Rollover @ 8000 13 Bits Cycle Count													Rollover @ 3072 12 Bits Cycle Offset												Cycle Timer
18h	TAG1		IR Port1						TAG2		IR Port2						Reserved															MonTag	Isoch Port Number
1Ch	CLrATF	ClrITF	ClrGRF	Reserved		Trigger Size									ATFSize									ITFSize									FIFO Control
20h	ENSp		Reserved		RegRW	Reserved																											Diagnostics
24h	RdPHY	WrPHY	Reserved		PHYRgAd				PHYRgData								Reserved				PHYRxAd				PHYRxData								PHY Chip Access
28h	Reserved																																Reserved
2Ch	Reserved																																Reserved
30h	ATF_Full	ATF_Empty	ConErr	AdrClr	Control	RAMTest	AdrCounter												Reserved					ATFSpaceCount									ATF Status (Read/Write)
34h	ITF_Full	ITF_Empty	Reserved																					ITFSpaceCount									ITF Status (Read Only)
38h	Reserved																																Reserved
3Ch	GRF_Empty	Cd	PacCom	GRF_TotalCount										GRF_Size										WriteCount									GRF Status (Read Only)
40h	AccFl	AccFM	LPS	SRst	Reserved																												Host Control
44h	Reserved											GPO2_Ctl					Reserved			GPO1_Ctl					Reserved			GPO0_Ctl					Mux Control
48h	ACKCnt			Reserved	tCode				PktID								NodeID						Reserved		AckCode				AckErr	Reserved			ACK FIFO (see Note B)
4Ch	Reserved																																Reserved
50h	Reserved																																Reserved
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

NOTES: A. All gray areas (bits) are reserved bits.
B. This register is new to the TSB42AC3.

Figure 3−1. TSB42AC3 Internal Register Map

3.2.1 Version/Revision Register (@00h)

The version/revision register allows software to be written that supports multiple versions of the high-speed serial-bus link-layer controllers. This register is at address 00h and is read only. The initial value is 3031−3044h.

Table 3−1. Version/Revision Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0 − 15	Version	Version	Version of the TSB42AC3
16 − 31	Revision	Revision	Revision of the TSB42AC3

3.2.2 Node-Address/Transmitter Acknowledge Register (@04h)

The node-address/transmitter acknowledge register controls which packets are accepted/rejected and presents the last acknowledge received for packets sent from the ATF. This register is at offset 04h. The bus number and node number fields are read/write. The AT acknowledge (ATAck) received is normally read only. Setting the regRW bit in the diagnostic register makes these fields read/write. Every PHY register 0 status transfer to the TSB42AC3 automatically updates the node number field and the root field. The initial value for this register is FFFF−0130h.

Table 3−2. Node-Address/ Transmitter Acknowledge Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0 − 9	BusNumber	Bus number	BusNumber is the 10-bit IEEE 1212 bus number that the TSB42AC3 uses with the node number in the source address for outgoing packets and to accept or reject incoming packets. The TSB42AC3 always accepts packets with a bus number equal to 3FFh.
10 − 15	NodeNumber	Node number	NodeNumber is the 6-bit node number that the TSB42AC3 uses with the bus number in the source address for outgoing packets and to accept or reject incoming packets. The TSB42AC3 always accepts packets with the node address equal to 3Fh. After bus reset, the node number is automatically set to the node’s Physical_ID by a PHY register 0 transfer.
16	Root	Root	If Root =1 this node is root. This bit is Read only.
17 − 22	Reserved	Reserved	Reserved
23 − 27	ATAck	Address transmitter acknowledge received	ATAck is the last acknowledge received by the transmitting node in response to a packet sent from the asynchronous transmit-FIFO. ATAck=0_XXXX => The low order 4 bits present normal AckCode receive from the receiving node. ATAck=1_0000 => An acknowledge timeout occurred. ATAck=1_0011 => Ack packet error (ack parity error, ack too long or ack too short).
28 − 30	Reserved	Reserved	Reserved
31	AckV	Acknowledge valid	Whenever an ack packet is received, AckValid is set to 1. After the node-address/transmitter acknowledge register is read, AckValid is automatically reset to 0. This bit is also used to indicate arbitration failure. If a nonbroadcast asynchronous packet is in the ATF ready to transmit and a TxRdy interrupt occurs, and AckValid is 0, this indicates no ack packet was received and no ack time-out occurred. The packet is still in the ATF and the TSB42AC3 automatically arbitrates for the bus again. Under normal conditions AckValid = 0 means ATAck contains last received ack code information.

3.2.3 Control Register (@08h)

The control register dictates the basic operation of the TSB12LV0C. This register is at address 08h and is read/write. The initial value is 0000_0000h.

Table 3−3. Control-Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	IdVal	ID valid	When IdVal is set, the TSB42AC3 accepts packets addressed to the IEEE 1212 address set (Node Number) in the node-address register. When IdVal is cleared, the TSB42AC3 accepts only broadcast packets.
1	RxSId	Received self-ID packets	When RxSId is set, the self-identification packets generated by the cable PHY during bus initialization are received and placed into the GRF as a single packet. Each self-identification packet is composed of two quadlets, where the second quadlet is the logical inverse of the first. If ACK (4 bits) equals 1h, then the data is good. If ACK equals Dh, then the data is wrong. When RxSld is set link-on packets and PHY configuration packets are also received and placed into the GRF. For these packets, only the first quadlet of each packet is stored in the GRF.
2	BsyCtrl	Busy control	When this bit is set, this node sends an ack_busy_x acknowledge packet in response to all received nonbroadcast asynchronous packets. When this bit is cleared, this node sends an ack_busy_x acknowledge packet only if the GRF is full (i.e., normal operation).
3	RAI	Received all isochronous packets	If RAI = 1 and RxIEn = 1, the TSB42AC3 receives all isochronous packets into the GRF.
4	RcvCySt	Receive cycle start	If RcvCySt = 1, the TSB42AC3 stores all received cycle-start packets in the GRF.
5	TxAEn	Transmitter enable	When TxAEn is cleared, the transmitter does not arbitrate or send asynchronous packets. After a bus reset, TxAEn is cleared since the node number may have changed.
6	RxAEn	Receiver enable	When RxAEn is cleared, the receiver does not receive any asynchronous packets. After a bus reset, RxAEn is cleared since the node number may have changed.
7	TxIEn	Transmit isochronous enable	When TxIEn is cleared, the transmitter does not arbitrate or send isochronous packets.
8	RxIEn	Receive isochronous enable	When RxIEn is cleared, the receiver does not receive isochronous packets.
9	AckCEn	Ack complete enable	When AckCEn is set, the TSB42AC3 sends an ack_complete code (0001) to the transmit node for receiving a nonbroadcast write request packet if the GRF is not full and there is no error in the packet. When AckCEn is cleared, the TSB42AC3 sends an ack_pending code (0010) for the above condition.
10	RstTx	Reset transmitter	When RstTx is set, the entire transmitter resets synchronously. This bit clears itself.
11	RstRx	Reset receiver	When RstRx is set, the entire receiver resets synchronously. This bit clears itself.
12−14	Reserved	Reserved	Reserved
15	11bitLREQ	11-Bit LREQ	When 11bitLREQ is set, it enables the TSB42AC3 to send an 11-bit bus request for the backplane PHY, which is 11 bits long.
16−19	Reserved	Reserved	Reserved
20	CyMas	Cycle master	When CyMas is set and the TSB42AC3 is attached to the root PHY, the cycle master function is enabled. When the cycle_count field of the cycle timer register increments, the transmitter sends a cycle-start packet. This bit is not cleared upon bus reset. If another node is selected as root during a bus reset, the transaction layer in the now nonroot TSB42AC3 node must clear this bit.
21	CySrc	Cycle source	When CySrc is set, the cycle_count field increments and the cycle_offset field resets for each positive transition of CYCLEIN. When CySrc is cleared, the cycle_count field increments when the cycle_offset field rolls over.
22	CyTEn	Cycle-timer enable	When CyTEn is set, the cycle_offset field increments. This bit must be set to transmit cycle-start packets if node is cycle master.
23	TrgEn	Trigger size function enable	If TrgEn is set, the receiver partitions the received packet into trigger size blocks. Trigger size is defined in the FIFO control register. The purpose of the trigger size function is to allow the receiver to receive a packet larger than the GRF size. The host bus can read the received data when each block is available without waiting for the whole packet to be loaded into the GRF. Host bus latency is therefore reduced.

Table 3−3. Control-Register Field Descriptions (Continued)

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
24	IRP1En	IR port 1 enable	When IRP1En is set, the receiver accepts isochronous packets when the channel number matches the value in the IR Port1 field at address 18h.
25	IRP2En	IR port 2 enable	When IRP2En is set, the receiver accepts isochronous packets when the channel number matches the value in the IR Port2 field at address 18h.
26 − 29	Reserved	Reserved	Reserved
30	FlshACKFI-FO	Flush acknowledge FIFO	Writing 1 to this bit automatically clears the ACK FIFO. This bit is self cleaning. Setting RstTX also clears the ACK FIFO.
31	FhBad	Flush Bad Packets	When FhBad is set, the receiver flushes any received bad packets (including a partial packet due to a GRF full condition) and does not generate a RxDta interrupt. Setting FhBad also disables the TrgEn function.

3.2.4 Interrupt and Interrupt-Mask Registers (@0Ch, @10h)

The interrupt and interrupt-mask registers work in tandem to inform the host bus interface when the state of the TSB42AC3 changes. The interrupt mask register is read/write. When regRW (diagnostic register @20h) is cleared to 0, the interrupt register (except for the Int bit) is cleared. When regRW is set to 1, the interrupt register (including the Int bit) is read/write.

The interrupt bits all work the same. For example, when a PHY interrupt occurs, the PhInt bit is set. If the PhIntMask bit is set, then the INT bit is set. If the IntMask is set, then the signal INT is asserted. The logic for the interrupt bit is shown in Figure 3−2. Table 3−4 defines the interrupt and interrupt-mask register field descriptions. As shown in Figure 3−2, the INT bit is the OR of all AND of interrupt bits and interrupt mask bits 1−31. When all the interrupt bits are cleared, INT equals 0. When any of the interrupt bits and their corresponding interrupt mask bits are set, INT is set 1, even if the INT bit was just cleared.

To reset the interrupt register, the host controller needs to write back the last value that was read. For example, if 3A7B00CFh was read from the interrupt register, in order to cause all bits to reset to 0, the host controller must write a 3A7B00CFh to the interrupt register.

The interrupt register initial value is 1000_0000h.

The interrupt register initial value is 0000_0000h.

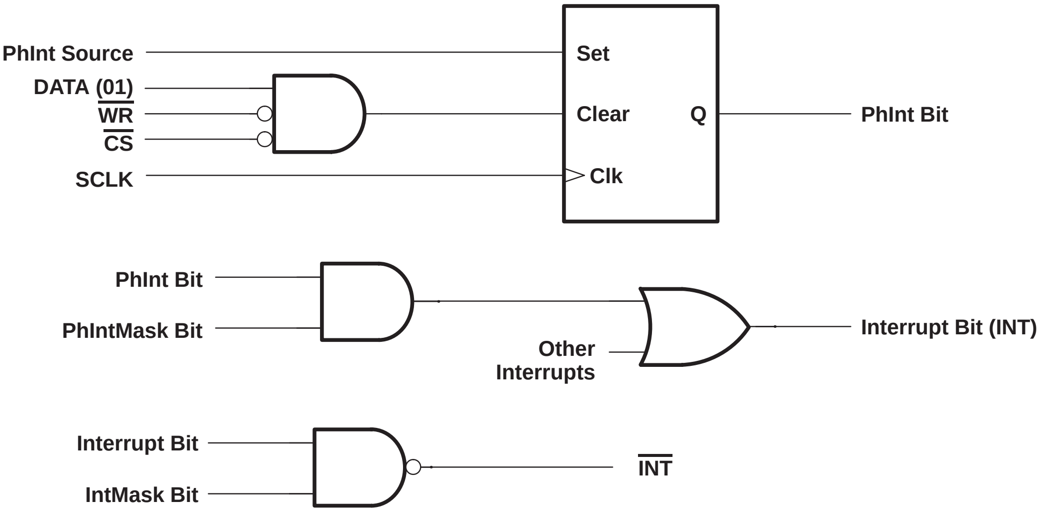


Figure 3−2. Interrupt Logic Diagram Example

Table 3−4. Interrupt- and Mask-Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	Int	Interrupt	The Int bit is the Or of all AND of interrupt bits and interrupt mask bits 1 − 31.
1	PhInt	Phy chip interrupt	When PhInt is set, the PHY chip has signaled an interrupt through the PHY interface.
2	PhyRRx	Phy register information received	When PhyRRx is set, a register value has been transferred to the PHY chip access register (offset 24h) from the PHY interface.
3	PhRst	Phy reset started	When PhRst is set, a PHY-layer reconfiguration has started (1394 bus reset).
4	SIDComp	Self ID Complete	When SIDComp is set, a complete bus reset process is finished. If the RxSld bit of the control register (@08h) is set, the GRF contains all received self-ID packets.
5	TxRdy	Transmitter ready	When TxRdy is set, the transmitter is idle and ready. If TxRdy is set to 1 and AckV (bit 31 @04h) remains 0 for a nonbroadcast asynchronous packet, the transmitter failed arbitration and arbitrates for the bus again when the bus is idle.
6	RxDta	Receiver has data	In normal mode and when set, RxDta indicates that the receiver has accepted a block of data (if TrgEn = 0, a block of data means a packet) into the GRF interface. However, during the self-ID portion of a bus reset, this bit is set after each self-ID process is done.
7	CmdRst	Command reset received	When CmdRst is set, the receiver has been sent a quadlet write request addressed to the RESET_START CSR register.
8	ACKRCV	Receive ACK packet Interrupt	This interrupt is triggered when an acknowledge packet is received or a timeout has occurred after an asynchronous packet is sent. To enable this register, the mask interrupt should be set to 1.
9	ACKDISC	ACK discard	This bit is set when an incoming acknowledge packet cannot be pushed into the ACK beacuse the ACK FIFO is full.
10	Reserved	Reserved	Reserved
11	ITBadF	Bad packet formatted in ITF	When ITBadF is set, the transmitter has detected invalid data at the isochronous transmit-FIFO interface.
12	ATBadF	Bad packet formatted in ATF	When ATBadF is set, the transmitter has detected invalid data at the asynchronous transmit-FIFO interface. If the first quadlet of a packet is not written to the ATF_First or ATF_First&Update address, the transmitter enters a state denoted by an ATBadF interrupt. An underflow of the ATF also causes an ATBadF interrupt. If this state is entered, no asynchronous packets can be sent until the ATF is cleared by way of the CLR ATF control bit. Isochronous packets can be sent while in this state.
13	Reserved	Reserved	Reserved
14	SntRj	Busy acknowledge sent by the receiver	SntRj is set when a GRF overflow condition occurs. The receiver is then forced to send a busy acknowledge packet in response to a packet addressed to this node.
15	HdrEr	Header error	When HdrEr is set, the receiver detected a header CRC error on an incoming packet that may have been addressed to this node. The packet is discarded.
16	TCErr	Transaction code error	When TCErr is set, the transmitter detected an invalid transaction code in the data at the transmit FIFO interface.
17−18	Reserved	Reserved	Reserved
19	CyTmOut	Cycle timer out	This bit is set if the isochronous cycle lasts for more than the nominal 125 μs.
20	CySec	Cycle second incremented	When CySec is set, the cycle-second field in the cycle-timer register is incremented. This occurs approximately every second when the cycle timer is enabled.
21	CySt	Cycle started	When CySt is set, the transmitter has sent or the receiver has received a cycle-start packet.
22	CyDne	Cycle done	When CyDne is set, a subaction gap has been detected on the bus after the transmission or reception of a cycle-start packet. This indicates that the isochronous cycle is over.
23	CyPnd	Cycle pending	When CyPnd is set, the cycle-timer offset is set to 0 (rolled over or reset) and remains set until the isochronous cycle ends.
24	CyLst	Cycle lost	When CyLst is set, the cycle timer has rolled over twice without the reception of a cycle-start packet. This occurs only when this node is not the cycle master.
25	CArbFI	Cycle arbitration failed	When CArbFI is set, the arbitration to send the cycle-start packet has failed.
26−28	Reserved	Reserved	Reserved

Table 3−4. Interrupt- and Mask-Register Field Descriptions (Continued)

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
29	ArbGp	Arbitration gap	Arbitration gap occurred
30	FrGp	Subaction gap	Subaction gap occurred
31	IArbFI	Isochronous arbitration failed	When IArbFI is set, the arbitration to send an isochronous packet has failed.

3.2.5 Cycle-Timer Register (@14h)

The cycle-timer register contains the second_count, cycle_count, and cycle_offset fields of the cycle timer. This register is controlled by the cycle master, cycle source, and cycle timer enable bits of the control register. This register is read/write and must be written to as a quadlet. The initial value of the cycle-timer register is 0000_0000h.

Table 3−5. Cycle-Timer Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0−6	seconds_count	Seconds count	1-Hz cycle-timer counter
7−19	cycle_count	Cycle count	8,000-Hz cycle-timer counter
20−31	cycle_offset	Cycle offset	24.576-MHz cycle-timer counter

3.2.6 Isochronous Receive-Port Number Register (@18h)

The isochronous receive-port number register controls which isochronous channels are received by this node. If the RAI bit of the control register is set, this register value is a *don't care* since all channels are received. The register is read/write. The initial value of the isochronous receive-port number register is 0000_0000h.

Table 3−6. Isochronous Receive-Port Number Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0−1	TAG1	Tag bit 1	Isochronous data format tag. See IEEE 1394-1995 6.2.3 and IEC 61883.
2−7	IRPort1	Isochronous receive TAG bits and port 1 channel number	IRPort1 contains the channel number of the isochronous packets the receiver accepts when IRP1En is set. See Table 4−6 and Table 4−7 for more information.
8−9	TAG2	Tag bit 2	Isochronous data format tag. See IEEE 1394-1995 6.2.3.
10−15	IRPort2	Isochronous receive TAG bits and port 2 channel number	IRPort2 contains the channel number of the isochronous packets the receiver accepts when IRP2En is set (bits 8 and 9 are reserved as TAG bits). See Table 4−6 and Table 4−7 for more information.
16−30	Reserved	Reserved	Reserved
31	MonTag	Monitor tag enable	When MonTag is set, the tag bit comparison is enabled. If both TAGx and IRPortx match for port number x, the matching receive isochronous packet is stored in the GRF.

3.2.7 FIFO Control Register (@1Ch)

The FIFO control register is used to clear the ATF, ITF, GRF, and set up a trigger size for the trigger-size function. ATF size and ITF size fields are specified in term of quadlets.

GRF Size = [2560 – (ATF size) – (ITF size)] quadlets. This register is read/write. The initial value of this register is 07FD_3299h.

Table 3−7. FIFO Control Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	ClrATF	Clear asynchronous transfer FIFO	Writing 1 to this bit automatically clears the ATF to 0. This bit is self clearing.
1	ClrITF	Clear isochronous transfer FIFO	Writing 1 to this bit automatically clears the ITF to 0. This bit is self clearing.
2	ClrGRF	Clear general receive FIFO	Writing 1 to this bit automatically clears the GRF to 0. This bit is self clearing.
3−4	Reserved	Reserved	Reserved
5−13	Trigger Size	Trigger size in quadlets	Trigger size is used to partition a received packet into several smaller blocks of data. For example: if trigger size = 8, total received packet size (excluding header CRC and data CRC) = 20 quadlets, the receiver creates three blocks of data in the GRF. Each block starts with a packet token quadlet to indicate how many quadlets follow this packet token. The first and the second block have nine quadlets (counting the packet token quadlet). The third block has five quadlets (including a packet token quadlet). Each block triggers one RxDta interrupt. The purpose of the trigger size function is to allow the receiver to receive a packet larger than the GRF size. The host bus can read the received data when each block is available without waiting for the whole packet to be loaded into the GRF. Host bus latency is therefore reduced. If TrgEn bit is 0 or FhBad bit is 1 in the control register, the trigger size is ignored.
14−22	ATFSize	Asynchronous transmitter FIFO size	ATFSize allocates ATF space size in quadlets. The value in this register indicates the actual FIFO size divided by 5. ATFSize must be less than or equal to 2560 and total transmit FIFO space (ATFSize + ITFSize) must also be less than or equal to 2560.
23−31	ITFSize	Isochronous transmitter FIFO size	ITFSize allocates ITF space size in quadlets. The value in this register indicates the actual FIFO size divided by 5. ITFSize must be less than or equal to 2560 and total transmit FIFO space (ATFSize + ITFSize) must also be less than or equal to 2560.

3.2.8 Diagnostic Control Register (@20h)

The diagnostic control and status register allows for the monitoring and control of the diagnostic features of the TSB42AC3. The regRW and ENSp bits are read/write. When regRW is cleared, all other bits are read only. When regRW is set, all bits are read/write.

The initial value of the diagnostic control and status register is 0000_0000h.

Table 3−8. Diagnostic Control and Status Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	ENSp	Enable snoop	When ENSp is set, the receiver accepts all packets on the bus regardless of the address or format. The receiver uses the snoop data format defined in Section 4.4.
1−3	Reserved	Reserved	Reserved
4	regR/W	Register read/ write access	When regR/ W is set, most registers become fully read/write.
5−31	Reserved	Reserved	Reserved

3.2.9 PHY-Chip Access Register (@24h)

The PHY-chip access register allows access to the registers in the attached PHY chip. The most significant 16 bits send read and write requests to the PHY-chip registers. The least significant 16 bits are for the PHY-chip to respond to a read request sent by the TSB42AC3. The PHY-chip access register also allows the PHY interface to send important information back to the TSB42AC3. When the PHY interface sends new information to the TSB42AC3, the PHY register information-information-receive (PHYRRx) interrupt is set. The register is at address 24h and is read/write. The initial value of the PHY-chip access register is 0000_0000h.

Table 3−9. PHY-Chip Access Register

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	RdPhy	Read PHY-chip register	When RdPhy is set, the TSB42AC3 sends a read register request with address equal to phyRgAd to the PHY interface. This bit is cleared when the request is sent.
1	WrPhy	Write PHY-chip register	When WrPhy is set, the TSB42AC3 sends a write register request with an address equal to phyRgAd on to the PHY interface. This bit is cleared when the request is sent.
2−3	Reserved	Reserved	Reserved
4−7	PhyRgAd	PHY-chip register address	PhyRgAd is the address of the PHY-chip register that is to be accessed.
8−15	PhyRgData	PHY-chip register data	PhyRgData is the data to be written to the PHY-chip register indicated in PhyRgAd.
16−19	Reserved	Reserved	Reserved
20−23	PhyRxAd	PHY-chip register received address	PhyRxAd is the address of the register from which PhyRxData came.
24−31	PhyRxData	PHY-chip register received data	PhyRxData contains the data from register addressed by PhyRxAd.

3.2.10 Asynchronous Transmit-FIFO (ATF) Status Register (@30h)

The ATF status register allows access to the registers that control or monitor the ATF. All the FIFO flag bits are read only and the FIFO control bits are read/write. This register provides RAM test mode control and status signals. In a RAM test read/write mode, the following steps should be followed:

1. Enable RAM test mode by setting the RAMTest bit (bit 5 in the register)
2. Set the AdClr bit in order to clear the RAM internal address counter
3. Perform the host bus read/write access to location c0h. This accesses RAM starting at location 00h. With every read/write access, the RAM internal address counter increments by one.

The initial valve of this register is 4000_0099h.

Table 3−10. ATF Status Register

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	Full	ATF full flag	When full is set, the FIFO is full. Write operations are ignored.
1	Empty	ATF-empty flag	When empty is set, the FIFO is empty.
2	ConErr	Control bit error	Each location in the FIFO is 33 bits wide. The MSB is called the control bit (cd bit), which is used to indicate the first quadlet of each packet in the ATF or the ITF. If the cd bit is 1, the quadlet at that location is the first quadlet of the packet in ATF or ITF, or a packet token in the GRF (packet token quadlet is defined in section 3.3.4). In RAM test mode, all FIFOs become a RAM. Control bits can be verified indirectly. If ConErr is1, the read value of the control bit does not match the write value, which is defined by the control bit (bit 4 in this register). ConErr is cleared to 0 by writing a 1 to the AdrClr bit or 0 to the RAMTest bit.
3	AdrClr	Address clear control	Set AdrClr to 1 to clear AdrCounter and ConErr to 0 during the next RAM access. The RAM test mode accesses location 0. AdrClr clears itself to 0.
4	Control	Control bit	The value of the control bit is used to relate the MSB of access RAM location in RAM test mode. For RAM test mode, WRITE− control bit value concatenated with DATA0 − DATA31 writes to the location pointed by the AdrCounter. For RAM test mode, READ− the read location is pointed to by the current AdrCounter. The read control counter bit is compared with control bit (bit 4) of ATF status register, if it does not match, it sets ConErr to 1.
5	RAMTest	RAM test mode	When RAM test to 1, all FIFO functions are disabled. Write to or Read from address c0h writes to or reads from the location pointed to by AdrCounter. After each write or read, the AdrCounter is incremented by 1. The AdrCounter address range is from 0 to 2499. For normal FIFO operation, clear RAMTest to 0. AdrClr and AdrCounter are in a *don't care* state in this case.
6−14	AdrCounter	Address counter	Gives the address location
15−22	Reserved	Reserved	Reserved
23−31	ATFSpace Count	ATF space count in quadlets	ATF available space for loading next packet into ATF. The value shows the actual internal 12 bit value divided by 5. If ATFSpaceCount is larger than the next packet, then the software can burst write the next packet into the ATF. It only requires two host bus transactions: one ATF status read and one burst write to ATF.

3.2.11 Isochronous Transmit FIFO (ITF) Status Register (@34h)

The ITF status register allows access to the registers that control or monitor the ITF. All the FIFO flag bits are read only and the FIFO control bits are read/write. The initial value of the isochronous transmit FIFO status register is 4000_0099h.

Table 3−11. ITF Status Register

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	Full	ITF full flag	When full is set, the FIFO is full and all subsequent writes are ignored.
1	Empty	Empty	When empty is set, ITF is empty.
2−22	Reserved	Reserved	Reserved
23−31	ITFSpace-Count	ITF space count in quadlets	ITF available space for loading the next packet to the ITF. The value shows the actual internal 12 bit value divided by 5. If ITFSpaceCount is larger than the next packet quadlet, then the software can burst write the next packet into the ITF. It only requires two host bus transactions: one ITF status read and one burst write to the ITF.

3.2.12 General Receive FIFO (GRF) Status Register (@3Ch)

The GRF status register allows access to the registers that control or monitor the GRF. All the FIFO flag bits are read only and the FIFO control bits are read/write. The initial value of the GRF status register is 8001_9800h.

Table 3−12. GRF Status Register

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	Empty	GRF empty flag	When empty is set, the GRF is empty.
1	cd	GRF controller bit	If cd = 1, the packet token is on the top of GRF and the next GRF read will be the packet token.
2	PacCom	Packet complete	When cd = 1 and PacCom = 1, the next block of data from the GRF is the last one for the packet. When cd = 1 and PacComp = 0, the next block of data from the GRF is just one block for the current received packet. If the trigger size function is disabled or flush bad packet bit is set, cd = 1 and PacCom is 1. This means each received packet only contains one block of GRF data. When cd = 0 PacCom is not valid.
3−12	GRFTotal Count	Total GRF data count stored in quadlet	GRF stored data count which includes all stored received packets and internally-generated packet tokens. The value shows the actual number of quadlets in the GRF divided by 5.
13−22	GRFSize	GRF size	GRFSize = 2560−(ATFSize+ITFSize) GRFSize is the total assigned space for the GRF. The value in this register indicates the actual FIFO size divided by 5.
23−31	WriteCount	Received data quadlet count of next block in GRF	This number is valid only when the cd bit is 1. It indicates the received data quadlet count of the next block. WriteCount does not account for the packet token quadlet. The packet token is always stored on the top of each received data block to provide a status report. This allows software to burst read the next block from the GRF. If trigger-size function is disabled or the flush bad received packets bit is set: To read each received packet from GRF, first read the GRF status register and make sure cd = 1, so the packet token is on the top of GRF. Next, perform a burst read from the GRF to read (WriteCount+1) quadlets, which includes the packet token. In cases where the trigger size function is enabled and FhBad = 0, read each block of received data as above, until PacCom is 1, which indicates that the block is the ending block of the current packet.

3.2.13 Host Control Register (@40h)

The host bus control register resides in the host processor clock (BCLK) domain. All the bits in this register are R/W with an initial value of 0000_0000h. Table 3−13 describes the bit fields of this register.

Table 3−13. Host Control Register Description

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0	AccsFailINT	Access failed interrupt	This bit is set when a host bus access is attempted to a register in the SCLK domain when SCLK is not running. To clear this bit, write a 1 to this bit location; a write of 0 has no effect (unless the regRW bit is set in the diagnostics register). Reset value = 0.
1	AccsFailM	Access failed interrupt mask	This bit is located in the host clock domain. If set to 1, the AccsFailINT is enabled. If set to 0, the AccsFailINT is masked off. Reset value = 0 (interrupt masked).
2	LPS_EN	LPS enable	A write of 1 to this bit enables generation of LPS (PowerOn signal). A write of 0 has no effect on LPS_EN. This bit is cleared while SoftReset bit is set to 1. Reset value = 1.
3	SoftReset	Software reset	A write of 1 to this bit generates a reset to the link and FIFO logic, clear TxAEn, RxAEn, TxIEn, and RxIEn in the control register, and clears LPS_EN in the this register. This bit remains set until a 0 is written to it. This bit does not change any other register values (except for the specified control register bits and the bits effected by these bits). Reset value = 0.
4 – 31	Reserved	Reserved	Reserved

3.2.14 Mux Control Register (@42h)

The MUX control register resides in the BCLK domain. After reset, the GRFEMP, CYDNE, and CYST pins have the same functionality as the TSB12LV01A and TSB12LV01B. Table 3−14, Table 3−15, and Table 3−16 describe the bit field of this register. Logic high on each GPO pin indicates that the corresponding internal device event or bus event has taken place. For example, if the GPO0 field is set to ‘00101’ and a high state is seen on pin 48 (GRFEMP/GPO0), the ATF Empty flag has been set. The power-up reset value of this register is 0000_0000h.

Table 3−14. Mux Control Register Description (GPO0 Field)

GPO0 FIELD (BITS 27–31)					DESCRIPTION OF GPO0 PIN (PIN 48)
0	0	0	0	0	GRF empty
0	0	0	0	1	Cycle done interrupt
0	0	0	1	0	GRF empty
0	0	0	1	1	Cycle started interrupt
0	0	1	0	0	ATF full
0	0	1	0	1	ATF empty
0	0	1	1	0	ITF full
0	0	1	1	1	ITF empty
0	1	0	0	0	ATAck Rcvd
0	1	0	0	1	SCLK/2
0	1	0	1	0	ArbGap
0	1	0	1	1	FairGap
0	1	1	0	0	GRF confirm
0	1	1	0	1	PacCom
0	1	1	1	0	Constant zero (drive low)
0	1	1	1	1	Constant one (drive high)
1	0	0	0	0	CD
1	X	X	X	X	GRF empty

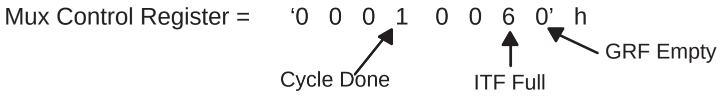
Table 3−15. Mux Control Register Description (GPO1 Field)

GPO1 FIELD (BITS 19–23)					DESCRIPTION OF GPO1 PIN (PIN 49)
0	0	0	0	0	Cycle done interrupt
0	0	0	0	1	Cycle done interrupt
0	0	0	1	0	GRF empty
0	0	0	1	1	Cycle started interrupt
0	0	1	0	0	ATF full
0	0	1	0	1	ATF empty
0	0	1	1	0	ITF full
0	0	1	1	1	ITF empty
0	1	0	0	0	ATAck Rcvd
0	1	0	0	1	SCLK/2
0	1	0	1	0	ArbGap
0	1	0	1	1	FairGap
0	1	1	0	0	GRF confirm
0	1	1	0	1	PacCom
0	1	1	1	0	Constant zero (drive low)
0	1	1	1	1	Constant one (drive high)
1	0	0	0	0	CD
1	X	X	X	X	Cycle done interrupt

Table 3−16. Mux Control Register Description (GPO2 Field)

GPO2 FIELD (BITS 11–15)					DESCRIPTION OF GPO2 PIN (PIN 50)
0	0	0	0	0	Cycle start interrupt
0	0	0	0	1	Cycle done interrupt
0	0	0	1	0	GRF empty
0	0	0	1	1	Cycle started interrupt
0	0	1	0	0	ATF full
0	0	1	0	1	ATF empty
0	0	1	1	0	ITF full
0	0	1	1	1	ITF empty
0	1	0	0	0	ATAck Rcvd
0	1	0	0	1	SCLK/2
0	1	0	1	0	ArbGap
0	1	0	1	1	FairGap
0	1	1	0	0	GRF confirm
0	1	1	0	1	PacCom
0	1	1	1	0	Constant zero (drive low)
0	1	1	1	1	Constant one (drive high)
1	0	0	0	0	CD
1	X	X	X	1	Cycle started interrupt

EXAMPLE: To monitor GRFEMP, ITF full, and Cycle Done on the general-purpose output pins, the following setting for the MUX control register may be used:



Mux Control Register = ‘0 0 0 1 0 0 6 0’ h

In this case:

GPO0 = ‘00000’ b

GPO1 = ‘00110’ b

GPO2 = ‘00001’ b

3.2.15 Acknowledge (ACK) FIFO Register (@ 48h)

The ACK FIFO retains the last six acknowledges returned by external nodes in response to the last six asynchronous packets transmitted from the TSB42AC3. The host processor tracks which acknowledge was returned for each of the last six asynchronous packets by accessing the ACK FIFO via the ACK FIFO register. The power-up reset value of this register is 0000_0000h.

Table 3−17. ACK FIFO Register Field Descriptions

BITS	ACRONYM	FUNCTION NAME	DESCRIPTION
0−2	AckCnt	Acknowledge Count	This binary encoded value represents the number of acknowledges currently available in the ACK FIFO.
3	Reserved	Reserved	Reserved
4−7	tCode	Transaction code	This field contains the transaction code for the current packet. See Table 6−9 of the IEEE1394−1995 Standard.
8−15	PktID	Packet ID	Packet identifier − This field encodes the packet identification information for the current transmit packet. This field represents bits 8 through 20 of the first quadlet of the transmitted 1394 packet, respectively (tlabel)
16−21	NodeID	Node ID	Destination node ID − not valid for asynchronous streaming packet.
22−23	Reserved	Reserved	Reserved
24−27	AckCode	Acknowledge Code	The value in the field represents the 1394 ACK code generated by the receiving node. ACK_Complete is always returned by the link layer controller internally for asynchronous streaming and broadcast packet. A list of ACK codes is included in Table 4−5.
28	AckErr	Acknowledge code error	When this bit is set to 1, an acknowledge code was returned with an error. This indicates that the asynchronous packet has experienced a transmit failure.
29−31	Reserved	Reserved	Reserved

3.3 FIFO Access

Access to all the transmit FIFOs is fundamentally the same; only the address to where the write is made changes.

3.3.1 General

The TSB42AC3 controller FIFO-access address map shown in Figure 3−3 illustrates how the FIFOs are mapped. The suffix_First denotes the FIFO location where the first quadlet of a packet should be written when the writer wants to transmit the packet. The first quadlet will be held in the FIFO until a quadlet is written to an update location.

The suffix_Continue denotes a write to the FIFO location where the second through n−1 quadlets of a packet could be written. The data is not confirmed for transmission.

The last quadlet of a multiple quadlet packet should be written to the FIFO location with the notation_Continue and Update. The suffix_Continue and update denotes a write to the FIFO location where the second through n quadlets of a packet could be written when the writer wants the packet to be transmitted as soon as possible. However, in this case the writes to the FIFO must be put into the FIFO faster than data is removed from the FIFO and placed on the 1394 bus or an error will result.

	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31	
80h	ATF_First	ATF Normal access FIFO Locations
84h	ATF_Continue	
88h	Reserved	
8Ch	ATF_Continue & Update	
90h	ITF_First	ITF Normal access FIFO Locations
94h	ITF_Continue	
98h	Reserved	
9Ch	ITF_Continue & Update	
A0h	ATF_Burst_Write	ATF Burst Write
A4h	Reserved	
A8h	Reserved	
ACh	Reserved	
B0h	ITF_Burst_Write	ITF Burst Write
B4h	Reserved	
B8h	Reserved	
BCh	Reserved	
C0h	GRF Data	GRF Read Location
C4h	Reserved	
C8h	Reserved	
CCh	Reserved	

Figure 3−3. TSB42AC3 Controller-FIFO-Access Address Map

3.3.2 ATF Access

The procedure to access the ATF through 80h, 84h, and 8Ch is as follows:

1. Write the first quadlet of the packet to ATF location 80h and sets the control bit to 1 to indicate the first quadlet of the packet, the data is not confirmed for transmission.
2. Write the second to n−1 quadlets of the packet to AT F location 84h. Burst write can be used to write n−2 quadlets into ATF, which requires only one host write transaction. The data is not confirmed for transmission.
3. Write the last quadlet of the packet to the ATF location 8Ch. It can support burst write, which allows multiple quadlets to load into ATF and the data is confirmed for transmission. If consecutive writes to ATF_Continue and update do not keep up with the data being put on the 1394 bus, an ATF underflow error occurs.

If the first quadlet of a packet is not written to the ATF_FIRST address, the transmitter enters a state denoted by an ATBadF interrupt. An underflow of the ATF also causes an ATBadF interrupt. When this state is entered, no asynchronous packets can be sent until the ATF is cleared via the ClrATF control bit. Isochronous packets can be sent while in this state. For example, if an asynchronous write request packet is addressed to a nonexistent address, the TSB42AC3 waits until a time out occurs and sets ATAck (in the node address register) to ‘1_0000’b. After the asynchronous packet is sent, the sender reads ATAck. If ATAck = ‘1_0000”b, then a time out has occurred (i.e., no response from any node was received).

The procedure to access ATF through A0h is as follows:

- Write to address A0h (ATF burst write) writes the whole packet into ATF. The first quadlet written into the ATF has the control bit set to 1 to indicate this is the first quadlet of the packet, the rest of the packet have the control bit set to 0. The last quadlet written into ATF confirms the packet for transmission.
- To do burst write, the host bus must continuously drive $\overline{CS}$ low, TSB42AC3 loads DATA0−DATA31 to ATF during each rising edge of BCLK when $\overline{CS}$ is low, and at the same time it asserts $\overline{CA}$ and $\overline{CA}$ is one cycle behind $\overline{CS}$. The control bit is 0 for ATF_Continue and ATF_Continue and Update.

ATF access example:

The first quadlet of n quadlets is written to ATF location 80h. Quadlets (2 to n−1) are written to ATF location 84h. The last quadlet (nth) is written to the ATF location 8Ch. If the ATFEmpty bit is true, it is set to false and the TSB42AC3 requests the PHY to arbitrate for the bus. To ensure that an ATF underflow condition does not occur, loading of the ATF in this manner is recommended.

After loading the ATF with an asynchronous packet and sending it, the software driver needs to wait until the TxRdy (bit 5) of the interrupt register is set to 1 before reading ATFEmpty. TxRdy is set to 1 indicates either the asynchronous packet is sent from the ATF or time out due to the arbitration failure. If the ATFEmpty flag is set to 1, then the asynchronous packet is sent. If the ATFEmpty flag is set to 0, then the arbitration fails and this node needs to rearbitrate for the bus. AckV is read after the ATFEmpty flag is checked It is recommended that a delay of several clock cycles after checking ATFEmpty before reading the AckV. AckV is 1, indicating that an ACK packet has been received. In order to receive the next Ack code, the TxRdy bit needs to be cleared to 0.

Example 1−1. Non-Burst Write

80h (ATF_First)	DATA1[0:31]
84h (ATF_Continue)	DATA2[0:31]
.	.
.	.
84h (ATF_Continue)	DATA(n−1)[0:31]
8Ch (ATF_Continue & Update)	DATAn[0:31]

Example 1−2. Allowable Burst Write

80h (ATF_First)	DATA1[0:31]
84h (ATF_Continue) (burst write)	DATA2[0:31]
.	.
.	.
84h (ATF_Continue) (burst write)	DATA(n−1)[0:31]
8Ch (ATF_Continue & Update)	DATAn[0:31]

Example 1−3. Allowable Burst Write, But Riskier

80h (ATF_First)	DATA1[0:31]
8Ch (ATF_Continue & Update) (burst write)	DATA2[0:31]
.	.
.	.
8Ch (ATF_Continue & Update)	DATAn[0:31]

NOTE:

If writes to ATF_Continued & update do not keep up with data being put on the 1394 bus, an ATF underflow error will occur.

Example 1−4. Allowable Burst Write

A0h (ATF burst write)	DATA1[0:31]
.	.
.	.
A0h (ATF burst write)	DATAn[0:31]

Example 1−4 only requires one host bus write transaction. The packet is stored in the ATF in the following format:

{1, DATA1[0:31]}
{0, DATA2[0:31]}
{0, DATA3[0:31]}
.
.
{0, DATA(n−1)[0:31]}
{0, DATAn[0:31]}

3.3.3 ITF Access

The procedure to access to the ITF through 90h, 94h, and 9Ch is as follows:

1. Write the first quadlet of the packet to ITF location 90h and set the control bit to 1 to indicate the first quadlet of the packet, the data is not confirmed for transmission.
2. Write second to n−1 quadlets of the packet to ITF location 94h. Burst write can be used to write n−2 quadlets into ITF, which requires only one host write transaction, the data is not confirmed for transmission.
3. Write the last quadlet of the packet to ITF location 9Ch. It supports burst write, which allows multiple quadlets to load into ITF. The data is confirmed for transmission. If consecutive writes to ITF_Continue and update does not keep up with the data being put on the 1394 bus, an ITF underflow error occurs.

If the first quadlet of a packet is not written to the ITF_FIRST, the transmitter enters a state denoted by an ITFBadF interrupt. An underflow of the ITF also causes an ITFBadF interrupt. When this state is entered, no isochronous packets can be sent until the ITF is cleared by the ClrITF control bit. Asynchronous packets can be sent while in this state.

The procedure to access the ITF through B0h is as follows:

- Write to address B0h (ITF burst write) writes the whole packet into ITF. The first quadlet written into ITF has the control bit set to 1 to indicate this is the first quadlet of the packet. The termination of the burst write on the host interface confirms the packet for transmission.

ITF access example:

Assume there are n quadlets needed to write to ITF for transmission.

Example 1−5. Non-Burst Write

90h (ITF_First)	DATA1[0:31]
94h (ITF_Continue)	DATA2[0:31]
.	.
.	.
94h (ITF_Continue)	DATA(n−1)[0:31]
9Ch (ITF_Continue & Update)	DATAn[0:31]

Example 1−6. Allowable Burst Write

90h (ITF_First)	DATA1[0:31]
94h (ITF_Continue) (burst write)	DATA2[0:31]
.	.
.	.
94h (ITF_Continue) (burst write)	DATA(n−1)[0:31]
9Ch (ITF_Continue & Update)	DATAn[0:31]

Example 1−7. Allowable Burst Write, But Riskier

```
90h (ITF_First)                                   DATA1[0:31]
9Ch (ITF_Continue & Update) (burst write)         DATA2[0:31]
          .                                               .
          .                                               .
9Ch (ITF_Continue & Update) (burst write)         DATAn[0:31].
```

NOTE:

If consecutive writes to ITF_Continue & Update do not keep up with data being put on the 1394 bus, an ITF underflow error will occur.

Example 1−8. Allowable Burst Write

```
B0h (ITF burst write)            DATA1[0:31]

B0h (ITF burst write)            DATA2[0:31]
          .                            .
          .                            .
B0h (ITF burst write)            DATA(n−1)[0:31]

B0h (ITF burst write)            DATAn[0:31]
```

Example 1−8 only requires one host bus write transaction. The packet stores in ITF as following format:

```
{1, DATA1[0:31]}
{0, DATA2[0:31]}
{0, DATA3[0:31]}
        .
        .
{0, DATA(n−1)[0:31]}
{0, DATAn[0:31]}
```

3.3.4 General-Receive FIFO (GRF)

Access to the GRF is done with a read from the GRF, which requires a read from address C0h.

Read from the GRF can be done in burst mode. Before reading the GRF, check whether the RxDta interrupt is set, which indicates data stored in GRF is ready to read. The GRF status register may also be read and the cd bit checked if it is 1 and the write count is greater than 0. The cd bit is equal to 1 means the packet token is on top of GRF. The whole block of data contains one packet token followed by received quadlets equal to the write count.

When packet token is read, it has the following format:

- Bit 0−6 reserved
- Bit 7−10 ackSnpd. When snoop mode is enabled, this field indicates the acknowledge seen on the bus after the packet is received. If snoop mode is disabled, ackSnpd contains 4’b0.
- Bit 11 PacComp − same value as in the GRF status register when cd bit is 1. PacComp means packet complete. If PacComp is 1, this block is the last block of this packet or this block contains the whole receive packet.
- Bit 12 EnSp (bit0 of diagnostic register). If EnSp is 1, GRF contains snooped packets which includes asynchronous packets and isochronous packets. When snoop mode is enabled, all header and data CRC quadlets are stored in the GRF.
- Bit 13−14 RcvPktSpd − receive packet speed

    00 − 100 Mbits/s
    01 − 200 Mbits/s
    10 − 400 Mbits/s

- Bit 15−23 WriteCount − quadlet count in this block excluding packet token. WriteCount is the same number shown in GRF status register when cd bit is 1.
- Bit 24−27 tCode − received packet tCode. For received self-ID packets, phy configuration, and Link-on packets, the tCode field contains 4’b1110 to indicate these special packets.
- Bit 28−31 Ack − Ack code sent to the transmit node for this packet when PacComp = 1. If PacComp = 0, this field is don’t care. If EnSp is 1(snoop mode is enabled), this field indicates whether the entire packet snooped was correct. For received PHY configuration and Link-on packets, this field is 4’b0000.

If trigger size function is enabled, RxDta interrupt triggers whenever each block in GRF is available for read for the same long received packet. To enable trigger size, TrgEn of the control register should be set to 1, FhBad of the control register should be cleared to 0, and the trigger size of the FIFO control register should be set to greater than 5. Therefore, the trigger size function does not apply to receive self-ID packets, PHY configuration packet, link-on packets, or quadlet read or write packets.

As an example, if a read response for data block packet is received at 400 Mbits/s, the total received data is 14 quadlets excluding header CRC and data CRC, trigger size function is enabled, and trigger size is six. The packet token is shown in hex format.

The following example generates three RxDta interrupts.

The data is stored in GRF as follows:

```
{1, 0004_0670}      <− first packet token, PacComp = 0
{0, quadlet_1[0:31]}
{0, quadlet_2[0:31]}
{0, quadlet_3[0:31]}
{0, quadlet_4[0:31]}
{0, quadlet_5[0:31]}
{0, quadlet_6[0:31]}

{1, 0004_0670}       <− second packet token, PacComp = 0
{0, quadlet_7[0:31]}
{0, quadlet_8[0:31]}
{0, quadlet_9[0:31]}
{0, quadlet_10[0:31]}
{0, quadlet_11[0:31]}
{0, quadlet_12[0:31]}
{1, 0014_0271}       <− the last packet token, PacComp = 1, Ack = 4’0001
{0, quadlet_13[0:31]}
{0, quadlet_14[0:31]}
```

The following example generates one RxDta interrupt. If the trigger size function is disabled, the data is stored in the GRF as follows:

```
{1, 0014_0E71}      <− packet token, PacComp = 1, WriteCount = 14, Ack = 4’0001
{0, quadlet_1[0:31]}
{0, quadlet_2[0:31]}
{0, quadlet_3[0:31]}
{0, quadlet_4[0:31]}
{0, quadlet_5[0:31]}
{0, quadlet_6[0:31]}
{0, quadlet_7[0:31]}
{0, quadlet_8[0:31]}
{0, quadlet_9[0:31]}
{0, quadlet_10[0:31]}
{0, quadlet_11[0:31]}
{0, quadlet_12[0:31]}
{0, quadlet_13[0:31]}
{0, quadlet_14[0:31]}
```

3.3.5 RAM Test Mode

The purpose of RAM mode is to test the RAM with writes and reads. During RAM test mode, RAM, which makes up the ATF, ITF, and GRF, is accessed directly from the host bus. Different data is written to and read back from the RAM and compared with what was expected to be read back. ATF status, ITF status, and GRF status are not changed during RAM test mode, but the stored data in RAM is changed by any write transaction. To enable RAM test mode, set RAMTest bit of the ATF status register. Before beginning any read or write to the RAM, the AdrClr bit of the ATF status register should be set to clear ConErr. This action also clears the AdrClr bit.

During RAM test mode, the host bus address should be C0h. The first host bus transaction (either read or write) accesses location 0 of the RAM. The second host bus transaction accesses location 1 of the RAM. The nth host bus transaction accesses location n−1 of the RAM. After each transaction, the internal RAM address counter is incremented by one.

The RAM has 2560 locations with each location containing 33 bits. The most significant bit is the control bit. When the control bit is set, that indicates the quadlet is the start of the packet. In order to set the control bit, the control bit of the ATF status register has to be set. In order to clear the control bit, the control bit of the ATF status register has to be cleared. When a write occurs, the 32 bits of data from the host bus is written to the low order 32 bits of the RAM and the value in control bit 1 is written to the control bit. When a read occurs, the low order 32 bits of RAM are sent to the host data bus and the control bit is compared to the control bit of the ATF status register. If the read value does bit match the write value, ConErr of the ATF status register is set. This does not stop operation and another read or write can immediately be transmitted. To clear ConErr, set AdrClr of the ATF status register.

Another way to access a specific location in the RAM during RAM test mode is to write the desired value to AdrCounter of the ATF status register. The next RAM test read or write accesses the location pointed to by AdrCounter. AdrCounter contains current RAM address in RAM test mode.

During RAM test mode, any location inside the FIFO can be accessed by writing the address to AdrCounter of the ATF status register. Each read or write accesses the location pointed to by AdrCounter and AdrCounter increments by 1 after each transaction. Set AdrClr of the ATF status register clears the AdrCounter to 0 and clear ConErr of the ATF status register to 0.

Set RAMTest (bit 5) of the ATF status register to 1 to enable RAM test mode. A write to address C0h writes {Control1, DATA0−DATA31} to the location pointed to by AdrCounter. A read from address C0h reads from the location pointed to by AdrCounter. The control bit value can be determined by checking ConErr (bit 2) and Control1 (bit 4) of the ATF status register.

Table 3−18. Control Bit Value

CONERR	CONTROL1	CONTROL BIT VALUE
1	1	0
0	1	1
1	0	1
0	0	0

Another way to read the control bit value is to read the cd bit (bit 1) of the GRF status register before reading a quadlet from address C0h in RAM test mode. The cd bit contains the control bit value pointed to by the current address counter.

The ATF start address is 0. The ITF start address is equal to the ATF size. The GRF start address is equal to (ATF size + ITF size). FIFO operation temporarily stops during RAM test mode. Clear RAMTest (bit 5) of the ATF status register to 0 resumes normal FIFO operation.

4 TSB42AC3 Data Formats

The data formats for transmission and reception of data are shown in the following sections. The transmit format describes the expected organization of data presented to the TSB42AC3 at the host-bus interface. The receive formats describe the data format that the TSB42AC3 presents to the host-bus interface.

4.1 Asynchronous Transmit (Host Bus to TSB42AC3)

Asynchronous transmit refers to the use of the asynchronous-transmit FIFO (ATF) interface. There are two basic formats for data to be transmitted. The first is for quadlet packets and the second is for block packets. For transmit, the FIFO address indicates the beginning, middle, and end of a packet. All packet formats described in this section refer to the way the packets are stored in the internal FIFO memory of the TSB42AC3. The host application must conform to the packet formats specified in this section when accessing the ATF for a write operation and the GRF for a read operation.

4.1.1 Quadlet Transmit

The IEEE 1394-1995 standard specifies four types of quadlet transmit packets: write request, read request, write response, and read response packets. Table 4−1 describes the details of each packet.

4.1.1.1 Quadlet Write-Request and Read-Request Packets

The format for a quadlet write-request packet is shown in Figure 4−1. The first quadlet contains the packet control information. The second and third quadlets contain the 64-bit quadlet-aligned destination address. The fourth quadlet is the quadlet data used. The format for a quadlet read-request packet is shown in Figure 4−2.

<table>
<tr><th>0 1 2 3 4 5 6 7 8 9 10 11 12 13</th><th>14 15</th><th>16 17 18 19 20 21</th><th>22 23</th><th>24 25 26 27</th><th>28 29 30 31</th></tr>
<tr><td>Reserved</td><td>spd</td><td>tLabel</td><td>rt</td><td>tCode</td><td>priority</td></tr>
<tr><td colspan="2">destinationID</td><td colspan="4">destinationOffsetHigh</td></tr>
<tr><td colspan="6">destinationOffsetLow</td></tr>
<tr><td colspan="6">quadlet data</td></tr>
</table>

Figure 4−1. Quadlet-Transmit Format (Write Request)

<table>
<tr><th>0 1 2 3 4 5 6 7 8 9 10 11 12 13</th><th>14 15</th><th>16 17 18 19 20 21</th><th>22 23</th><th>24 25 26 27</th><th>28 29 30 31</th></tr>
<tr><td>Reserved</td><td>spd</td><td>tLabel</td><td>rt</td><td>tCode</td><td>priority</td></tr>
<tr><td colspan="2">destinationID</td><td colspan="4">destinationOffsetHigh</td></tr>
<tr><td colspan="6">destinationOffsetLow</td></tr>
</table>

Figure 4−2. Quadlet-Transmit Format (Read Request)

4.1.1.2 Quadlet Write-Response and Read-Response Packets

The format for a quadlet write-response packet is shown in Figure 4−3. The first quadlet contains the packet control information. The first 16 bits of the second quadlet is the destination identifier, which is the address of the destination or requesting node. The second quadlet also contains the response code of this transaction. The third quadlet is reserved. For a quadlet read-response packet, which is shown in Figure 4−4, the fourth quadlet is the quadlet data used.

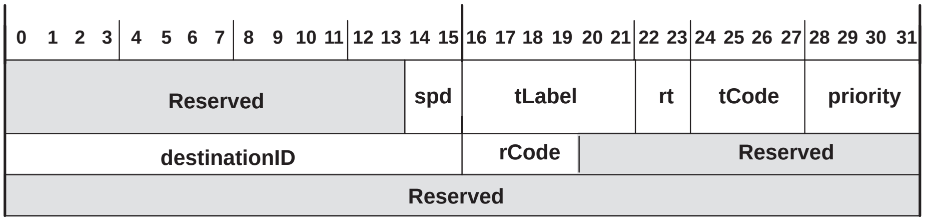


Figure 4−3. Quadlet-Transmit Format (Write Response)

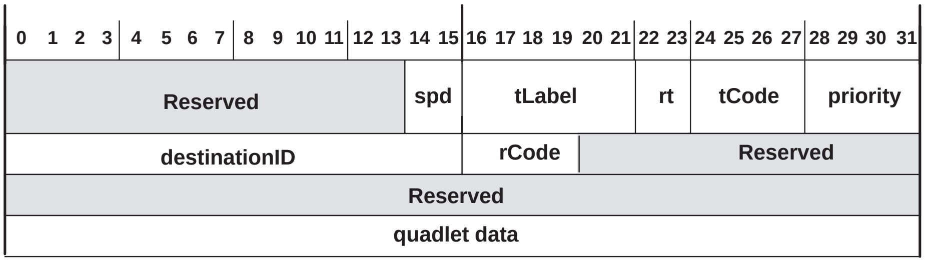


Figure 4−4. Quadlet-Transmit Format (Read Response)

Table 4−1. Quadlet-Transmit Format

<table>
<tr><th>FIELD NAME</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td>spd</td><td colspan="3">The spd field indicates the speed at which the current packet is to be sent (00 = S100, 01 = S200, 10 = S400, and 11 is undefined).</td></tr>
<tr><td>tLable</td><td colspan="3">The tLabel field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This field is used to pair up a response packet with its corresponding request packet.</td></tr>
<tr><td>rt</td><td colspan="3">The rt field is the retry code for the current packet: 00 = new, 01 = retry_X, 10 = retry_A, and 11 = retry_B.</td></tr>
<tr><td>tCode</td><td colspan="3">The tCode field is the transaction code for the current packet (see Table 6−10 of IEEE 1394−1995 standard).</td></tr>
<tr><td>priority</td><td colspan="3">The priority field contains the priority level for the current packet. For cable implementation, all zeros indicate fair arbitration.</td></tr>
<tr><td>sourceID</td><td colspan="3">This is the node ID (bus ID and physical ID) of the sender of this packet.</td></tr>
<tr><td>destinationID</td><td colspan="3">The destinationID field is the concatenation of the 10-bit bus number and the 6-bit node number that forms the destination node address of the current packet.</td></tr>
<tr><td rowspan="9">rCode</td><td colspan="3">Specifies the result of the read request transaction. The response code that may be returned to the requesting agent are defined as follows:</td></tr>
<tr><th>Response Code</th><th>Name</th><th>Description</th></tr>
<tr><td>0</td><td>Resp_complete</td><td>Node successfully completed requested operation.</td></tr>
<tr><td>1−3</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>4</td><td>Resp_conflict_error</td><td>Resource conflict detected by responding agend. Request may be retried.</td></tr>
<tr><td>5</td><td>Resp_data_error</td><td>Hardware error. Data not available.</td></tr>
<tr><td>6</td><td>Resp_type_error</td><td>Field within request packet header contains unsupported or invalid value.</td></tr>
<tr><td>7</td><td>Resp_address_error</td><td>Address location within specified node not accessible</td></tr>
<tr><td>8−Fh</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>destination OffsetHigh
destination OffsetLow</td><td colspan="3">The concatenation of these two fields addresses a quadlet in the destination node address space. This address must be quadlet aligned (modulo 4).</td></tr>
<tr><td>quadlet data</td><td colspan="3">For write requests and read response, the quadlet data field holds the data to be transferred. For write responses and read requests, this field is not used and should not be written into the FIFO.</td></tr>
</table>

4.1.2 Block Transmit

The IEEE 1394−1995 standard specifies four types of block transmit packets: write request, write response, read request, and read response packet. Table 4−2 describes the details of each packet.

4.1.2.1 Block Write-Request and Read-Request packets

The format for a block write-request packet is shown in Figure 4−5. The first quadlet contains the packet control information. The second and third quadlets contain the 64-bit quadlet-aligned address. The first 16 bits of the fourth quadlet contain the dataLength field. This is the number of bytes of data in the packet. The remaining 16 bits represent the extended_tCode field (see Table 6−11 of IEEE 1394−1995 standard for more information on extend_tCodes). The block data, if any, follows the extended_tCode. The format for a block read-request is shown in Figure 4−6.

0 1 2 3 4 5 6 7 8 9 10 11 12 13	14 15	16 17 18 19 20 21	22 23	24 25 26 27	28 29 30 31
Reserved	spd	tLabel	rt	tCode	priority
destinationID		destinationOffsetHigh			
destinationOffsetLow					
dataLength		extended_tCode			
block data					

Figure 4−5. Block-Transmit Format (Write Request)

0 1 2 3 4 5 6 7 8 9 10 11 12 13	14 15	16 17 18 19 20 21	22 23	24 25 26 27	28 29 30 31
Reserved	spd	tLabel	rt	tCode	priority
destinationID		destinationOffsetHigh			
destinationOffsetLow					
dataLength		extended_tCode			

Figure 4−6. Block-Transmit Format (Read Request)

4.1.2.2 Block Read-Response and Write-Response Packets

The format for a block read-response packet is shown in Figure 4−7. The first quadlet contains the packet control information. The first 16 bits of the second quadlet is the destination identifier, which is the address of the destination or requesting node. The second quadlet also contains the response code of this transaction. The third quadlet is reserved. The first 16 bits of the fourth quadlet contains the dataLength field. This is the number of bytes of data in the packet. The remaining 16 bits represent the extended_tCode field. The block data, if any, follows the extended_tCode. The format for a block write response is shown in Figure 4−8.

0 1 2 3 4 5 6 7 8 9 10 11 12 13	14 15	16 17 18 19	20 21	22 23	24 25 26 27	28 29 30 31
Reserved	spd	tLabel		rt	tCode	priority
destinationID		rCode	Reserved			
Reserved						
dataLength		extended_tCode				
block data						

Figure 4−7. Block-Transmit Format (Read Response)

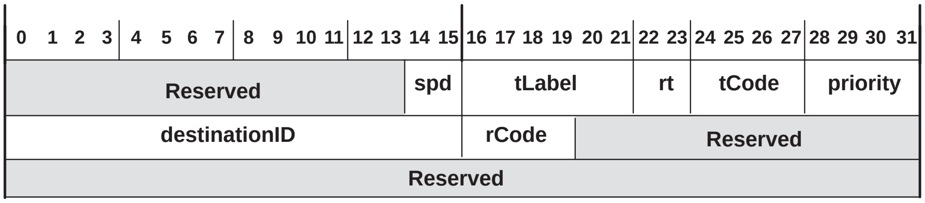


Figure 4−8. Block-Transmit Format (Write Response)

Table 4−2. Block-Transmit Format Functions

FIELD NAME	DESCRIPTION		
spd	The spd field indicates the speed at which the current packet is to be sent (00 = S100, 01 = S200, 10 = S400, and 11 is undefined).		
tLabel	The tLabel field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This field is used to pair up a response packet with its corresponding request packet.		
rt	The rt field is the retry code for the current packet: 00 = new, 01 = retry_X, 10 = retry_A, 11 = retry_B.		
tCode	The tCode field is the transaction code for the current packet (see Table 6−10 of IEEE 1394−1995 standard).		
priority	The priority field contains the priority level for the current packet.		
destinationID	The destinationID field is the concatenation of the 10-bit bus number and the 6-bit node number that forms the destination node address of the current packet.		
rCode	Specifies the result of the read request transaction. The response codes that may be returned to the requesting agent are defined as follows:		
	Response Code	**Name**	**Description**
	0	resp_complete	Node successfully completed requested operation.
	1−3	Reserved	Reserved
	4	resp_conflict_error	Resource conflict detected by responding agent. Request may be retried.
	5	resp_data_error	Hardware error. Data not available.
	6	resp_type_error	Field within request packet header contains unsupported or invalid value.
	7	resp_address_error	Address location within specified node not accessible.
	8−Fh	Reserved	Reserved

4.2 Asynchronous Receive (TSB42AC3 to Host Bus)

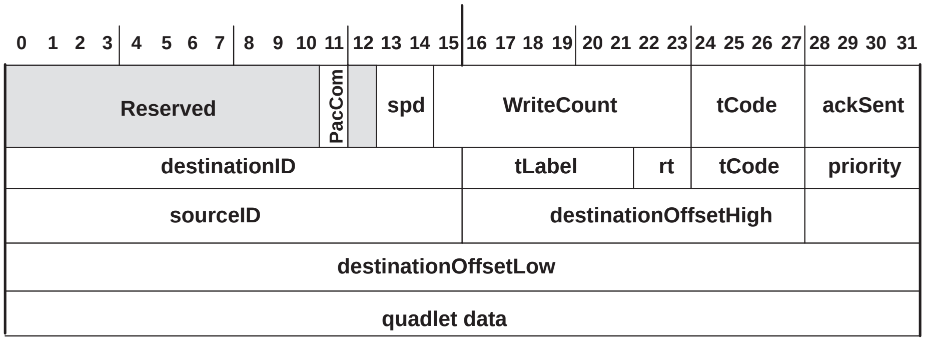
The general-receive FIFO (GRF) is shared by asynchronous data and isochronous data. There are two basic formats for data to be received. The first format is for quadlet packets and the second format is for block packets. For block receives, the data length, which is found in the header of the packet, determines the number of bytes in the packet. All packet formats described in this section refer to the way the packets are stored in the internal FIFO memory of the TSB42AC3.

4.2.1 Quadlet Receive

The IEEE 1394−1995 standard specifies four types of quadlet receive packet: write request, read request, write response, and read response packets. Table 4−3 describes the detail of the packet.

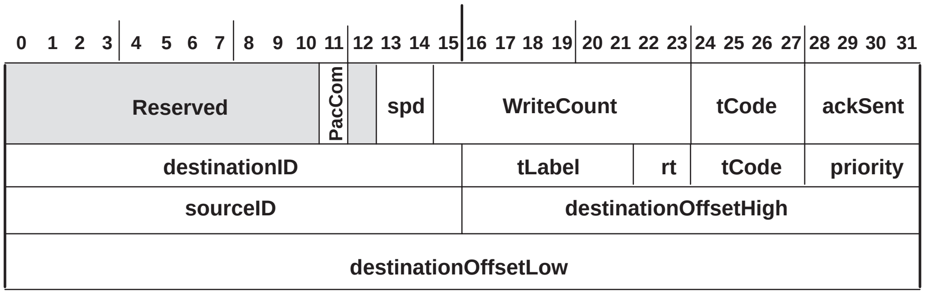
4.2.1.1 Quadlet Write-Request and Read-Request Packets

The format for a quadlet write-request packet is shown in Figure 4−9. The first quadlet read from the GRF is the packet token described in section 3.3.4. It contains packet reception status information added by the TSB42AC3. The first 16 bits of the second quadlet contains the destination node and bus ID. The remaining 16 bits contain the packet control information. The first 16 bits of the third quadlet contains the node and bus ID of the source. The remaining 16 bits of the third quadlet and the entire fourth quadlet contains the 48-bit quadlet aligned destination offset address. The fifth quadlet contains the data used by the write request packet. The format for a quadlet read-request packet is shown in Figure 4−10.



0 1 2 3 4 5 6 7 8 9 10	11	12	13 14	15 16 17 18 19 20 21 22 23	24 25 26 27	28 29 30 31
Reserved	PacCom		spd	WriteCount	tCode	ackSent
destinationID	tLabel	rt	tCode	priority		
sourceID	destinationOffsetHigh					
destinationOffsetLow						
quadlet data						

Figure 4−9. Quadlet-Receive Format (Write Request)

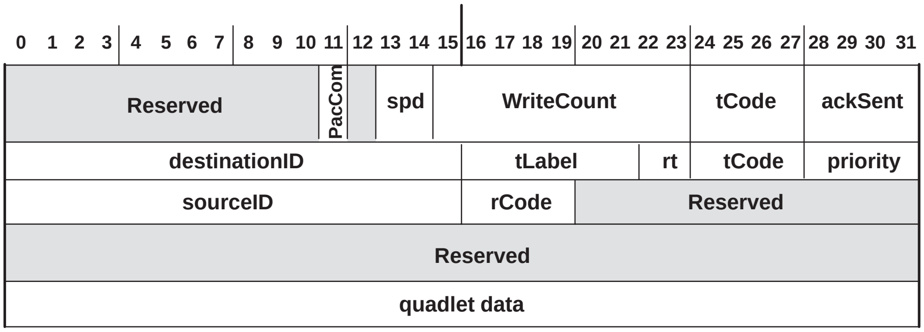


0 1 2 3 4 5 6 7 8 9 10	11	12	13 14	15 16 17 18 19 20 21 22 23	24 25 26 27	28 29 30 31
Reserved	PacCom		spd	WriteCount	tCode	ackSent
destinationID	tLabel	rt	tCode	priority		
sourceID	destinationOffsetHigh					
destinationOffsetLow						

Figure 4−10. Quadlet-Receive Format (Read Request)

4.2.1.2 Quadlet Read-Response and Write-Response Packets

The format for a quadlet read-response packet is shown in Figure 4−11. The first quadlet reads from the GRF is the packet token described in section 3.3.4. It contains packet reception status information added by the TSB42AC3. The first 16 bits of the second quadlet contains the destination node and bus ID. The remaining 16 bits contain the packet control information. The first 16 bits of the third quadlet contain the node and bus ID of the source. The third quadlet also contains the response code of this transaction. The fourth quadlet is reserved. The fifth quadlet is the quadlet data used. The format for a quadlet write-response packet is shown in Figure 4−12.



0 1 2 3 4 5 6 7 8 9 10	11	12	13 14	15 16 17 18 19 20 21 22 23	24 25 26 27	28 29 30 31
Reserved	PacCom		spd	WriteCount	tCode	ackSent
destinationID	tLabel	rt	tCode	priority		
sourceID	rCode	Reserved				
Reserved						
quadlet data						

Figure 4−11. Quadlet-Receive Format (Read Response)

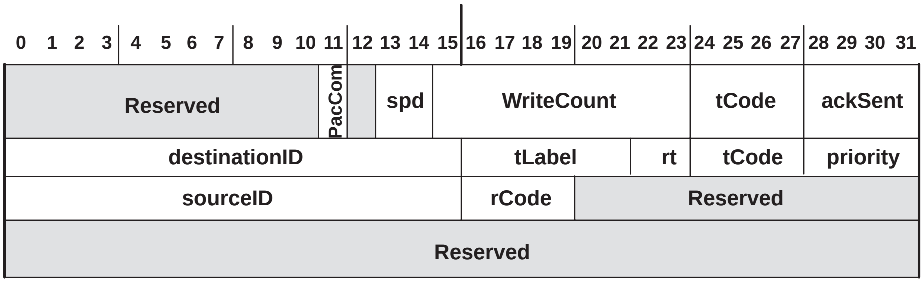


Figure 4−12. Quadlet-Receive Format (Write Response)

Table 4−3. Quadlet-Receive Format Functions

<table>
<tr><th>FIELD NAME</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td>PacCom</td><td colspan="3">Packet Complete. When PacCom = 1, the current block of data is the last one for the packet. When PacCom = 0, the current block of data is just another block of the current packet.</td></tr>
<tr><td>spd</td><td colspan="3">The spd field indicates the speed at which the current packet is to be sent (00 = S100, 01 = S200, and 10 = S400, and 11 is undefined).</td></tr>
<tr><td>WriteCount</td><td colspan="3">WriteCount indicates the number of data quadlets in the packet.</td></tr>
<tr><td>tCode</td><td colspan="3">The tCode field is the transaction code for the current packet (See Table 6−10 of IEEE 1394-1995 standard).</td></tr>
<tr><td>ackSent</td><td colspan="3">This 5-bit field holds the acknowledge code sent by the receiver for the current packet (See Table 6−13 of the IEEE 1394-1995 standard).</td></tr>
<tr><td>destinationID</td><td colspan="3">The destinationID field is the concatenation of the 10-bit bus number and the 6-bit node number that forms the destination node address of the current packet.</td></tr>
<tr><td>tLabel</td><td colspan="3">The tLabel field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This field is used to pair up a response packet with its corresponding request packet.</td></tr>
<tr><td>rt</td><td colspan="3">The rt field is the retry code for the current packet is: 00 = new, 01 = retry_X, 10 = retryA, and 11 = retryB.</td></tr>
<tr><td>priority</td><td colspan="3">The priority field contains the priority level for the current packet.</td></tr>
<tr><td>sourceID</td><td colspan="3">This is the node ID (bus ID and physical ID) of the sender of this packet.</td></tr>
<tr><td>destination OffsetHigh,
destination OffsetLow</td><td colspan="3">The concatenation of these two fields addresses a quadlet in the destination node address space. This address must be quadlet aligned (modulo 4).</td></tr>
<tr><td rowspan="9">rCode</td><td colspan="3">Specifies the response to an earlier corresponding request action. The response codes that may be returned to the requesting agent are defined as follows:</td></tr>
<tr><th>Response Code</th><th>Name</th><th>Description</th></tr>
<tr><td>0</td><td>resp_complete</td><td>Node successfully completed requested operation.</td></tr>
<tr><td>1−3</td><td>Reserved</td><td></td></tr>
<tr><td>4</td><td>resp_conflict_error</td><td>Resource conflict detected by responding agent. Request may be retried.</td></tr>
<tr><td>5</td><td>resp_data_error</td><td>Hardware error. Data not available.</td></tr>
<tr><td>6</td><td>resp_type_error</td><td>Field within request packet header contains unsupported or invalid value.</td></tr>
<tr><td>7</td><td>resp_address_error</td><td>Address location within specified node not accessible.</td></tr>
<tr><td>8–Fh</td><td>Reserved</td><td></td></tr>
<tr><td>quadlet data</td><td colspan="3">For write requests and read responses, the quadlet data field holds the data to be transferred. For write responses and read requests, this field is not used and should not be written into the FIFO.</td></tr>
</table>

4.2.2 Block Receive

The IEEE 1394−1995 standard specified four types of block receive packets: write request, read request, write response, and read response packet. Table 4−4 describes the detail of the packet.

4.2.2.1 Block Write-Request and Read-Request Packets

The format for a block write-request packet is shown in Figure 4−13. The first quadlet read from the GRF is the packet token described in section 3.3.4. It contains packet-reception status information added by the TSB42AC3. The first 16 bits of the second quadlet contains the destination node and bus ID. The remaining 16 bits contains the packet control information. The first 16 bits of third quadlet contains the node and bus ID of the source. The remaining 16 bits of the third quadlet contains and the entire fourth quadlet contain the 48-bit, quadlet aligned destination offset address. The first 16 bits of the fifth quadlet contain the dataLength field. The remaining 16 bits represent the extended_tCode field. The block data, if any, follows the extended_tCode. The format for a block read-request packet is shown in Figure 4−14.

<table>
<tr><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>8</th><th>9</th><th>10</th><th>11</th><th>12</th><th>13</th><th>14</th><th>15</th><th>16</th><th>17</th><th>18</th><th>19</th><th>20</th><th>21</th><th>22</th><th>23</th><th>24</th><th>25</th><th>26</th><th>27</th><th>28</th><th>29</th><th>30</th><th>31</th></tr>
<tr><td colspan="11">Reserved</td><td>PacCom</td><td></td><td colspan="2">spd</td><td colspan="9">WriteCount</td><td colspan="4">tCode</td><td colspan="4">ackSent</td></tr>
<tr><td colspan="16">destinationID</td><td colspan="6">tLabel</td><td colspan="2">rt</td><td colspan="4">tCode</td><td colspan="4">priority</td></tr>
<tr><td colspan="16">sourceID</td><td colspan="16">destinationOffsetHigh</td></tr>
<tr><td colspan="32">destinationOffsetLow</td></tr>
<tr><td colspan="16">dataLength</td><td colspan="16">extended_tCode</td></tr>
<tr><td colspan="32">block data (if any)</td></tr>
</table>

Figure 4−13. Block-Receive Format (Write Request)

<table>
<tr><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>8</th><th>9</th><th>10</th><th>11</th><th>12</th><th>13</th><th>14</th><th>15</th><th>16</th><th>17</th><th>18</th><th>19</th><th>20</th><th>21</th><th>22</th><th>23</th><th>24</th><th>25</th><th>26</th><th>27</th><th>28</th><th>29</th><th>30</th><th>31</th></tr>
<tr><td colspan="11">Reserved</td><td>PacCom</td><td></td><td colspan="2">spd</td><td colspan="9">WriteCount</td><td colspan="4">tCode</td><td colspan="4">ackSent</td></tr>
<tr><td colspan="16">destinationID</td><td colspan="6">tLabel</td><td colspan="2">rt</td><td colspan="4">tCode</td><td colspan="4">priority</td></tr>
<tr><td colspan="16">sourceID</td><td colspan="16">destinationOffsetHigh</td></tr>
<tr><td colspan="32">destinationOffsetLow</td></tr>
<tr><td colspan="16">dataLength</td><td colspan="16">extended_tCode</td></tr>
</table>

Figure 4−14. Block-Receive Format (Read Request)

4.2.2.2 Block Read-Response and Write-Response Packets

The format for a block read-response packet is shown in Figure 4−15. The first quadlet read from the GRF is the packet token described in section 3.3.4. It contains the packet-reception information added by the TSB42AC3. The first 16 bits of the second quadlet contains the destination node and bus ID. The remaining 16 bits contain the packet control information. The first 16 bits of the third quadlet contain the node and bus ID of the source. The third quadlet also contains the response code of this transaction. The fourth quadlet is reserved. The first 16 bits of fifth quadlet contains the dataLength field. The remaining 16 bits represent the extended_tCode field. The block data, if any, follows the extend_tCode. The format for a block write-response packet is shown in Figure 4−16.

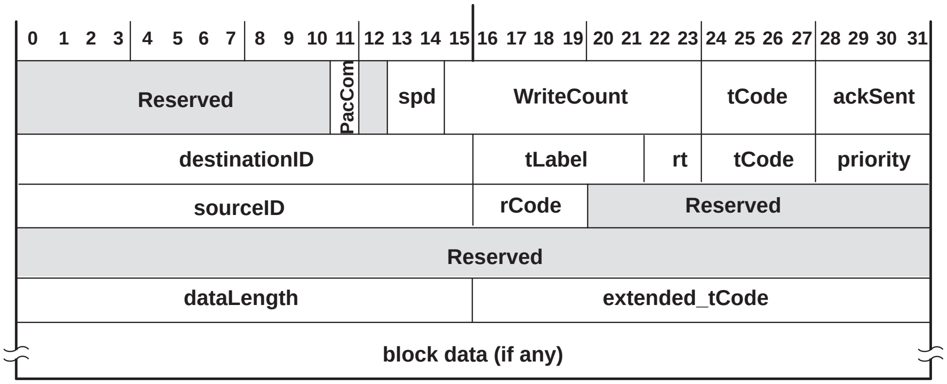


Figure 4−15. Block-Receive Format (Read Response)

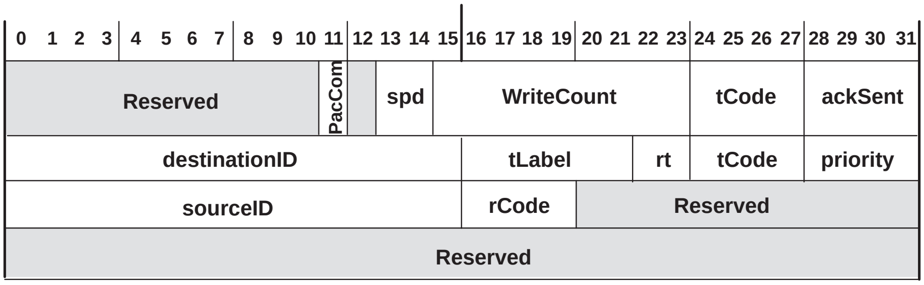


Figure 4−16. Block-Receive Format (Write Response)

Table 4−4. Block-Receive Format Functions

FIELD NAME	DESCRIPTION
PacCom	Packet Complete. When PacCom = 1, the current block of data is the last one for the packet. When PacCom = 0, the current block of data is just another block of the current packet.
spd	The spd field indicates the speed at which the current packet is to be sent (00 = S100, 01= S200, 10 = S400, and 11 is undefined).
WriteCount	WriteCount indicates the number of data quadlets in the packet.
tCode	The tCode field is the transaction code for the current packet (See Table 6−10 of IEEE 1394−1995 standard).
ackSent	This 5-bit field holds the acknowledge code sent by the receiver for the current packet (See Table 6−13 of IEEE 1394−1995 standard).
destinationID	The destinationID field is the concatenation of the 10-bit bus number and 6-bit node number that forms the destination node address of the current packet.
tLabel	The tLabel field is the transaction label, which is a unique tag for each outstanding transaction between two nodes. This field is used to pair up a response packet with its corresponding request packet.
rt	The rt field is the retry code for the current packet: 00 = new, 01= retry_X, 10 = retry_A, and 11 = retry_B.
priority	The priority field contains the priority level for the current packet
sourceID	This is the node ID (bus ID and physical ID) of the sender of this packet.

<table>
<tr><th>FIELD NAME</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td rowspan="9">rCode</td><td colspan="3">Specifies the response to an earlier corresponding request action. The response codes that may be returned to the requesting agent are defined as follows:</td></tr>
<tr><th>Response Code</th><th>Name</th><th>Description</th></tr>
<tr><td>0</td><td>resp_complete</td><td>Node successfully completed requested operation.</td></tr>
<tr><td>1−3</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>4</td><td>resp_conflict_error</td><td>Resource conflict detected by responding agent. Request may be retried.</td></tr>
<tr><td>5</td><td>resp_date_error</td><td>Hardware error. Data not available.</td></tr>
<tr><td>6</td><td>resp_type_error</td><td>Field within requested packet header contains unsupported or invalid value.</td></tr>
<tr><td>7</td><td>resp_address_error</td><td>Address location within specified node not accessible.</td></tr>
<tr><td>8−Fh</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>Block data</td><td colspan="3">The block data field contains the data to be sent.</td></tr>
</table>

4.3 Asynchronous Acknowledge Buffer

The asynchronous acknowledge buffer retains the last six acknowledges returned by external nodes in response to the last six asynchronous packets transmitted from the TSB42AC3. The host processor can track which acknowledge was returned for each of the last six asynchronous packets by accessing this buffer via the ACK FIFO register.

The acknowledge tracking buffer contains a 32-bit quadlet for every asynchronous packet transmitted from the node. This quadlet contains information on the acknowledge received, the destinationID, the tLabel, retry code, tCode, and ack count for a transmitted packet.

The ACK FIFO register (@ 48h) also gives information on transmitted asynchronous packets. This register is updated after each full read from the ACK FIFO register (upper and lower 16 bits). Bits 4−7 give the ACK code for the transmitted packet. The ACK_ERR and ACK codes are described in Table 4−5. This ACK code is from the receiving node if the asynchronous packet was transmitted correctly or from the transmitter logic if an error occurred on transmission.

Table 4−5. ACK Code Description

ERRORBIT_ACK CODE	DESCRIPTION
0_0001	ACK_COMPLETE
0_0010	ACK_PENDING
0_0100	ACK_BUSY_X
0_0101	ACK_BUSY_A
0_0110	ACK_BUSY_B
0_1011	ACK_TARDY
0_1100	ACK_CONFLICT_ERROR
0_1101	ACK_DATA_ERROR
0_1110	ACK_TYPE_ERROR
0_1111	ACK_ADDRESS_ERROR
1_0000	ACK_TIMEOUT
1_0011	ACK_PACKET_ERROR

4.4 Isochronous Transmit (Host Bus to TSB42AC3)

The format of the isochronous transmit packet is shown in Figure 4−17 and is described in Table 4−6. The data for each channel must be presented to the isochronous transmit FIFO (ITF) interface in this format in the order that packets are to be sent. The transmitter requests the bus to send any packets available at the isochronous transmit interface immediately following reception or transmission of the cycle-start message.

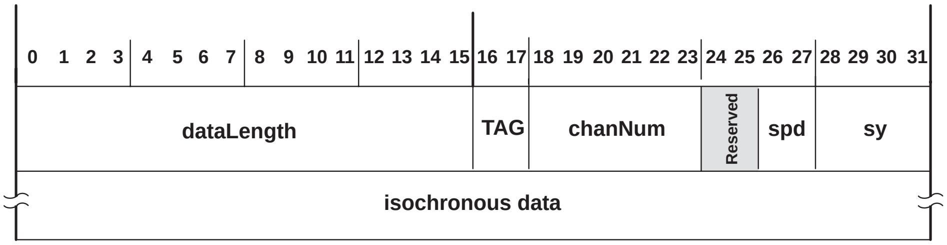


Figure 4−17. Isochronous-Transmit Format

Table 4−6. Isochronous-Transmit Functions

FIELD NAME	DESCRIPTION
dataLength	The dataLength field indicates the number of bytes in the current packet.
TAG	The TAG field indicates the format of data carried by the isochronous packet (00 = formatted, 01 – 11 are reserved).
chanNum	The chanNum field carries the channel number with which the current data is associated.
spd	The spd field indicates the speed at which the current packet is to be sent (00 = S100, 01 = S200, 10 = S400, and 11 is undefined).
sy	The sy field carries the transaction layer-specific synchronization bits.
isochronous data	The isochronous data field contains the data to be sent with the current packet. The first byte of data must appear in byte 0 of the first quadlet of this field. If the last quadlet does not contain four bytes of data, the unused bytes should be padded with zeros.

4.5 Isochronous Receive (TSB42AC3 to Host Bus)

The format of the isochronous receive packet is shown in Figure 4−18 and is described in Table 4−7. The data length, which is found in the header of the packet, determines the number of bytes in an isochronous packet.

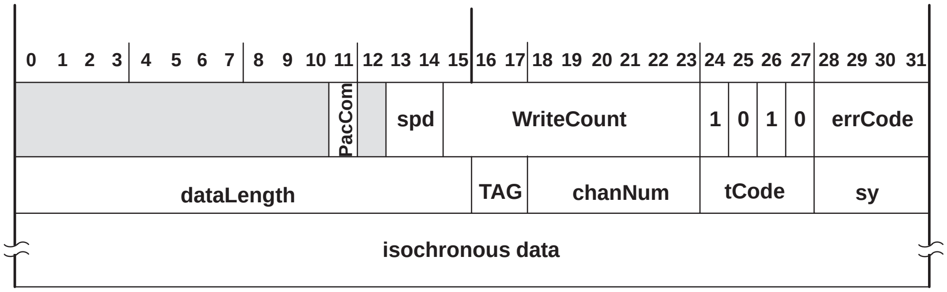


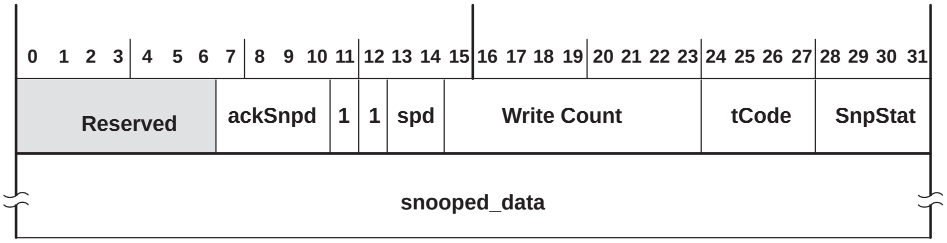
Figure 4−18. Isochronous-Receive Format

Table 4−7. Isochronous-Receive Functions

FIELD NAME	DESCRIPTION
PacCom	Packet complete. When PacCom = 1, the current block of data is the last one for the packet. When PacCom = 0, the current block of data is just another block of the current packet.
spd	The spd field indicates the speed at which the current packet is to be sent (00 = S100, 01 = S200, 10 = S400, and 11 is undefined).
WriteCount	WriteCount indicates the number of data quadlets in the packet.
errCode	The errCode field indicates whether the current packet has been received correctly. The possibilities are Complete, DataErr, or CRCErr,and have the same encoding as the corresponding acknowledge codes (see Table 6−13 of the IEEE 1394−1995 standard).
dataLength	The dataLength field indicates the number of bytes in the current packet.
TAG	The TAG field indicates the format of data carried by isochronous packet (00 = formatted, 01 – 11 are reserved).
chanNum	The chanNum field contains the channel number with which this data is associated.
tCode	The tCode field carries the transaction code for the current packet (tCode = Ah).
sy	The sy field carries the transaction layer-specific synchronization bits.
isochronous data	The isochronous data field has the data to be sent with the current packet. The first byte of data must appear in byte 0 of the first quadlet of this field. If the last quadlet does not contain four bytes of data, the unused bytes should be padded with zeros.

4.6 Snoop Receive

The format of the snoop data is shown in Figure 4−19. The receiver module can be directed to receive any and all packets that pass by on the serial bus. In this mode, the receiver presents the data received to the receive-FIFO interface.



NOTES: A. Bit 11 (PacCom)=1
B. Bit 12 (EnSp) = 1. This is bit 0 of the diagnostic register.

Figure 4−19. Snoop Format

Table 4−8. Snoop Functions

FIELD NAME	DESCRIPTION
ackSnpd	Acknowledge snooped. This field indicates the acknowledge seen on the bus after the packet is received.
spd	This field indicates the speed at which the packet was sent (00 = S100, 01 = S200, 10 = S400, and 11 is undefined).
WriteCount	WriteCount indicates the number of data quadlets in the packet.
tCode	The tCode field is the transaction code for the current packet (See Table 6−10 of the IEEE 1394−1995 standard).
SnppStat	This field indicates whether the entire packet snooped was received correctly. A value equal to the ack_complete acknowledge code indicates complete reception. This field has the same encoding as the corresponding acknowledge codes (See Table 6−3 of the IEEE 1394−1995 standard).
snooped data	This field contains the entire packet received or as much as could be received into the GRF.

4.7 CycleMark

The format of the CycleMark data is shown in Figure 4−20 and is described in Table 4−9. The receiver module inserts a single quadlet to mark the end of an isochronous cycle. The quadlet is inserted into the GRF.

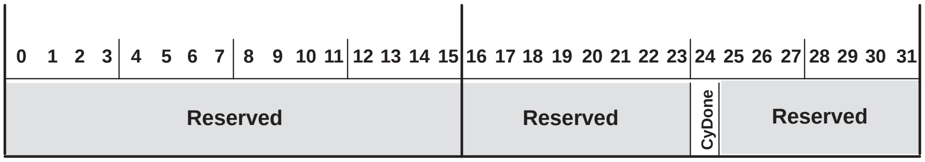


Figure 4−20. CycleMark Format

Table 4−9. CycleMark Function

FIELD NAME	DESCRIPTION
CyDone	The CyDone field indicates the end of an isochronous cycle.

4.8 PHY Configuration Transmit

The transmit format of the PHY-configuration packet is shown in Figure 4−21 and described in Table 4−10. The PHY-configuration packet contains three quadlets, which are loaded into the ATF. The first quadlet is the tCode for an unformatted packet. This is written into ATF_First at address 80h and has a value of 0000_00E0h. The second quadlet consists of actual data. This is written into the ATF_Continue at address 84h and has a value of the first quadlet of the PHY-configuration packet. The third quadlet is the logical inverse of the second quadlet and written into the ATF_Continue and Update at address 8Ch and has a value of the second quadlet of the PHY-configuration packet.

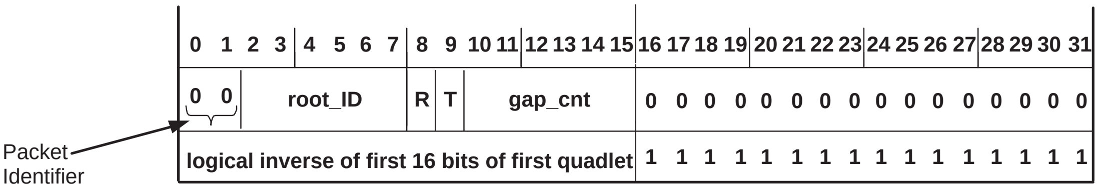


Figure 4−21. PHY-Configuration Packet Format

There is a possibility of a false header error on receipt of a PHY configuration packet. If the first 16 bits of a PHY configuration packet happen to match the destination identifier of a node (bus number and node number), the TSB42AC3 on those nodes issues a header error, since the node misinterprets the PHY configuration packet as a data packet addressed to the node. The suggested solution to this potential problem is to assign bus numbers that all have the most significant bit set to 1. Since the all-ones case is reserved for addressing the local bus, this leaves only 511 available unique bus identifiers. This is an artifact of the IEEE 1394−1995 standard.

The PHY configuration packet can perform the following functions:

- Set the gap count field of all nodes on the bus to a new value. The gap count, if set intelligently, can optimize bus performance.
- Force a particular node to be the bus root after the next bus reset.

It is not valid to transmit a PHY configuration packet with both the ‘R’ bit and ‘T’ bit set to zero. This would cause the packet to be interpreted as an extended PHY packet.

Table 4−10. PHY-Configuration Functions

FIELD NAME	DESCRIPTION
00	The00 field is the PHY configuration packet indentifier.
root_ID	The root_ID field is the physical_ID of the node to have its force_root bit set (only meaningful when R is set).
R	When R is set, the force-root bit of the node identified in root_ID is set and the force_root bit of all other nodes are cleared. When R is cleared, root_ID is ignored.
T	When T is set, the gap count field of all the nodes is set to the value in the gap_cnt field.
gap_cnt	The gap_cnt field contains the new value for gap count for all nodes. This value goes into effect immediately upon receipt and remains valid after the next bus reset. After the second reset, gap_cnt is set to 63h unless a new PHY-configuration packet is received.

4.9 Link-On Transmit

The transmit format of the link-on packet is shown in Figure 4−22 and described in Table 4−11. The link-on packet contains three quadlets, which are loaded into the ATF. The first quadlet is the tCode for an unformatted packet. This is written into ATF_First at address 80h and has a value of 0000_00E0h. The second quadlet consists of actual data. This is written into the ATF_Continue at address 84h and has a value of the first quadlet of the link-on packet. The third quadlet is the logical inverse of the second quadlet and written into the ATF_Continue and Update at address 8Ch and has a value of the second quadlet of the link-on packet.

There is a possibility of a false header error on receipt of a link−on packet. If the first 16 bits of a link-on packet happen to match the destination identifier of a node (bus number and node number), the TSB42AC3 on those nodes issues a header error, since the node misinterprets the link-on packet as a data packet addressed to the node. The suggested solution to this potential problem is to assign bus numbers that all have the most significant bit set to 1. Since the all-ones case is reserved for addressing the local bus, this leaves only 511 available unique bus identifiers. This is an artifact of the IEEE 1394−1995 standard.

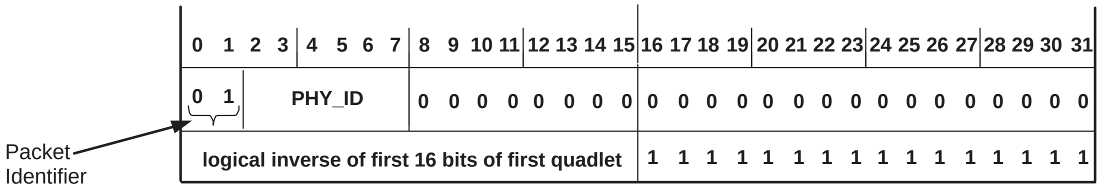


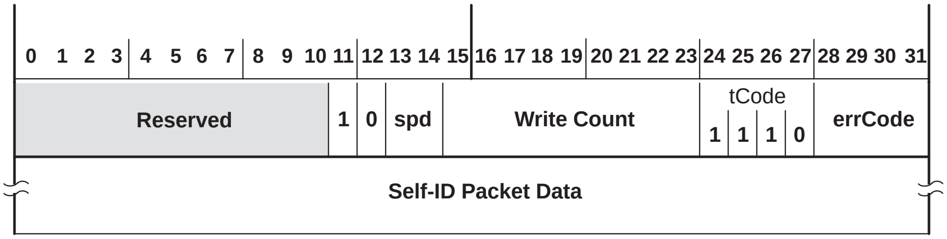
Figure 4−22. Link-On Packet Format

Table 4−11. Link-On Packet Functions

FIELD NAME	DESCRIPTION
01	The 01 field is the link-on packet identifier.
PHY_ID	This field is the physical_ID of the node this packet is addressed to.

4.10 Receive Self-ID

The format of the receive self-ID packet is shown in Figure 4−23 and described in Table 4−12. The first quadlet is the packet token with the special code of Eh. The quadlets that follow are a concatenation of all received self-ID packets. See paragraph 4.3.4.1 of the IEEE 1394−1995 standard for additional information about self-ID packets.



NOTES: A. Bit 11 (PacCom) = 1
B. Speed should be S100 (spd=00).

Figure 4−23. Receive Self-ID Packet Format(RxSID bit = 1)

Table 4−12. Received Self-ID Packet Functions

FIELD NAME	DESCRIPTION
spd	The spd field indicates the speed at which the current packet is to be sent (00 = S100, 01 = S200, 10 = S400, and 11 is undefined).
WriteCount	WriteCount indicates the number of data quadlets in the packet.
errCode	The errCode field indicates whether the current packet has been received correctly. The possibilities are Complete, DataErr, or CRCErr and have the same encoding as the corresponding acknowledge codes (see Table 6−13 of the IEEE 1394−1995 standard).
Self-ID packet data	This field contains a concatenation of all the self-ID packets received (see self-ID packet description below).

The cable PHY sends one to three self-ID packets at the base rate (100 Mbits/s) during the self-ID phase of arbitration or in response to a ping packet. The number of self-ID packets sent depends on the number of PHY ports. Figure 4−24, Figure 4−25, and Figure 4−26 show the format of the cable PHY self-ID packets. Table 4−13 describes the details of these packets.

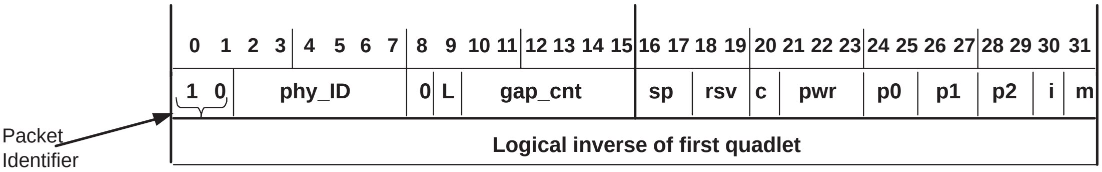


Figure 4−24. PHY Self-ID Packet #0 Format

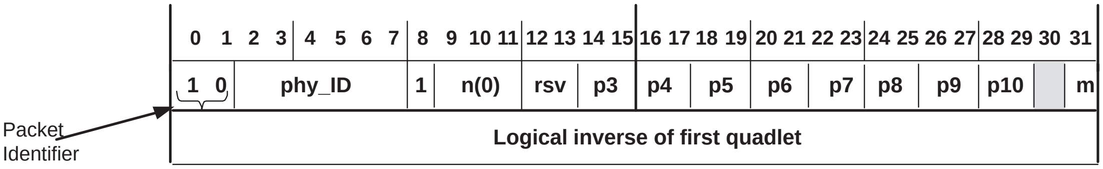


Figure 4−25. PHY Self-ID Packet #1 Format

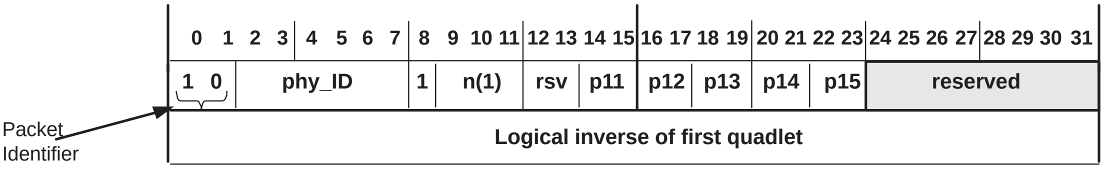


Figure 4−26. PHY Self-ID Packet #2 Format

Table 4−13. PHY Self-ID Packet Fields

FIELD NAME	DESCRIPTION
10	The 10 field is the self-ID packet identifier.
phy_ID	The phy_ID field contains the physical identification of the node transmitting the self-ID packet.
L	If set, this node has an active link and transaction layers. In discrete PHY implementations, this shall be the logical AND of Link_active and LPS active.
gap_cnt	The gap_cnt field contains the current value for the current node PHY_CONFIGURATION.gap_count field.
sp	The sp field contains the PHY speed capability. The code is:
	00 98.304 Mbits/s
	01 98.304 Mbits/s and 196.608 Mbits/s
	10 98.304 Mbits/s 196.608 Mbits/s, and 393.216 Mbits/s
	11 Extended speed capabilities reported in PHY register 3
c	If set and the link_active flag is set, this node is contender for the bus or isochronous resource manager as described in clause 8.4.2 of IEEE Std 1394−1995.
pwr	Power consumption and source characteristics: 000 Node does not need power and does not repeat power.
	001 Node is self-powered and provides a minimum of 15 W to the bus.
	010 Node is self-powered and provides a minimum of 30 W to the bus.
	011 Node is self-powered and provides a minimum of 45 W to the bus.
	100 Node may be powered from the bus and is using up to 3 W. No additional power is needed to enable the link[‡].
	101 Reserved for future standardization.
	110 Node is powered from the bus and is using up to 3 W. An additional 3 W is needed to enable the link[‡].
	111 Node is powered from the bus and is using up to 3 W. An additional 7 W is needed to enable the link[‡].
p0 – p15	The p0–p15 field indicates the port connection status. The code is: 00 Not present on the current PHY
	01 Not connected to any other PHY
	10 Connected to the parent node
	11 Connected to the child node
i	If set, this node initiated the current bus reset (i.e., it started sending a bus_reset signal before it received one).[†]

FIELD NAME	DESCRIPTION
m	If set, another self-ID packet for this node immediately follows (i.e., if this bit is set and the next self-ID packet received has a different phy_ID, then a self-ID packet was lost).
n	Extended self-ID packet sequence number
rsv	Reserved and set to all zeros.

† The link is enabled by the link-on PHY packet described in clause 7.5.2 of the IEEE 1394.a spec.; this packet may also enable application layers.
‡ There is no assurance that exactly one node will have this bit set. More than one node may request a bus reset at the same time.

4.11 Received PHY Configuration and Link-On Packet

The format of the received PHY-configuration and link-on packet is similar to the received self-ID packet. In this case, the value of the errCode is 0000. Only the first quadlet of each packet is stored in the GRF. If the received second quadlet of each packet is not the inverse of the first one, the packet is ignored. See paragraph 4.3.4.2 of the IEEE 1394−1995 standard for additional information on link-on packets and paragraph 4.3.4.3 for additional information on PHY-configuration packets.

5 Electrical Characteristics

5.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, V_{CC}	−0.5 V to 3.6 V
Input voltage range, V_I (standard TTL/LVCMOS)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, (standard TTL/LVCMOS) V_O	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (TTL/LVCMOS) ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} (TTL/LVCMOS) ($V_O < 0$ or $V_O > V_{CC}$) (see Note 2)	±20 mA
Continuous total power dissipation	See Maximum Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Industrial temperature, T_A	−40°C to 85°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This applies to external input and bidirectional buffers.
2. This applies to external output and bidirectional buffers.

MAXIMUM DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
PZT	1500 mW	16.9 mW/°C	739.5 mW

PACKAGE THERMAL RESISTANCE (R_θ) CHARACTERISTICS†

PARAMETER		TEST CONDITIONS	PZT PACKAGE			UNIT
			MIN	NOM	MAX	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Board mounted, No air flow		59		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			13		°C/W
T_J	Junction temperature				115	°C

† Thermal resistance characteristics very depending on die and leadframe pad size as well as mold compound. These values represent typical die and pad sizes for the respective packages. The R value decreases as the die or pad sizes increases. Thermal values represent PWB bands with minimal amounts of metal.

5.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	
Transition time, (t_t) (10% to 90%)	0		6	ns
Operating free-air temperature, T_A	0	25	70	°C
Virtual junction temperature, T_J†	0	25	115	°C

† The junction temperatures listed reflect simulation conditions. The absolute maximum junction temperature is 150°C. The customer is responsible for verifying the junction temperature.

5.3 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -8$ mA[†]		$V_{CC} - 0.6$			V
		$I_{OH} = -4$ mA[‡]		$V_{CC} - 0.6$			
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA[†]				0.5	V
		$I_{OL} = 4$ mA[‡]				0.5	
I_{IL}	Low-level input current[§]	V_I = GND	TTL/LVCMOS			−1	µA
			D0−D7, CTL0, CTL1			−20	
I_{IH}	High-level input current	$V_I = V_{CC}$	TTL/LVCMOS			1	µA
			D0−D7, CTL0, CTL1			20	
I_{OZ}	High-impedance-state output current[¶]	$V_O = V_{CC}$ or GND				±20	µA
$I_{CC(Q)}$	Static supply current	$I_O = 0$			88		µA
$I_{CC(Dynamic)}$	Dynamic supply current				120		mA

[†] This test condition is for terminals D0 − D7, CTL0, CTL1, LREQ, and POWERON

[‡] This test condition is for terminals DATA0 − DATA31, $\overline{\text{CA}}$, $\overline{\text{INT}}$, CYCLEOUT, GRFEMP, CYDNE, and CYST.

[§] This specification only applies when pullup and pulldown terminator is turned off.

[¶] Three-state output must be in high-impedance mode.

5.4 Host-Interface Timing Requirements, $T_A = 25°C$ (see Note 3)

PARAMETER		MIN	MAX	UNIT
t_{c1}	Cycle time, BCLK (see Figure 6−1)	14		ns
$t_{w1(H)}$	Pulse duration, BCLK high (see Figure 6−1)	3		ns
$t_{w1(L)}$	Pulse duration, BCLK low (see Figure 6−1)	3		ns
t_{su1}	Setup time, DATA0 − DATA31 valid before BCLK↑ (see Figure 6−2, Figure 6−4, Figure 6−6)	2.5		ns
t_{h1}	Hold time, DATA0 − DATA31 valid after BCLK↑ (see Figure 6−2, Figure 6−4, Figure 6−6)	1		ns
t_{su2}	Setup time, ADDR0−ADDR7 valid before BCLK↑ (see Figure 6−2, Figure 6−3, Figure 6−4)	7		ns
t_{h2}	Hold time, ADDR0 − ADDR7 valid after BCLK↑ (see Figure 6−2, Figure 6−3, Figure 6−4)	1		ns
t_{su3}	Setup time, $\overline{\text{CS}}$ low before BCLK↑ (see Figure 6−2, Figure 6−3, Figure 6−4)	7.5		ns
t_{h3}	Hold time, $\overline{\text{CS}}$ low after BCLK↑ (see Figures 6−2, Figure 6−3, Figure 6−4)	0.5		ns
t_{su4}	Setup time, $\overline{\text{WR}}$ valid before BCLK↑ (see Figure 6−2, Figure 6−3, Figure 6−4)	7		ns
t_{h4}	Hold time, $\overline{\text{WR}}$ valid after BCLK↑ (see Figure 6−2, Figure 6−3, Figure 6−4)	0.5		ns

NOTE 3: These parameters are not production tested.

5.5 Host-Interface Switching Characteristics Over Recommended Operating Free-Air Temperature Range, $C_L = 45$ pF (Unless Otherwise Noted)

PARAMETER		MIN	MAX	UNIT
t_{d1}	Delay time, BCLK↑ to $\overline{\text{CA}}$↓ (see Figure 6−2, Figure 6−3, Figure 6−5, Figure 6−6, and Figure 6−7)	3	8	ns
t_{d2}	Delay time, BCLK↑ to $\overline{\text{CA}}$↑ (see Figure 6−2, Figure 6−3, Figure 6−5, Figure 6−6, and Figure 6−7)	3	8	ns
t_{d3}	Delay time, BCLK↑ to DATA0 − DATA31 valid (see Figure 6−3, Figure 6−5, Figure 6−7, and Note 3)		8.5	ns
t_{d4}	Delay time, BCLK↑ to DATA0 − DATA31 invalid (see Figure 6−3, Figure 6−5, Figure 6−7, and Note 3)	2		ns

NOTE 3: These parameters are not production tested.

5.6 Cable PHY-Layer-Interface Timing Requirements Over Recommended Operating Free-Air Temperature Range (see Note 3)

PARAMETER		MIN	MAX	UNIT
t_{c2}	Cycle time, SCLK (see Figure 6−8)	20		ns
$t_{w2(H)}$	Pulse duration, SCLK high (see Figure 6−8)	4		ns
$t_{w2(L)}$	Pulse duration, SCLK low (see Figure 6−8)	4		ns
t_{su5}	Setup time, D0 − D7 valid before SCLK↑ (see Figure 6−10)	2.5		ns
t_{h5}	Hold time, D0 − D7 valid after SCLK↑ (see Figure 6−10)	0		ns
t_{su6}	Setup time, CTL0 − CTL1 valid before SCLK↑ (see Figure 6−10)	2.5		ns
t_{h6}	Hold time, CTL0 − CTL1 valid after SCLK↑ (see Figure 6−10)	0		ns

NOTE 3: These parameters are not production tested.

5.7 Cable PHY-Layer-Interface Switching Characteristics Over Recommended Operating Free-Air Temperature Range, C_L = 45 pF (Unless Otherwise Noted) (see Note 3)

PARAMETER		MIN	MAX	UNIT
t_{d5}	Delay time, SCLK↑ to D0 − D7 valid (see Figure 6−9)		10	ns
t_{d6}	Delay time, SCLK↑ to D0 − D7 invalid (see Figure 6−9)	2.5		ns
t_{d7}	Delay time, SCLK↑ to D0 − D7 invalid (see Figure 6−9)	2.5		ns
t_{d8}	Delay time, SCLK↑ to CTL0 − CTL1 valid (see Figure 6−9)		9	ns
t_{d9}	Delay time, SCLK↑ to CTL0 − CTL1 invalid (see Figure 6−9)	2.5		ns
t_{d10}	Delay time, SCLK↑ to CTL0 − CTL1 invalid (see Figure 6−9)	2.5		ns
t_{d11}	Delay time, SCLK↑ to LREQ↓ (see Figure 6−11)	3.5	9	ns

NOTE 3: These parameters are not production tested.

5.8 Miscellaneous Timing Requirements Over Recommended Operating Free-Air Temperature Range (see Figure 6−13 and Note 3)

PARAMETER		MIN	MAX	UNIT
t_{c3}	Cycle time, CYCLEIN (see Figure 6−13)	124.99	125.01	µs
$t_{w3(H)}$	Pulse duration, CYCLEIN high (see Figure 6−13)	62		µs
$t_{w3(L)}$	Pulse duration, CYCLEIN low (see Figure 6−13)	62		µs

NOTE 3: These parameters are not production tested.

5.9 Miscellaneous Signal Switching Characteristics Over Recommended Operating Free-Air Temperature Range (see Note 3)

PARAMETER		MIN	MAX	UNIT
t_{d12}	Delay time, SCLK↑ to $\overline{\text{INT}}$↓ (see Figure 6−12)		10.5	ns
t_{d13}	Delay time, SCLK↑ to $\overline{\text{INT}}$↑ (see Figure 6−12)		10.5	ns
t_{d14}	Delay time, SCLK↑ to CYCLEOUT↑ (see Figure 6−14)	3.5	10	ns
t_{d15}	Delay time, SCLK↑ to CYCLEOUT↓ (see Figure 6−14)	3.5	10	ns

NOTE 3: These parameters are not production tested.

6 Parameter Measurement Information

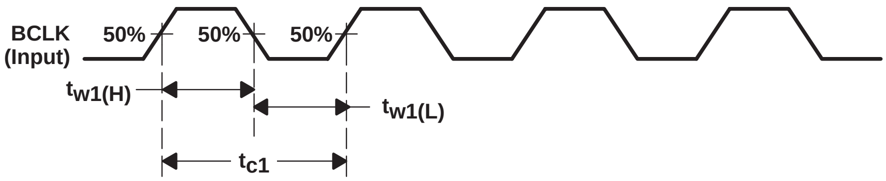
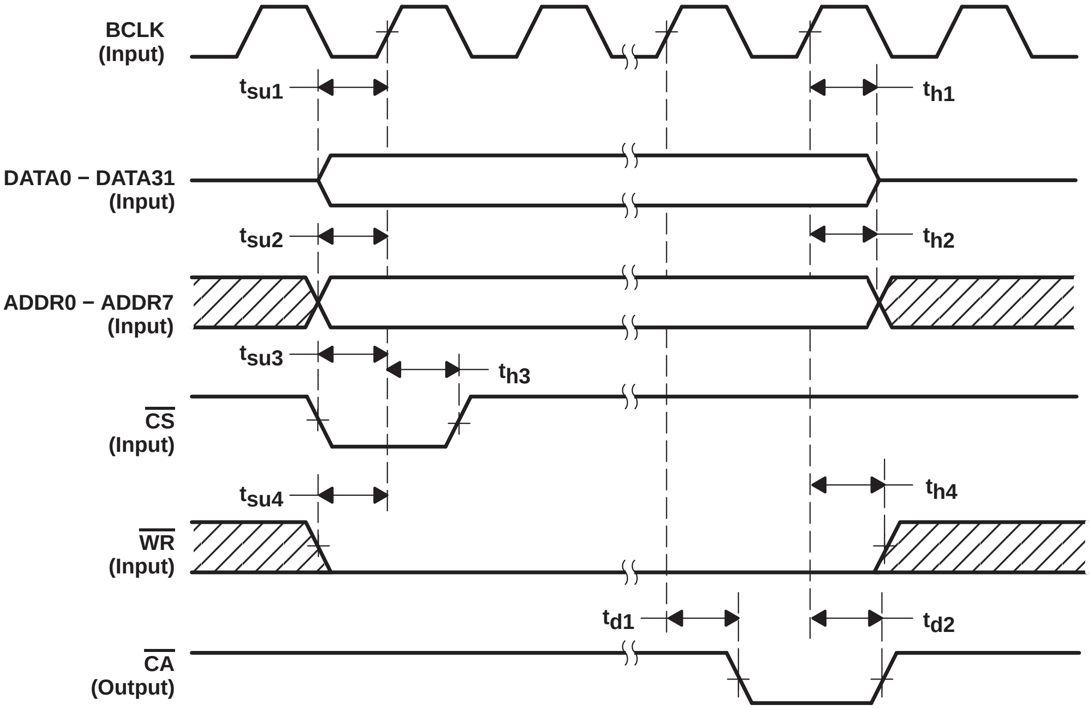
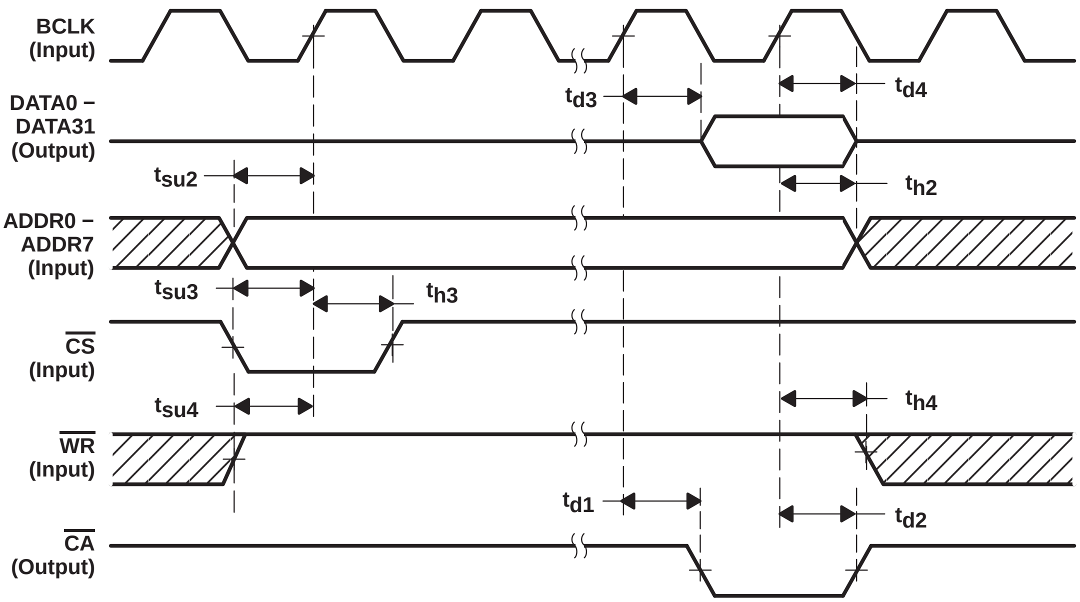


Figure 6−1. BCLK Waveform



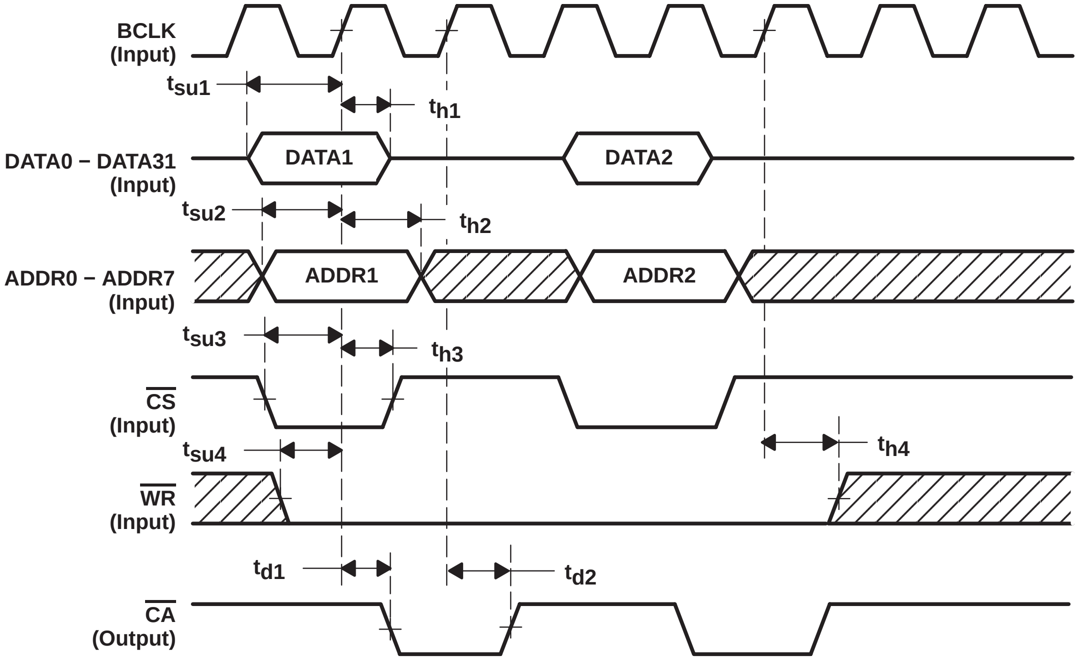
NOTE A: Following a $\overline{CS}$ assertion, there may be a maximum of nine rising edges of BCLK before a $\overline{CA}$ is returned. $\overline{CA}$ must be returned before another $\overline{CS}$ may be asserted.

Figure 6−2. Host-Interface Write-Cycle Waveforms (Address: 00h − 2Ch)



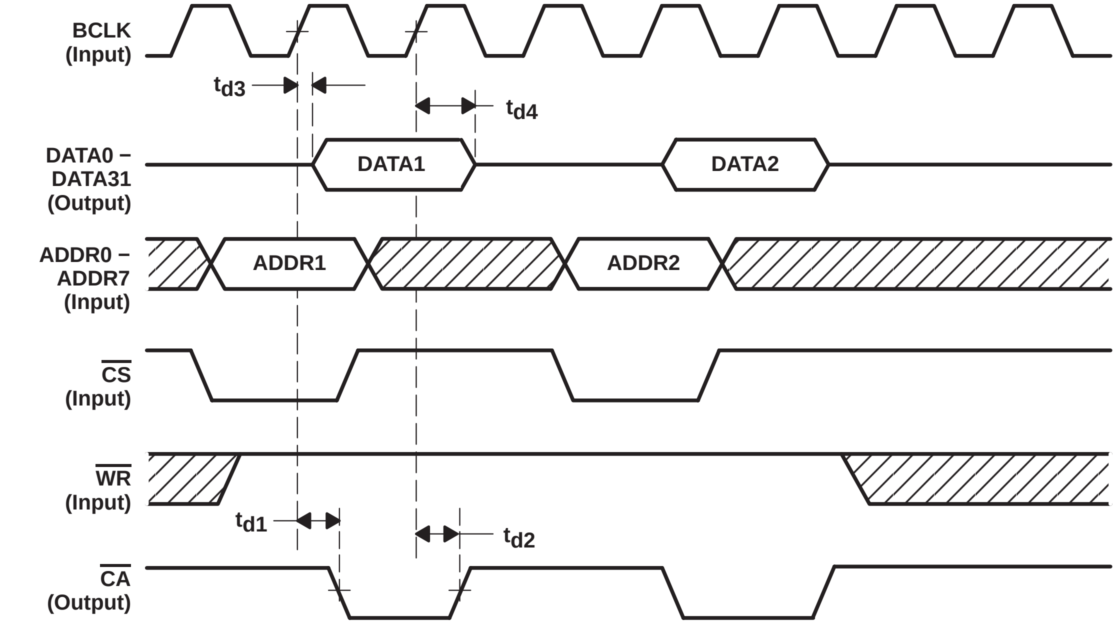
NOTE A: Following a $\overline{CS}$ assertion, there may be a maximum of nine rising edges of BCLK before a $\overline{CA}$ is returned. $\overline{CA}$ must be returned before another $\overline{CS}$ may be asserted.

Figure 6−3. Host-Interface Read-Cycle Waveforms (Address: 00h − 2Ch)



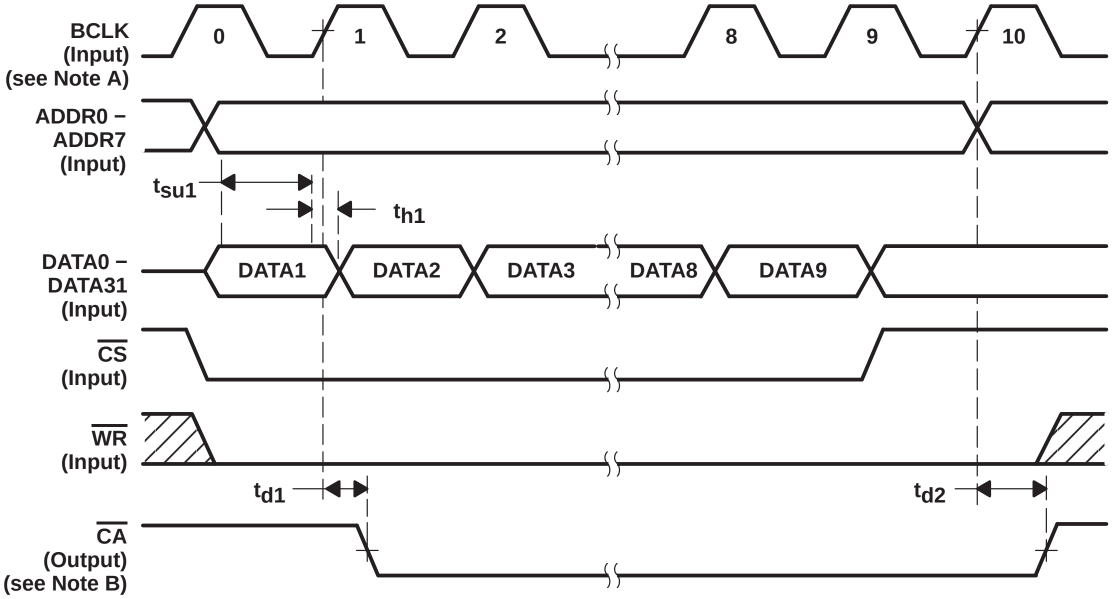
NOTE A: There must be a minimum of three rising edges of BCLK between assertions of $\overline{CS}$.

Figure 6−4. Host-Interface Quick Write-Cycle Waveforms (Address ≥ 30h)



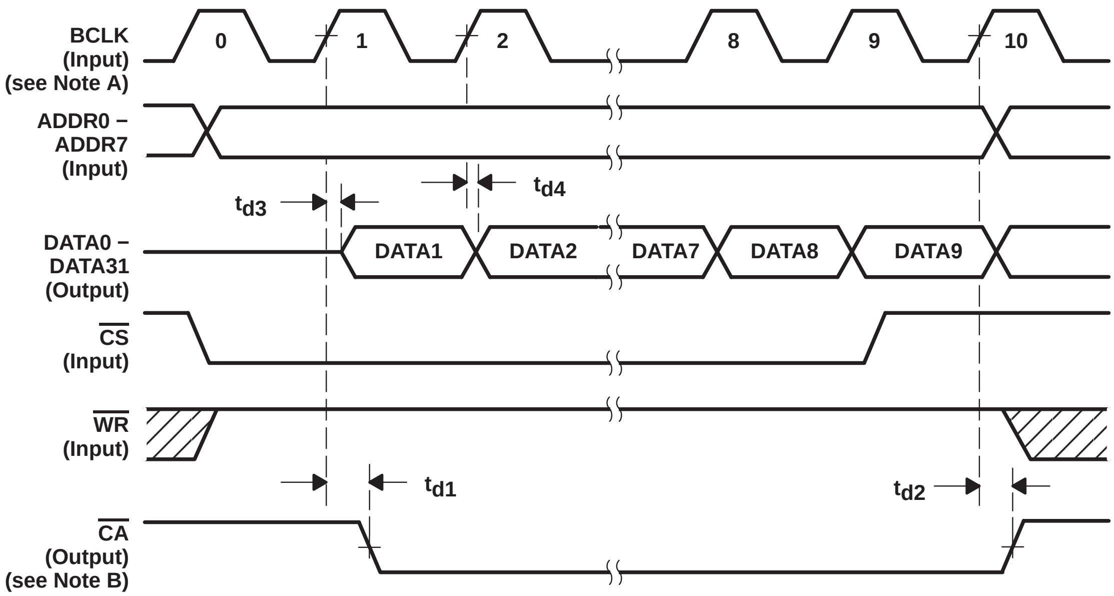
NOTE A: There must be a minimum of three rising edges of BCLK between assertions of $\overline{\text{CS}}$.

Figure 6−5. Host-Interface Quick Read-Cycle Waveforms (ADDRESS ≥ 30h)



NOTES: A. At the nth BCLK rising edge, DATAn is written into the FIFO.
B. $\overline{\text{CA}}$ is one cycle delay from respective $\overline{\text{CS}}$.

Figure 6−6. Burst Write Waveforms



NOTES: A. At the (nth+1) BCLK rising edge, the host bus should latch DATAn.
B. CA is one cycle delay from respective CS.
C. These waveforms only apply to address C0h.

Figure 6−7. Burst Read Waveforms

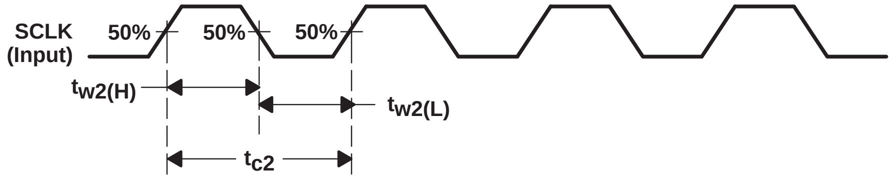


Figure 6−8. SCLK Waveform

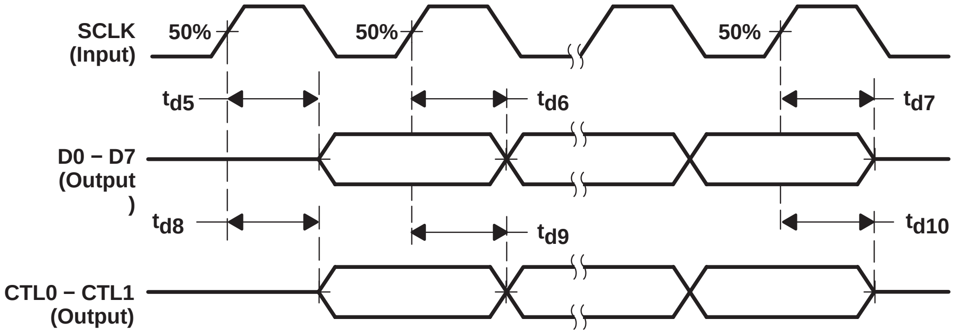


Figure 6−9. TSB42AC3-to-PHY Layer Interface Transfer Waveforms

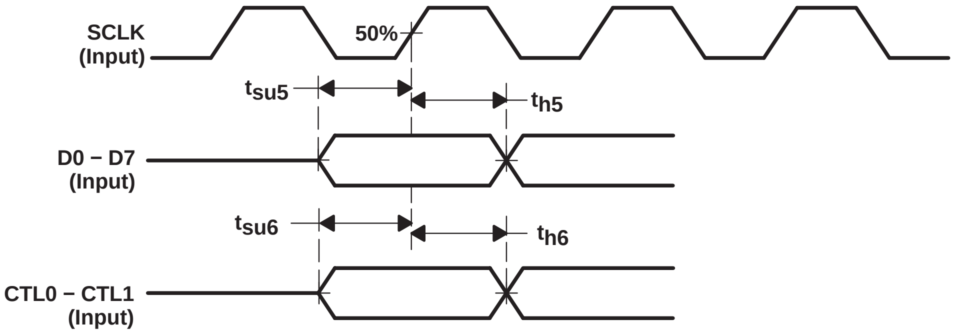


Figure 6−10. PHY Layer Interface-to-TSB42AC3 Transfer Waveforms

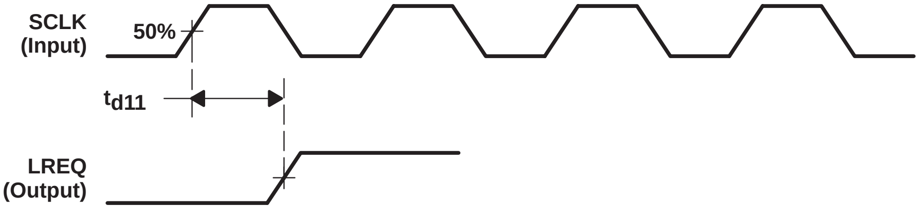


Figure 6−11. TSB42AC3 Link-Request-to-PHY-Layer Interface Waveforms

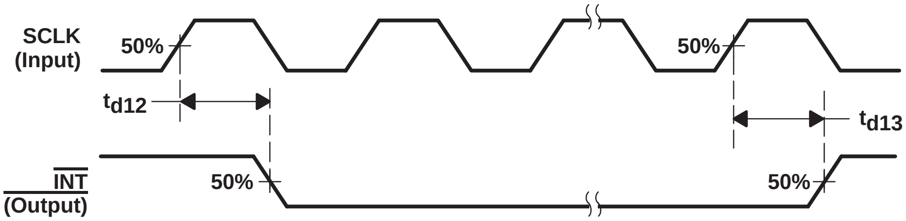


Figure 6−12. Interrupt Waveform

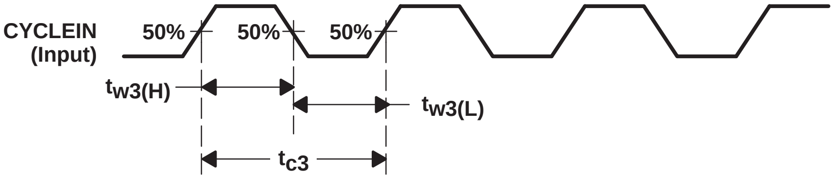


Figure 6−13. CYCLEIN Waveform

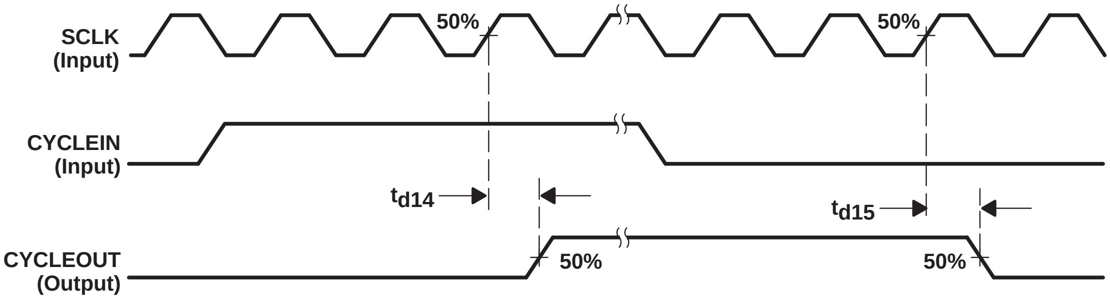


Figure 6−14. CYCLEIN and CYCLEOUT Waveforms

7 Principles of Operation

7.1 PHY/LLC Interface Operation

The TSB42AC3 is designed to operate with a physical-layer controller (PHY) such as the Texas Instruments TSB21LV03C, TSB41AB1, TSB41AB2, TSB41AB3, TSB41LV04A, TSB41LV06A (cable PHY), and TSB14AA1A (backplane PHY). The interface to the PHY consists of the SCLK, CTL0−CTL1, D0−D7, LREQ, and POWERON terminals on the TSB42AC3, as shown in Figure 7−1.

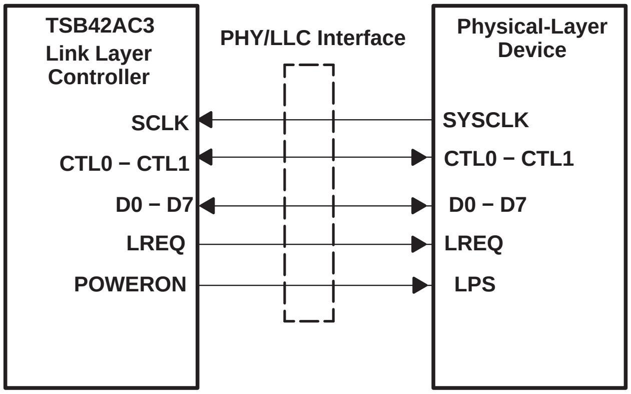


Figure 7−1. PHY-LLC Interface

The SYSCLK from the PHY terminal provides either a 49.152-MHz interface clock for S400, S200, and S100 data transfers or a 24.576-MHz interface clock for S50 data transfer. All control and data signals are synchronized to and sampled on the rising edge of SYSCLK.

The CTL0 and CTL1 terminals form a bidirectional control bus, which controls the flow of information and data between the PHY and TSB42AC3.

The D0−D7 terminals form a bidirectional data bus, which is used to transfer status information, control information, or packet data between the PHY and TSB42AC3. In S50 and S100 operation, only the D0 and D1 terminals are used; in S200 operation, only the D0−D3 terminals are used; and in S400 operation, all D0−D7 terminals are used for data transfer. During S200, S100, and S50 operations, unused Dn terminals need to be pull down on the PHY side and pull high on the LLC side.

The LREQ terminal is controlled by the TSB42AC3 to send serial service requests to the PHY in order to request access to the serial bus for packet transmission, to read or written PHY registers, or control arbitration acceleration.

The POWERON and LPS terminals are used for power management of the PHY and TSB42AC3. The POWERON terminal indicates the power status of the TSB42AC3 and may be used to reset the PHY−LLC interface or to disable the SCLK.

The PHY normally controls the CTL0−CTL1 and D0−D7 bidirectional buses. The LLC is allowed to drive these buses only after the LLC has been granted permission to do so by the PHY. There are four operations that may occur on the PHY-LLC interface: link service request, status transfer, data transmit, and data receive. The TSB42AC3 issues a service request to read or write a PHY register, to request the PHY to gain control of the serial bus in order to transmit a packet, or to control arbitration acceleration.

The PHY may initiate a status transfer either autonomously or in response to a register read request from the LLC. The PHY initiates a data receive operation whenever a packet is received from the serial bus. The PHY initiates a data transmit operation after winning control of the serial bus following a bus request by the LLC.

The encoding of the CTL0−CTL1 bus is shown in Table 7−1 and Table 7−2.

Table 7−1. CTL Encoding When PHY Has Control of the Bus

CTL0	CTL1	NAME	DESCRIPTION OF ACTIVITY
0	0	Idle	No activity (this is the default mode).
0	1	Status	Status information is being sent from the PHY to the LLC
1	0	Receive	An incoming packet is being sent from the PHY to the LLC
1	1	Grant	The LLC has been given control of the bus to send an outgoing packet.

Table 7−2. CTL Encoding When LLC Has Control of the Bus

CTL0	CTL1	NAME	DESCRIPTION OF ACTIVITY
0	0	Idle	The LLC releases the bus (transmission has been completed)
0	1	Hold	The LLC is holding the bus while data is being prepared for transmission or indicating that another packet is to be transmitted (concatenated) without arbitrating.
1	0	Transmit	An outgoing packet is being sent from the LLC to the PHY
1	1	Reserved	Reserved

7.2 TSB42AC3 Service Request

When the LLC needs to request the bus or access a register that is located in the PHY, a serial stream of information is sent across the LREQ line as shown in Figure 7−2. Each cell represents one clock sample time.

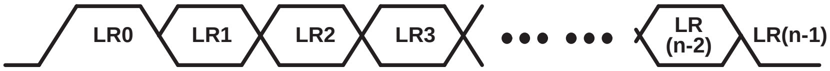


Figure 7−2. LREQ Timing

The length of the stream varies depending on whether the transfer is a bus request, a read command, or a write command as shown in Table 7−3. Regardless of the type of transfer, a start bit of 1 is required at the beginning of the stream and a stop bit of 0 is required at the end of the stream. Bit 0 is the MSB and is transmitted first. The LREQ terminal is normally low.

Table 7−3. Request Bit Length

REQUEST TYPE	NUMBER OF BITS
Bus request (cable)	7
Bus request (backplane)	11
Read register request	9
Write register request	17
Acceleration control request (cable)	6

Encoding for the request type is shown in Table 7−4.

Table 7−4. Request Type Encoding

LR1−LR3	NAME	DESCRIPTION
000	ImmReq	Immediate bus request. Upon detection of idle, the PHY takes control of the bus immediately without arbitration.
001	IsoReq (cable)	Isochronous bus request. Upon detection of idle, the PHY arbitrates for the bus without waiting for a subaction gap.
010	PriReq (cable)	Priority bus request. The PHY arbitrates for the bus after a subaction gap and ignores the fair protocol.
011	Fair/Urgent Req	Fair or urgent bus request. The PHY arbitrates after a subaction gap using fair protocol. Fair/Urgent Req is used for fair transfers with the request priority field differentiating fair and urgent transfers for the backplane environment.
100	RdReq	Read register request. The PHY returns the specified register contents through a status transfer.
101	WrReq	Write register request. Write to the specified register.
110	AccelCtl (cable)	Acceleration control request. Enable or disable asynchronous arbitration acceleration.
111	Reserved	Reserved

For a bus request in the cable environment, the length of the LREQ data stream is 7 or 8 bits as shown in Table 7−5.

Table 7−5. Bus Request for Cable Environment

BIT(S)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1−3	Request type	Indicates the type of bus request (see Table 7−4 for the encoding of this field)
4−6	Request speed	Indicates the speed at which the PHY sends the packet for this request. This field has the same encoding as the speed code from the first symbol of the receive packet. See Table 7−6 for the encoding of this field. This field can be expanded to support data higher than 400 Mbit/s in the future.
7	Stop bit	Indicates the end of the transfer (always 0).

The 3-bit request speed field used in bus request is shown in Table 7−6.

Table 7−6. Bus Request Speed Encoding

LR4−LR6	DATA RATE
000	S100
010	S200
100	S400
All Others	Invalid

NOTE:

The cable PHY accepts a bus request with an invalid speed code and process the bus request normally. However, during packet transmission for such a request, the PHY ignores any data presented by the TSB42AC3 and transmits a null packet.

The backplane PHY accepts an LREQ transfer bus request in the backplane format. This request is 11 bits long and has the format shown in Table 7−7. This is an optional feature of the backplane environment; it allows the priority of a packet to be changed on a packet by packet basis. When using normal cable LREQs that are 7 bits long, the packet will have the priority contained in the priority register of the backplane PHY. For this case to change the priority, requires software to change the value of the priority register inside the backplane PHY.

Table 7−7. Bus Request for Backplane Environment

BIT(S)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1−3	Request type	Indicates the type of bus request (see Table 7−4 for the encoding of this field)
4−5	Request speed	Ignored (set to 00 for cable S100) for backplane environment
6−9	Request priority	Indicates the priority of urgent requests. It is only used with a FairReq request type. All zeros indicate a fair request. All ones are reserved (this priority is implied by a PriReq). Other values are used to indicate the priority of an urgent request.
10	Stop bit	Indicates the end of the transfer (always 0)

For a read register request, the length of the LREQ bit stream is 9 bits as shown in Table 7−8.

Table 7−8. Read Register Request

BIT(S)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1−3	Request type	Always *100* indicating this is a read register request
4−7	Address	The address of the PHY register to be read.
8	Stop bit	Indicates the end of the transfer (always 0)

For a write register request, the length of the LREQ bit stream is 17 bits as shown in Table 7−9.

Table 7−9. Write Register Request

BIT(S)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1−3	Request type	Always *101* indicating this is a write register request
4−7	Address	The address of the PHY register to be written to
8−15	Data	The data that is to be written to the specified register address
16	Stop bit	Indicates the end of the transfer (always 0)

For an acceleration control request (cable only), the length of the LREQ bit stream is 6 bits as shown in Table 7−10.

Table 7−10. Acceleration Control Request (Cable Only)

BIT(S)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1−3	Request type	Always *110* indicating this is an acceleration control request
4	Control	Asynchronous period arbitration acceleration is enabled if 1 and disabled if 0
5	Stop bit	Indicates the end of the transfer (always 0)

For fair or priority access, the TSB42AC3 sends the bus request (Fair/Urgent Req or PriReq) at least one clock cycle after the PHY-LLC interface becomes idle. When the link senses that the CTL terminals are in a receive state (‘b10), then it knows that its request has been lost (cleared). This is true anytime during or after a bus request transfer by the link. Additionally, the PHY ignores any fair/urgent or priority request if it asserts the receive state, while the link is requesting the bus. When the link finds the CTL terminals in a receive state, the link reissues the bus request transfer one clock cycle after the next interface idle.

For cable PHY, the cycle master node uses a priority bus request (PriReq) to send a cycle start message. After receiving or transmitting a cycle start message, the TSB42AC3 can issue an isochronous bus request (IsoReq). The cable PHY clears an isochronous request only when the serial bus has been won.

To send an acknowledge packet, the link must issue an immediate bus request (ImmReq) during the reception of the packet addressed to it. This is required because the delay from end-of-packet to acknowledge requests adds directly to the minimum delay every PHY must wait after every packet to allow an acknowledge to occur. After the packet ends, the PHY immediately takes control of the bus and grants the bus to the link. If the header cyclic redundancy check (CRC) of the packet is corrupted, the link releases the bus immediately. The link cannot use this grant to send another type of packet. To ensure this, the link must wait 160 ns after the end of the received packet to allow the PHY to grant it the bus for the acknowledgement and then the link releases the bus and proceeds with another request.

Although improbable, it is conceivable that two separate nodes can believe that an incoming packet is intended for them. The nodes then issue an ImmReq request before checking the CRC of the packet. Since both PHYs seize control of the bus at the same time, a temporary, localized collision of the bus occurs. As soon as the two nodes check the CRC, the mistaken node drops its request and the false line is removed. The only side effect is the loss of the intended acknowledgement packet (that is handled by the higher-layer protocol).

For write register requests, the PHY loads the specified data into the addressed register as soon as the request transfer is complete. For read register requests, the PHY returns the contents of the addressed register to the TSB42AC3 at the next opportunity through a status transfer. When the status transfer is interrupted by an incoming packet, the PHY continues to attempt the transfer of the requested register until it is successful. A write or read register request may be made at any time, including while a bus request is pending. Once a read register request is made, the PHY ignores further read register requests until the register contents are successfully transferred to the link. A bus reset does not clear a pending read request.

The cable PHY includes several arbitration acceleration enhancements, which allow the PHY to improve bus performance and throughput by reducing the number and length of inter-packet gaps. These enhancements include autonomous (fly-by) isochronous packet concatenation, autonomous fair and priority packet concatenation onto acknowledge packets, and accelerated fair and priority request arbitration following acknowledge packets. The enhancements are enabled when the EAA bit in the cable PHY register 5 is set.

The arbitration acceleration enhancements may interfere with the ability of the cycle master node to transmit the cycle start message under certain circumstances. The acceleration control request is therefore provided to allow the TSB42AC3 to temporarily enable or disable the arbitration acceleration enhancements of the cable PHY during the asynchronous period. The link typically disables the enhancements when its internal cycle counter rolls over indicating that a cycle start message is imminent, and then reenables the enhancements when it receives a cycle start message. The acceleration control request may be made at any time and is immediately serviced by the cable PHY. Additionally, a bus reset or isochronous bus request causes the enhancements to be re-enabled if the EAA bit is set.

7.3 Status Transfer

When the PHY has status information to transfer to the link, it initiates a status transfer. The PHY waits until the interface is idle to perform the transfer. The PHY initiates the transfer by asserting status (‘b01) on the CTL terminals, along with the first two bits of status information on D0 and D1. The PHY maintains CTL status for the duration of the status transfer. The PHY can temporarily halt a status transfer by asserting something other than status on the CTL terminals. This is done in the event that a packet arrives before the status transfer completes. There must be at least one idle cycle between consecutive status transfers.

The PHY normally sends only the first 4 bits of status to the link. These bits are status flags that are needed by link state machines. The PHY sends an entire 16-bit status packet to the link after a read register request or when the PHY has pertinent information to send to the link or transition layers. The only defined condition where the PHY automatically sends a register to the link is after self-ID, where the PHY sends the physical-ID register that contains the new node address. All status transfers are either 4 or 16 bits, unless interrupted by a received packet. The status flags are considered to have been successfully transmitted to the link immediately upon being sent, even if a received packet subsequently interrupts the status transfer. Register contents are considered to have been successfully transmitted only when all 8 bits of the register have been sent. A status transfer is retried after being interrupted only if any status flags remain to be sent or if a register transfer has not yet completed.

The definitions of the bits in the status transfer are shown in Table 7−11 and the timing is shown in Figure 7−3.

Table 7−11. Status Bit Description

BIT(S)	NAME	DESCRIPTION
0	Arbitration reset gap	Indicates that the PHY has deselected that the bus has been idle for an arbitration reset gap time (as defined in IEEE Std 1394−1995). This bit is used by the link in its busy/retry state machine.
1	Subaction gap	Indicates that the PHY has detected that the bus has been idle for a subaction gap time (as defined in IEEE Std 1394−1995). This bit is also used by the link to detect the completion of an isochronous cycle (cable).
2	Bus reset	Indicates that the PHY has entered the bus reset start state
3	Reserved	Reserved
4−7	Address	This field holds the address of the PHY register whose contents are being transferred to the link.
8−15	Data	This field holds the register contents.

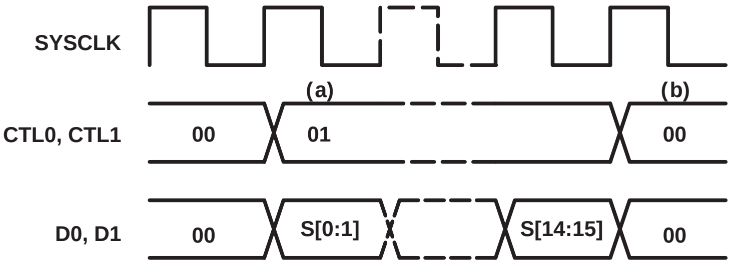


Figure 7−3. Status Transfer Timing

The sequence of events for a status transfer is as follows:

1. Status transfer initiated. The PHY indicates a status transfer by asserting status on the CTL lines along with status data on the DO and D1 lines (only 2 bits of status are transferred per cycle). Normally (unless interrupted by an incoming packet), a status transfer will be either two or eight cycles long. A 2-cycle (4 bit) transfer occurs when only status information is to be sent. An 8-cycle (16 bit) transfer occurs when register data is to be sent in addition to any status information.
2. Status transfer terminated. The PHY normally terminates a status transfer by asserting idle on the CTL lines. The PHY may also interrupt a status transfer at any cycle by asserting receive on the CTL lines to begin a receive operation. The PHY asserts at least one cycle of idle between consecutive status transfers.

7.4 Transmit Operation

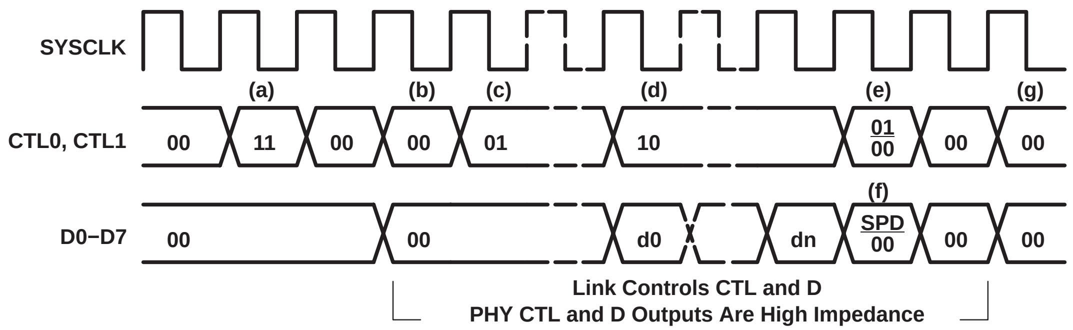
When the TSB42AC3 requests access to the serial bus through the LREQ terminal, the PHY arbitrates to gain control of the serial bus. If the PHY wins the arbitration, it grants the bus to the link by asserting the grant state (‘b11) on the CTL terminals for one SYSCLK cycle, followed by idle for one clock cycle. The TSB42AC3 then takes control of the bus by asserting either idle (‘b00), hold (‘b01), or transmit (b’10) on the CTL terminals. Unless the TSB42AC3 is immediately releasing the interface, the TSB42AC3 may assert the idle state for at most one clock cycle before it must assert either hold or transmit on the CTL terminals. The hold state is used by the link to retain control of the bus, while it prepares data for transmission. The link may assert hold for zero or more clock cycles (i.e., the link need not assert hold before transmit). The PHY asserts data-prefix on the serial bus during this time.

When the TSB42AC3 is ready to send data, the link asserts transmit on CTL terminals as well as sending the first bits of packet data on the D lines. The transmit state is held on the CTL terminals until the last bits of data has been sent. The link then asserts either hold or idle on the CTL terminals for one clock cycle and then asserts idle for one additional cycle before releasing the interface bus and placing its CTL and D terminals in high-impedance. The PHY then regains control of the interface bus.

The hold state asserted at the end of the packet transmission indicates to the PHY that the TSB42AC3 is requesting to send another packet (concatenated packet) without releasing the serial bus. The PHY responds to this concatenation request by waiting the required minimum packet separation time and then asserting grants as before. This function may be used to send a unified response after sending an acknowledge, or to send consecutive isochronous packet during a single isochronous period. Unless multi-speed concatenation is enabled, all packets transmitted during a single bus ownership must be of the same speed (since the speed of the packet is set before the first packet). If multi-speed concatenation is enabled (when the EMSc bit of cable PHY register 5 is set), the link must specify the speed code of the next concatenation packet on the D terminals when it asserts hold on the CTL terminals at the end of the packet. The encoding for this speed code is the same as the speed code that precedes received packet data as given in Figure 7−4.

As noted above, when the link has finished sending the last packet for the current bus ownership, it releases the bus by asserting idle on the CTL terminals for two clock cycles. The PHY begins asserting idle on the CTL terminals one clock cycle after sampling second idle from the link. Whenever the D and CTL terminals change ownership between the PHY and the link, there is an extra clock period allowed so that both sides of the interface can operate on registered versions of the interface signals, rather than having to respond CTL state on the next cycle.

The timing of a packet transmission is shown in Figure 7−4.



NOTE: SPD = Speed code, see Table 7−6. d0−dn = Packet data

Figure 7−4. Normal Packet Transmission Timing

The sequence of events for a normal packet transmission is as follows:

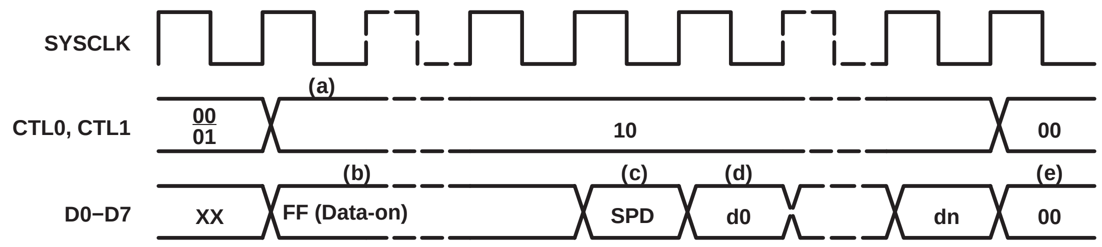
1. Transmit operation initiated. The PHY asserts grant on the CTL terminals followed by idle to hand over control of the interface to the link so that the link may transmit a packet. The PHY releases control of the interface (i.e., it places its CTL and D outputs in a high-impedance state) following the idle cycle.
2. Optional idle cycle. The link may assert, at most, one idle cycle preceding assertion of either hold or transmit. This idle cycle is optional; the link is not required to assert idle preceding either hold or transmit.
3. Optional hold cycles. The link may assert hold for up to 47 cycles preceding assertion of transmit. These hold cycle(s) are optional; the link is not required to assert hold preceding transmit.

7.5 Receive Operation

Whenever the PHY detects the data-prefix state on the serial bus, it initiates a receive operation by asserting receive on the CTL terminals and a logic 1 on each of the D terminals (data-on indication). The PHY indicates the start of a packet by placing the speed code (encoded as shown in Table 7−6) on the D terminals, followed by the packet data. The PHY holds the CTL terminals in the receive state until the last symbol of the packet has been transferred. The PHY indicates the end of packet data by asserting idle on the CTL terminals. All received packets are transferred to the TSB42AC3. Note that the speed code is part of the PHY-LLC protocol and is not included in the calculation of CRC or any other data protection mechanisms.

It is possible for the PHY to receive a null packet, which consists of the data-prefix state on the serial bus followed by the data-end state, without any packet data. A null packet is transmitted whenever the packet speed exceeds the capability of the receiving PHY or whenever the link releases the bus immediately without transmitting any data. In this case, the PHY asserts receive on the CTL terminals with the data-on indication (all 1’s) on the D terminals, followed by idle on the CTL terminals, without any speed code or data being transferred. In all cases, the PHY sends at least one data-on indication before sending the speed code or terminating the receive operation.

The cable PHY also transfers its own self-ID packet, transmitted during the self-ID phase of bus initialization, to the link. This packet is transferred to the link just as any other received self-ID packet.



NOTE: SPD = Speed code, see Table 7−6. d0−dn = Packet data

Figure 7−5. Normal Packet Reception Timing

The sequence of events for a normal packet reception is as follows:

1. Receive operation initiated. The PHY indicates a receive operation by asserting receive on the CTL lines. Normally, the interface is idle when receive is asserted. However, the receive operation may interrupt a status transfer operation that is in progress so that the CTL lines may change from status to receive without an intervening idle.
2. Data-on indication. The PHY asserts the data-on indication code on the D lines for one or more cycles preceding the speed-code.
3. Speed-code. The PHY indicates the speed of the received packet by asserting a speed-code on the D lines for one cycle immediately preceding the packet data. The link decodes the speed-code on the first receive cycle for which the D lines are not the data-on code. If the speed-code is invalid or indicates a speed higher than which the link is capable of handling, the link should ignore the subsequent data.
4. Receive data. Following the data-on indication (if any) and the speed-code, the PHY asserts packet data on the D lines with receive on the CTL lines for the remainder of the receive operation.
5. Receive operation terminated. The PHY terminated the receive operation by asserting idle on the CTL lines. The PHY asserts at least one cycle of idle following a receive operation.

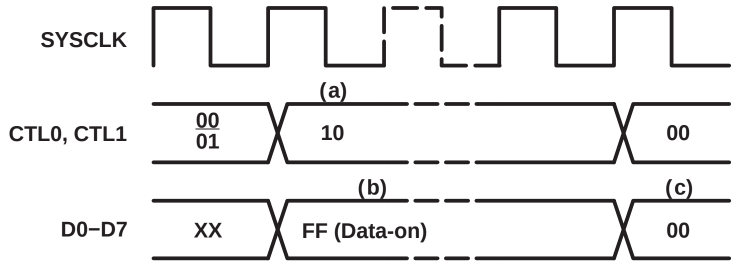


Figure 7−6. Null Packet Reception Timing

The sequence of events for a null packet reception is as follows:

1. Receive operation initiated. The PHY indicates a receive operation by asserting receive on the CTL lines. Normally, the interface is idle when receive is asserted. However, the receive operation may interrupt a status transfer operation that is in progress so that the CTL lines may change from status to receive without an intervening idle.
2. Data-on indication. The PHY asserts the data-on indication code on the D lines for one or more cycles.
3. Receive operation terminated. The PHY terminates the receive operation by asserting idle on the CTL lines. The PHY shall assert at least one cycle of idle following a receive operation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TSB42AC3PZT	Obsolete	Production	TQFP (PZT) | 100	-	-	Call TI	Call TI	0 to 70	

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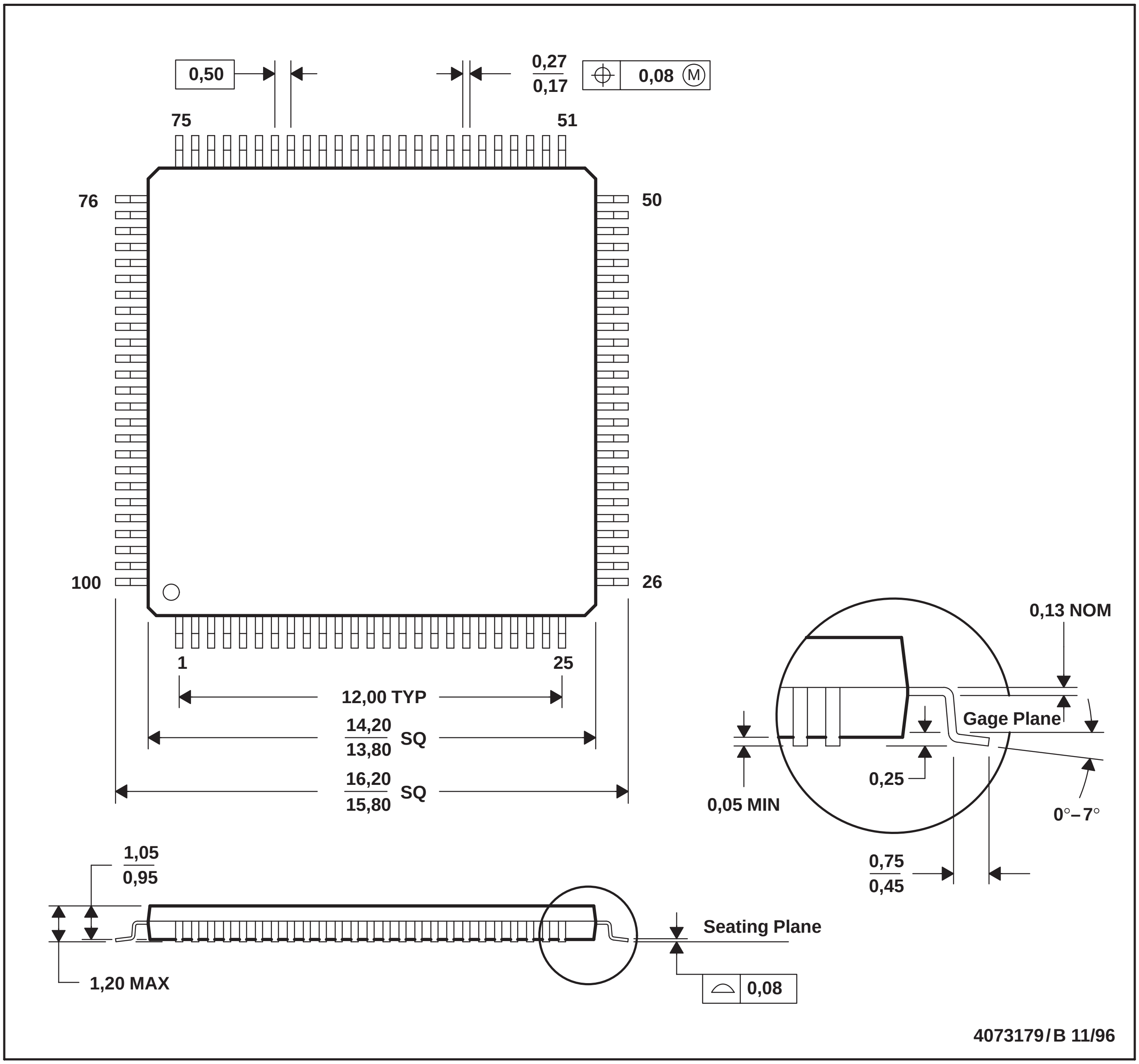
PZT (S-PQFP-G100) PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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