TXB0604 345Mbps Auto-Bidirectional Level Translator for High-Speed Interfaces

1 Features

- 0.9V to 2V on A port and 1.65V to 3.6V on B port ($V_{CCA} \leq V_{CCB}$)
- Maximum data rates:
  - >345Mbps (15pF load)
  - >190Mbps (100pF load)
- Supports high-speed interfaces such as QSPI, OSPI, eSPI
- No direction control signal needed
- V_{CC} isolation feature: if either V_{CC} input is at GND, all outputs are in the high-impedance state
- Schmitt-trigger inputs allow for slow or noisy inputs
- Output enable (OE) input circuit referenced to V_{CCA}
- Latch-up Performance Exceeds 100mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - A Port:
    - 2000V Human-Body Model (A114-B)
    - 1000V Charged-Device Model (C101)
  - B Port:
    - 2000V Human-Body Model (A114-B)
    - 1000V Charged-Device Model (C101)

2 Applications

- Data Center and Enterprise Computing
- Desktop PC
- Personal Electronics

3 Description

The TXB0604 is an 4-bit non-inverting auto-bidirectional translator that uses two separate configurable power-supply rails. This voltage translator/ line redriver can be used to remedy voltage domain mismatches in addition to signal boosting in long-cabling transmission applications.

The TXB0604 leverages a patented design to achieve high data throughput for memory-intensive interfaces like Quad-SPI between BMC and Flash devices without signal integrity losses associated with excessive output parasitic capacitance.

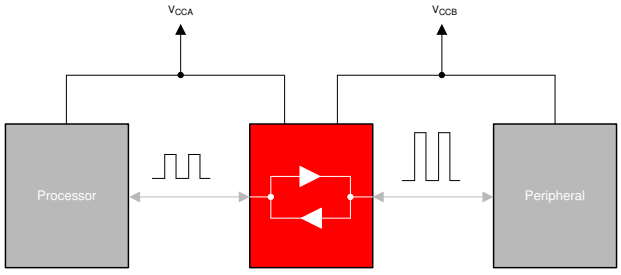
The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 0.9V to 2V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65V to 3.6V.

When the OE input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state during power up or power down, OE must be tied to GND through a pulldown resistor. The current sourcing capability of the driver determines the minimum value of the resistor. The TXB0604 device is designed so the OE input circuit is supplied by V_{CCA}.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TXB0604PW	TSSOP (14)	5.00mm × 4.40mm
TXB0604RGY	VQFN (14)	3.50mm x 3.50mm
TXB0604RWB	X2QFN (12)	1.6mm x 1.6mm
TXB0604RUT	UQFN (12)	2.00mm x 1.70mm
TXB0604DYY	SOT23-THN (14)	4.20mm × 3.26mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Typical Application Block Diagram for TXB0604

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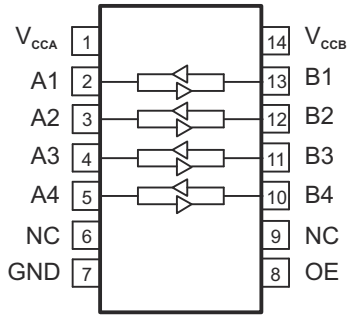
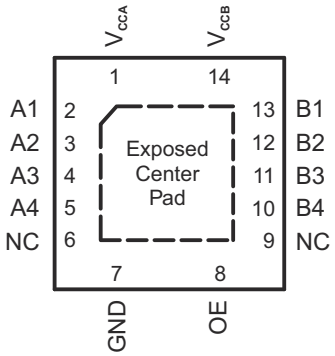
4 Pin Configuration and Functions



NC − No internal connection

Figure 4-1. DYY or PW Package, 14-Pin SOT23-THN or TSSOP (Top View)



NC − No internal connection

Figure 4-2. RGY Package, 14-Pin VQFN With Exposed Thermal Pad (Top View)

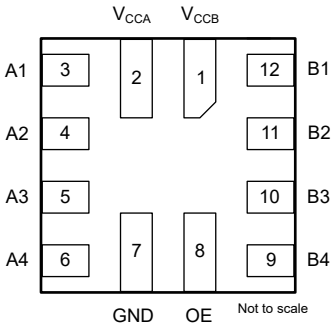


Figure 4-3. RWB Package, 12-Pin X2QFN (Top View)

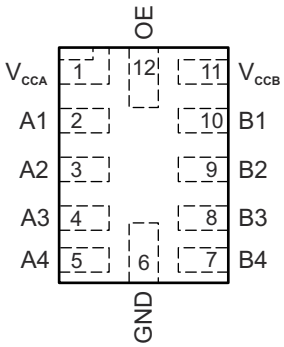


Figure 4-4. RUT Package, 12-Pin UQFN (Top View)

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Table 4-1. Pin Functions

PIN					I/O	DESCRIPTION
NAME	DYY, PW	RGY	RUT	RWB		
A1	2	2	2	3	I/O	Input/output 1. Referenced to V_{CCA}.
A2	3	3	3	4	I/O	Input/output 2. Referenced to V_{CCA}.
A3	4	4	4	5	I/O	Input/output 3. Referenced to V_{CCA}.
A4	5	5	5	6	I/O	Input/output 4. Referenced to V_{CCA}.
B1	13	13	10	12	I/O	Input/output 1. Referenced to V_{CCB}.
B2	12	12	9	11	I/O	Input/output 2. Referenced to V_{CCB}.
B3	11	11	8	10	I/O	Input/output 3. Referenced to V_{CCB}.
B4	10	10	7	9	I/O	Input/output 4. Referenced to V_{CCB}.
GND	7	7	6	7	—	Ground
NC	6, 9	6,9	—	—	—	No connection. Not internally connected.
OE	8	8	12	8	I	Tri-state output-mode enable. Pull OE low to place all outputs in tri-state mode. Referenced to V_{CCA}.
V_{CCA}	1	1	1	2	—	A-port supply voltage 0.9V ≤ V_{CCA} ≤ 2V and V_{CCA} ≤ V_{CCB}.
V_{CCB}	14	14	11	1	—	B-port supply voltage 1.65V ≤ V_{CCB} ≤ 3.6V.
Thermal pad	—		—	—	—	For the RGY package, the exposed center thermal pad must either be connected to Ground or left electrically open.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage A		–0.5	2.5	V
V_{CCB}	Supply voltage B		–0.5	4.6	V
V_I	Input Voltage(2)	I/O Ports (A Port)	–0.5	2.5	V
V_I	Input Voltage(2)	I/O Ports (B Port)	–0.5	4.6	V
V_I	Input Voltage(2)	OE	–0.5	2.5	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A Port	–0.5	2.5	V
		B Port	–0.5	4.6	
V_O	Voltage applied to any output in the high or low state(2) (3)	A Port	–0.5	V_{CCA} + 0.5	V
		B Port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current		–50	50	mA
	Continuous current through V_{CC} or GND		–100	100	mA
T_{stg}	Storage temperature		–65	150	°C
T_j	Junction Temperature			150	°C

(1) Stresses beyond those listed under *Section 5.1* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 5.3* Exposure beyond the limits listed in *Section 5.3* may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	A/B Port	±2	kV
		Charged device model (CDM), per JEDEC specification, JESD220C101	A/B Port	±1	kV

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage A				0.9	2	V
V_{CCB}	Supply voltage B				1.65	3.6	V
V_I	Input voltage	A-port I/O's	0.9V to 2V	1.65V to 3.6V	0	V_{CCA}	V
		B-port I/O's	0.9V to 2V	1.65V to 3.6V	0	V_{CCB}	
		OE Input	0.9V to 2V	1.65V to 3.6V	0	2	
T_A	Operating free-air temperature				–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All control inputs and data I/Os of this device have weak pulldowns to ensure the line is not floating when undefined external to the device. The input leakage from these weak pulldowns is defined by the I_I specification indicated under *Section 5.4*

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5.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)						UNIT
					–40°C to 85°C			–40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{T+}	Positive-going input-threshold voltage	Data Inputs (Ax) (Referenced to V_{CCI})	0.9V	1.65V	0.53		0.66	0.53		0.66	V
			1.2V	1.8V	0.71		0.86	0.71		0.86	
			1.8V	2.5V	1.05		1.24	1.04		1.24	
			2V	3.6V	1.15		1.36	1.15		1.36	
	Positive-going input-threshold voltage	Data Inputs (Bx) (Referenced to V_{CCI})	0.9V	1.65V	0.86		1.16	0.84		1.16	V
			1.2V	1.8V	0.93		1.24	0.91		1.24	
			1.8V	2.5V	1.23		1.56	1.23		1.56	
			2V	3.6V	1.72		2.11	1.72		2.11	
	Positive-going input-threshold voltage	OE (Referenced to V_{CCA})	0.9V	1.65V	0.53		0.66	0.52		0.66	V
			1.2V	1.8V	0.69		0.85	0.68		0.85	
			1.8V	2.5V	0.97		1.17	0.96		1.17	
			2V	3.6V	1.05		1.26	1.05		1.26	
V_{T-}	Negative-going input-threshold voltage	Data Inputs (Ax) (Referenced to V_{CCI})	0.9V	1.65V	0.29		0.40	0.29		0.41	V
			1.2V	1.8V	0.39		0.51	0.39		0.52	
			1.8V	2.5V	0.59		0.74	0.59		0.75	
			2V	3.6V	0.67		0.82	0.67		0.83	
	Negative-going input-threshold voltage	Data Inputs (Bx) (Referenced to V_{CCI})	0.9V	1.65V	0.58		0.83	0.58		0.85	V
			1.2V	1.8V	0.65		0.91	0.65		0.93	
			1.8V	2.5V	0.99		1.28	0.99		1.29	
			2V	3.6V	1.47		1.83	1.47		1.84	
	Negative-going input-threshold voltage	OE (Referenced to V_{CCA})	0.9V	1.65V	0.29		0.40	0.29		0.41	V
			1.2V	1.8V	0.39		0.51	0.39		0.52	
			1.8V	2.5V	0.59		0.74	0.59		0.75	
			2V	3.6V	0.67		0.82	0.67		0.83	
ΔV_T	Input-threshold hysteresis ($V_{T+} – V_{T-}$)	Data Inputs (Ax) (Referenced to V_{CCI})	0.9V	1.65V	0.22		0.30	0.21		0.30	V
			1.2V	1.8V	0.30		0.38	0.28		0.38	
			1.8V	2.5V	0.41		0.54	0.39		0.54	
			2V	3.6V	0.44		0.58	0.42		0.58	
	Input-threshold hysteresis ($V_{T+} – V_{T-}$)	Data Inputs (Bx) (Referenced to V_{CCI})	0.9V	1.65V	0.19		0.44	0.17		0.44	V
			1.2V	1.8V	0.19		0.43	0.17		0.43	
			1.8V	2.5V	0.19		0.38	0.18		0.38	
			2V	3.6V	0.22		0.32	0.21		0.32	
	Input-threshold hysteresis ($V_{T+} – V_{T-}$)	OE (Referenced to V_{CCA})	0.9V	1.65V	0.21		0.30	0.20		0.30	V
			1.2V	1.8V	0.27		0.37	0.26		0.37	
			1.8V	2.5V	0.33		0.48	0.32		0.48	
			2V	3.6V	0.35		0.49	0.34		0.49	
V_{OHA}	Port A output high voltage	I_{OH} = –20uA	0.9V to 1.2V	1.65V to 3.6V	VCCA - 0.2			VCCA - 0.2			V
			1.2V to 2V		VCCA - 0.4			VCCA - 0.4			
V_{OLA}	Port A output low voltage	I_{OL} = 20uA	0.9V to 2V	1.65V to 3.6V			0.2			0.25	V
V_{OHB}	Port B output high voltage	I_{OH} = –20uA	0.9V to 1.2V	1.65V to 3.6V	VCCB - 0.2			VCCB - 0.2			V
			1.2V to 2V		VCCB - 0.4			VCCB - 0.4			
V_{OLB}	Port B output low voltage	I_{OL} = 20uA	0.9V to 2V	1.65V to 3.6V			0.2			0.25	V

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over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)						UNIT
					–40°C to 85°C			–40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
I_I	Input leakage current	OE $V_I = V_{CC}$ or GND	0.9V to 2V	1.65V to 3.6V			±1			±2	µA
I_{OZ}	High-impedance state output current	OE = GND	0.9V to 2V	1.65V to 3.6V			±1			±3	µA
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND, $I_O = 0$	0.9V	1.65V to 3.6V			6			17	µA
			1.2V to 2V	1.65V to 3.6V			9			24	
			2V	0V			4			19	
			0V	3.6V			±7.5			±8.5	
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND, $I_O = 0$	0.9V	1.65V to 3.6V			10			13	µA
			1.2V to 2V	1.65V to 3.6V			10			13	
			2V	0V			6			12	
			0V	3.6V			2			5	
I_{CCZA}	High-impedance state V_{CCA} supply current	$V_I = V_{CCI}$ or GND $I_O = 0$, OE = GND	0.9V to 2V	1.65V to 3.6V			6			21	µA
I_{CCZB}	High-impedance state V_{CCB} supply current	$V_I = V_{CCI}$ or GND $I_O = 0$, OE = GND	0.9V to 2V	1.65V to 3.6V			4			8	µA
C_i	Control Input Capacitance	OE	0.9V to 2V	1.65V to 3.6V			3			3	pF
C_{io}	Input-to-output internal capacitance	A port	0.9V to 2V	1.65V to 3.6V			5			7	pF
		B port	0.9V to 2V	1.65V to 3.6V			8			9	pF

(1) V_{CCI} is the V_{CC} associated with the input port
(2) V_{CCO} is the V_{CC} associated with the output port

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5.5 Switching Characteristics, V_{CCA} = 0.9V

PARAMETER		FROM	TO	TEST CONDITIONS	LOAD	B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	-40°C to 85°C	C_L =15pF	5.1		13.0	4.4		9.2	4.1		9.4	ns
				-40°C to 85°C	C_L =100pF	6.6		17.6	5.6		12.1	6.2		11.7	
				-40°C to 125°C	C_L =15pF	5.1		13.0	4.4		9.2	4.1		9.4	ns
				-40°C to 125°C	C_L =100pF	6.6		17.6	5.6		12.1	6.2		11.7	
t_{PLH}	Propagation Delay (Low-to-High)			-40°C to 85°C	C_L =15pF	5.8		14.8	5.1		10.4	4.7		10.2	ns
				-40°C to 85°C	C_L =100pF	7.3		18.3	6.3		12.9	5.8		11.7	
				-40°C to 125°C	C_L =15pF	5.8		14.8	5.1		10.4	4.7		10.2	ns
				-40°C to 125°C	C_L =100pF	7.3		18.3	6.3		12.9	5.8		11.7	
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	-40°C to 85°C	C_L =15pF	4.0		9.6	3.6		8.3	3.4		7.8	ns
				-40°C to 85°C	C_L =100pF	5.1		12.0	4.7		10.8	4.6		10.4	
				-40°C to 125°C	C_L =15pF	4.0		9.6	3.6		8.3	3.4		7.8	ns
				-40°C to 125°C	C_L =100pF	5.1		12.0	4.7		10.8	4.6		10.4	
t_{PLH}	Propagation Delay (Low-to-High)			-40°C to 85°C	C_L =15pF	3.7		8.2	3.5		7.0	3.4		6.7	ns
				-40°C to 85°C	C_L =100pF	5.1		10.9	4.9		9.7	4.7		9.3	
				-40°C to 125°C	C_L =15pF	3.7		8.2	3.5		7.0	3.4		6.7	ns
				-40°C to 125°C	C_L =100pF	5.1		10.9	4.9		9.7	4.7		9.3	
t_{DCW}	Direction Change Wait Time	A or B	B or A	-40°C to 125°C				40			35			35	ns
t_{en}	Enable Time	OE	B	-40°C to 125°C				577			557			588	ns
		OE	A					447			353			330	
t_{dis}	Disable Time	OE	B	-40°C to 125°C				87			87			86	ns
		OE	A					95			95			96	
t_{rA} ,t_{fA}	Ouput Rise/ Fall Time	B	A	-40°C to 85°C	C_L =15pF			1			1			1	ns
				-40°C to 85°C	C_L =100pF			7.5			7.4			7.3	ns
				-40°C to 125°C	C_L =15pF			1			1			1	ns
				-40°C to 125°C	C_L =100pF			7.5			7.4			7.3	ns
t_{rB} ,t_{fB}	Ouput Rise/ Fall Time	A	B	-40°C to 85°C	C_L =15pF			2.6			1.2			1	ns
				-40°C to 85°C	C_L =100pF			11.6			8.1			6.9	ns
				-40°C to 125°C	C_L =15pF			2.6			1.2			1	ns
				-40°C to 125°C	C_L =100pF			11.6			8.1			6.9	ns

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PARAMETER		FROM	TO	TEST CONDITIONS	LOAD	B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{sk(o)}$	Channel-to-channel skew	A or B	B or A	-40°C to 125°C	C_L =15pF			0.5			0.5			0.5	ns
$Z_{OS,B}$	One-Shot Impedance	B	A	-40°C to 125°C			27.8			22.3			21		Ω
Data Rate	Maximum data rate	A or B	B or A	-40°C to 125°C	C_L =15pF (1)	85	142		129	180		128	166		Mbps
		A or B	B or A	-40°C to 125°C	C_L =100pF (1)	83	118		54	137		48	137		Mbps

(1) C_L is given as a lumped capacitance at the output.

5.6 Switching Characteristics, V_{CCA} = 1.2V

PARAMETER		FROM	TO	TEST CONDITIONS	LOAD	B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	-40°C to 85°C	C_L =15pF	4.2		12.0	3.5		7.9	3.1		6.6	ns
				-40°C to 85°C	C_L =100pF	5.7		16.6	4.7		10.9	4.2		8.9	
				-40°C to 125°C	C_L =15pF	4.2		12.0	3.5		7.9	3.1		6.6	ns
				-40°C to 125°C	C_L =100pF	5.7		16.6	4.7		10.9	4.2		8.9	
t_{PLH}	Propagation Delay (Low-to-High)			-40°C to 85°C	C_L =15pF	4.5		13.3	3.8		8.9	3.4		7.4	ns
				-40°C to 85°C	C_L =100pF	6.1		16.8	5.1		11.3	4.5		9.4	
				-40°C to 125°C	C_L =15pF	4.5		13.3	3.8		8.9	3.4		7.4	ns
				-40°C to 125°C	C_L =100pF	6.1		16.8	5.1		11.3	4.5		9.4	
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	-40°C to 85°C	C_L =15pF	2.8		6.9	2.5		5.4	2.3		4.8	ns
				-40°C to 85°C	C_L =100pF	3.8		8.3	3.4		6.8	3.3		6.2	
				-40°C to 125°C	C_L =15pF	2.8		6.9	2.5		5.4	2.3		4.8	ns
				-40°C to 125°C	C_L =100pF	3.8		8.3	3.4		6.8	3.3		6.2	
t_{PLH}	Propagation Delay (Low-to-High)			-40°C to 85°C	C_L =15pF	2.7		6.3	2.4		5.0	2.2		4.5	ns
				-40°C to 85°C	C_L =100pF	3.8		8.0	3.5		6.7	3.3		6.3	
				-40°C to 125°C	C_L =15pF	2.7		6.3	2.4		5.0	2.2		4.5	ns
				-40°C to 125°C	C_L =100pF	3.8		8.0	3.5		6.7	3.3		6.3	
t_{DCW}	Direction Change Wait Time	A or B	B or A	-40°C to 125°C				40			35			35	ns
t_{en}	Enable Time	OE	B	-40°C to 125°C				463			433			429	ns
		OE	A					413			319			296	

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PARAMETER		FROM	TO	TEST CONDITIONS	LOAD	B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{dis}	Disable Time	OE	B	-40°C to 125°C				89			87			86	ns
		OE	A					95			95			95	
t_{rA} ,t_{fA}	Ouput Rise/ Fall Time	B	A	-40°C to 85°C	C_L =15pF			0.8			0.8			0.8	ns
					C_L =100pF			6.1			6.1			6.2	
				-40°C to 125°C	C_L =15pF			0.8			0.8			0.8	
					C_L =100pF			6.1			6.1			6.2	
t_{rB} ,t_{fB}	Ouput Rise/ Fall Time	A	B	-40°C to 85°C	C_L =15pF			2.6			1.3			1	ns
					C_L =100pF			11.6			8.1			6.9	
				-40°C to 125°C	C_L =15pF			2.6			1.3			1	
					C_L =100pF			11.6			8.1			6.9	
$t_{sk(o)}$	Channel-to-channel skew	A or B	B or A	-40°C to 125°C	C_L =15pF			0.5			0.5			0.5	ns
$Z_{OS,A}$	One-Shot Impedance	A or B	B or A				27.8			22.3			21		Ω
Data Rate	Maximum data rate	A or B	B or A		C_L =15pF (1)	142	211		208	292		229	309		Mbps
		A or B	B or A		C_L =100pF (1)	103	141		137	149		140	149		

(1) C_L is given as a lumped capacitance at the output.

5.7 Switching Characteristics, V_{CCA} = 1.5V ± 0.1V

PARAMETER		FROM	TO	TEST CONDITIONS	LOAD	B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	-40°C to 85°C	C_L =15pF	3.8		11.9	3.2		7.6	2.8		6.1	ns
				-40°C to 85°C	C_L =100pF	5.2		16.7	4.3		10.7	3.8		8.5	
				-40°C to 125°C	C_L =15pF	3.8		11.9	3.2		7.6	2.8		6.1	ns
				-40°C to 125°C	C_L =100pF	5.2		16.7	4.3		10.7	3.8		8.5	
t_{PLH}	Propagation Delay (Low-to-High)			-40°C to 85°C	C_L =15pF	4.0		13.1	3.4		8.4	3.0		6.7	ns
				-40°C to 85°C	C_L =100pF	5.5		16.7	4.5		11.0	4.0		8.9	
				-40°C to 125°C	C_L =15pF	4.0		13.1	3.4		8.4	3.0		6.7	ns
				-40°C to 125°C	C_L =100pF	5.5		16.7	4.5		11.0	4.0		8.9	

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PARAMETER		FROM	TO	TEST CONDITIONS	LOAD	B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	-40°C to 85°C	C_L =15pF	2.5		6.4	2.2		4.7	2.0		4.1	ns
				-40°C to 85°C	C_L =100pF	3.4		7.7	3.0		6.1	2.9		5.4	
				-40°C to 125°C	C_L =15pF	2.5		6.4	2.2		4.7	2.0		4.1	ns
				-40°C to 125°C	C_L =100pF	3.4		7.7	3.0		6.1	2.9		5.4	
t_{PLH}	Propagation Delay (Low-to-High)			-40°C to 85°C	C_L =15pF	2.4		5.9	2.1		4.5	1.9		3.9	ns
				-40°C to 85°C	C_L =100pF	3.4		7.5	3.1		6.1	2.9		5.5	
				-40°C to 125°C	C_L =15pF	2.4		5.9	2.1		4.5	1.9		3.9	ns
				-40°C to 125°C	C_L =100pF	3.4		7.5	3.1		6.1	2.9		5.5	
t_{DCW}	Direction Change Wait Time	A or B	B or A	-40°C to 125°C				40			35			35	ns
t_{en}	Enable Time	OE	B	-40°C to 125°C				382			356			350	ns
			A	-40°C to 125°C				408			313			291	
t_{dis}	Disable Time		B	-40°C to 125°C				89			88			87	
			A	-40°C to 125°C				95			95			95	
t_{rA} ,t_{fA}	Ouput Rise/ Fall Time	B	A	-40°C to 85°C	C_L =15pF			0.8			0.8			0.8	ns
				-40°C to 85°C	C_L =100pF			5.8			5.9			6	
				-40°C to 125°C	C_L =15pF			0.8			0.8			0.8	
				-40°C to 125°C	C_L =100pF			5.8			5.9			6	
t_{rB} ,t_{fB}	Ouput Rise/ Fall Time	A	B	-40°C to 85°C	C_L =15pF			2.6			1.3			1	ns
				-40°C to 85°C	C_L =100pF			11.6			8.1			6.9	
				-40°C to 125°C	C_L =15pF			2.6			1.3			1	
				-40°C to 125°C	C_L =100pF			11.6			8.1			6.9	
$t_{sk(o)}$	Channel-to-channel skew	A or B	B or A	-40°C to 125°C				0.5			0.5			0.5	ns
$Z_{OS,A}$	One-Shot Impedance	A or B	A or B	-40°C to 125°C			27.8			22.3			21		Ω
Data Rate	Maximum data rate	A or B	B or A	C_L =15pF (1)		154	237		244	372		308	378		Mbps
		A or B	B or A	C_L =100pF (1)		104	145		151	199		147	221		

(1) C_L is given as a lumped capacitance at the output.

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5.8 Switching Characteristics, V_{CCA} = 1.8V ± 0.15V

PARAMETER		FROM	TO	TEST CONDITIONS	LOAD	B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	-40°C to 85°C	C_L =15pF	3.7		11.7	3.0		7.3	2.7		5.8	ns
				-40°C to 85°C	C_L =100pF	5.1		16.5	4.1		10.4	3.6		8.3	
				-40°C to 125°C	C_L =15pF	3.7		11.7	3.0		7.3	2.7		5.8	ns
				-40°C to 125°C	C_L =100pF	5.1		16.5	4.1		10.4	3.6		8.3	
t_{PLH}	Propagation Delay (Low-to-High)			-40°C to 85°C	C_L =15pF	3.9		12.8	3.2		8.0	2.8		6.4	ns
				-40°C to 85°C	C_L =100pF	5.4		16.4	4.4		10.6	3.9		8.5	
				-40°C to 125°C	C_L =15pF	3.9		12.8	3.2		8.0	2.8		6.4	ns
				-40°C to 125°C	C_L =100pF	5.4		16.4	4.4		10.6	3.9		8.5	
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	-40°C to 85°C	C_L =15pF	2.5		6.2	2.1		4.4	1.9		3.7	ns
				-40°C to 85°C	C_L =100pF	3.3		7.5	2.9		5.8	2.8		5.1	
				-40°C to 125°C	C_L =15pF	2.5		6.2	2.1		4.4	1.9		3.7	ns
				-40°C to 125°C	C_L =100pF	3.3		7.5	2.9		5.8	2.8		5.1	
t_{PLH}	Propagation Delay (Low-to-High)			-40°C to 85°C	C_L =15pF	2.3		5.7	2.0		4.2	1.8		3.6	ns
				-40°C to 85°C	C_L =100pF	3.3		7.3	3.0		5.8	2.8		5.2	
				-40°C to 125°C	C_L =15pF	2.3		5.7	2.0		4.2	1.8		3.6	ns
				-40°C to 125°C	C_L =100pF	3.3		7.3	3.0		5.8	2.8		5.2	
t_{DCW}	Direction Change Wait Time	A or B	B or A	-40°C to 125°C				40			35			35	ns
t_{en}	Enable Time	OE	A or B	-40°C to 125°C				348			320			315	ns
			A or B	-40°C to 125°C				407			313			290	
t_{dis}	Disable Time		A or B	-40°C to 125°C				94			91			89	
			A or B	-40°C to 125°C				94			95			95	
t_{rA} ,t_{fA}	Ouput Rise/ Fall Time	B	A	-40°C to 85°C	C_L =15pF			0.8			0.8			0.8	ns
				-40°C to 85°C	C_L =100pF			5.8			5.8			5.9	
				-40°C to 125°C	C_L =15pF			0.8			0.8			0.8	
				-40°C to 125°C	C_L =100pF			5.8			5.8			5.9	
t_{rB} ,t_{fB}	Ouput Rise/ Fall Time	A	B	-40°C to 85°C	C_L =15pF			2.6			1.3			1	ns
				-40°C to 85°C	C_L =100pF			11.6			8.1			7	
				-40°C to 125°C	C_L =15pF			2.6			1.3			1	
				-40°C to 125°C	C_L =100pF			11.6			8.1			7	

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PARAMETER		FROM	TO	TEST CONDITIONS	LOAD	B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{sk(o)}$	Channel-to-channel skew	A or B	B or A	-40°C to 125°C	C_L =15pF			0.5			0.5			0.5	ns
$Z_{OS,A}$	One-Shot Impedance	A or B	A or B	-40°C to 125°C			27.8			22.3			21		Ω
Data Rate	Maximum data rate	A or B	B or A	C_L =15pF (1)		158	260		269	402		345	449		Mbps
		A or B	B or A	C_L =100pF (1)		107	150		156	213		190	236		

(1) C_L is given as a lumped capacitance at the output.

5.9 Switching Characteristics: T_{sk}, T_{MAX} (-40°C to 125°C)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CCI}	V_{CCO}	Operating free-air temperature (T_A)			UNIT
					-40°C to 125°C			
					MIN	TYP	MAX	
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input One channel switching 20% of pulse > 0.7*V_{CCO} 20% of pulse < 0.3*V_{CCO}	TX Line: 20inch + 50pF Cload	0.9V - 2V	1.8V - 2V	70	99		Mbps
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input One channel switching 20% of pulse > 0.7*V_{CCO} 20% of pulse < 0.3*V_{CCO}	TX Line: 20inch + 50pF Cload	1.2V - 2V	1.8V - 2V	80	111		Mbps
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input One channel switching 20% of pulse > 0.7*V_{CCO} 20% of pulse < 0.3*V_{CCO}	TX Line: 20inch + 50pF Cload	1.65V - 2V	1.8V - 2V	80	115		Mbps
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input One channel switching 20% of pulse > 0.7*V_{CCO} 20% of pulse < 0.3*V_{CCO}	TX Line: 20inch + 50pF Cload	0.9V - 2V	3.6V	82	120		Mbps
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input One channel switching 20% of pulse > 0.7*V_{CCO} 20% of pulse < 0.3*V_{CCO}	TX Line: 20inch + 50pF Cload	1.2V - 2V	3.6V	132	170		Mbps
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input One channel switching 20% of pulse > 0.7*V_{CCO} 20% of pulse < 0.3*V_{CCO}	TX Line: 20inch + 50pF Cload	1.65V - 2V	3.6V	142	187		Mbps

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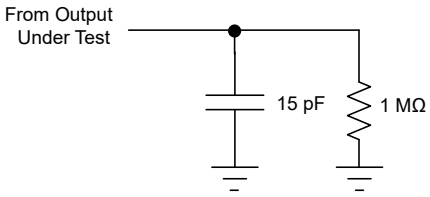
6 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators that have the following characteristics:

- PRR 10MHz
- Z_O = 50W
- dv/dt ≥ 1V/ns

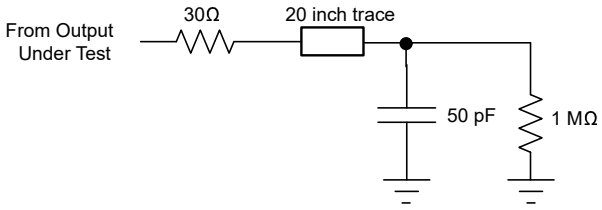
Note

All parameters and waveforms are not applicable to all devices.



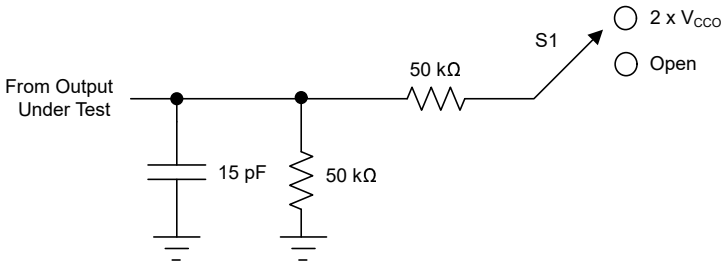
A. The outputs are measured one at a time, with one transition per measurement.

Figure 6-1. Lumped Capacitive Load Circuit For Maximum Data Rate & Propagation Delay, Output Rise, And Fall Time Measurement



A. The outputs are measured one at a time, with one transition per measurement.

Figure 6-2. Long Trace + Capacitive Load Circuit For Maximum Data Rate



A. The outputs are measured one at a time, with one transition per measurement.

Figure 6-3. Load Circuit For Enable and Disable Time Measurement

Table 6-1. Switch Position For Enable and Disable Time Measurement

TEST(1)	S1
t_{PZL}, t_{PLZ}	2 × V_{CCO}
t_{PHZ}, t_{PZH}	Open

(1) See Figure 6-3

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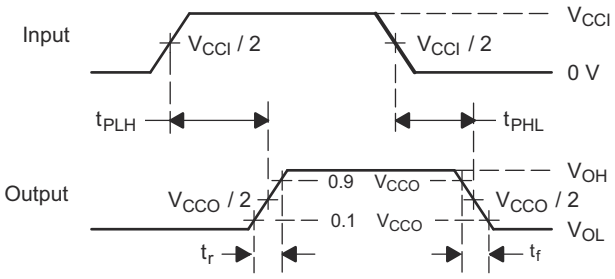

A. V_{CCI} is the V_{CC} associated with the input port.
B. V_{CCO} is the V_{CC} associated with the output port.
C. t_{PLH} and t_{PHL} are the same as t_{pd}.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 6-4. Voltage Waveforms Propagation Delay Times

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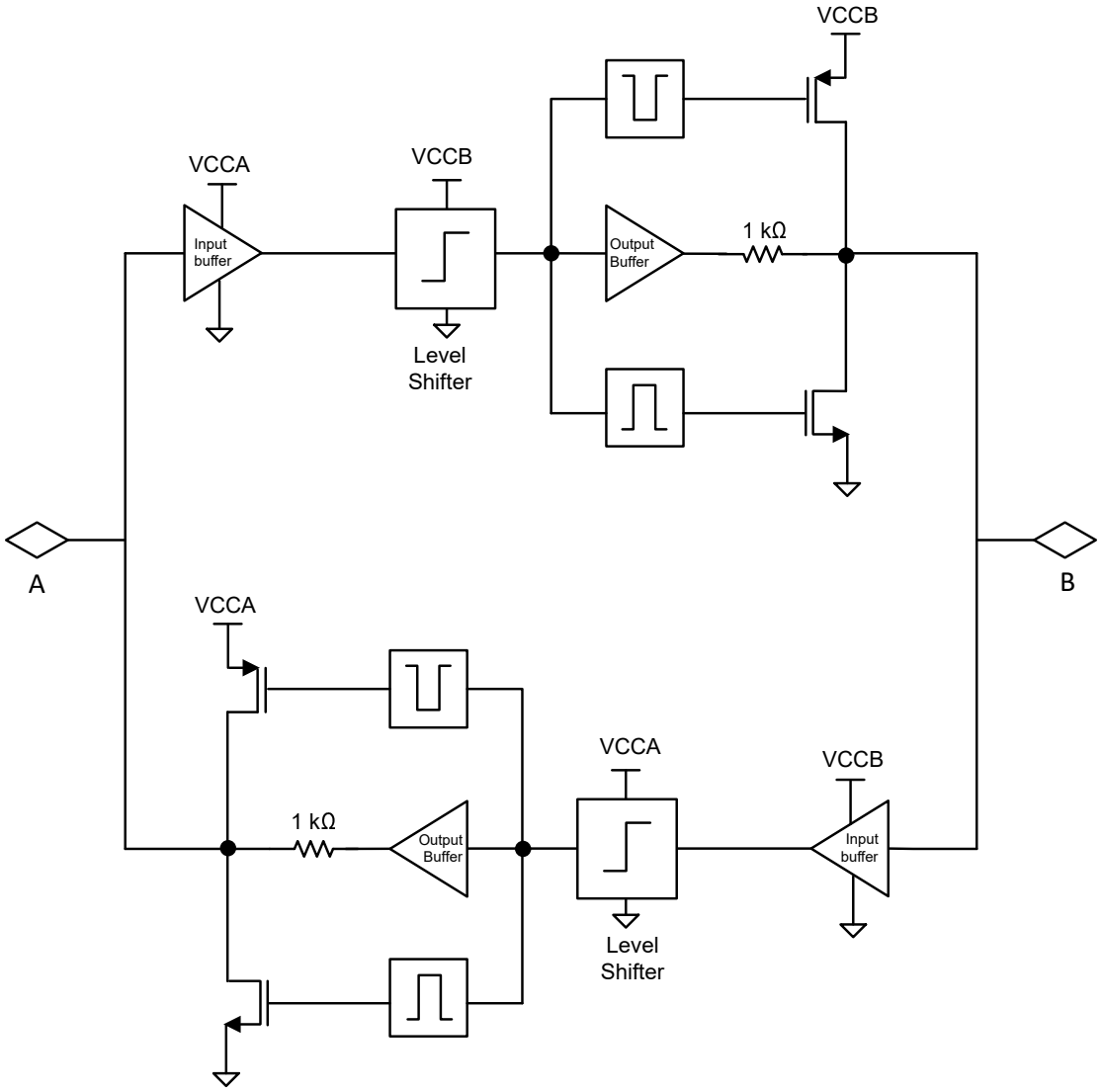
7 Detailed Description

7.1 Overview

The TXB0604 device is a 4-bit, bidirectional voltage-level translator with auto-direction sensing specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 0.9V to 2V, while the B port can accept I/O voltages from 1.65V to 3.6V. The device is a buffered architecture with edge-rate accelerators (one-shots) to improve the overall data rate. This device can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI's TXS010X products.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Architecture

The TXB0604 device architecture (see Figure 7-1) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a DC state, the output drivers of the device maintain a high or low, but are designed to be weak, so the output drivers can be overdriven by an external driver when data on the bus flows the opposite direction.

The output one-shots detect rising or falling edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one-shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is approximately 28Ω at V_{CCO} = 1.8V, approximately 22Ω at V_{CCO} = 2.5V, and 21Ω at V_{CCO} = 3.3V.

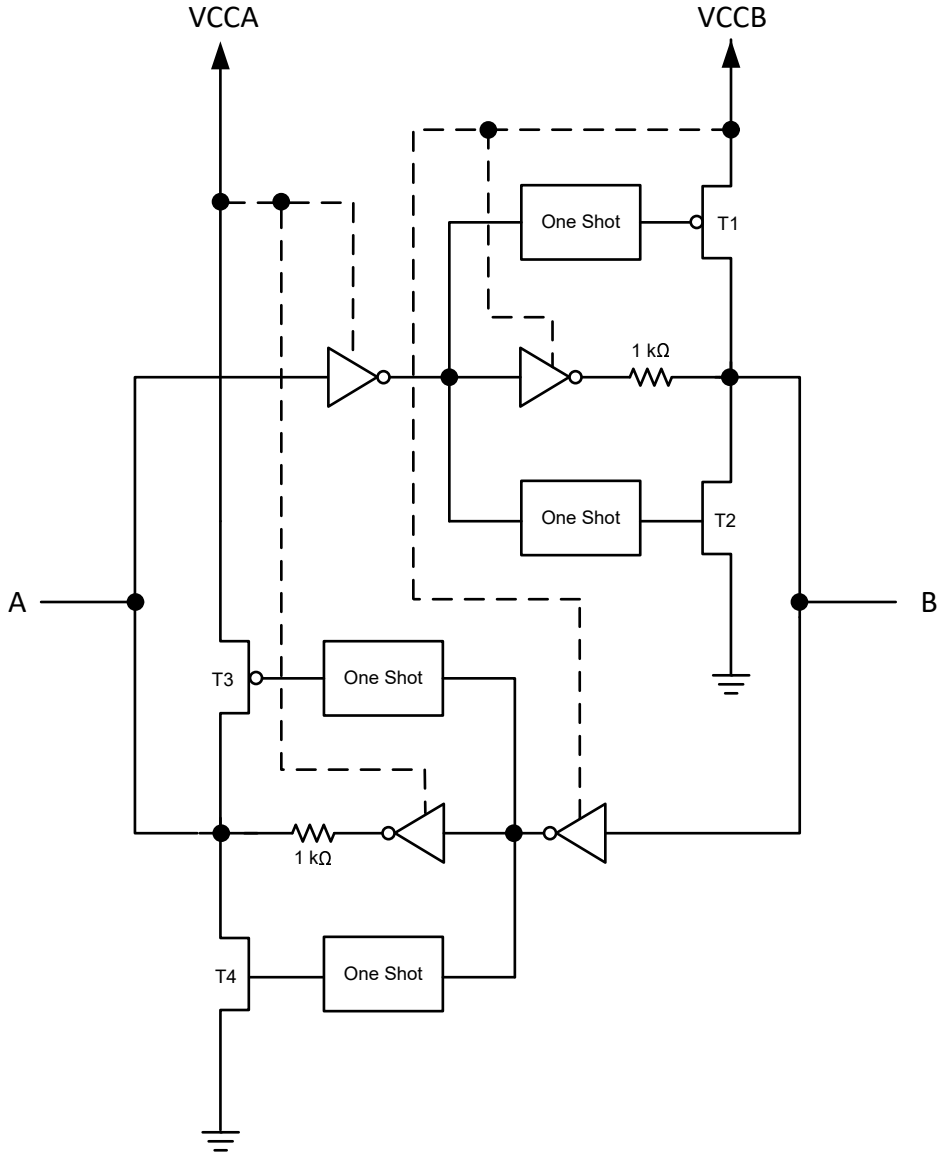

Figure 7-1. Architecture of TXB0604 Device I/O Cell

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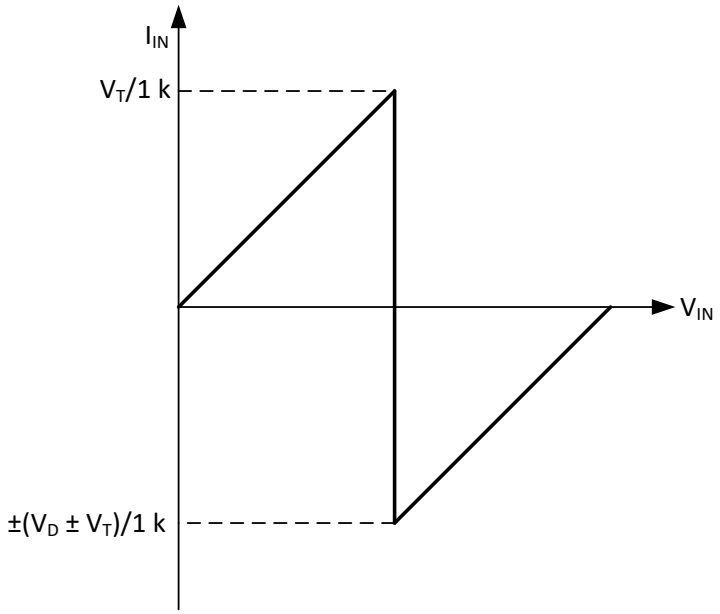
7.3.2 Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the device are shown in Figure 7-2. For proper operation, the device driving the data I/Os of the TXB0604 device must have drive strength of at least ±3mA.



A. V_T is the input threshold of the TXB0604 device, (typically V_{CC} / 2).
B. V_D is the supply voltage of the external driver.

Figure 7-2. Typical I_{IN} vs V_{IN} Curve

7.3.3 Output Load Considerations

TI recommends following careful PCB layout practices to minimize signal distortion and ringing. Impedance matching techniques should be implemented to reduce output oscillations and ensure signal integrity. Series termination resistors are recommended at the device outputs to match the total output impedance to the transmission line.

For example, given that the device output impedance is 21Ω (V_{CCA} = 0.9 to 2V and V_{CCB} = 3.3V), adding a series resistor value of 30Ω provides an effective source impedance close to 50Ω, matching a typical controlled-impedance trace or cable.

7.3.4 Enable and Disable

The TXB0604 has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

7.3.5 Pullup or Pulldown Resistors on I/O Lines

The device is designed to support high-drive applications with either a lumped capacitive load of up to 100pF or a signal trace length of up to 20 inches with a 50pF load. The output drivers of the TXB0604 device have low DC drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 20kΩ to ensure that they do not contend with the output drivers of the TXB0604 device.

For the same reason, the TXB0604 device must not be used in applications such as I^2C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI TXS series of level translators.

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7.3.6 Dummy Cycles

When TXB0604 is used in Quad-SPI (QSPI) interfaces between a microcontroller and serial flash memory, the direction of the data flow can change dynamically between the controller and the memory device. Given the TXB0604 features automatic direction sensing, a minimum turn-around time of 40ns is required for the device to transition from one direction to the other. This is shown under the Switching Characteristics table as t_{DCW} - Direction Change Wait Time.

The ensure proper bus timing, the QSPI controller must insert sufficient dummy clock cycles after the command and address phase before data is sampled from the flash memory. The total dummy period must be greater or equal to the TXB0604 turn-around time of 40ns.

As an example, at a QSPI clock frequency of 104MHz:

$$1/104MHz \quad = \quad 9.6ns \tag{1}$$

$$40ns/9.6ns \quad = \quad 4.16ns \quad \rightarrow \quad 5 \quad dummy \quad cycles \tag{2}$$

Many flash devices, such as the ISSI IS25LQ040B, specificy 8 dummy cycles at 104MHz frequency, which satisfies the TXB0604 requirement and provides additional margin.

7.4 Device Functional Modes

The device has two functional modes, enabled and disabled. To disable the device, set the OE input to low, which places all I/Os in a high impedance state. Setting the OE input to high will enable the device.

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8 Application and Implementation

Note

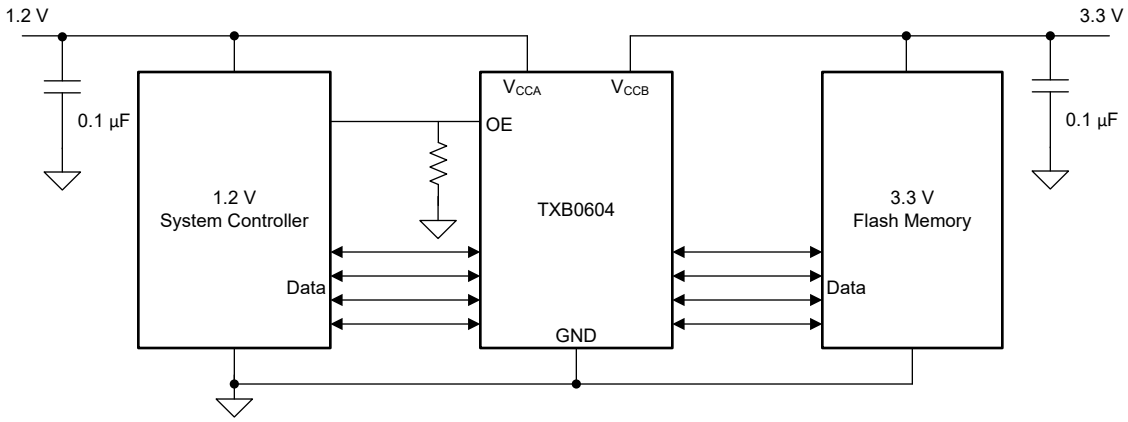
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TXB0604 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI TXS010X products. Any external pulldown or pullup resistors are recommended larger than 20kΩ.

The device features enhanced output drive strength for use in high-speed interfaces such as QSPI, OSPI, eSPI, etc. The device is designed to support high-drive applications with either a lumped capacitive load of up to 100pF at 190Mbps or a signal trace length of up to 20 inches with a 50pF load at 142Mbps.

8.2 Typical Application



8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1. And make sure the $V_{CCA} \leq V_{CCB}$.

Table 8-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	0.9V to 2V
Output voltage range	1.65V to 3.6V

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8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Series resistor at the device outputs
  - Series resistors must be placed at the device outputs to improve signal integrity and to match the total output impedance to the external transmission path. For example, given that the device output impedance is 21Ω, a 30Ω series resistor provides an effective source impedance close to 50Ω, matching a typical controlled-impedance PCB trace or cable connection.
- Input voltage range
  - Use the supply voltage of the device that is driving the TXB0604 device to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port.
- An external pulldown or pullup resistor decreases the output V_{OH} and V_{OL}. Use the below equations to draft estimate the V_{OH} and V_{OL} as a result of an external pulldown and pullup resistor.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 1.5k\Omega) \quad (3)$$

$$V_{OL} = V_{CCx} \times 1.5k\Omega / (R_{PU} + 1.5k\Omega) \quad (4)$$

Where

- V_{CCx} is the output port supply voltage on either V_{CCA} or V_{CCB}
- R_{PD} is the value of the external pull down resistor
- R_{PU} is the value of the external pull up resistor
- 1.5kΩ is the counting the variation of the serial resistor 1kΩ in the I/O line.

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ADVANCE INFORMATION

9 Power Supply Recommendations

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. Please ensure that $V_{CCA/B}$ is powered on before the I/O ports.

The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver.

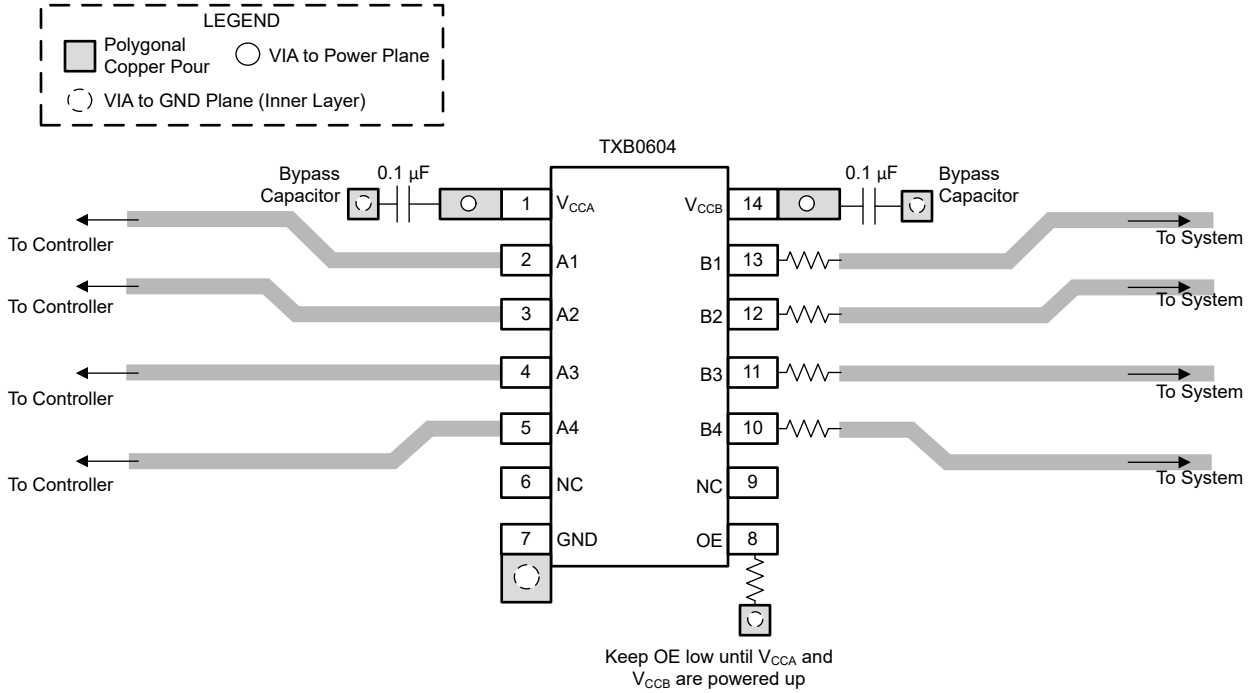
10 Layout

10.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors must be used on power supplies, and must be placed as close as possible to the V_{CCA}, V_{CCB} pin and GND pin.
- Series resistors must be placed at the device outputs to improve signal integrity and match the total output impedance to the external transmission path. For example, given that the device output impedance is 21Ω, a 30Ω series resistor provides an effective source impedance close to 50Ω, matching a typical controlled-impedance PCB trace or cable connection.
- During operation, the data direction changes dynamically between the host and the target device. A direction-change delay (t_{DCW}) must be provided before the bus switches direction between the host and target device. Ensure that the delay between direction changes meets the t_{DCW} requirement listed in the Switching Characteristics table. In QSPI applications, this delay corresponds to dummy clock cycles inserted between the command/address and data phases to satisfy the required turn-around time.

10.2 Layout Example



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11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2025	*	Initial Release

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

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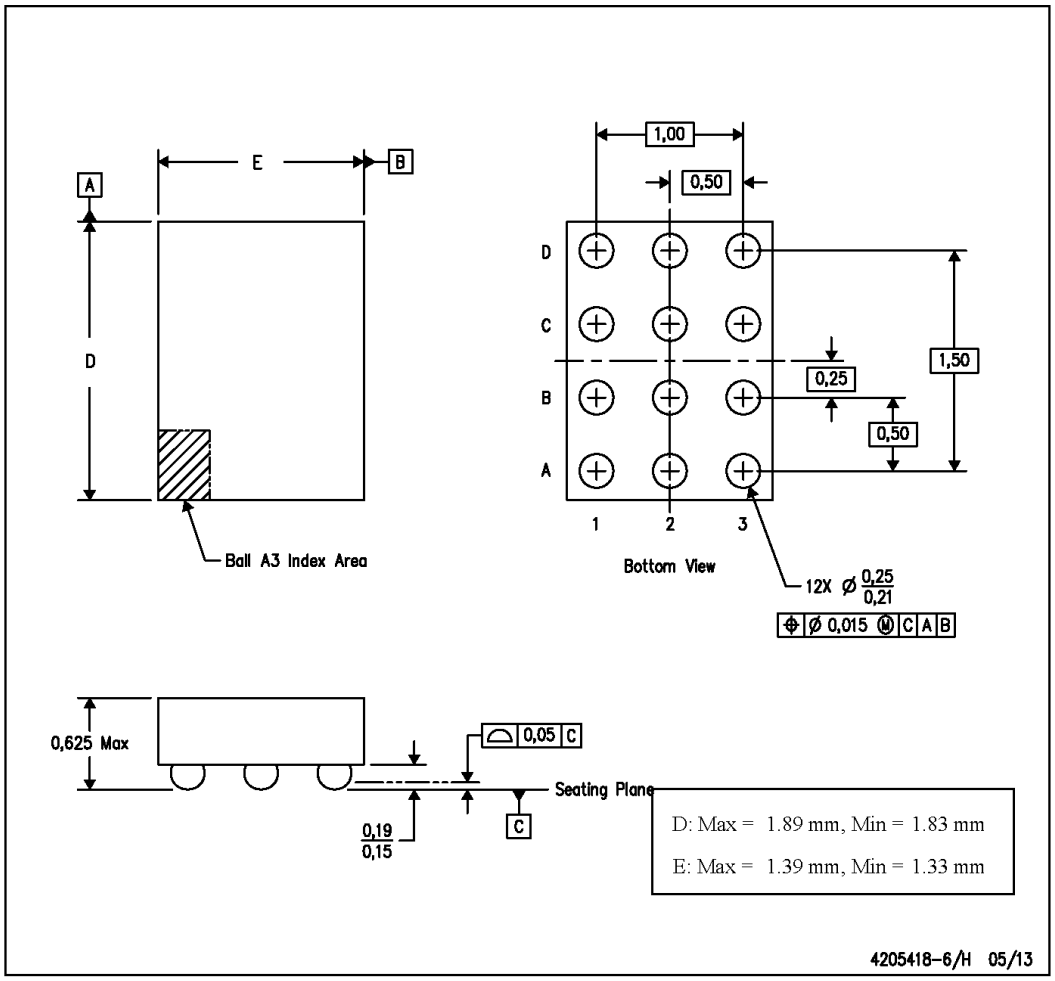
ADVANCE INFORMATION

MECHANICAL DATA

YZT (R–XBGA–N12) (CUSTOM) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTXB0604DYYR	Active	Preproduction	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTXB0604PWR	Active	Preproduction	TSSOP (PW) | 14	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTXB0604RUTR	Active	Preproduction	UQFN (RUT) | 12	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTXB0604RWBR	Active	Preproduction	X2QFN (RWB) | 12	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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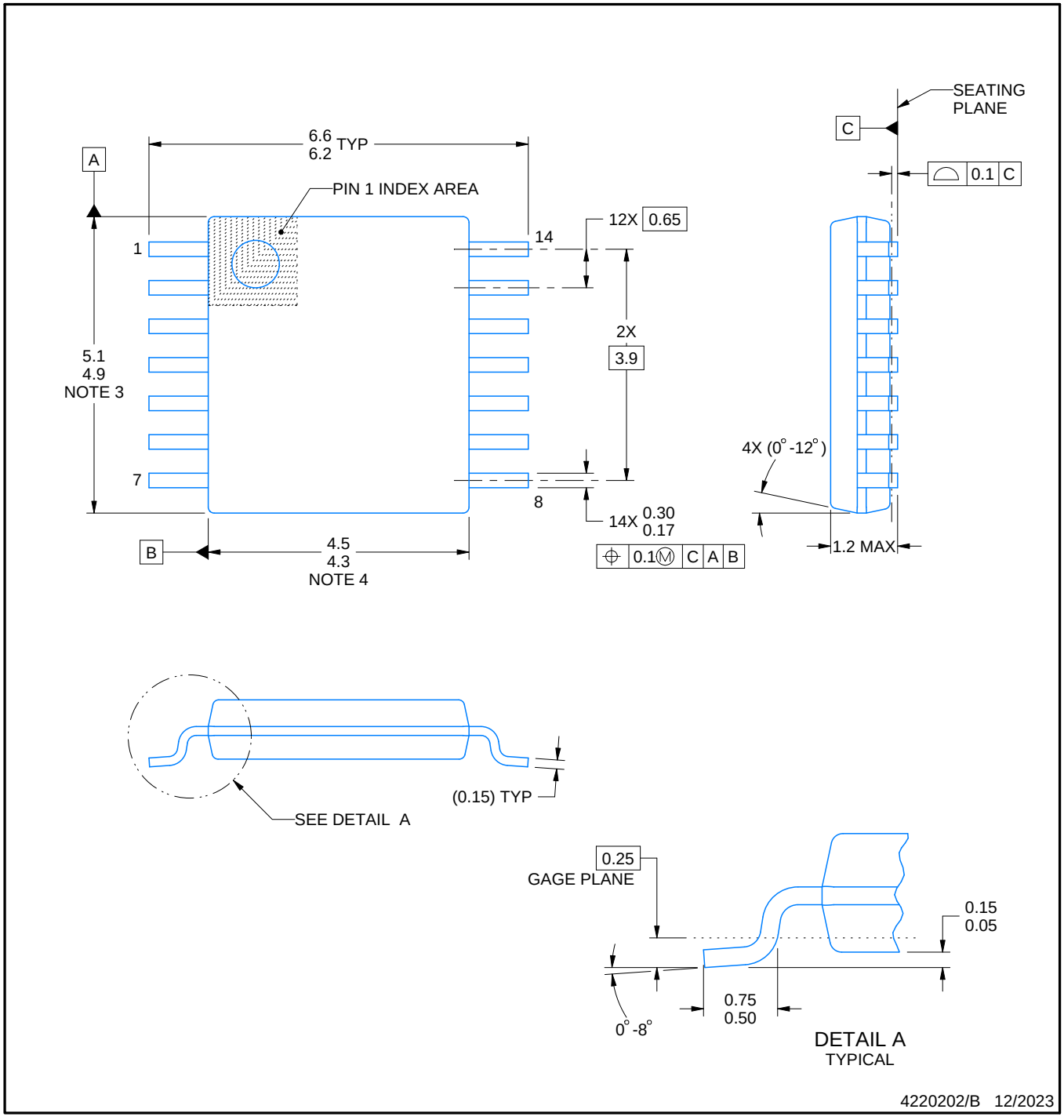
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

PW0014A

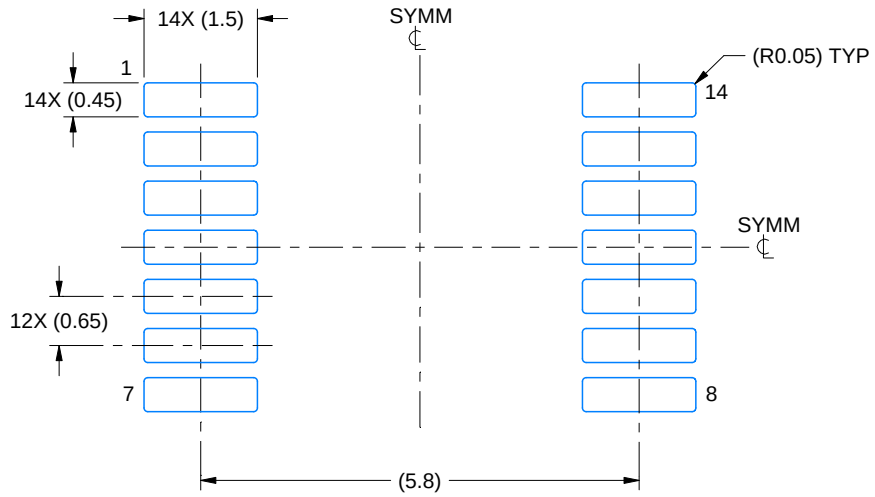
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

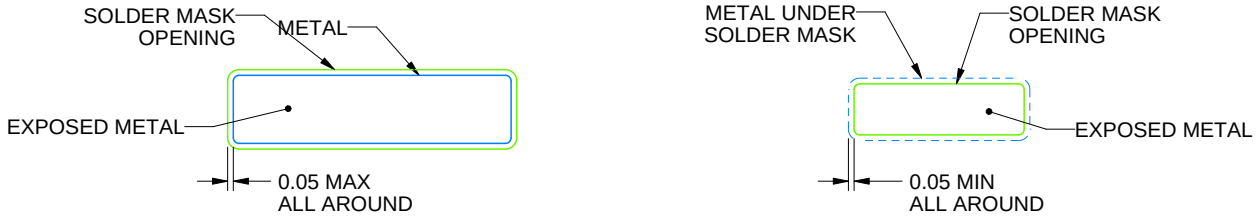


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

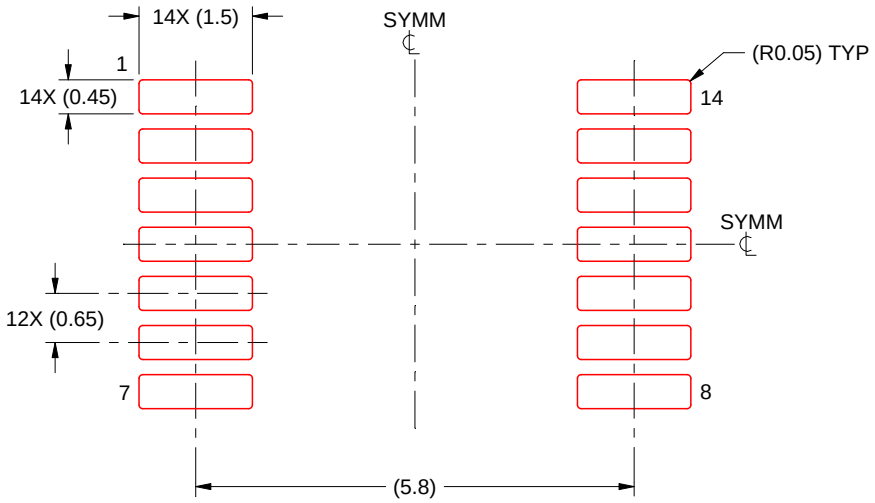


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

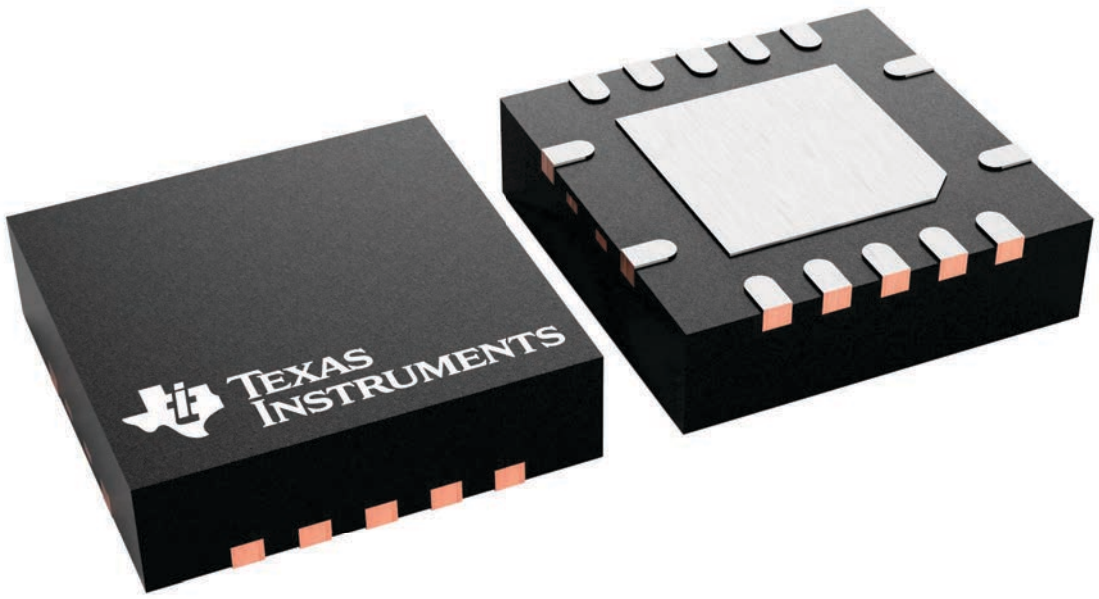
RGY 14

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



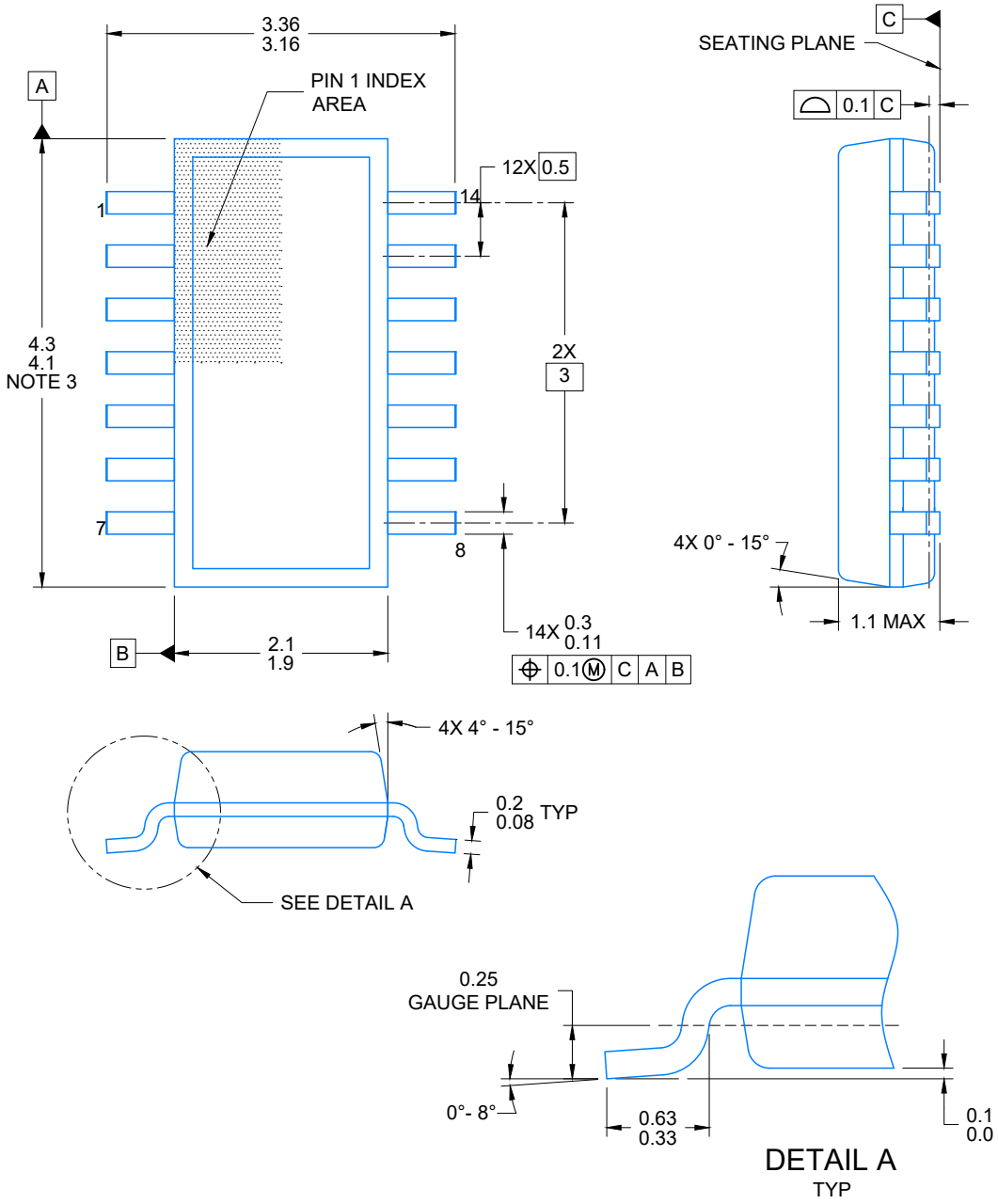
4231541/A

PACKAGE OUTLINE

DYY0014A

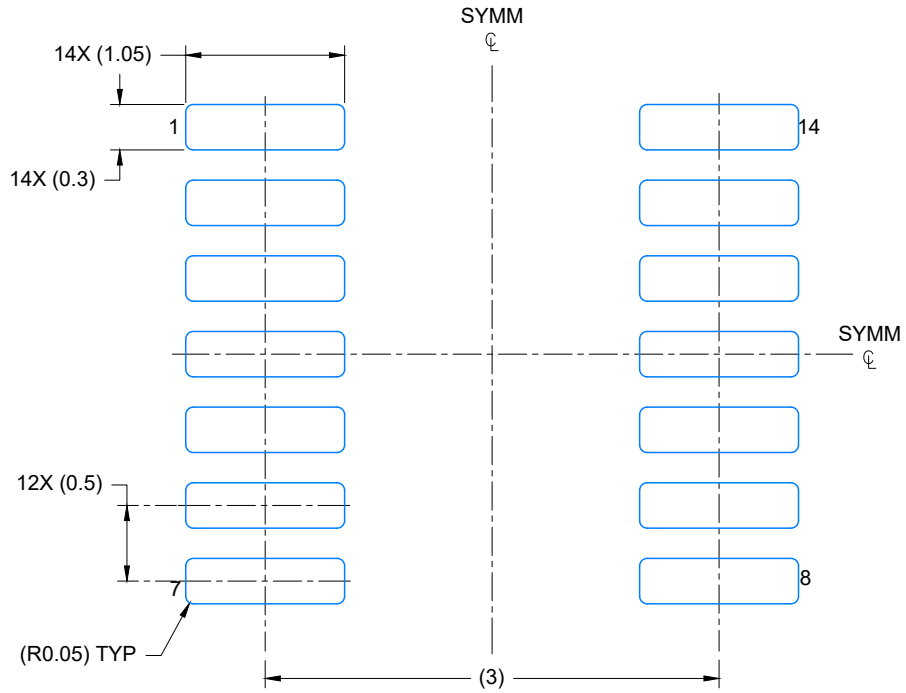
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

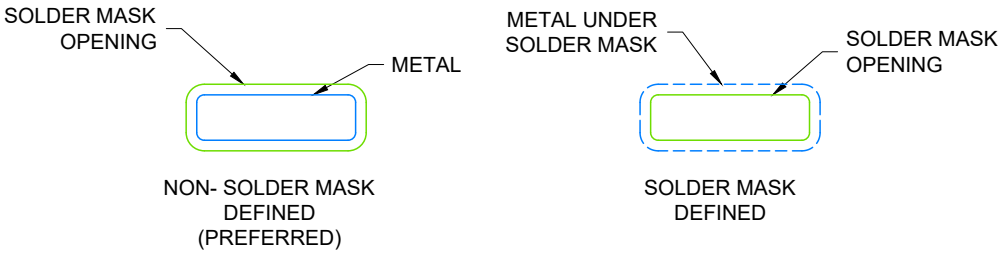


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

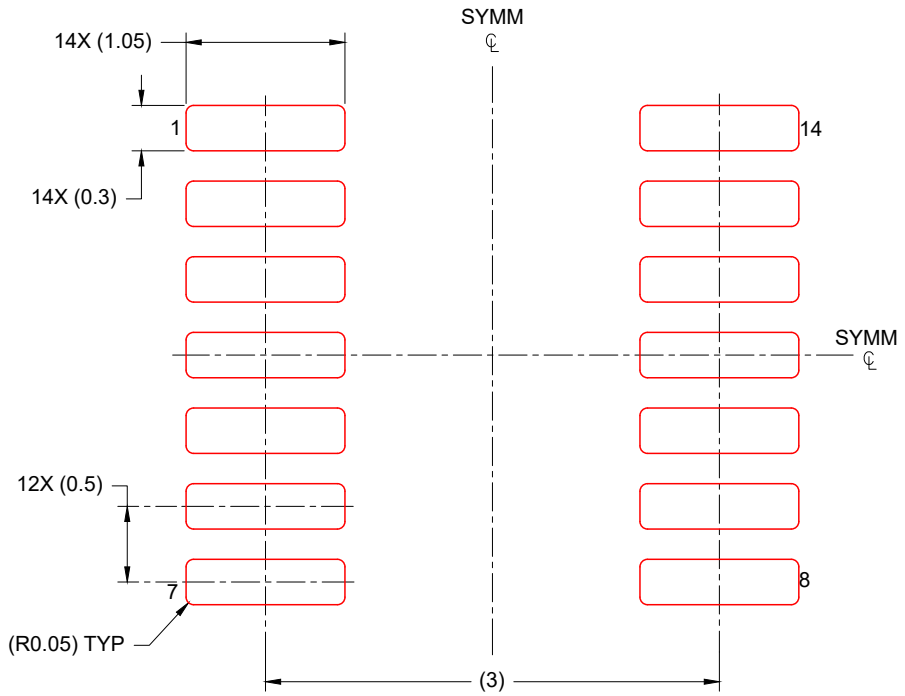


SOLDER MASK DETAILS

4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

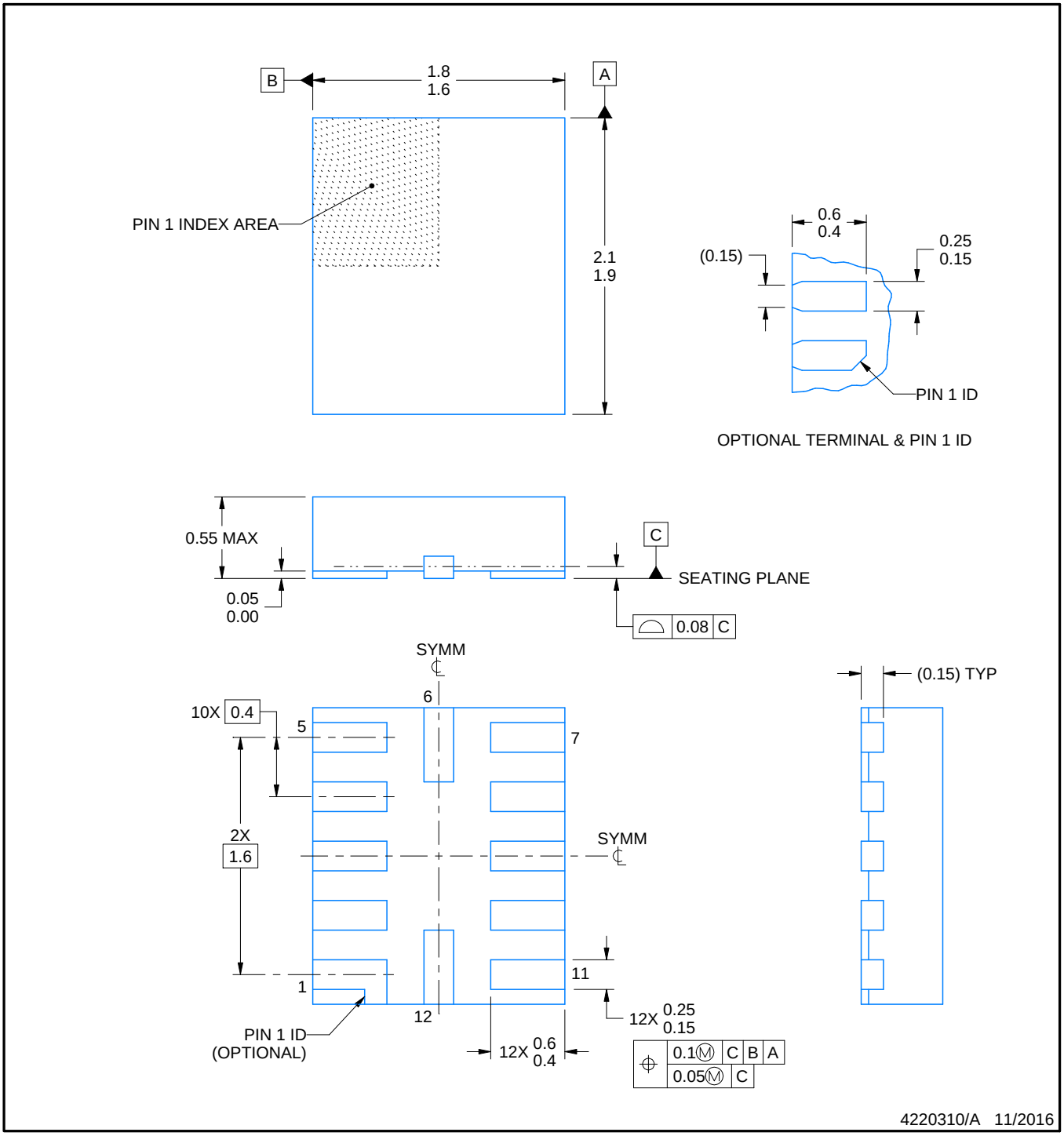
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RUT0012A

PACKAGE OUTLINE

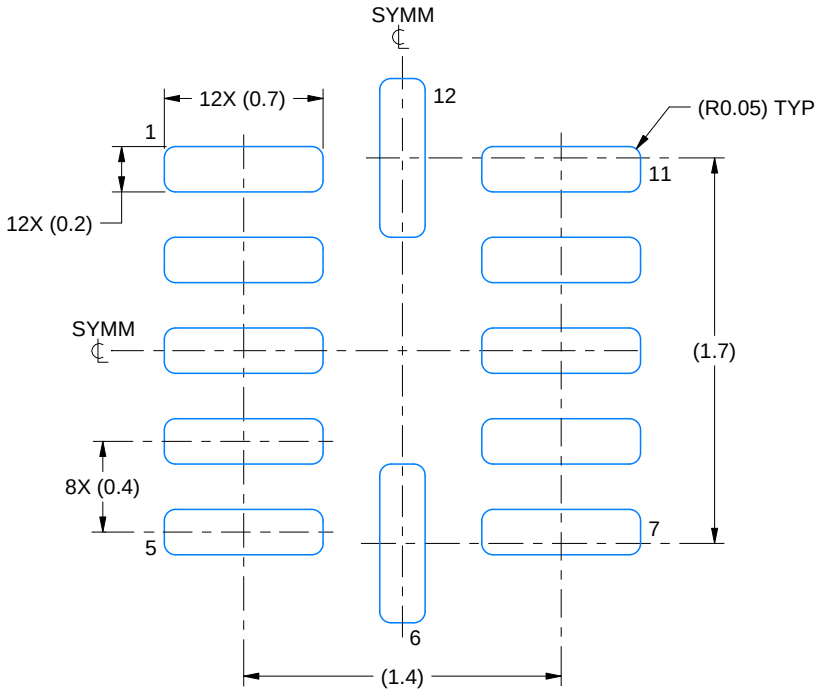
UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

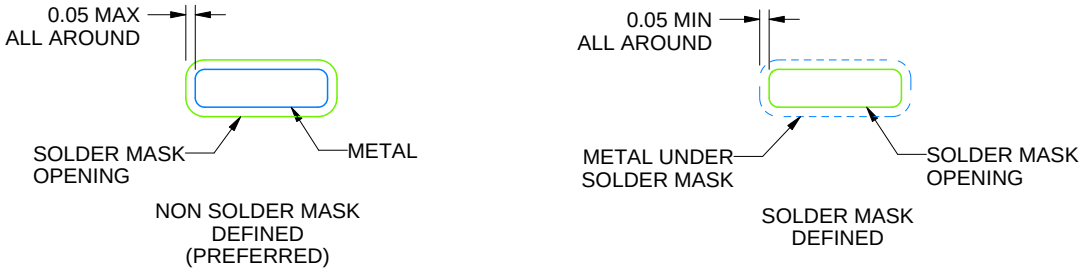


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

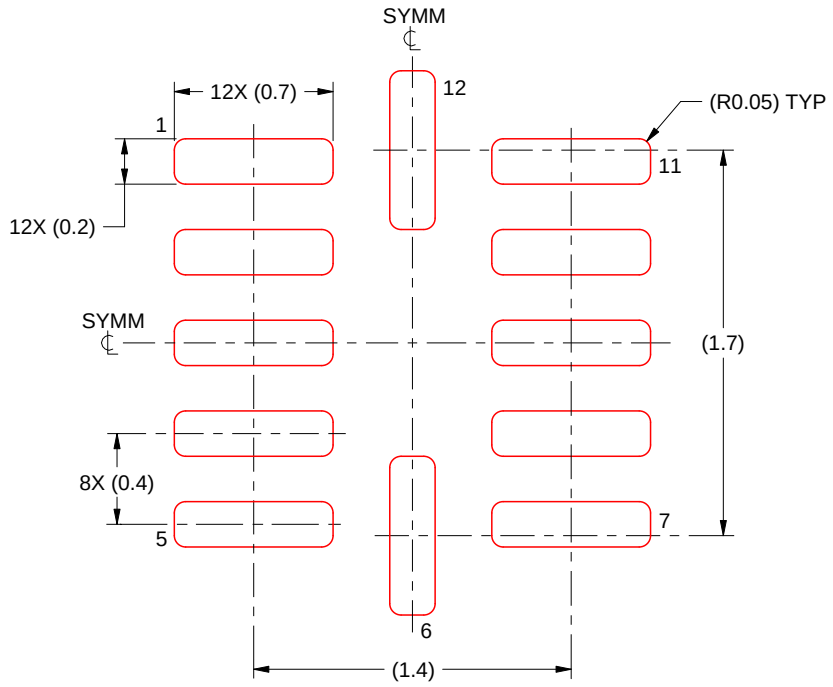


SOLDER MASK DETAILS

4220310/A 11/2016

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4220310/A 11/2016

NOTES: (continued)

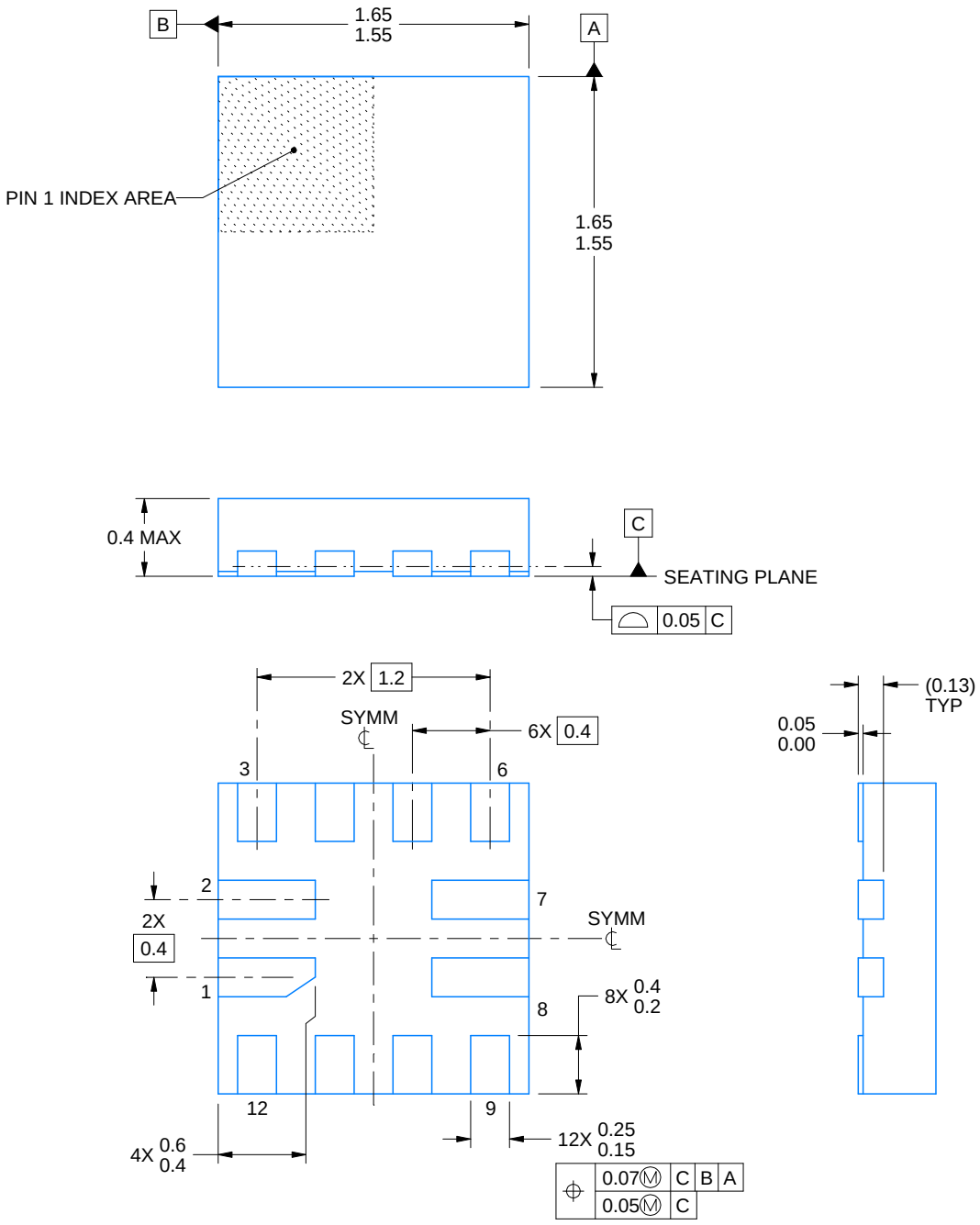
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RWB0012A

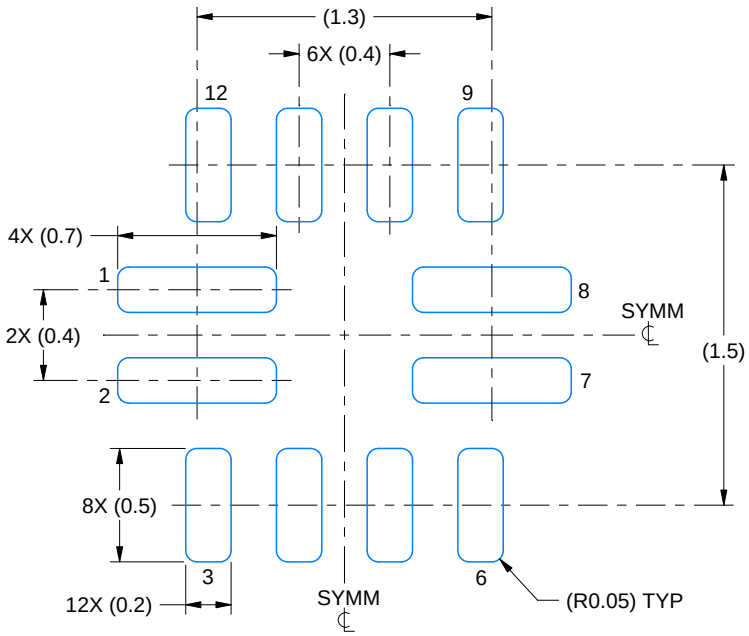
X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

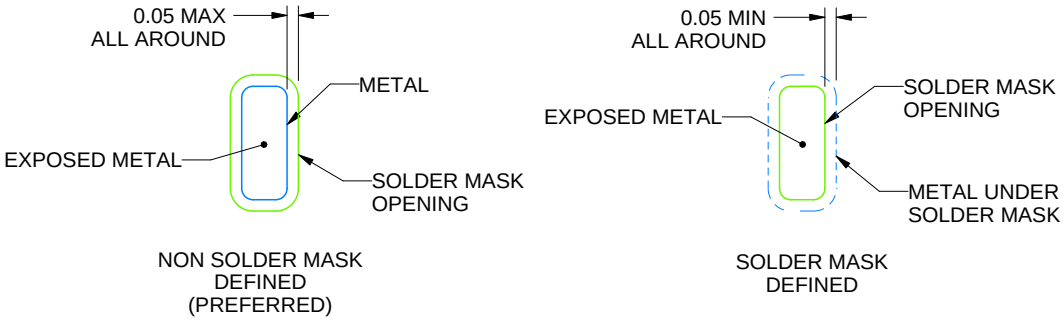


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS

4221631/B 07/2017

NOTES: (continued)

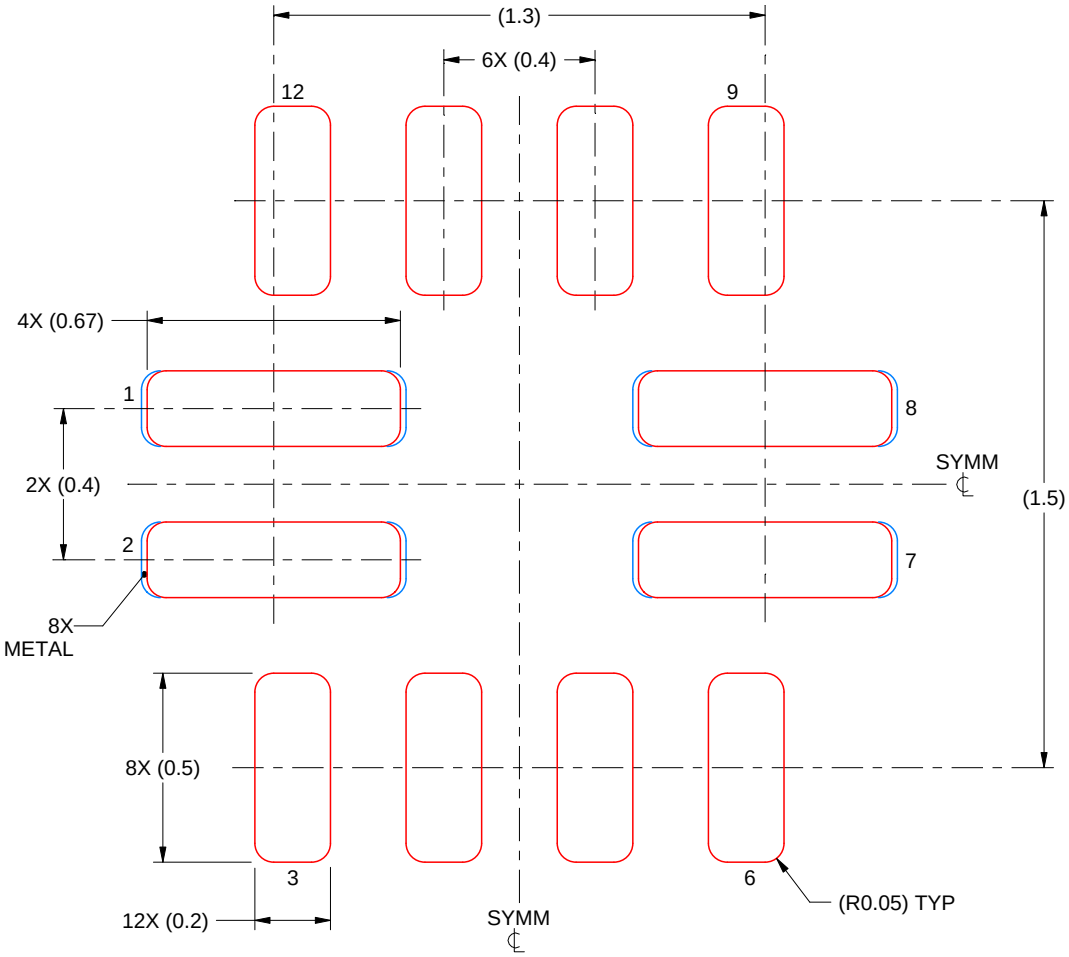
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RWB0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PADS 1,2,7 & 8
96% PRINTED SOLDER COVERAGE BY AREA
SCALE:50X

4221631/B 07/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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