

TXG4122 ±40V Bidirectional Ground-Level Translator for I2C

1 Features

- Bidirectional I2C compatible communication
- Support for Standard-mode, Fast-mode, and Fast-mode Plus I2C operation
- Supports DV shifts up to ±40V
- Data rate up to 1MHz
- Side 1 Supply Range: 3V to 5.5V
- Side 2 Supply Range: 2.25V to 5.5V
- Maximum capacitive load:
 - 80pF (Side 1) and 550pF (Side 2)
- Open -drain outputs with current sink capability:
 - 16.5mA (Side 1) and 30mA (Side 2)
- Low power consumption at 400kHz (typical):
 - $I_{CC1} = 4.2\text{mA}$, $I_{CC2} = 0.9\text{mA}$
- Operating temperature from -40°C to $+125^{\circ}\text{C}$
- CMTI of $2\text{kJ}/\mu\text{s}$
- Latch-up performance exceeds 100mA per JESD 78, class II
- ESD protection exceeds JESD 22
 - 2000V human-body model
 - 500V charged-device model
- Package options provided: SOIC (8D), WSON (8DSG), SOT-23 (8DDF)

2 Applications

- [Test and Measurement](#)
- [Factory Automation](#)
- [Appliances](#)
- [Personal Electronics](#)
- [Electric Power Steering](#)
- [Vehicle Control Unit](#)
- [Automotive Display](#)
- [Head Unit and Digital Cockpit](#)

3 Description

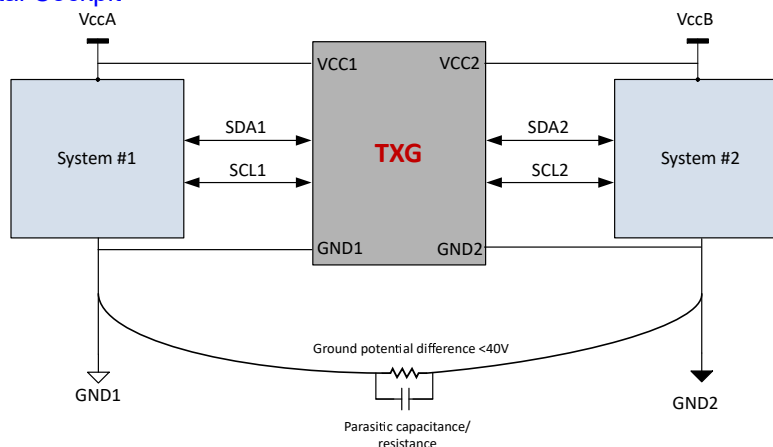
The TXG4122 device is a dual bidirectional, non-galvanic based voltage and ground-level translator for I2C. This device supports two separate configurable power-supply rails. Side 1 is designed to track VCC1 which accepts any supply voltage from 3V to 5.5V. Side 2 is designed to track VCC2 which accepts any supply voltage from 2.25V to 5.5V. Compared to traditional level shifters, the TXG4122 can solve the challenges of voltage translation across different ground levels up to ±40V. Both GND1 or GND2 can have an offset ground as long as the difference between GND1 and GND2 remains -40V to +40V.

The [Simplified Block Diagram](#) shows a common use case where DC shift occurs between GND1 to GND2 due to parasitic resistance or capacitance. The TXG4122 is able to support I2C-based communication between systems that have different supply voltages and different ground references. The leakage between GND1 and GND2 is typically 25nA when VCC to GND is shorted.

Package Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TXG4122	DSG (WSON-8)	2.00mm × 2.00mm
	DDF (SOT-8)	2.80mm × 2.90mm
	D (SOIC-8)	4.90mm × 3.90mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Block Diagram

Table of Contents

1 Features	1	8.2 Functional Block Diagram.....	15
2 Applications	1	8.3 Feature Description.....	16
3 Description	1	8.4 Device Functional Modes.....	16
4 Pin Configuration and Functions—TXG4122	3	9 Application and Implementation	17
5 Specifications	4	9.1 Application Information.....	17
5.1 Absolute Maximum Ratings.....	5	9.2 Typical Application.....	17
5.2 ESD Ratings.....	5	9.3 Power Supply Recommendations.....	18
5.3 Recommended Operating Conditions.....	6	9.4 Layout.....	18
5.4 Thermal Information.....	6	10 Device and Documentation Support	20
5.5 Electrical Characteristics.....	7	10.1 Documentation Support.....	20
5.6 Supply Current Characteristics.....	8	10.2 Receiving Notification of Documentation Updates..	20
5.7 Switching Characteristics, $V_{CCA} = 3.3 \pm 0.3V$	9	10.3 Support Resources.....	20
5.8 Switching Characteristics, $V_{CCA} = 5 \pm 0.5V$	10	10.4 Trademarks.....	20
5.9 Typical Characteristics.....	11	10.5 Electrostatic Discharge Caution.....	20
6 AC Noise Tolerance	13	10.6 Glossary.....	20
7 Parameter Measurement Information	14	11 Revision History	20
7.1 Load Circuit and Voltage Waveforms.....	14	12 Mechanical, Packaging, and Orderable Information	20
8 Detailed Description	15		
8.1 Overview.....	15		

4 Pin Configuration and Functions—TXG4122

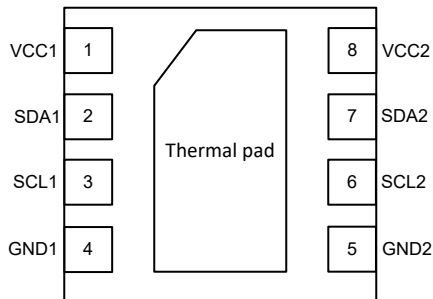


Figure 4-1. DSG 8-Pin WSON Top View

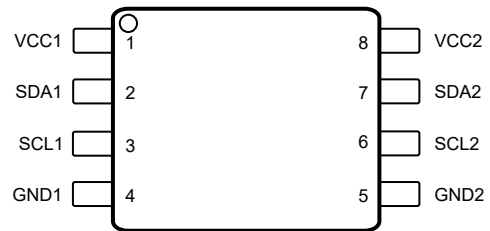


Figure 4-2. DDF Package 8-Pin SOT-23 and D Package 8-Pin SOIC Top View

Table 4-1. TXG4122 Pin Functions

NAME	PIN		I/O	DESCRIPTION
	DSG	DDF, D		
VCC1	1	1	—	Side 1 supply voltage
VCC2	8	8	—	Side 2 supply voltage
SDA1	2	2	I/O	Serial data input/output, side 1
SCL1	3	3	I/O	Serial clock input/output, side 1
SDA2	7	7	I/O	Serial data input/output, side 2
SCL2	6	6	I/O	Serial clock input/output, side 2
GND1	4	4	—	Ground reference for VCC1
GND2	5	5	—	Ground reference for VCC2
—	Thermal pad	—	—	Keep thermal pad floating.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC1} to V_{GND1}	Supply voltage to ground voltage, Side 1		-0.5	6.5	V
V_{CC2} to V_{GND2}	Supply voltage to ground voltage, Side 2		-0.5	6.5	V
V_{GND1} to V_{GND2}	V_{GND1} to V_{GND2}		-45	45	V
V_I	SDA1, SCL1	I/O Ports (Side 1) to V_{GND1}	-0.5	$V_{CC1} + 0.5$	V
	SDA2, SCL2	I/O Ports (Side 2) to V_{GND2}	-0.5	$V_{CC2} + 0.5$	
V_O	SDA1, SCL1	I/O Ports (Side 1) to V_{GND1}	-0.5	$V_{CC1} + 0.5$	V
	SDA2, SCL2	I/O Ports (Side 2) to V_{GND2}	-0.5	$V_{CC2} + 0.5$	
I_I	SDA1, SCL1	I/O Ports (Side 1) to V_{GND1}		20	mA
	SDA2, SCL2	I/O Ports (Side 2) to V_{GND2}		100	mA
I_O	SDA1, SCL1	I/O Ports (Side 1) to V_{GND1}		20	mA
	SDA2, SCL2	I/O Ports (Side 2) to V_{GND2}		100	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC1}	Supply voltage - V _{CC1} to GND1		3.0	5.5	V
V _{CC2}	Supply voltage - V _{CC2} to GND2		2.25	5.5	V
V _{GND1} to V _{GND2}	Voltage Between GND1 and GND2	Voltage Between GND1 and GND2	-40	40	V
V _{SDA1} , V _{SCL1}	I2C input and output signal voltages	Side 1	0	V _{CC1}	V
V _{SDA2} , V _{SCL2}	I2C input and output signal voltages	Side 2	0	V _{CC2}	V
V _{IL1}	Low-level input voltage	Side 1		622	mV
V _{IH1}	High-level input voltage	Side 1	0.7 × V _{CC1}		V
V _{IL2}	Low-level input voltage	Side 2		0.35 × V _{CC2}	V
V _{IH2}	High-level input voltage	Side 2	0.47 × V _{CC2}		V
I _{OL1}	Low-level output current	Side 1		16.5	mA
I _{OL2}	Low-level output current	Side 2		30	mA
C1	Capacitive load	Side 1		80	pF
C2	Capacitive load	Side 2		550	pF
f _{MAX}	I2C operating frequency ⁽¹⁾			1	MHz
T _A	Operating free-air temperature		-40	125	°C

- (1) Maximum frequency is a function of the RC time constant on the bus. If the system has less bus capacitance, then higher frequencies can be achieved.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TXGx122	UNIT
		D (SOIC)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	118.40	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	54.00	°C/W
R _{θJB}	Junction-to-board thermal resistance	62.48	°C/W
Y _{JT}	Junction-to-top characterization parameter	13.00	°C/W
Y _{JB}	Junction-to-board characterization parameter	61.72	°C/W
R _{θJC(bottom)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	Operating free-air temperature (T _A)			UNIT
			–40°C to 125°C			
			MIN	TYP	MAX	
V _{ILT1}	Voltage input threshold low (SDA1 and SCL1)		463		622	mV
V _{IHT1}	Voltage input threshold high (SDA1 and SCL1)		505		678	mV
V _{HYST1}	Voltage input hysteresis	V _{IHT1} - V _{ILT1}	42			mV
V _{OL1}	Low-level output voltage (SDA1 and SCL1)	0.5mA ≤ (I _{SDA1} and I _{SCL1}) ≤ 16.5mA			787	mV
ΔV _{OIT1}	Low-level output voltage to high-level input voltage threshold difference, SDA1 and SCL1	0.5mA ≤ (I _{SDA1} and I _{SCL1}) ≤ 16.5mA	57			mV
V _{ILT2}	Voltage input threshold low (SDA2 and SCL2)		0.34 × V _{CC2}		0.36 × V _{CC2}	V
V _{IHT2}	Voltage input threshold high (SDA2 and SCL2)		0.47 × V _{CC2}		0.49 × V _{CC2}	V
V _{HYST2}	Voltage input hysteresis	V _{IHT2} - V _{ILT2}	0.12 × V _{CC2}			V
V _{OL2}	Low-level output voltage	0.5mA ≤ (I _{SDA1} and I _{SCL1}) ≤ 30mA			452	mV
I _{I (Side 1)}	Input leakage current (SDA1, SCL1)	V _{SDA1} , V _{SCL1} = V _{CC1} = 5.5V			0.71	μA
I _{I (Side 2)}	Input leakage current (SDA2, SCL2)	V _{SDA2} , V _{SCL2} = V _{CC2} = 5.5V			0.15	μA
C _i	Input capacitance to local ground	V _I = 0.4 × sin(2E6*πt) + V _{DDX} / 2 V _O = V _{CC}			20	pF
C _{GND}	Cap between grounds	All channels combined (V _{CC} both sides are powered on)			49	pF
		All channels combined (V _{CC} to GND shorted)			58	pF
Leakage	Current Leakage between GND1 and GND2	All channels combined (VCC to GND shorted)		25	52	nA
		All channels combined (VCC both sides are powered on and inputs are all high)		17	52	nA
		All channels combined (VCC both sides are powered on and inputs are all low)		23	42	μA
CMT1	Common Mode Transient Immunity	Input toggling at 1Mbps Ground shift up to 40V			2	kV/μs
V _{UVLO+}	Positive-Going Undervoltage Lockout Voltage	Side 1			2.9	V
		Side 2			2.3	V
V _{UVLO-}	Negative-Going Undervoltage Lockout Voltage	Side 1	2.2			V
		Side 2	1.6			V
V _{UVLO_Hys}	Undervoltage Lockout Hysteresis	Side 1	43.9			mV
		Side 2	94.3			mV

5.6 Supply Current Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC1}	V _{CC2}	Operating free-air temperature (T _A)			UNIT
					–40°C to 125°C			
					MIN	TYP	MAX	
I _{CC1}	Supply current, Side 1	SDA1/SCL1 = V _{CC1}	3V – 5.5V	2.25V – 5.5V	2.2	3.1	mA	
		SDA1/SCL1 = GND1			2.8	4.3	mA	
		SDA1/SCL1 = 400kHz square wave R1 = 300Ω, C1 = 80pF			2.7	4.2	mA	
I _{CC2}	Supply current, Side 2	SDA2/SCL2 = V _{CC2}	3V – 5.5V	2.25V – 5.5V	0.44	0.8	mA	
		SDA2/SCL2 = GND2			0.6	1.1	mA	
		SDA2/SCL2 = 400kHz square wave R2 = 220Ω, C2 = 550pF			0.53	0.9	mA	
I _{CC1}	Supply current, Side 1	VSDA1, VSCL1 = GND1, VSDA2, VSCL2 = GND2, R1 and R2 = Open, C1 and C2 = Open	3.3V	3.3V	2.8	3.7	mA	
		VSDA1, VSCL1 = V _{CC1} , VSDA2, VSCL2 = V _{CC2} , R1 and R2 = Open, C1 and C2 = Open			2.2	2.9	mA	
I _{CC2}	Supply current, Side 2	VSDA1, VSCL1 = GND1, VSDA2, VSCL2 = GND2, R1 and R2 = Open, C1 and C2 = Open	3.3V	3.3V	0.62	0.9	mA	
		VSDA1, VSCL1 = V _{CC1} , VSDA2, VSCL2 = V _{CC2} , R1 and R2 = Open, C1 and C2 = Open			0.5	0.7	mA	
I _{CC1}	Supply current, Side 1	VSDA1, VSCL1 = GND1, VSDA2, VSCL2 = GND2, R1 and R2 = Open, C1 and C2 = Open	5V	5V	3.1	4.1	mA	
	Supply current, Side 1	VSDA1, VSCL1 = V _{CC1} , VSDA2, VSCL2 = V _{CC2} , R1 and R2 = Open, C1 and C2 = Open			2.3	3	mA	
I _{CC2}	Supply current, Side 2	VSDA1, VSCL1 = GND1, VSDA2, VSCL2 = GND2, R1 and R2 = Open, C1 and C2 = Open	5V	5V	0.7	1	mA	
	Supply current, Side 2	VSDA1, VSCL1 = V _{CC1} , VSDA2, VSCL2 = V _{CC2} , R1 and R2 = Open, C1 and C2 = Open			0.5	0.8	mA	

5.7 Switching Characteristics, $V_{CCA} = 3.3 \pm 0.3V$

over recommended operating conditions, unless otherwise noted

PARAMETER	Test Conditions	Supply Voltage Side 2 (V_{CC2})									UNIT		
		2.5 ± 0.25V			3.3 ± 0.3V			5.0 ± 0.5V					
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
t_{r1}	Output signal fall time (SDA1, SCL1)	0.7 × $V_{CC1} \geq V_O \geq 0.3 \times V_{CC1}$, R1 = 300Ω, C1 = 80pF		42			42			42			ns
		0.9 × $V_{CC1} \geq V_O \geq 900$ mV, R1 = 300Ω, C1 = 80pF		69			69			69			ns
t_{r2}	Output signal fall time (SDA2, SCL2)	0.7 × $V_{CC2} \geq V_O \geq 0.3 \times V_{CC2}$, R2 = 220Ω, C2 = 550pF		64			26			36			ns
		0.9 × $V_{CC2} \geq V_O \geq 400$ mV, R2 = 220Ω, C2 = 550pF		51			76			156			ns
t_{r1}	Output signal rise time (SDA1, SCL1)	0.7 × $V_{CC1} \geq V_O \geq 0.3 \times V_{CC1}$, R1 = 300Ω, C1 = 80pF		23			23			23			ns
t_{r2}	Output signal rise time (SDA2, SCL2)	0.7 × $V_{CC2} \geq V_O \geq 0.3 \times V_{CC2}$, R2 = 220Ω, C2 = 550pF		109			109			109			ns
t_{pLH1-2}	Low-to-high propagation delay, side 1 to side 2	$V_I = 535$ mV, $V_O = 0.7 \times V_{CC2}$, R1 = 300Ω, R2 = 220Ω, C1 = 80pF, C2 = 550pF		272			272			271			ns
t_{pHL1-2}	High-to-low propagation delay, side 1 to side 2	$V_I = 550$ mV, $V_O = 0.3 \times V_{CC2}$, R1 = 300Ω, R2 = 220Ω, C1 = 80pF, C2 = 550pF		139			178			124			ns
t_{pLH2-1}	Low-to-high propagation delay, side 2 to side 1	$V_I = 0.4 \times V_{CC2}$, $V_O = 0.7 \times V_{CC1}$, R1 = 300Ω, R2 = 220Ω, C1 = 80pF, C2 = 550pF		143			153			138			ns
t_{pHL2-1}	High-to-low propagation delay, side 2 to side 1	$V_I = 0.4 \times V_{CC2}$, $V_O = 0.3 \times V_{CC1}$, R1 = 300Ω, R2 = 220Ω, C1 = 80pF, C2 = 550pF		236			208			188			ns
PWD_{1-2}	Pulse width distortion $ t_{pHL1-2} - t_{pLH1-2} $	R1 = 300Ω, R2 = 220Ω, C1 = 80pF, C2 = 550pF		187			177			193			ns
PWD_{2-1}	Pulse width distortion $ t_{pHL2-1} - t_{pLH2-1} $	R1 = 300Ω, R2 = 220Ω, C1 = 80pF, C2 = 550pF		52			85			73			ns
t_{LOOP1}	Round-trip propagation delay on side 1	0.4V ≤ $V_I \leq 0.3 \times V_{CC1}$, R1 = 300Ω, C1 = 80pF, R2 = 220Ω, C2 = 550pF		314			300			303			ns

5.8 Switching Characteristics, $V_{CCA} = 5 \pm 0.5V$

over recommended operating conditions, unless otherwise noted

PARAMETER		Test Conditions	Supply Voltage Side 2 (V_{CC2})									UNIT
			2.5 ± 0.25V			3.3 ± 0.3V			5.0 ± 0.5V			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{f1}	Output signal fall time (SDA1, SCL1)	$0.7 \times V_{CC1} \geq V_O \geq 0.3 \times V_{CC1}$, R1 = 300Ω, C1 = 80pF			67			67			67	ns
		$0.9 \times V_{CC1} \geq V_O \geq 900mV$, R1 = 300Ω, C1 = 80pF			122			122			123	ns
t_{f2}	Output signal fall time (SDA2, SCL2)	$0.7 \times V_{CC2} \geq V_O \geq 0.3 \times V_{CC2}$, R2 = 220Ω, C2 = 550pF			64			26			36	ns
		$0.9 \times V_{CC2} \geq V_O \geq 400mV$, R2 = 220Ω, C2 = 550pF			52			76			156	ns
t_{r1}	Output signal rise time (SDA1, SCL1)	$0.7 \times V_{CC1} \geq V_O \geq 0.3 \times V_{CC1}$, R1 = 300Ω, C1 = 80pF			23			23			23	ns
t_{r2}	Output signal rise time (SDA2, SCL2)	$0.7 \times V_{CC2} \geq V_O \geq 0.3 \times V_{CC2}$, R2 = 220Ω, C2 = 550pF			109			109			109	ns
t_{pLH1-2}	Low-to-high propagation delay, side 1 to side 2	$V_I = 535mV$, $V_O = 0.7 \times V_{CC2}$, R1 = 300Ω, R2 = 220Ω, C1 = 80pF, C2 = 550pF			284			283			283	ns
t_{pHL1-2}	High-to-low propagation delay, side 1 to side 2	$V_I = 550mV$, $V_O = 0.3 \times V_{CC2}$, R1 = 300Ω, R2 = 220Ω, C1 = 80pF, C2 = 550pF			125			164			110	ns
t_{pLH2-1}	Low-to-high propagation delay, side 2 to side 1	$V_I = 0.4 \times V_{CC2}$, $V_O = 0.7 \times V_{CC1}$, R1 = 300Ω, R2 = 220Ω, C1 = 80pF, C2 = 550pF			148			157			143	ns
t_{pHL2-1}	High-to-low propagation delay, side 2 to side 1	$V_I = 0.4 \times V_{CC2}$, $V_O = 0.3 \times V_{CC1}$, R1 = 300Ω, R2 = 220Ω, C1 = 80pF, C2 = 550pF			249			222			202	ns
PWD_{1-2}	Pulse width distortion $ t_{pHL1-2} - t_{pLH1-2} $	R1 = 300Ω, R2 = 220Ω, C1 = 80pF, C2 = 550pF			205			194			210	ns
PWD_{2-1}	Pulse width distortion $ t_{pHL2-1} - t_{pLH2-1} $	R1 = 300Ω, R2 = 220Ω, C1 = 80pF, C2 = 550pF			59			92			80	ns
t_{LOOP1}	Round-trip propagation delay on side 1	$0.4V \leq V_I \leq 0.3 \times V_{CC1}$, R1 = 300Ω, C1 = 80pF, R2 = 220Ω, C2 = 550pF			330			315			319	ns

5.9 Typical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

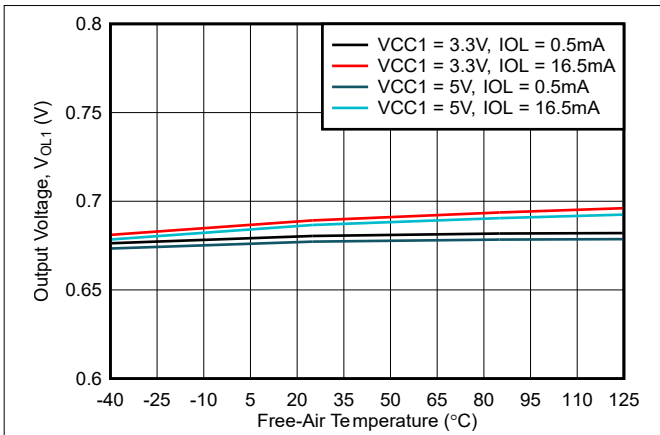


Figure 5-1. Side 1: Output Low Voltage vs Free-Air Temperature

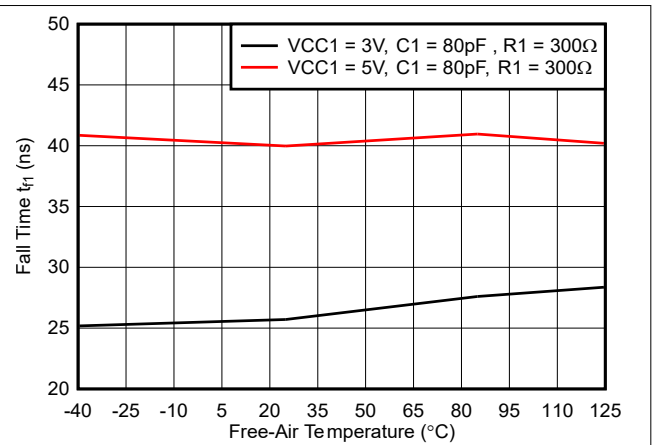


Figure 5-2. Side 1: Output Fall Time vs Free-Air Temperature

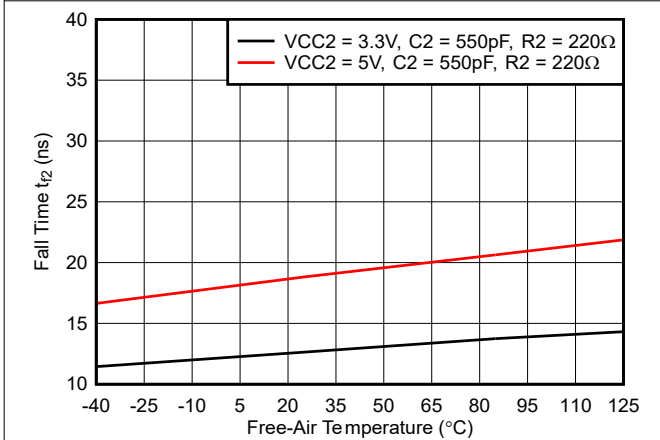


Figure 5-3. Side 2: Output Fall Time vs Free-Air Temperature

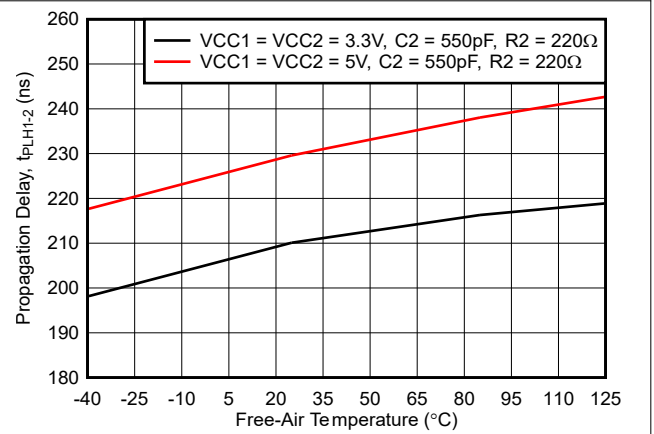


Figure 5-4. Propagation Delay, T_{PLH1-2} , vs Temperature

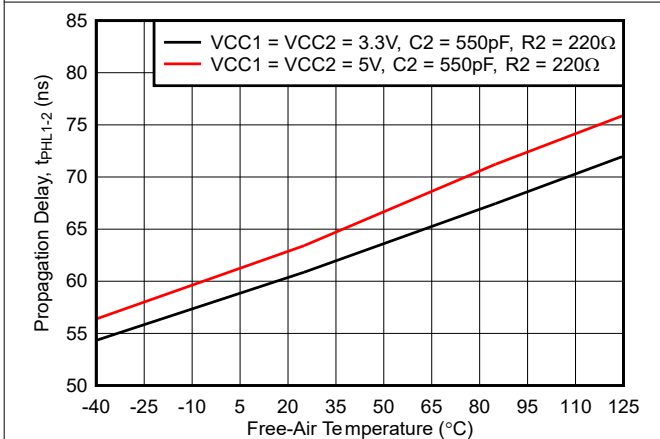


Figure 5-5. Propagation Delay, T_{PHL1-2} , vs Temperature

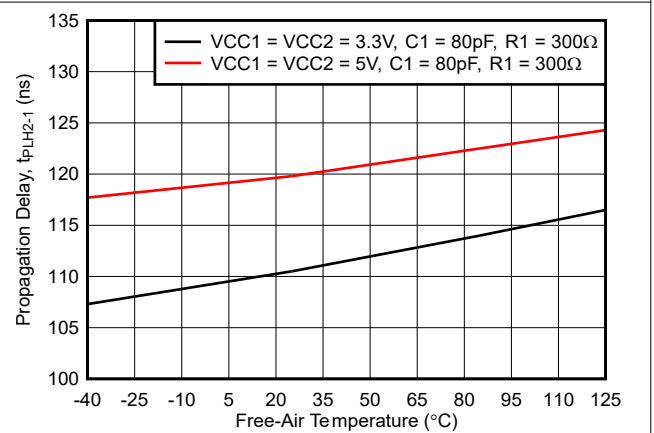


Figure 5-6. Propagation Delay, T_{PLH2-1} , vs Temperature

5.9 Typical Characteristics (continued)

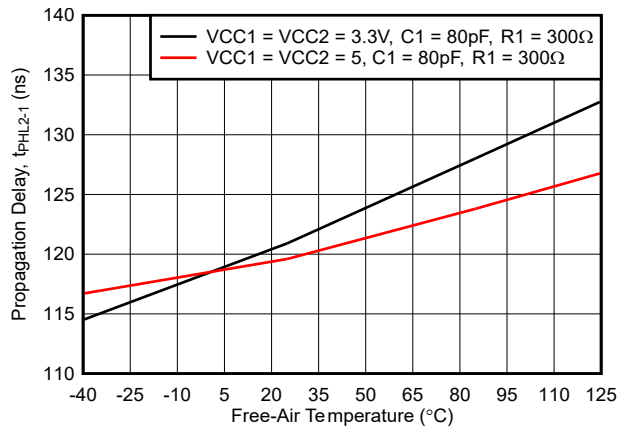


Figure 5-7. Propagation Delay, T_{PHL2-1} , vs Temperature

6 AC Noise Tolerance

TXGx122 supports I/O voltage translation in environments with noisy grounds. The plot below illustrates the amount of noise that GND1 and GND2 can reject in terms peak-to-peak voltage over frequency without disrupting communication between two systems.

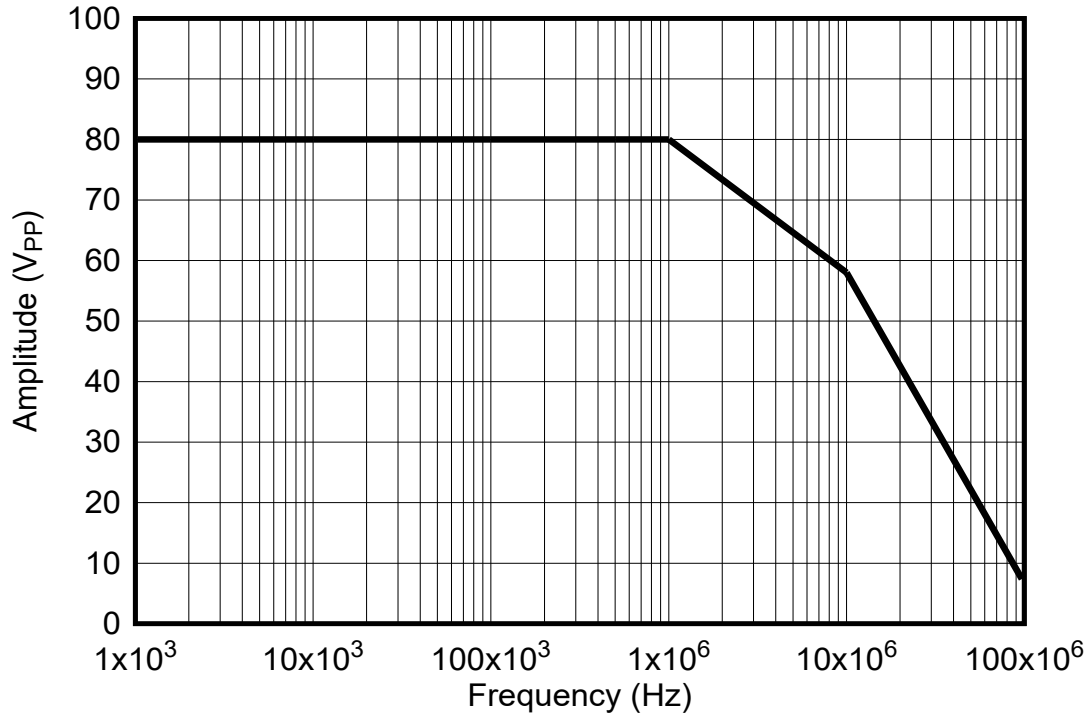


Figure 6-1. Noise Immunity

7 Parameter Measurement Information

7.1 Load Circuit and Voltage Waveforms

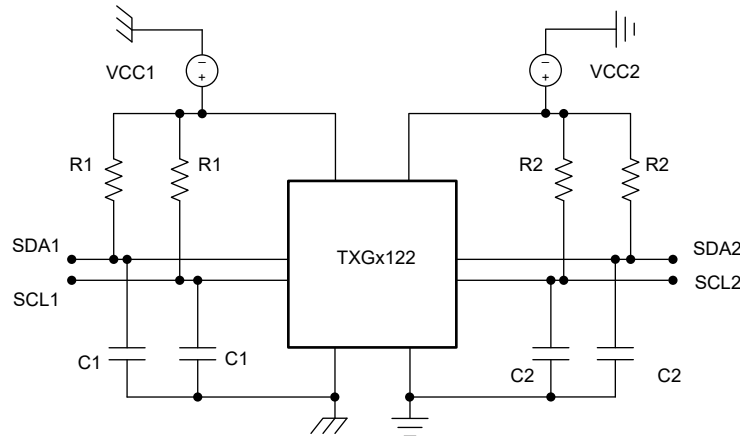


Figure 7-1. Test Circuit

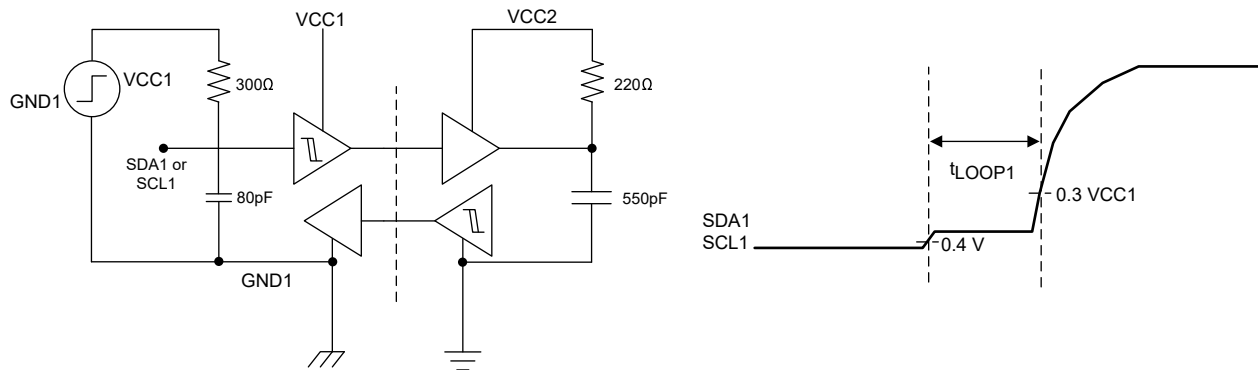


Figure 7-2. t_{LOOP1} Setup and Timing Diagram

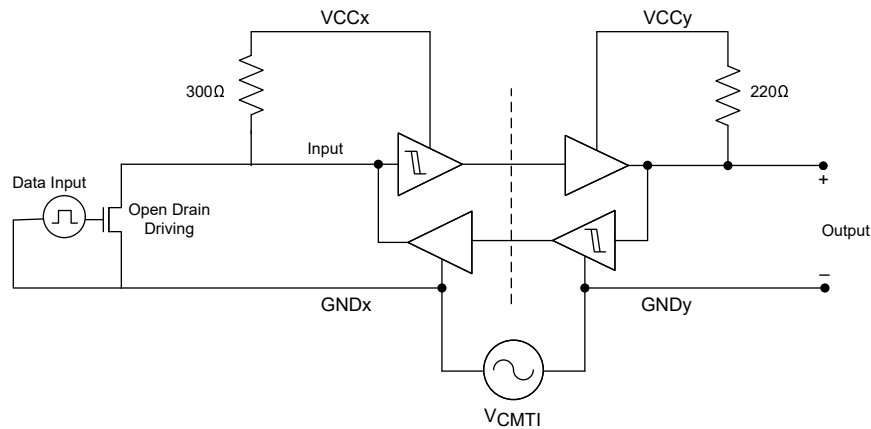


Figure 7-3. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

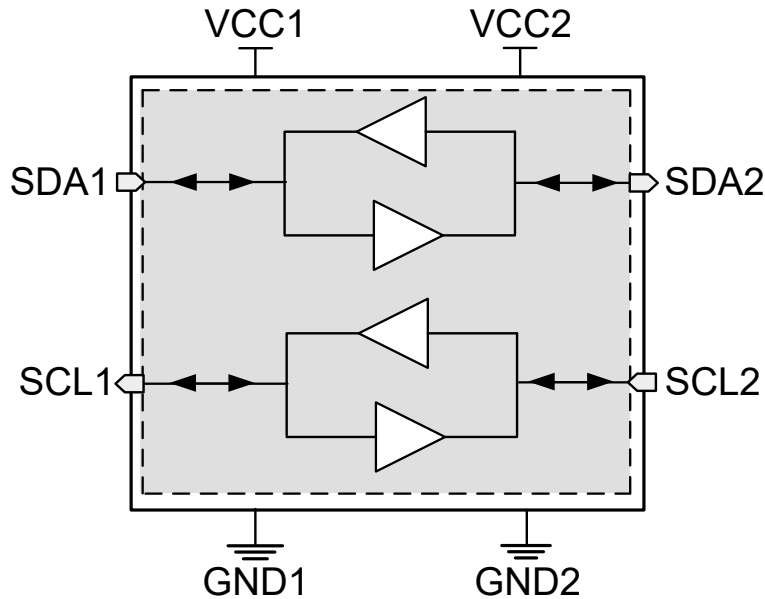
The TXG4122 is a dual bidirectional translator intended for I2C or SMBus systems. This translator is able to support logic-level shifting and ground-level shifting up to $\pm 40V$. As with standard I2C systems, SDA and SCL I/O lines are open-drain and require external pull-up resistors to the systems's supply rail.

- Idle state: When no device drives the bus, the pull-up resistors force SDA and SCL high, representing a logic '1'
- Active low: Any device can assert a logic '0' by pulling the respective line to ground.

Select the pull-up resistor value so the I2C rise-time specification is met for the measured bus capacitance and supply voltage. For more information, see [I2C Bus Pullup Resistor Calculation](#). TXG4122 can support Standard-mode ($\leq 100kHz$), Fast-mode ($\leq 400kHz$), and Fast-mode Plus ($\leq 1MHz$).

The Side 1 of this device works from 3V to 5.5V and Side 2 works from 2.25V to 5.5V. For best signal integrity, connect Side 1 (SDA1, SCL1) to the host controller – the MCU, SoC, or any single-master node. Connect Side 2 (SDA2, SCL2) to the shared I2C bus that links multiple peripherals. The maximum load on Side 1 is $\leq 80pF$ and maximum load on Side 2 is $\leq 550pF$.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bidirectional Level Translation

The TXG4122 can provide bidirectional voltage level translation (up-translation and down-translation) in mixed-mode applications. It is operational from 3V to 5.5V on Side 1 and 2.25V to 5.5V on Side 2.

8.4 Device Functional Modes

Table 8-1. Function Table

VCC1 ⁽¹⁾	VCC2	SDA1/SCL1	SDA2/SCL2
> UVLO	> UVLO	H or Open	H or Open
		L	L
< UVLO	> UVLO	High-Z	H or Open
> UVLO	< UVLO	H or Open	High-Z
< UVLO	< UVLO	High-Z	High-Z

(1) > UVLO = VCC above the UVLO threshold; < UVLO = VCC below the UVLO threshold; L = Low; H or Open = High or Released; High-Z = High Impedance

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TXG4122 is used for level translation, enabling communication between devices or systems operating at different interface and ground voltages. The TXG4122 device is ideal for use in applications where an open-drain driver is connected to the data I/Os. Figure 9-1 is an example of two systems that translate from 3.3V to 5.5V across an I2C interface while also seeing a ground shift of -1V on GND2 while GND1 remains at 0V.

9.2 Typical Application

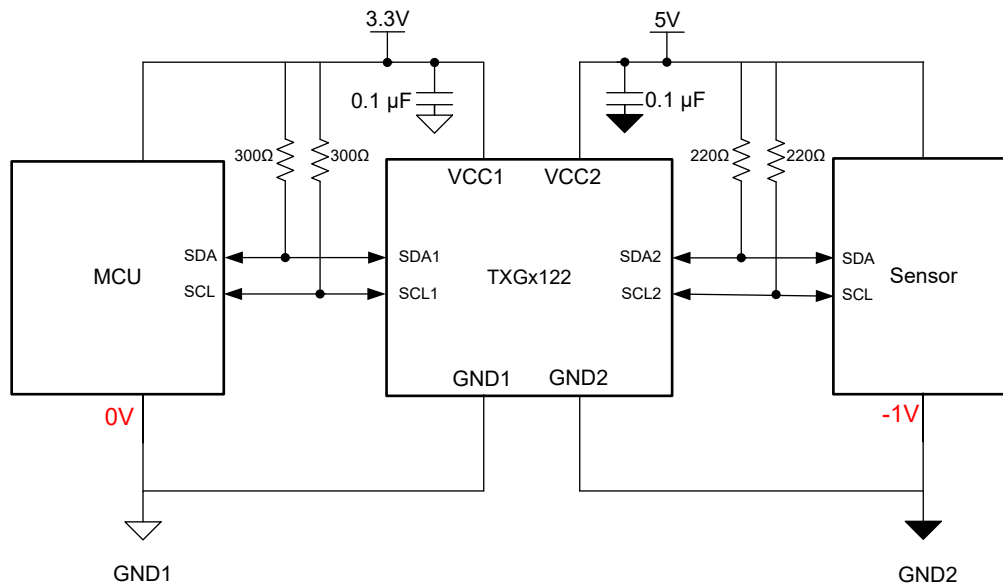


Figure 9-1. TXG4122 in Industrial Applications

9.2.1 Design Requirements

Use the parameters listed in Table 9-1 for this design example.

Table 9-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
SDA1/SCL1	3V to 5.5V
SDA2/SCL2	2.25V to 5.5V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Supply Voltage Selection
 - Set VCC1 to the supply of the Side 1 domain (3.0 to 5.5V) and VCC2 to the supply of the Side 2 domain (2.25V to 5.5V). These ranges are assymmetric.
 - Pull-up resistors on each side must be connected to that side's VCC so that the logic-high level matches the local domain voltage.
- Pull-up Resistor Selection (RP)
 - Side 1 and Side 2 have different sink current limits (IOL1 = 16.5mA, IOL2 = 30mA) and different maximum capacitive loads (C1 = 80pF, C2 = 550pF), so the pull-up resistor must be selected independently for each side.
 - For each side, verify that VCC / RP does not exceed the rated IOL and that the rise time meets the I2C specifications for the target bus speed.
- Ground Offset Voltage
 - The DC offset between GND1 and GND2 must not exceed $\pm 40V$. For dynamic ground shifts, ensure dv/dt stays below the CMTI rating of 2kV/ μs .
 - Ensure the supply voltage on each side does not exceed 5.5V above its local ground reference (VCC1 to GND1 $\leq 5.5V$ and VCC2 to GND2 $\leq 5.5V$ - per Recommended Operating Conditions). This constraint is independent of the ground offset between GND1 and GND2.

9.2.3 Application Curve

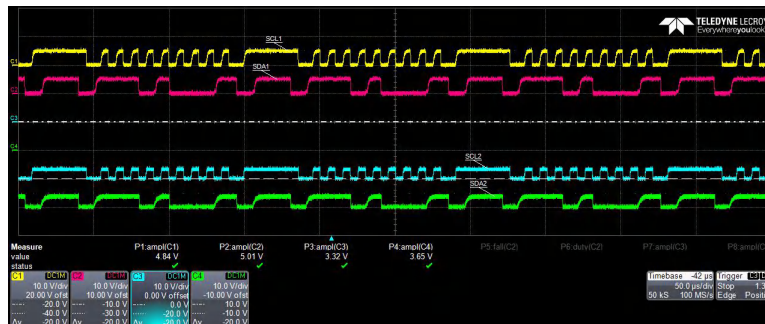


Figure 9-2. Down Translation at 1 MHz (5V to 3.3V) with Ground Shift of -20V

9.3 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate. Please make sure the difference between VCC and GND remains at 5.5V at all times (per Recommended Operating Conditions).

9.4 Layout

9.4.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible. A 0.1 μF capacitor is recommended, but transient performance can be improved by having 1 μF and 0.1 μF capacitors in parallel as bypass capacitors.
- A 0.1 μF capacitor can be added between GND1 and GND2 to improve performances of CMTI.

9.4.2 Layout Example

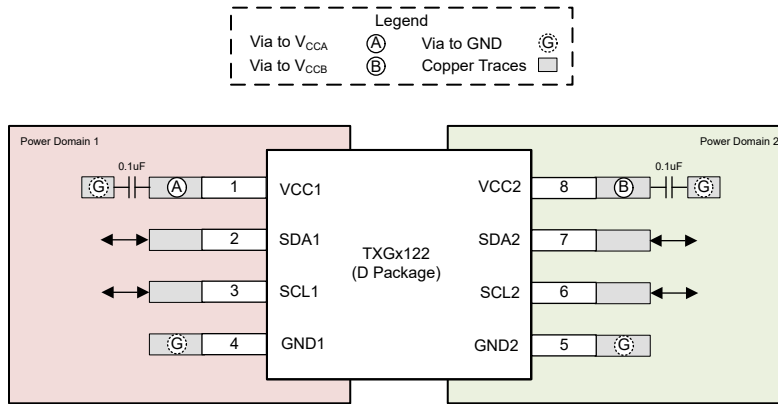


Figure 9-3. Layout Example – TXG4122

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Understanding Schmitt Triggers application report](#)
- Texas Instruments, [CMOS Power Consumption and \$C_{pd}\$ Calculation application report](#)

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2026	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXG4122DR	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TG4122

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

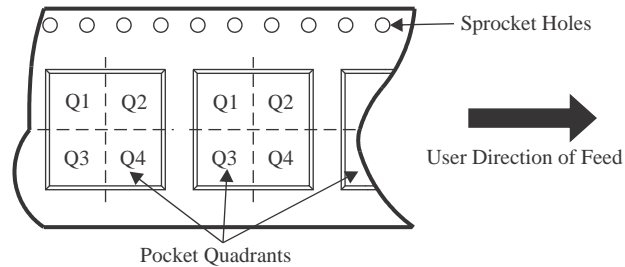
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXG4122DR	SOIC	D	8	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXG4122DR	SOIC	D	8	3000	340.5	336.1	32.0



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025