Application Brief

Using a Watchdog Timer Within TPLD

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What is a Watchdog Timer?

A watchdog timer (WDT) is a timer that is used to monitor signals for switching. The primary purpose of a WDT is to prevent a system from becoming stuck in an infinite loop, hanging, or experiencing a runtime error that can cause the system to become unresponsive. Many synchronous systems have some kind of watchdog timer installed, such as microcontrollers, or CPUs have watch dog timers built in.

How to Setup a Watchdog Timer in InterConnect Studio

InterConnect Studio (ICS) is a software tool used to design, simulate, and configure the TPLD family of devices.

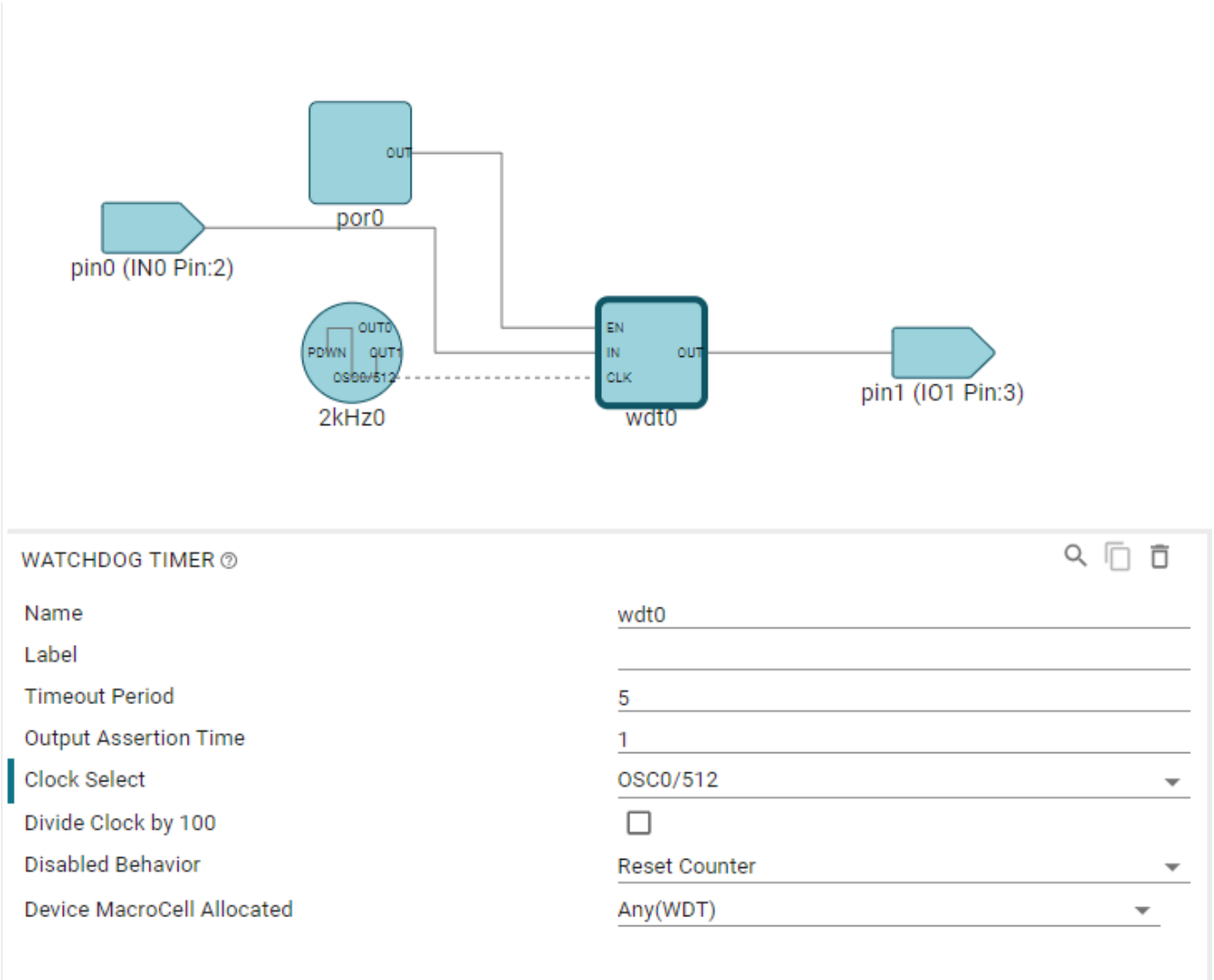

Figure 1. Basic Usage of WDT

Figure 1 shows the initial state of a watchdog timer within ICS. The three most important settings are *timeout period*, *output assertion time*, and *clock select*. Timeout period refers to how long the watchdog waits to detect an edge from input IN. Output assertion time is how long the output of the WDT outputs logic LOW before resetting. Both of these values are integers for a counter to count through, so the clock select is the determining factor for the scale at which the aforementioned settings are based on.

- **EN** – The EN port (enable) turns on the WDT. While this port is logic LOW the WDT is inactive and outputs LOW.
- **IN** – The IN port is the signal to be monitored by the WDT.
- **CLK** – The CLK port is a visual representation of the internal clock going into the WDT. Since there is no external clock option for the watchdog timer the only way to adjust this value is through the *Clock Select* setting.
- **OUT** – The OUT port is the result of the monitoring. If the input signal is meeting the monitored timing, the port is logic HIGH, but once the WDT triggers, the OUT port is a single pulse of logic LOW.

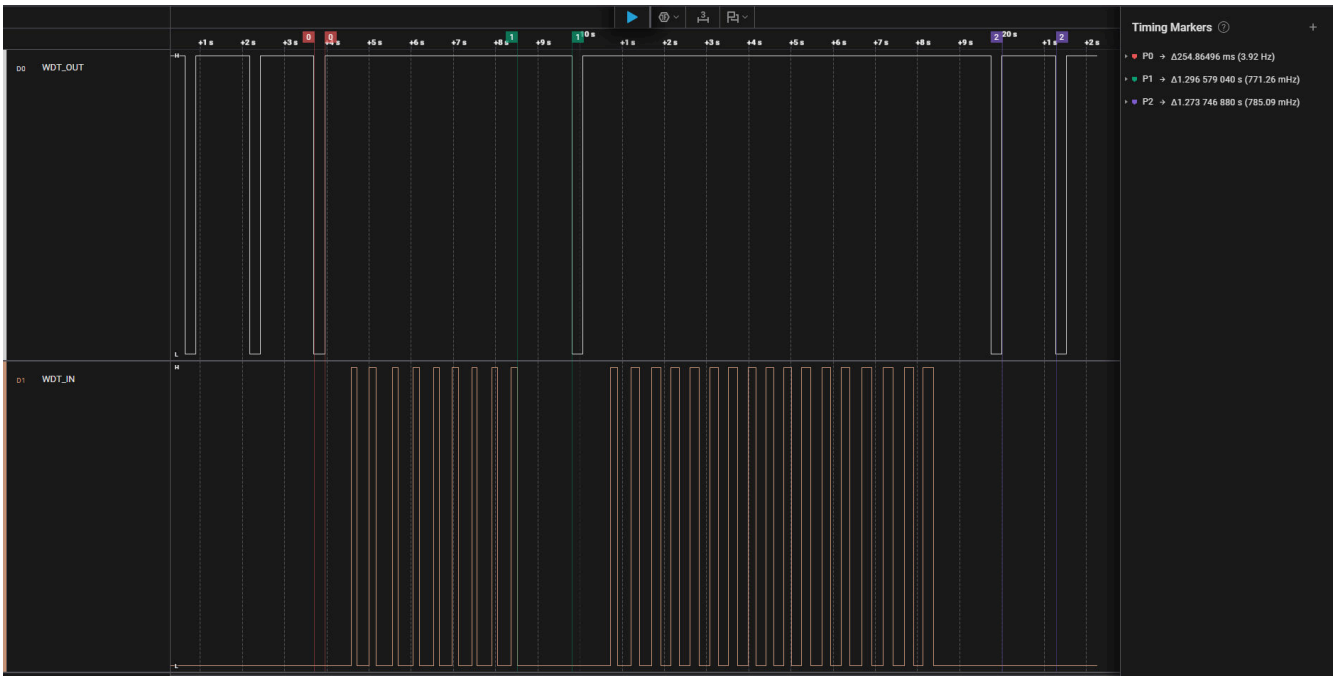

Figure 2. Basic WDT Waveforms

Figure 2 shows the basic WDT waveform where P0 is the output assertion time, and P1 and P2 are the timeout period. Figure 3 shows increasing the output assertion time and Figure 4 shows increasing both the output assertion time and the timeout period.

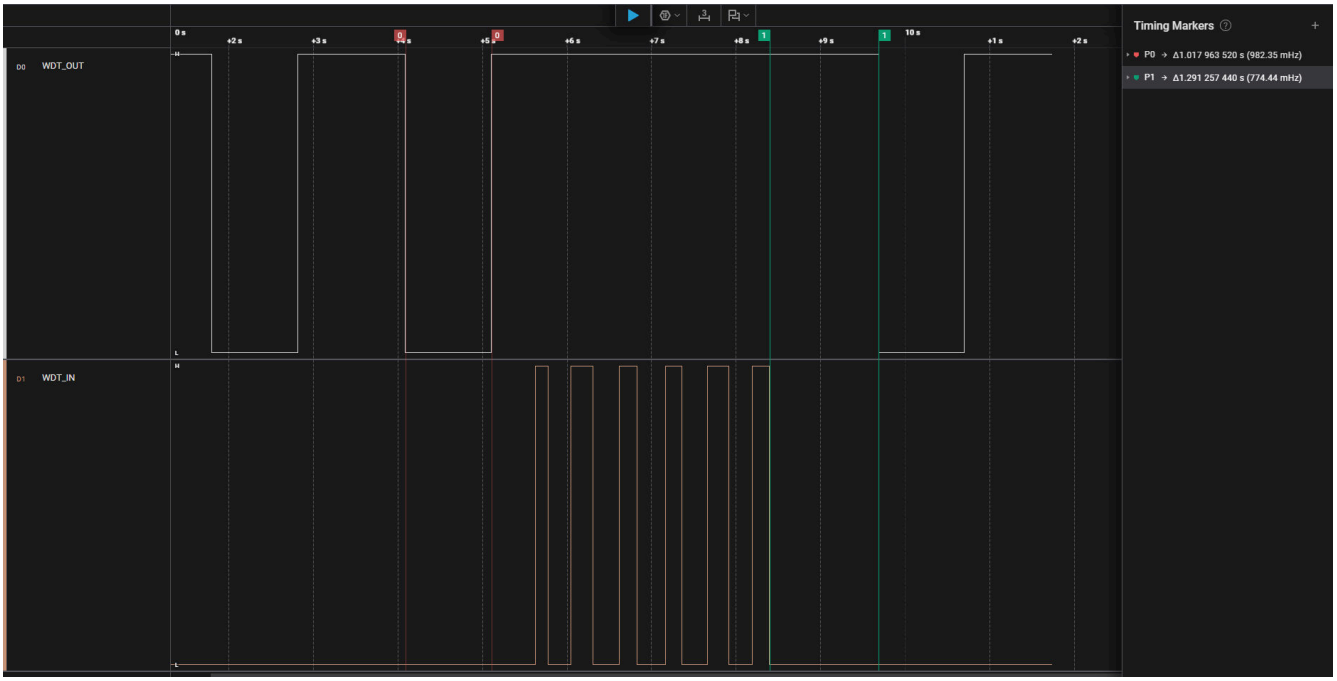

Figure 3. WDT With Longer Output Assertion Time

Figure 4. WDT With Longer Timeout Period and Longer Output Assertion Time

Building a Watchdog Timer With Components

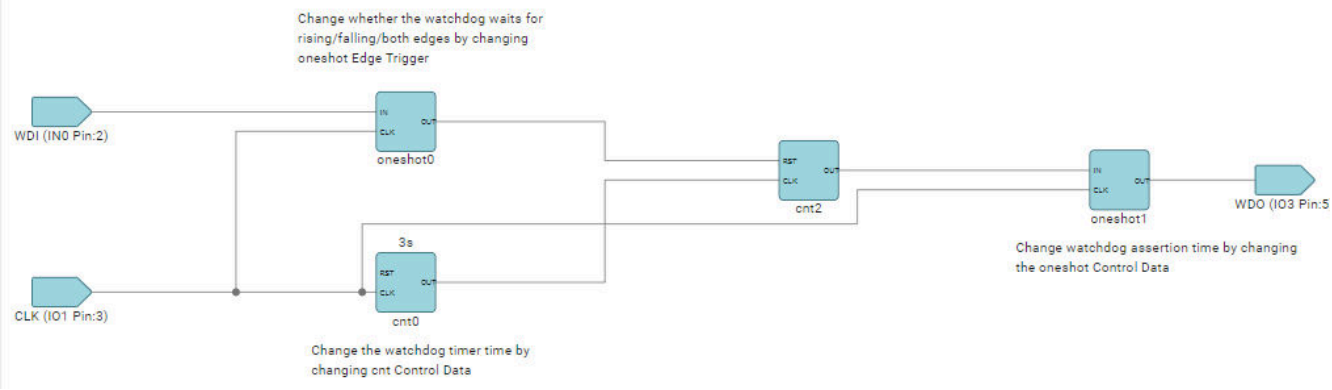

Figure 5. Example of a Discreet Watchdog

Creating a WDT discreetly is possible, as shown in Figure 5. The disadvantage of building a WDT without the single WDT block is that the design separates the settings into individual blocks which can cause confusion when adjusting the design in the future. The advantage of building a WDT without the single WDT block is an increase in flexibility, as well as the ability to use a clock external to the TPLD device as the controlling timer.

The design from Figure 5 uses cnt0 to control the time between checks (timeout period), and oneshot1 controls the time the watchdog spends LOW (output assertion time). The design also takes advantage of the external clock to allow for synchronicity with other devices in the system.

Building a Design Around WDT

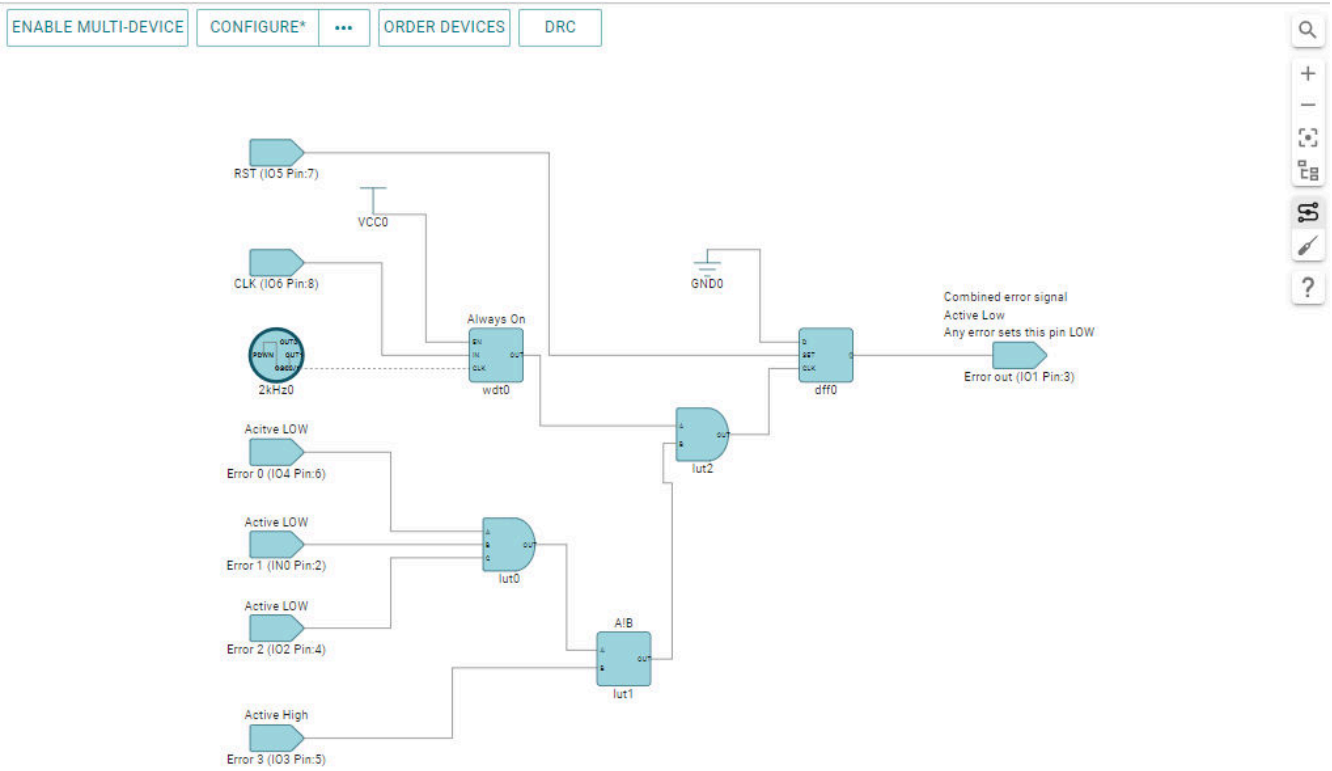

Figure 6. Combination of Error Signals

The most common design for a WDT is a combination of error signals, with a reset latch at the output. This type of design can be observed in Figure 6. The concept of this design is to gather potential error signals—whether those signals are active HIGH or active LOW—and combine the signals into one error signal for the system.

In this design, the WDT is monitoring a clock signal, and if that clock frequency is slower than 400Hz the circuit latches to hold the system in reset until the error is reset by an external signal. At which point, the system resets the error latch or resets the entire device to resume operation. The rest of the system is simply combining the other potential error signals to the latch as well.

Ordering Information

Hardware used in support of this document can be found in Table 1.

Table 1. Ordering Information

Device	EVM
All TPLD	TPLD-PROGRAM
TPLD1202	TPLD1202-DYY-EVM TPLD1202-RWB-EVM
TPLD2001	TPLD2001-DGS-EVM TPLD2001-RJY-EVM

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