Application Brief

High-Speed Operation in TPLD

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As industry trends push towards faster, higher frequency operation, TI remains committed to helping our customers innovate. To that end, TI's Programmable Logic Devices have been designed to interface with high frequency signals.

The TPLD1202 and TPLD2001 both include a 25MHz oscillator block internal to the device. This allows for high-speed data processing and precise timing control. This oscillator is independent of the other oscillators in the device, so designers can use whichever oscillator makes sense for any given block in a design and can turn off oscillators when not in use, which saves power.

Frequency Limits

While they both support internal frequencies of up to 25MHz using the internal oscillator, TPLD1202 and TPLD2001 both have upper limits on their input and output frequencies. TPLD1202 supports inputs with frequencies of up to 10MHz and can output up to 5MHz.

TPLD2001 has maximum limits on input and output frequencies determined by the pin of the device and the operating voltage, as listed in Table 1.

Table 1. TPLD2001 Input and Output Frequency Limits

	1.8V VCC or Low-Voltage Input		3.3V VCC and Higher with Schmitt Trigger or Non-Schmitt Trigger Inputs	
	IO14, IO15, IO17	Other	IO14, IO15, IO17	Other
Fin Max	10MHZ	10MHz	25MHz	10MHz
Fout Max	10MHZ	8MHz	12MHz	8MHz

Design Considerations

When using a high frequency input to the TPLD, TI recommends using an impedance matched trace with a 50Ω termination resistor to ground as close as possible to the TPLD. An example of this can be found on the TPLD2001-DGS-EVM.

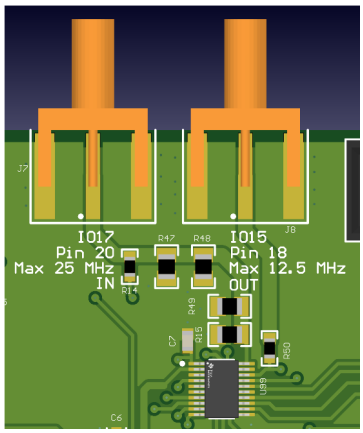

Figure 1. High Frequency IOs on the TPLD2001-DGS-EVM

Here, four 200Ω resistors are intended to be soldered in parallel, creating a 50Ω termination to ground. The 200Ω resistors are used because using multiple resistors lowers the power through each individual resistor, allowing the user to use a wider array of resistors.

When using a high frequency output from the TPLD, TI recommends using an impedance matched 50Ω trace to allow for good signal quality. On the TPLD2001-DGS-EVM, R50 is included on the board to allow for this.

When using the high speed IOs on the TPLD2001 EVMs, TI recommends soldering the device to the U99 soldering mount rather than using the socket on the board. TI also recommends de-populating R14 to disconnect the IO17 line from the trace leading to the rest of the board to reduce parasitics.

For more information on TPLD, visit the TPLD product page or ask our engineers a question on the TI E2E™ Logic Support Forum.

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