Application Brief

Suggested DC/DC Converters and PMIC for Powering DDR5, LPDDR5, and LPDDR5X Memory

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Introduction

DDR (Double Data Rate) memory has been around for many years and allows faster speed, higher power efficiency, and increased capacity than previous generations for a wide range of applications. This article will briefly introduce different DDR5 variations and suggest power management ICs and DC/DC converters to provide a simple power management design.

DDR5

DDR5 is the fifth generation of double data rate synchronous dynamic random-access memory (DDR SDRAM). DDR5 is available in several different variations of Dual in-line Memory Modules (DIMM) and discrete memory ICs. The most popular options are the DIMM variants, which use a dedicated power management integrated circuit (PMIC) directly on the module to provide all the necessary voltages for the on-board discrete memory ICs. The PMIC requires an I2C and I3C bus interface for configuration, fault conditions, and telemetry of voltage, current, power, and temperature. The input voltage to the DIMM can be 5V or 12V, depending on the DIMM variant. DDR5 is used in higher performance applications that need high bandwidth, such as enterprise servers. The JESD79-5B standard is the JEDEC compliance document for powering DDR5. Table 1 shows how a PMIC provides on-DIMM power to the DDR5 rails.

Table 1. DDR5 on DIMM Power

DDR5 Rail	Description	Voltage	Current Capability	PMIC
VDD	Supply Voltage	1.1V	up to 12A	TPS53830A
VDD1	Supply Voltage (optional)	1.1V	up to 6A, reduces VDD to 6A	
VDDQ	I/O Supply Voltage	1.1V	up to 6A	
VPP	Pump Voltage	1.8V	up to 5A	
1.8V_ LDO	PMIC to HUB	1.8V	up to 10mA	
1.0V_LDO	PMIC to HUB	1.0V	up to 60mA	

LPDDR5 and LPDDR5X

LPDDR5 is the fifth generation of low-power, double data rate dynamic random-access memory. It offers lower power consumption and a lower data rate than DDR5 but still provides high bandwidth. LPDDR5 has lower latency and faster response times than DDR5 making it preferred for applications like mobile devices, infotainment, and video. LPDDR5 is not offered in a traditional DIMM form-factor like DDR5 with the power management design located on the module, so the power management design must be designed by the user. LPDDR5 uses on-die termination (ODT) to integrate internal termination resistors inside the memory IC to reduce reflected signals and improve speed. Earlier versions of DDR memory required active bus termination with an external regulator (VTT) to source and sink current with termination resistors. LPDDR5 does not need the VTT rail or external termination resistors. The current requirement depends on the number of die and the number of channels integrated within the LPDDR5 memory IC. LPDDR5 includes Dynamic Voltage Frequency Scaling (DVFS) feature to optimize power consumption or performance, which is especially useful in battery operated mobile applications. Note that some System-on-Chip (SoC) vendors may or may not support the

DVFSC (core logic) and DVFSQ (I/O) features. For more information, the JESD209-5C standard is the JEDEC compliance document for powering LPDDR5 and LPDDR5X.

Table 2 shows a list of suggested DC/DC converter designs to power LPDDR5 and LPDDR5X. The DC/DC converters are chosen for their wide input voltage range, high reference voltage accuracy, small package size, scalable output current versions, and available power good and enable pins. Since the required output current for LPDDR5 and LPDDR5X can vary, the designs shown below are a rule-of-thumb estimate that will support many use-cases.

Table 2. LPDDR5 and LPDDR5X Power for 5V, 12V, and up to 24V Input

LPDDR5 Rail	Description	Nominal Voltage	DVFS	Iout	Both DVFS disabled	Only DVFSC enabled	Only DVFSQ enabled	Discrete Solution
VDD1	Core Supply, Pump Voltage	1.8V	N/A	up to 1A	TPS51488	TPS51488	TPS51488	TPS62932
VDD2H	Core Logic Supply	1.05V	DVFSC disabled	up to 8A				TPS51386
VDDQ	I/O Supply	0.5V	DVFSQ disabled	up to 2A			TPS543320 or TPS62868	TPS543320 or TPS62868
		0.3V	DVFSQ enabled		N/A	N/A		
VDD2L	Core Logic Supply	0.9V	DVFSC enabled	up to 1.5A	N/A	TPS54388	N/A	TPS54338

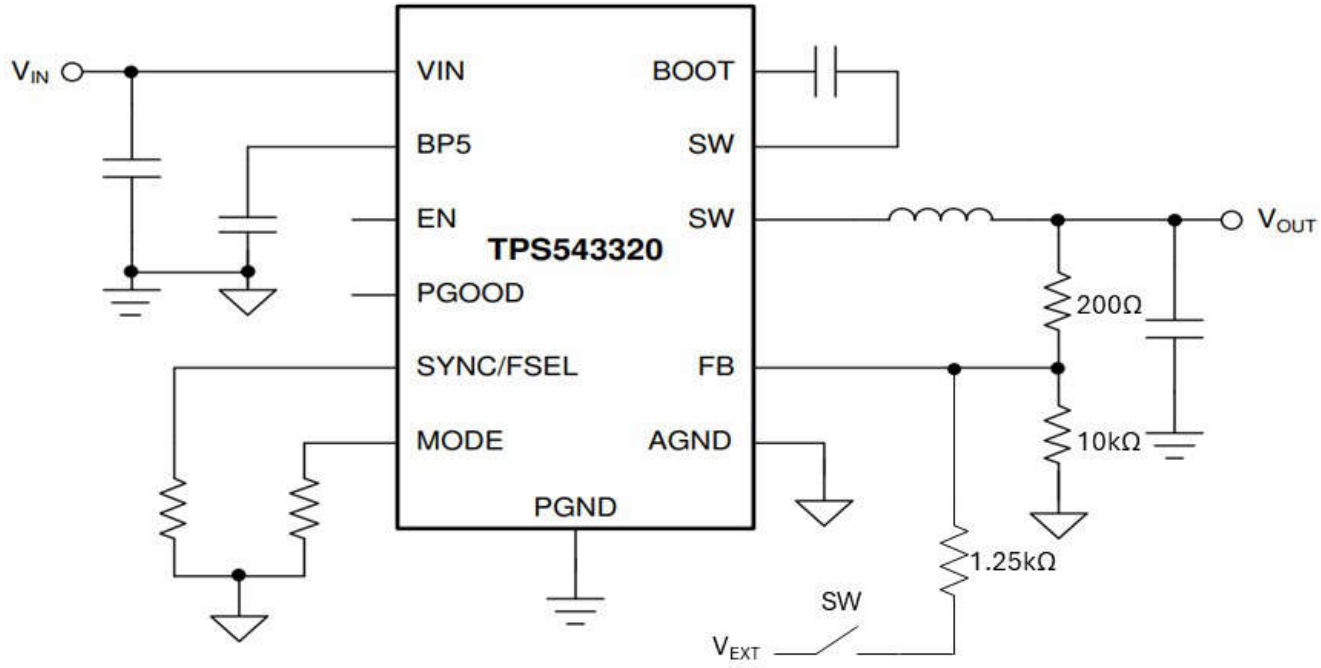
Table 3. Suggested DC/DC Converters and PMIC

Device	Description	Note
TPS51488	4.5V to 24V input, LPDDR5 Memory Power PMIC	Contact local sales representative or visit TI E2E support forums for the data sheet.
TPS54338	3.8V to 28V input, 3A buck converter	4A and 5A versions available in same package (TPS54438, TPS54538)
TPS543320	4V to 18V input, 3A buck converter	Supports 0.5V output with 0.3V capability. 6A and 8A versions available in same package (TPS543620, TPS543820).
TPS51386	4.5V to 24V input, 8A buck converter	12A available in 3x4mm package (TPS51375)
TPS62932	3.8V to 30V input, 2A buck converter	3A version available in the same package (TPS62933)
TPS62868	2.4V to 5.5V input, 4A buck converter	Supports 0.5V and 0.3V with I2C interface. 6A version available in the same package (TPS62869)

Although several JEDEC common standards exclude the 0.3V support for DVFSQ for the discrete VDDQ voltage design implementation, it is possible for the TPS543320 to support DVFSQ control with a few additional components in the feedback loop. Equation 1 calculates the output voltage when the switch is open and Equation 2 calculates the voltage when the switch is closed. An additional MOSFET switch and resistor are added to inject current into the feedback pin when the switch is closed to reduce the output voltage below the reference voltage. Please note to calculate for any voltage-drop due to trace loss.

$$VOUT = VFB \times \left(\frac{R1}{R2}\right) + 1\Big) \quad (1)$$

$$VOUT = VFB \times \left(\frac{R1}{R2} + 1\right) - \frac{R1}{R3} \times \left(VEXT - VFB\right) \quad (2)$$



The voltage requirements for LPDDR5 and LPDDR5X are the same. LPDDR5X uses advanced equalization and signaling techniques to achieve a higher memory bandwidth, up to 8500Mbps from 6400Mbps of LPDDR5. The same devices powering LPDDR5 will also work to power LPDDR5X.

There are sequencing requirements for LPDDR5 and LPDDR5X rails, according to the JEDEC standard. The higher voltage rails need to reach their voltage level at the same time or before the lower voltage rails during the converter's start-up sequence and complete start-up within 20ms. The power rails should power-down in the reverse order as start-up. If using VDD2L, VDD2L should never exceed VDD2H by a small margin, such as 0.3V, and VDD2H should not exceed VDD1 to avoid forward-biasing internal diodes. To simplify design, the TPS51488 follows the power rail sequencing requirements. The discrete DC/DC converters suggested in this document contain both enable and power good pins to help facilitate power supply sequencing to stagger start-up and power-down.

Summary

There are many DC/DC converters preferred to power LPDDR5 and LPDDR5X. The more difficult rail is the 0.3V VDDQ when DVFSQ is enabled but using the circuit method described will help achieve the lower voltage. An I2C-controlled, lower input voltage DC/DC converter can also be selected. The DC/DC converters featured in this document have the following attributes.

- Wide input-voltage range
- High reference voltage accuracy
- Small package size
- Scalable output current versions
- Power good and enable pins

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