*Reliability Report*

# *ADC12DJ5200-SEP Production Flow and Reliability Report*


**ABSTRACT**

This report presents the reliability and qualification results for the ADC12DJ5200-SEP, a radiation-hardness-assured (RHA), 30krad, 12-bit, dual 5.2-GSPS or single 10.4-GSPS Analog-to-Digital Converter (ADC). The ADC12DJ5200-SEP is manufactured with a controlled baseline and has the following advantages compared to commercial-grade devices:

- An extended product life cycle
- Controlled baseline: one fab, assembly and test site
- Product traceability
- Lot-acceptance testing


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# 1 Texas Instruments Space-Enhanced Product Qualification and Reliability Report

TI qualification testing is a risk mitigation process that is engineered to assure device longevity in customer applications. Wafer fabrication process and package level reliability are evaluated in a variety of ways that may include accelerated environmental test conditions with subsequent derating to actual use conditions. Manufacturability of the device is evaluated to verify a robust assembly flow and assure continuity of supply to customers. TIs Space Enhanced Products (SEP) are qualified with industry standard test methodologies performed to the intent of Joint Electron Devices Engineering Council (JEDEC) standards and procedures.

# 2 Space-Enhanced Product Production Flow

## 2.1 Device Introduction

The ADC12DJ5200-SEP is a radiation-tolerant device in an organic flip-chip package that is designed for space applications. The 10 × 10mm 144ALR package utilizes eutectic tin-lead (SnPb) die-bumps and external SnPb BGA balls. The device was verified as single event latch-up (SEL) immune to 43MeV × $cm^2$/ mg at a junction temperature of 125°C. The ADC12DJ5200-SEP is manufactured with TI's internal 65nm CMOS C021.A process.

Each fabrication lot is tested according to the MIL-STD-883 requirements for Radiation Lot Acceptance Testing (RLAT) up to 30krad(Si) and each assembly and test lot follows the process flow shown in Figure 2-1. To verify the quality of ADC12DJ5200-SEP, the device has been tested and qualified to meet space-grade requirements for VLEO, LEO and MEO missions. See Section 3 for further details.

## 2.2 ADC12DJ5200-SEP Space-Enhanced Product Production Flow

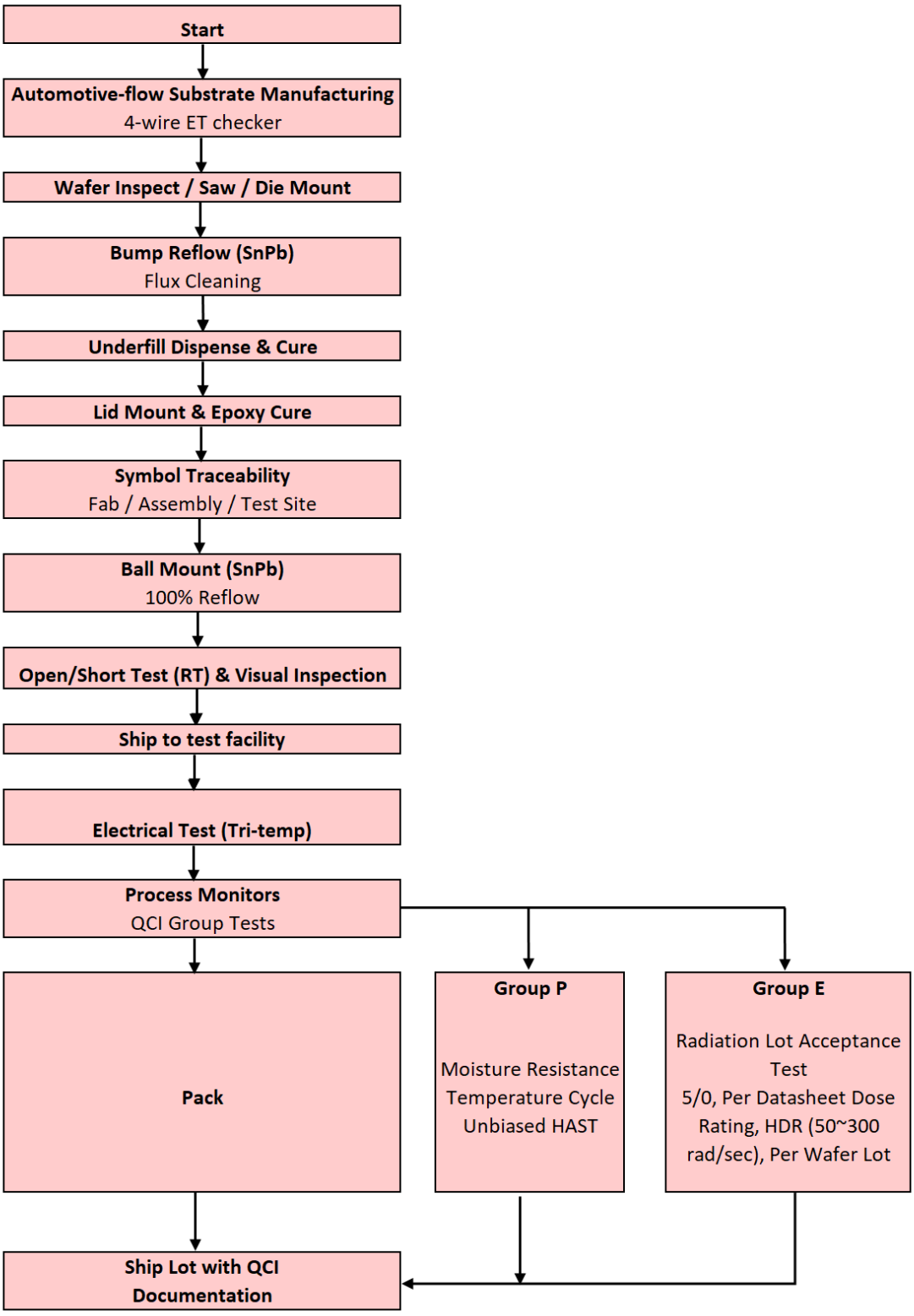


**Figure 2-1. ADC12DJ5200-SEP Space-Enhanced Product Production Flow Chart**

# 3 Device Qualification

The following is the device qualification summary.

### Qualification by Similarity (Qualification Family)

A new device can be qualified either by performing full scale quality and reliability tests on the actual device or using previously qualified devices through Qualification by Similarity (QBS) rules. By establishing similarity between the new device and those qualified previously, repetitive tests will be eliminated, allowing for timely production release. When adopting QBS methodology, the emphasis is on qualifying the differences between a previously qualified product and the new product under consideration. The QBS rules for a technology, product, test parameters or package shall define which attributes are required to remain fixed in order for the QBS rules to apply. The attributes which are expected and allowed to vary will be reviewed and a QBS plan shall be developed, based on the reliability impact assessment above, specifying what subset of the full complement of environmental stresses is required to evaluate the reliability impact of those variations. Each new device shall be reviewed for conformance to the QBS rule sets applicable to that device. See JEDEC JESD47 for more information.

**Table 3-1. Space-Enhanced Products New Device Qualification Matrix**

| Note that qualification by similarity (“qualification family”) per JEDEC JESD47 is allowed. | | | | |
|---|---|---|---|---|
| **Description** | **Condition** | **Sample Size Used and Rejects** | **Lots Required** | **Test Method** |
| Electromigration | Maximum Recommended Operating Conditions | N/A | N/A | Per TI Design Rules |
| Electrical Characterization | TI Data Sheet | 30 | 1 | N/A |
| Electrostatic Discharge Sensitivity | HBM | 3 units/voltage | 1 | JS-001 |
| | CDM | | | JS-002 |
| Latch-up | Per Technology | 3/0 | 1 | EIA/JESD78 |
| Physical Dimensions | TI Data Sheet | 5/0 | 1 | EIA/JESD22- B100 |
| Thermal Impedance | Theta-JC on board | Per pin-package | N/A | Modeling |
| Bias Life Test | 125°C / 1000 hours or equivalent | 77/0 | 1 | JESD22-A108* |
| Temperature Humidity Bias | 85°C / 85% / 1000 hours | 77/0 | 1 | JESD22-A110* |
| Extended THB | 85°C / 85% / 2600 hours (for reference) | 77/0 | 1 | JESD22-A110* |
| Unbiased HAST | 110°C / 85% / 528 hours | 77/0 | 1 | JESD22-A.118* |
| Temperature Cycle | -55°C to +125°C non-biased for 1000 cycles | 77/0 | 1 | JESD22-A104* |
| High Temperature Storage Life | 150°C, 1000 hours | 77/0 | 1 | JESD22-A103* |
| Solderability | 22 leads, min 3 devices, 245C +5C | 22/0 | 1 | J-STD-002 |
| Flammability | Method A / Method B | 5/0 | 1 | UL 94V0, Method A |
| Radiation Response Characterization | Total Ionization Dose (TID) | Two units / dose level | 1 | MIL-STD-883/Method 1019 |
| Radiation Response Characterization | Single Event Latch-up (SEL) | 3 | 1 | MIL-STD-883/Method 1019 |
| RLAT | Radiation Lot Acceptance Testing | 5/0 | | MIL-STD-883/Method 1019 |
| Outgassing Characterization, packaged unit | TML (Total Mass Lost)<=1%, CVCM (Collected Volatile Condensable material) <=0.1% | 5/0 | 1 | ASTM E595 |
| *Precondition performed per JEDEC Std. 22, Method A112/A113. | | | | |

# 4 Outgas Test Report

Outgassing test was performed on 5 units. A total mass loss (TML) of 1.00% and collected volatile condensable material (CVCM) of 0.10% were used as screening levels for rejection of spacecraft materials. The outgas test was performed in a vacuum environment of less than $5 \times 10^{-5}$ torr according to ASTM E595, for a duration of 24 hours, at 125°C. The TML and CVCM were measured after the test.

**Table 4-1. Outgas Test Results**

| Sample | TML<br>< 1.0% | CVCM<br>< 0.1% |
|---|---|---|
| ADC12DJ5200ALRSEP | PASS | PASS |

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