Radiation Report

DAC39RF10-SP Single Event Effects Report

ABSTRACT

The rad-hard DAC39RF10-SP (DAC39RF10ACL-MLS) was tested under heavy ions and monitored for various single-event effects (SEE). No incidences of single-event latch-up (SEL) or single-event function interrupts (SEFI) were detected up to 120 MeV·cm^2/mg, the highest tested effective linear energy transfer (LET_{EFF}). SEL testing was performed at the maximum recommended operating supply voltages and junction temperature (125°C). Single event upsets (SEU) were detected in the high-speed digital path and analog circuitry, but the DAC39RF10-SP always self-recovers from an upset event with no user intervention.

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1 Introduction

The DAC39RF10-SP is a radiation-hardened-by-design (RHBD) RF-sampling, multi-Nyquist, digital-to-analog converter (DAC) that can directly synthesize frequencies from DC to above 12GHz. The device can be used as a non-interpolating or interpolating DAC for either direct RF-sampling or complex baseband signal generation. The maximum input data rate is 20.8GSPS for a single channel or 10.4GSPS for two channels. The device can generate signals of up to 10GHz, 7.5GHz, and 5GHz signal bandwidth (8-bit, 12-bit, and 16-bit input resolution) at carrier frequencies exceeding 12GHz, enabling direct sampling beyond X-band. The DAC39RF10-SP also has the lowest additive phase and amplitude noise versus any space-grade DAC in the industry.

Table 1-1. Overview Information

Description	Device Information
Generic part number	DAC39RF10-SP
Orderable part number	DAC39RF10ACL-MLS
Device function	RF-sampling digital-to-analog converter
Device package	256-pin ACL FCBGA (17mm × 17mm)
Technology	TI C014.P CMOS 40nm
Exposure facility	Radiation Effects Facility Cyclotron Institute, Texas A&M University (15MeV/nucleon)
Heavy ion fluence per run	Up to 1×10^7ions/cm^2
Irradiation junction temperature	125°C (SEL); Ambient temp (SEFI/SEU)

2 Single-Event Effects

The primary concern of interest for the DAC39RF10-SP is the robustness against single-event latch-up (SEL) and single-event functional interrupt (SEFI).

In CMOS technologies, such as TI's 40nm CMOS (C014.P) process used on the DAC39RF10-SP, the CMOS circuitry inherently introduces a potential for SEL susceptibility. SEL can occur if excess current injection caused by the passage of an energetic ion is high enough to trigger the formation of a parasitic cross-coupled PNP and NPN bipolar structure (formed between the p-sub and n-well and n+ and p+ contacts). The parasitic bipolar structure initiated by a single event creates a high-conductance path (inducing a steady-state current that is typically orders of magnitude higher than the normal operating current). This current between power and ground persists or is latched until power is removed, the device is reset, or until the device is destroyed by the high current state. Understanding this concern, a custom PDK with careful layout considerations was made to achieve latch-up immunity in the DAC39RF10-SP compared to the standard C014.P design rules.

The DAC39RF10-SP was tested for SEL using a custom evaluation board which operates the device at maximum recommended power supply voltages. The device exhibits no SEL with heavy ions up to an LET_{EFF} = 120 MeV·cm^2/mg at a flux of approximately 10^5 ions/cm^2·s, fluence of approximately 10^7 ions/cm^2, and a die temperature of 125°C, achieved using Au ions.

The DAC39RF10-SP was also monitored for SEUs and SEFIs during every beam run. The DAC39RF10-SP configuration registers are immune to single event upset (SEUs) by employing a proprietary rad-hard flip-flop in the design and the device has been architected, verified, and validated to be SEFI-free up to an LET_{EFF} = 120 MeV·cm^2/mg. The device also auto-recovers from any potential SEU due to careful analog and digital design considerations and techniques.

3 Device and Test Board Information

The DAC39RF10-SP is packaged in a 256-pin FCBGA (TI package code ACL) organic substrate flip-chip package. The device under test (DUT) was tested in a high-frequency capable, open-top socket using a custom characterization board similar to the DAC39RF10EVM evaluation board. To test the DAC in functional modes, the DAC EVM is mated to TI's TSW14J59EVM FPGA capture card and pattern generator through an FMC+ connector.

Figure 3-2 shows the top view of the evaluation board and socket used for SEE testing.

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The DAC39RF10-SP is a flip-chip device, so heavy ion irradiation is done from the backside of the die. The metal lid was removed from the DUT to expose the die surface, then the silicon is lapped from the standard 775µm down to 50µm (target final thickness) to allow for beam penetration into the active area of the die. An example thickness profile is shown in Figure 3-1.

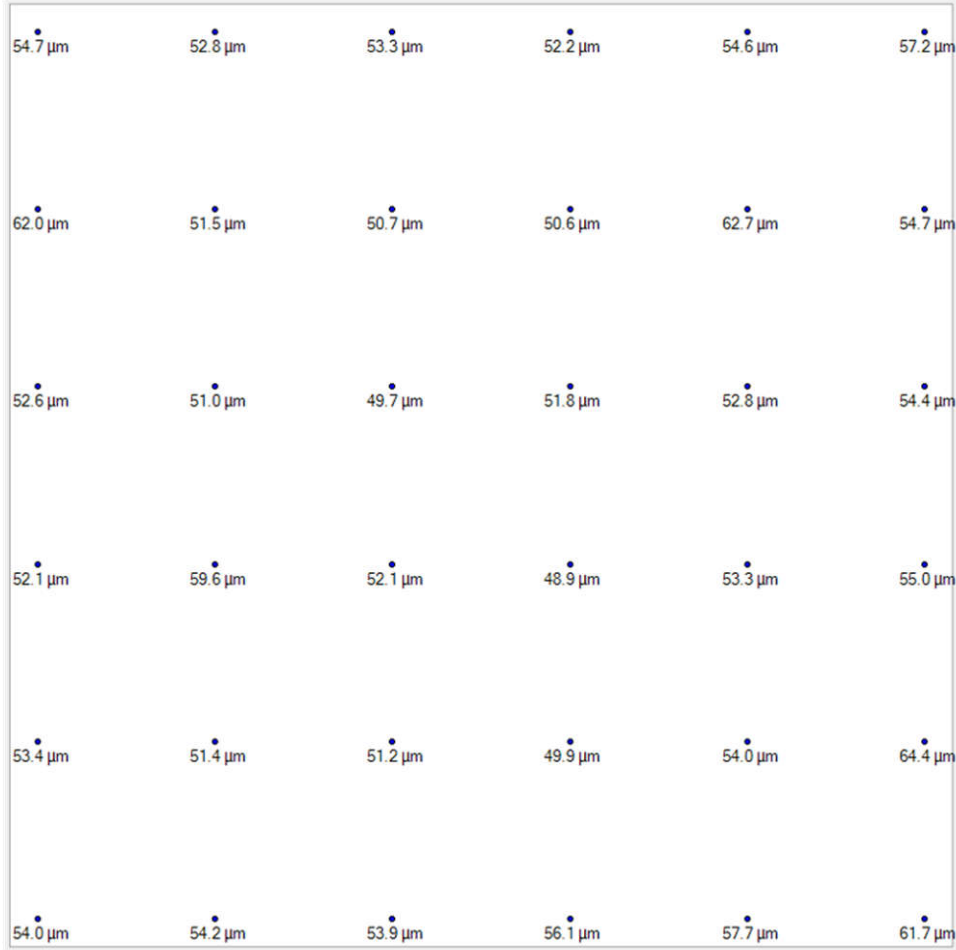

Figure 3-1. Silicon Thickness Profile of DUT_2301 (Target 50µm)

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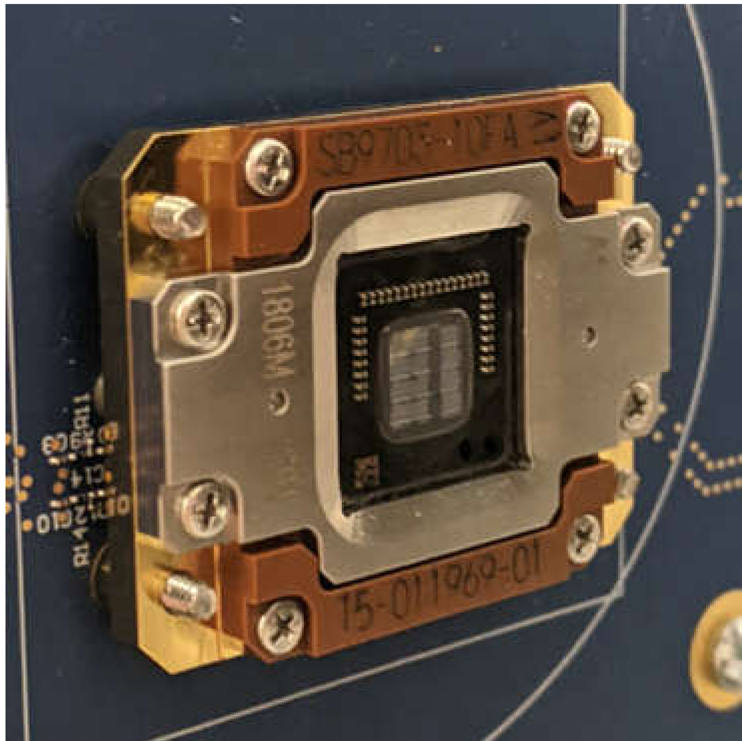

Figure 3-2. Photograph of Delidded and Thinned DAC39RF10-SP Sitting in the RF Test Socket

4 Irradiation Facility and Setup

The heavy-ion species used for the SEE studies on this product were provided and delivered by the TAMU Cyclotron Radiation Effects Facility using a superconducting K500 cyclotron and an advanced electron cyclotron resonance (ECR) ion source. Ion beams had good flux stability and high irradiation uniformity over a 1-inch diameter circular cross-sectional area for the in-air station. Uniformity is achieved by magnetic defocusing. The flux of the beam is regulated over a broad range spanning several orders of magnitude. For this characterization, ion flux of 10^5 ions/cm^2·s were used to provide heavy ion fluences of up to 10^7 ions/cm^2 for our runs. Ion uniformity for these experiments was typically >95%.

Figure 4-1 shows the full test setup used for the experiments at the TAMU facility. Although not visible in this photo, the beam port has a 1-mil Aramica window to allow in-air testing while maintaining the vacuum within the accelerator with only minor ion energy loss. A 50mm in-air gap between the device and the ion beam port window was maintained at these distances for all runs respective to the ion that was tested.

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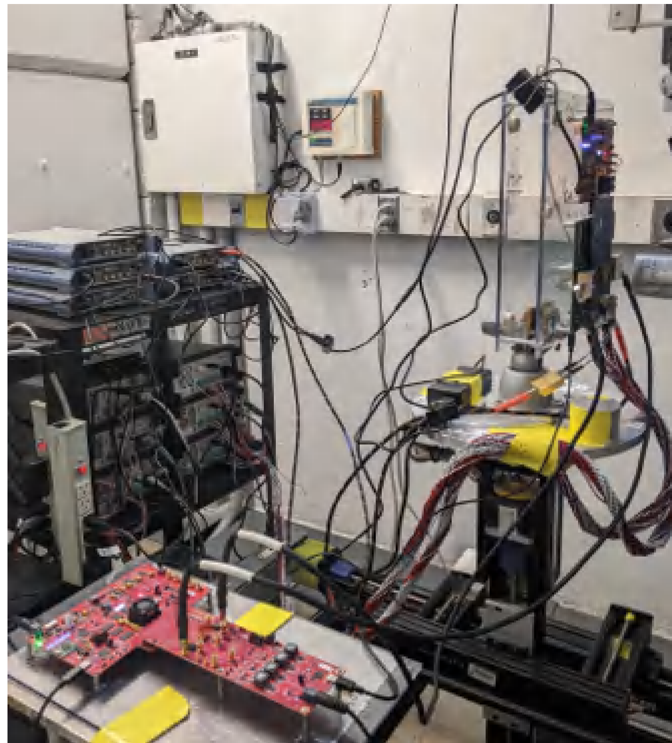

Figure 4-1. DAC39RF10-SP Mounted and Positioned for Heavy-Ion Exposure

5 Test Setup and Procedures

The DAC39RF10-SP was configured as follows for all SEE testing (unless otherwise noted):

- DACCLK = 10.24GHz from R&S® SGS100A
- JMODE3, 64b/66b encoding, 8x interpolation, and Subclass 1
- SerDes rate 10.56Gbps, 16 lanes, 2 lanes per stream (M = 8)
- NCO set to re-align with SYSREF in Subclass 1 (“Strategy #1”)
- SYSREF = 5MHz for this configuration (continuous SYSREF from LMK04832)
- Pattern generator = TSW14J59 Rev C using “6466b 2/11/2022” firmware and TSW_controller_051722 (FPGA reference clock from LMK is 160MHz)
- A 97MHz tone is sent over the JESD204C link and all four (4) of the DAC39RF10-SP’s NCOs are used to up-convert this tone to 297, 497, 697, and 897MHz, respectively.
- DAC outputs were monitored with either the ADC12DJ5200RFEVM (making it an effective and low-cost spectrum analyzer), an R&S® FSWP spectrum analyzer, or an oscilloscope with standard triggering functionality.
- Supplies set to +5% for SEL testing; forced air to achieve Tj > 125℃
- Supplies set to -5% for SEFI testing; ambient temperature (no forced air)

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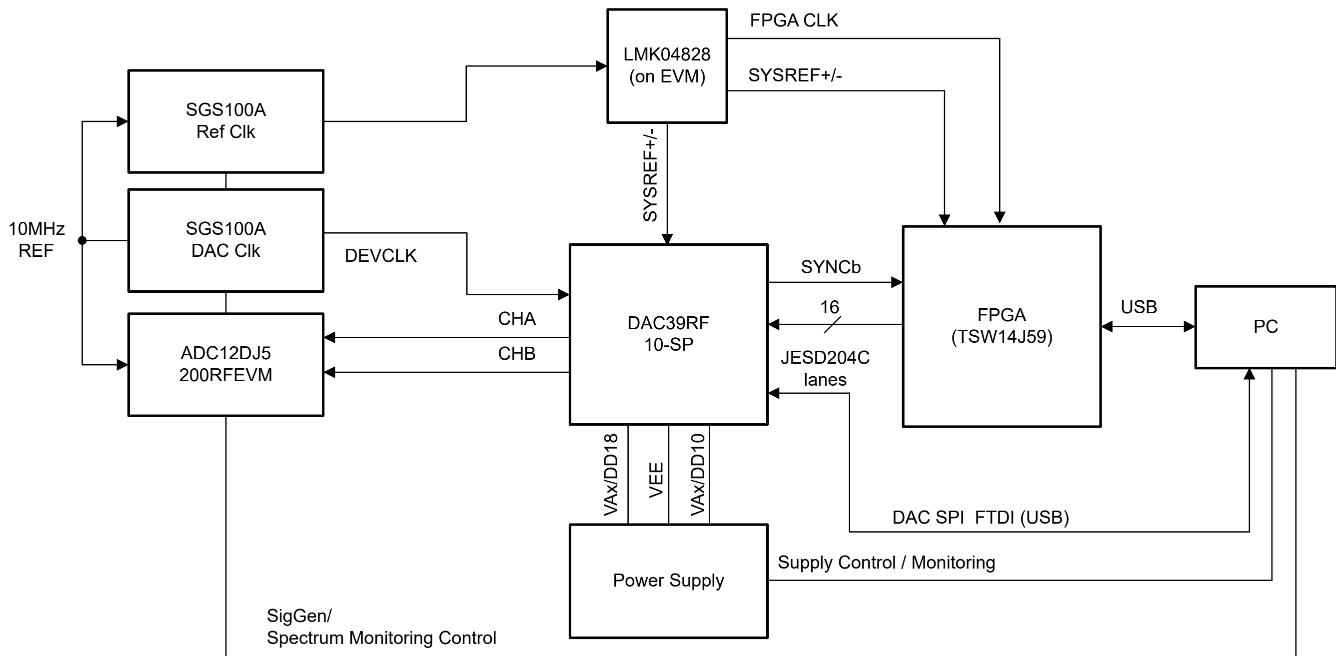

Figure 5-1. DAC39RF10 SEE Test Setup Block Diagram

6 Single-Event Latch-Up (SEL) Results

For SEL testing, the DAC39RF10-SP is biased to the datasheet maximum recommended supply voltages (+5% of the nominal values): VEE = -1.89V; VAx18 = VDD18 = 1.89V; VAx10 = VDD10 = 1.05V (the nominal supply voltages are VEE = -1.8V; VAx18 = VDD18 = 1.8V; VAx10 = VDD10 = 1.0V), and the die is heated externally to a junction temperature of >125°C. The die temperature was monitored using the on-die temperature sensor.

We also checked for SEL marginality on the DAC39RF10-SP using supply voltages set to +10% of the nominal voltages: VEE = -1.21V; VAx18 = VDD18 = 2.1V; VAx10 = VDD10 = 1.21V.

The species used for the SEL testing were gold (^{197}Au) ions and an angle of 45° to achieve an LET_{EFF} of >120 MeV·cm^2/mg. Ion flux target was set to 10^5 ions/cm^2·s and we ran to a fluence of 10^7 ions/cm^2. The SEL run is typically repeated to achieve a total fluence of 2e7 ions/cm^2 per DUT. No SEL events were observed during any beam runs across four different DUTs, indicating that the DAC39RF10-SP is SEL-free. Table 6-1 shows the SEL run conditions.

Table 6-1. SEL Run Conditions

Test ID	DUT #	Supply Rails	Tj (°C)	Beam Ion	Angle (°)	LET_{EFF} (MeV-cm^2/mg)	Flux (ions·cm^2/s)	Fluence (ions·cm^2)	SEL Observed ?	Device cfg
2022.06.02-06	2264	+5%	130	Au	45	121	1.00×10^5	1.00×10^7	No	JMODE3
2022.06.02-11	2264	+10%	140	Au	45	121	1.00×10^5	1.00×10^7	No	JMODE3
2022.06.02-13	2269	+5%	136	Au	45	121	1.00×10^5	1.00×10^7	No	JMODE3
2022.06.02-16	2269	+10%	143	Au	45	121	1.00×10^5	1.00×10^7	No	JMODE3
2023.09.12-01	2301	0%	109	Au	45	121	1.00×10^5	1.00×10^7	No	JMODE3
2023.09.12-02	2301	+5%	121	Au	45	121	1.00×10^5	2.00×10^7	No	JMODE3
2023.09.12-03	2301	+10%	131	Au	45	121	1.00×10^5	2.00×10^7	No	JMODE3
2023.09.12-04	2303	+5%	122	Au	45	121	1.00×10^5	2.00×10^7	No	JMODE3

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Table 6-1. SEL Run Conditions (continued)

Test ID	DUT #	Supply Rails	Tj (°C)	Beam Ion	Angle (°)	LET_{EFF} (MeV-cm²/mg)	Flux (ions·cm²/s)	Fluence (ions·cm²)	SEL Observed ?	Device cfg
2023.09.12-05	2303	+10%	134	Au	45	121	1.00×10^5	2.00×10^7	No	JMODE3

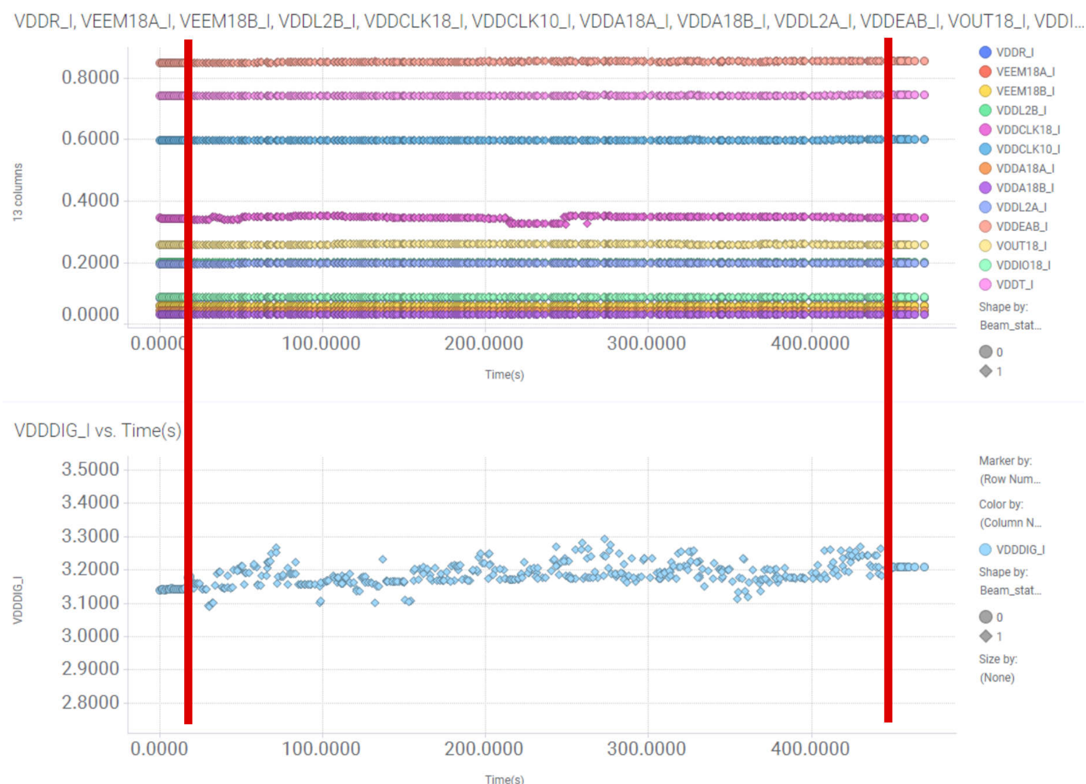

Figure 6-1. DAC39RF10-SP Current During SEL Run 2023.09.12-03

Note

The digital supply current is plotted separately since it consumes more current than other rails. You can observe minor fluctuations in current when the beam is active.

7 Single-Event Functional Interrupt (SEFI) Results

7.1 Converter Performance and Digital (DUC + JESD204C Link) Hardness

The DAC was configured in JMODE3 and a baseline FFT was captured on the spectrum monitoring software (HSDCPRO) showing four unique tones (all four NCOs have been programmed) and typical analog performance. During the beam run, the DAC output was monitored by taking repeated captures with the HSDCPRO software. No degradation was observed during or after the beam run. This result shows that the DAC39RF10-SP is not susceptible to SEFI that would permanently corrupt the DAC performance. This also demonstrates that the internal calibration and trim vectors and configuration registers are not corrupted by radiation.

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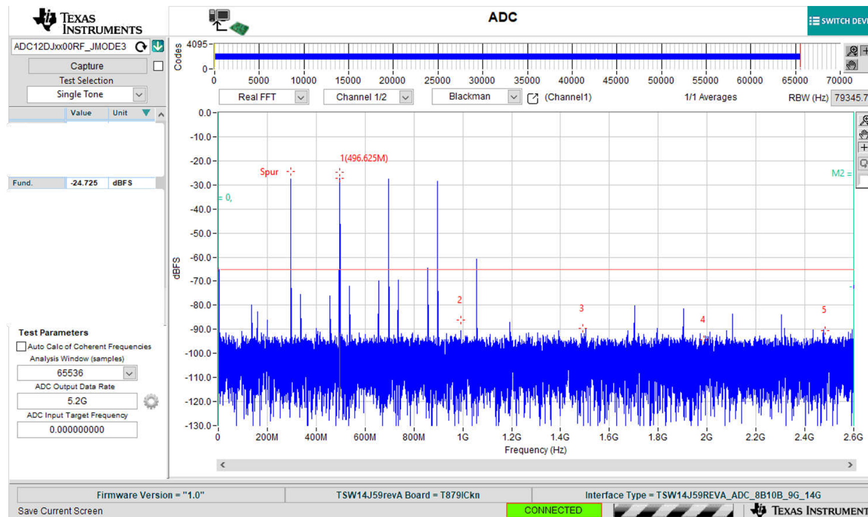

Figure 7-1. DAC39RF10-SP Baseline (Beam-Off) Performance and 4x NCOs Set for SEFI Testing

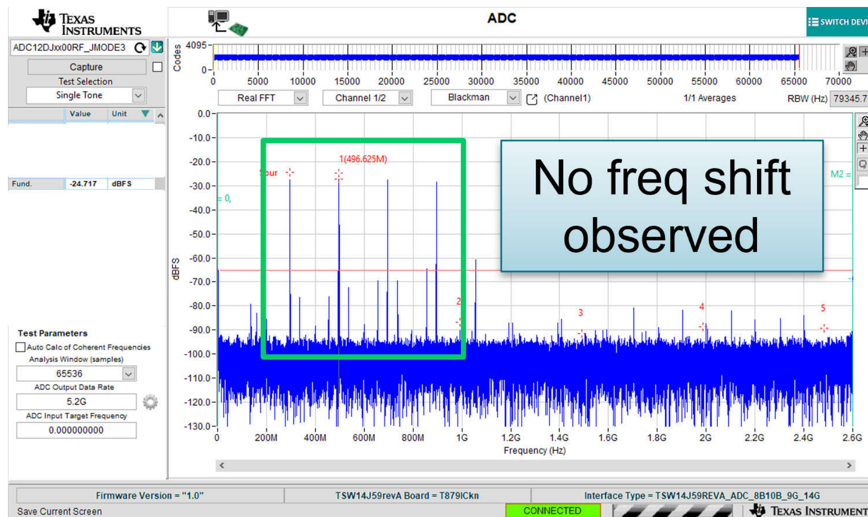

Figure 7-2. DAC39RF10-SP Performance Mid-Run

Note

The DAC39RF10-SP performance mid-run shows all four NCOs have not wandered and analog performance matches the baseline. SerDes link also remains up.

7.2 Configuration Register Hardness

The DAC was configured in an active conversion mode then all SPI registers were read, and the register contents were stored. After the beam run, the read-all register command was initiated, and the register contents were stored yet again. The pre- and post- SPI register dumps were then compared to ensure no values were changing due to ion strikes.

The only values changing are sticky alarms that need to be cleared manually (for example, 0x107 JESD_STATUS; 0x160–0x16F LANE_ERR; 0x410 SYNC_STATUS; 0x430 SYS_ALM). This result is not unexpected as these are read-only SPI status registers associated with JESD204C physical or link layers or write-to-clear status bits that get set when certain events occur in upset-vulnerable logic (an upset can cause an event to occur that gets detected and sets the sticky bit). All user programmable device configuration and fuse-backed register values remain unchanged after beam runs. See the appendix for more details.

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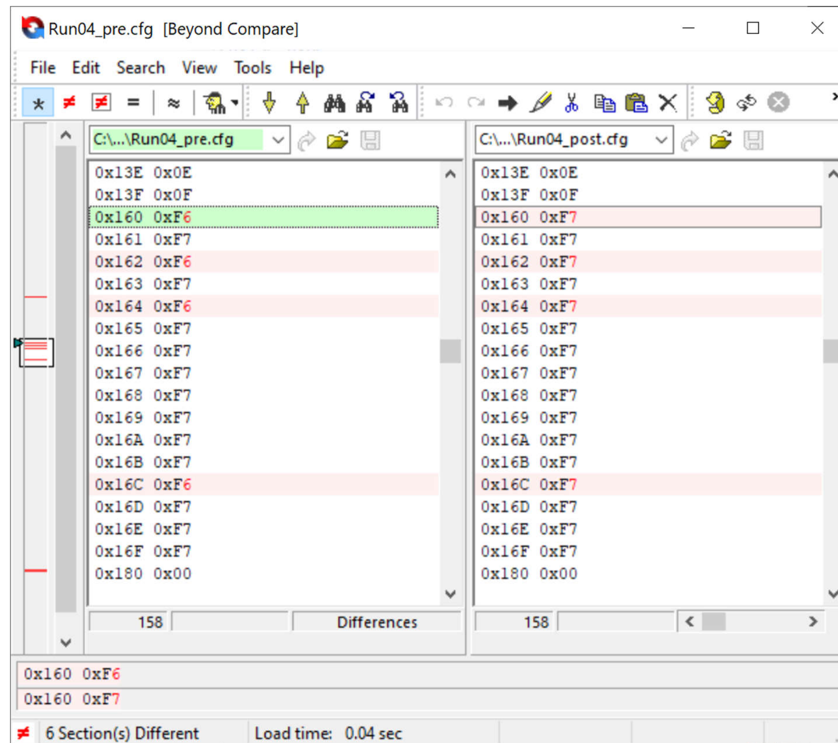

Figure 7-3. Pre- and Post-Beam Run (TestID 2022.06.02-04) SPI Register Dump Comparison

7.3 SPI Programming During Irradiation

Prior to a beam run, a SPI_RESET is initiated to reset the DAC configuration into the default state. The beam is then started, and a configuration file is loaded to program the DAC to a non-default state (JMODE4). The programming occurs while the beam is active through the SPI interface. The beam is then stopped and the read-all register command was initiated, and the register contents were stored. The post-beam-run register contents were reviewed, and the DAC was confirmed to be programmed to the expected non-default state with no configuration registers being altered by particle strikes during programming. This ensures that the DAC can be programmed properly in a radiation environment. This experiment was performed in TestID 2022-06-02.20 and repeated with TestID 2022-06-02.21.

The only values changing are sticky alarms that need to be cleared manually (for example, 0x107 JESD_STATUS; 0x160–0x16F LANE_ERR; 0x410 SYNC_STATUS; 0x430 SYS_ALM; 0x12C LANE_ARSTAT). As noted in the previous section, this is expected behavior.

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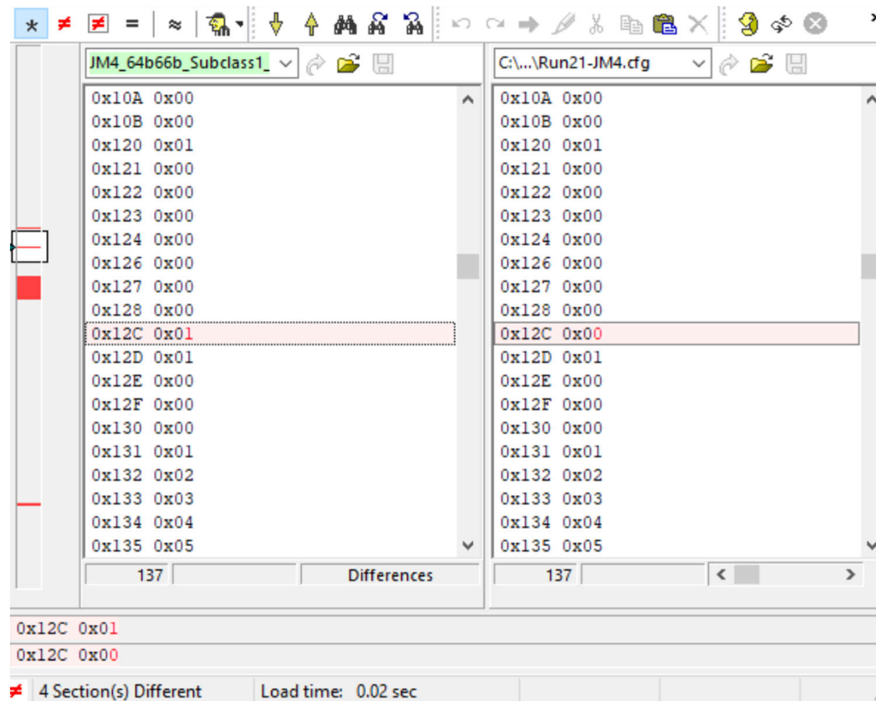

Figure 7-4. Pre and Post Beam Run (TestID 2022.06.02-21) SPI Register Dump Comparison Cont.

8 SEU Results

8.1 JESD204C Link Monitoring Results

The JESD204C receiver is a critical aspect of the DAC39RF10-SP, as this is how massive amounts of digital data are transmitted from the FPGA (or other logic device) to the DAC. During all beam runs, we were unable to observe any link-down events or ‘missing’ or ‘muted’ tones while monitoring the DAC output using the ADC12DJ5200RFEVM with HSDCPRO set up in continuous-capture mode. However, link-down alarm sticky bits were thrown during runs. This indicates that any link-down event that occurred auto-recovered, and without user intervention. In the tested 64b/66b encoding mode, this recovery time is nearly instant. In 8b/10b encoding mode (sometimes referred to as JESD204B), which was not tested, the DAC’s SYNCb signal is used to reset the transmitter and the time to bring the link back up depends on the user’s implementation of the protocol.

8.2 Digital Up-Converter and NCO Upset Recovery

During SEE testing, we employed “Strategy #1” for NCO upset recovery (see *Appendix – NCO Reliability*). With this strategy, we were unable to detect any NCO wandering which places NCO tones in the ‘wrong place’ or potentially ‘mute’ tones as seen in the FFT monitoring software (see Figure 8-1).

To prove the robustness of our SEU-recovery design methodology, we also experimented with the NCO running without using any hi-rel strategy. During these test runs, NCO wandering was observable and detectable.

Note

This data is presented to highlight the importance of following our hi-rel recommendations to enable automatic self-recovery from potential upsets.

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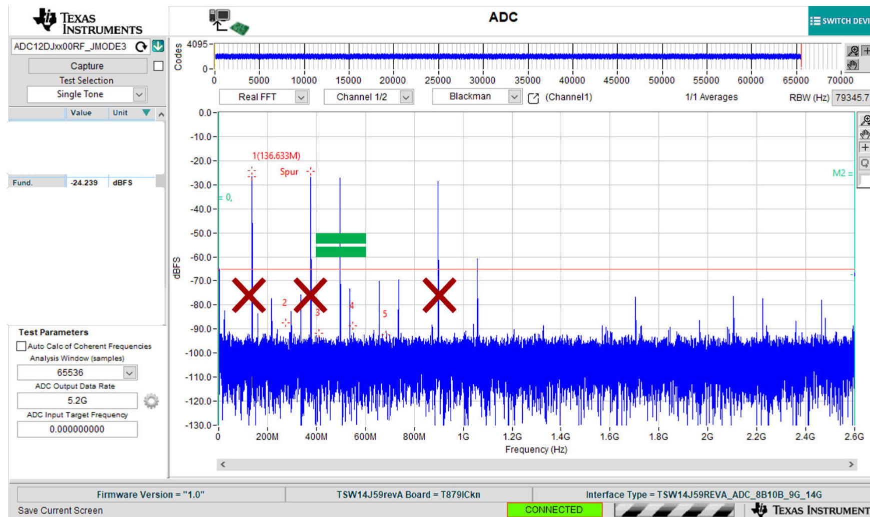

Figure 8-1. Run With No NCO Upset Recovery Strategy Not Employed

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Note

In a test run where NCO upset recovery strategy was not employed, this capture with the beam on shows an upset on three of the NCOs (these upsets were random and recoverable with the next ion strike). This data is presented to highlight the importance of following our hi-riel recommendations to enable automatic self-recovery from potential upsets.

8.3 Estimating Upset Rates in Unprotected Data Paths

To estimate the upset rate of the DAC39RF10-SP, we again performed tests with the NCOs running without employing any hi-rel mitigation strategies. The goal was to understand and quantify how often the unprotected, high-speed circuitry saw an upset (as noted previously, these events were undetectable with hi-rel mitigation strategies employed). If the scope trigger was lost on the output tones being monitored, we recorded the fluence at which this event occurred and then used this data to estimate the device cross section.

To reemphasize, the hardened configuration registers do not experience upset conditions. Also, single events in the analog (for example, in the clocking path or analog DAC cores) flushed out of the data path in a few clock cycles.

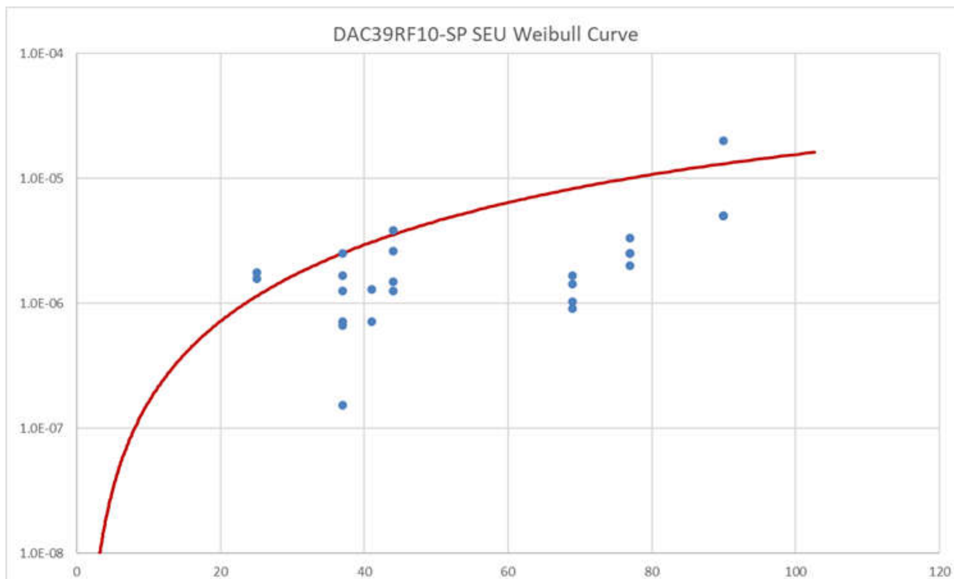

Figure 8-2. SEU Cross Section of the DAC39RF10-SP Unprotected Data Path Upset Rate

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Table 8-1. SEU Cross Section Weibull Parameters

A	Lo	W	s
4.00E-05	1	141	2.00E+00

8.4 Event Rate Calculations

Event rates were calculated for LEO (ISS) and GEO environments by combining CREME96 orbital integral flux estimations and simplified SEE cross sections according to methods described in *Heavy Ion Orbital Environment Single-Event Effects Estimations*. A minimum shielding configuration of 100mils (2.54mm) of aluminum, and worst-week solar activity (this is similar to a 99% upper bound for the environment) is assumed. Using the 95% upper bounds, the event rates for SEUs are shown in Table 8-2.

Table 8-2. SEU Event Rate Calculations for Worst-Week LEO and GEO Orbits

Orbit Type	Onset LET (MeV·cm^2/mg)	σ_{SAT} (cm^2)	Event Rate (/day)	Event Rate (FIT)	MTBE (YEARS)
LEO (ISS)	1.0000	5.00E-05	1.28E-06	5.33E+01	2.14E+03
GEO			1.05E-05	4.36E+02	2.62E+02

8.5 Summary of Radiation Hardness

- The DAC39RF10-SP does not exhibit SEL or SEFI beyond an LET of 120 MeV·cm^2/mg using datasheet maximum supply voltages and Tj = 125°C.
- The DAC's JESD204C link in the tested JMODEs always self-recovers from radiation events and without user intervention.
- The DAC in the tested JMODEs exhibits no functional interrupts (SEFIs) or performance degradations under the beam.
- No user-programmable or fuse-backed device registers are corrupted under the beam.
- Calibration and trim vectors are not corrupted under the beam.
- It is important to follow TI's recommendations when using the DAC39RRF10-SP in hi-rel systems and environments. Special care was taken in designing this product to provide robust hardness against and automatic recovery from single-events.
- The DAC39RF10-SP does not exhibit performance degradation up to 300 krad(Si) of TID and this data is presented in a separate report.

9 References

1. A. J. Tylka, J. H. Adams, P. R. Boberg, et al.,"CREME96: A Revision of the Cosmic Ray Effects on Micro-Electronics Code", *IEEE Trans. on Nucl. Sci., Vol. 44(6)*, Dec. 1997, pp. 2150-2160.
2. A. J. Tylka, W. F. Dietrich, and P. R. Boberg, "Probability distributions of high-energy solar-heavy-ion fluxes from IMP-8: 1973-1996", *IEEE Trans. on Nucl. Sci.,Vol. 44(6)*, Dec. 1997, pp. 2140-2149.
3. Cyclotron Institute, Texas A&M University, *Texas A&M University Cyclotron Institute Radiation Effects Facility*, webpage.
4. D. Kececioglu, *Reliability and Life Testing Handbook*, Vol. 1, PTR Prentice Hall, New Jersey, 1993, pp. 186-193.
5. G. Bruguier and J. M. Palau, "Single particle-induced latchup", *IEEE Trans. Nucl. Sci., Vol. 43(2)*, Mar. 1996, pp. 522-532.
6. M. Shoga and D. Binder, "Theory of Single Event Latchup in Complementary Metal-Oxide Semiconductor Integrated Circuits", *IEEE Trans. Nucl. Sci., Vol. 33(6)*, Dec. 1986, pp. 1714-1717.
7. Texas Instruments, *Radiation Handbook for Electronics*, e-book.
8. Vanderbilt University, *ISDE CRÈME-MC*, webpage.
9. Ziegler, James F. *SRIM- The Stopping and Range of Ions in Matter*, webpage.

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A Appendix: Recommendations for Hi-Rel Systems

A.1 Summary of Rad-Hard Design Features

Feature	Radiation Hardening
Writable SPI registers (excluding write-to-clear registers)	Implemented with upset-immune flip-flops. Radiation will not alter their state.
Read-only SPI registers *that return constant values*	Radiation will not alter their state (for example, CHIP_TYPE, CHIP_ID, CHIP_VERSION, VENDOR_ID).
Read-only SPI status registers associated with JESD204C physical or link layers (excluding write-to-clear registers)	The value returned may be affected by radiation (SYSREF_POS, LINK_UP, JSYNC_STATE, PLL_LOCKED, LANE_ARR, FIFO_STATUS, JCAP_STATUS, JCAP, BER_CNT, LANE_EQS, ESDONE, ESVO_S, ECOUNT, RXDMUX, CDRPHASE, RXCSA_S).
FUSE_DONE register	FUSE_DONE is upset-immune.
OCSTS register	Once the PHY is initialized and offset calibration is completed, OCSTS returns offset values that are upset-immune. However, an upset can cause a PHY PLL to lose lock which can re-trigger the offset calibration process, generating new offset calibration values.
Sticky SPI status registers (write-to-clear)	These bits get set when certain events occur in upset-vulnerable logic. An upset can cause the event to occur and set the sticky bit. An upset may also prevent an event from setting the sticky bit, however this is unlikely as the window of time that this can occur is very small. Once the sticky bit is set, an upset will *not* clear it (the flop that is read by SPI is upset immune).Examples: LANE_ERR, PLL_LOCK_LOST, SYS_ALM, REALIGNED, CLK_REALIGNED
JESD204C receiver	The JESD204C receiver is not upset-immune, but is designed to be free from functional interrupts (can recover automatically from upsets). See JESD204C Reliability section below.
Interpolation filters (DUC and DES2X filters)	The interpolation filters are not upset-immune and will generate glitches when upset. They do not suffer from functional interrupts.
NCOs in DUCs	See NCO Reliability section below.
Temperature sensor	The ADC inside the temperature sensor is not upset-immune. To improve reliability, it is recommended that TS_TEMP be read 3 or more times and the median value computed.

A.2 SPI Programming

The SPI interface and register set are implemented with upset-immune logic. The state of writable SPI registers will not be altered by radiation. The Fast-Reconfiguration interface is not upset-immune and should not be enabled in radiation environments.

A.3 JESD204C Reliability

The JESD204C receiver is implemented with high-speed flip-flops that are not single-upset-immune. As a result, the JESD204C link can experience various errors when exposed to radiation.

To improve the overall reliability of the link and verify the link can automatically recover from an upset, several recommendations must be followed.

1. Use subclass 1 operation by setting SUBCLASS = 1.
2. 64b/66b link encoding (JENC = 1) is preferred over 8b/10b encoding. The 64b/66b link layer provides full-time block and EMB synchronization (pilot) signals, so misalignment caused by radiation can be detected quickly and consistently. In contrast, the 8b/10b link layer relies on synchronization characters that do not have a high occurrence rate, so misalignment takes longer to detect.
3. Use a periodic and continuous SYSREF signal. Keep SYSREF alignment enabled at all times in the Tx and Rx devices. If radiation upsets the Tx or Rx LMFC/LEMC, the SYSREF signal will re-establish its phase and keep the Rx and Tx synchronized. If this recommendation is not followed, radiation can cause a persistent change in the link latency, or cause lanes to be persistently misaligned (causing persistent, corrupt samples to be sent to the DAC).
4. The adaptive equalizer loop in the PHY is not implemented for a radiation environment. Static equalization is recommended. See Equalizer Usage in Radiation Environments below.
5. The Tx logic device that provides data to the Rx must be designed with radiation tolerance in mind. Recommendations include:
    a. When possible, align counters continuously to SYSREF.

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   b. FIFOs must have a means to detect and recover automatically from upsets that can cause overflow or underflow conditions.

6. At this time, there is no known radiation-induced condition that causes the receiver to experience a functional interrupt (link goes down and remains down). However, the user can program JTT to get an additional level of protection from functional interrupts.

A.4 Equalizer Usage in Radiation Environments

Adaptive equalization is not supported in radiation environments. A particle upset can disturb the adaptive equalizer and recovery is not guaranteed. In hi-rel applications, the user should program EQ_OVR = 1 and program a fixed equalizer level using EQLEVEL.

The adaptive equalizer can be used during prototyping to determine a good level to use. Follow this procedure:

1. Enable the receiver with adaptive equalization (EQMODE=1, then JESD_EN=1).
2. Verify data is received successfully. Read EQLEVEL_S to get the current state of the adaptive equalizer. Multiple reads are recommended to verify the adaptation loop has settled. Record the value for future use (for example, in host system firmware).
3. In the radiation environment, enable the receiver with fixed equalization. Program EQLEVEL to the value obtained in step 2.

A.5 NCO Reliability

The NCO does not include radiation immune flip-flops. However there are several strategies that can be employed to make sure the NCO recovers from upset events. These are summarized in the following table and detailed in the following sections.

Strategy	Summary
1	Protect frequency and phase using SYSREF or JESD204C interface • Appropriate for phased arrays using more than one DAC39RF10-SP product • Maintains phase coherency between multiple DAC39RF10-SP chips or other components • NCO frequency must be a harmonic of SYSREF or the JESD204C synchronization bit
2	Protect frequency only using SYSREF • Appropriate for systems not requiring phase coherency • NCO frequency is not restricted to a harmonic of SYSREF • Cannot maintain phase coherence between multiple NCOs (even within one DAC39RF10-SP)
3	NCO self-sync (NCO_SS), and NCO self-coherent mode (NCO_SC) • Appropriate for phased array systems utilizing one DAC39RF-100SP, or for generating multi-tone signals with phase coherency (DDS_EN = 1) • SYSREF is not required • NCO frequency is not restricted to a harmonic of SYSREF • Phase coherency is maintained between the four NCOs inside one DAC39RF10-SP • No phase coherency is maintained with components outside the DAC39RF10-SP

A.6 NCO Frequency and Phase Correction (Strategy #1)

This strategy uses a periodic reference signal to correct any upsets in the NCO accumulator. This strategy is appropriate for phased-array systems or other systems where the NCO phase must remain coherent with other system components, including other DAC39RF10-SP parts.

1. Program NCO_AR = 1 to configure the accumulator to be reset on every synchronization event.
2. Configure the NCO to use SYSREF as the synchronization source (NCO_SYNC_SRC = 2). Program SPI_SYNC = 1.
3. Verify the SYSREF generator is configured for continuous/periodic output.
4. Since the accumulator will be reset periodically, you must ensure that the programmed NCO frequency is an integer multiple of the SYSREF frequency. Consider the frequency raster that your system requires when you choose the SYSREF frequency.

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5. If you cannot choose a SYSREF frequency that satisfies your frequency raster and is also a sub-harmonic of the multi-frame/EMB frequency, then you can use the LSB of the JESD204C data stream to periodically synchronize the NCO. Use NCO_SYNC_SRC = 3, and provide a periodic reference signal on the LSB of the I samples for DUC0.
6. If any NCO accumulator or internal frequency register is upset, it will be restored on the next synchronization event.

A.7 NCO Frequency Correction (Strategy #2)

This strategy also uses a periodic synchronization signal, but the NCO accumulator is not reset. Only the internal frequency registers inside each NCO are corrected by the synchronization signal. This ensures the NCO returns to the proper frequency after an upset occurs, but the phase of the NCO is not corrected. This strategy is appropriate for non-phased-array systems where an occasional, arbitrary phase jump can be tolerated.

1. Program NCO_AR = 0 to configure the accumulator to NOT be reset by a synchronization event.
2. Configure the NCO to use SYSREF as the synchronization source (NCO_SYNC_SRC = 2). Program SPI_SYNC = 1.
3. Verify the SYSREF generator is configured for continuous/periodic output.
4. Since the accumulator is not reset periodically, you have the freedom to program any NCO frequency regardless of the SYSREF frequency. The period of SYSREF must still be a multiple of the multi-frame/EMB period.
5. While the NCO is operating, any upset to its internal frequency register will be corrected on the next SYSREF pulse (the frequency word is re-copied from the SEU-immune FREQ register). The NCO will operate for a brief time at an improper frequency before returning to the correct frequency (but with arbitrary phase).

A.8 NCO Self-Sync/Self-Coherent Mode (Strategy #3)

This strategy uses an internal counter to continuously self-synchronize the NCOs and also configures all four NCOs to share a common phase reference counter. This protects the frequency of all NCOs and protects the phase difference between all NCOs (by sharing a common reference). In DDS mode, it also protects the amplitude setting of each NCO. This mode is appropriate for a multi-DUC, phased-array system utilizing a single DAC39RF10-SP part. It is also appropriate for applications that use the DAC to generate tones and do not want to provide a SYSREF signal. It can also be used in DDS mode applications, specifically ones that use multiple NCOs to cancel out harmonics in the DAC or external amplifier (where phase coherency between NCOs must be maintained).

1. Program NCO_AR = 0 to configure the accumulator to NOT be reset by a synchronization event.
2. Configure the NCOs for self-coherent mode by setting NCO_SC = 1.
3. Configure the NCOs for self-synchronizing mode by setting NCO_SS = 1.
4. While the NCO is operating, any upset to its frequency or phase will be corrected on the next internal synchronization event (see NCO_SS). If the shared reference counter is upset, all NCOs will experience a phase jump but will maintain coherency with respect to each other (they share a common reference counter).

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