*Technical White Paper*

# *Operational Amplifier Stability Theory and Compensation Methods*

*Art Kay, Collin Wells*

**ABSTRACT**

Operational Amplifiers (op amps) can become unstable when driving a capacitive load or from capacitance on the inverting input. This instability in op amps can show up as overshoot and ringing in response to an input, load transients, and—in the worst cases—an oscillation that is continuous and independent of the input signal. For example, an unstable amplifier can oscillate even when the input signal is a DC voltage. This document explains the theory behind what causes instability and provides options to eliminate this problem.

## Table of Contents

## Trademarks

E2E™ and TINA-TI™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

# 1 Introduction

This introduction provides simplified explanations of the factors that cause stability problems in operational amplifiers. The section introduces common examples of issues and common stabilizing tools. Finally, the introduction demonstrates how the datasheets for TI's operational amplifiers provide quick and simple designs for op amp stability, and TI's designs do not require the complex methods covered later in the document.

## 1.1 Simple Analogy Explaining Instability

Figure 1-1 illustrates an op amp circuit with stability issues and an equivalent control system diagram. Control system diagrams and control system terminology are often used in op amp stability discussions because much of the literature for stability was developed for control systems and then applied to op amp circuits. The inputs of the op amp correspond to the following blocks for the summing block of the control system:

- The amp open-loop gain ($A_{OL}$) is the control system gain block.
- The op amp feedback network corresponds to the beta feedback block (β).

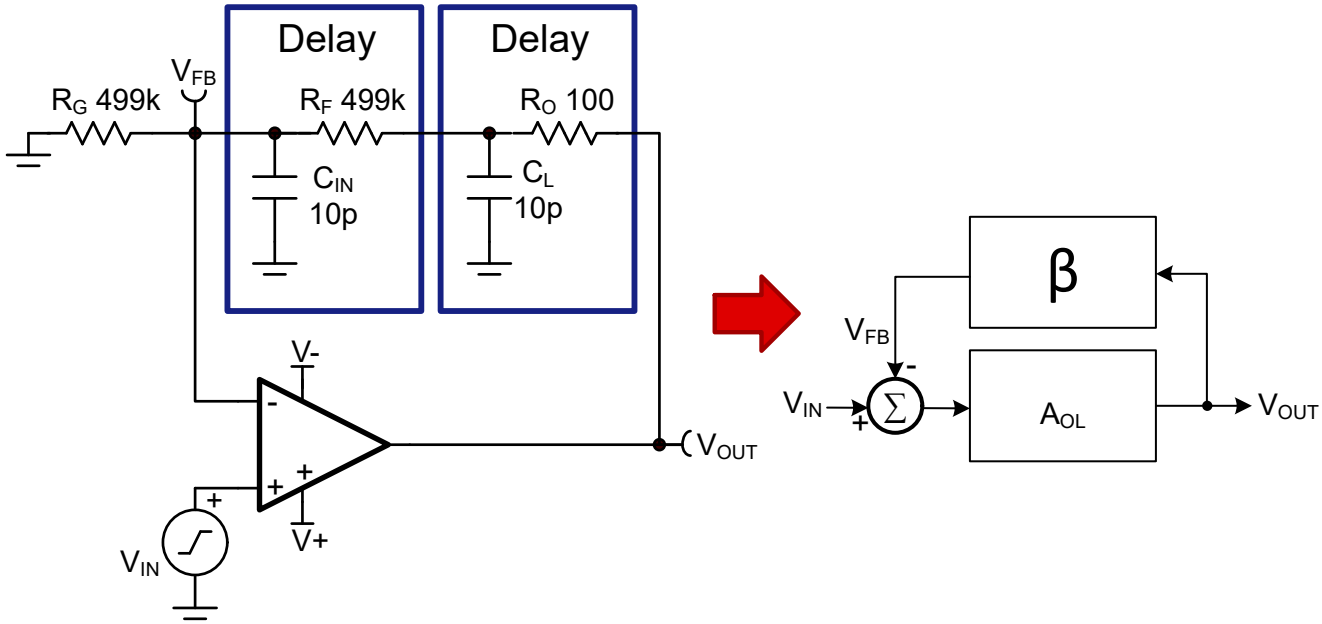


**Figure 1-1. Operational Amplifier Circuit and Control System Equivalent**

The circuit in Figure 1-1 is unstable because of the delay elements in the feedback network. The delay elements are simply RC low pass filters. A low pass filter naturally has a group delay or phase shift. The reason that this feedback delay causes instability can be understood by thinking of the op amp circuit as a control system. The input summing block of the op amp senses the output signal through the feedback network. The output of the summing block is the error signal. In this example, the target for $V_{OUT}$ is 2 × $V_{IN}$. When $V_{OUT}$ = 2$V_{IN}$ the error signal is zero. When the output is too high ($V_{OUT}$ > 2 × $V_{IN}$), the error signal is negative and the op amp tries to drive the output downward. Similarly, when the output is too low ($V_{OUT}$ < 2 × $V_{IN}$), the error signal is positive and the op amp tries to drive the output upward to cancel the error. Thus, the output is a constant value of $V_{OUT}$ = 2$V_{IN}$ when the system is in equilibrium.

However, the functionality of the system assumes the feedback signal ($V_{FB}$) is not significantly delayed. If $V_{FB}$ is significantly delayed, the op amp can incorrectly identify the output as going upward when the output is actually going downward. This outcome creates an error signal with the wrong polarity, which drives the output in the wrong direction. Instability of the op amp is caused by this delay in the feedback signal.

Many engineers see the circuit shown in Figure 1-1 and understand that the feedback delay is a problem, and the general assumption is no one intentionally designs such an impractical circuit. However, the circuit shown in Figure 1-1 is frequently inadvertently created by the internal open-loop output impedance ($R_O$ or $Z_O$), the input capacitance of the op amp, and any parasitic PCB capacitance ($C_{IN}$ = $C_{CM}$+$C_{PCB}$). Figure 1-2 shows the circuit redrawn to emphasize how the delay elements are created in a practical op amp circuit.

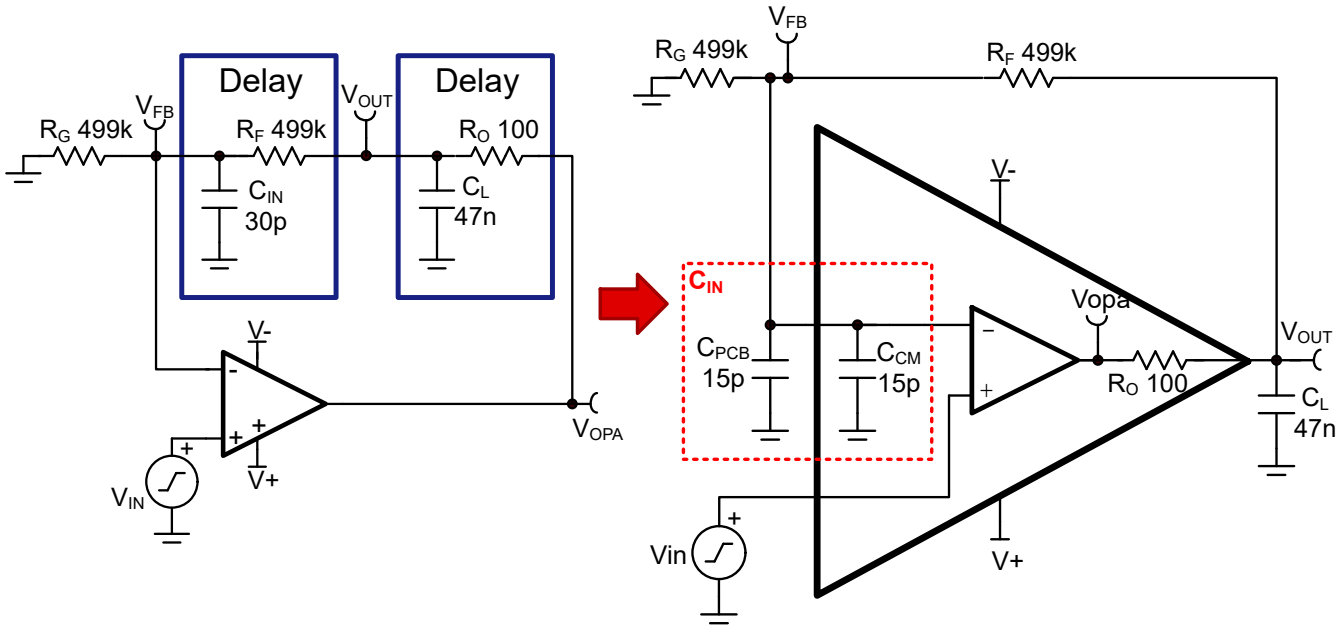


**Figure 1-2. Origin of Delay Elements in a Practical Circuit**

## 1.2 Circuits With Possible Stability Issues

Analyzing and compensating stability problems is one of the most challenging disciplines for analog system designers. Although developing a deep understanding on the subject of stability can take time and effort, identifying potential stability issues is relatively easy with a simple circuit inspection. For engineers who are new to stability analysis, identifying the problem is an important first step. Fortunately, this document helps new engineers compensate the amplifier to solve the stability issue, and many additional resources are available which provide support and assistance with these types of issues (for example, the Texas Instruments E2E™ community).

Figure 1-3 through Figure 1-5 illustrate examples of circuits with stability issues due to a load capacitance ($C_L$) on the output of the op amp. This load capacitance creates a delay in the feedback signal due to a delay from the RC time constant added by the internal open-loop output resistance $R_O C_L$. Figure 1-3 shows a common application where an op amp is used to buffer a voltage reference which drives an analog-to-digital converter. The problem in this application is that the output capacitors, C3 and C4, are directly connected to the amplifier output and this normally leads to stability problems. Figure 1-4 shows an op amp circuit driving a long cable. Cables can have significant capacitance per unit length, and can often introduce stability issues. Figure 1-5 shows an op amp driving a power MOSFET. This is a common application as the gate capacitance of a power MOSFET can be significant. The problem in each case is too much capacitance connected to the output of the op amp. A common correction for this type of issue is to use an isolation resistor between the op amp output and the load capacitance. Methods for selecting this resistor (see Isolation Resistor ($R_{ISO}$) Method) are covered later in this document.

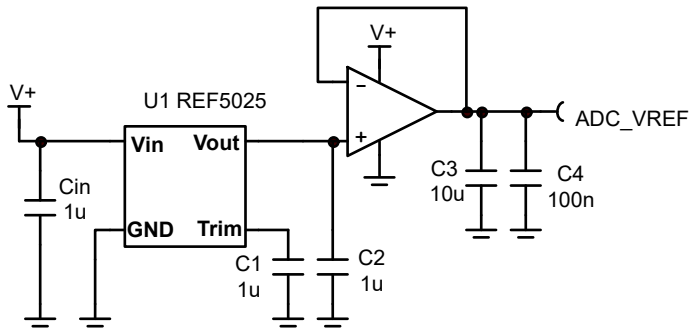


**Figure 1-3. Reference Buffer Capacitive Load Issue**

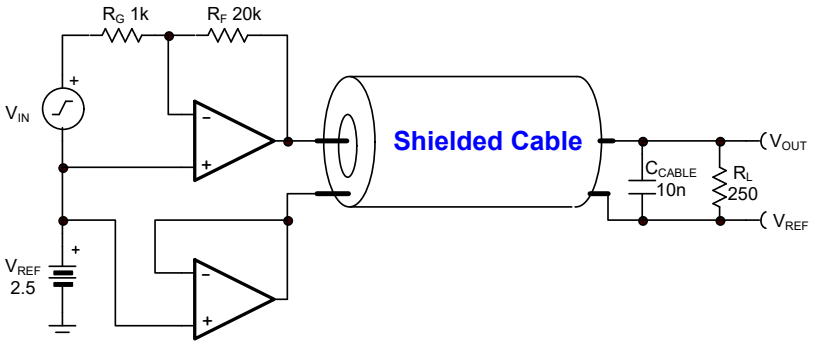


**Figure 1-4. Cable Drive Capacitive Load Issue**

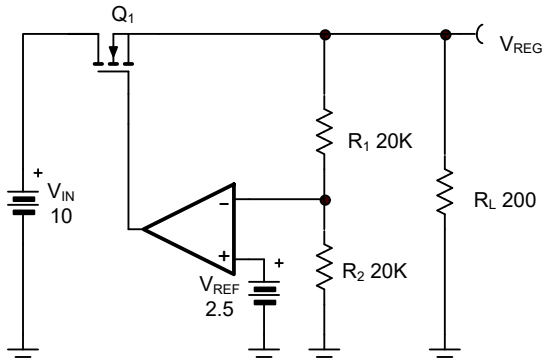


**Figure 1-5. MOSFET Gate Drive Capacitive Load Issue**

Figure 1-6 through Figure 1-8 illustrate examples of circuits with stability issues due to a capacitance on the inverting node of the op amp or large feedback resistors. The feedback delay that causes the instability is from the RC time constant of $R_F C_{IN}$. Figure 1-6 shows a photodiode transimpedance amplifier. Photodiodes can have significant parasitic capacitance and these circuits often use large feedback resistors for high transimpedance gain. Similar to the transimpedance circuit, input protection diodes can have high capacitance (see Figure 1-7). Also, low-power circuits generally use large feedback resistors to minimize power consumption. In this case, even if the input capacitance is relatively low, the large feedback elements can cause instability (see Figure 1-8). Stability problems related to capacitance on the inverting node can be corrected by adding a feedback capacitor. The details behind selecting this capacitor are covered later in this document (see Stability Corrections for Capacitance on the Inverting Node).

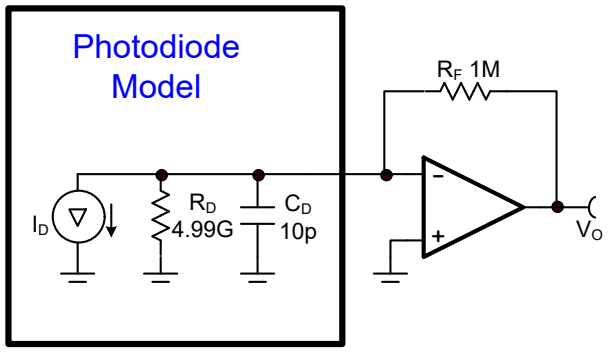


**Figure 1-6. Photodiode Transimpedance Amplifier Adds Capacitance to Inverting Node**

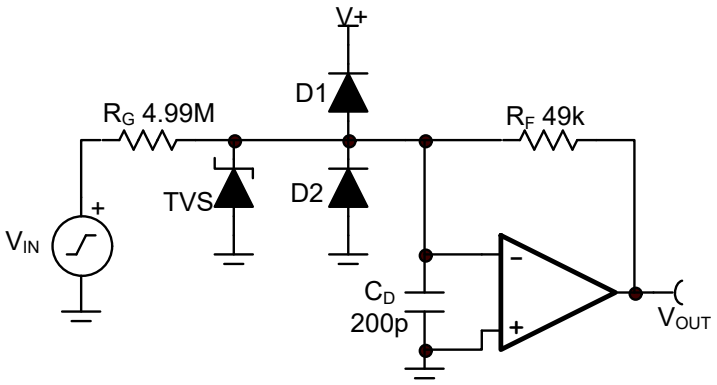


**Figure 1-7. Input Protection Diodes Add Capacitance to Inverting Node**

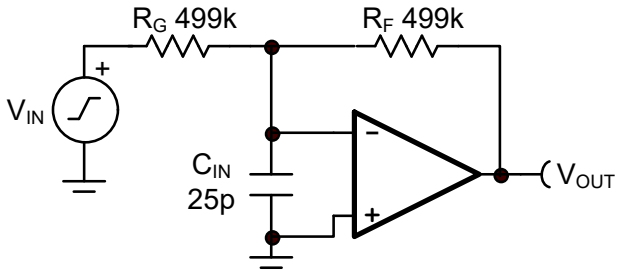


**Figure 1-8. Low-Power Circuit With Large Feedback Impacted by Capacitance on Inverting Node**

## 1.3 Simple Stability Correction Based on Datasheet Plots

Op amps can have stability problems when driving capacitive loads. The specific amount of capacitance that causes a stability issue is different for different op amp devices, based on the value of $Z_O$. Some op amps are specifically designed to operate with larger capacitive loads. Many op amp datasheets provide a graph of small-signal overshoot versus capacitive load or phase margin versus capacitive load. Percentage overshoot (PO) and phase margin (PM) are directly related to each other and engineers can convert between the two mathematically. A lower phase margin corresponds to a higher overshoot and decreased stability. TI recommends a phase margin of greater than 45° or less than 23% overshoot for good stability. Some engineers accept a phase margin as low as 30° or 41% overshoot. Engineers can adjust the criteria according to the application requirements.

Regardless of the criteria, engineers can use the datasheet graph to determine if the capacitive load is acceptable. In some cases, the graph includes multiple curves to show how different isolation resistors extend the capacitive load range for stable operation. The graphs also specify the op amp configuration used to drive the capacitive load because the configuration affects the stability. Figure 1-9 shows the small-signal overshoot graph for OPA192 in a buffer configuration. For this device, the maximum capacitive load for 20% overshoot and $R_{ISO}$ = 0Ω is about 200pF. For a 50Ω isolation resistor, the circuit can drive capacitances well beyond 1nF and still keep overshoot less than 20%. The 25Ω isolation resistance also extends the capacitance range well beyond 1nF, however, the overshoot increases to 25% over some capacitance ranges.

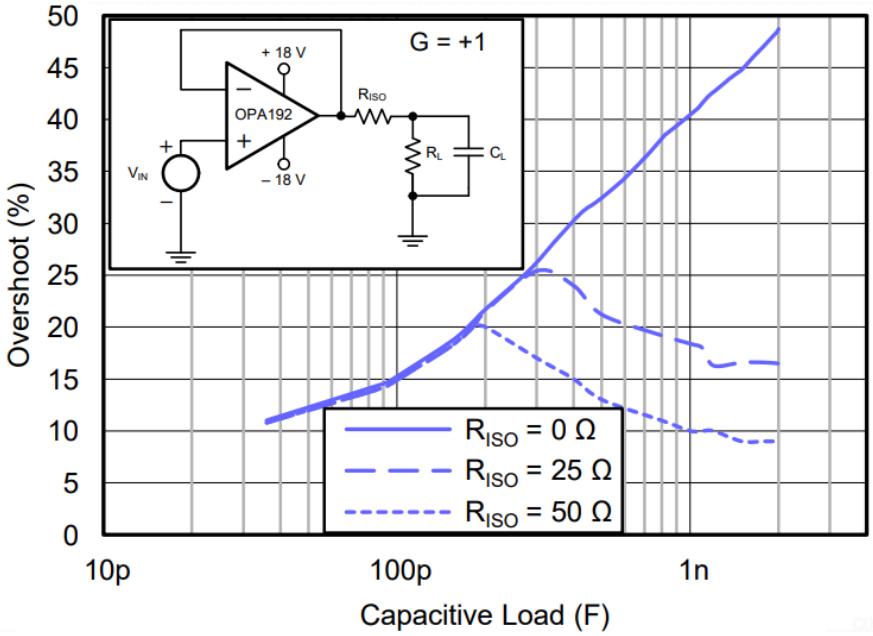


**Figure 1-9. Overshoot Versus Capacitive Load for OPA192 in G = +1V/V**

## 1.4 Introducing Lab Tools and Measurements

The stability of op amps can be measured with a signal generator and an oscilloscope. This type of testing is sometimes called non-invasive because the testing can be done without circuit modification, such as opening the feedback loop. This testing is normally done by applying a small signal input square wave and measuring the transient overshoot on the output signal. A small signal is generally defined as less than 100mVpp, but the actual threshold depends on the internal design of the op amp. Since the small signal threshold depends on the internal design of the op amp, TI's advice is to use a 10mVpp square wave to be certain that the input is small signal. For this test, the magnitude of the overshoot is directly related to the phase margin. Figure 1-10 illustrates the small signal square wave test, and Indirect (Non-Invasive) Stability Tests explains how to judge stability based on this test.

Another approach to measuring stability is to use a network analyzer. The network analyzer is used to measure the closed-loop frequency response (for example, gain and phase versus frequency). When using this method, instability can be identified by a large gain peak and a rapid phase shift of approximately 90°. Figure 1-11 shows a typical test setup that uses a network analyzer to test stability. Often, stability issues can be resolved using the simulation in Figure 1-11. Assuming the op amp is properly modeled, stability simulations accurately reflect the real-world equivalent circuit.

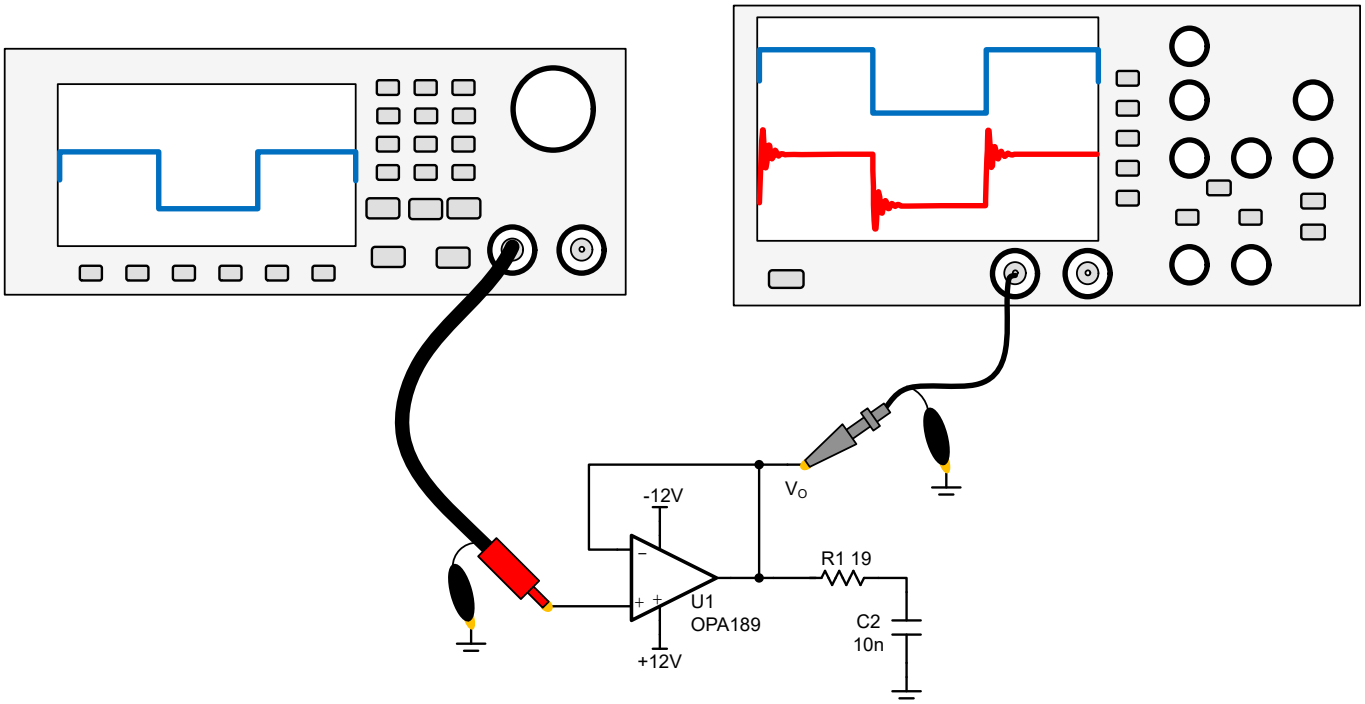


**Figure 1-10. Scope and Signal Generator Setup for Stability Measurement**

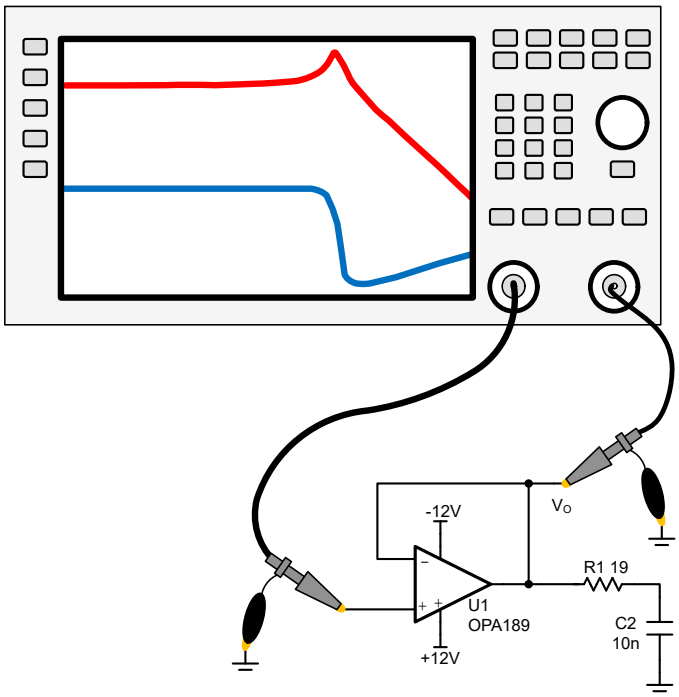


**Figure 1-11. Network Analyzer Setup for Stability Measurement**

## 2 Stability Theory for Operational Amplifiers

This section introduces the terminology and fundamentals of analyzing the stability of operational amplifiers. This section covers open-loop and closed-loop methods for testing the stability of op amps. The section also discusses the specific parameters that impact the stability of op amps.

## 2.1 Poles and Zeros

Understanding poles and zeros is a critical skill required for solving the stability problems of op amps. Poles are the roots of the s-domain equation in the denominator of the transfer function, and zeros are roots of the numerator (see Equation 1). Figure 2-1 shows the bode plot for a transfer function with a single pole. At the pole frequency, the magnitude plot is 3dB below the DC value ($G_{DC}$). After the pole frequency, the gain decreases by 20dB/decade. At the pole frequency, the phase plot has dropped by 45° from the DC phase. The phase shift starts approximately one decade before the pole and ends approximately one decade after the pole frequency for a total phase shift of –90°. The phase shift decreases at a rate of 45°/decade from roughly $f_P/10$ to $f_P \times 10$. Equation 2 shows the complex transfer function for a system with a single pole. Equation 3 shows the transfer functions gain magnitude in V/V and Equation 4 shows the phase shift.

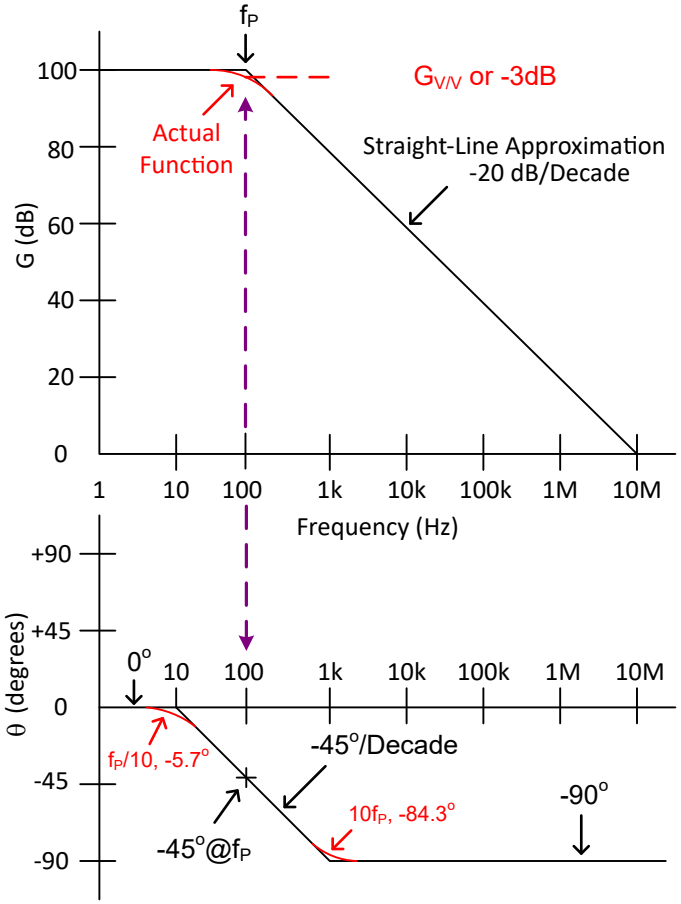


**Figure 2-1. Magnitude and Phase Graph of a Pole**

where s = j × ω, and$j = \sqrt{-1}$ (1)

$$G_{V/V} = \frac{V_{OUT}}{V_{IN}} = \frac{G_{DC}}{\left(\frac{s}{\omega P}\right) + 1} = \frac{G_{DC}}{j\left(\frac{f}{f_P}\right) + 1} \quad (2)$$

$$\left|G_{V/V}\right| = \frac{V_{OUT}}{V_{IN}} = \frac{G_{DC}}{\sqrt{\left(\frac{f}{f_P}\right)^2 + 1}} \quad (3)$$

$$\theta = -\tan^{-1}\left(\frac{f}{f_P}\right) \quad (4)$$

Figure 2-2 shows the bode plot for a transfer function with a single zero. At the zero frequency, the magnitude plot is 3dB above the DC value. After the zero frequency, the gain increases by 20dB/decade. At the zero

frequency, the phase plot has increased by 45° from the DC phase. The phase shift starts approximately one decade before the pole and ends approximately one decade after the pole frequency for a total phase shift of +90°. The phase shift increases at a rate of 45°/decade from roughly $f_Z/10$ to $f_Z \times 10$. Equation 5 shows the complex transfer function for a system with a single zero. Equation 6 shows the transfer functions gain magnitude in V/V and Equation 4 shows the phase shift.

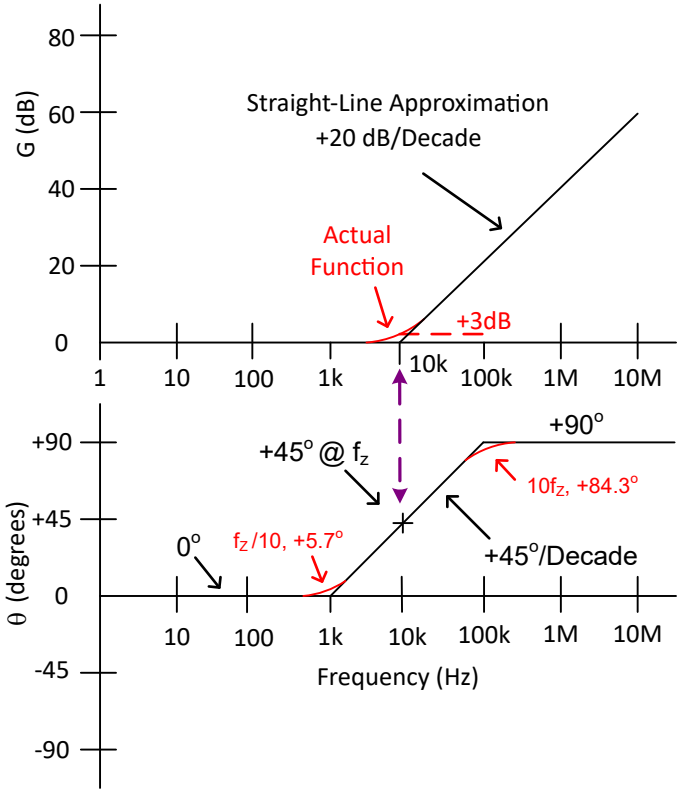


**Figure 2-2. Magnitude and Phase Graph of a Zero**

$$G_{V/V} = \frac{V_{OUT}}{V_{IN}} = G_{DC} \times \left(\left(\frac{s}{\omega_Z}\right) + 1\right) = G_{DC} \times \left(j\left(\frac{f}{f_Z}\right) + 1\right) \quad (5)$$

$$\left|G_{V/V}\right| = \frac{V_{OUT}}{V_{IN}} = G_{DC} \times \sqrt{\left(\frac{f}{f_Z}\right)^2 + 1} \quad (6)$$

$$\theta = \tan^{-1}\left(\frac{f}{f_Z}\right) \quad (7)$$

## 2.2 Operational Amplifier Model Requirements for Stability Verification

Figure 2-3 illustrates the minimum requirement for an op amp model that can be used for stability testing. The model must accurately match the real $A_{OL}$ over frequency, the open-loop output impedance, and input capacitance of the op-amp. The DC $A_{OL}$ value is modeled with the voltage-controlled voltage source on the input (VCVS1 = –1M V/V, for 120dB). The dominant pole is modeled with simple RC low pass filters. The output of the low pass filter is buffered with a voltage-controlled voltage source in a gain of 1V/V. The open-loop output impedance ($Z_O$) is modeled with a simple resistor in this case, but many devices require a complex impedance.

Figure 2-4 illustrates the graph of $A_{OL}$ for Figure 2-3. Notice that the DC $A_{OL}$ corresponds to VCVS1, and the dominant pole corresponds to 1/(2 × π × R1 × C1). Note that the dominant pole imparts a –90° phase shift. The phase shift at low frequency is 180° due to the op amps negative feedback. Beyond the dominant pole, many op amps have multiple secondary poles and zeros near the unity gain frequency of the amplifier, as well as input capacitance (see Modeling the $A_{OL}$ Secondary Poles and Zeros and Input Capacitance for details).

Figure 2-4 illustrates the open-loop output impedance for the model shown in Figure 2-3. This model uses a resistive open-loop output impedance ($Z_O$). Resistive $Z_O$ (denoted as $R_O$) is the easiest to understand and also the better case from a stability perspective. The initial theory, assuming $Z_O$ is resistive, is explained in this document, and later shows how a complex $Z_O$ can impact stability. Practical op amps can have a resistive $Z_O$ or complex $Z_O$. *Modeling the output impedance of an op amp for stability analysis* explains how to build a model with a complex $Z_O$. Most Texas Instruments' models accurately model both $Z_O$ and $A_{OL}$ over frequency so individually developing these models is generally unnecessary.

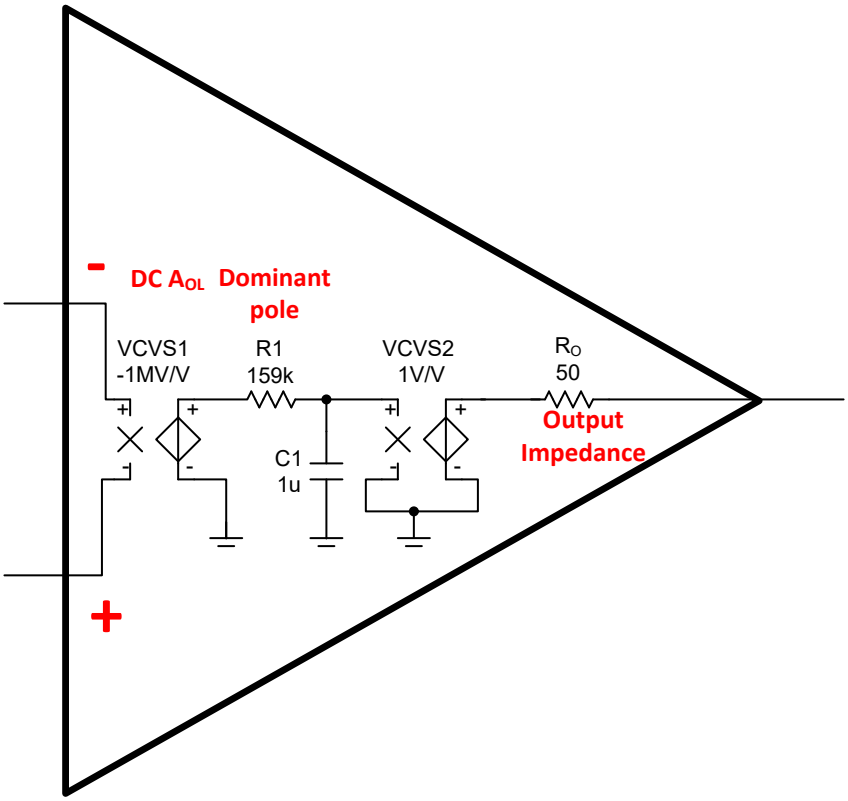


**Figure 2-3. Operational Amplifier Model for Stability Simulations**

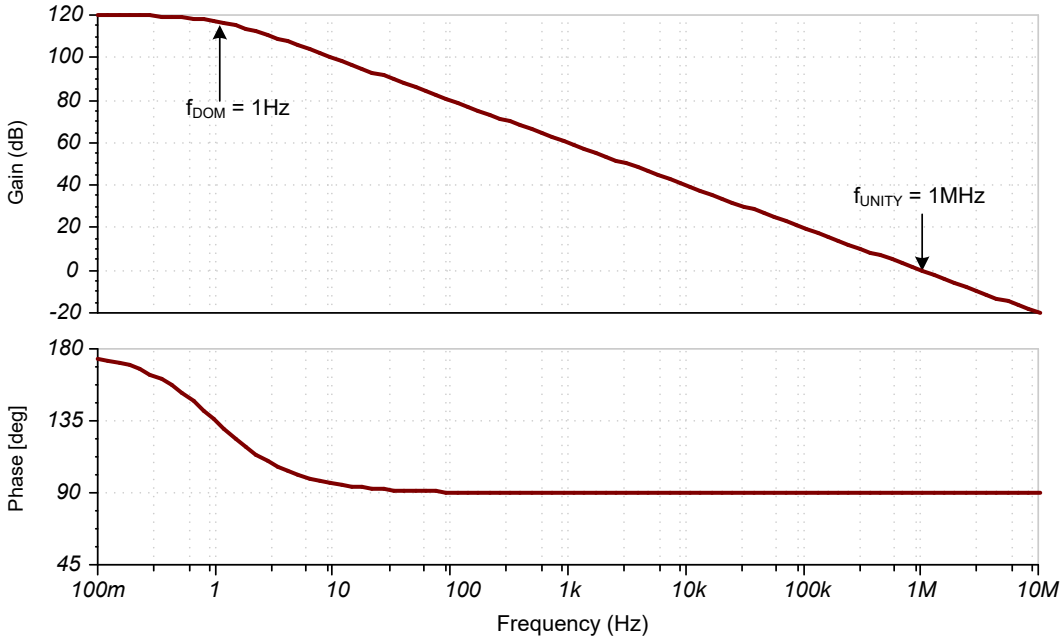


**Figure 2-4. Open-Loop Gain Versus Frequency for Stability Model**

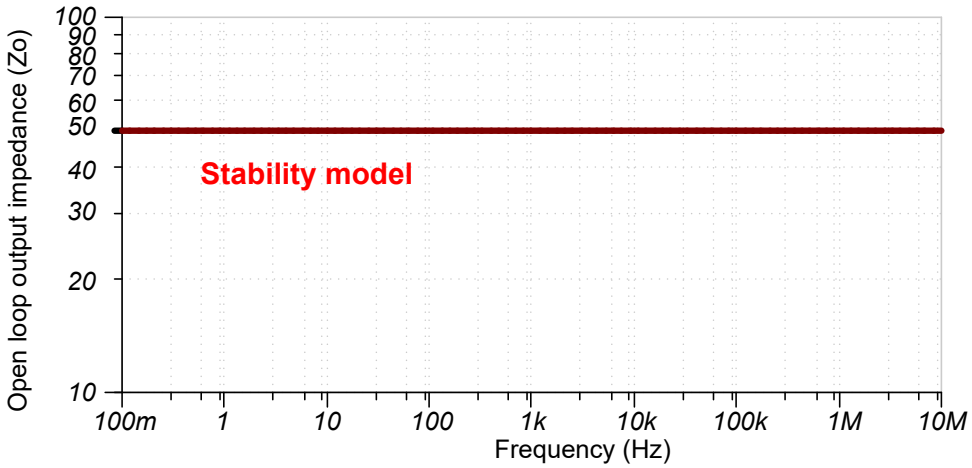


**Figure 2-5. Resistive Open-Loop Output Impedance Versus Frequency for Stability Model**

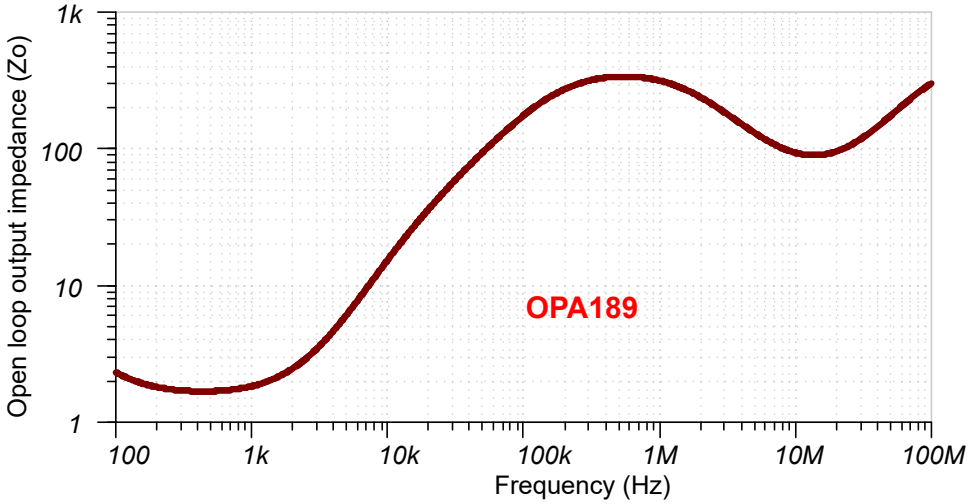


**Figure 2-6. Complex, Open-Loop, Output Impedance Example (OPA189)**

## 2.3 Stability Definitions Based on Control Loop Model

Figure 2-7 shows a simple non-inverting op amp circuit with a simple control-systems equivalent diagram. The control diagram models the op amp input as a summing block with the feedback path inverted. The open-loop gain across frequency is modeled as shown in Figure 2-3. The op amp feedback network forms the β factor in the control system. The feedback factor is the gain from the output to the inverting amplifier node ($\beta = V_{FB} / V_{OUT}$). For this example, β is a simple voltage divider, but in many cases, β can be a more complex relationship. The closed-loop gain equation can be derived by applying the input and output signals to the control system diagram and applying simple algebra (see Equation 10). The denominator of the closed-loop gain equation contains the term $A_{OL} \times \beta$. This term is critical to stability analysis and is called loop gain (see Equation 11). For very large values of loop gain, the closed-loop gain can be approximated as 1/β. The limit function in Equation 12 shows that when $A_{OL} \times \beta$ is much greater than 1, the 1 in the denominator can be ignored and the $A_{OL}$ terms cancel out leaving $A_{CL} \cong 1/\beta$. Substituting Equation 9 into Equation 12 and applying algebra produces the familiar gain equation for a non-inverting amplifier ($G = R_F / R_G + 1$).

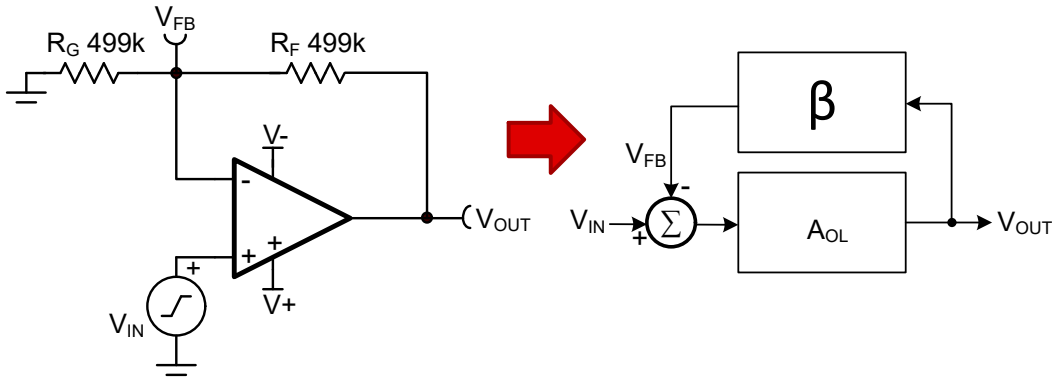


**Figure 2-7. Op Amp Circuit and Equivalent Controls System Diagram**

$$A_{OL} = \text{Open Loop Gain over frequency} \tag{8}$$

$$\beta = \text{Feedback Factor} = \frac{V_{FB}}{V_{OUT}} = \frac{R_G}{R_G + R_F} \tag{9}$$

$$A_{CL} = \text{Closed Loop Gain} = \frac{A_{OL}}{1 + A_{OL}\beta} \tag{10}$$

$$A_{OL}\beta = \text{Loop Gain} \tag{11}$$

$$A_{CL} = \lim_{A_{OL}\beta \to \infty} \left( \frac{A_{OL}}{1 + A_{OL}\beta} \right) \cong \frac{1}{\beta} = 1 + \frac{R_F}{R_G} \tag{12}$$

The closed-loop gain equation (Equation 10) can be used to determine amplifier stability. An amplifier is considered unstable when the denominator of $A_{CL}$ is zero. This happens when $A_{OL} \times \beta = -1$. Converting the linear value of loop gain to decibels ($A_{OL} \times \beta = -1$) means that the magnitude of $A_{OL} \times \beta$(dB) = 0dB, and the phase shift $A_{OL} \times \beta$(phase_shift) = –180°. If you remember the analogy in Section 1.1, the instability is due to a delay in the feedback. The –180° phase shift is the feedback delay that causes instability. The op amp *thinks* the output is going up when the output is actually going down. In any case, when loop gain in decibels is 0dB and the phase shift relative to the DC phase is 180°, the closed-loop gain becomes very large and the circuit is unstable. In Section 2.6, you can see that an indirect way of measuring circuit stability in the lab is to look for large gain peaking.

**Note**

**Criteria for stability:**

- Instability happens when the denominator of $A_{CL}$ is zero
- The denominator is zero when $A_{OL} \times \beta = -1$
- $A_{OL}\beta = -1$ sets the denominator of $A_{CL} = 0$
- $A_{OL}\beta = -1$ when $A_{OL}\beta(dB) = 0dB$ *and* $A_{OL}\beta(phase\_shift) = -180°$
- Phase shift is relative to the DC phase

Phase margin describes how close a circuit is to instability. Mathematically, this description is the amount of phase remaining when $A_{OL} \times \beta(dB) = 0dB$ before the phase shift $A_{OL} \times \beta(phase\_shift) = -180°$. For example, if the phase shift relative to DC is 170° when $A_{OL} \times \beta(dB) = 0dB$, then the phase margin is 10°. From a practical perspective, amplifiers with a very low phase margin are effectively nonfunctional. Poor phase margin leads to very large gain peaking, large overshoot, and oscillations. In some cases, the oscillations are continuous even when the input is a DC signal. Some engineers consider cases where the oscillations eventually settle out as an acceptable outcome. However, circuits that are marginally stable have large overshoot and oscillations for any change on the input, power supplies, or output loading.

**Note**

**Definition of phase margin:**

- Phase margin describes how close a circuit is to instability
- When $A_{OL} \times \beta(dB) = 0dB$ the phase margin is the phase remaining before $A_{OL} \times \beta(phase\_shift) = -180°$ and the circuit is unstable
- If the phase shift is 170° when $A_{OL} \times \beta(dB) = 0dB$, than the phase margin is 10°
- On a bode plot, phase margin is the phase shift relative to DC phase when $A_{OL}$ intersects 1/β, or when $A_{OL} \times \beta(dB) = 0dB$ (see Figure 2-8)
- Most op amp circuits have a phase of 180° at DC, so the phase margin can be read directly on the graph where 0° is unstable (see Figure 2-8)

If the phase margin is zero, the circuit generally oscillates continuously. Circuits with a low, but non-zero, phase margin have high gain peaking, large overshoot, and very poor settling times. The recommendations for minimum phase margin differ depending on the engineering reference. TI recommends using a phase margin ≥ 45° for good stability. For some circuits, achieving a 45° phase margin is a challenge, so a phase margin as low as 35° is potentially acceptable. Keep in mind that the parameters impacting stability (such as open-loop output impedance, open-loop gain, and external component values) all have tolerance, so generally, having a phase margin above 45° is advisable so the design is robust across process corners.

**Note**

**Phase margin general guidance:**

- TI recommends a phase margin ≥ 45° for stable circuits
- 45° > Phase margin ≥ 35° is considered marginally stable, but can be acceptable in some cases
- Phase margin < 35° is unstable and leads to large overshoot, gain peaking, and oscillations

When looking at open-loop gain and phase plots, engineers can find the phase margin by looking at the loop-gain phase at the frequency where 1/β intersects with $A_{OL}$. Alternatively, the phase margin can also be found at the frequency where the loop-gain magnitude is 0dB ($A_{OL} \times \beta(dB) = 0dB$). For most amplifiers, the DC loop-gain phase is 180°, so the phase margin is directly read from the graph. In Figure 2-8, the phase starts at 180° and drops to 8° when $A_{OL} \times \beta(dB) = 0dB$, so the phase margin is 8°.

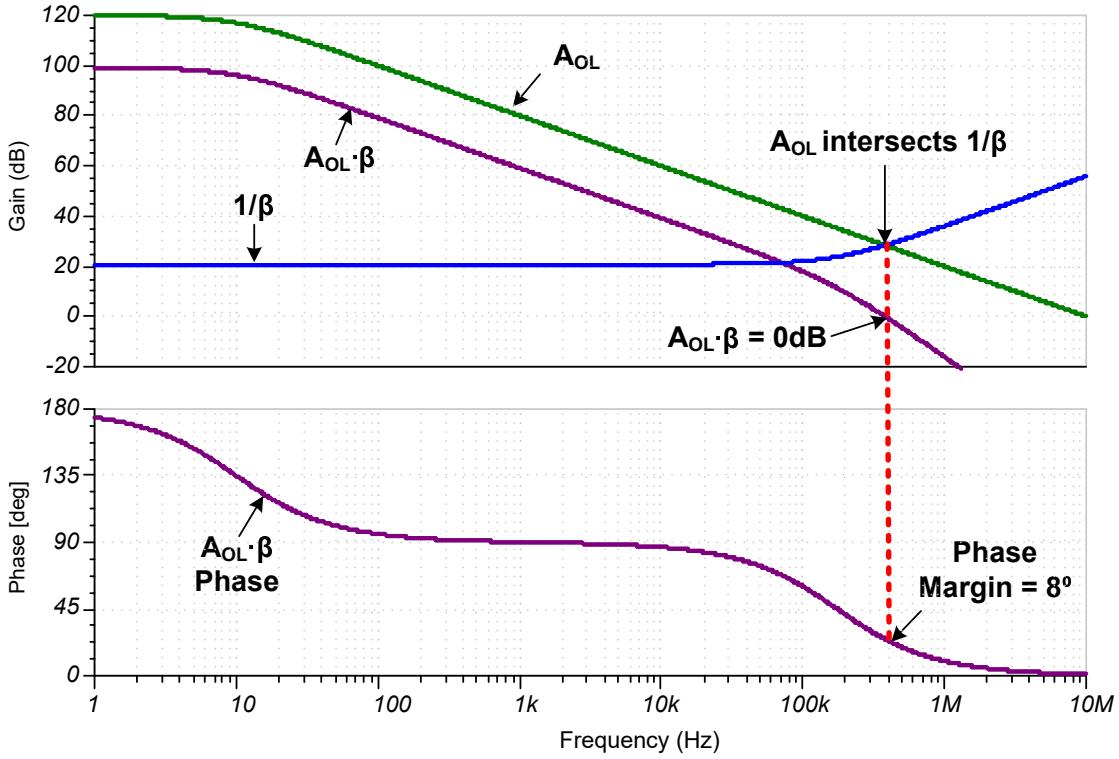


**Figure 2-8. Phase Margin Definition**

## 2.4 Graphing Loop-Gain Based on $A_{OL}$ and 1/β

The $A_{OL}$ curve is specified in the op amp datasheet and the 1/β curve can be approximated as the closed-loop gain of the amplifier. The loop-gain ($A_{OL}$ × β) curve can be derived by subtracting the 1/β curve from the $A_{OL}$ curve. The mathematical proof that allows for the loop-gain calculation uses the laws of logarithms (see Equation 13 and Equation 14). The logarithmic laws apply since our magnitude plots are normally given in decibels, and decibels are logarithmic. Applying the logarithm laws to loop gain shows that loop-gain can be calculated as $A_{OL}$(dB) – 1/β(dB), see Equation 15 and Equation 16. Figure 2-9 provides a graphic example for the loop gain calculation. At low frequency, $A_{OL}$ is 120dB and 1/β is 20dB, so by the calculation: $A_{OL}$ × β(dB) = $A_{OL}$(dB) – 1/β(dB) = 120dB – 20dB = 100dB. For the frequency where $A_{OL}$ = 1/β, the loop-gain is 0dB as expected ($A_{OL}$ × β(dB) = $A_{OL}$(dB) – 1/β(dB) = 20dB – 20dB = 0dB). The same approach can be followed for loop gain phase (see Figure 2-10).

$$\log(A \times B) = \log(A) + \log(B) \tag{13}$$

$$\log(A) = -\log\left(\frac{1}{A}\right) \tag{14}$$

$$20\log(A_{OL}\beta) = 20\log(A_{OL}) - 20\log\left(\frac{1}{\beta}\right) \tag{15}$$

$$A_{OL}\beta(dB) = A_{OL}\left(dB\right) - \frac{1}{\beta}\left(dB\right) \tag{16}$$

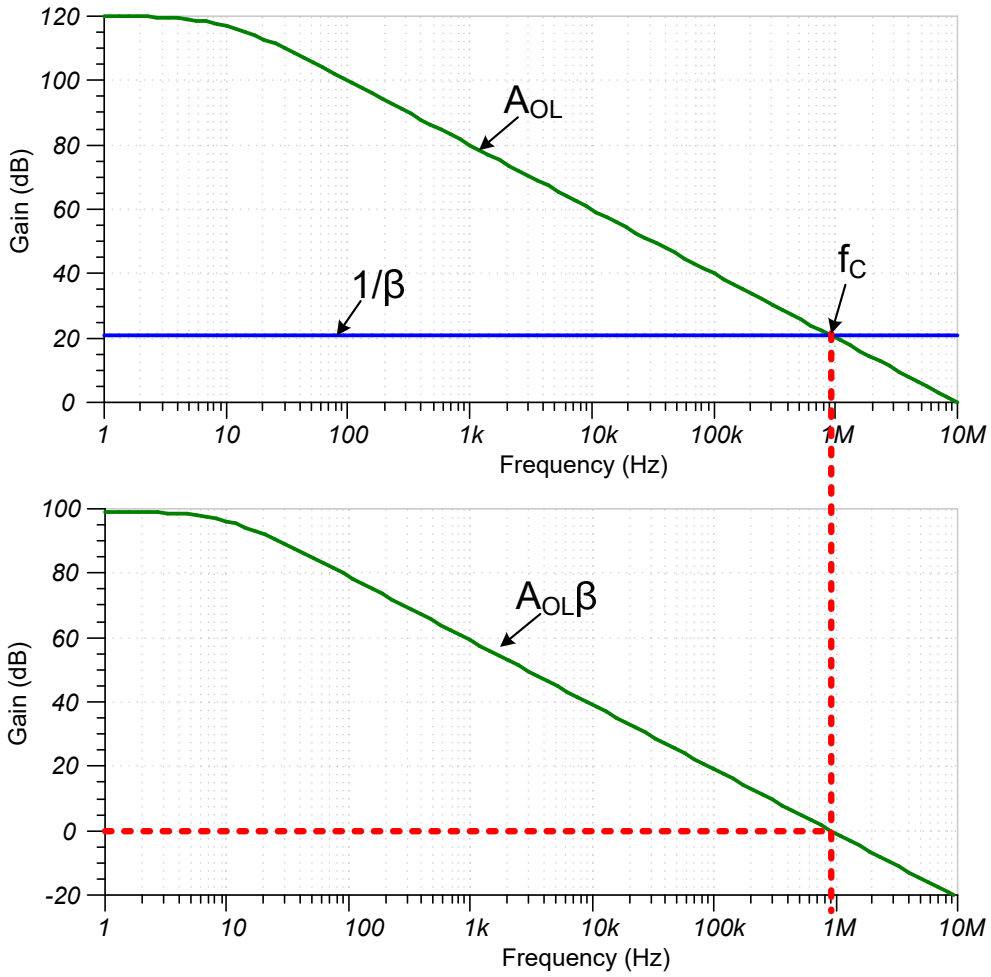


**Figure 2-9. Finding $A_{OL}$ × β Magnitude Graphically Given $A_{OL}$ and 1/β**

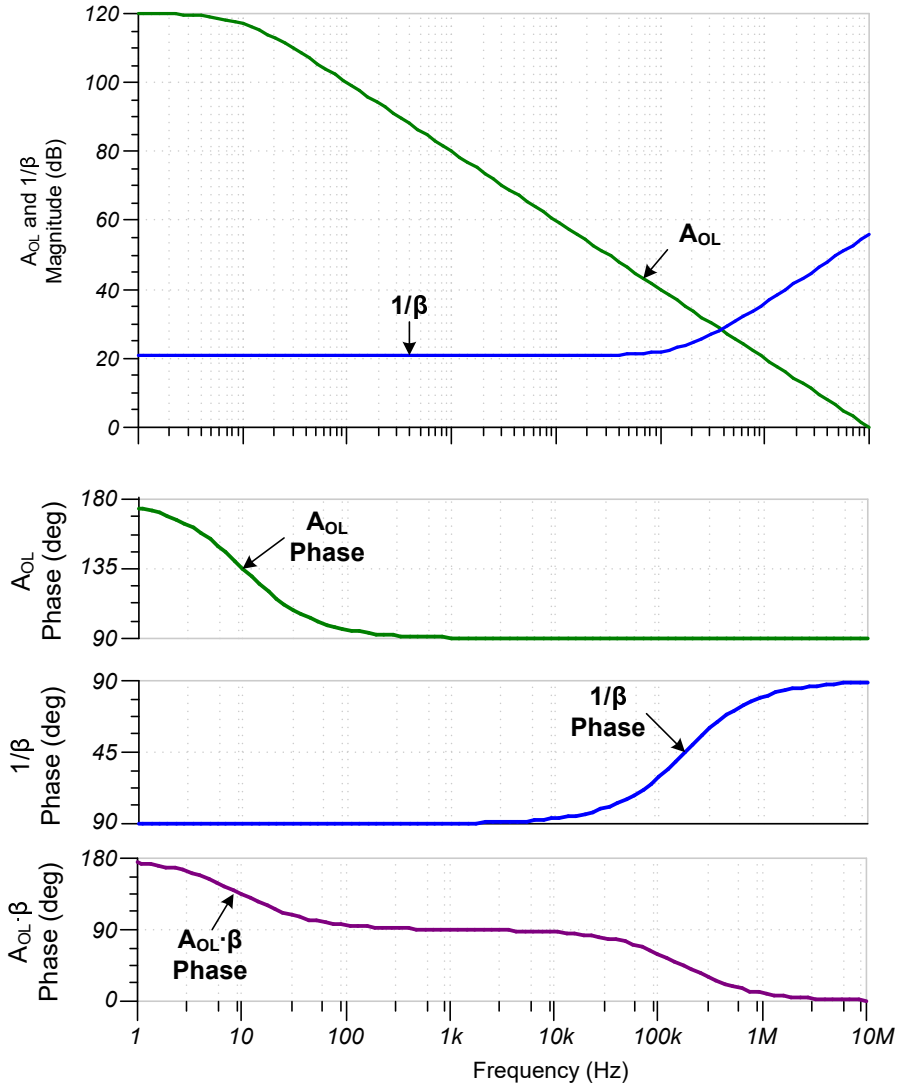


**Figure 2-10. Finding $A_{OL}$ × β Phase Graphically Given $A_{OL}$ and 1/β**

## 2.5 Rate of Closure Stability Test

Section 2.3 showed that the $A_{OL}$, $A_{OL}$ × β, and 1/β magnitude and phase curves can be used to find phase margin and confirm if a circuit is stable or not. The $A_{OL}$ and 1/β curves can also be used to confirm stable operation using a rate-of-closure (ROC) test. In general, the phase margin test is the better way to check stability as this test gives a numerical indication of how stable the circuit is. For example, a phase margin of 45° is acceptable, but 60° is more stable and has room for process variation. The rate-of-closure test really only tells if a circuit is stable or not but does not give any indication of how stable the circuit is. Nevertheless, the test is useful because engineers can immediately verify where the problem is located by graphical inspection. Furthermore, the rate-of-closure test provides insight into the items that need adjusted to fix the stability problem.

The rate-of-closure test examines the slope of the $A_{OL}$ and the 1/β curves where the items intersect. If the magnitude of the difference in slope is equal to 20dB/decade, the circuit is stable (see Figure 2-11). If the ROC ≥ 40dB, the circuit is unstable. For an ROC between 20dB/decade and 40dB/decade, the circuit is marginally stable. Figure 2-11 illustrates an unstable example, which has a 40dB rate of closure, and Figure 2-12 illustrates a stable example, which has a 20dB rate of closure. The rate-of-closure for Figure 2-11 is calculated as ROC = |Slope($A_{OL}$) – Slope(1/β) = |(–20dB/dec) – (+20dB/dec)| = 40dB/dec. The rate-of-closure for Figure 2-12 is calculated as ROC = |Slope($A_{OL}$) – Slope(1/β) = |(–20dB/dec) – (0dB/dec)| = 20dB/dec.

$$\text{Rate\_of\_Closure} = \left|\text{Slope}(A_{OL}) - \text{Slope}\left(\frac{1}{\beta}\right)\right| \tag{17}$$

**Note**

**Rate-of-closure:**

- Rate of closure = 20dB/dec is required for high stability
- 20db/dec < Rate of closure < 40dB/dec is marginally stable
- Rate of closure ≥ 40dB/dec is unstable

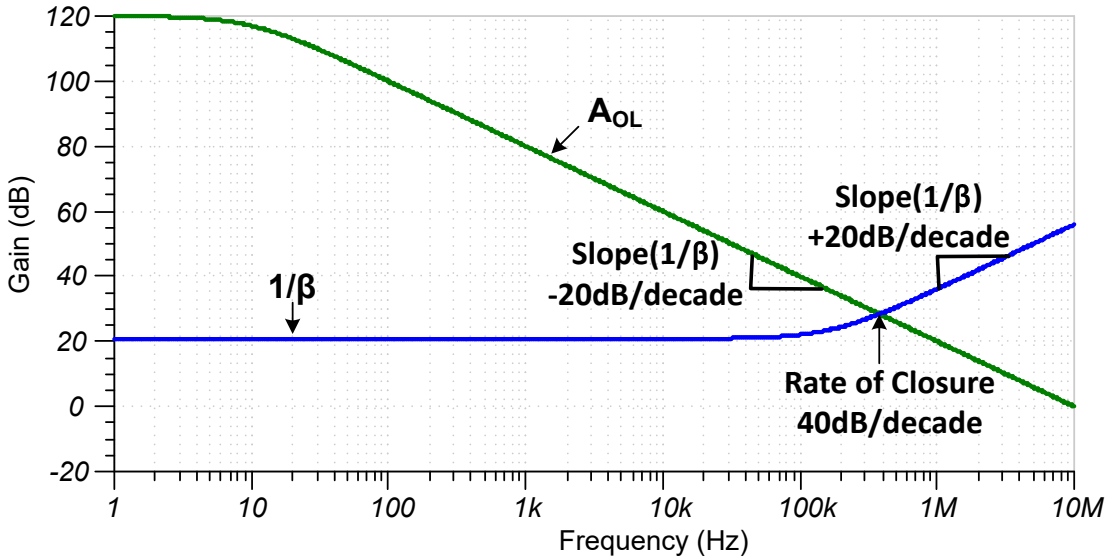


**Figure 2-11. Unstable Rate-of-Closure Example (ROC = 40dB/decade)**

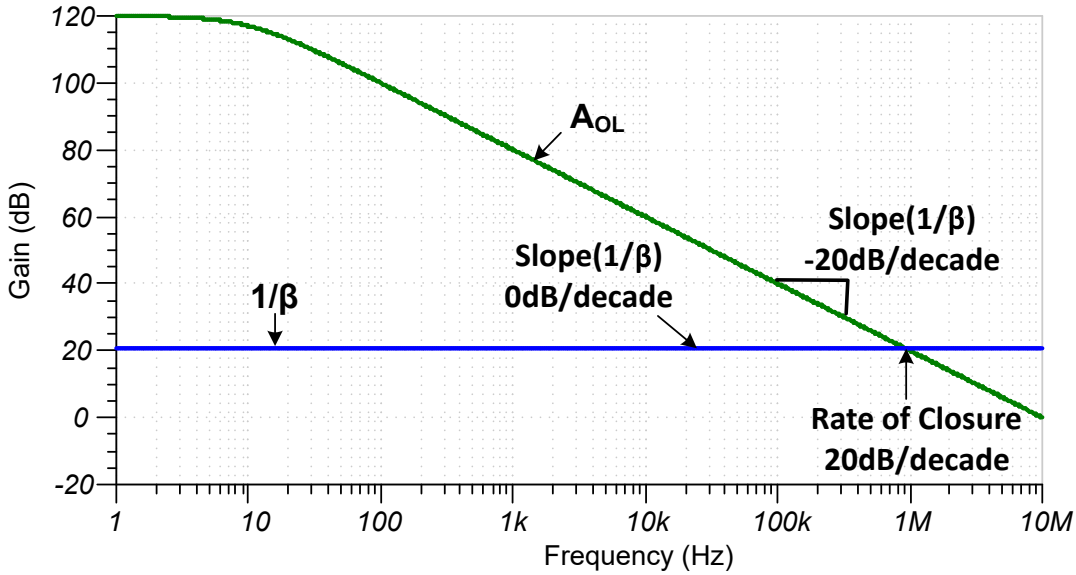


**Figure 2-12. Stable Rate-of-Closure Example (ROC = 20dB/decade)**

## 2.6 Indirect (Non-Invasive) Stability Tests

Determining the phase margin with an open-loop test is considered a direct stability test because the loop-gain phase shift is directly measured or simulated. This test is generally the preferred method for confirming stability and the results are more reliable. However, an open-loop test can be impractical in a closed-loop system because the ability to *Break-the-loop* to test the open-loop results is limited. Stability can also be checked by looking at the percentage overshoot in a small-signal step on an op amp (see Figure 2-13). There is a direct relationship between the percentage overshoot and the phase margins for second-order systems. Remember, a first-order system contains a single pole and a second-order system has two poles. In a passive system, a

first-order system is an RC network, and a second-order system uses an RLC network. In the case of an op amp circuit, the closed-loop output impedance acts like an inductor and the op amp load is a capacitor. The response for circuits with op amp stability issues can usually be approximated fairly well by assuming the system is a second-order system, even though the order can be higher. The graph shown in Figure 2-14 can be used to find the phase margin based on percentage overshoot, and this graph assumes the system is a second-order system.

AC gain peaking can also be used as an indirect method to find phase margin (see Figure 2-15). Again, this method assumes that the system is a second-order system. The graph shown in Figure 2-14 can be used to find the phase margin based on the percentage overshoot, and this graph assumes the system is a second-order system. The graph in Figure 2-16 can be used to find phase margin based on the percentage overshoot (PO). Alternatively, Analog Engineer's Calculator is a software tool that allows engineers to enter values for overshoot and AC peaking to determine the phase margin.

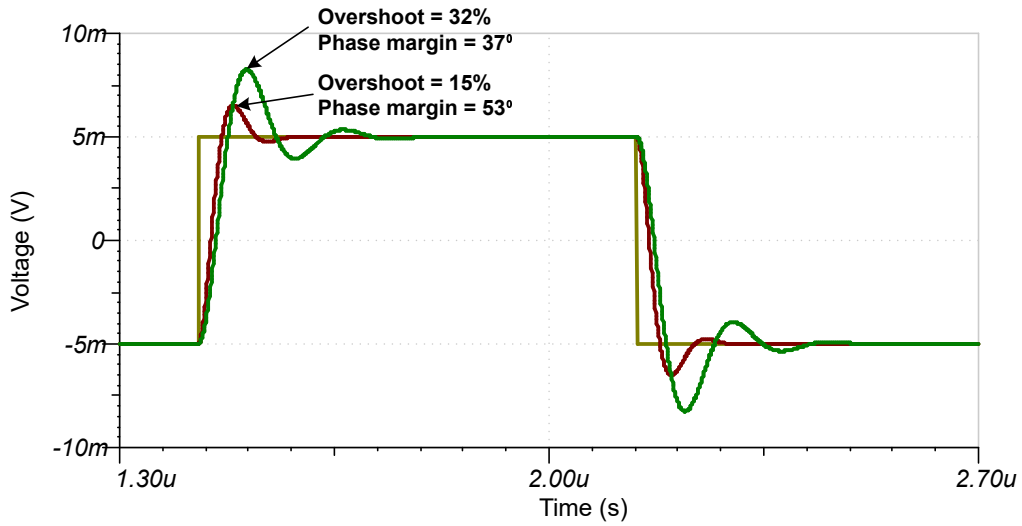


**Figure 2-13. Percentage Overshoot is a Measurement of Stability**

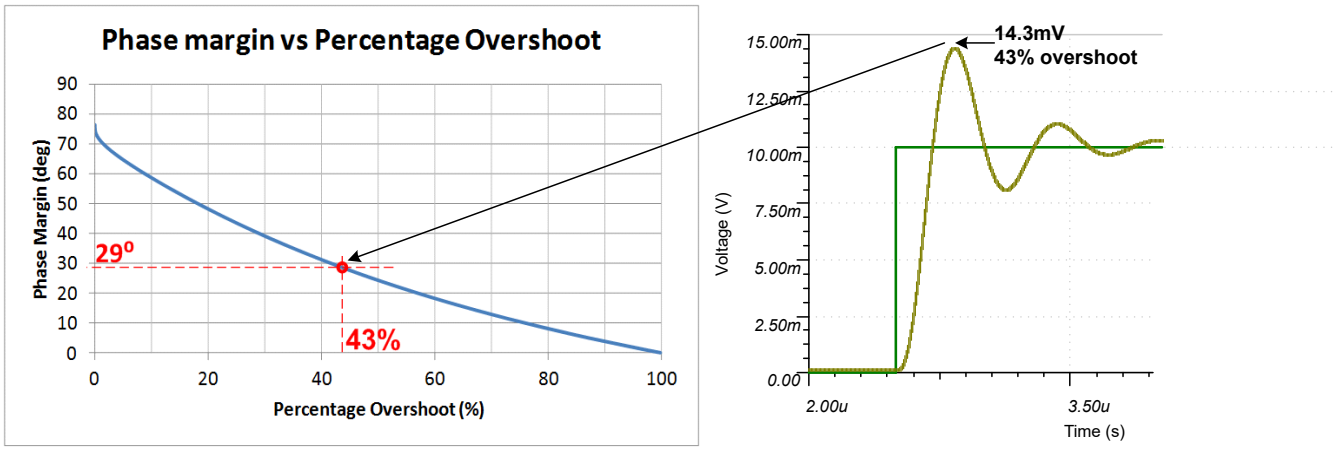


**Figure 2-14. Finding the Phase Margin Based on the Percentage Overshoot**

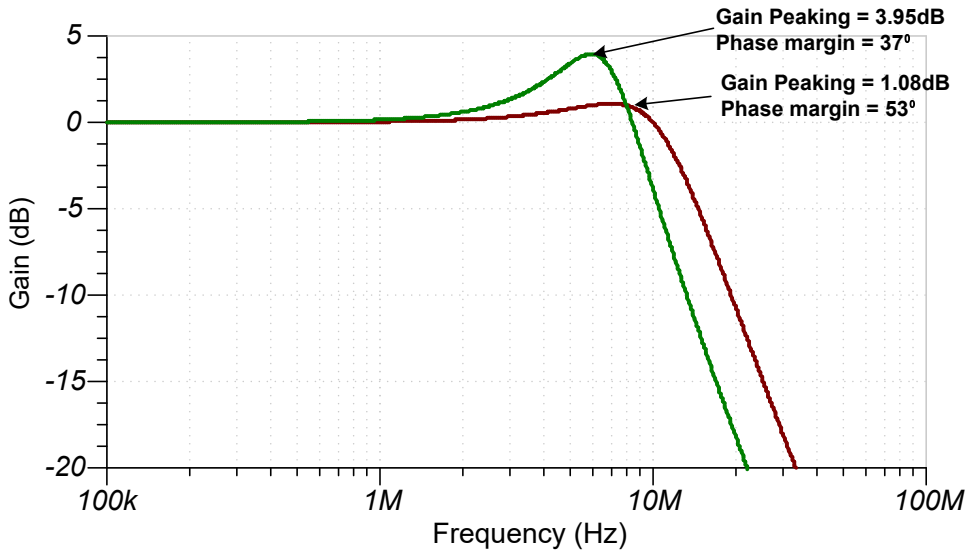


**Figure 2-15. AC Gain Peaking is a Measurement of Stability**

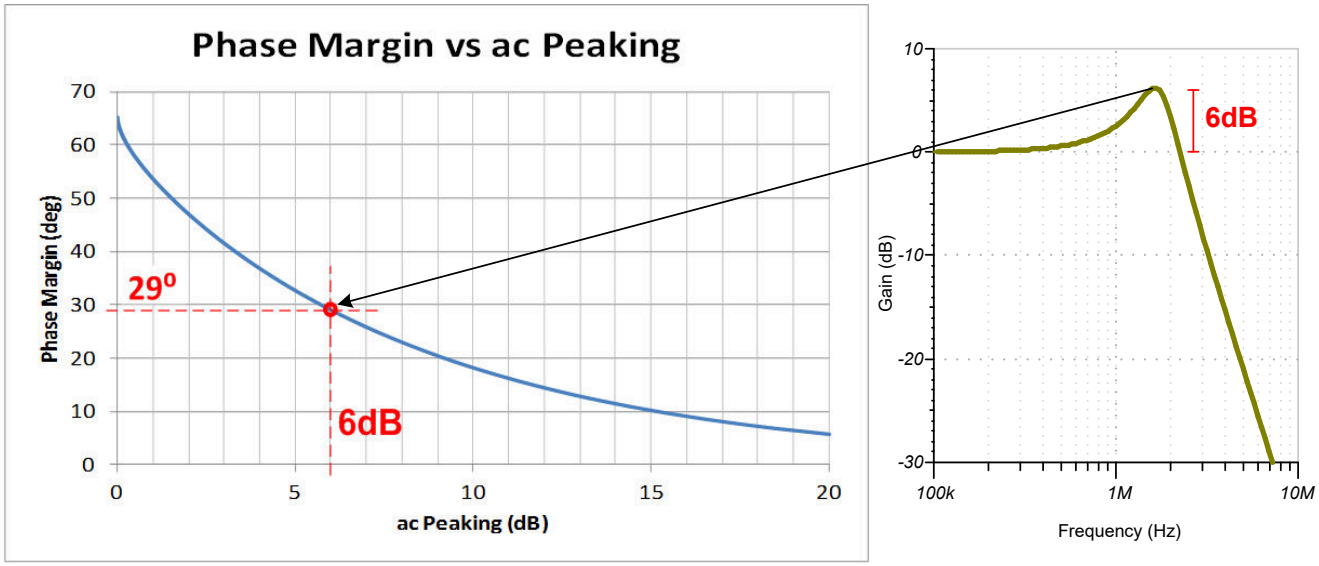


**Figure 2-16. Finding the Phase Margin Based on AC Peaking in Decibels**

## 3 Simulating Open-Loop Stability Tests

As discussed in Section 2.3, op amp stability and the phase margin are determined by graphing the magnitude and phase of $A_{OL}$, $A_{OL} \times \beta$, and $1/\beta$. These parameters are measured or simulated in an open-loop op amp configuration. This section discusses methods to generate these curves using SPICE simulation. The examples given in this document use TINA-TI™ SPICE, but the general methods are the same regardless of the simulator.

### 3.1 Breaking the Loop the Wrong Way

Since the stability tests are for an open-loop configuration, the natural approach to running the test is to break the feedback path at the op amp output and place a test signal on the feedback network (see Figure 3-1). Unfortunately, this method does not work because the op amp input offset ($V_{OS}$) drives the output signal to the power supply rails. When the output is driven into the supply rail, the op amp is in a saturated nonlinear operating condition, so the AC transfer function is not accurate. Figure 3-2 shows the AC transfer function for the op amp in Figure 3-1. The op amp in Figure 3-1 can have a DC $A_{OL}$ of 120dB but the plot shows only 29dB. The location of the dominant pole and phase shift characteristics are also completely different than what is expected. Thus, this simple method of breaking the loop is not useful for generating the open-loop AC plots.

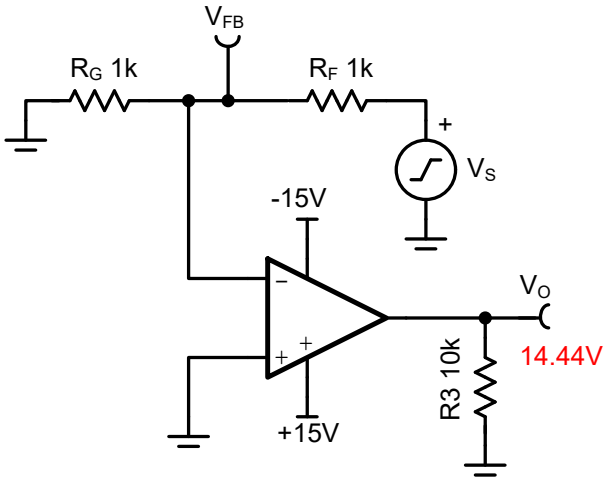


**Figure 3-1. Incorrect Way to Break the Feedback Loop (Saturated Output)**

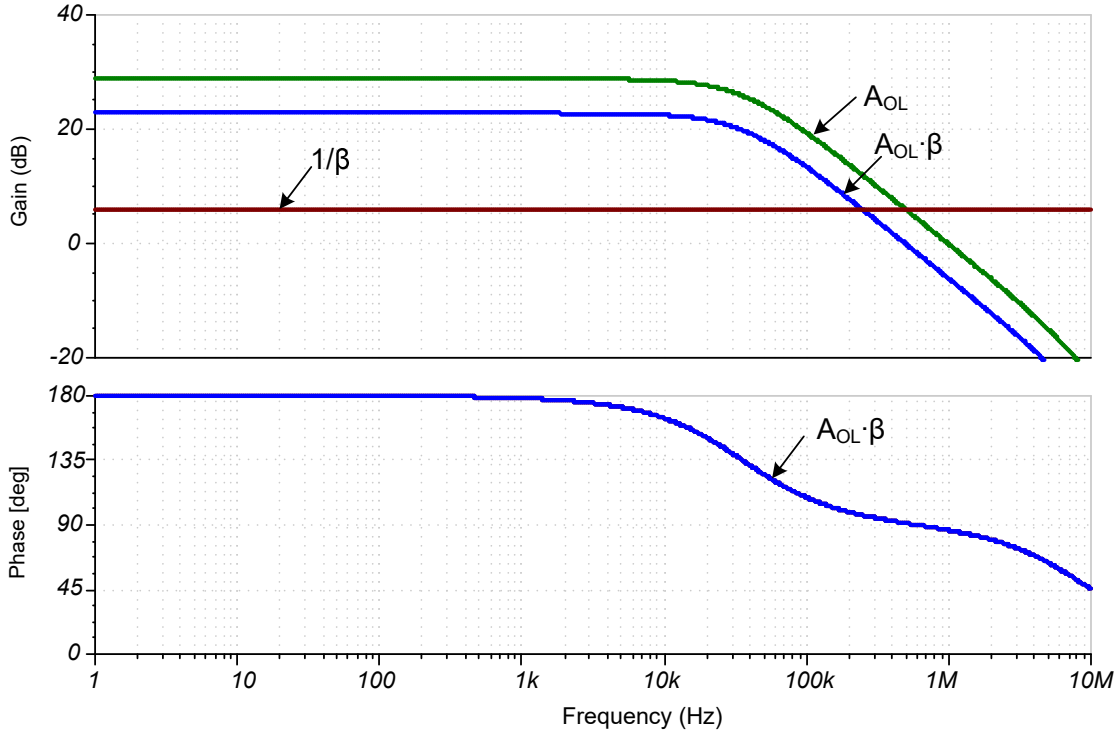


**Figure 3-2. Incorrect Open-loop Response Due to Output Saturation**

## 3.2 Breaking the Loop With LC Test Circuit

Figure 3-3 shows an open-loop stability test configuration where the feedback loop is broken with a 1TH inductor, and the signal is injected using a 1TF capacitor. The very large values for the capacitor and inductor are not practical for real-world circuit implementations, but work well for most simulation cases. The inductor acts like a short at DC, but acts like an open for AC frequencies (recall Equation 18). Conversely, the capacitor acts like an open at DC, but acts like a short for AC frequencies (recall Equation 19 ). Thus, at DC the circuit is in a closed-loop configuration, and at AC the circuit is in an open-loop configuration (see Figure 3-4 and Figure 3-5). The reason the very large values are used for the inductors and capacitors is to allow for a very low-frequency open-loop operation. For example, in many cases, the simulation is run from 0.1Hz to see the dominant pole. The large LC values allow for the circuit to operate in open-loop even at this low frequency.

$$X_L = 2 \times \pi \times f \times L \tag{18}$$

$$X_C = 1/(2 \times \pi \times f \times C) \quad (19)$$

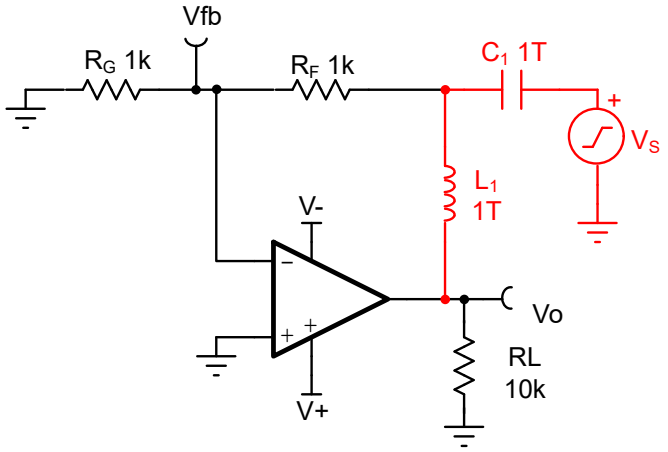


**Figure 3-3. Open-Loop Test Configuration for Stability Verification**

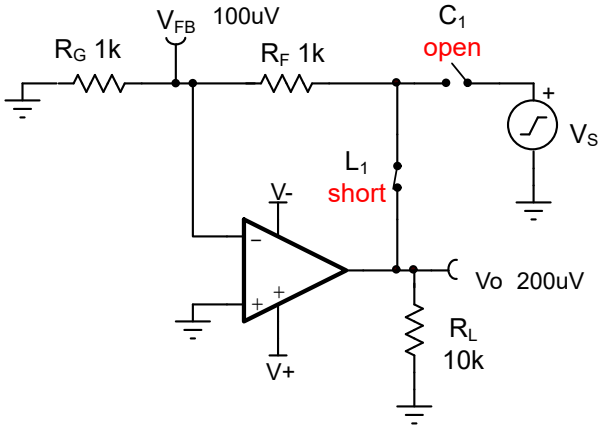


**Figure 3-4. Open-loop Test Configuration for Stability Verification at DC**

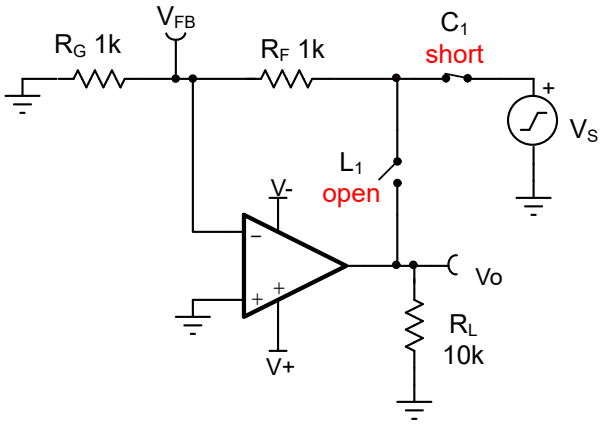


**Figure 3-5. Open-Loop Test Configuration for Stability Verification for AC Frequencies**

Running an AC transfer characteristic for the test circuit in Figure 3-3, generates the graph shown in Figure 3-6. In TINA™SPICE you can identify the curves with the question mark button (see Figure 3-6). For stability analysis $A_{OL}$, $A_{OL}$ × β, and 1/β magnitude curves are needed, and the $A_{OL}$ × β phase curve is needed. Deleting the unnecessary curves helps improve the readability of the graph. Also, adjusting the y-axis scaling to show magnitude in 20dB increments, and phase in 45° increments, can make interpreting the results easier. The last step is to add a legend to show the phase-margin. In TINA™ SPICE this can be done by placing a cursor on

$A_{OL}$ × β and finding the frequency where $A_{OL}$ × β = 0dB. Once the cursor is in position, pressing the legend tool generates a legend on the graph that shows the gain and phase for all pertinent curves at the cursor frequency. In Figure 3-7 the legend indicates a phase margin of 65.7°.

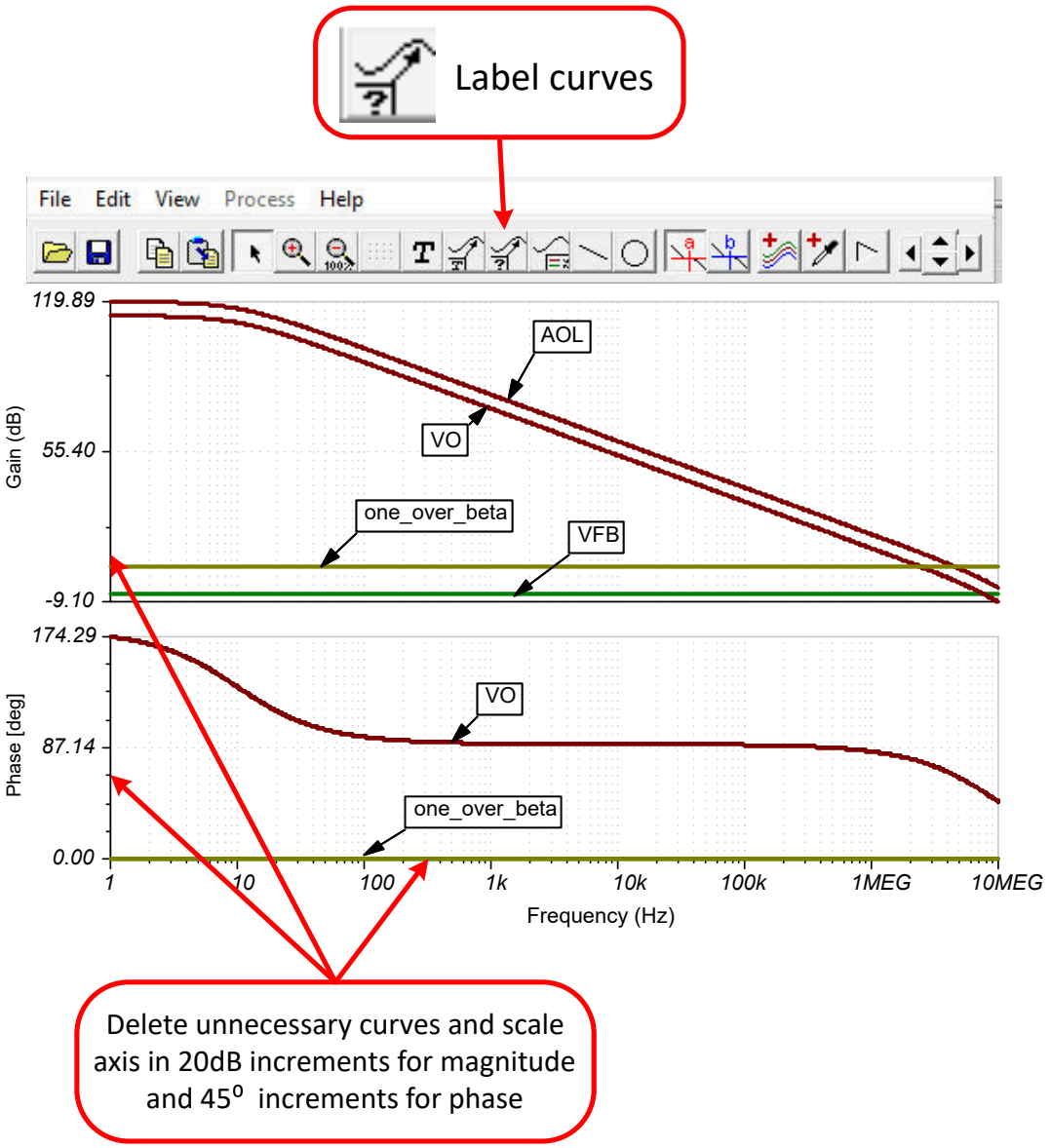


**Figure 3-6. Delete Unnecessary Curves and Adjust Scale**

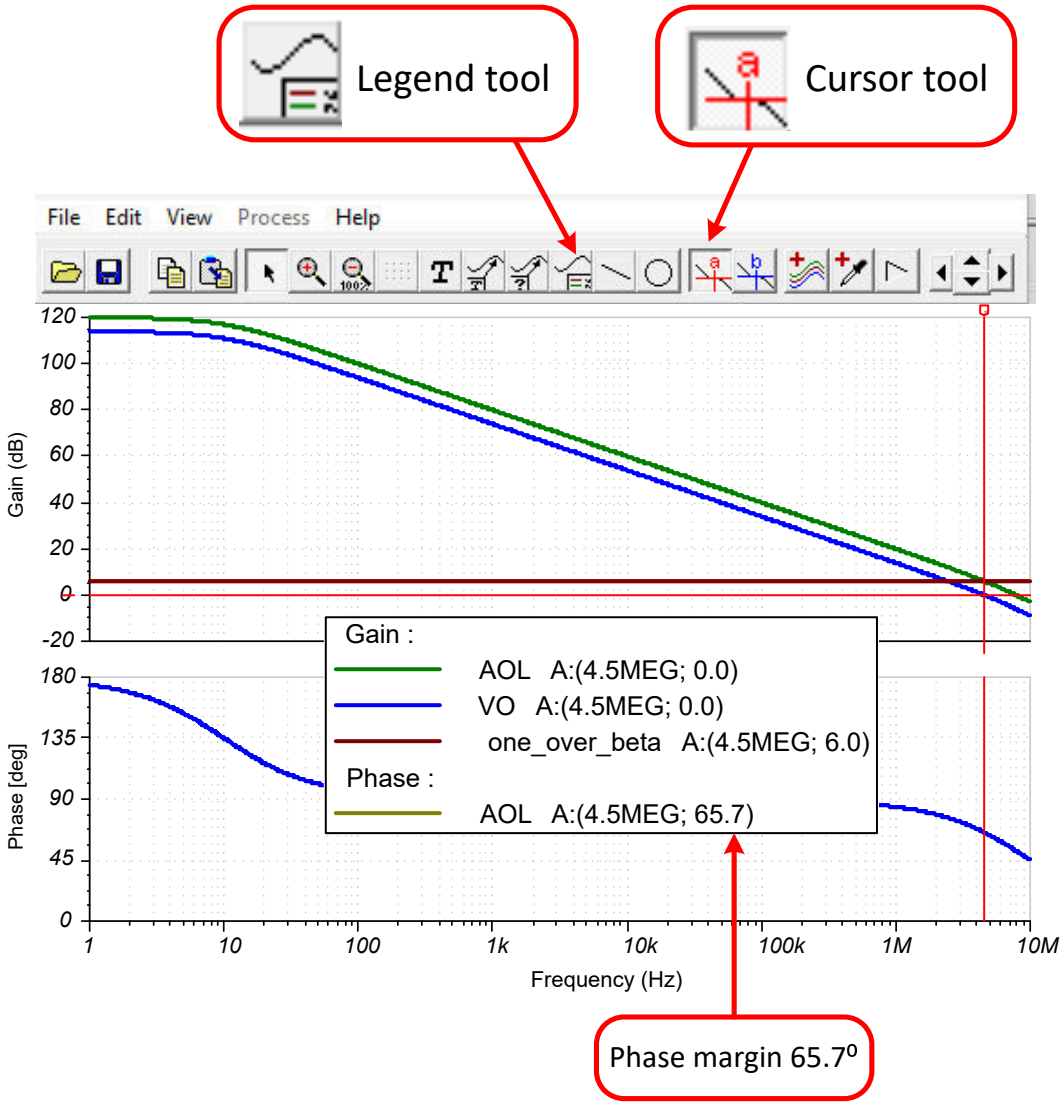


**Figure 3-7. Display Phase Margin With Legend**

## 3.3 Differential Loop Break Test

A method for breaking the feedback loop at the output of the amplifier is covered in Section 3.2. One problem with this approach is that the approach isolates the op amp output impedance from the feedback network. In some cases, using the output loop break method can mask stability issues because of the output impedance isolation from the feedback network.

The circuit in Figure 3-8 eliminates the limitations of Figure 3-3 by breaking the feedback loop at the input. However, this method isolates the input capacitance of the op amp from the feedback network. To solve this problem, a capacitor is connected to the feedback loop opposite of the test inductor (see $C_{IN}$ in Figure 3-8). The value for $C_{IN}$ includes the common mode capacitance from the op amp datasheet and any parasitic PCB capacitance ($C_{IN} = C_{CM} + C_{PCB}$). The op amp parasitic capacitance is normally found in the op amp datasheet table under the *Input Impedance* section (see Table 3-1).

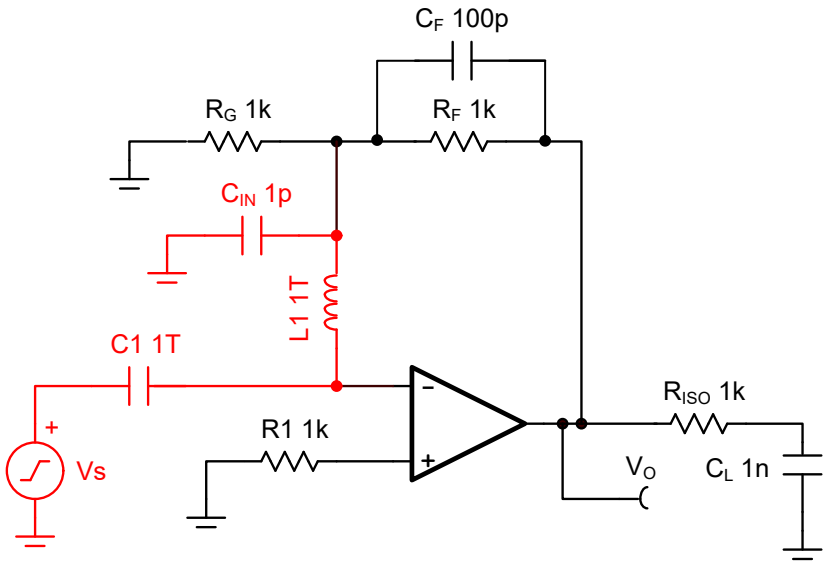


**Figure 3-8. Breaking the Feedback Loop at the Input**

The circuit in Figure 3-8 works well for single-ended configurations, but can have accuracy issues for differential circuits, such as Figure 3-9. The accuracy issues stem from the fact that the inverting and non-inverting paths are cross connected, where both receive feedback from the output. Thus, a circuit that differentially breaks the feedback paths is required. Figure 3-11 shows the development of the differential loop-break circuit. In this circuit, two inductors (L1 and L2) are used to break the feedback paths. The test signal and associated coupling capacitor connect directly to the op amp inputs. The test inductors isolate the input capacitance from the feedback network, so the entire input impedance network is duplicated and connected to the feedback ($R_{ID}$, $C_{ID}$, $C_{CM1}$, $C_{CM2}$). The loop gain is measured directly between the feedback paths, and loaded $A_{OL}$ is measured directly at the output ($A_{OL\_LD}$). The term *loaded $A_{OL}$* is used to explain that the shape of the $A_{OL}$ curve is different than what is published in the datasheet because of load capacitance and the feedback network. Finally, any input voltage signal sources must be shorted and any current signal sources must be opened.

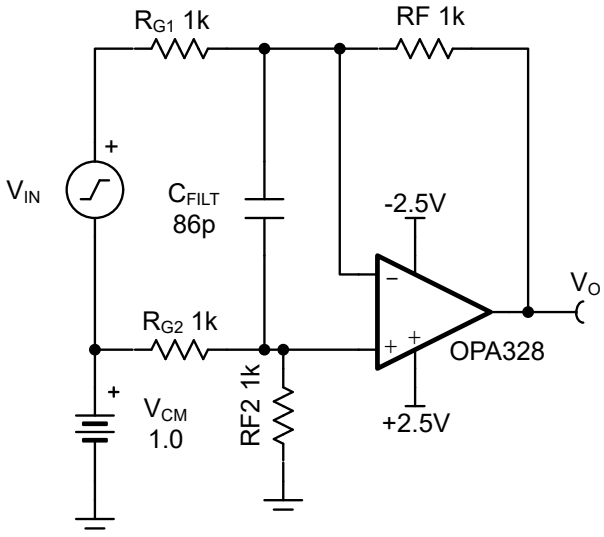


**Figure 3-9. Example Differential Circuit With Stability Issues**

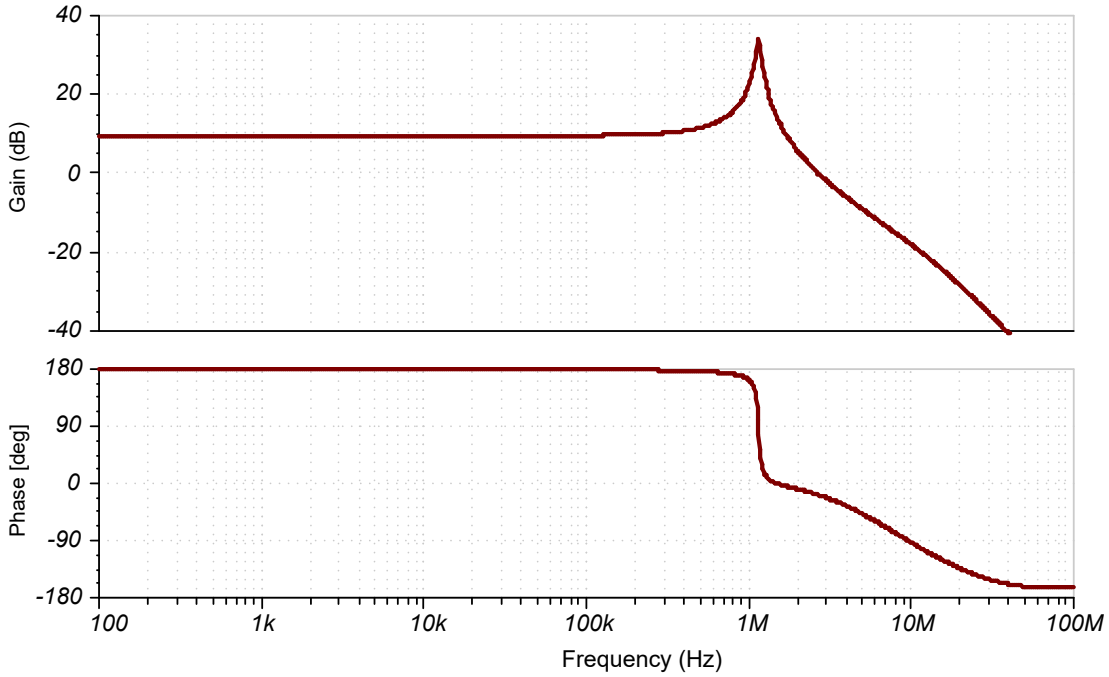


**Figure 3-10. Example Differential Circuit Closed-Loop AC Response**

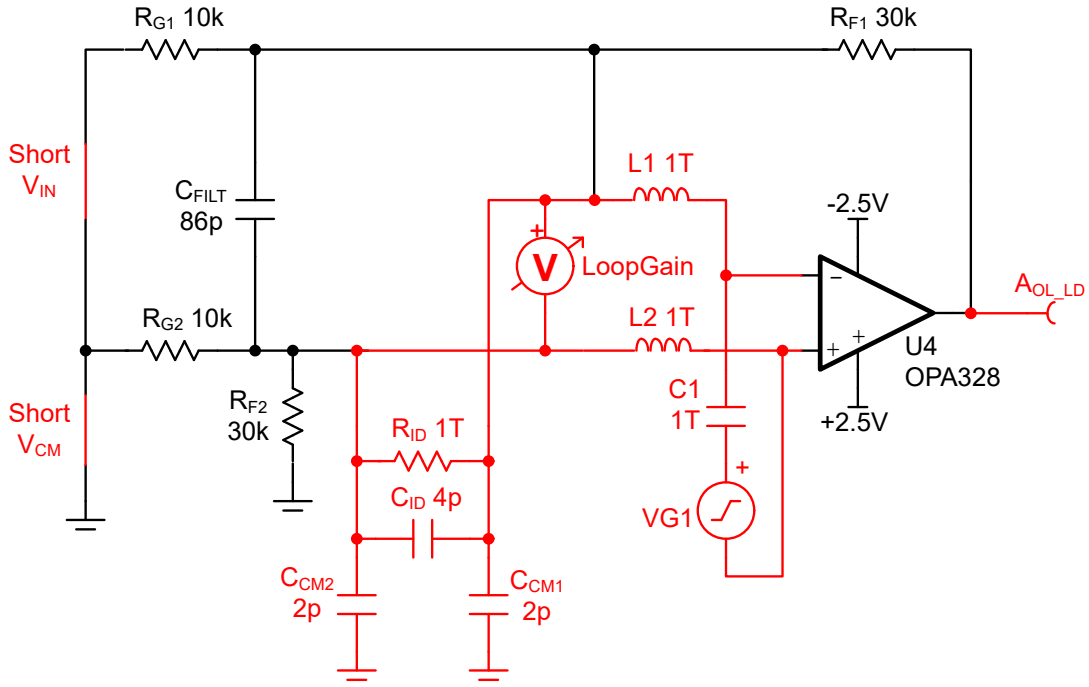


**Figure 3-11. Differential Loop Break Test**

**Table 3-1. Input Impedance From OPA328 Datasheet**

| Parameter | | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|
| $Z_{ID}$ | Differential | | 1 \|\| 4 | | TΩ \|\| pF |
| $Z_{ICM}$ | Common-mode | | 1 \|\| 2 | | TΩ \|\| pF |

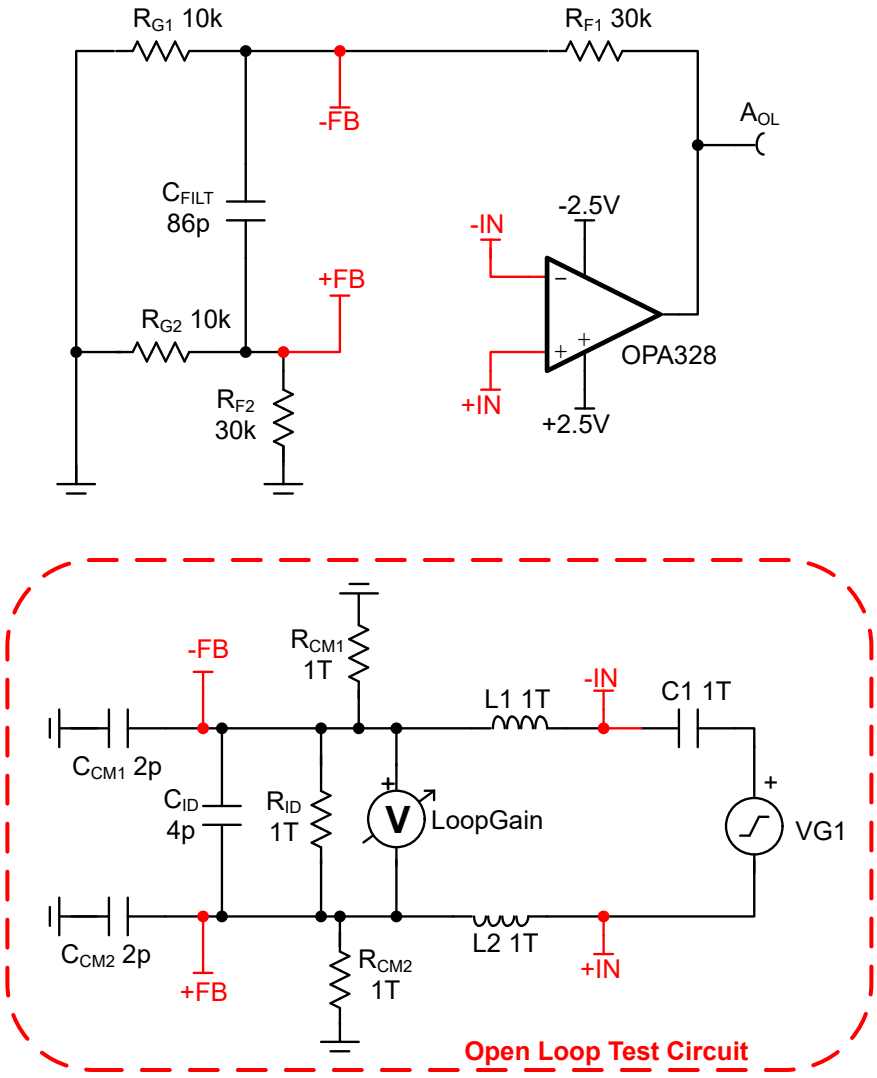


**Figure 3-12. Simplified Differential Loop Break Test**

The test circuit connections in Figure 3-11 are messy and difficult to manage. For this reason, a better approach is to copy the open-loop test circuit shown in Figure 3-12. This circuit has two input connection test points (-IN and +IN), and two feedback connection test points (-FB and +FB). The test points, labeled in red, connect the test circuit to the op amp circuit. The open-loop test circuit can be reused in any op amp stability test. The only change required is to adjust the values of $C_{CM}$, $C_{ID}$, $R_{ID}$, and $R_{CM}$ to reflect the op amp datasheet. In Figure 3-12, the input impedance values are updated according to the datasheet (Table 3-1). The connections between the feedback network and the op amp inputs are broken and connected to the test points (shown in red on Figure 3-12).

Figure 3-13 shows the AC transfer function for the circuit in Figure 3-12. For the differential loop break approach, the $A_{OL\_LD}$ curve and the loop gain curve are generated automatically. Technically, only the loop gain curve is required to measure phase margin. However, the post processor can be used to generate the 1/β curve by dividing $A_{OL}$ by loop gain ($1/\beta = A_{OL} / (A_{OL} \times \beta)$).

Often, when engineers are first exposed to the differential loop break method, the method seems complex and to require significant extra work. However, when implementing the test by reusing the test circuit, the method only takes a few minutes to implement the differential loop break test. Furthermore, the improved accuracy of this method, makes the method a requirement in many cases. In general, TI recommends using the differential loop break test in all cases because the test is easy to implement, and is the most accurate loop break method.

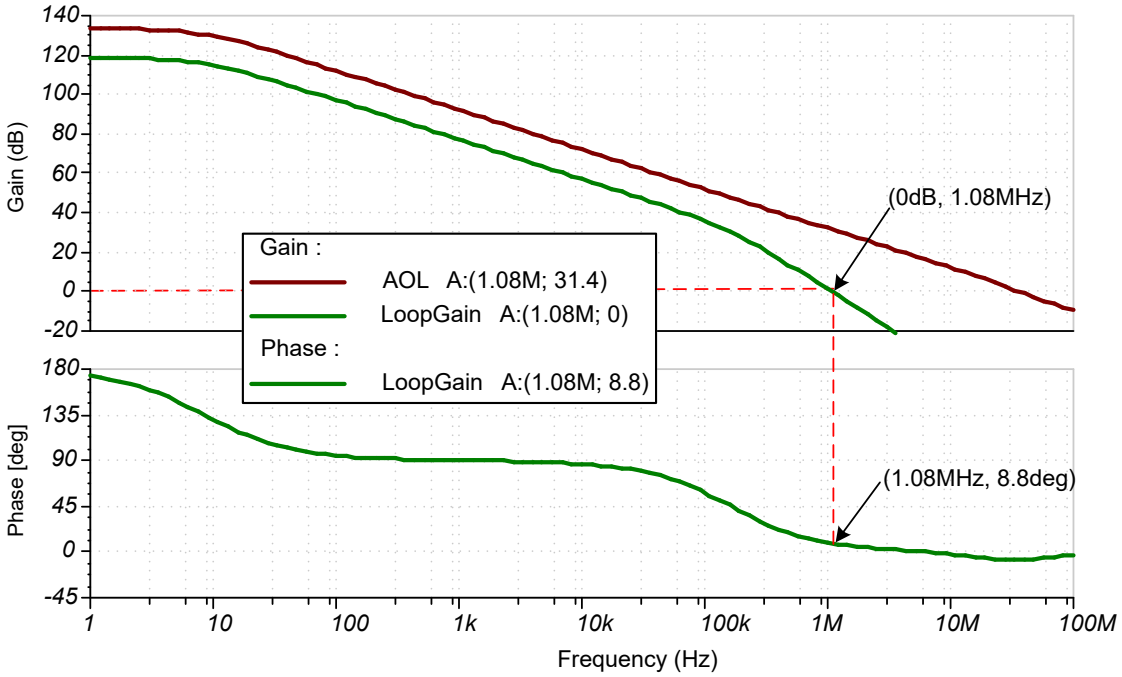


**Figure 3-13. Open-Loop AC Response for Simplified Differential Loop Break Test**

## 4 Stability Correction for Capacitive Load

This section describes in detail why a capacitive load causes instability and provides correction options for this problem. Specifically, the section examines how adding a capacitive load changes the shape of the open-loop gain curve by adding an additional pole. The stability problem is resolved by adding a zero to the open-loop gain response to cancel the effects of the pole.

## 4.1 Isolation Resistor ($R_{ISO}$) Method

Figure 4-1 illustrates a circuit with capacitive load that is unstable (PM = 22.5°). Inspecting the open-loop graph shows that the reason for the instability is a second pole in the $A_{OL}$ curve. The second pole sets the rate of closure to 40dB/dec. The capacitive load added the secondary pole. This example circuit shows how an isolation resistor can stabilize the circuit. First, clarify why the capacitive load adds the additional pole in $A_{OL}$.

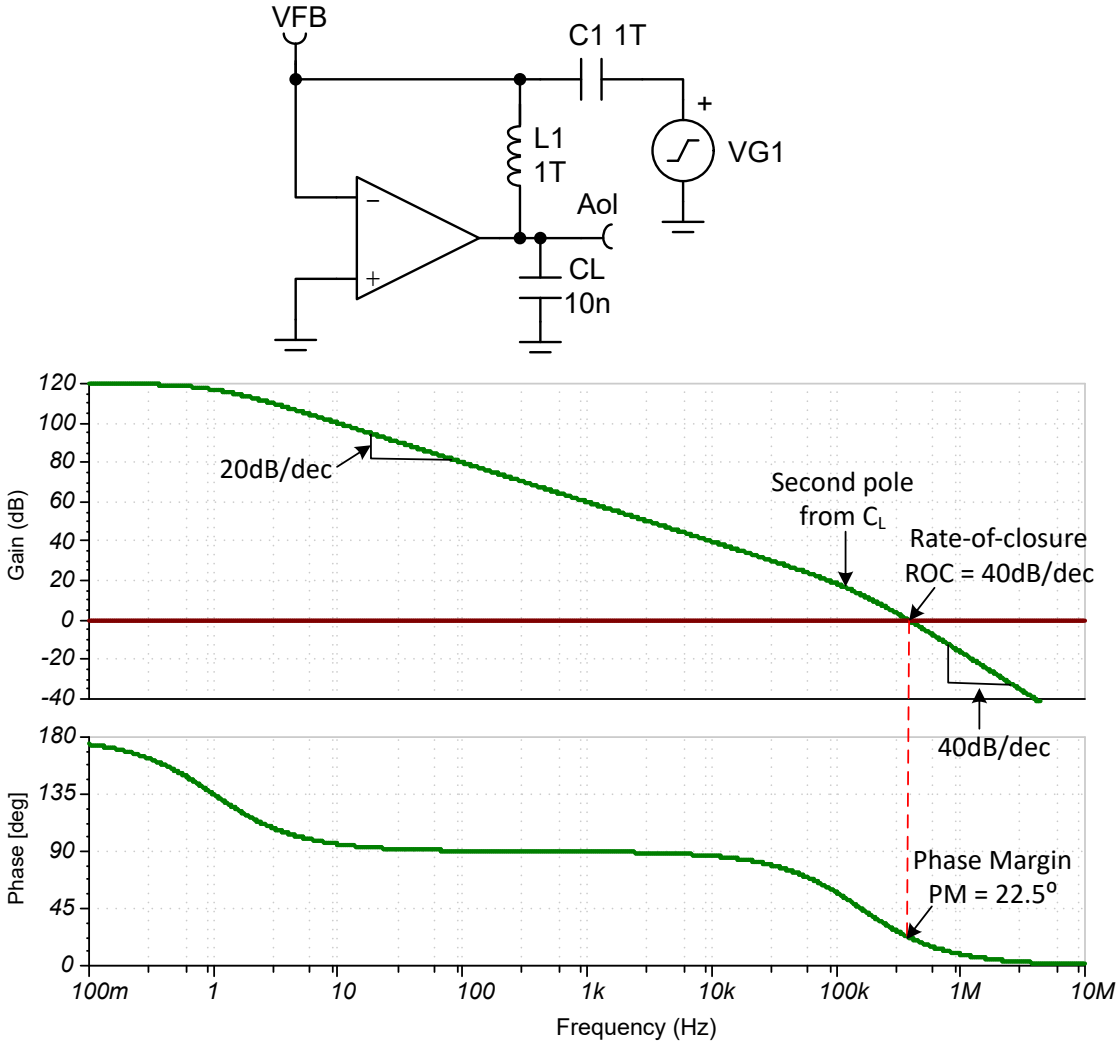


**Figure 4-1. Capacitive Load Creates Instability With Secondary Pole**

Figure 4-2 shows how the op amp open-loop test circuit can be simplified into an RC low pass filter. The top of the figure illustrates the standard open-loop circuit with the loop broken at the output. The output-break circuit is used to simplify the discussion, as the other circuits look more complex. The center figure substitutes the op amp with the op amp model from Figure 2-3. The center figure also simplifies the drawing by shorting the test capacitor and opening the inductor. In the bottom image, the input signal source is combined with the AC $A_{OL}$ model ($A_{OL} \times V_{IN}$). The bottom figure shows that the output impedance and load capacitance form a low pass filter ($R_O \times C_L$). This low pass filter is what adds the secondary pole that causes the instability seen in Figure 4-1.

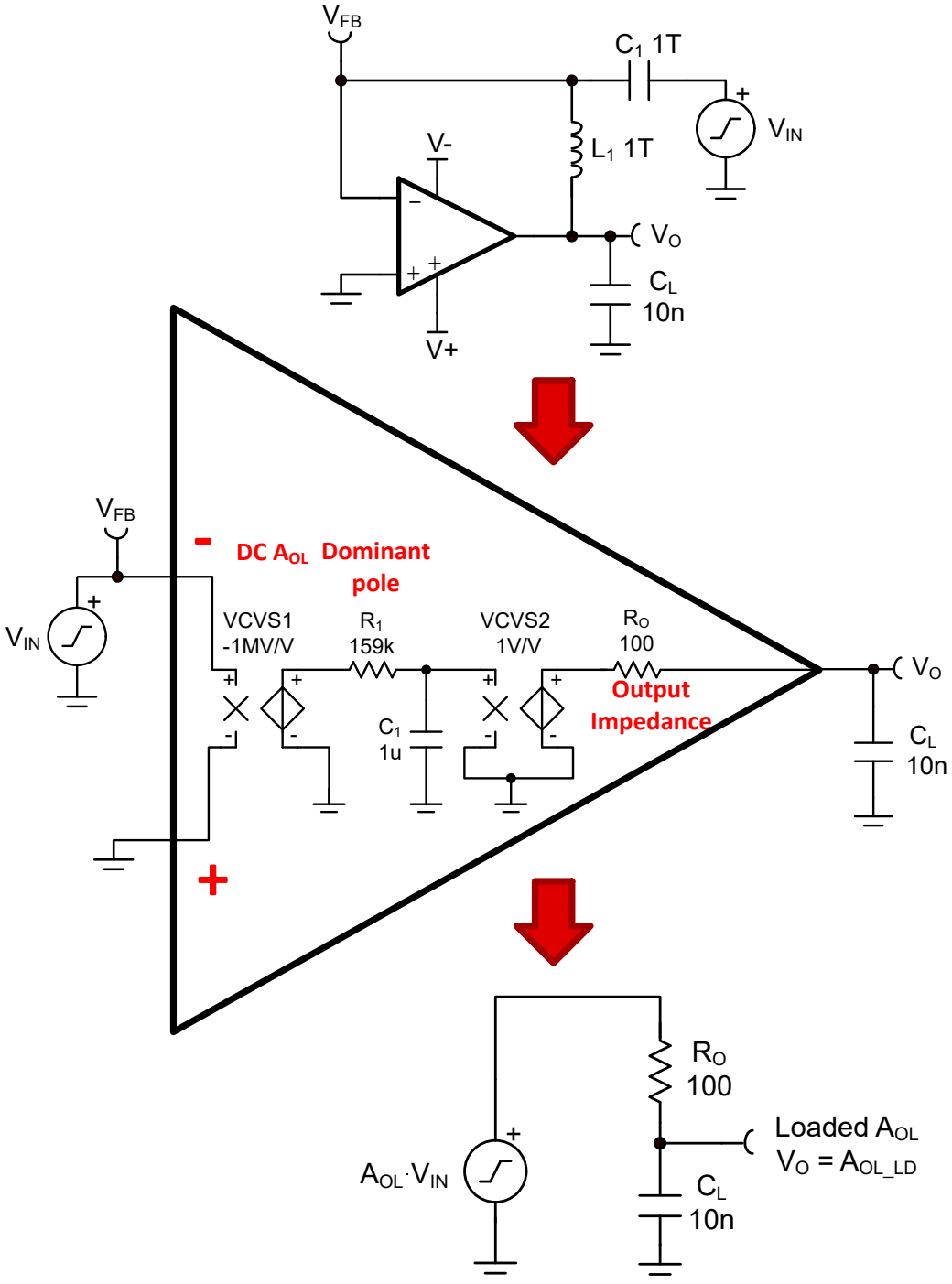


**Figure 4-2. Open-Loop Test Circuit Simplified Into Low-pass Filter**

Figure 4-3 shows how the low-pass filter is applied to the $A_{OL}$ curve of the datasheet to create the loaded $A_{OL}$ curve ($A_{OL\_LD}$). The $A_{OL}$ curve at the top of the graph has a single dominant pole (1Hz) which introduces a total phase shift of 90°. The low pass filter introduces a second pole (158kHz) and additional 90° of phase shift. Since the $A_{OL} \times V_{IN}$ and low pass filter are cascaded, the two transfer functions are multiplied. However, the multiplication of linear factors converts to addition because the curves are in decibels. Thus, engineers can directly add the top two curves to generate the loaded $A_{OL}$. The key point here is that the capacitive load and op amp open-loop output impedance add an additional pole in the loaded $A_{OL}$.

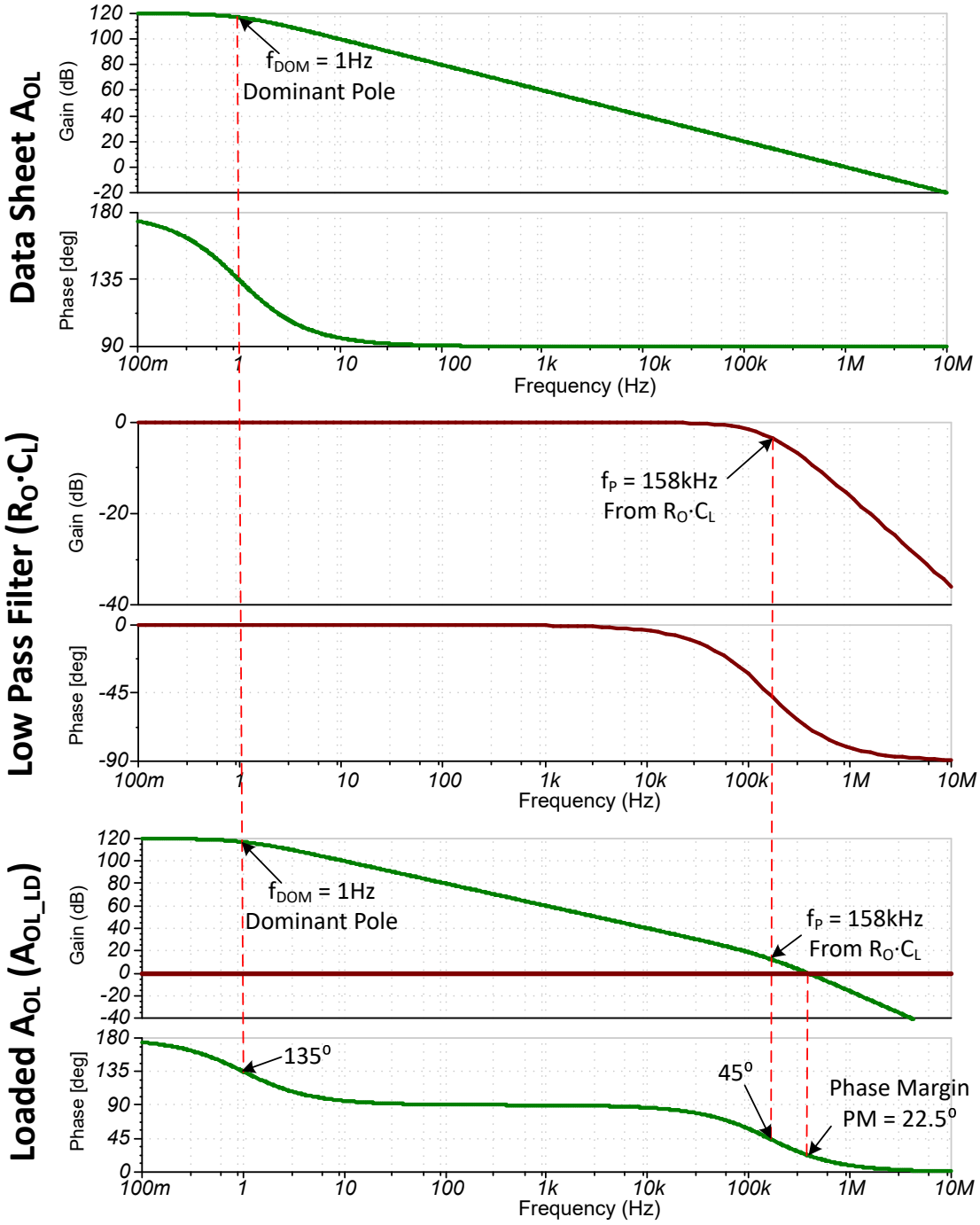


**Figure 4-3. $A_{OL}$ Loaded by Low-Pass Filter ($R_O \times C_L$)**

A correction option to the instability caused by the secondary pole in the loaded $A_{OL}$ is to add an isolation resistor between the op amp and $C_L$ (see Figure 4-4). The isolation resistance creates a zero that cancels the secondary pole. Figure 4-4 shows the open-loop response for the same amplifier used in Figure 4-1 with an isolation resistor. Inspecting the $A_{OL}$ curve shows that the pole and zero are located very close together so the items effectively cancel out. Closely inspecting the region between $f_P$ and $f_Z$ shows a slight change in slope and a small dip in phase. If the pole and zero are further separated, the slope change and phase dip are more obvious. The key point here is that the phase margin for the uncompensated amplifier is 22° (see Figure 4-1), and for the compensated amplifier is 87° (see Figure 4-4).

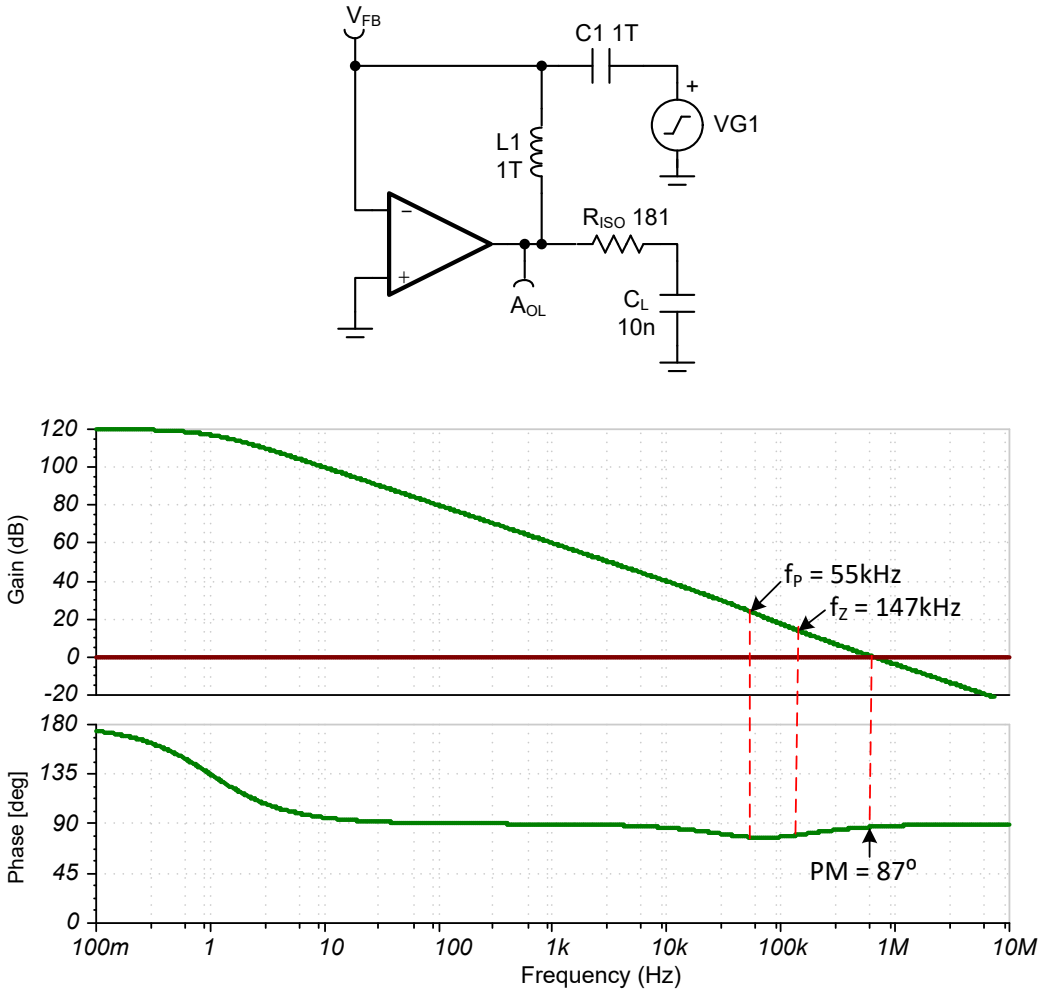


**Figure 4-4. $R_{ISO}$ Compensation Cancels Second Pole With Zero**

Figure 4-5 shows how the op amp open-loop test circuit can be simplified into an RC network for the $R_{ISO}$ case. The top of the figure illustrates the standard open-loop circuit with the loop broken at the output. The center figure substitutes the op amp with the op amp model from Figure 2-3. The center figure also simplifies the drawing by shorting the test capacitor and opening the inductor. In the bottom image the input signal source is combined with the AC $A_{OL}$ model ($A_{OL} \times V_{IN}$). The bottom figure shows that the output impedance and load capacitance form RC voltage divider network. This network contains a pole and a zero.

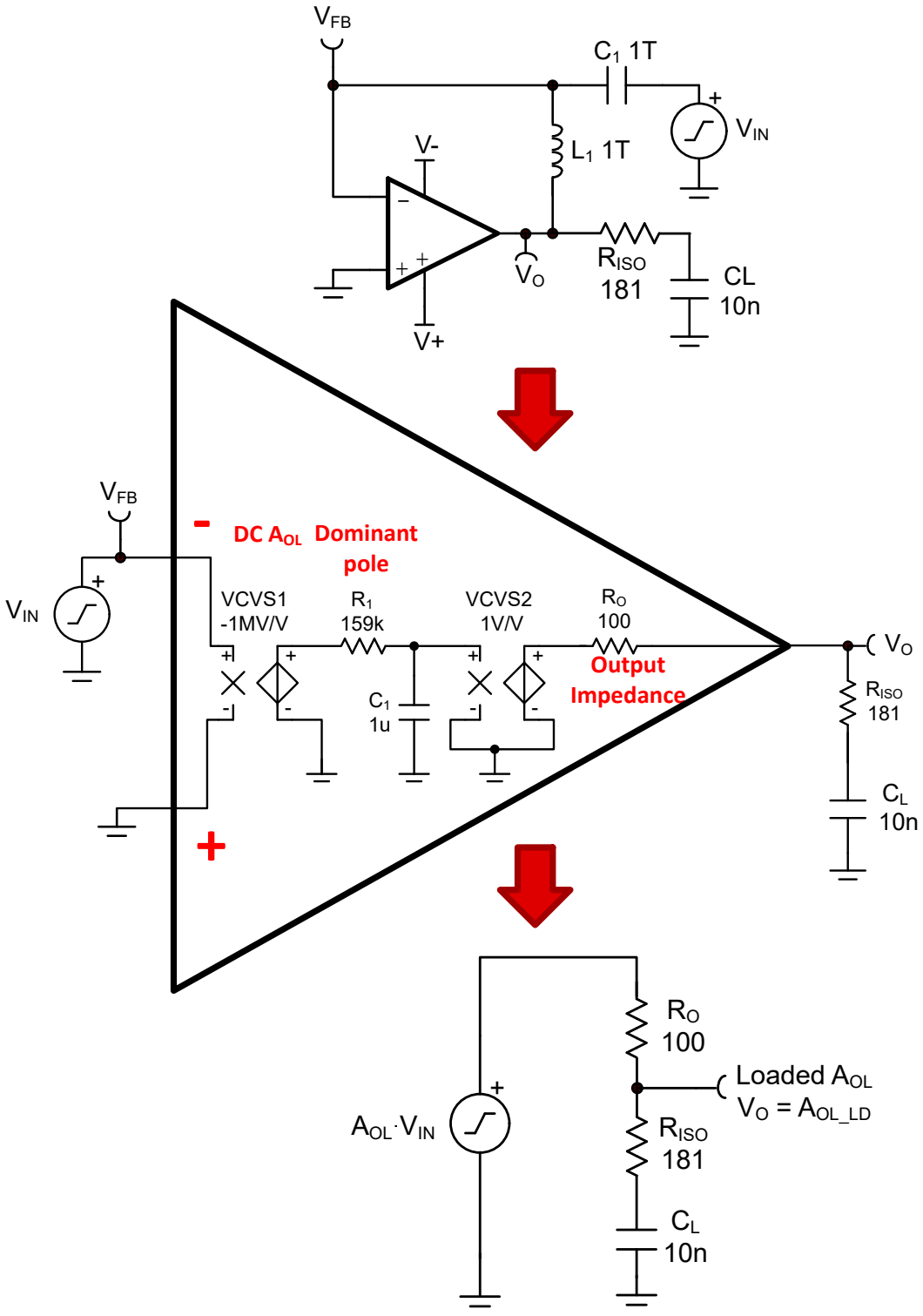


**Figure 4-5. Open-Loop Test Circuit Simplified Into Simple RC Filter With Pole and Zero**

The transfer function for the circuit shown in Figure 4-6 can be derived by thinking of the circuit as a voltage divider (see Equation 22). The equation for a resistive voltage divider is well know by most electrical engineers, but adding a capacitor can be confusing for engineers not familiar with reactive circuits. The problem is actually fairly easy to solve if engineers remember that the impedance of a capacitor is represented by $X_C = 1/(s \times C_L)$, where $s = j \times \omega$, and see Equation 20. Thus, the total impedance of $Z_2$ is $R_{ISO} + 1/(s \times C_L)$. Substituting $Z_2$ into Equation 22 produces Equation 23. Applying algebra to Equation 23 produces Equation 24. To find the equations for the pole frequency of Equation 24 solve for the root of the denominator (find s for, see Equation 21 ). The pole frequency is the negative of the root ($\omega_P$ = –Root, or $f_P$ = –Root/(2π) ). The same procedure is applied to the numerator to find the zeros. The frequency equation for the poles and zeros are given in Equation 25 and Equation 26. Algebra is applied to Equation 25 to solve for $R_{ISO}$ (see Equation 27), and this equation is used in $R_{ISO}$ conservative design method.

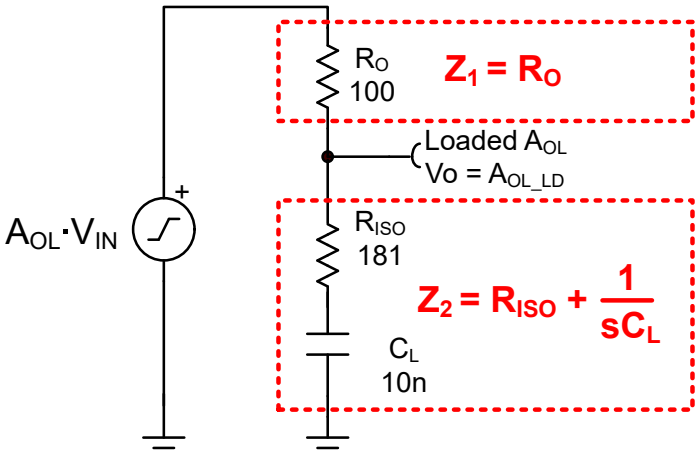


**Figure 4-6. RC Network Forms a Voltage Divider**

$$j = \sqrt{-1} \tag{20}$$

$$1 + s \times (R_{ISO} + R_O) \times C_L = 0 \tag{21}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2}{R_1 + R_2} \tag{22}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{Z_2}{Z_1 + Z_2} = \frac{R_{ISO} + \frac{1}{s \times C_L}}{\left(R_{ISO} + \frac{1}{s \times C_L}\right) + R_O} \tag{23}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{1 + s \times R_{ISO} C_L}{1 + s \times (R_{ISO} + R_O) \times C_L} \tag{24}$$

$$f_Z = \frac{1}{2 \times \pi \times R_{ISO} \times C_L} \tag{25}$$

$$f_P = \frac{1}{2 \times \pi \times (R_O + R_{ISO}) \times C_L} \tag{26}$$

Figure 4-7 is a graphical example of how the $A_{OL}$ curve from the op amp datasheet is loaded by the RC network shown in Figure 4-6. Note that this network adds both a pole and zero into the loaded $A_{OL}$ transfer function. Technically, the $A_{OL}$ curve is multiplied by the pole-zero transfer function, but doing multiplication translates to addition in decibels since the curves are logarithmic. Examining the pole-zero filter in Figure 4-7 shows that the pole and zero locations are very close to each other and practically cancel. The gain of the pole-zero filter only drops by about 4dB and the phase dips briefly by about 11°. The resultant loaded $A_{OL}$ has a small drop in gain and dip in phase corresponding to the filter response. However, relative to the scale of $A_{OL}$, the pole-zero filter impact on loaded $A_{OL}$ is very small and almost imperceptible. The phase margin after using the zero to cancel the pole is approximately 87°.

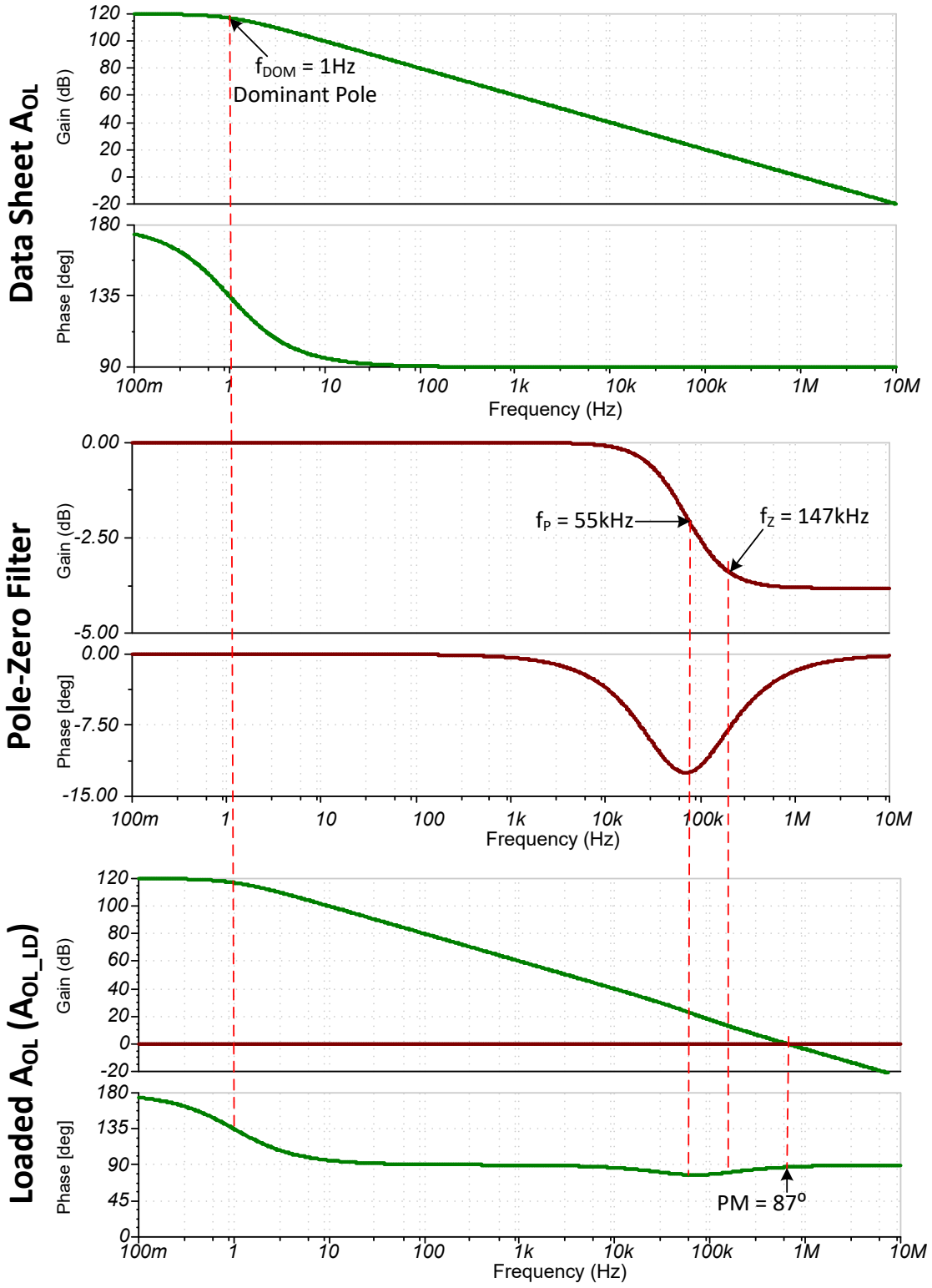


**Figure 4-7. $A_{OL}$ Loaded by Pole-Zero Filter**

The $R_{ISO}$ conservative design method shows a method for choosing $R_{ISO}$ that is stable with significant process variation. The conservative approach designs a circuit that has a higher phase margin than $R_{ISO}$ design method for minimum $R_{ISO}$. This approach is also more tolerant to process, temperature, and component variation. Unfortunately, this approach also requires a larger value for $R_{ISO}$. Larger $R_{ISO}$ leads to a lower bandwidth and a larger voltage drop across $R_{ISO}$ for circuits that drive a load.

**Note**

**$R_{ISO}$ conservative design method:**

1. Set the zero in loaded $A_{OL}$ to a gain 20dB above the intersection of $A_{OL}$ and 1/β. This is done in SPICE by positioning a cursor on $A_{OL\_LD}$ and determining the frequency 20dB above the intersection of $A_{OL}$ and 1/β. See Figure 4-8 for the $f_Z$ position in this example.
2. Use the frequency from step 1 with Equation 27 to find $R_{ISO}$.
3. This method sets the zero one decade before $A_{OL}$ intersects 1/β. This mostly cancels the effects of the pole, so the phase margin is approximately 90° for an op amp with a single dominant pole. Most op amps have additional poles and zeros near the unity gain bandwidth, so the phase margin is also impacted by the secondary poles.
4. This method results in a larger value for $R_{ISO}$ than $R_{ISO}$ design method for minimum $R_{ISO}$. Larger $R_{ISO}$ reduces the bandwidth and introduces a larger voltage drop when sourcing or sinking current to a load ($I_L$).

$$R_{iso} = \frac{1}{2 \times \pi \times f_{ZERO} \times C_{LOAD}} \quad (27)$$

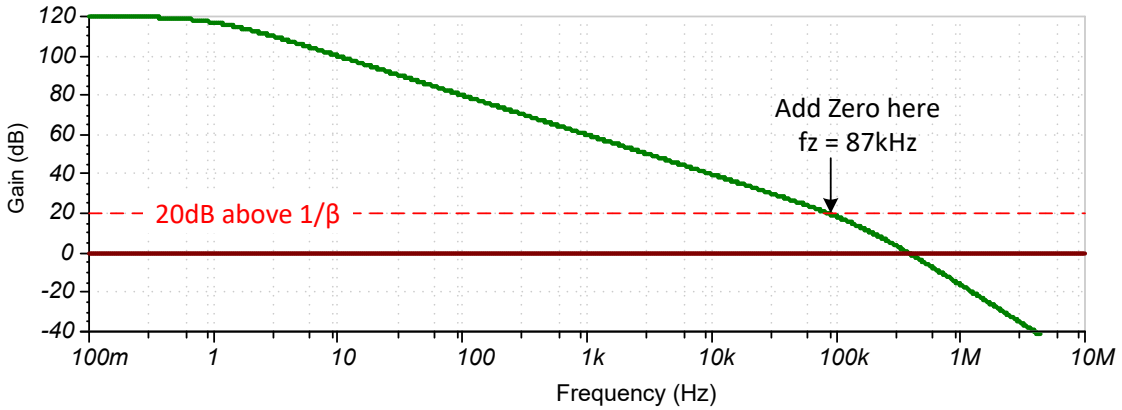


**Figure 4-8. Find Zero Location for Conservative Design Procedure**

$R_{ISO}$ design method for minimum $R_{ISO}$ shows the design procedure that produces the minimum value for $R_{ISO}$. For an op amp with a single dominant pole, this method results in a phase margin of at least 45°. Most op amps have additional poles and zeros near the unity gain bandwidth, so the phase margin is impacted by the secondary poles. Using the minimum value for $R_{ISO}$ provides the maximum bandwidth and has the minimum voltage drop when driving load impedances ($V_{DROP} = I_L \times R_{ISO}$). However, the minimum $R_{ISO}$ also has less tolerance to process, temperature, and component variation.

**Note**

**$R_{ISO}$ design method for minimum $R_{ISO}$:**

1. Select $R_{ISO}$ using Equation 28
2. This method finds the minimum value for $R_{ISO}$ and still generally achieves at 45° or more of phase margin.
3. The equation places the zero directly at the location where $A_{OL}$ intersects 1/β.
4. When choosing a standard resistor value always round the resistance to a larger value.

$$R_{ISO} = \frac{1 + \sqrt{1 + \left(8\pi \times R_O \times C_{LOAD} \times f_{gbw}\right)}}{4\pi \times C_{LOAD} \times f_{gbw}} \quad (28)$$

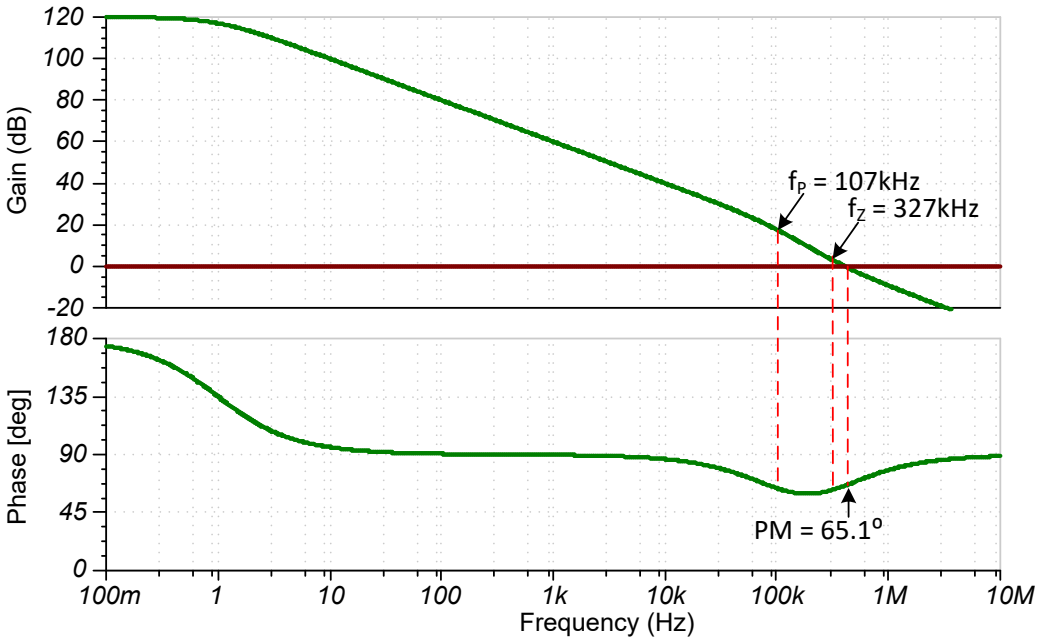


**Figure 4-9. Open-Loop Response for Minimum $R_{ISO}$**

Figure 4-10 shows the transient overshoot for the example circuit with $R_{ISO}$ = 0Ω, $R_{ISO}$ = 48.6Ω, and $R_{ISO}$ = 181Ω. Based on these results, the circuit without an isolation resistance ($R_{ISO}$ = 0Ω) has large overshoot and ringing. The circuit with minimum isolation resistance ($R_{ISO}$ = 48.6Ω), has a relatively small overshoot and good phase margin. The circuit with $R_{ISO}$ = 181Ω has practically no overshoot and excellent phase margin. Measuring the overshoot at the output of the op amp is important to get an idea of the stability of the circuit.

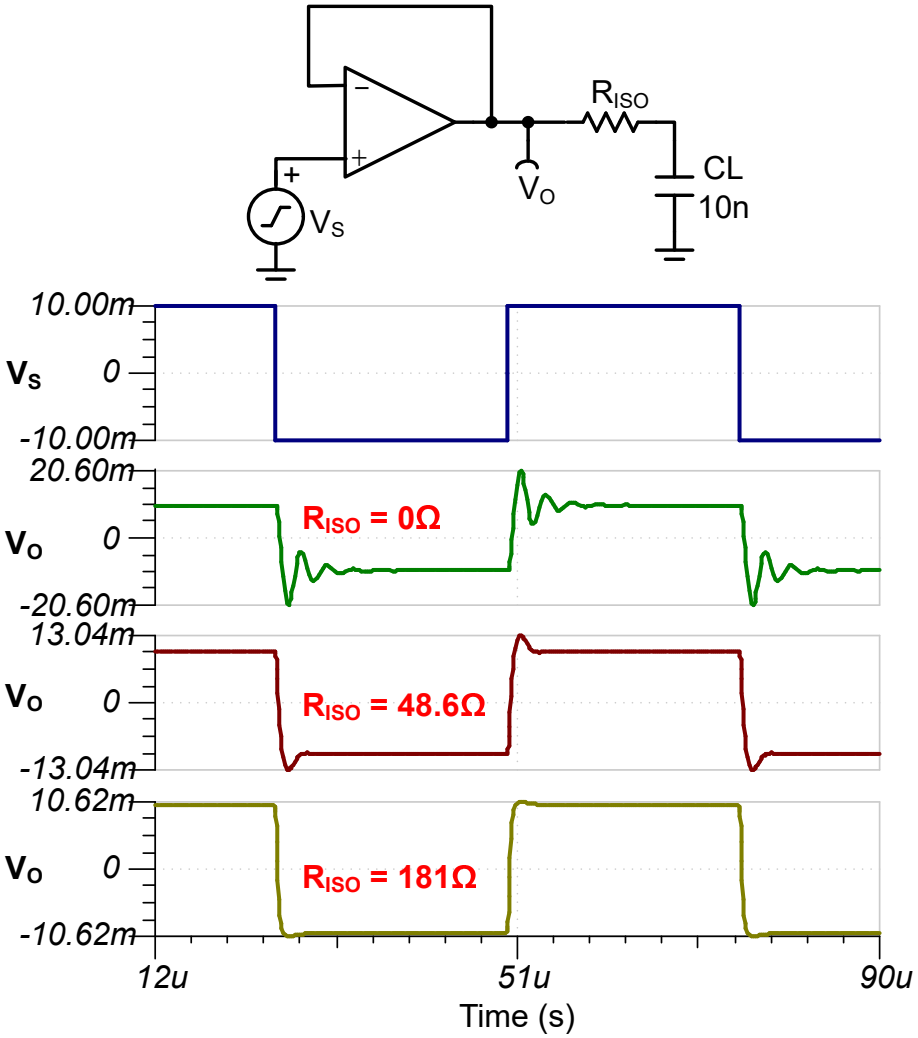


**Figure 4-10. Transient Response for Different Values of $R_{ISO}$**

Figure 4-11 shows the AC response of the op amp circuit regarding the load. The objective here is to show the frequency response at the load and not to measure stability by looking at AC gain peaking. To measure stability using AC gain peaking, the measurement must be made directly at the op amp output, not at the load. $R_{ISO}$ and $C_L$ form a low pass filter, so larger values of $R_{ISO}$ reduces the bandwidth. Figure 4-11 shows that the isolation resistance causes the bandwidth to drop from 602kHz for $R_{ISO}$ = 0Ω to 107kHz for $R_{ISO}$ = 181Ω.

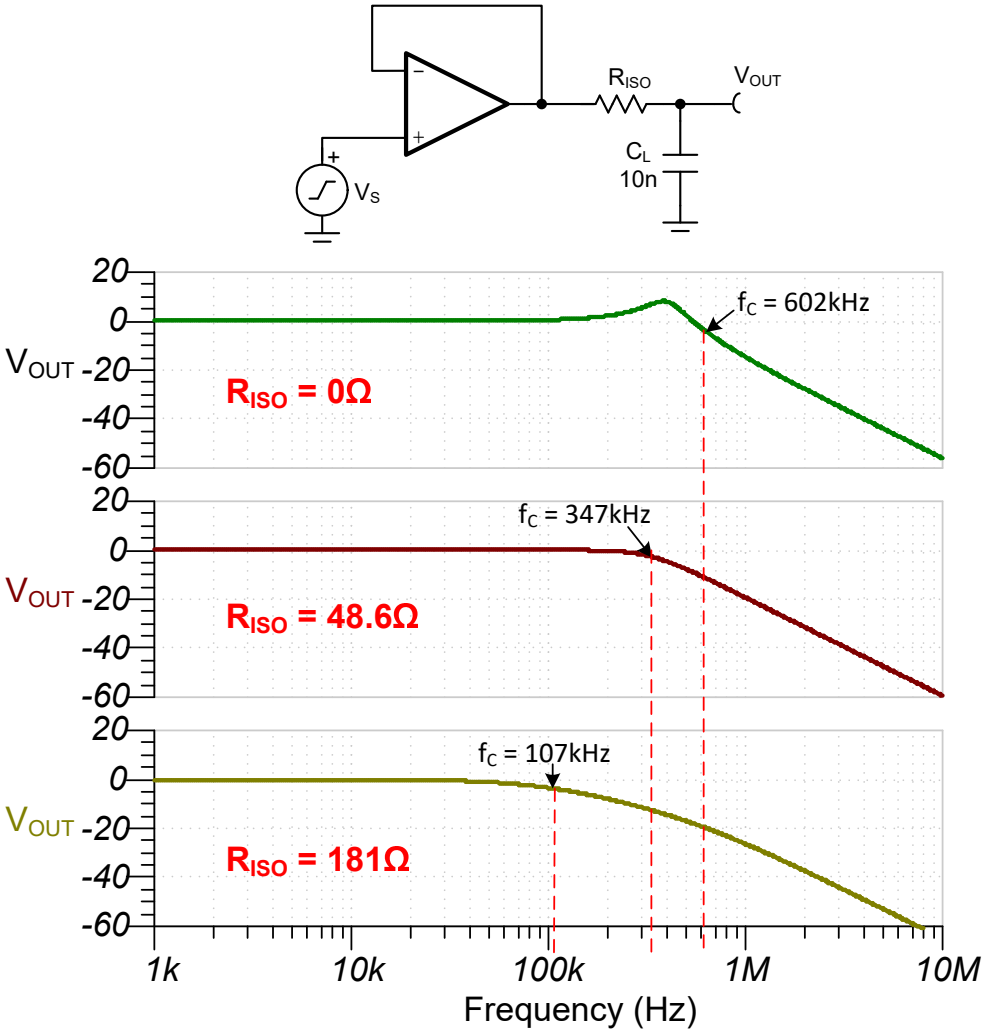


**Figure 4-11. Bandwidth for Different Values of $R_{ISO}$**

## 4.2 Dual Feedback Method

Figure 4-12 illustrates the main disadvantage of the $R_{ISO}$ method. When an amplifier with an isolation resistance drives a resistive load, a voltage divider is formed. The voltage divider attenuates the amplifier output at the load:

$$V_{OUT} = V_O \times R_L / (R_L + R_{ISO}) \quad (29)$$

The graph in Figure 4-12 shows that the 10mV step input is attenuated by 2.67mV at the output. The attenuation is a gain error that can be calibrated out if the load resistance is well controlled, but this is not practical in some cases. The $R_{ISO}$-dual-feedback topology eliminates the voltage divider effect seen in the $R_{ISO}$ method by using an output sense feedback path. Figure 4-13 shows the $R_{ISO}$-dual-feedback implementation with the same op amp and capacitive load as Figure 4-5. Notice that $V_{OUT}$ on the $R_{ISO}$-dual-feedback circuit settles to the same voltage as the input signal. The amplifier output ($V_O$ in Figure 4-13) settles to a voltage greater than the input signal to compensate for the drop across $R_{ISO}$. The voltage swing of the $R_{ISO}$-dual-feedback circuit at the load ($R_L$) is limited by the voltage drop across $R_{ISO}$.

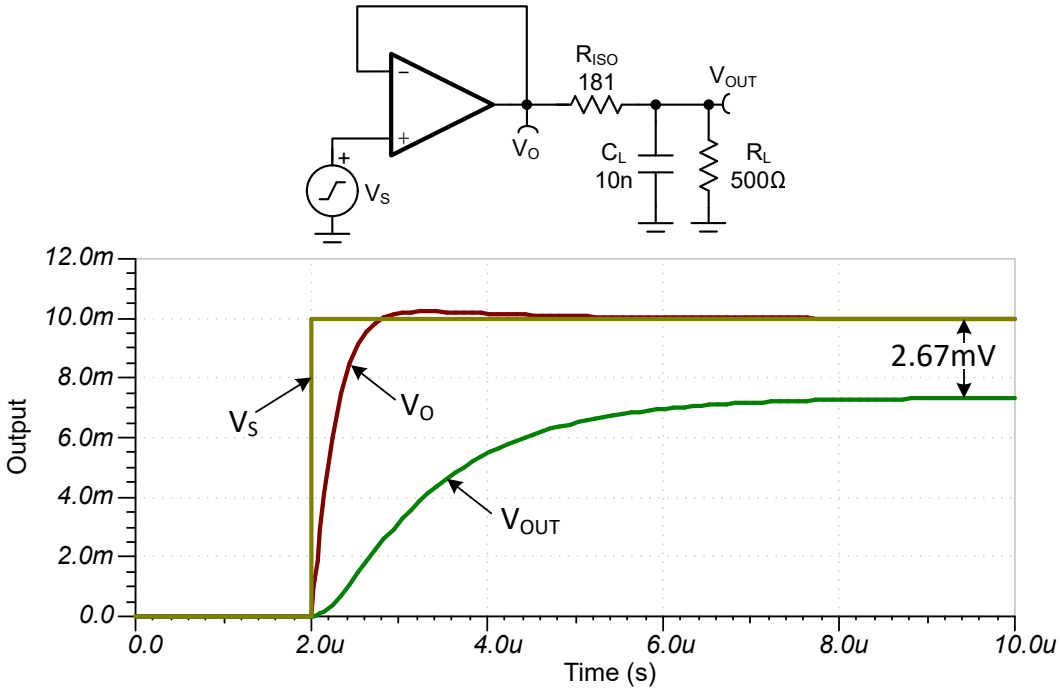


**Figure 4-12. $R_{ISO}$ Voltage Attenuation at the Load**

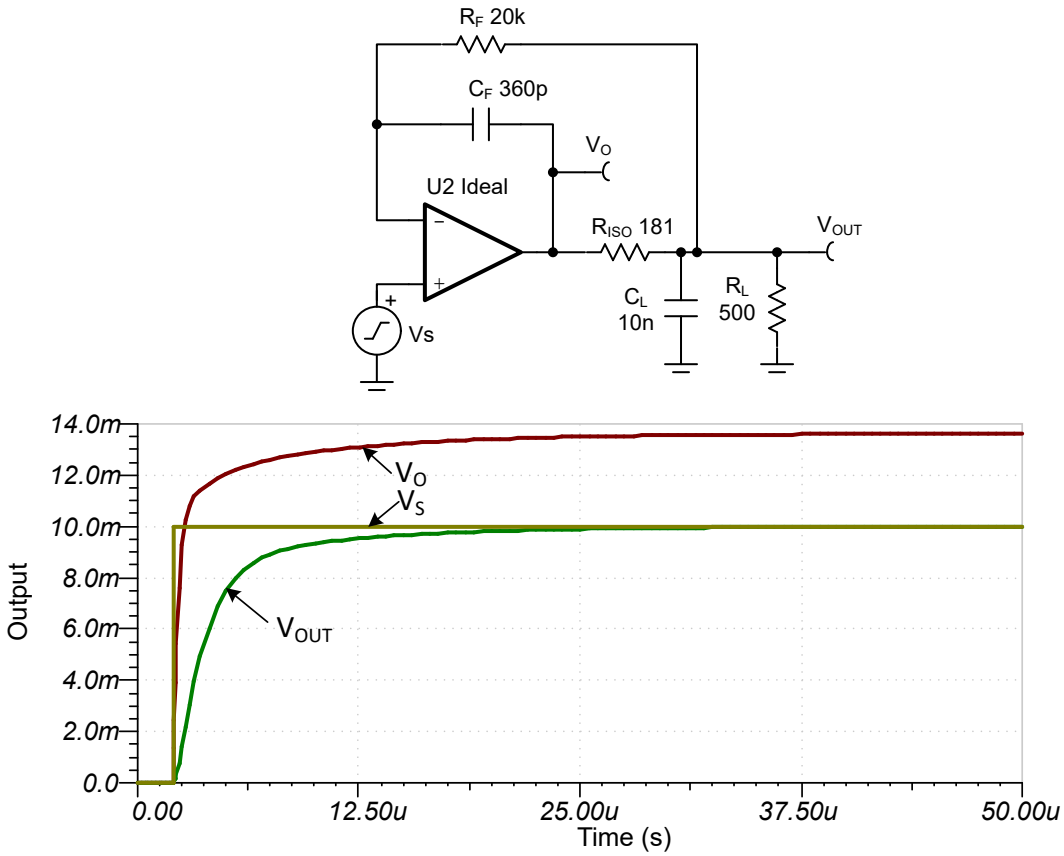


**Figure 4-13. $R_{ISO}$-Dual-Feedback Voltage at Load Equal to Input ($V_S = V_{OUT}$)**

At low frequencies, the impedance of a capacitor can be considered an open circuit, and at high frequencies the impedance is a short circuit:

$$X_C = 1/(2 \times \pi \times f \times C) \quad (30)$$

The $R_{ISO}$-dual-feedback circuit operation can be understood by considering the low and high-frequency operation separately (see Figure 4-14). At low frequency, the feedback capacitor is open and the feedback resistor $R_F$ senses the output $V_{OUT}$. The op amp adjusts the output $V_O$ until $V_O = V_{OUT}$. For the DC circuit, the voltage on the inverting and non-inverting input are equal due to the virtual short. Since there is no current flowing through $R_F$, there is no drop across $R_F$ so $V_{OUT} = V_{INV} = V_S$. At high frequencies, the feedback capacitor $C_F$ acts like a short. Compared to the low impedance of the $C_F$ capacitor at high frequency, the feedback resistor is an open circuit. For the high frequency operation, the circuit looks the same as the $R_{ISO}$ circuit. Thus, for a low frequency operation, the feedback resistor forces the output to be equal to the source voltage, and for a high frequency operation, the isolation resistance provides stability for the capacitive load.

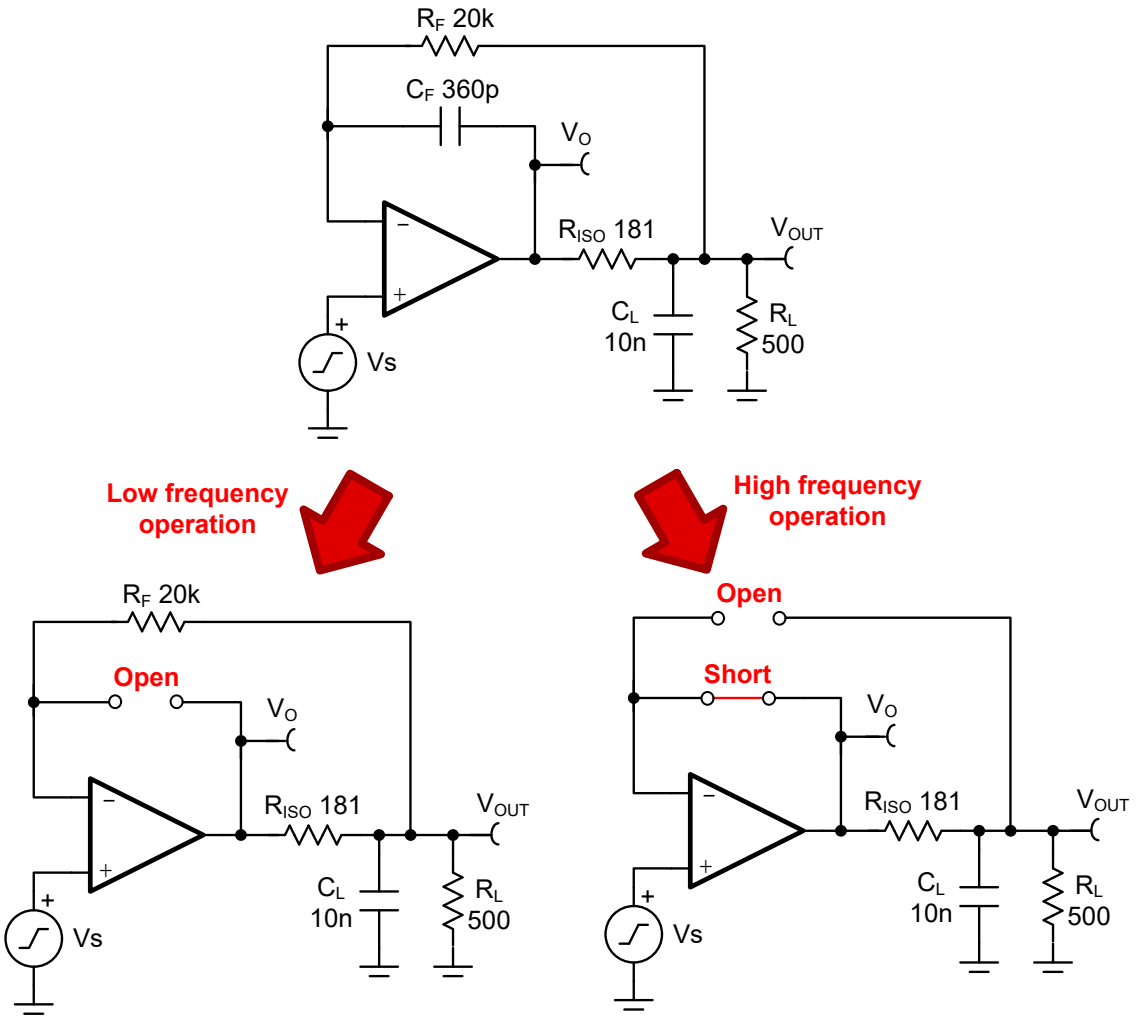


**Figure 4-14. AC and DC Operation of $R_{ISO}$-Dual-Feedback Configuration**

$R_{ISO}$-Dual-Feedback design method illustrates the step-by-step method for choosing the components for the $R_{ISO}$-dual-feedback topology. First, select $R_{ISO}$ using the same methods explained in $R_{ISO}$ conservative design method or $R_{ISO}$ design method for minimum $R_{ISO}$. Second, choose $R_F$ to be at least 100 times larger than $R_{ISO}$. Setting $R_F$ greater than $R_{ISO}$ makes $R_F$ effectively open in the AC case (see Figure 4-14). Finally, choose $C_F$ according to Equation 31. Check the transient and AC response and adjust $C_F$ within the bounds of the inequality given in Equation 32 to improve the response. The derivation of the inequality is covered in Equation 31 and Equation 32.

**Note**

**$R_{ISO}$-Dual-Feedback Design Method**

1. Select $R_{ISO}$ using the $R_{ISO}$ conservative design method or $R_{ISO}$ design method for minimum $R_{ISO}$.
2. Set $R_F \geq 100 \times R_{ISO}$.
3. Set $C_F$ according to Equation 31.

$$C_F = \frac{4 \times R_{ISO} \times C_L}{R_F} \tag{31}$$

$$\frac{2 \times R_{ISO} \times C_L}{R_F} \leq C_F \leq \frac{10 \times R_{ISO} \times C_L}{R_F} \tag{32}$$

The values for Figure 4-15 were derived using $R_{ISO}$-Dual-Feedback design method and rounded to standard resistor and capacitor values. This example uses the same amplifier from Figure 4-5. The nominal value for $C_F$ is 180pF from Equation 31. $C_F$ can be adjusted from 90pF to 905pF according to Equation 32 to improve settling and overshoot. This circuit is used throughout this section for transient and open-loop discussions.

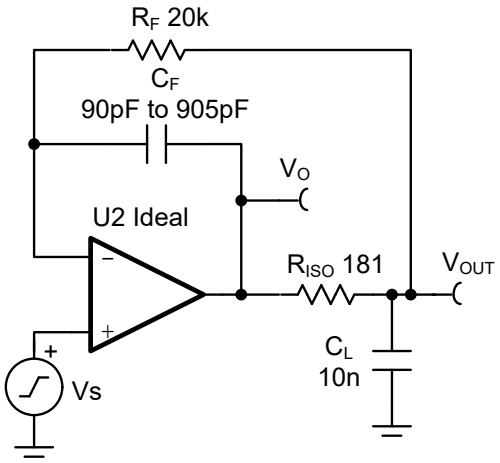


**Figure 4-15. $R_{ISO}$-Dual-Feedback Configuration From Design Procedure**

The design procedure in RISO-Dual-Feedback design method uses the inequality in Equation 32 to select the feedback capacitor. This inequality is used to prevent a resonance in the feedback network. To understand this potential resonance, splitting the feedback network into two paths using superposition is useful. Figure 4-16 and Figure 4-17 illustrate the two feedback paths. Each path constitutes a 1/β, and the combined 1/β is the minima of the two separate paths. The minima of the two paths are used to combine the two 1/β because the two 1/β are in parallel and the lowest impedance in parallel dominates.

The feedback path through $R_F$ is separated from the overall feedback network by opening $C_F$ (see FB1 in Figure 4-16). FB1 is a simple RC filter that generates a zero in 1/β1 (see Equation 33). The transfer function for 1/β1 approaches 0dB and low frequency and increases at 20dB per decade at high frequency. Equation 35 shows the zero frequency, where 1/β1 is +3dB. The feedback through $C_F$ is separated from the overall feedback network by opening $R_{ISO}$ (see FB2 in Figure 4-17). For this analysis we assume that the capacitive reactance of $C_L$ is very low so that the reactance acts as a short. The transfer function of 1/β2 has both a pole and a zero (see Equation 34). The pole is located at 0Hz, so the function continuously rolls off at 20dB/decade for low frequency. At higher frequency, the pole is canceled by the zero, so 1/β2 flattens out at approximately 0dB. The zero frequency for FB2 is given in Equation 36. Figure 4-18 illustrates 1/β1, 1/β2, and the combined 1/β. Since both feedback paths contain complex numbers, the combined 1/β do not linearly add as there is some calculation in the complex addition. Notice that the combined 1/β shows a resonant peak where the two 1/β functions cross. This resonance can cause instability if the inequality in Equation 32 is not followed.

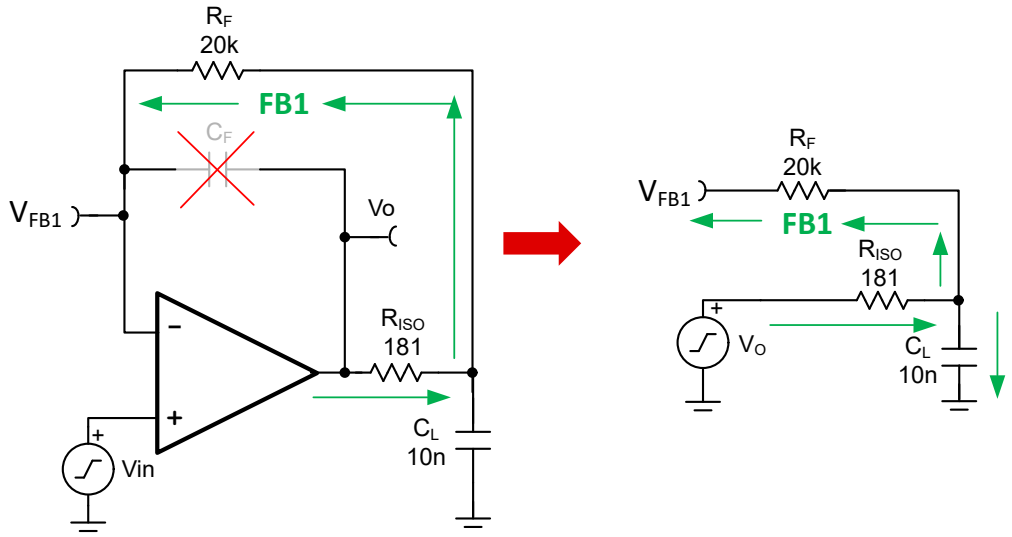


**Figure 4-16. Superposition of Feedback Paths for 1/β (Feedback Through $R_F$)**

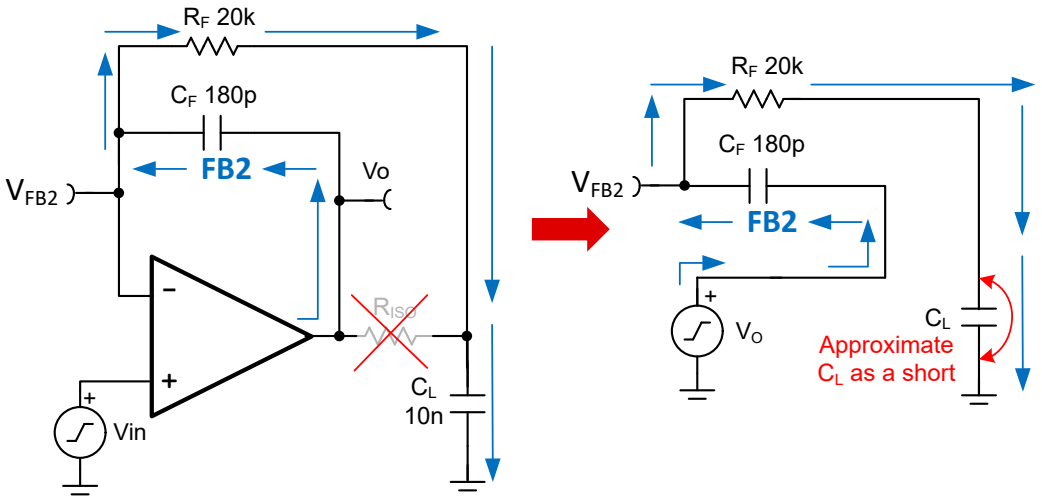


**Figure 4-17. Superposition of Feedback Paths for 1/β (Feedback Through $C_F$)**

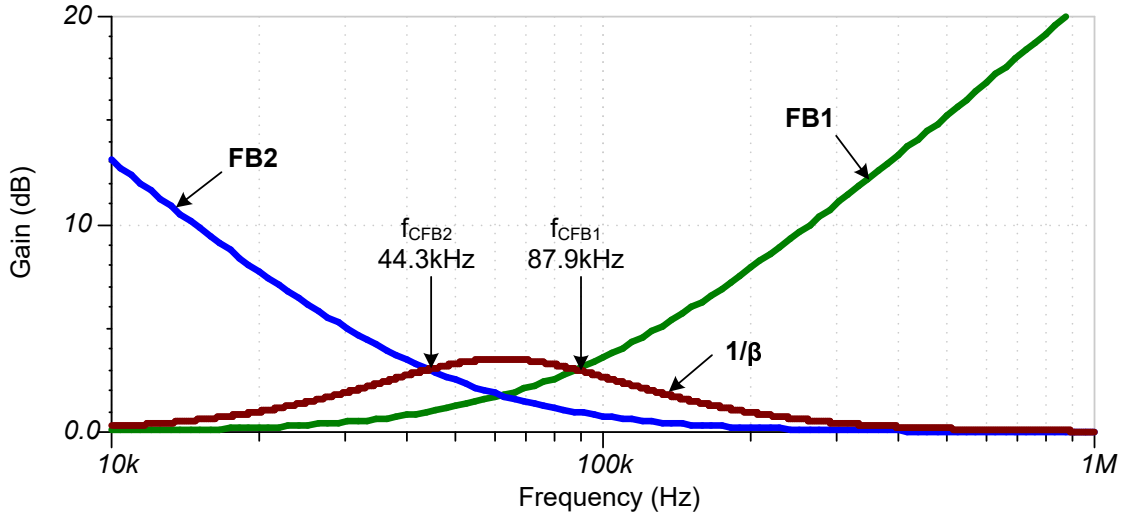


**Figure 4-18. 1/β for Both Feedback Paths and Combined 1/β**

$$\frac{1}{\beta_1} = \frac{V_O}{V_{FB1}} = \frac{s}{1/(R_{ISO} \times C_L)} + 1 \quad (33)$$

$$\frac{1}{\beta_2} = \frac{V_O}{V_{FB2}} = \frac{R_F \times C_F + 1}{R_F \times C_F \times s} \quad (34)$$

$$f_{FB1} = \frac{1}{2 \times \pi \times R_{ISO} \times C_L} \quad (35)$$

$$f_{FB2} = \frac{1}{2 \times \pi \times R_F \times C_F} \quad (36)$$

The resonance in 1/β occurs when the 3dB points on 1/β1 and 1/β2 are too close together. For example, if the 3dB point on 1/β2 is much lower than the 3dB point on 1/β1, then the two curves combine to form a relatively flat 1/β. Conversely, when the two 3dB points are close together, the two curves combine to form a resonant peak in 1/β (see Figure 4-19). This relationship between the cutoff frequencies determines the basis for the inequality (see Equation 37 through Equation 40 for derivation). Inspecting Figure 4-19, you can graphically see that $f_{CB1} > f_{CB2}$ minimizes resonant peaking (see Equation 37 and Equation 38). To complete this derivation, remember that taking the reciprocal on both sides of the inequality flips the inequality sign for positive numbers (see Equation 39). Dividing by $2 \times \pi \times R_F$ yields Equation 40. Based on empirical results, $C_F$ must be at least two times $C_L \times R_{ISO} / R_F$ to avoid instability due to the resonance. The factor of 10 for the maximum value of $C_F$ was selected empirically to achieve a reasonable settling time. Technically, a larger factor can be used but then the settling is unnecessarily long.

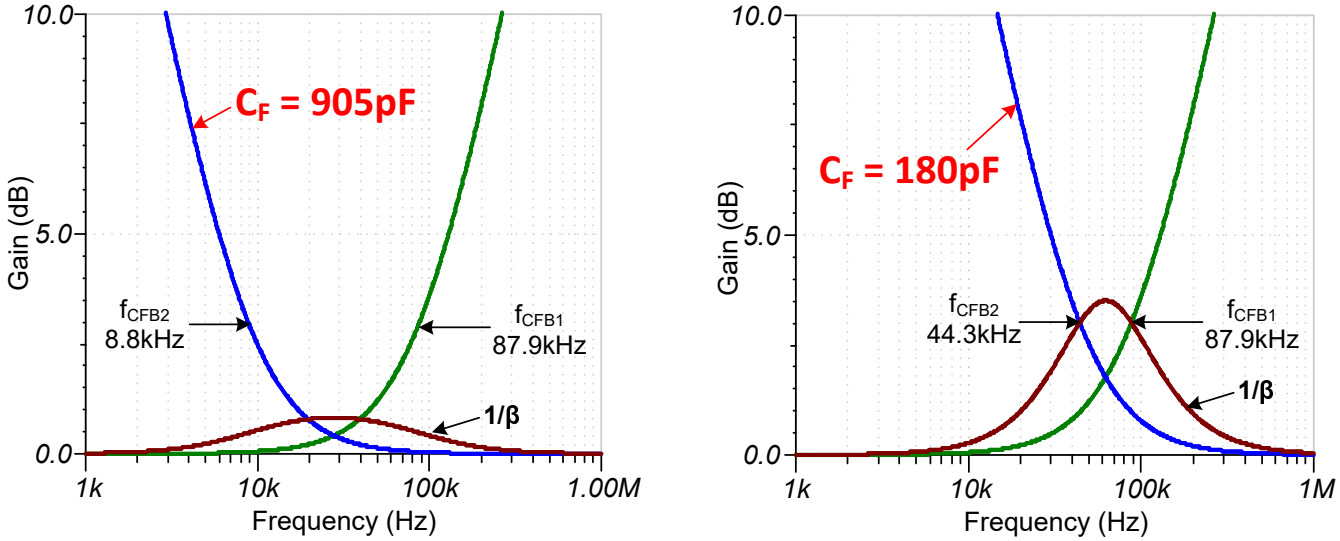


**Figure 4-19. Impact of 3dB Spacing on 1/β Curves for Resonant Peaking**

$$f_{CFB1} > f_{CFB2} \quad (37)$$

$$\frac{1}{2 \times \pi \times R_{ISO} \times C_L} > \frac{1}{2 \times \pi \times R_F \times C_F} \quad (38)$$

$$2 \times \pi \times R_{ISO} \times C_L < 2 \times \pi \times R_F \times C_F \quad (39)$$

$$C_F > \frac{R_{ISO} \times C_L}{R_F} \quad (40)$$

The transient response of the circuit from Figure 4-15 is simulated in Figure 4-20 across the range of $C_F$ from the design procedure. The target value of $C_F$ from the procedure is 362pF, but the range allows for $C_F$ from 90.5pF to 905pF. Figure 4-20 shows that the percentage overshoot is highest for the smallest capacitance, so if overshoot is a concern, choose a larger $C_F$ value. Figure 4-21 illustrates the same transient response with the axis scaled to illustrate a 0.1% settling time. Since the output settles to 5mV, the axis is adjusted to 5mV ±

0.01mV for 0.1% settling. In general, the settling time increases for larger values of $C_F$. The exception to this trend happens for very low values of $C_F$, where the feedback is starting to become resonant (181pF in this case). Thus, overshoot decreases for larger values of $C_F$ and settling time decreases. The recommended value of 362pF assumes the goal is for the shortest settling time while avoiding the resonance. See table Table 4-1 for a summary of settling time and overshoot versus $C_F$.

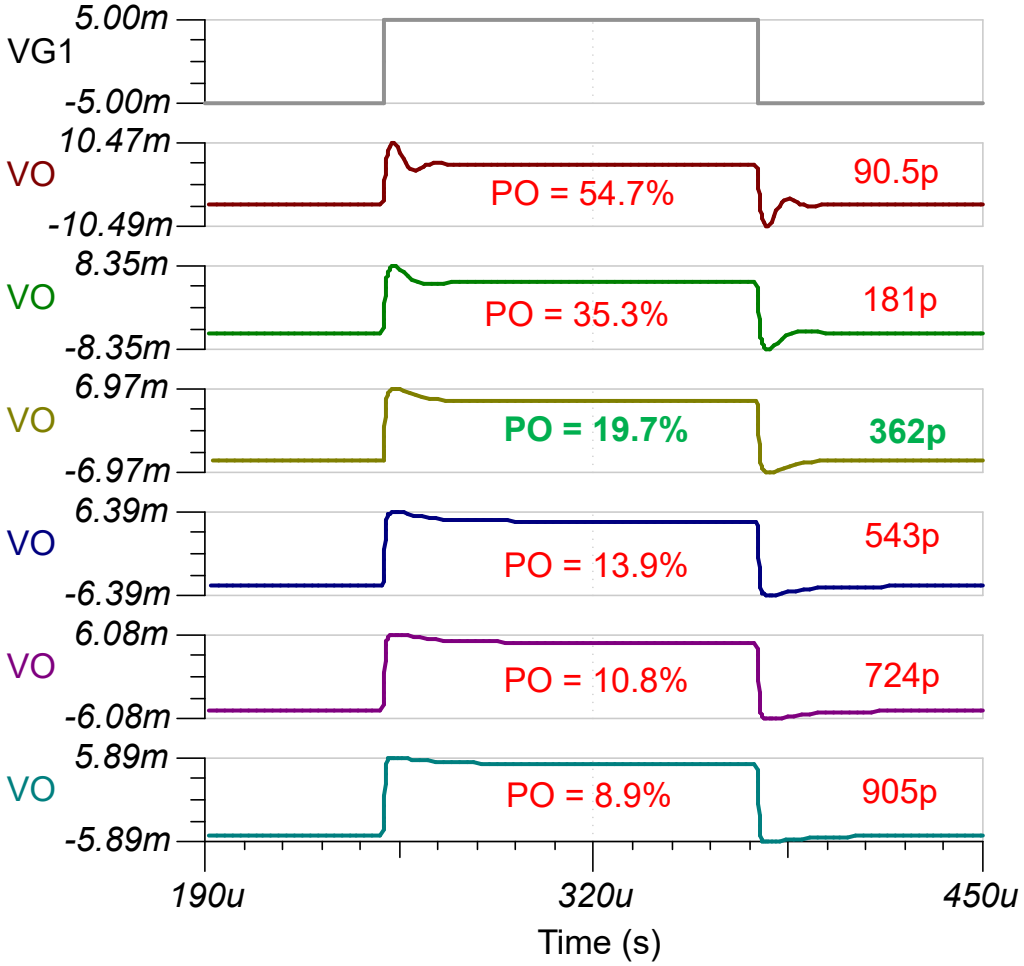


**Figure 4-20. RISO-Dual-Feedback Transient Response**

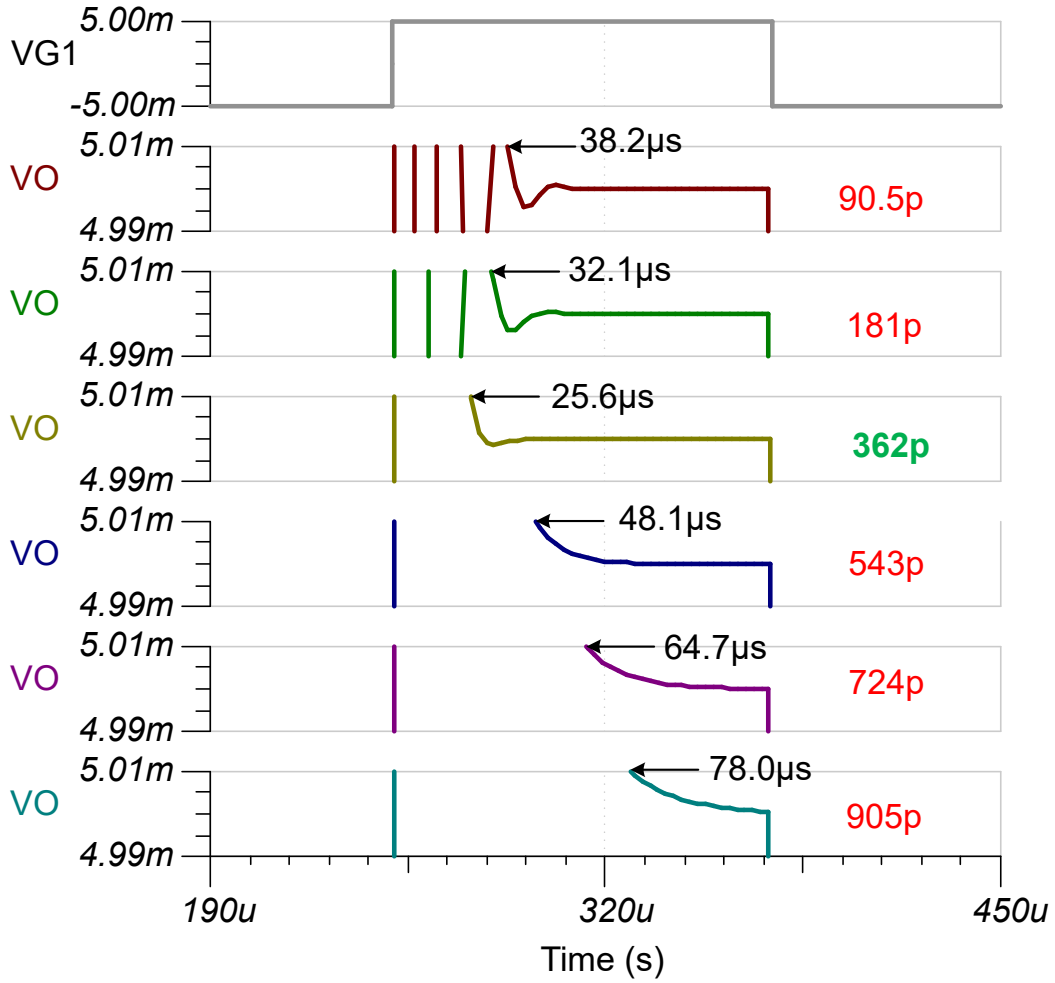


**Figure 4-21. $R_{ISO}$-Dual-Feedback 0.1% Settling Transient Response**

Figure 4-22 illustrates the open-loop response for Figure 4-15. The portion of the curve where 1/β1 and 1/β2 intersect is magnified and shown for different values of $C_F$. The phase response for different values of $C_F$ is also shown. Note that the highest magnitude of resonant peaking and most dramatic phase shift occurs for the smallest feedback capacitor. Notice that the resonance occurs at a frequency below the point where $A_{OL}$ intersects 1/β. Meaning, the resonance occurs below the point where phase margin is tested. This means that the resonance does not have a significant effect on phase margin. For circuits with very low $C_F$, the resonance can cause instability even though the phase margin is good. Table 4-1 shows the settling time, percentage overshoot, and phase margin across the range of $C_F$ for Figure 4-15. Note that the phase margin looks good for all cases and shows no relationship to the percentage overshoot. This outcome is because phase shift from the resonance happens at a frequency below the phase margin test. Thus, instability due to the feedback resonance is not detected by the phase margin test. To avoid feedback resonance, adhere to the capacitance range in Equation 32 and inspect the 1/β curve for resonant peaking.

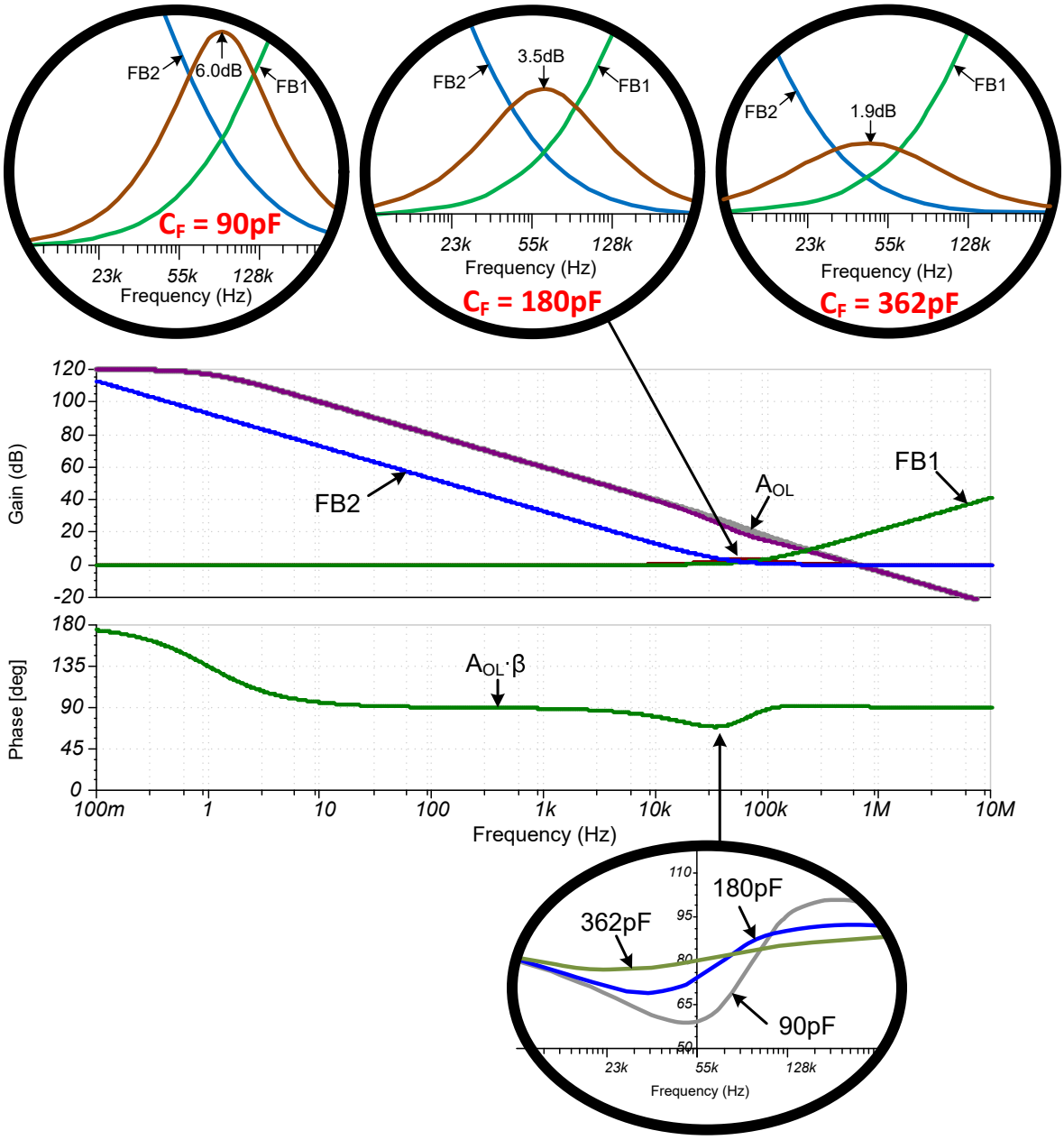


**Figure 4-22. Open-Loop Dual-Feedback Response for Different $C_F$**

**Table 4-1. $R_{ISO}$-Dual-Feedback Transient Summary**

| $C_F$ (pF) | 0.1% Settling (µs) | Percent Overshoot | Phase Margin Open-Loop Test |
|---|---|---|---|
| 90.5 | 38.2 | 54.7 | 95.0° |
| 181 | 32.1 | 35.3 | 91.0° |
| 362 | 25.6 | 19.7 | 89.1° |
| 543 | 48.1 | 13.9 | 88.5° |
| 724 | 64.7 | 10.8 | 88.1° |
| 905 | 78.0 | 8.6 | 88.0° |

Inspecting the transient response in Figure 4-21 shows that graphs with low values of $C_F$ have a dampened sinusoidal oscillation, whereas graphs with low $C_F$ have an initial overshoot and a long settling tail. This settling behavior depends on whether the poles in the closed-loop transfer function are real or complex conjugates. The transfer function for a system with complex conjugate poles is given in Equation 41 and the transient step response is given in Equation 42. Note that the transient step response for complex poles is an exponentially dampened sinusoidal function. The transfer function for a system with two real poles is given in Equation 43 and the transient step response is given in Equation 44. The transient step response for real poles contains two exponential functions with two different time constants. Normally, the exponential with the short time constant has a large coefficient that corresponds to the overshoot. The exponential with the short time constant has a coefficient that cancels the other exponential when settled (5-time constants). The combination of the two exponentials produces a large overshoot with a long settling tail. Thus, for the dual-feedback circuit, large values of $C_F$ produce the smallest overshoot but have the longest settling tail (see Figure 4-23). From a practical perspective, the response with the dampened sinusoidal waveform is an indication of instability, whereas the single overshoot with a long settling tail indicates two real poles. The main concern with the system containing two real poles is that the long settling time limits the accuracy and speed of the system (see Demystifying pole-zero doublets).

$$G_I(s) = \frac{{\omega_n}^2}{s^2 + 2\zeta\omega_n s + \omega_n} \tag{41}$$

$$\mathcal{L}^{-1}\left(G_I(s) \times \frac{1}{s}\right) = 1 - e^{-\zeta\omega_n t}\left(\cos(\omega_d t) - \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\omega_d t\right) \tag{42}$$

$$G_R(s) = \frac{1 + s/\omega_z}{(1 + s/\omega_1)(1 + s/\omega_2)} \times \frac{1}{s} \tag{43}$$

$$\mathcal{L}^{-1}\left(G_R(s) \times \frac{1}{s}\right) = 1 - \left(V_1 e^{-\omega_1 t} - V_2 e^{-\omega_2 t}\right) \tag{44}$$

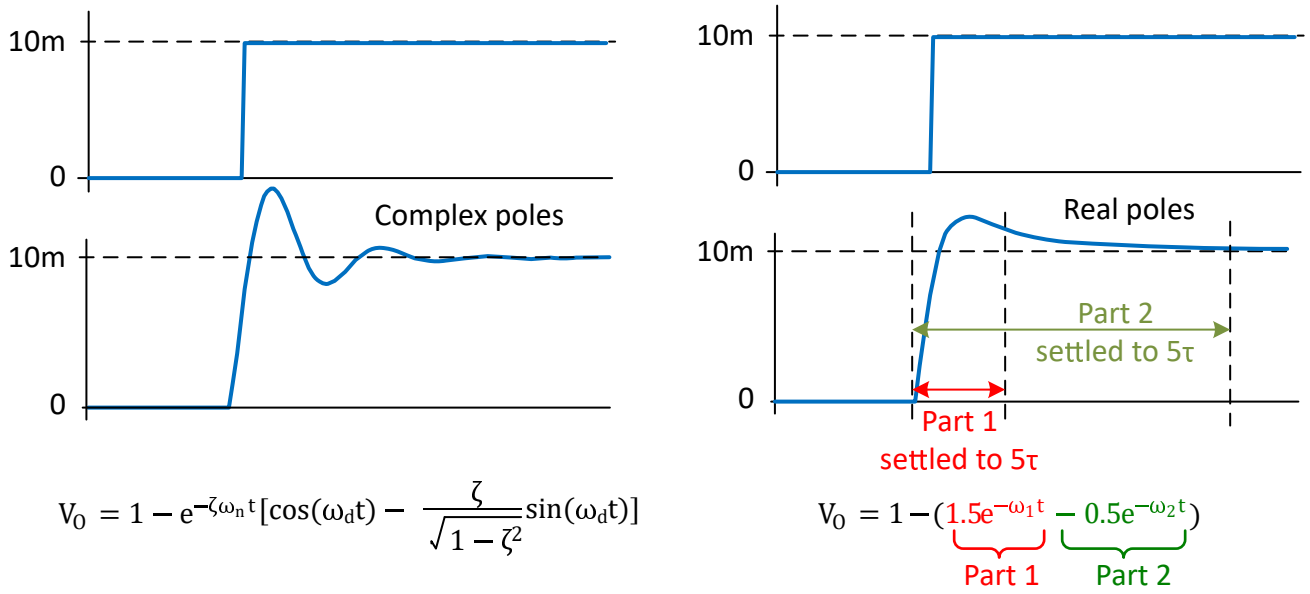


**Figure 4-23. Step Response for Complex Versus Real Poles**

### 4.2.1 $R_{ISO}$-Dual-Feedback With $R_L$

The design procedure, open-loop response, and transient response in Dual Feedback Method apply to the dual-feedback configuration ***without a load resistance***. The effects of the load resistance are not included in the equations and examples because omitting $R_L$ produces the worst-case results. In general, the $R_{ISO}$-dual-feedback method is used with loads; although in many cases, the load impedance is not defined or potentially varies across a large range. Thus, using the design procedure produces an amplifier that is stable across a wide range of loads. This section shows updated equations and how $R_L$ impacts the transient and open-loop response for the $R_{ISO}$-dual-feedback configuration.

Figure 4-16 and Figure 4-17 show how the superposition method can be used to analyze the two feedback paths for $R_{ISO}$-dual-feedback. The same method can be applied to derive the 1/β paths with a load resistance $R_L$. The main impact that adding a load resistance has on the RISO-dual-feedback configuration is on feedback path two. Figure 4-24 illustrates the modified 1/β response, Equation 45 illustrates the resultant 1/β2 equation, and Equation 46 provides the zero frequency.

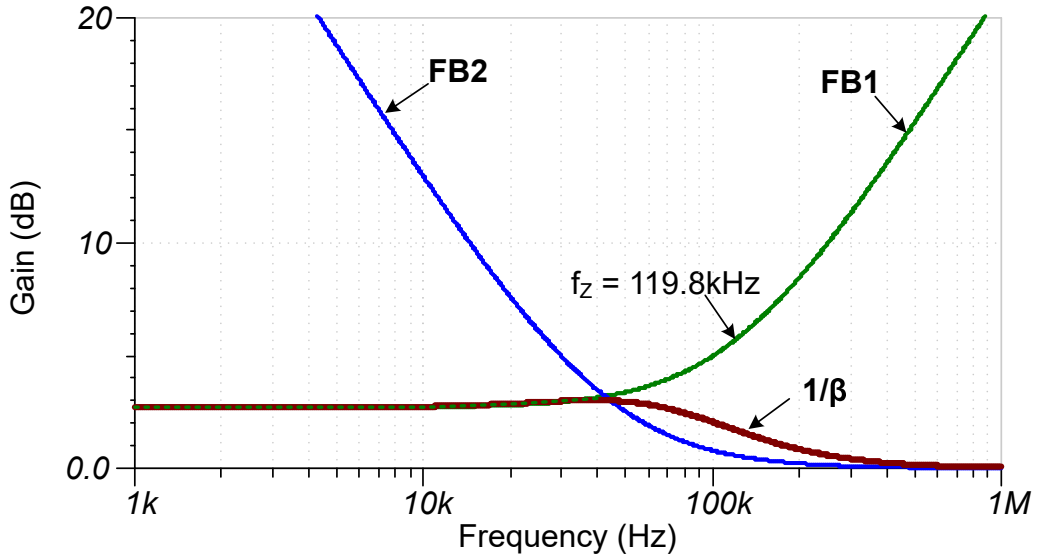


**Figure 4-24. 1/β for Both Feedback Paths and Combined 1/β With $R_L$ = 500Ω**

$$\frac{V_O}{V_{FB}} = \frac{s}{\left(\frac{1}{R_{ISO} \times C_L}\right)} + \frac{R_{ISO} + R_L}{R_L} \tag{45}$$

$$f_Z = \frac{R_{ISO} + R_L}{2 \times \pi \times R_{ISO} \times R_L \times C_L} \tag{46}$$

Figure 4-25 shows the percentage overshoot with a 500Ω load, and Figure 4-20 shows the same response without a load resistance. Figure 4-26 shows the 0.1% settling time with a 500Ω load, and Figure 4-21 shows the same response without a load resistance. Comparing the graphs to each other shows that including the load resistance dramatically reduced the overshoot. The comparison also shows that the loaded case generally has a longer settling time. Both cases have two real poles for $C_F \geq 262pF$. The two real poles produce a transient response with two exponential functions. One of the exponentials has a short time-constant and the other has a long time-constant. For the unloaded case, the short time constant produces an overshoot and the long time-constant is subtracted to cancel the overshoot (see Figure 4-23). For the loaded case, the short time-constant produces an undershoot and the long time-constant adds with the short time-constant to settle to the final value (see Figure 4-27). Table 4-2 summarizes the results for the loaded case. The main point of this section is that loading impacts the transient response for $R_{ISO}$-dual-feedback, therefore, confirm the operation of the circuit across the range of load resistances, as well as the range of load capacitances.

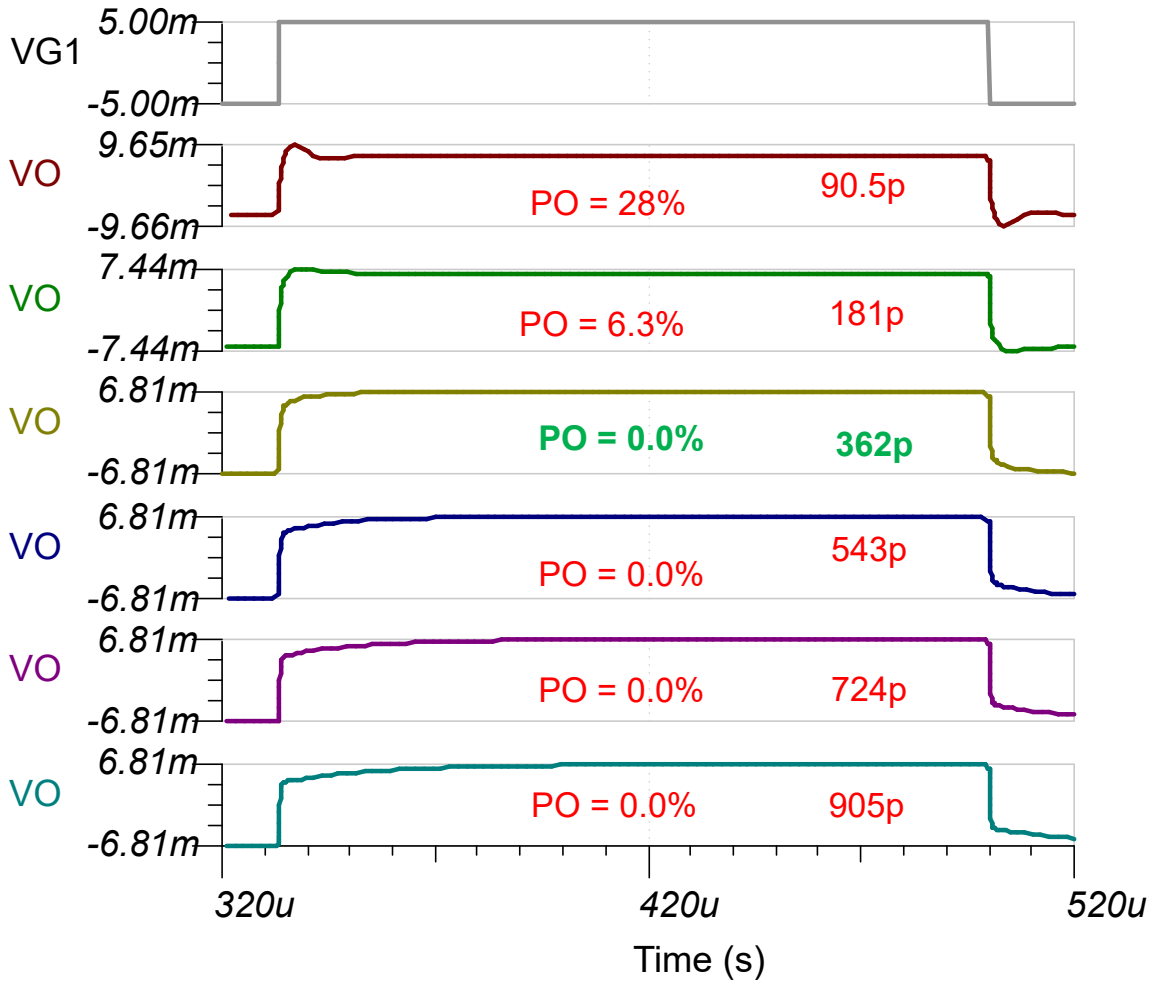


**Figure 4-25. RISO-Dual-Feedback Transient Response With RL**

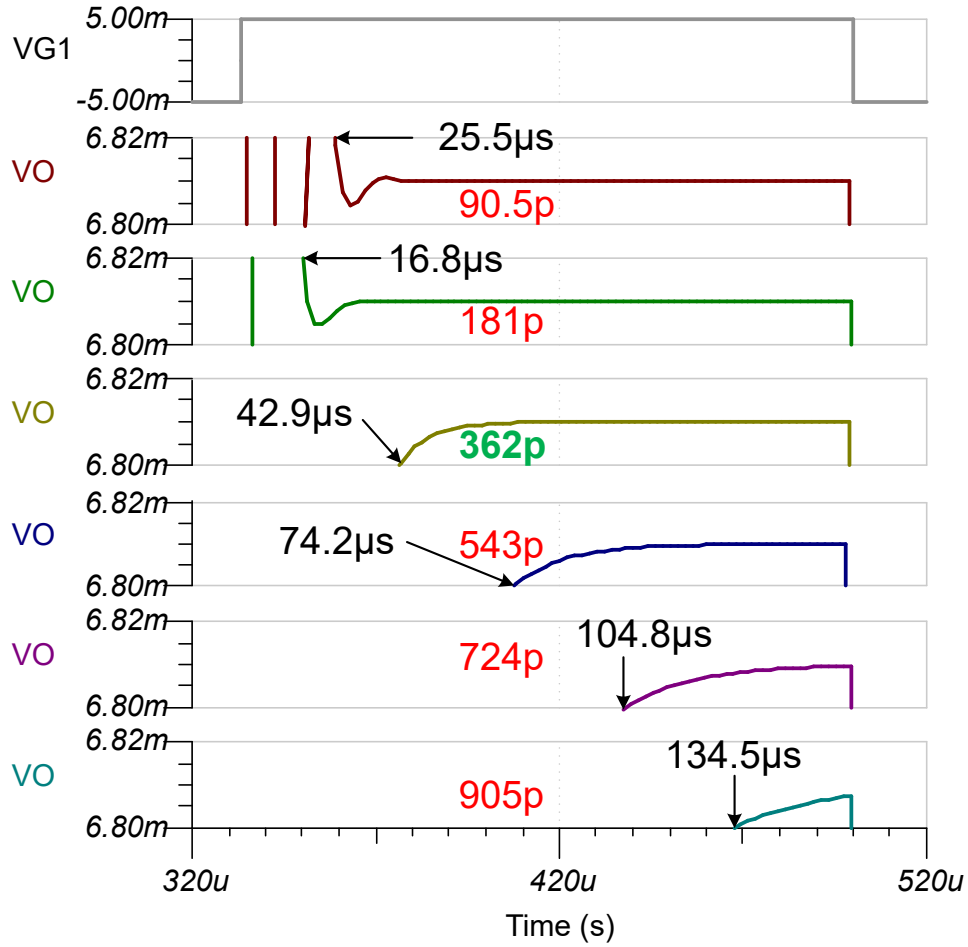


**Figure 4-26. $R_{ISO}$-Dual-Feedback 0.1% Settling Transient Response With RL**

**Table 4-2. $R_{ISO}$-Dual-Feedback With $R_L$ Transient Summary**

| $C_F$ (pF) | 0.1% Settling (µs) | Percent Overshoot | Phase Margin Open-Loop Test |
|---|---|---|---|
| 90.5 | 25.5 | 28.0 | 95.0° |
| 181 | 16.8 | 6.3 | 91.1° |
| 362 | 42.9 | 0.0 | 89.1° |
| 543 | 74.2 | 0.0 | 88.5° |
| 724 | 104.8 | 0.0 | 88.2° |
| 905 | 134.5 | 0.0 | 88.0° |

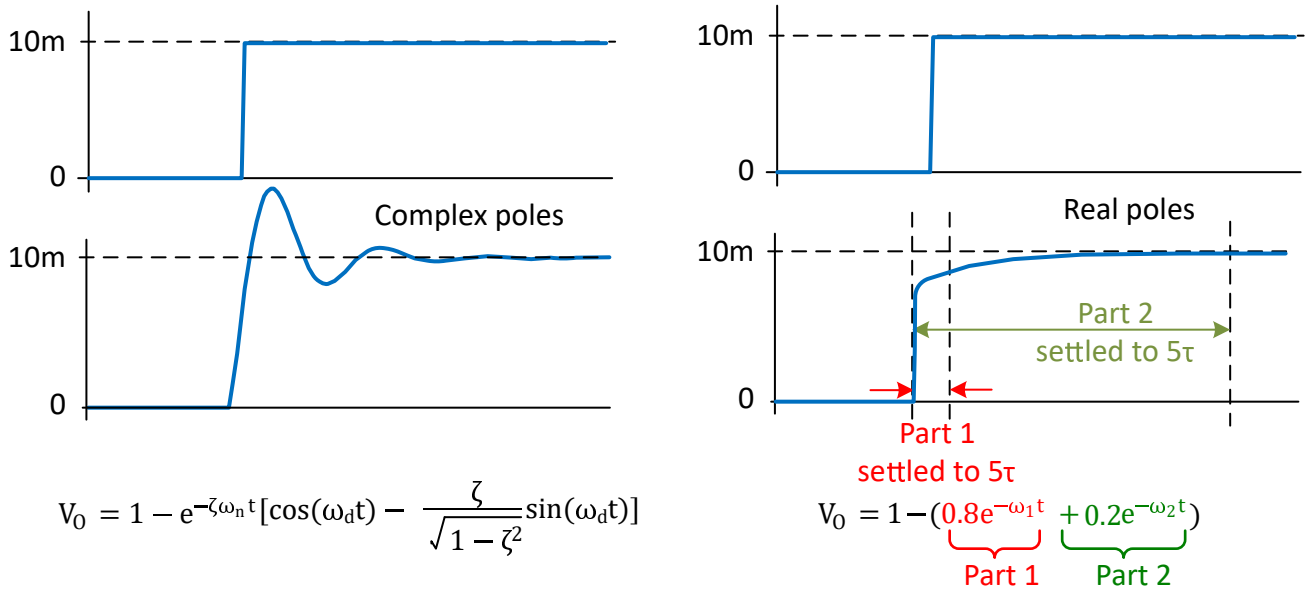


**Figure 4-27. Step Response for Complex Versus Real Poles With RL = 500Ω**

### *4.2.2 Dual Feedback With $R_{FX}$ Method*

A modification of the $R_{ISO}$-dual-feedback circuit adds an additional resistor $R_{FX}$ in series with the $C_F$ capacitor, as show in Figure 4-28. The circuit is referred to as $R_{ISO}$+DFB+$R_{FX}$ for brevity. The circuit has some 1/β feedback behavioral similarities to the *Noise-Gain* circuit, in that the $R_{FX}$ component adds an additional zero-pole pair to the 1/β network. This modification of the $R_{ISO}$+DFB circuit is not useful, and often detrimental, when circuit compensation goals allow the selection of the Minimum $R_{ISO}$ value, as defined in earlier sections. The minimum $R_{ISO}$ method always has the fastest settling times for resistive output impedances. The merit of the $R_{ISO}$+DFB+$R_{FX}$ circuit is to increase the output transient settling time when larger $R_{ISO}$ values are required to stabilize capacitive loads. Circuits that require larger $R_{ISO}$ values are often associated with complex *inductive* open-loop output impedances, as described in later sections (see Instability Due to Resonance From Complex Output Impedance), or ones where the capacitive load is variable and a larger $R_{ISO}$ resistor is required to cover all cases. The $R_{ISO}$+DFB+$R_{FX}$ circuit improves response times by allowing smaller values of $C_F$ than are allowed in a traditional $R_{ISO}$+DFB circuit.

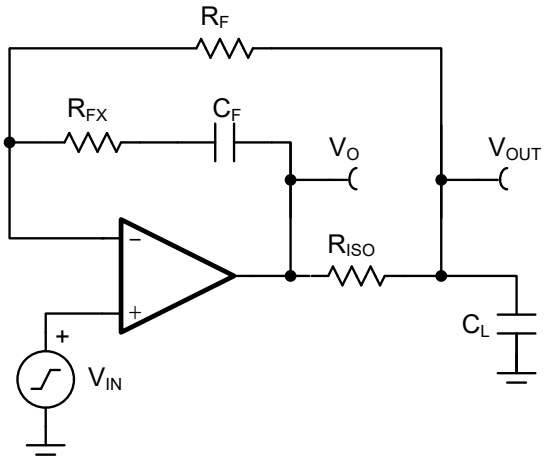


**Figure 4-28. Closed-Loop $R_{ISO}$-Dual-Feedback With $R_{FX}$**

Dual Feedback Method defines methods to avoid resonance in the $R_{ISO}$+DFB circuit, which occurs if the zero in 1/β from $R_{ISO} \times C_L$ occurs at the same, or lower frequencies than the $R_F \times C_F$ pole in 1/β. The criteria therefore defines how to select the $C_F$ value, which in turn sets the minimum $R_F \times C_F$ time-constant. Up to this point, the document has covered the transient response for circuits to a small-signal input step. Circuit stability is also sensitive to a step response in the load current (see Output Load Step for Stability Testing). For the $R_{ISO}$+DFB configuration, the input step response settling time is set by $R_{ISO} \times C_L$, whereas the response to a load current step is set by $R_F \times C_F$ (see Optimizing Input and Output Transient Settling Times for more details). Figure 4-29 shows an example of the $R_{ISO}$-DFB circuit responding to both an input step and load transient for OPA2991. Examining the transient response shows that the circuit settles significantly faster to the input step than the output load transient ($R_F \times C_F$ is greater than $R_{ISO} \times C_L$). Therefore, if the $C_F$ capacitor can be made smaller, the output settling time is improved. The $R_{FX}$ circuit addition allows for smaller $C_F$ values.

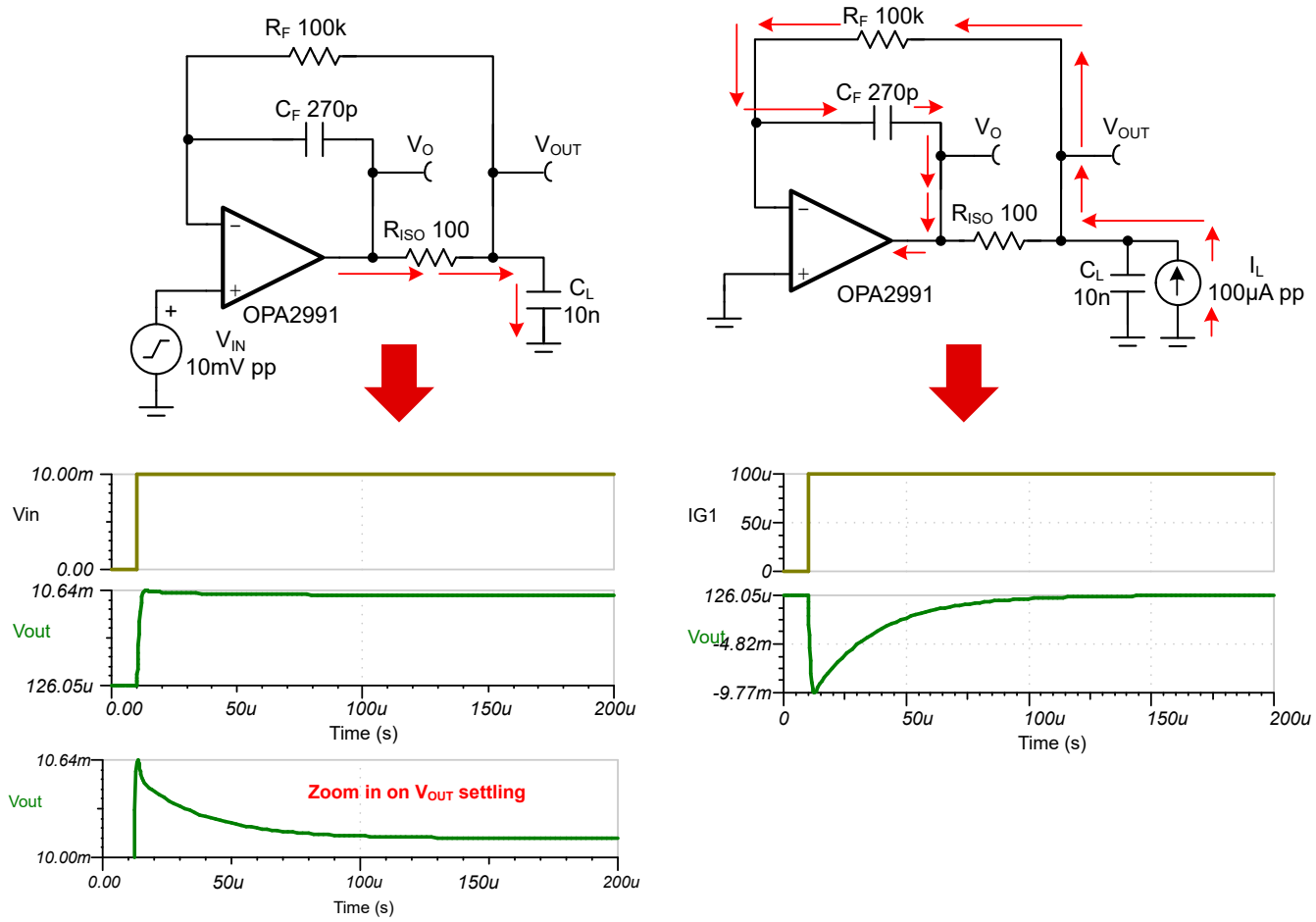


**Figure 4-29. Input Step Versus Output Load Transient Settling for $R_{ISO}$-Dual-Feedback**

For the example, $R_{ISO}$+DFB circuit in Figure 4-30, the 1µF capacitor only requires a 4.07Ω resistor using equaiton for minimum $R_{ISO}$, but in this example the capacitor is overcompensated with a 49Ω resistor. To avoid feedback resonance, the circuit requires a $C_F$ capacitor of 4 × ($R_{ISO}$ × $C_L$) / $R_F$ = 40nF to avoid unwanted peaking in 1/β (see Equation 31 in $R_{ISO}$-Dual-Feedback design method). Figure 4-31 shows a stable open-loop AC response for Figure 4-30 with a phase margin of 89.75°.

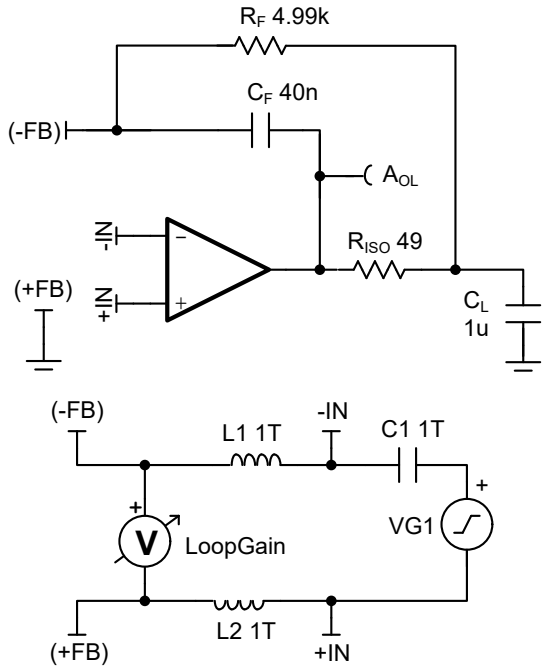


**Figure 4-30. Open-Loop Test Circuit for $R_{ISO}$+DFB+$R_{FX}$ Circuit With $R_{FX}$ = 0Ω**

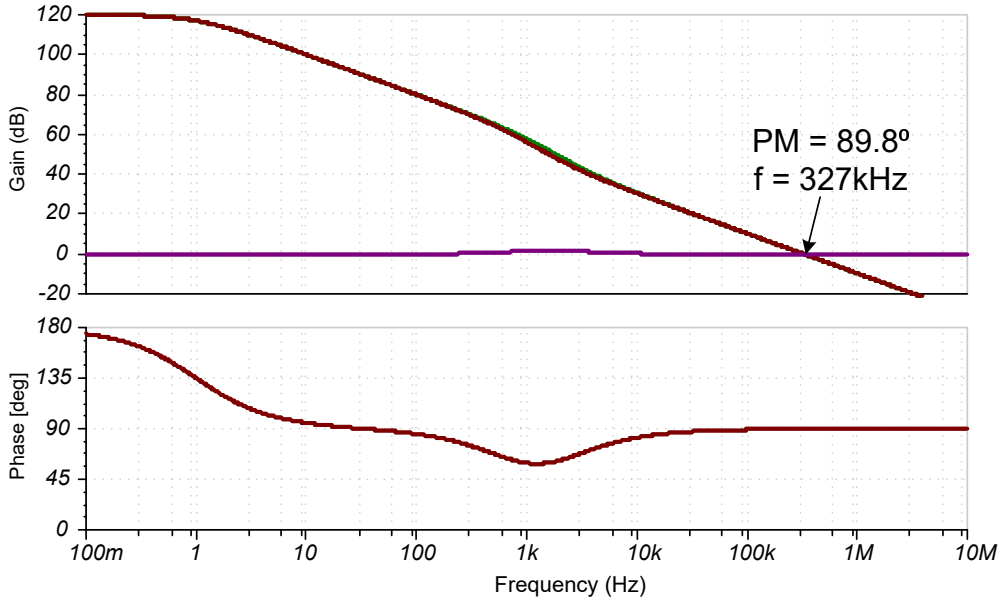


**Figure 4-31. Open-Loop AC Response for $R_{ISO}$+DFB+$R_{FX}$ Circuit With $R_{FX}$ = 0Ω**

Adding the $R_{FX}$ resistor creates a *noise-gain* type response in 1/β where the high-frequency 1/β value is equal to $1+R_{FX}/R_F$. Since the circuit has a noise-gain response, the selection of the high-frequency gain has the same requirement to intersect the $A_{OL}$ curve at 20dB/decade (see Noise Gain for Stability Compensation). An easy way to observe the noise-gain behavior is to start with a high value for $R_{FX}$, like 1MΩ, so identifying the maximum high-frequency gain the circuit can tolerate is easy. In the figure below, the 1/β curve crosses $A_{OL}$ at a level of roughly 20dB (see Figure 4-32). This circuit is very unstable as-is, but shows that the maximum allowable value for $R_{FX}$ is roughly 45kΩ (1+45k/4.99k ≅ 10V/V (or 20dB)). The pole and zero frequencies, along with the $A_{OL}$ and 1/β intersection frequency ($f_{INT}$), can be calculated using Equation 47 through Equation 49.

$$f_P = \frac{1}{2 \times \pi \times (R_{ISO} + R_O) \times C_L} = \frac{1}{2 \times \pi \times (49\Omega + 100\Omega) \times (1\mu F)} = 1.06\ \text{kHz} \quad (47)$$

$$f_Z = \frac{1}{2 \times \pi \times R_{ISO} \times C_L} = \frac{1}{2 \times \pi \times (49\Omega) \times (1\mu F)} = 3.18\ \text{kHz} \quad (48)$$

$$f_{INT} = \sqrt{f_P \times f_O} = \sqrt{(1.06\ \text{kHz}) \times (1\ \text{MHz})} = 32.56\ \text{kHz} \quad (49)$$

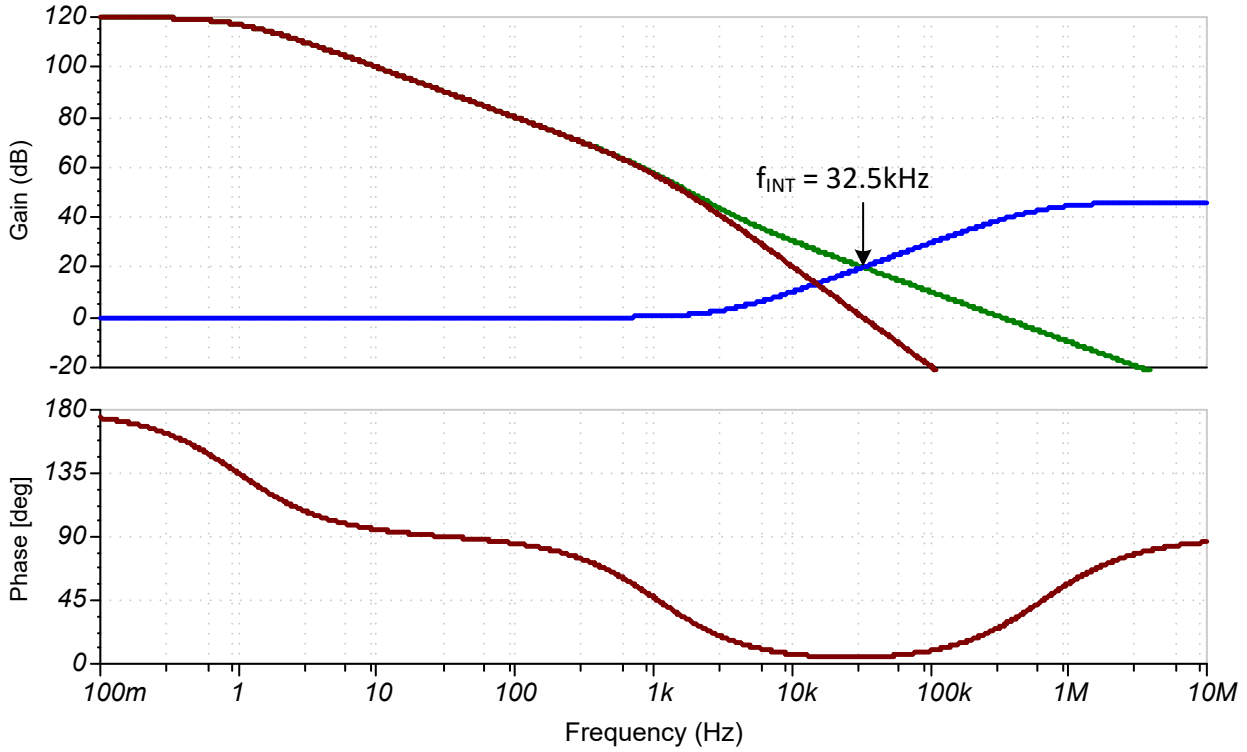


**Figure 4-32. Open-Loop Response of $R_{ISO}$+DFB+$R_{FX}$ Circuit With $R_{FX}$ = 1MΩ to Find $f_{INT}$**

The next step is to improve settling times by lowering the $C_F$ value from what was used in the $R_{ISO}$+DFB circuit. To avoid having 1/β intersect $A_{OL}$ at a 40dB rate-of-closure, back off the maximum $R_{FX}$ value by approximately 30% as calculated in Equation 50. The factor of 0.7 reduces the noise gain by 30%, which causes the noise gain curve to flatten out before the curve intersects 1/β.

$$R_{FX} = 0.7 \times \left( \frac{f_P \times f_O \times R_F}{f_Z \times \sqrt{f_P \times f_O}} - R_F \right) = 0.7 \times \left( \frac{(1.06\ \text{kHz}) \times (1\ \text{MHz}) \times (4.99\ \text{k}\Omega)}{(3.18\ \text{kHz}) \times \sqrt{(1.06\ \text{kHz}) \times (1\ \text{MHz})}} - 4.99\ \text{k}\Omega \right) = 32.32\ \text{k}\Omega \quad (50)$$

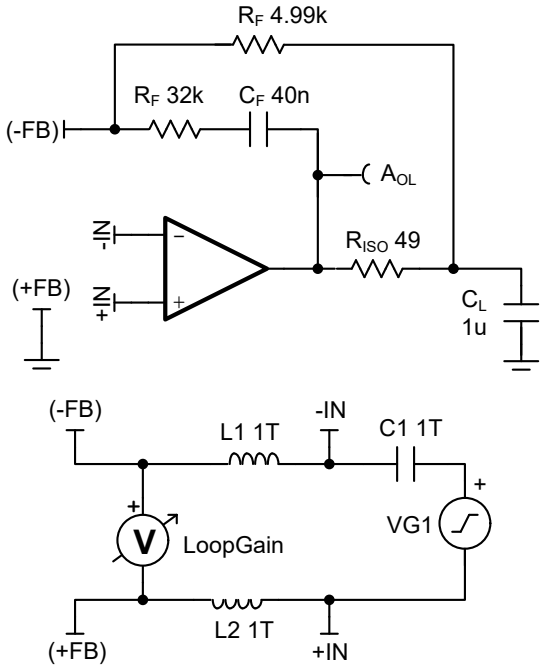


**Figure 4-33. Open-Loop Test Circuit for $R_{ISO}$+DFB+$R_{FX}$ Circuit With $R_{FX}$ = 32kΩ**

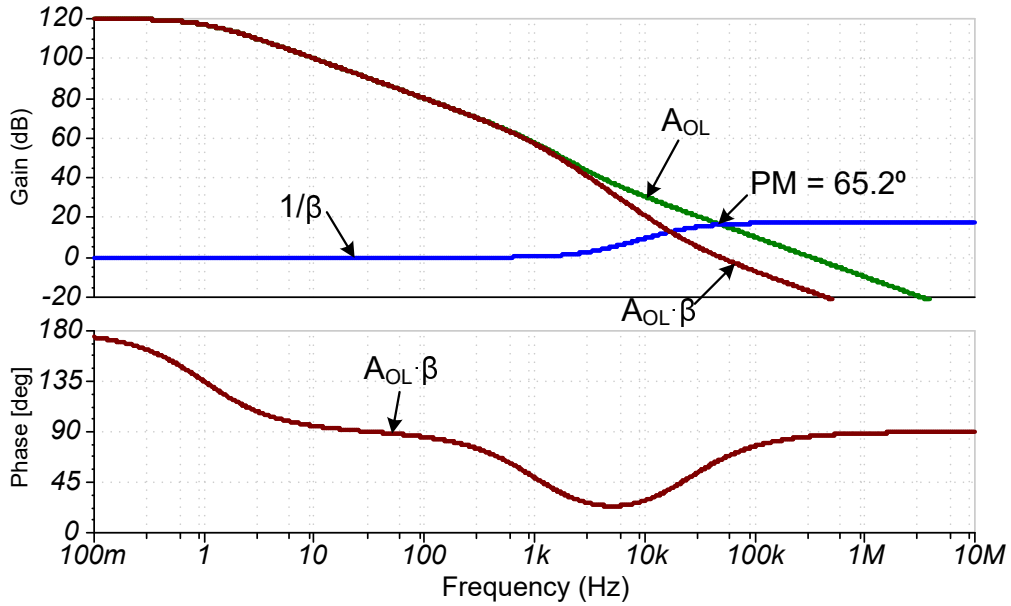


**Figure 4-34. Open-Loop AC Response for $R_{ISO}$+DFB+$R_{FX}$ Circuit With $R_{FX}$ = 32kΩ**

As mentioned earlier, the main benefit of adding $R_{FX}$ is that a much lower value of $C_F$ capacitor can be used. The easiest way to understand how $R_{FX}$ allows for a reduction in $C_F$ is to analyze the circuit by separating the two feedback paths, as was done in Dual Feedback Method. The zero frequency for FB1 only depends on $R_{ISO}$ and $C_L$, so changing $C_F$ does not affect the response of FB1 (see Equation 51). The zero frequency of FB2 ($f_{FB2}$) is set by $R_F$, $C_F$, and $R_{FX}$ (see Equation 52). Decreasing $C_F$ causes $f_{FB2}$ to shift to higher frequencies (see Equation 52 and Figure 4-35). Shifting $f_{FB2}$ too high in frequency creates the same resonance that was discussed in Dual Feedback Method. The same rough rules of 2 to 4 times lower than the frequency of the noise-gain pole apply to select the $C_F$ capacitor to avoid resonance, and so the capacitor can be selected to be roughly $C_F = 4 \times (1/(2 \times \pi \times (R_F + R_{FX}) \times f_{INA})) = 520pF$, where 510pF is the closest standard value. The open-loop plot for this capacitor shows a stable phase-margin of 71.5° (see Figure 4-37 and Figure 4-38). Figure

4-36 illustrates the resonance that can occur when the value selected for $C_F$ is too small. Notice that the gain plot shows a resonant peak in 1/β, and the phase plot shows a rapid phase shift at the same frequency.

$$f_{FB1} = \frac{1}{2 \times R_{ISO} \times C_L} = \frac{1}{2 \times (49\Omega) \times (1\mu F)} = 3.25\text{kHz} \quad (51)$$

$$f_{FB2} = \frac{1}{2 \times (R_F + R_{FX}) \times C_F} = \frac{1}{2 \times (4.99\ \text{k}\Omega + 32\ \text{k}\Omega) \times (40\text{nF})} = 107.6\text{Hz} \quad (52)$$

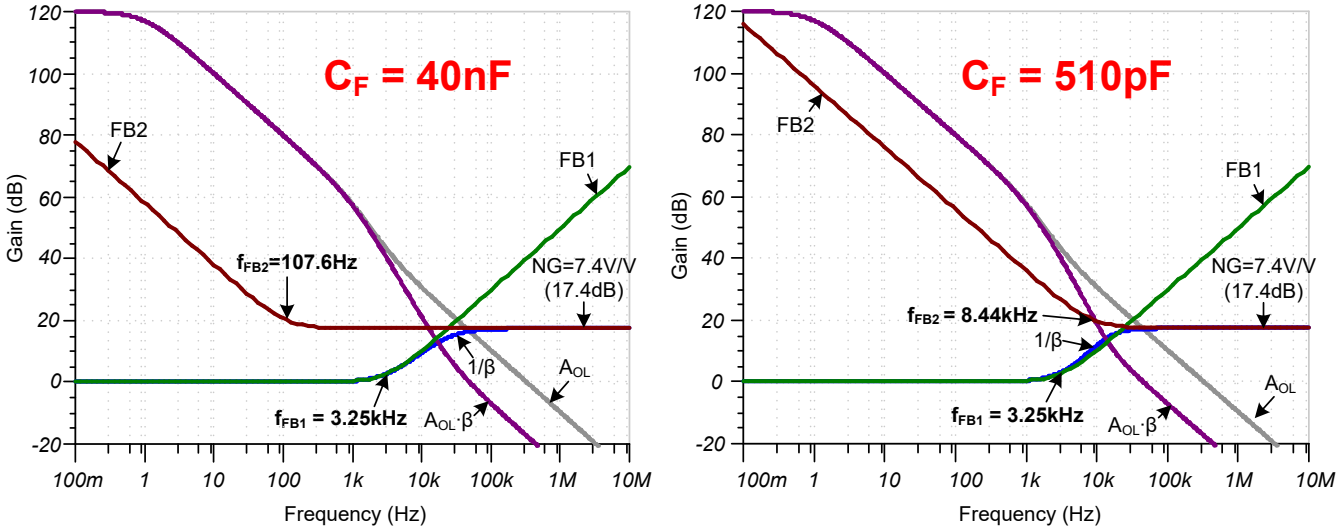


**Figure 4-35. Open-Loop AC Response of $R_{ISO}$+DFB+$R_{FX}$ for $C_F$ = 40nF and 510pF**

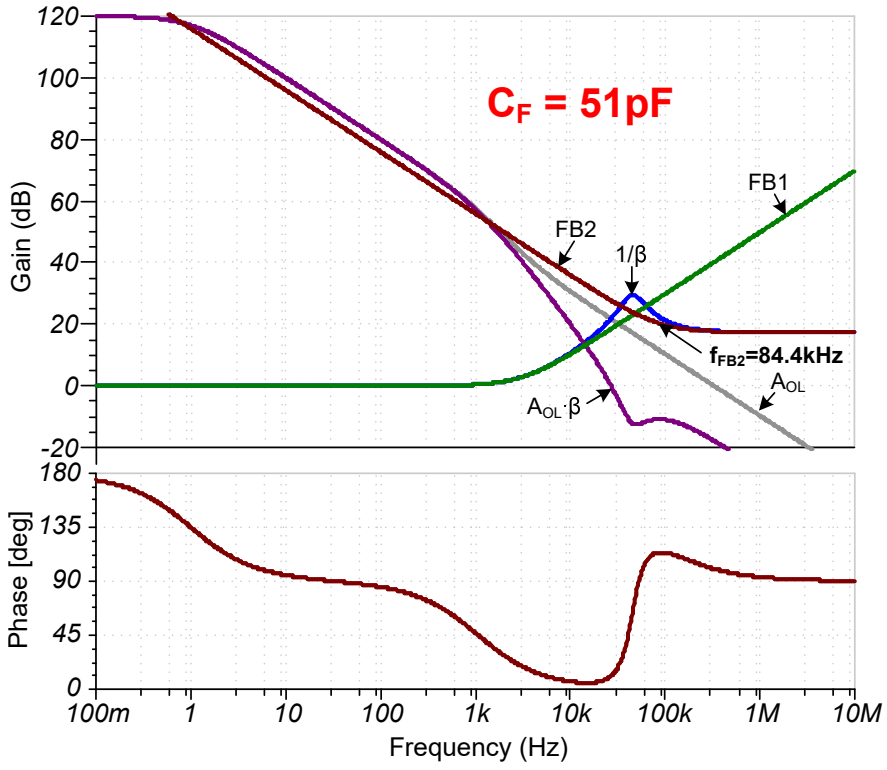


**Figure 4-36. Resonance Example Where $C_F$ is Too Small ($f_{FB2}$ is Too High)**

**Note**

**Design procedure for $R_{ISO}$+DFB+$R_{FX}$ compensation**

1. Select $R_{ISO}$ to overcompensate the circuit. $R_{ISO} \geq 0.5 \times R_O$ is a good starting point ($R_{ISO} = 0.5 \times (100\Omega) = 50\Omega$ or $49\Omega$ for standard value.
2. Select $R_F = 100 \times R_{ISO} = 4990\Omega$.
3. Select $R_{FX}$ based on $R_F$, $f_Z$, $f_O$, and $f_P$ frequencies

$$f_P = \frac{1}{2 \times \pi \times (R_{ISO} + R_O) \times C_L} = \frac{1}{2 \times \pi \times (49\Omega + 100\Omega) \times (1\mu F)} = 1.06\ \text{kHz} \quad (53)$$

$$f_Z = \frac{1}{2 \times \pi \times R_{ISO} \times C_L} = \frac{1}{2 \times \pi \times (49\Omega) \times (1\mu F)} = 3.183\text{kHz} \quad (54)$$

$$R_{FX} = 0.7 \times \left( \frac{f_P \times f_O \times R_F}{f_Z \times \sqrt{f_P \times f_O}} - R_F \right) = 0.7 \times \left( \frac{(1.06\ \text{kHz}) \times (1\ \text{MHz}) \times (4.99\ \text{k}\Omega)}{(3.18\ \text{kHz}) \times \sqrt{(1.06\ \text{kHz}) \times (1\ \text{MHz})}} - 4.99\ \text{k}\Omega \right) = 32.32\ \text{k}\Omega \quad (55)$$

4. Select $C_F$ to avoid resonance in 1/β network by setting the integrator zero 4 times lower than the $f_{INT}$ frequency.

$$f_{INT} = \sqrt{f_P \times f_O} = \sqrt{(1.06\ \text{kHz}) \times (1\ \text{MHz})} = 32.56\ \text{kHz} \quad (56)$$

$$C_F = \frac{4}{2 \times \pi \times (R_{FX} + R_F) \times f_{INT}} = \frac{4}{2 \times \pi \times (32.32\text{k}\Omega + 4.99\text{k}\Omega) \times 32.56\text{kHz}} = 524.0\text{pF} \quad (57)$$

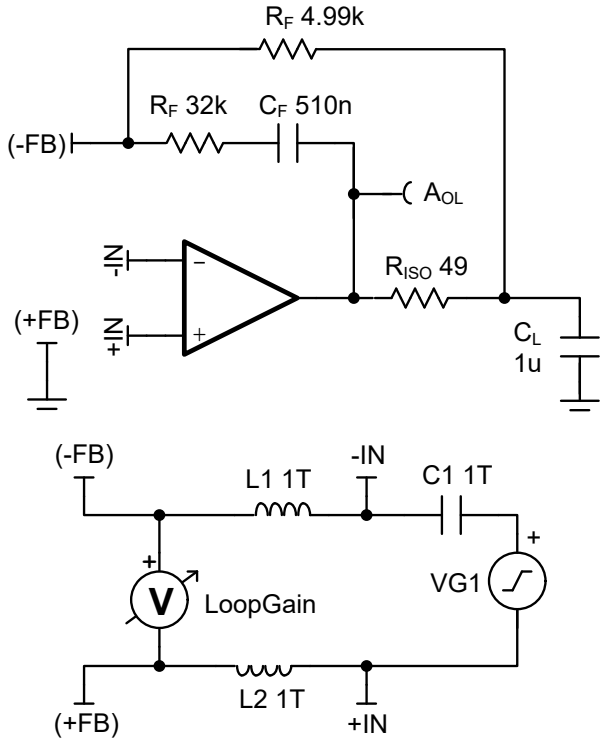


**Figure 4-37. Open-Loop Circuit for Final $R_{ISO}$+DFB+$R_{FX}$ Component Values**

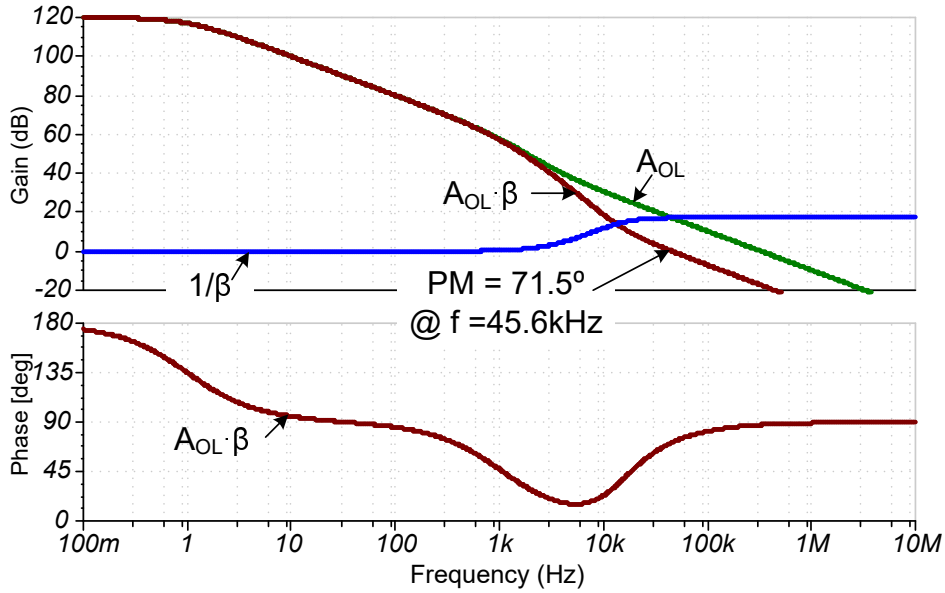


**Figure 4-38. AC Response $R_{ISO}$+DFB+$R_{FX}$ With Final Components ($R_{FX}$ = 32kΩ, $C_F$ = 520pF)**

Figure 4-39 compares the load transient results for the properly compensated $R_{ISO}$+DFB+$R_{FX}$ versus the $R_{ISO}$+DFB results. The $R_{FX}$ addition that allows the smaller value of $C_F$ enables nearly an order of magnitude faster settling.

**Note**

The input step response also settles more quickly for the $R_{FX}$ configurations (see Figure 4-41).

Finally, one disadvantage of the $R_{ISO}$+DFB+$R_{FX}$ circuit is that the circuit has higher noise than the standard $R_{ISO}$+DFB circuit for the same cap loading due to the increase in noise-gain at higher frequencies (see Figure 4-41). Noise is expected to be roughly increased by the high-frequency 1/β gain (1+$R_{FX}$/$R_F$).

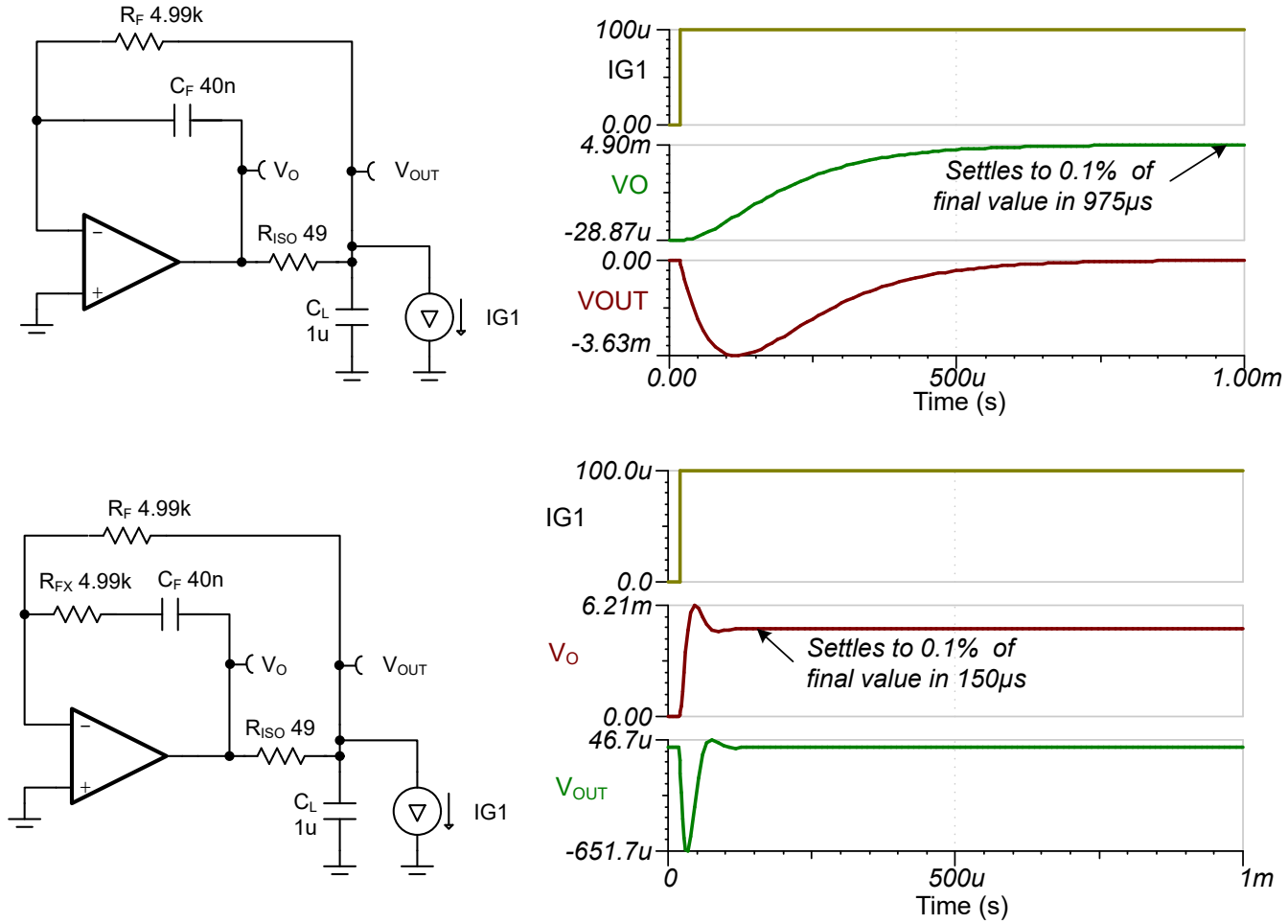


**Figure 4-39. Comparison of Load Transient Response With and Without $R_{FX}$**

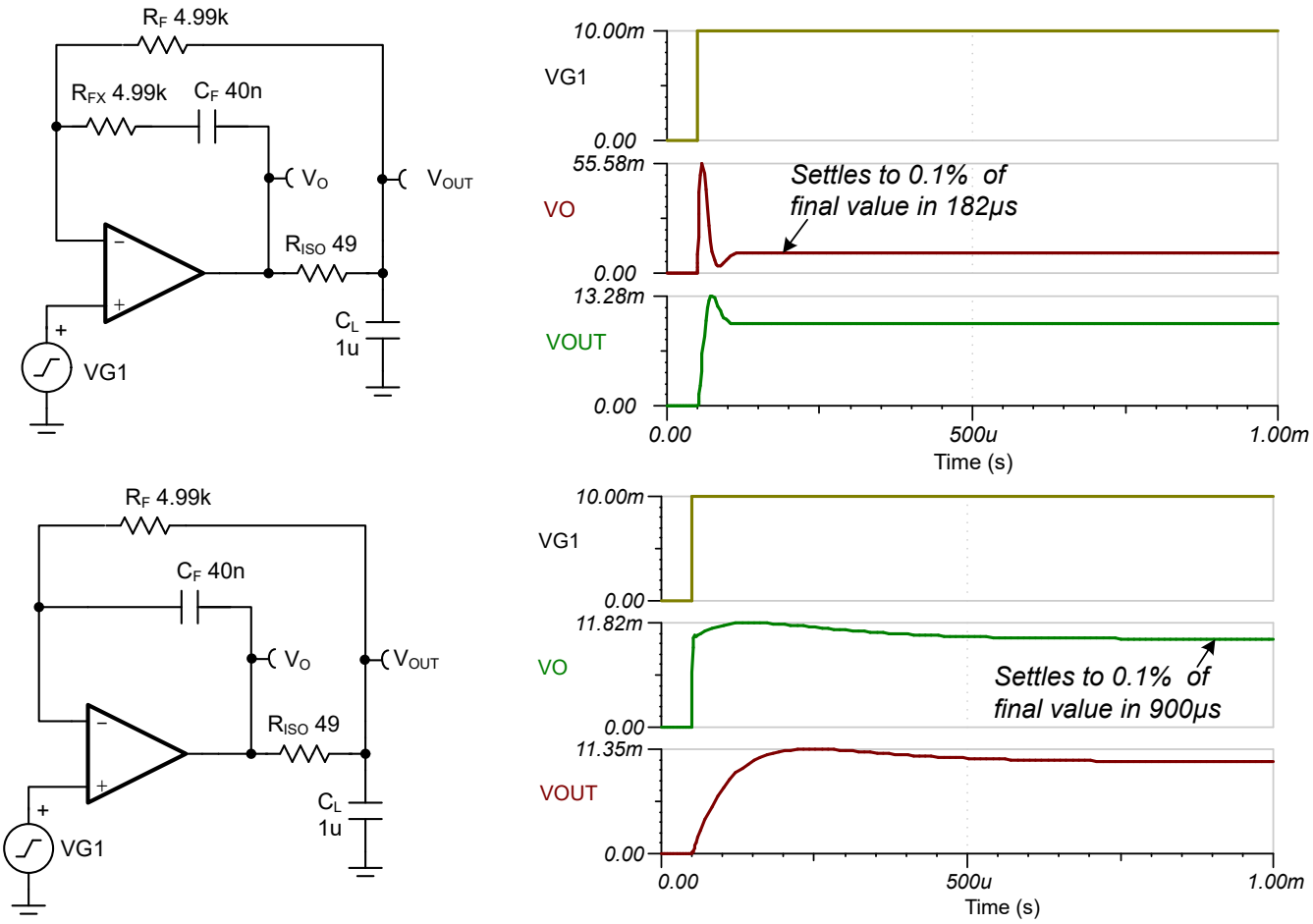


**Figure 4-40. Comparison of Input Transient Response With and Without $R_{FX}$**

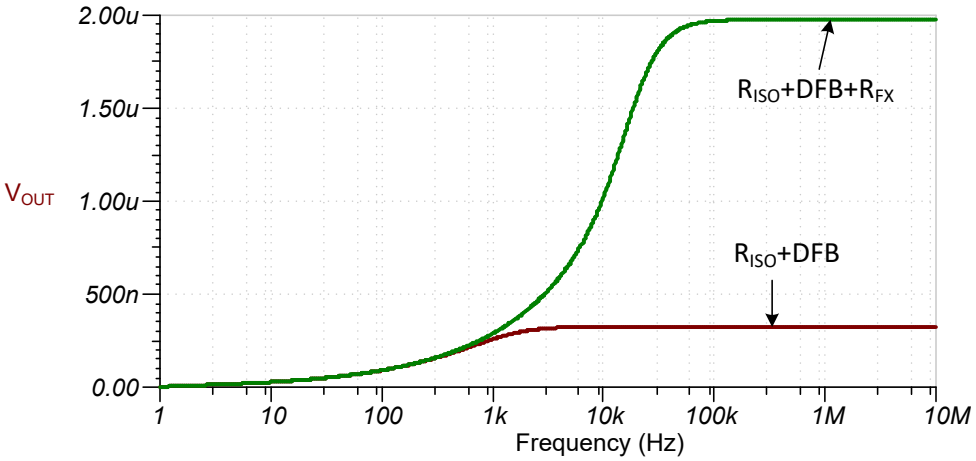


**Figure 4-41. Noise Measured at $V_{OUT}$ With and Without $R_{FX}$**

### 4.3 Snubber Circuit for Compensating Power Amplifiers and Reference Drive

In some cases, where an op amp drives a capacitive load, using an isolation resistance is not practical. One example is a power amplifier that drives a capacitor in parallel with a low-value resistive load, or other cases where the amplifier must supply larger output currents. Figure 4-42 shows an unstable power op amp driving a 50Ω load in parallel with a 10nF capacitor. This example can be stabilized with a 20Ω isolation resistance using Equation 58 (see Figure 4-43).The intended load voltage for this application is 10Vpk with a load current of 200mApk. However, the 20Ω isolation resistance significantly limits the output swing and load current. Also, the 20Ω isolation resistance dissipates 408mWpk (see Figure 4-44). The isolation resistance must be a physically large and expensive component to meet the required power rating.

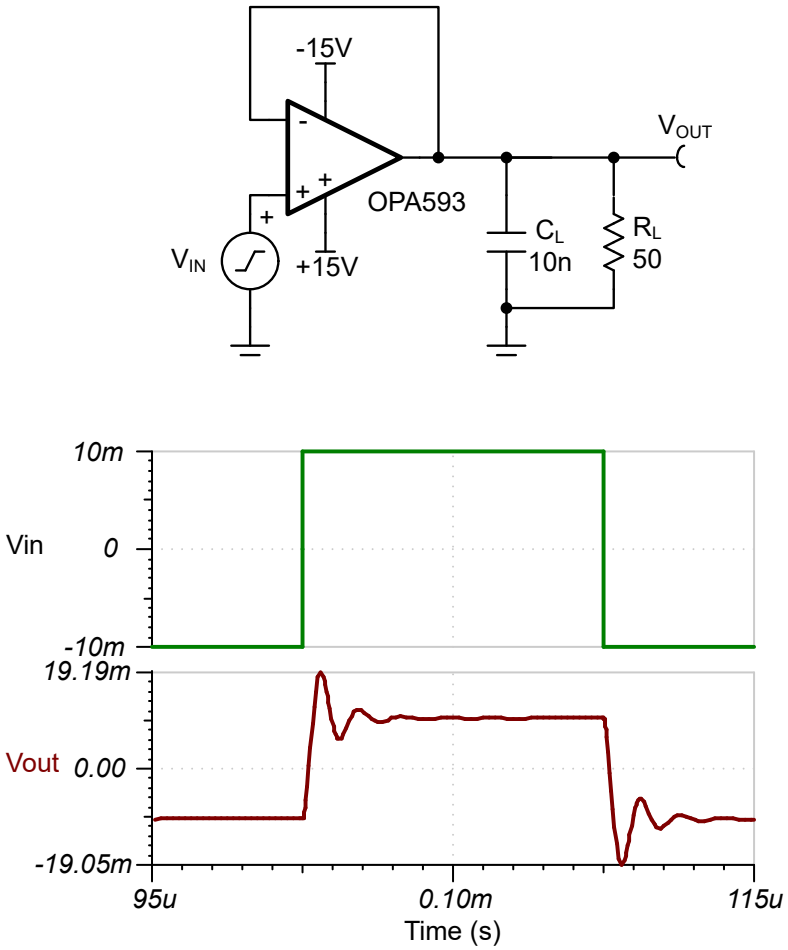


**Figure 4-42. Power Op Amp With Stability Problem (OPA593)**

$$R_{ISO} = \frac{1 + \sqrt{1 + \left(8\pi \times R_O \times C_{LOAD} \times f_{gbw}\right)}}{4\pi \times C_{LOAD} \times f_{gbw}} = \frac{1 + \sqrt{1 + (8\pi \times (230\Omega) \times (10nF) \times (10MHz))}}{4\pi \times (10nF) \times (10MHz)} = 20\Omega \quad (58)$$

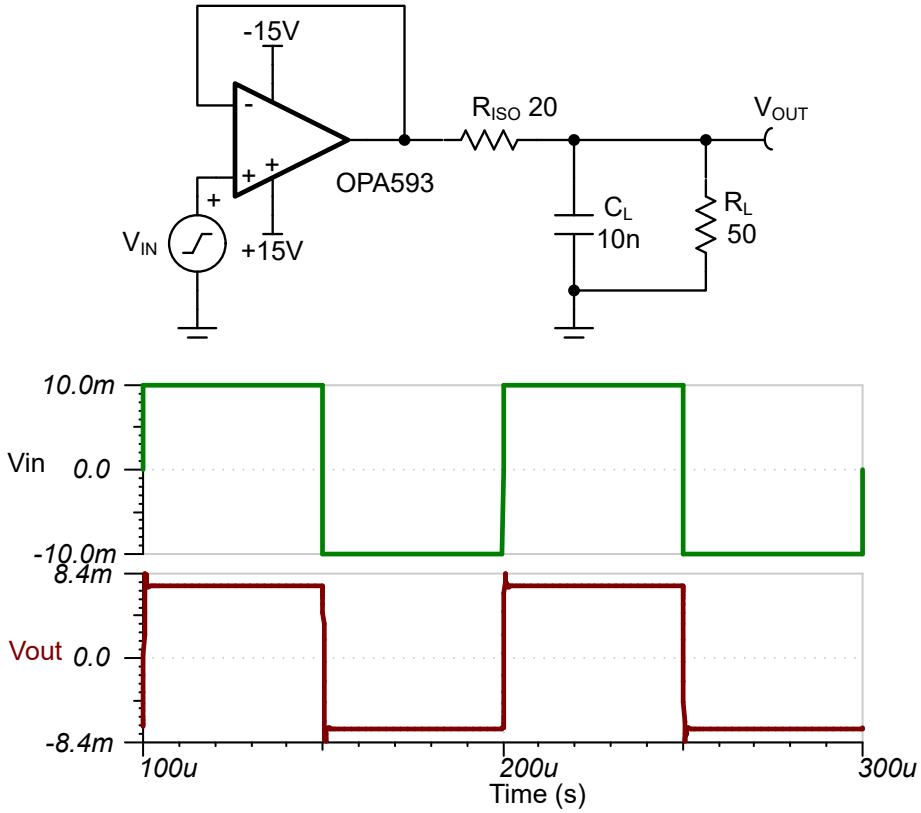


**Figure 4-43. Power Op Amp Stabilized With $R_{ISO}$ Method (OPA593)**

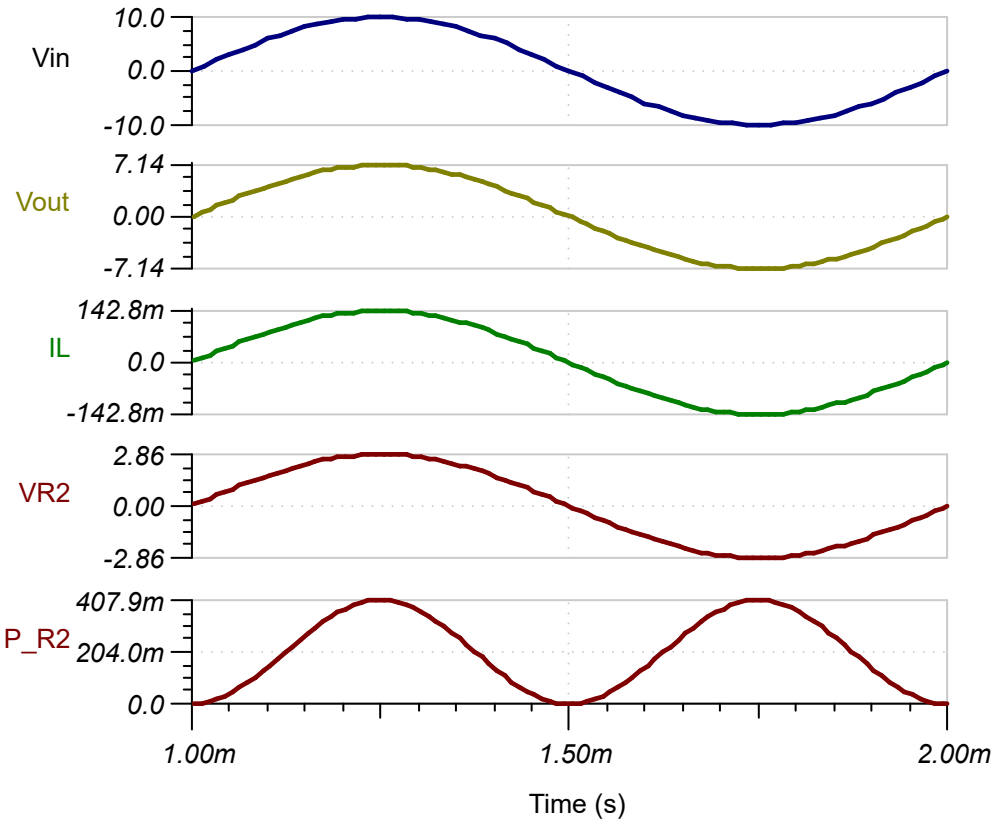


**Figure 4-44. Power Dissipated in $R_{ISO}$ and Voltage Drop Across $R_{ISO}$ (OPA593)**

A better approach for an op amp that needs to deliver significant output current is to use a snubber circuit. A snubber is a generic term for a series RC circuit that *snubs* out oscillations. In this case, the snubber stabilizes the op amp so that the op amp can drive the capacitive load without adding a series isolation resistance. Figure 4-45 shows the op amp with the snubber circuit and the associated transient response. Note that the percentage overshoot is only 10.5%. Also, there is no DC power or voltage drop as there was with the $R_{ISO}$ case. The circuit has some transient current and power dissipation in $R_{SN}$ when $C_{SN}$ charges.

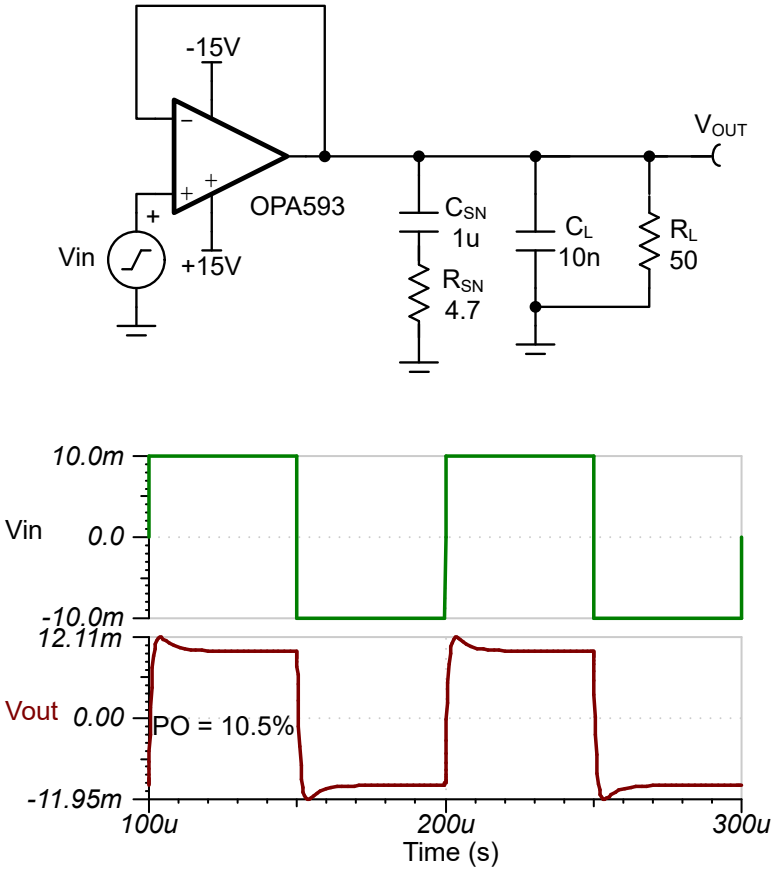


**Figure 4-45. Snubber Stabilizes OPA593 Power Op Amp**

The snubber capacitor is selected to be about 100 times larger than the capacitive load. Typically, the snubber capacitor ($C_{SN}$) is in the 1µF to 10µF range, and the snubber resistor is between the 1Ω to 100Ω range. Since $C_{SN}$ is 100 times larger than the load capacitance, $C_{SN}$ dominates the response and sets a low frequency pole at Equation 59. $R_{SN}$ sets a zero that cancels the pole according to Equation 60. To achieve stability, this zero needs to occur at a frequency below where $A_{OL}$ × β=0dB. At high frequency, the original capacitive load, $C_L$, introduces an additional pole at Equation 61. Figure 4-46 illustrates the open-loop response for the snubber circuit. Notice the rate-of-closure is 20dB/decade and the phase margin is 79.9° because the snubber zero cancels the $C_{SN}$ pole, and the original $C_L$ pole.

$$f_{P1} \cong \frac{\frac{R_O}{R_L} + 1}{2 \times \pi \times (C_{SN} + C_L) \times R_O} \quad (59)$$

$$f_Z \cong \frac{1}{2 \times \pi \times C_{SN} \times R_{SN}} \quad (60)$$

$$f_{P2} \cong \frac{1}{2 \times \pi \times C_{SN} \times R_{SN}} \quad (61)$$

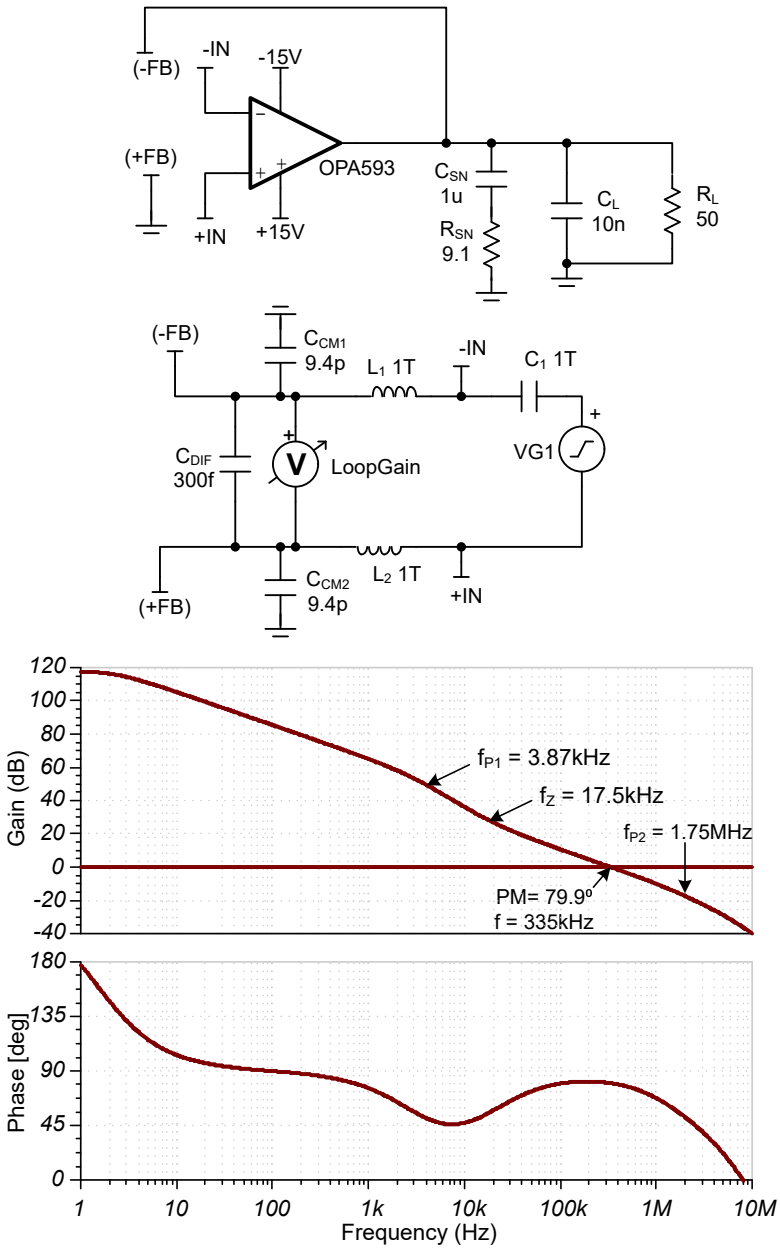


**Figure 4-46. Power Op Amp With Snubber Open-Loop Response**

Method for choosing snubber components shows how to choose $R_{SN}$ and $C_{SN}$ for the snubber circuit. In summary, a value for $C_{SN}$ is selected that is significantly larger than the capacitive load. Then, parameter stepping is used to sweep the $R_{SN}$ value and look for the best transient response (see Figure 4-47). Once $C_{SN}$ and $R_{SN}$ are selected, check the open-loop response for phase margin.

**Note**

**Method for choosing snubber components**

1. Select $C_{SN} \geq 100 \times C_L$.
2. Set $R_{SN(MIN)} = 1\Omega$.
3. The maximum $R_{SN}$ is set with:

$$R_{SN(MAX)} \cong \frac{1}{2 \times \pi \times C_{SN} \times f_Z} \quad (62)$$

4. Use SPICE parameter stepping on $R_{SN}$ with a transient small signal step. Choose $R_{SN}$ according to your desired percentage overshoot (see Figure 4-47).
   a. The the minimum $R_{SN}$ is typically unstable because the zero frequency is too high.
   b. The maximum $R_{NS}$ is typically unstable because $R_{SN}$ is creating an open-circuit for $C_{SN}$, which effectively removes $C_{SN}$ from the circuit.
   c. Using the parameter stepping you can choose the lowest overshoot. However, some overshoot gives a faster response. Keep the speed versus stability trade-offs in mind when choosing $R_{SN}$.

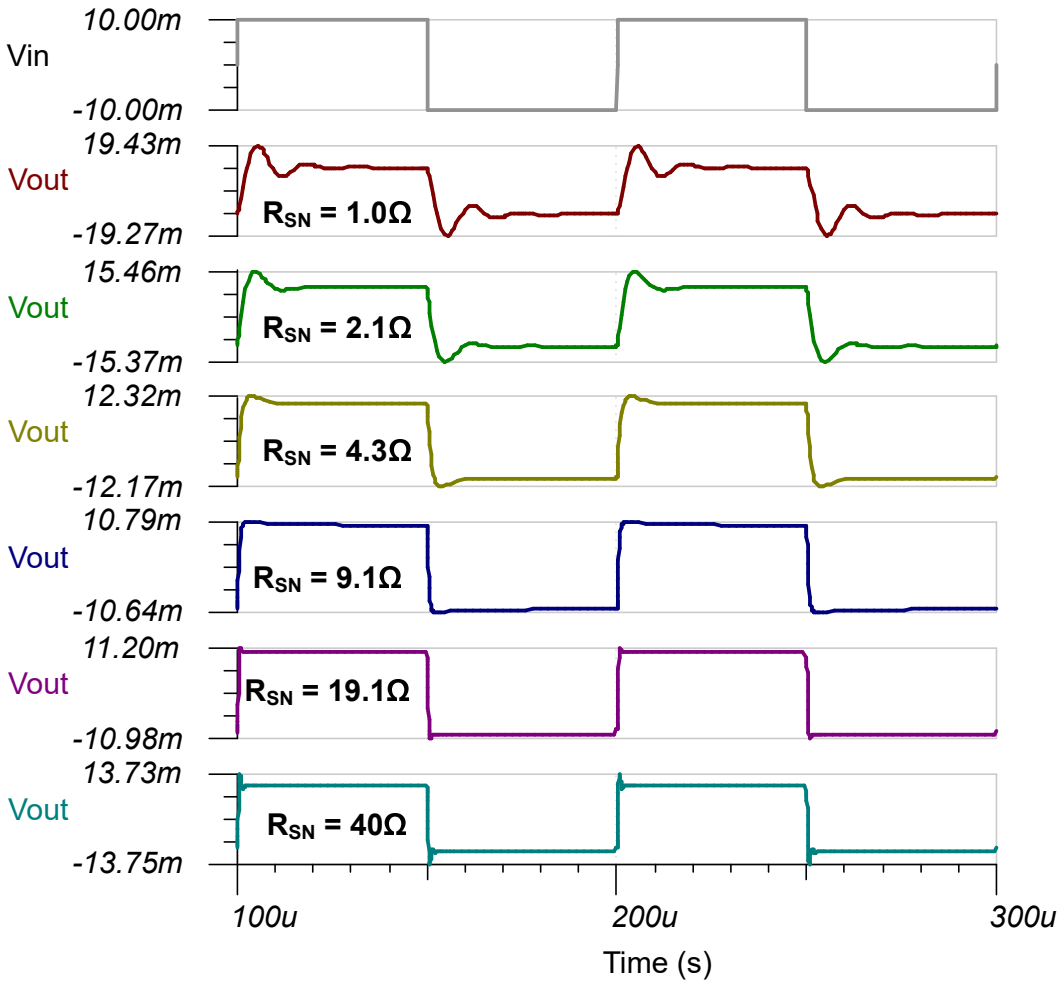


**Figure 4-47. Power Op Amp With Snubber Closed-Loop Transient Response**

Reference drivers are another common circuit that often uses the snubber compensation method. A reference driver is a circuit that buffers a voltage reference output to increase the transient response speed and the output current drive of a voltage reference. Normally, voltage reference circuits have a large filter capacitor at the output

to act as a charge reservoir as well as a noise filter. When an op amp is used as a reference buffer, engineers want the filter capacitor directly at the output of the op amp. However, doing this causes a stability problem.

Stabilizing this circuit is possible using the $R_{ISO}$ method or $R_{ISO}$-dual-feedback method, but the isolation resistance limits the output current and transient response speed. The snubber method is better as there is no resistance between the amplifier output and the load. Note that the load in this case is often the reference input to an ADC which has a rapid transient current demand during conversion. The op amp, snubber capacitor, and load capacitor all provide the transient current to the load (ADC input transient).

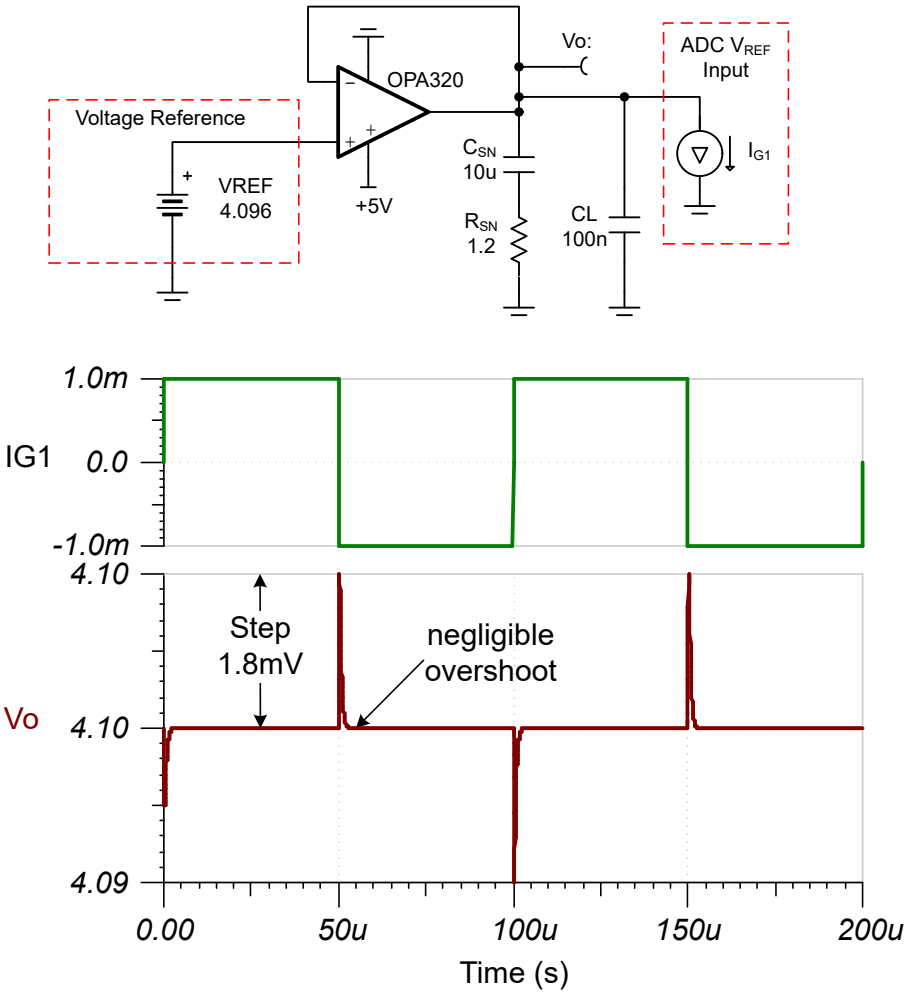


**Figure 4-48. Reference Buffer With Snubber Transient Response (OPA320)**

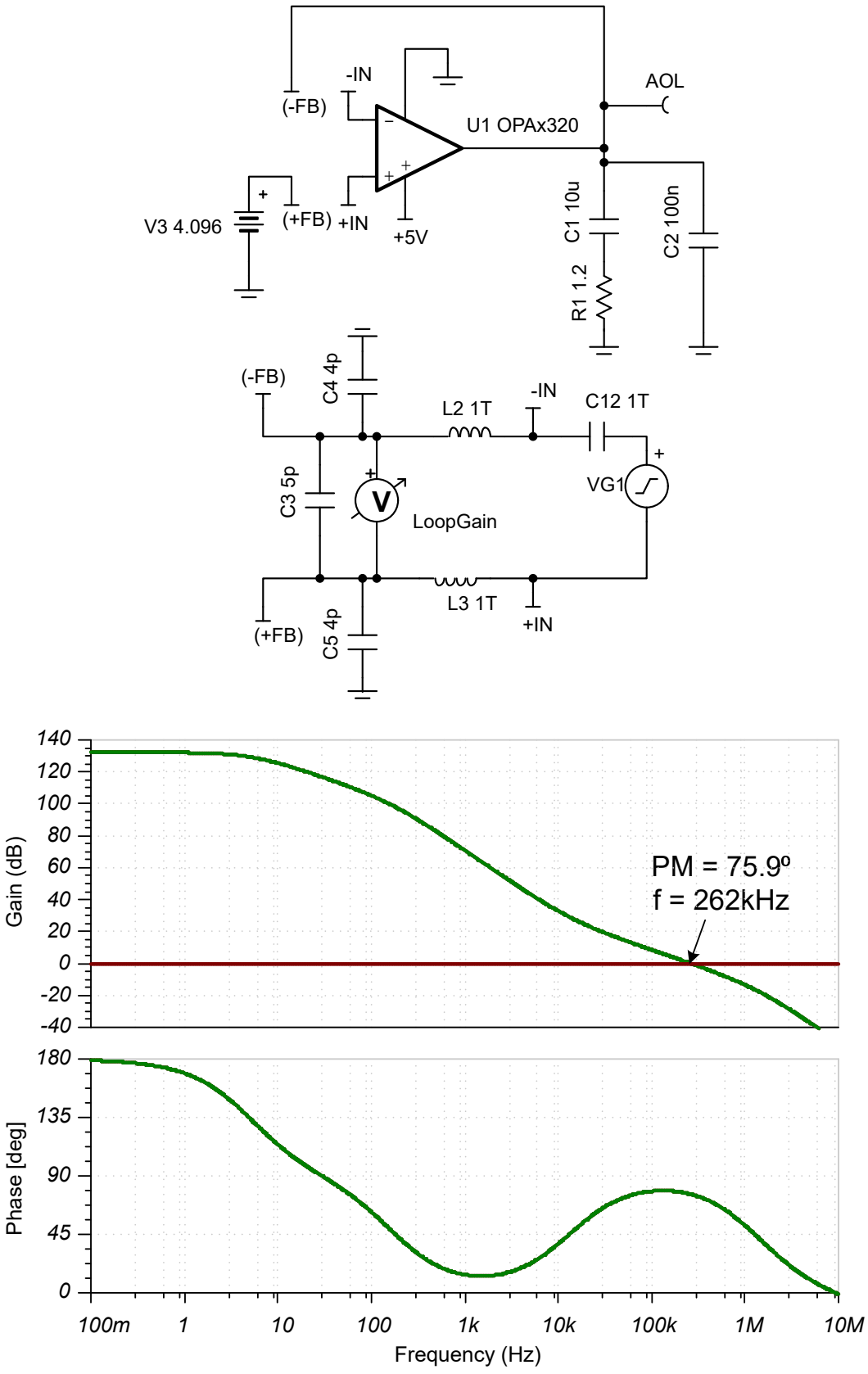


**Figure 4-49. Reference Buffer With Snubber Open-Loop Response (OPA320)**

## 4.4 Noise Gain for Stability Compensation

The term noise-gain is used to describe the gain seen by the noise source in an op amp. By definition, the noise source is on the noninverting input, so noise gain is simply the gain seen by a signal source at the noninverting input. Noise gain is equivalent to 1/β. The noise gain compensation technique increases 1/β before the noise gain intersects $A_{OL}$ to avoid the secondary pole in $A_{OL}$ from the load capacitance. Similar to snubber compensation, noise gain is useful in op amps a with high output current because there is no need for an isolation resistor. Figure 4-50 illustrates a power op amp driving a capacitive load. The load current in this example can be as high as 300mA, so using an isolation resistor is not practical. The open-loop response for this circuit is unstable with a phase margin of 29.3° (see Figure 4-51).

Figure 4-50 shows the closed-loop noise gain circuit to allow OPA593 to drive a 10nF load. Figure 4-53 shows the open-loop circuit with the noise gain compensation added and Figure 4-54 shows the response. At low frequency, the capacitor $C_G$ is essentially open and the circuit has 1/β = 0dB. At higher frequency, the capacitive reactance of $C_G$ is lower and 1/β begins to increase. Further increase in frequency eventually causes the capacitive reactance of $C_G$ to act as a short and the maximum 1/β is achieved (see Equation 67). Equation 63 shows the transfer function for 1/β, Equation 64 shows the zero frequency, and Equation 65 shows the pole frequency. The design procedure for noise gain compensation provides details for component selection. The procedure forces the final gain of 1/β to be greater than the pole from $C_L$. The procedure also sets the zero in 1/β to a lower frequency than the intersection of 1/β and $A_{OL}$ to achieve a 20dB/decade rate-of-closure. Note that as the name *Noise Gain* implies, the gain of the circuit is not flat across frequency, but has an increased gain near the unity gain bandwidth. Thus, over some frequency range the noise and signal increase due to the noise gain.

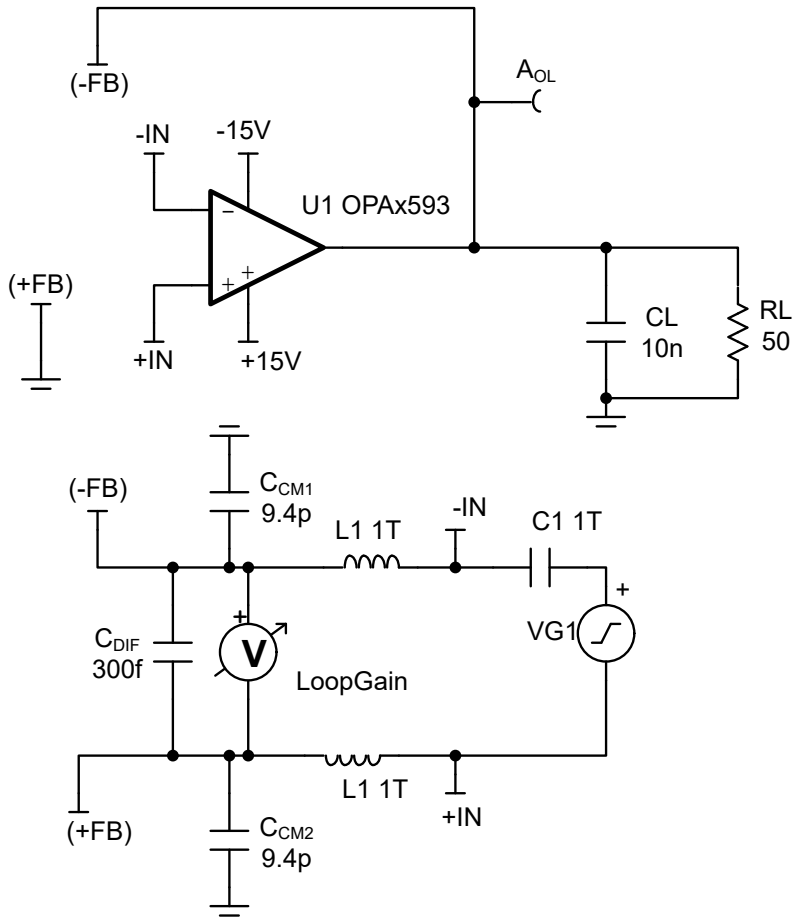


**Figure 4-50. Unstable Power Op Amp Driving a Capacitive Load**

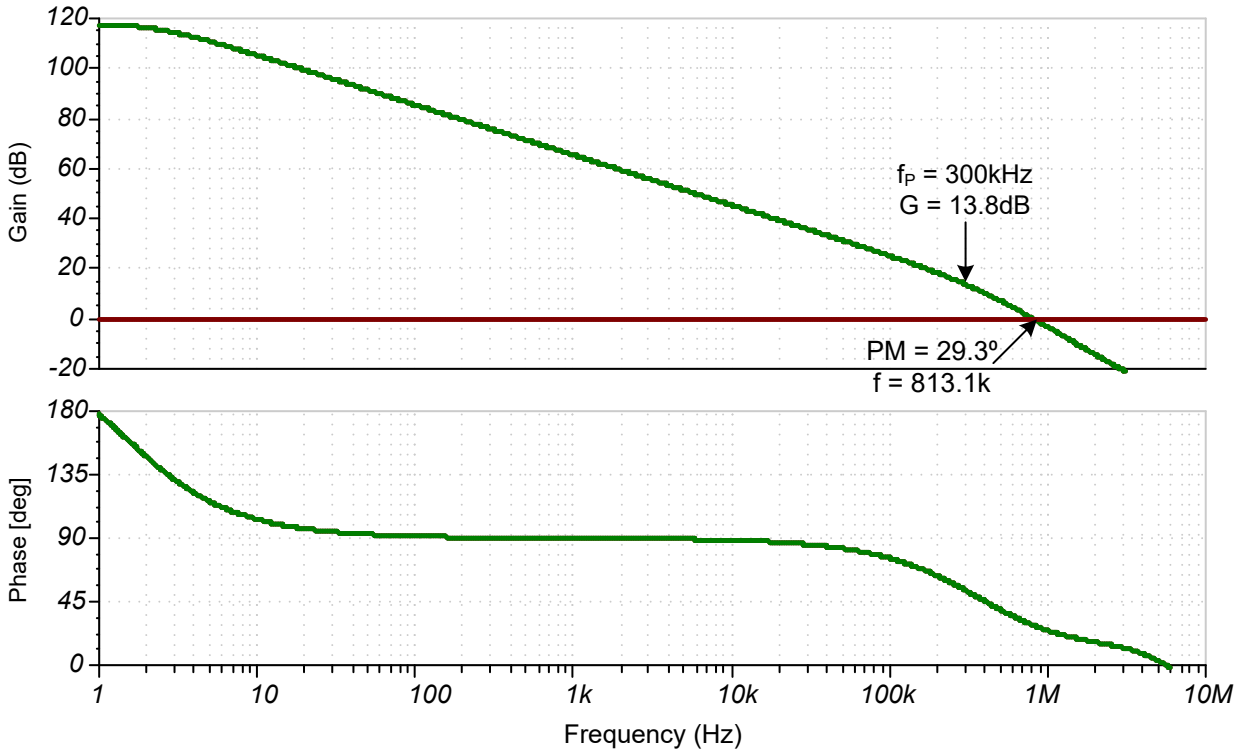


**Figure 4-51. Response for Unstable Power Op Amp Driving a Capacitive Load**

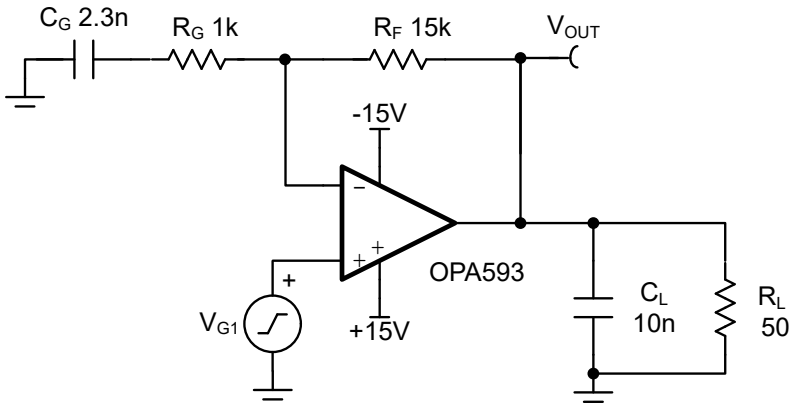


**Figure 4-52. Noise Gain Circuit to Stabilize OPA593 for $C_L$ = 10nF**

$$\frac{1}{\beta} = \frac{V_O}{V_{FB}} = \frac{(R_G + R_F) \times C_G \times s + 1}{R_G \times C_G \times s + 1} \quad (63)$$

$$f_Z = \frac{1}{2 \times \pi \times (R_G + R_F) \times C_G} \quad (64)$$

$$f_P = \frac{1}{2 \times \pi \times R_G \times C_G} \quad (65)$$

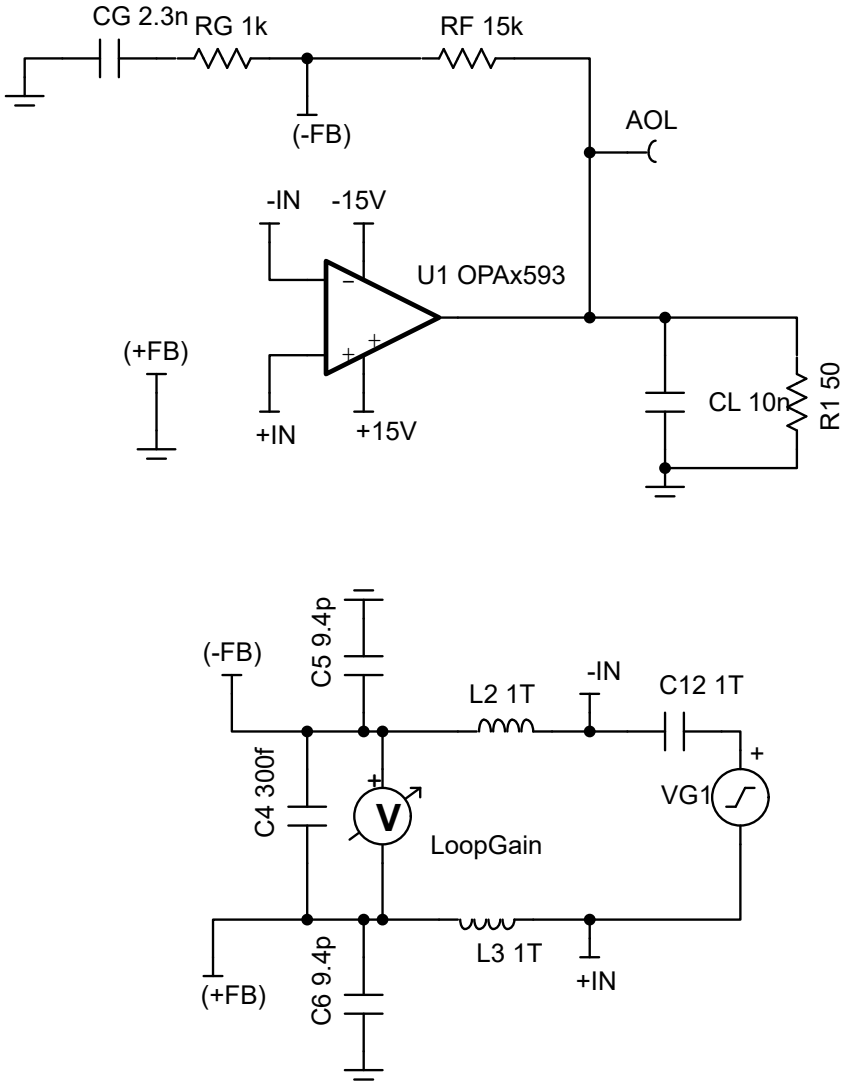


**Figure 4-53. Noise Gain Compensation Open-Loop Circuit**

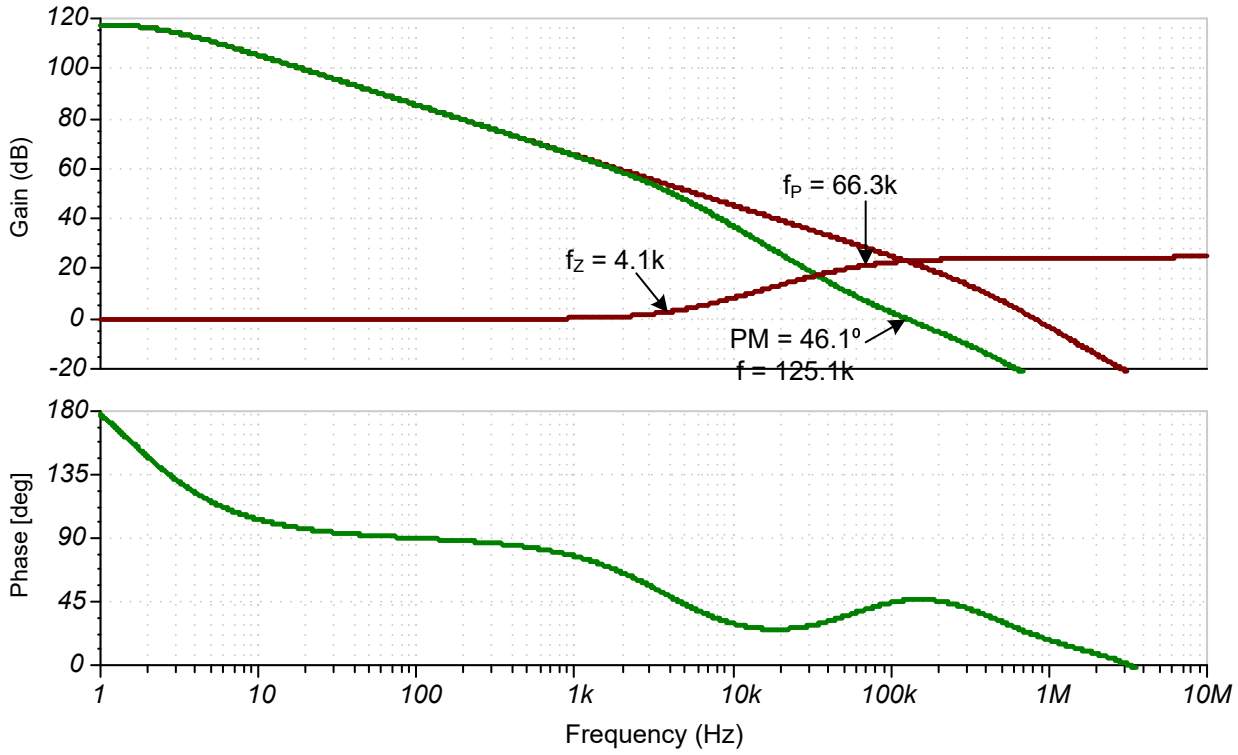


**Figure 4-54. Response of Noise Gain Compensation Open-Loop Circuit**

**Note**

Design procedure for noise gain compensation

1. Find the frequency $f_X$ and amplitude $G_X$ of the pole from the capacitive load. This can be done with SPICE cursors or using Equation 66. In this example, $Z_O$ is not flat, so using SPICE provides the better estimate ($f_X$ = 300kHz, $G_X$ = 13.8dB).
2. Set the NG ≥ $G_X$ (see Equation 67). This makes the rate-of-closure 20dB/decade where $A_{OL}$ intersects 1/β.
3. Select the capacitor $C_G$ to force the pole in 1/β to occur before 1/β intersects $A_{OL}$ using Equation 68.

$$f_X = \frac{1}{2 \times \pi \times R_O \times C_L} \quad (66)$$

$$NG = \frac{R_F}{R_G} + 1 = \frac{15k\Omega}{1k\Omega} + 1 = 16 \quad \text{or } 24.1dB \quad (67)$$

$$C_G = \frac{1}{2 \times \pi \times R_G \times f_X} = \frac{1}{2 \times \pi \times 1k\Omega \times 70kHz} = 2.3nF \quad \text{or } 2.4nF \text{ standard value} \quad (68)$$

## 4.5 Feedback Capacitor ($C_F$) Compensation for Capacitive Load

For circuits that have a gain greater than 1V/V, stabilizing capacitive loads using a feedback capacitor is potentially possible. This method is understood by considering the rate of closure rules. Figure 4-55 shows an open-loop op amp circuit in a gain of 21V/V driving a 4.7nF load. Figure 4-56 shows the response of the circuit in Figure 4-55 with and without the 82pF feedback capacitor. The capacitive load adds a second pole in the $A_{OL}$ curve, as was discussed in Section 4.1. The 1/β curve for the uncompensated response intersects $A_{OL}$ at a 40dB/decade rate-of-closure, indicating instability. The 82pF feedback capacitor adds a pole in 1/β just before 1/β intersects $A_{OL}$. Thus, the response with $C_F$ = 82pF has a rate of closure of 20dB/decade (ROC = | –40dB/decade – (–20dB/decade) | = 20dB/decade). Furthermore, the compensated circuit has a phase margin of 53.3° and the uncompensated phase margin is 31.4°.

Note that this method works because 1/β is decreasing at 20dB/decade when 1/β intersects $A_{OL}$. This can only happen for circuits with gain greater than 1V/V (or 0dB) because the feedback capacitor roll-off gains (1/β) from the DC value to 0dB. Although theoretically using this method for low gains seems possible, from a practical perspective, the method works better for gains greater than 10V/V. Lower gains potentially do not have enough gain range to create the required 20dB/decade slope to improve the rate-of-closure and stabilize the circuit.

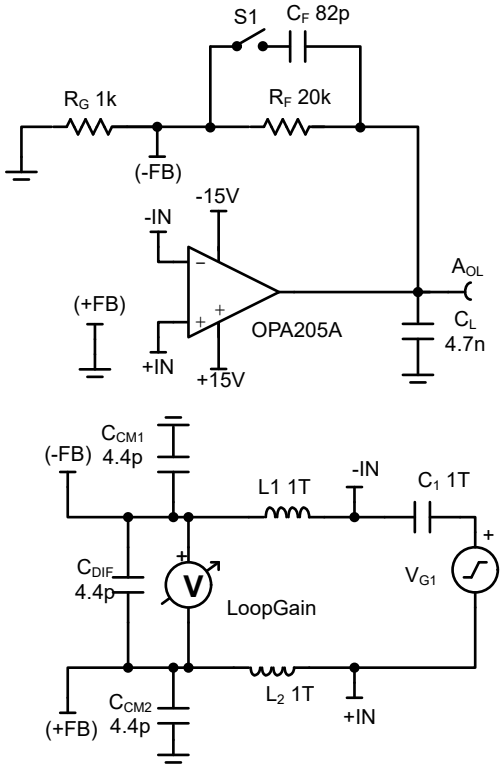


**Figure 4-55. Open-Loop Circuit for $C_F$ Compensation for Capacitive Load**

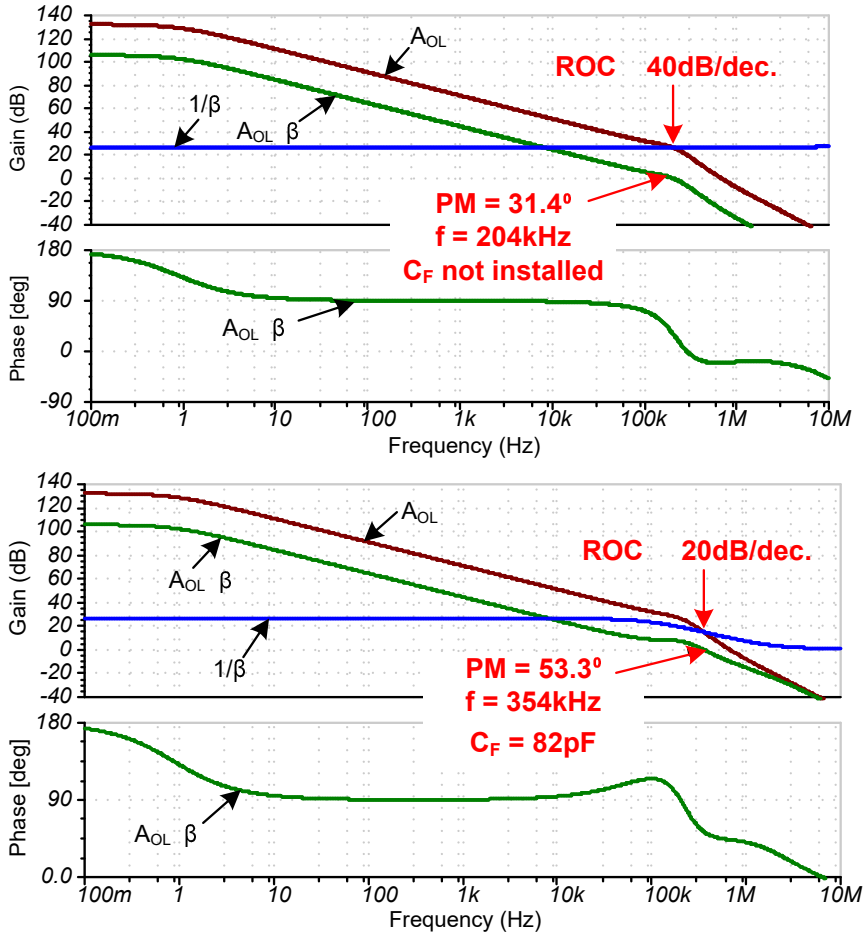


**Figure 4-56. Open-Loop Response for $C_F$ Compensation for Capacitive Load**

To stabilize the capacitive load, the feedback capacitor must position a pole in 1/β just below the point at which $A_{OL}$ intersects 1/β (rule-of-thumb: $f_P \cong f_O/2$). The key point is to make sure that after the feedback capacitor is added the rate-of-closure improves to 20dB/decade, and the resultant phase margin is better than 45°. Method for selecting $C_F$ to compensate for capacitive load summarizes the procedure for selecting compensation components.

**Note**

**Method for selecting $C_F$ to compensate for capacitive load**

1. Perform an open-loop circuit simulation for the circuit with stability issues due to capacitive load.
2. Using a cursor, find the frequency where $A_{OL}$ intersects 1/β ($f_O$ = 204kHz in this example).
3. Choose $C_F$ to add a pole to 1/β before 1/β intersects $A_{OL}$ ($f_P \cong f_O$ /2). For this example, an 82pF capacitor sets the frequency to 100kHz ( $f_O$ /2 ≅100kHz).

$$C_F = \frac{1}{2 \times \pi \times f_P \times R_F} = \frac{1}{2 \times \pi \times (100\text{kHz}) \times (20\text{k}\Omega)} \cong 79.6\text{pF} \cong 82\text{pF}\left(\text{standard value}\right)$$

In general, TI advises testing stability using multiple methods. Specifically, complete both an open-loop and closed-loop test before concluding that the circuit is stable. Typically, the results of the two methods correlate but do not exactly match the second order transient response covered in Indirect (Non-Invasive) Stability Tests. If the open-loop and closed-loop results do not correlate well, look for circuit wiring issues, or model problems. Figure 4-57 illustrates the closed-loop transient response for the same circuit tested as open-loop in Figure 4-55. The transient response proves that the feedback capacitor is an effective way to stabilize the circuit.

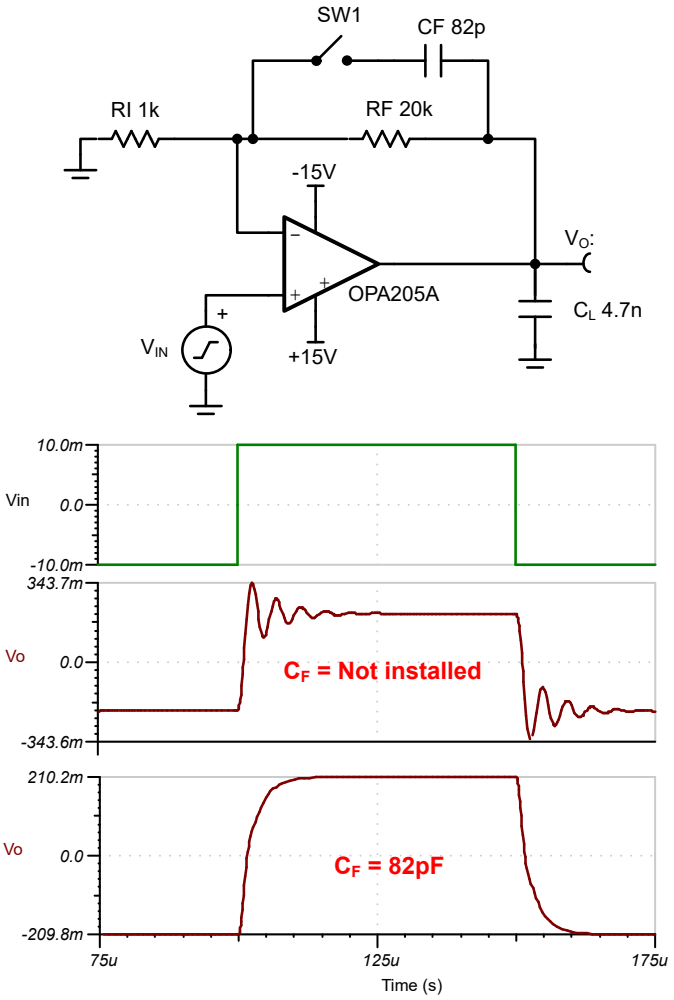


**Figure 4-57. Transient Response of $C_F$ Compensation for Capacitive Load**

## 5 Stability Corrections for Capacitance on the Inverting Node

The feedback resistor in conjunction with the op amp input capacitance creates a low pass filter that adds a delay or phase shift in the feedback path. This issue can happen because the feedback resistors are large, because the input capacitance is large, or a combination of the two. Meaning, when the total RC time constant is within the bandwidth of the circuit, the circuit has stability problems. As a result, high speed amplifiers tend to be more susceptible to this issue as the zero introduced from $R_F \times C_F$ is more likely to be inside the bandwidth of the amplifier. Figure 1-6, Figure 1-7, and Figure 1-8 illustrate three common examples of circuits with this issue.

### 5.1 Input Capacitance Instability Due to Zero in 1/β

Figure 5-1 shows the closed-loop frequency response of a circuit where the capacitance on the inverting node causes a stability problem. In this example, the capacitance on the inverting node is only 1pF, so the issue is that the feedback resistor is relatively large (1MΩ). The gain peaking and rapid phase shift of this closed-loop response is evidence of the stability problem (Gain Peaking = 23.9dB – 6dB = 17.9dB). Based on the indirect stability tests from Figure 5-4, a gain peaking of 17.9dB correlates to a phase margin of 7.3°.

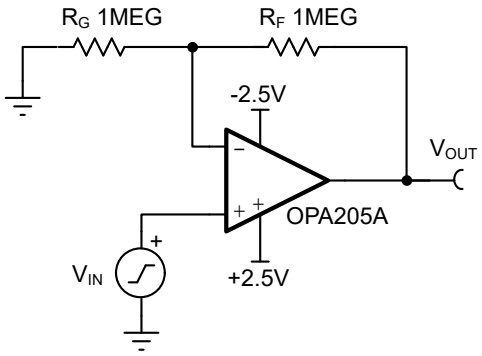


**Figure 5-1. Unstable Because of Large Feedback in Conjunction With CIN**

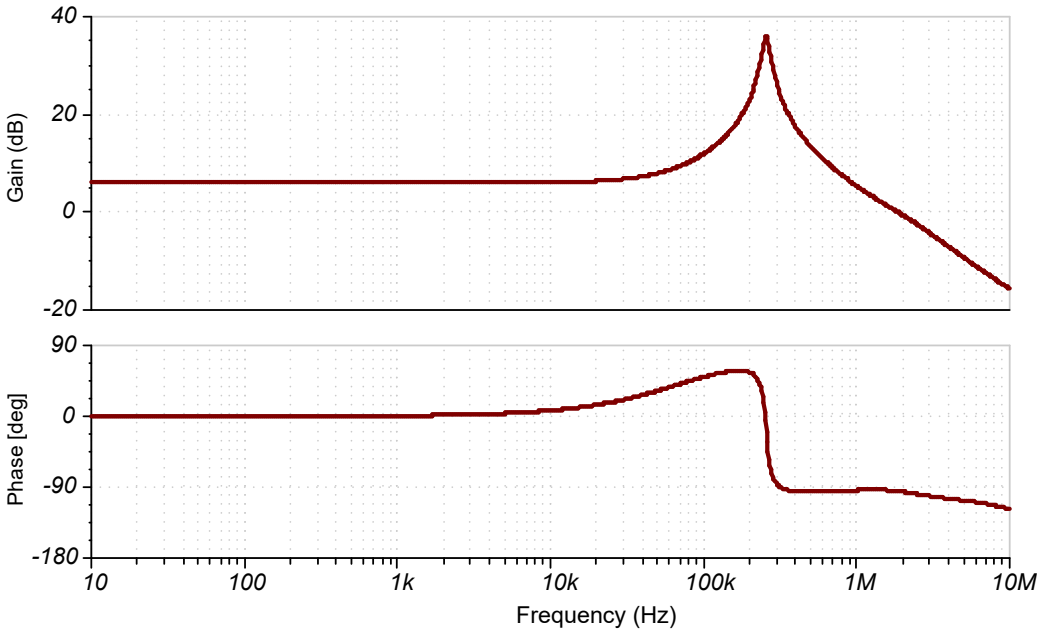


**Figure 5-2. Closed-Loop Response for OPA396 With $R_F = R_G = 1M\Omega$**

Figure 5-4 illustrates the open-loop response for the same circuit in the Figure 5-1 example. The test circuit shown in Figure 5-3 illustrates how the open-loop response was generated. Inspecting the open-loop response shows that the stability issue is caused by a zero in 1/β, which sets the rate-of-closure to be 40dB/decade. The closed-loop gain is really the same as 1/β for high values of loop gain, so think of the increase in 1/β as an increase in closed-loop gain (see Equation 12). The closed-loop gain for this op amp circuit is $G = R_F/R_G + 1$, or $G = Z_F/Z_G + 1$ considering that the feedback elements are complex impedances. In this case, $Z_G$ is $R_G \,||\, Z_{CG}$, where $Z_{CG} = 1/(j \times 2 \times \pi \times f \times C_{IN})$. Note that in Figure 5-3, $C_{IN} = C_{CM}$ is in parallel with $R_G$. In general, $C_{IN}$ also contains PCB parasitic capacitance, so the value is larger than $C_{CM}$. For high frequencies, $Z_{CG}$ becomes very small, so gain increases at higher frequencies (see Equation 69 and Equation 70). Mathematically, the closed-loop transfer function has a zero that occurs at a frequency based on the parallel combination of $R_F$ and $R_G$ and the input capacitance $C_{IN}$ (see Equation 71 and Equation 72).

$$\uparrow G_{CL} \cong \left\lceil \frac{1}{\beta} = \frac{Z_F}{Z_G \downarrow} \right. \text{ for high frequency} \tag{69}$$

$$Z_G = \left(\frac{1}{j \times 2 \times \pi \times f \times C_{IN}}\right) \Big|\Big| R_G \tag{70}$$

$$G_{CL} = \left(\frac{R_F}{R_G} + 1\right) \times \left(\frac{s}{\left(\frac{R_F + R_G}{R_F \times R_G \times C_{IN}}\right)} + 1\right) \tag{71}$$

$$f_Z = \frac{R_F + R_G}{2 \times \pi \times R_F \times R_G \times C_{IN}} \quad (72)$$

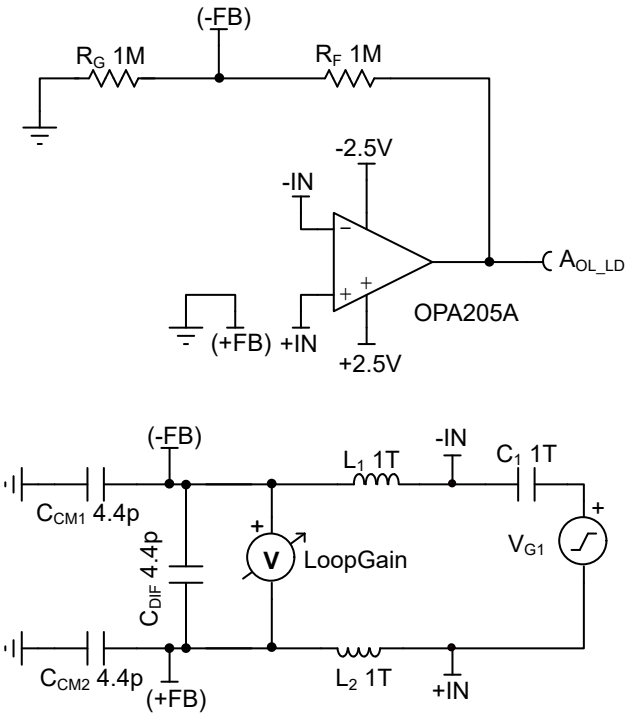


**Figure 5-3. Open-Loop Test for OPA396**

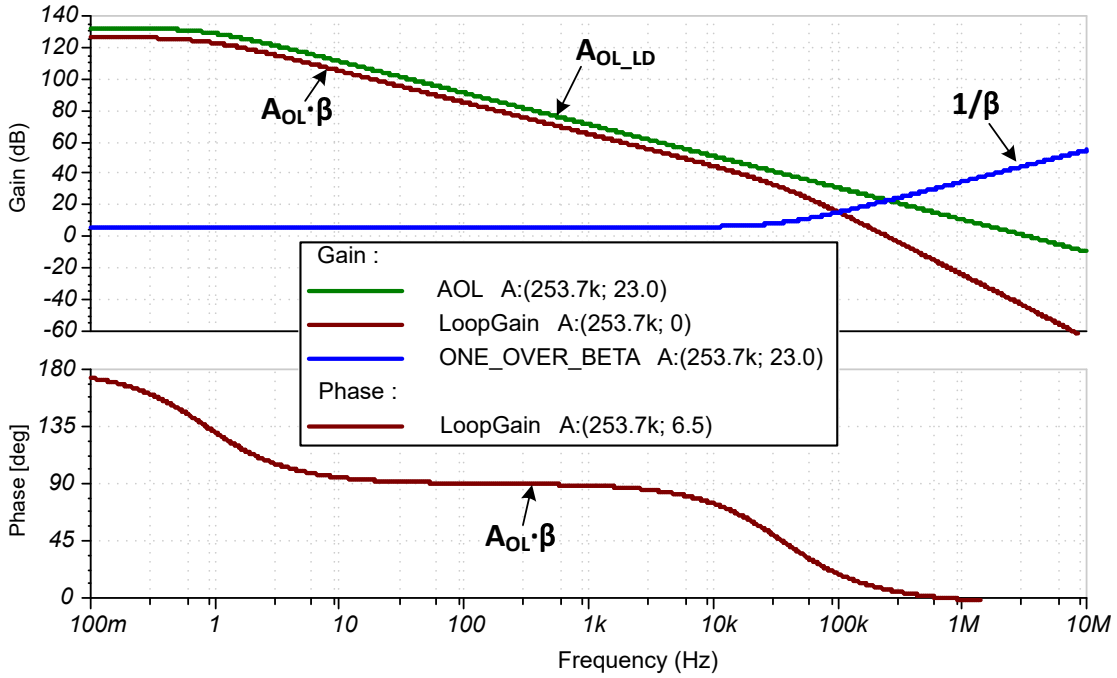


**Figure 5-4. Open-Loop Response for OPA396**

## 5.2 Feedback Capacitor Solves Stability Issue for Capacitance on the Inverting Node

In the previous section, adding a capacitor to the inverting node caused the closed-loop gain (1/β) to increase at high frequency (see Equation 69). This increase happened because $Z_G$ increased at high frequency due to a zero from the input capacitance. The way to counteract the increase in 1/β is to add a pole to cancel the zero. This counteraction can be done by adding a feedback capacitor as shown in Figure 5-5. The closed-loop gain equation for Figure 5-5 is given in Equation 73. Inspecting the gain equation, note that there is a zero at Equation 74 and a pole at Equation 75.

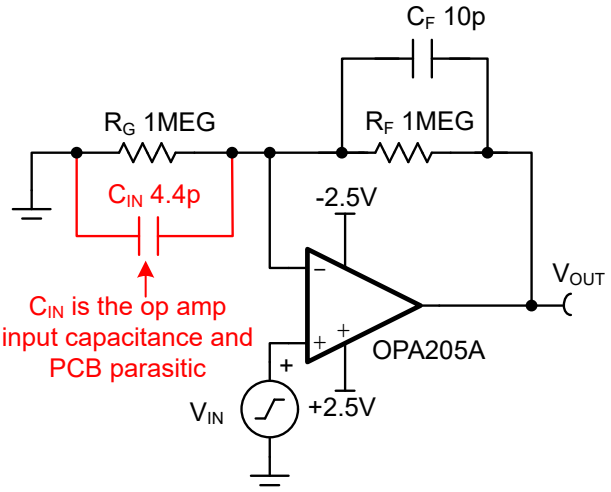


**Figure 5-5. $C_F$·$R_F$ Creates Pole that Cancels the Zero from $C_{IN}$**

$$G_{CL} = \left(\frac{R_F}{R_G} + 1\right) \times \left( \frac{\frac{s}{\left(\frac{R_F + R_G}{R_F \times R_G \times (C_{IN} + C_F)}\right)} + 1}{\frac{s}{\left(\frac{1}{R_F \times C_F}\right)} + 1} \right) \tag{73}$$

$$f_Z = \frac{R_F + R_G}{2 \times \pi \times R_F \times R_G \times (C_{IN} + C_F)} \tag{74}$$

$$f_P = \frac{1}{2 \times \pi \times R_F \times C_F} \tag{75}$$

$C_F$ creates a pole that cancels zero from $C_{IN}$. However, the value of $C_F$ must be selected properly so the $R_F||C_F$ pole provides a return phase margin greater than 45°. Figure 5-6 shows the open-loop response of a circuit with a zero in 1/β due to capacitance on the inverting amplifier node. Figure 5-7 zooms in on the area where 1/β intersects $A_{OL}$, and shows the effect that different values of $C_F$ have on the pole placement and stability. The unstable case in Figure 5-7 sets the pole after 1/β intersects $A_{OL}$ so that the rate of closure is 40dB/decade. The minimum value of $C_F$ that stabilizes the circuit sets the pole directly on the intersection of 1/β intersects $A_{OL}$. The bottom left case in Figure 5-7 illustrates what happens when $C_F$ is increased beyond the minimum value. The pole frequency is moved to a lower frequency, so that the circuit has better phase margin. In the bottom left case $f_P > f_Z$, the zero causes an increase in 1/β near the intersection of $A_{OL}$. The increase in 1/β is sometimes called noise gain and causes an increase in total output noise. The bottom right case in Figure 5-7 illustrates what happens when $f_P < f_Z$. In this case, the pole causes the gain to decrease to 0dB or 1V/V. The gain decreases to 0dB because the capacitive reactance of $C_F$ shorts out the feedback network so that the circuit becomes a unity gain follower. This circuit has the advantage of lower noise but the bandwidth is more limited.

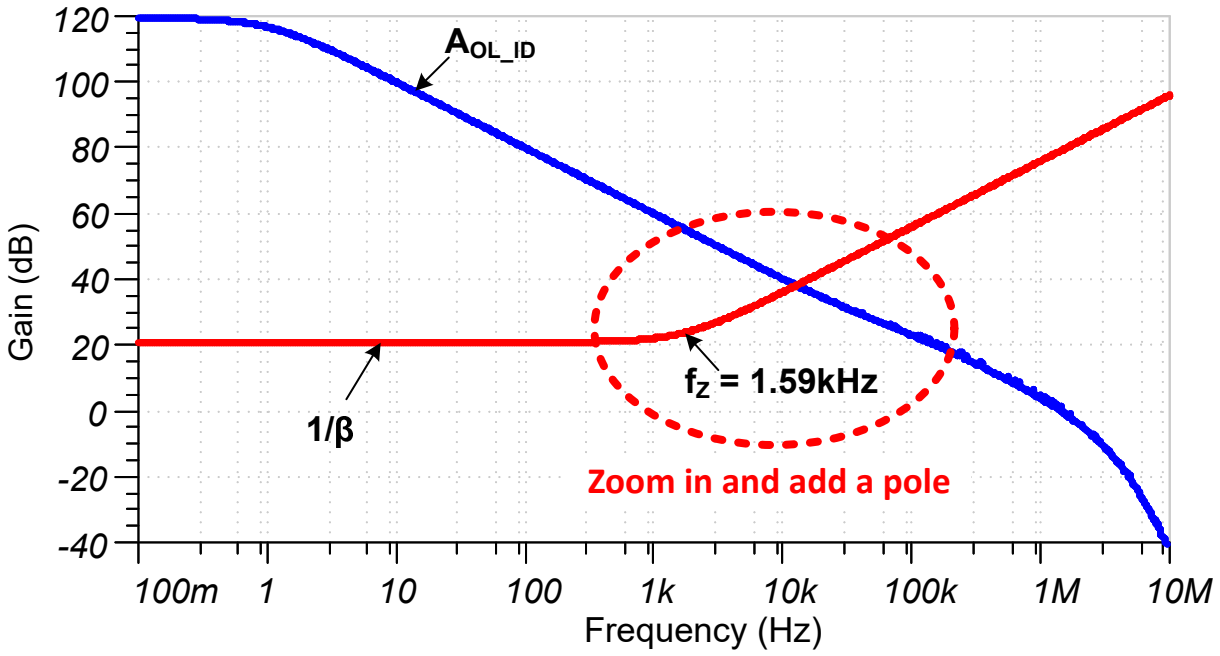


**Figure 5-6. Investigate the Impact of a Pole in 1/β in the Region Near the Intersection of $A_{OL}$ and 1/β**

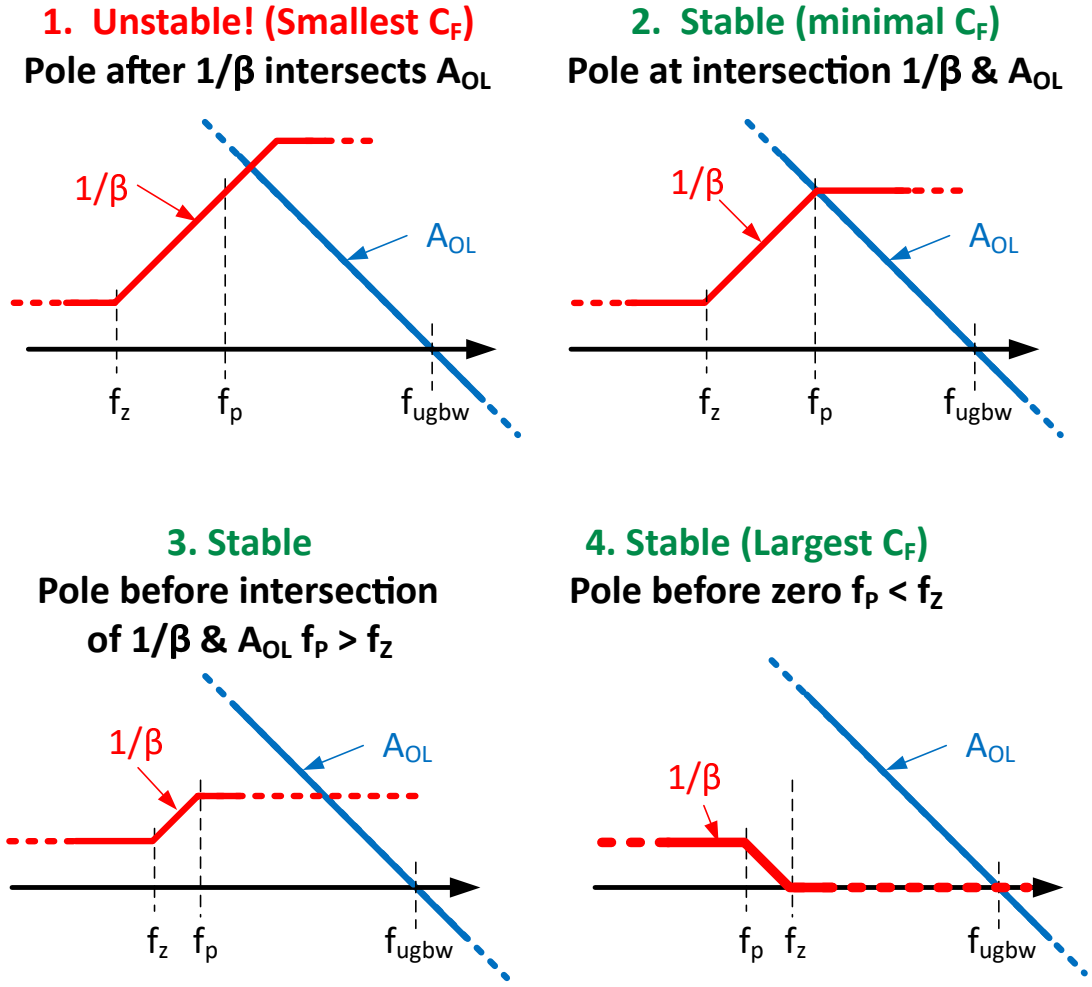


**Figure 5-7. Pole Placement Impact on Stability for Circuit With Zero in 1/β**

## 5.3 Minimum, Balanced, and Maximum Feedback Capacitance

Figure 5-8 shows a circuit with a large capacitance on the inverting node from the TVS diode between the inputs. The circuit stability issue is corrected by using the smallest possible feedback capacitor for stability. The capacitor value was found using Equation 76, and the pole frequency can be found with Equation 77. Generally, to improve the robustness of the design rounding this capacitor up the nearest standard value or higher is advisable. The minimum feedback capacitance for stability places a zero directly on the intersection of $A_{OL}$ and 1/β to set the rate-of-closure to 20dB/dec (see Figure 5-9).

$$C_{F(min)} = \sqrt{\frac{C_{IN}}{2 \times \pi \times R_F \times f_{UGBW}}} = \sqrt{\frac{1nF}{2 \times \pi \times (1M\Omega)(1MHz)}} = 12.6pF \quad (76)$$

$$f_P = \frac{1}{2 \times \pi \times C_F \times R_F} = \frac{1}{2 \times \pi \times (12.6pF)(1MHz)} = 12.6kHz \quad (77)$$

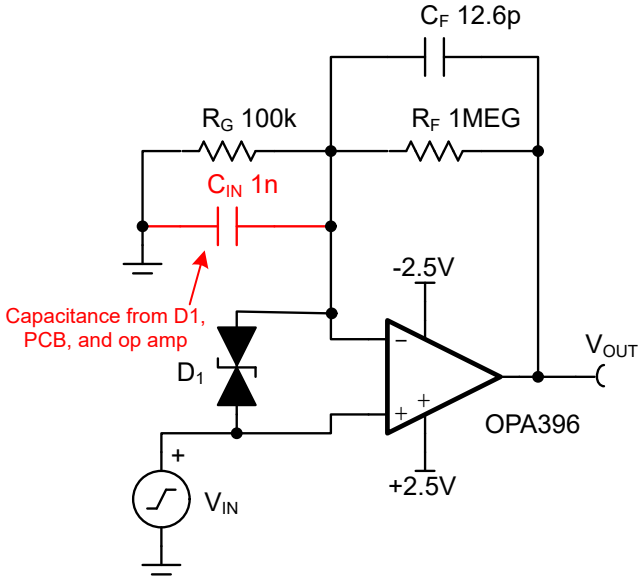


**Figure 5-8. Minimum CF for Stabilizing Capacitance on the Inverting Node**

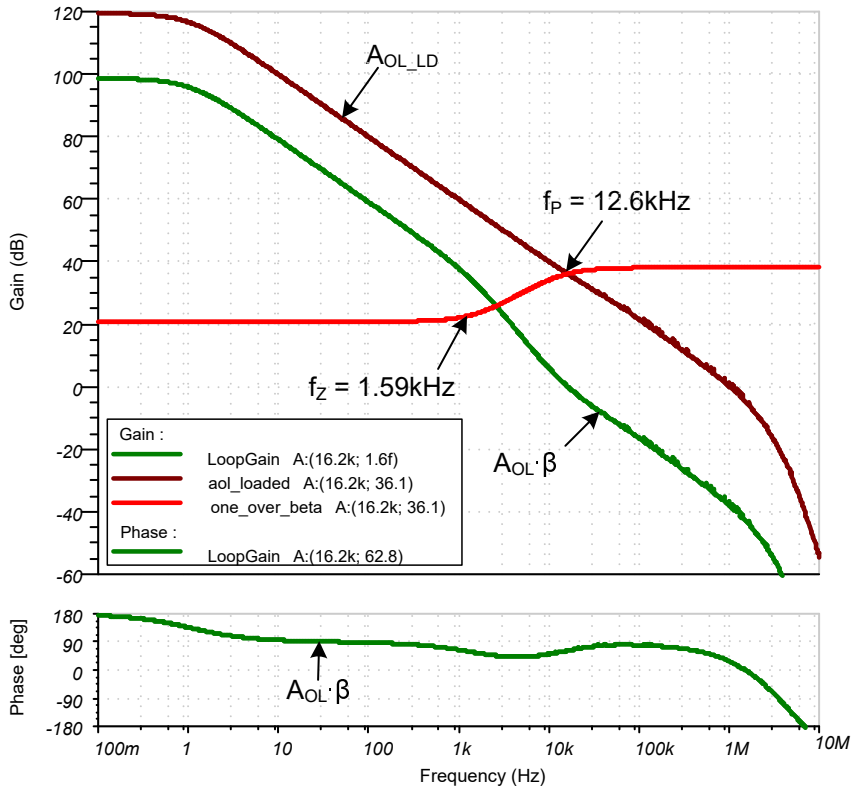


**Figure 5-9. Open-Loop Response Using Minimum $C_F$ for Stability**

Figure 5-8 shows the case where the feedback capacitor used to stabilize the circuit is selected so that the RC time constant on the feedback and inverting node are equal ($R_G \times C_{IN} = R_F \times C_F$). For this balanced case, the value of $C_F$ can be selected using Equation 76. Using the balanced method, the pole from the feedback capacitor is placed directly on the zero from the input capacitor so that 1/β looks relatively flat (see Figure 5-9). The balanced approach is often used because the approach is easy to select the feedback capacitor, and provides a robust option. The bandwidth of the balanced approach is lower than the minimum $C_F$ method, so the noise is also lower.

$$C_F = \frac{R_{IN} \times C_{IN}}{R_F} = \frac{(100k\Omega)(1nF)}{(1M\Omega)} = 100pF \tag{78}$$

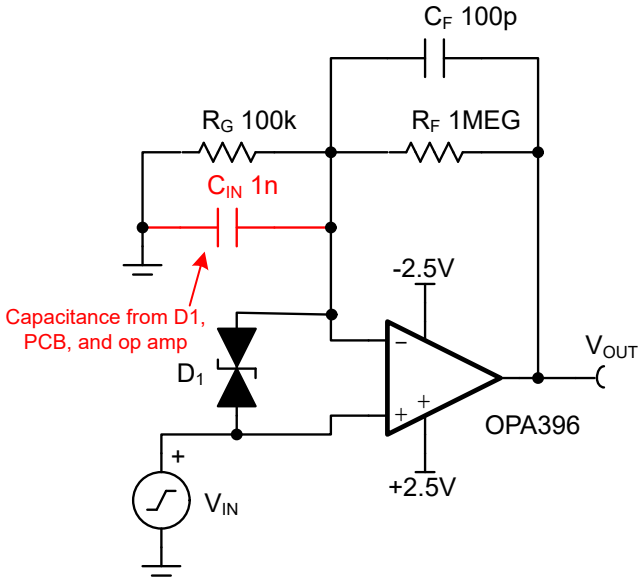


**Figure 5-10. Balanced $C_F$ for Stabilizing Capacitance on the Inverting Node**

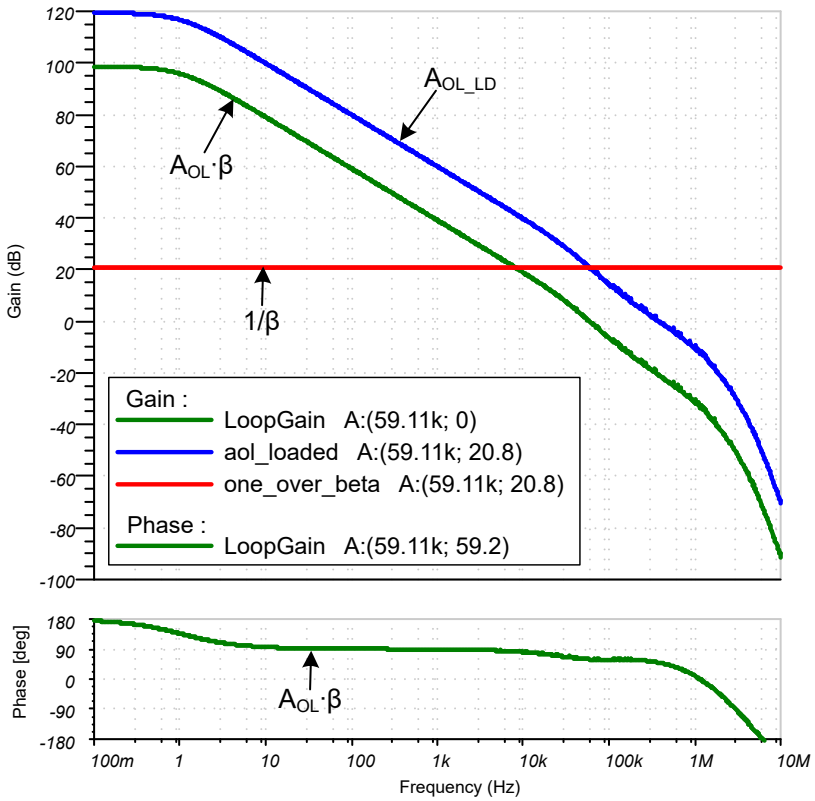


**Figure 5-11. Open-Loop Response Using Balanced CF for Stability**

Figure 5-12 shows the circuit where a large feedback capacitor is selected so that $f_P < f_Z$ and Figure 5-13 shows the open-loop response. Increasing the feedback capacitor beyond the value used in the balanced approach further reduces bandwidth and noise. The feedback capacitor for this case can be selected based on the bandwidth requirement (see Equation 79). However, selecting a value for $C_F$ that is too large and causes stability issues is possible. The feedback capacitor in series with the input capacitance creates a capacitive load for the op amp. In general, series capacitors add according to Equation 80, and for this example the total is calculated as Equation 81. If $C_F$ and $C_{IN}$ are large enough, the total capacitive load can cause instability. For the circuit in Figure 5-12, the phase margin is 42.8°, whereas the balanced case had a phase margin of 59.2°, so clearly the large feedback capacitor has degraded stability. For circuits with small $C_{IN}$, the value $C_F$ can be generally increased without stability concerns because the total series capacitance is small.

$$f_P\left(500\text{pF}\right) = \frac{1}{2 \times \pi \times R_F \times C_F} = 318\text{Hz} \tag{79}$$

$$C_{TOTAL} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \ldots + \frac{1}{C_N}} \tag{80}$$

$$C_{TOTAL} = \frac{1}{\frac{1}{1\text{nF}} + \frac{1}{500\text{pF}}} = 333\text{pF} \tag{81}$$

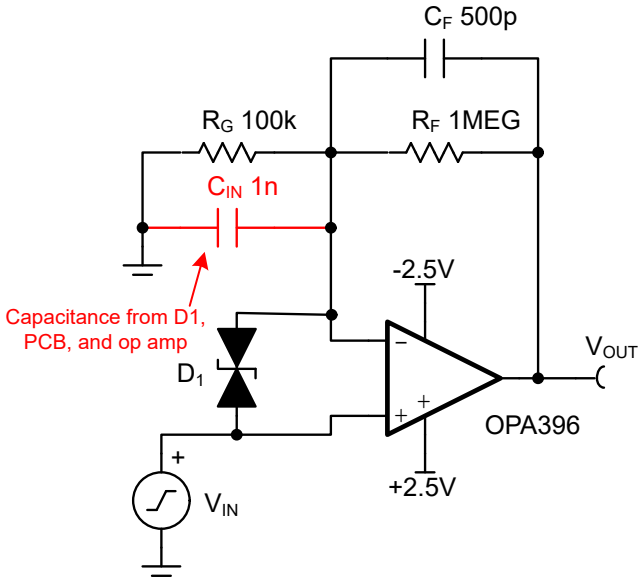


**Figure 5-12. Large CF for Stability ($f_P$ Greater Than $f_Z$)**

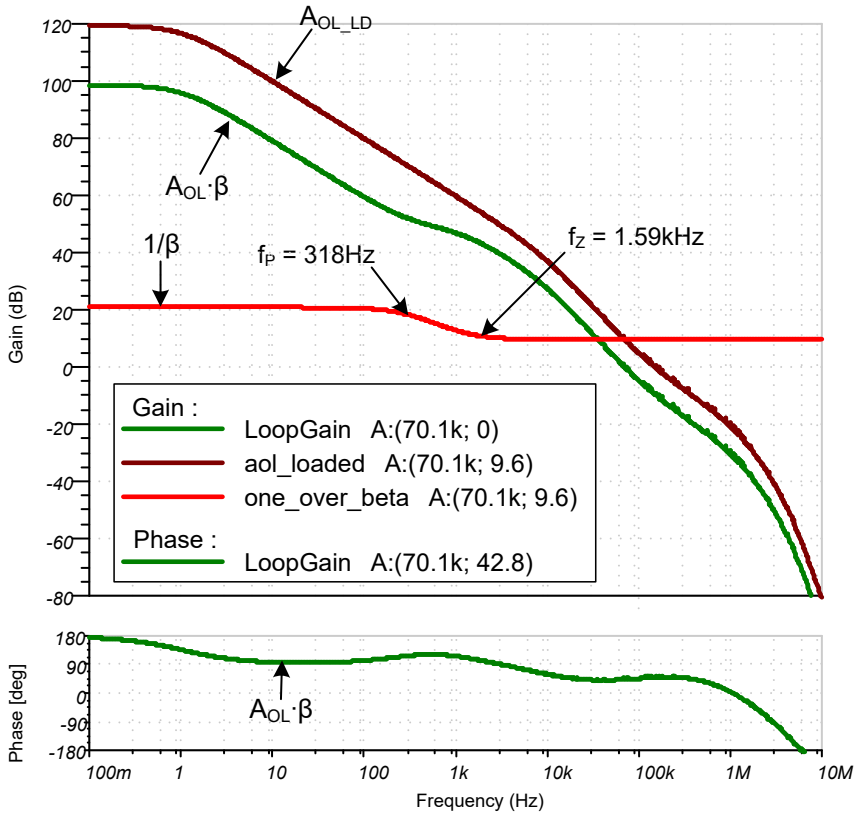


**Figure 5-13. Open-Loop Response Using Large $C_F$ for Stability ($f_P$ Greater Than $f_Z$)**

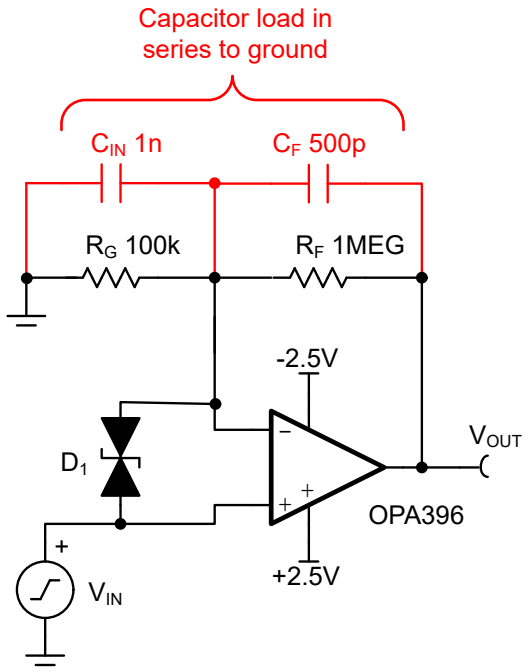


**Figure 5-14. Large $C_F$ and Large $C_{IN}$ Combine Into Capacitive Load**

Figure 5-15 summarizes the three different design cases (large $C_F$, balanced $C_F$, and minimum $C_F$). The top graph shows the gain versus frequency, the center graph shows the noise spectral density, and the bottom graph shows the total RMS noise. The main point of this summary is that using a larger value of $C_F$ decreases noise and bandwidth. Another point is that the gain versus frequency plot does not necessarily look like a first order low pass filter because the feedback capacitor and the $A_{OL}$ roll-off create a second order system at high frequency. The capacitive load also causes some gain peaking just before the gain starts to roll-off. The gain plot follows the 1/β plot for large loop gains.

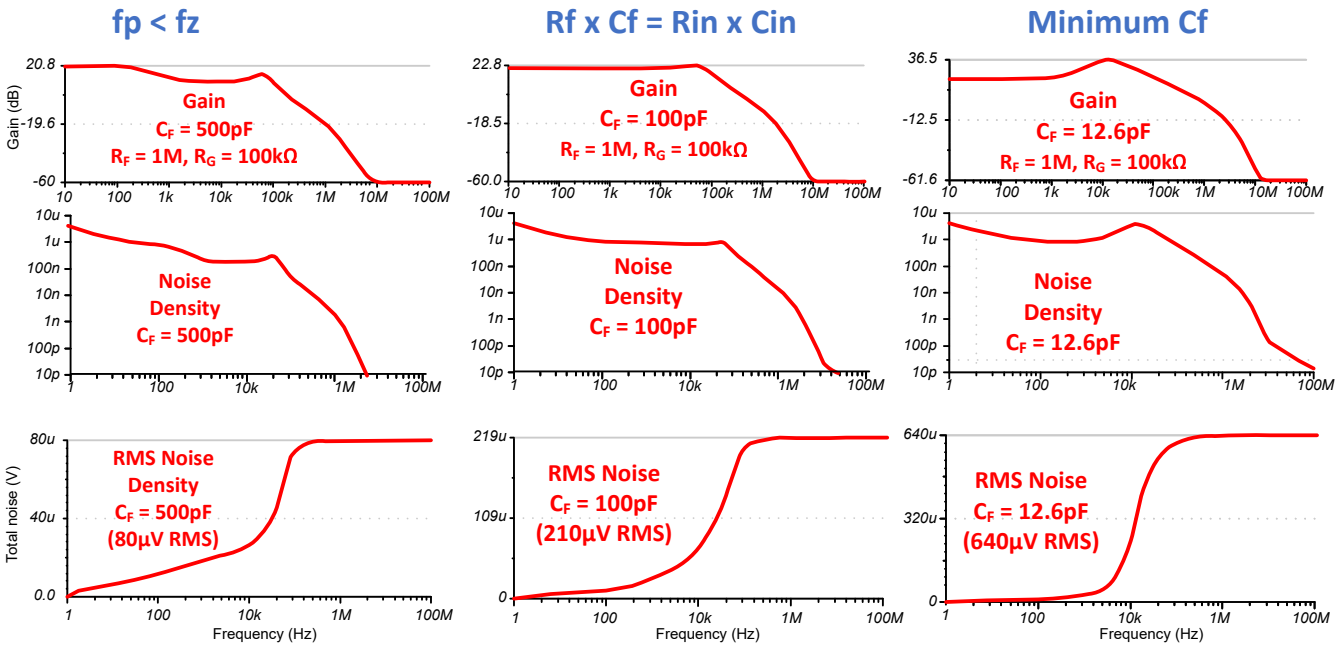


**Figure 5-15. Gain, Noise Density, and Total Noise for Different Values of $C_F$ (OPA396)**

The Analog Engineers Calculator has a utility that allows graphing the open-loop and closed response for a circuit with capacitance on the inverting node. The tool also has a recommend compensation button that chooses the minimum value for $C_F$ according to Equation 76. This tool requires the user to enter a few

parameters for the op amp (gain bandwidth, $A_{OL}$, $R_O$, and second pole). The tool assumes a resistive output impedance, so for circuits with complex output impedance a simulation is required for better accuracy.

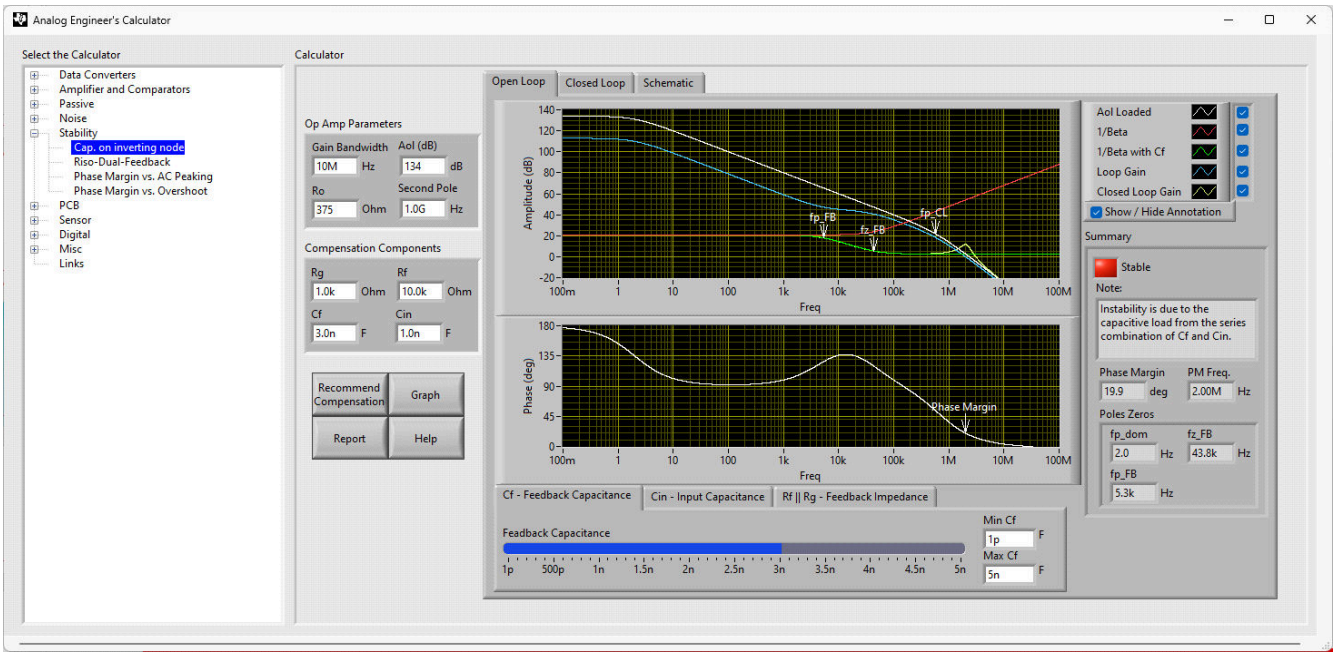


**Figure 5-16. Software Tool to Analyze and Optimize Circuits With Capacitance on the Inverting Input**

## 5.4 Transimpedance Case

The transimpedance amplifier is a common example of a circuit that has stability problems due to capacitance on the inverting node. While the stability concerns with a transimpedance amplifier can be solved using the methods described in previous sections, looking at this configuration separately is worthwhile as the configuration is very common and some additional detail is helpful. The transimpedance amplifier converts a current input to an output voltage. Transimpedance amplifiers are frequently connected to photodiodes because photodiodes output a current proportional to light. A reverse biased photodiode is generally connected directly to the inverting input with respect to ground. Reverse biased photodiodes can have significant capacitance because the cathode and anode act as a parallel plate capacitor with the depletion region acting as the dielectric. Note that the photodiode model contains a current source to emulate the diode output current versus light. The photodiode model also contains the junction capacitance ($C_J$) and a parasitic leakage resistance $R_S$. The op amp transimpedance gain is set by $R_F$, so often large values of $R_F$ are used to amplify the small photodiode currents. The combination of the large feedback resistor with the photodiode capacitance often leads to instability. Figure 5-17 illustrates the transimpedance configuration connected to a photodiode as well as the photodiode equivalent circuit.

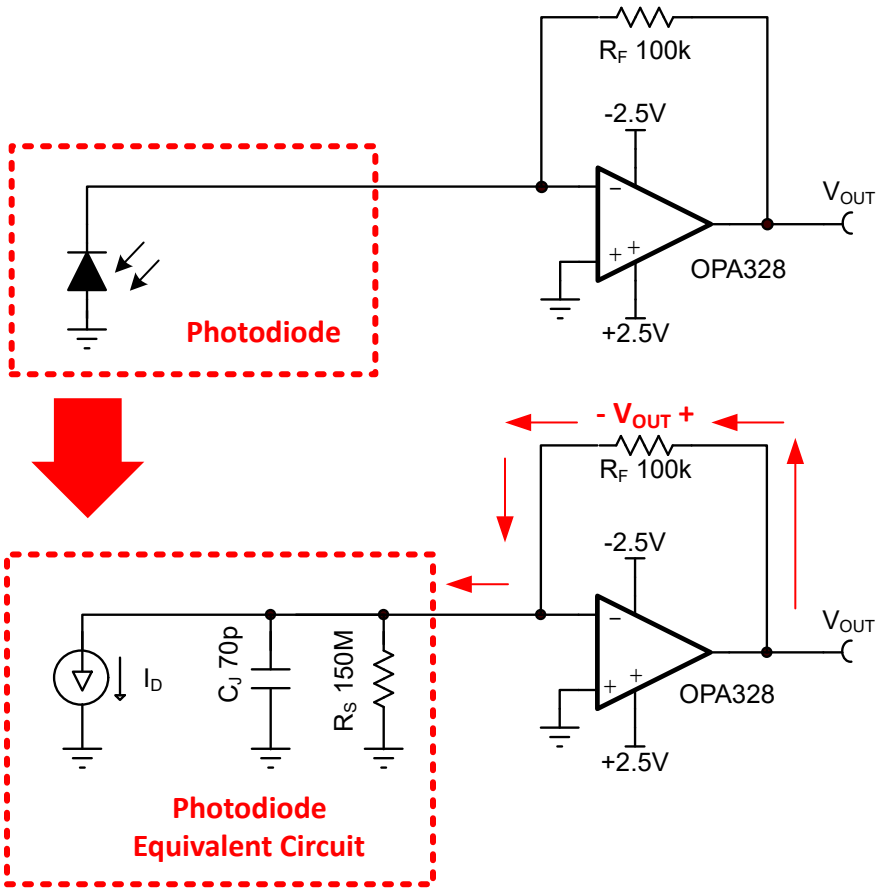


**Figure 5-17. Photodiode Model for Transimpedance Amplifier**

Figure 5-18 shows the uncompensated closed-loop transimpedance amplifier that is used for this example. Figure 5-19 shows the closed-loop AC response for Figure 5-18. Note that the gain shown in this example is the transimpedance gain ($V_{OUT}/I_D$ ). The DC transimpedance gain is approximately equal to $R_F$, or in decibels $20 \times \log(R_F)$. The large AC peaking and large rapid phase shift is an indication that the circuit is not stable. The reason this circuit is unstable is the large capacitance on the inverting node in conjunction with the large feedback resistor ($C_J$ = 70pF, and $R_F$ = 100kΩ).

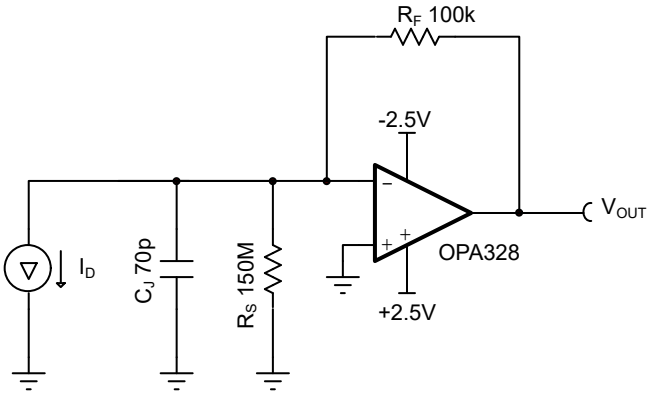


**Figure 5-18. Unstable Transimpedance (Photodiode) Amplifier**

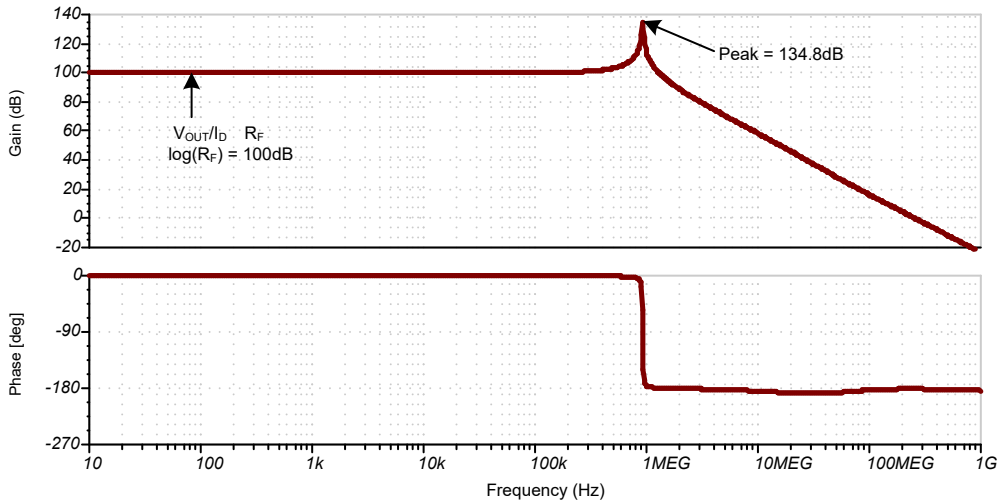


**Figure 5-19. Response for Unstable Transimpedance (Photodiode) Amplifier**

The circuit for testing the open-loop response of the transimpedance amplifier is shown in Figure 5-20, and the open-loop AC response is shown in Figure 5-22. The open-loop response shows that a zero in 1/β causes the rate-of-closure to be 40dB/dec where $A_{OL}$ intersects 1/β. The circuit stability challenges are confirmed by the 1.5° phase margin. As we saw earlier in this section, the correction is to cancel the pole with a zero by adding a feedback capacitor ($C_F$).

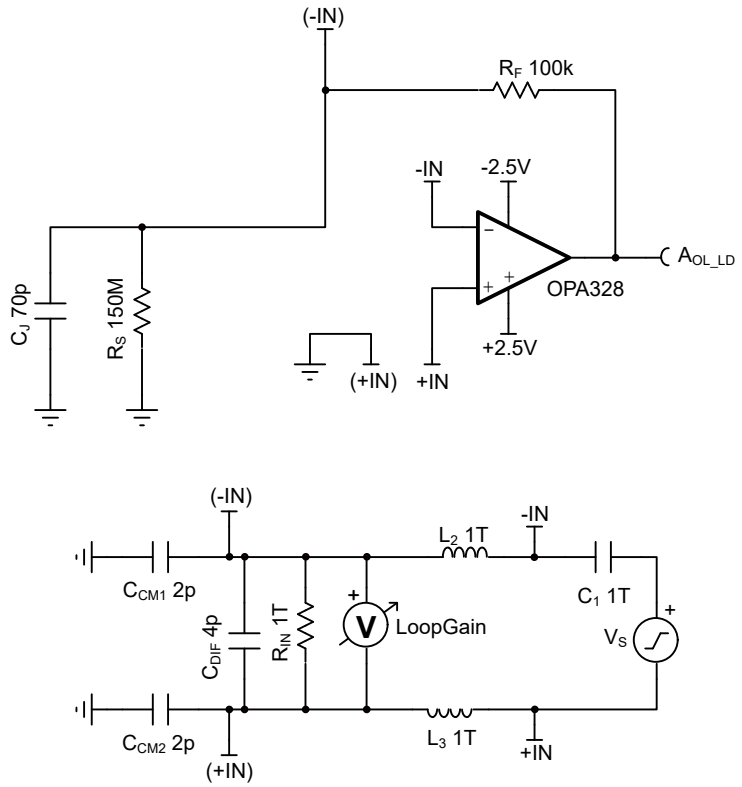


**Figure 5-20. Open-Loop Test Circuit for Unstable Transimpedance (Photodiode) Amplifier**

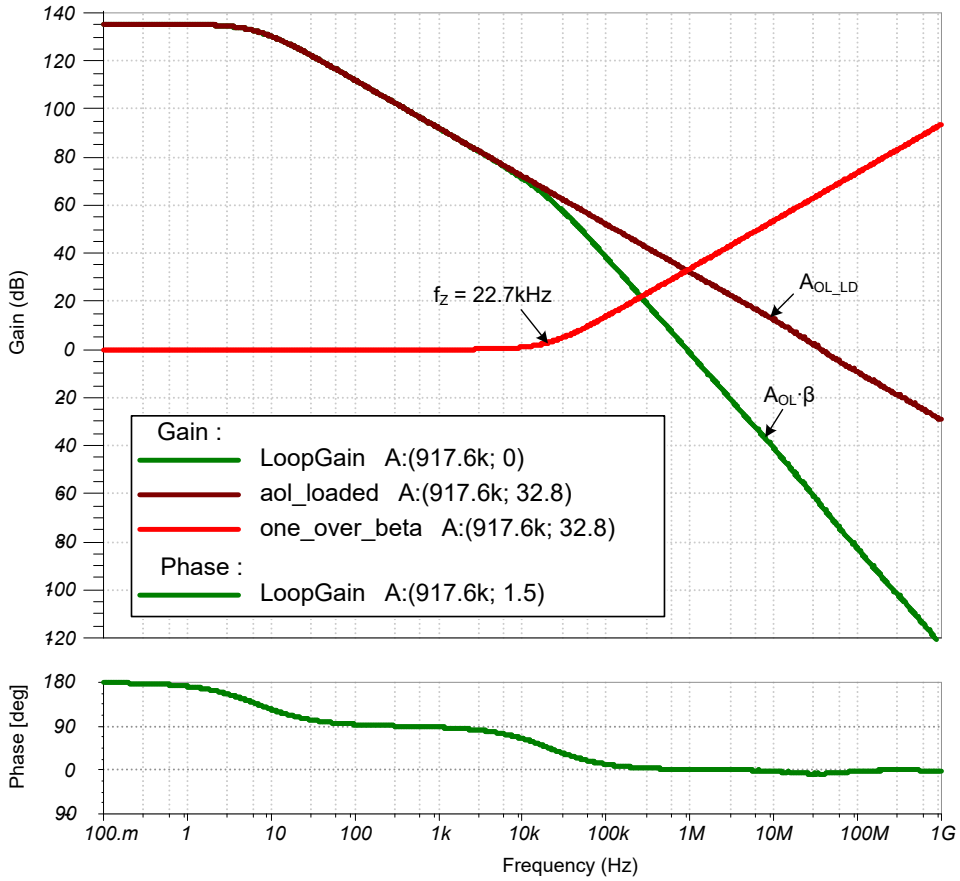


**Figure 5-21. AC Open-Loop Response for Unstable Transimpedance Amplifier**

Equation 82 can be used to select the minimum value of $C_F$ for stability ($C_{F(MIN)}$ = 1.67pF in this example). The location of the zero and pole in 1/β can be found in Equation 83 and Equation 85, respectively. Figure 5-22 graphs the open-loop response with the minimum $C_F$. Notice that the phase margin for the circuit with minimum $C_F$ is 51.4°, whereas phase margin was 1.5° without $C_F$.

$$C_{F(min)} = \sqrt{\frac{C_J}{2 \times \pi \times R_F \times f_{UGBW}}} = \sqrt{\frac{70pF}{2\pi(100k)(40MHz)}} = 1.67pF \quad (82)$$

$$f_Z = \frac{R_S + R_F}{2 \times \pi \times C_J \times R_S \times R_F} = \frac{150M\Omega + 100k\Omega}{2 \times \pi \times (70pF)(150M\Omega)(100k\Omega)} = 22.7kHz \quad (83)$$

$$f_Z \cong \frac{1}{2 \times \pi \times C_J \times R_f} = 22.7kHz, \text{ for } R_S \gg R_F \quad (84)$$

$$f_P = \frac{1}{2 \times \pi \times C_F \times R_F} = \frac{1}{2 \times \pi \times (1.67pF)(100k\Omega)} = 953kHz \quad (85)$$

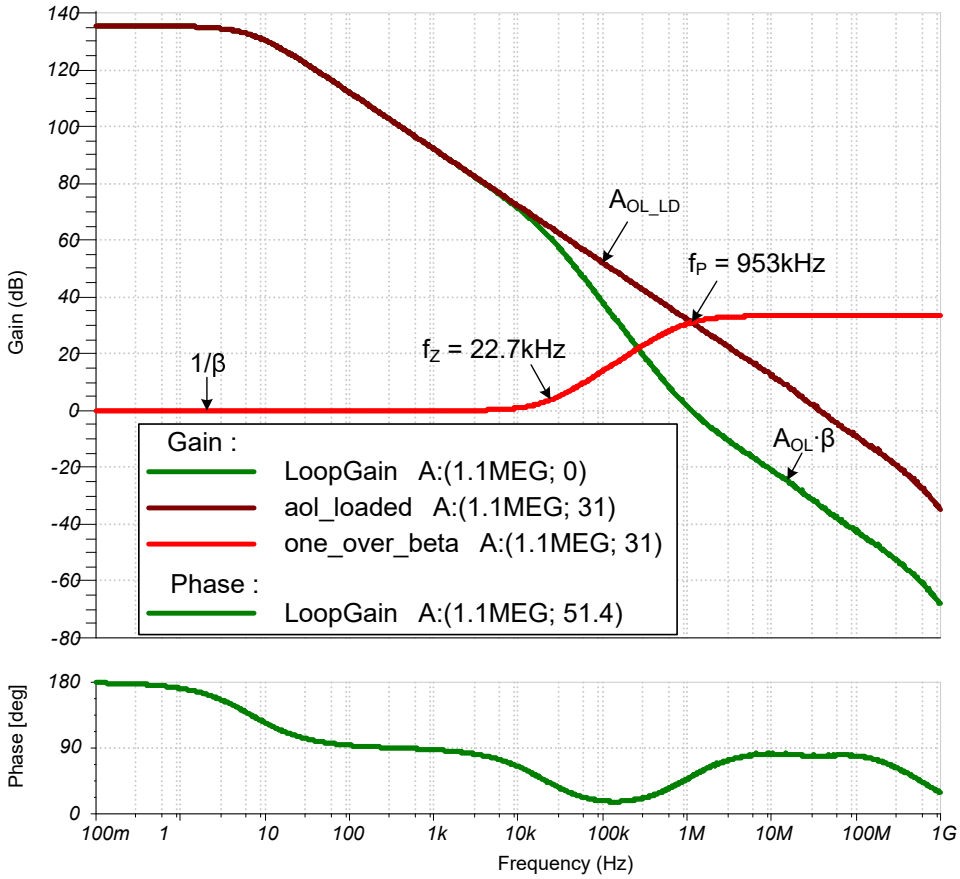


**Figure 5-22. AC Open-Loop Response for Stable Transimpedance Amplifier Using Minimum $C_F$**

Increasing the value of $C_F$ beyond the minimum value of $C_F$ generally improves the stability further. However, for larger values of $C_F$, the series combination of $C_F$ and $C_J$ can potentially create a capacitive load from the output to ground that can cause stability problems. The value of $C_F$ also determines the closed-loop transimpedance bandwidth (see Equation 86) as well as the total output noise. Increasing the value of $C_F$ reduces the bandwidth and noise. Figure 5-24 shows the closed-loop frequency response for the circuit in Figure 5-23 with different feedback capacitors. You can see that the circuit with no feedback capacitor (0F) has a large 34dB gain peak, and with the minimum (1.7pF) capacitor the gain peak is eliminated and the maximum transimpedance bandwidth is achieved. Using larger feedback capacitors further reduce the bandwidth but can introduce a stability issue at some point due to capacitive loading ($C_L = C_F + C_J$).

$$f_{BW} = \frac{1}{2 \times \pi \times R_F \times C_F} \tag{86}$$

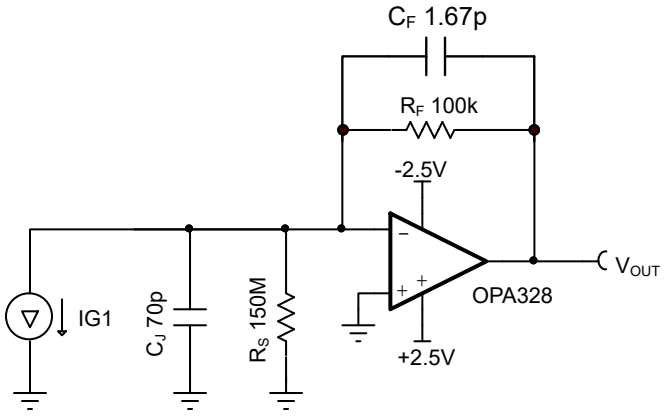


**Figure 5-23. AC Closed-Loop Transimpedance Circuit**

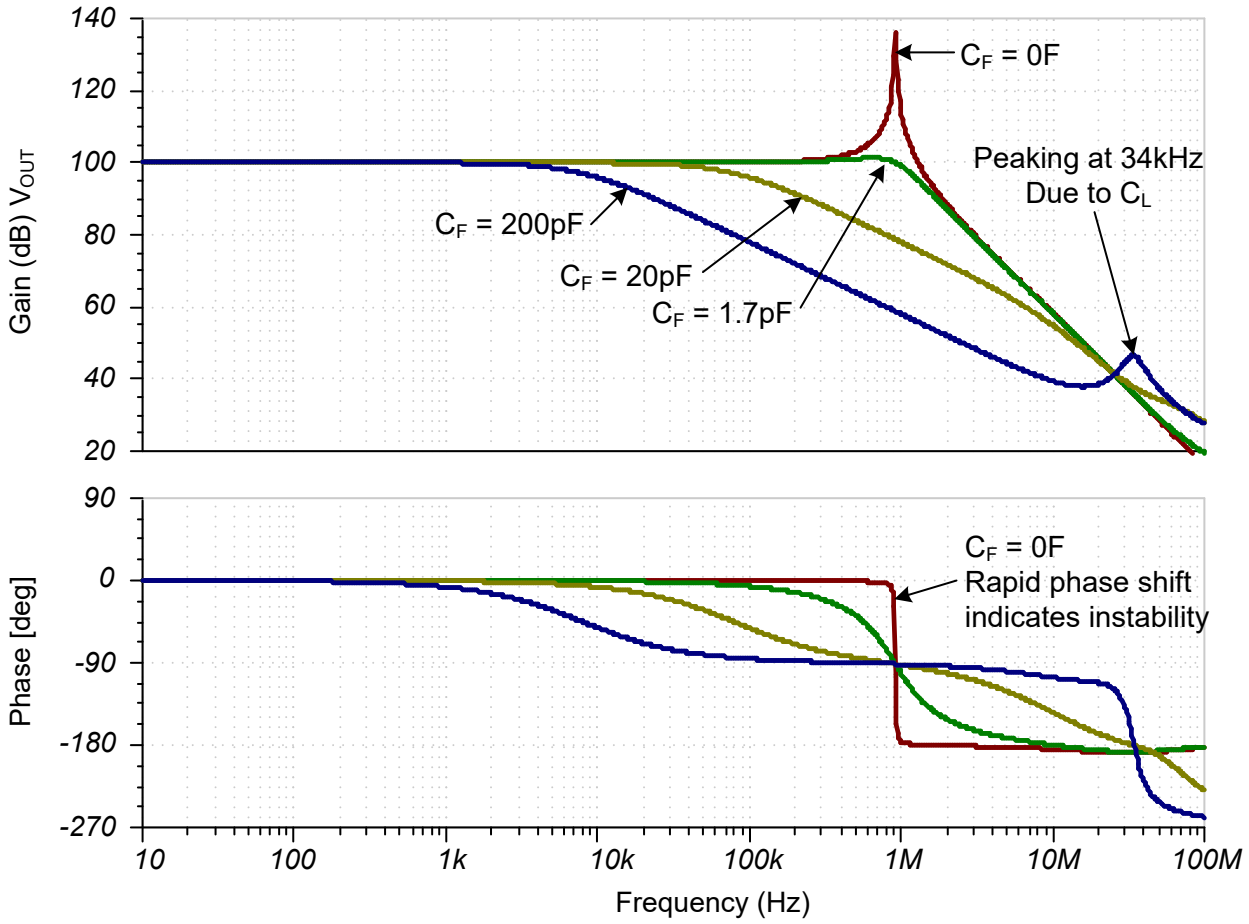


**Figure 5-24. AC Closed-Loop Response for Different Feedback Capacitor**

# 6 Complex Open-Loop and Closed-Loop Output Impedance

Up to this point, the document has considered the open-loop output impedance ($Z_O$) to be a purely resistive value. Meaning, the value of $Z_O$ used in previous analysis was flat across frequency and did not contain any imaginary numbers. This section covers complex output impedance. In this instance, the term *complex* is used to describe an impedance that contains imaginary numbers from reactive impedance components. The magnitude of complex impedance is *not* flat across frequency. Furthermore, up to this point, the document uses the op amp open-loop output impedance as part of the stability analysis. Some op amp datasheets specify open-loop output impedance and others specify closed-loop output impedance. Depending on the specific stability problem, sometimes the closed-loop impedance can better facilitate analysis, and in other cases the open-loop impedance is better. This section shows how to mathematically convert open-loop output impedance to closed-loop and shows how to analyze stability using closed-loop output impedance. To clarify the difference between open-loop and closed-loop output impedance, this document designates $Z_O$ for open-loop output impedance and $Z_{OUT}$ for closed-loop.

## 6.1 Converting Open-Loop Output Impedance to Closed-Loop Output Impedance

Equation 87 shows how to translate open-loop output impedance ($Z_O$) to closed-loop output impedance ($Z_{OUT}$). Notice that $Z_O$ is divided by $1+\beta \times A_{OL}(f)$ which is generally a very large value at low frequency. Thus, at low frequency $Z_{OUT}$ is very small. As frequency increases $A_{OL}(f)$ decreases by 20dB/dec, so the closed-loop output impedance increases by 20dB/dec. Meaning, when $Z_O$ is resistive (flat versus frequency), $Z_{OUT}$ looks inductive (increasing by 20dB/dec over frequency). This principle can be shown mathematically by substituting $A_{OL}(f)$ using a single pole $A_{OL}$ model (see Equation 87 and Equation 88). Using algebra to simplify Equation 88 yields Equation 89. Inspecting Equation 89 shows that $Z_{OUT}$ has a zero at the dominant pole frequency of $A_{OL}$, and the pole at the bandwidth limit of the amplifier. Between the low frequency dominant pole and the high frequency bandwidth limit the $Z_{OUT}$ looks inductive. Also, since equation translating open-loop to closed-loop output impedance includes β, the closed-loop output impedance is gain dependent. Figure 6-2 shows the open-loop output impedance for OPA320 and Figure 6-3 shows the closed-loop impedance for several different gains.

$$Z_{OUT}(f) = \frac{Z_O}{1 + \beta \times A_{OL}(f)} \tag{87}$$

$$Z_{OUT}(f) = \frac{Z_O}{1 + \beta \times \frac{A_{OL\_DC}}{1 + s/\omega_{DOM}}} \tag{88}$$

$$Z_{OUT}(f) = K \times \frac{\frac{s}{\omega_{DOM}} + 1}{\frac{s}{(A_{OL\_DC} \times \beta + 1) \times \omega_{DOM}} + 1} = K \times \frac{\frac{s}{\omega_{DOM}} + 1}{\frac{s}{\omega_P} + 1} \tag{89}$$

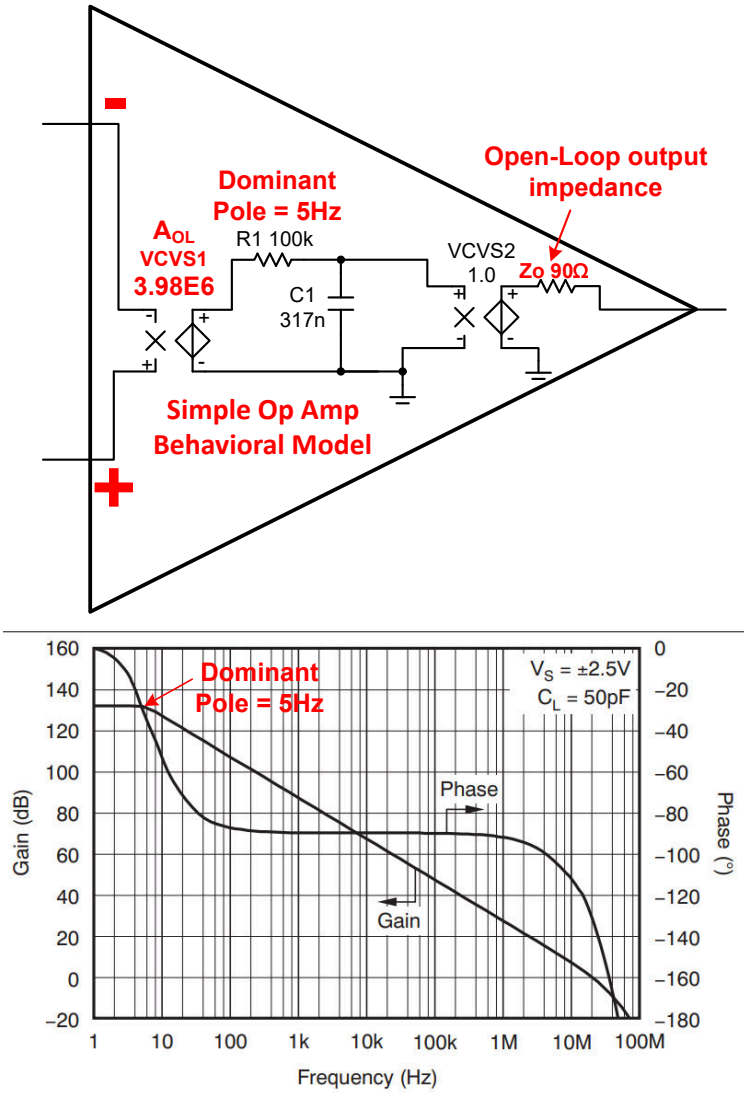


**Figure 6-1. Op Amp Behavioral Model With Single Dominant Pole (OPA320)**

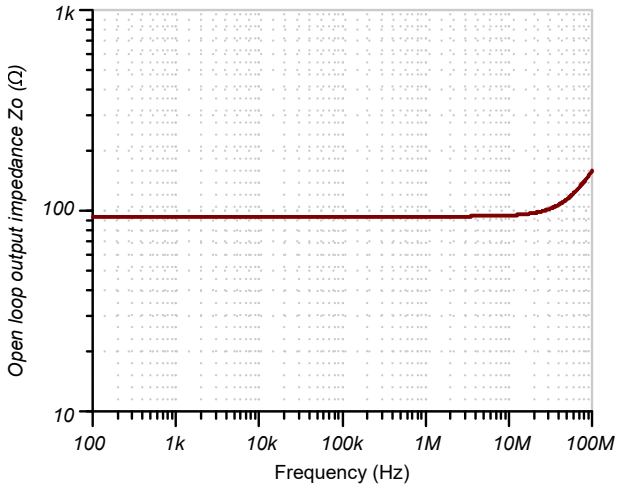


**Figure 6-2. Open-Loop Output Impedance $Z_O$ for OPA320**

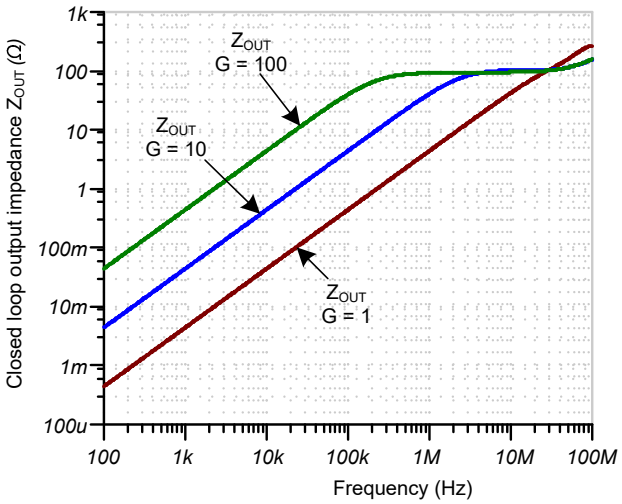


**Figure 6-3. Closed-Loop Output Impedance $Z_{OUT}$ for OPA320**

## 6.2 Open-Loop and Closed-Loop Model Test

Figure 6-4 illustrates the SPICE test circuit used to generate the open-loop output impedance graph. The circuit uses a large 1TH test inductor in the feedback path to create a closed-loop DC bias path, but an open-loop response for AC frequencies. The current source at the output injects a current into the output impedance so that the output voltage is equal to the output impedance. When displaying the response in SPICE, make sure to display the results as a linear value on a logarithmic scale and not in decibels. Figure 6-5 shows that the simulated $Z_O$ compares well to the measured $Z_O$ as specified in the OPA189 data sheet. The correct modeling of $Z_O$ is critical for doing stability testing, so confirming the model accuracy using this test method is important. Note that the vast majority of Texas Instruments op amp models have an accurate $Z_O$ model.

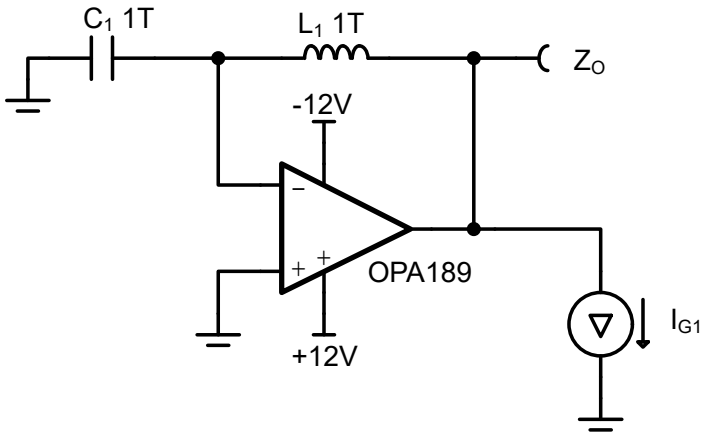


**Figure 6-4. Test Circuit for Open-Loop Output Impedance ($Z_O$)**

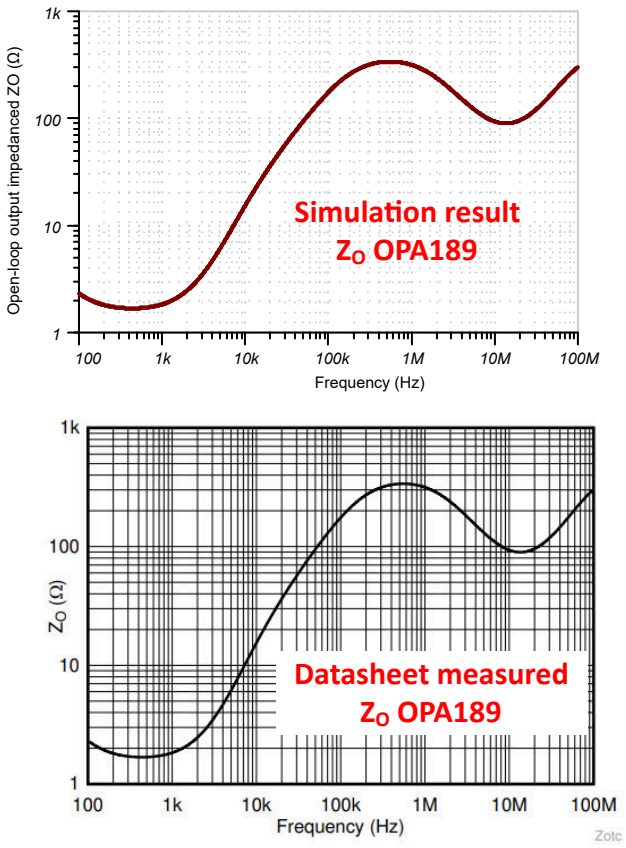


**Figure 6-5. Simulated Versus Measured Open-Loop Output Impedance**

Figure 6-6 illustrates how to test closed-loop output impedance versus frequency. For this test, inject a test current and monitor the output voltage. The example shows a unity gain configuration, but the test must be done in whatever gain is used in the application. The simulated output voltage is equal to the closed-loop output impedance. Make sure to display the results as a linear value on a logarithmic scale and not in decibels.

Figure 6-7 compares the closed-loop and open-loop output impedance for the OPA189. The OPA189 is an interesting example because the open-loop impedance is not flat across frequency. Rather, the OPA189 open-loop impedance has multiple different regions where the impedance acts inductive, capacitive, or resistive. Recall that the impedance of an inductor increases at 10x/dec ($Z_L = j \times 2 \times \pi \times f \times L$), and the impedance of a capacitor decreases at 10x/dec ($Z_C = 1/(j \times 2 \times \pi \times f \times C)$. In this open-loop graph example, notice that $Z_O$ increases from about 10Ω to 100Ω in one decade, so that region is called *inductive*. For the closed-loop plot, the slope of each region is increased by 10 times per decade, as discussed in Section 6. Thus, a capacitive region in open-loop becomes resistive in closed-loop because the capacitive pole is canceled by zero introduced in the translation from open-loop to closed-loop (see Figure 6-7). Likewise, resistive open-loop impedance translates to inductive closed-loop, and inductive open-loop translates to double-inductive closed-loop. The term double inductive refers to the slope of 100x/dec in the closed-loop impedance. A double inductive slope can only be produced in a circuit with gain, as there are no physical double inductive circuit elements.

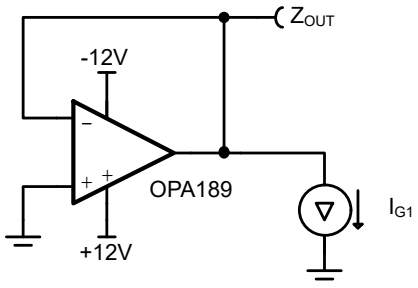


**Figure 6-6. Test Circuit for Closed-Loop Output Impedance ($Z_{OUT}$)**

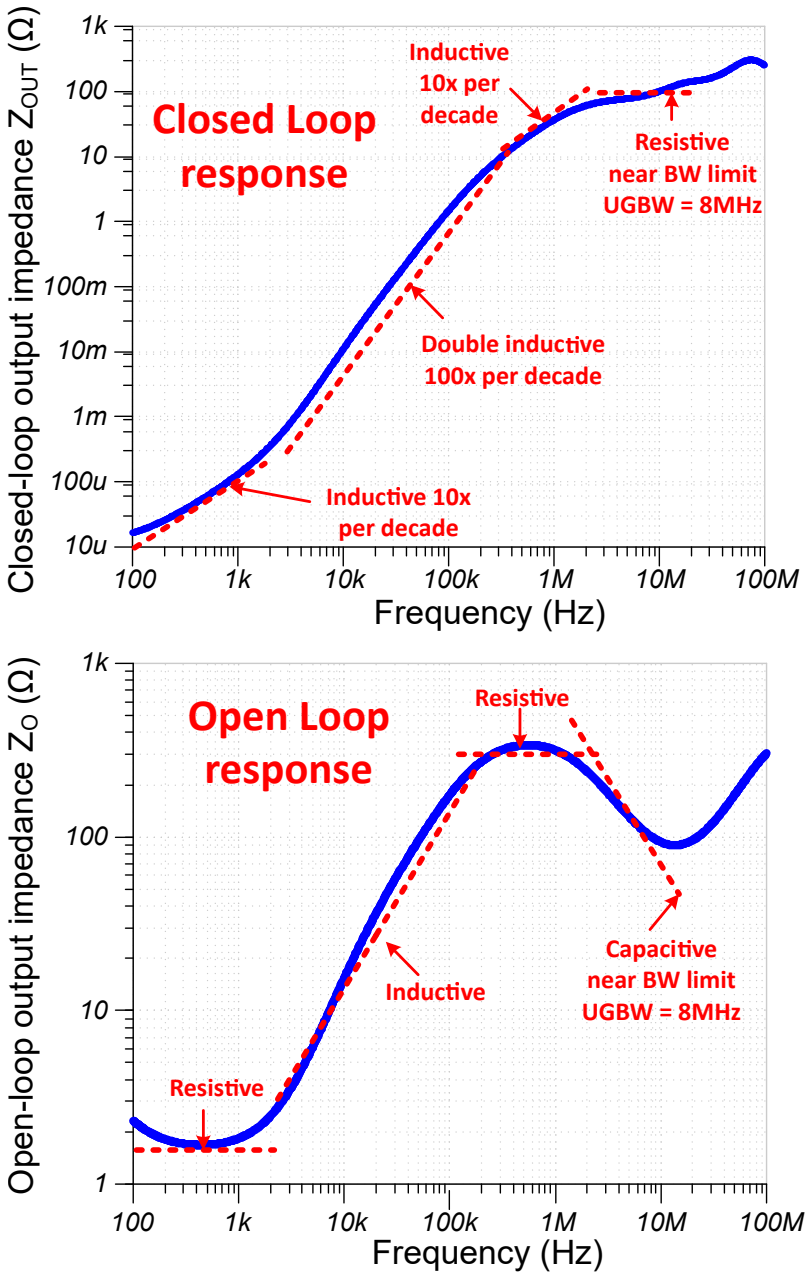


**Figure 6-7. Open-Loop Versus Closed-Loop Output Impedance for OPA189**

## 6.3 Instability Due to Resonance From Complex Output Impedance

Up to this point, the stability analysis in this document has assumed that the open-loop output impedance ($Z_O$) is flat across frequency (resistive). Also, larger values of $Z_O$ require larger isolation resistance for stability and make the amplifier more sensitive to capacitive load. Meaning, the largest $Z_O$ value is the worst case from a stability perspective. To select the appropriate compensation, using the largest value of $Z_O$ seems to be a good design approach, but in reality, there are additional considerations.

Figure 6-8 shows the open-loop output impedance for the OPA189. Using the maximum value for $Z_O$ in Equation 90 yields the minimum value of $R_{ISO}$ that stabilizes the op amp. In this example, $R_{ISO}$ = 19Ω stabilizes the amplifier. However, looking at the open-loop AC response, the phase margin of 37.7° indicates poor stability (see Figure 6-9 and Figure 6-10). More importantly, resonant peak can be seen in the gain plot which is coincident with a rapid shift in phase (resonance at f = 90kHz in Figure 6-10). The resonance is the main cause of instability and this section explains the cause and resolution of this issue.

$$R_{ISO} = \frac{1 + \sqrt{1 + \left(8\pi \times R_O \times C_{LOAD} \times f_{gbw}\right)}}{4\pi \times C_{LOAD} \times f_{gbw}} = \frac{1 + \sqrt{1 + (8\pi \times 300\Omega \times 10nF \times 14MHz)}}{4\pi \times 10nF \times 14MHz} = 19\Omega \quad (90)$$

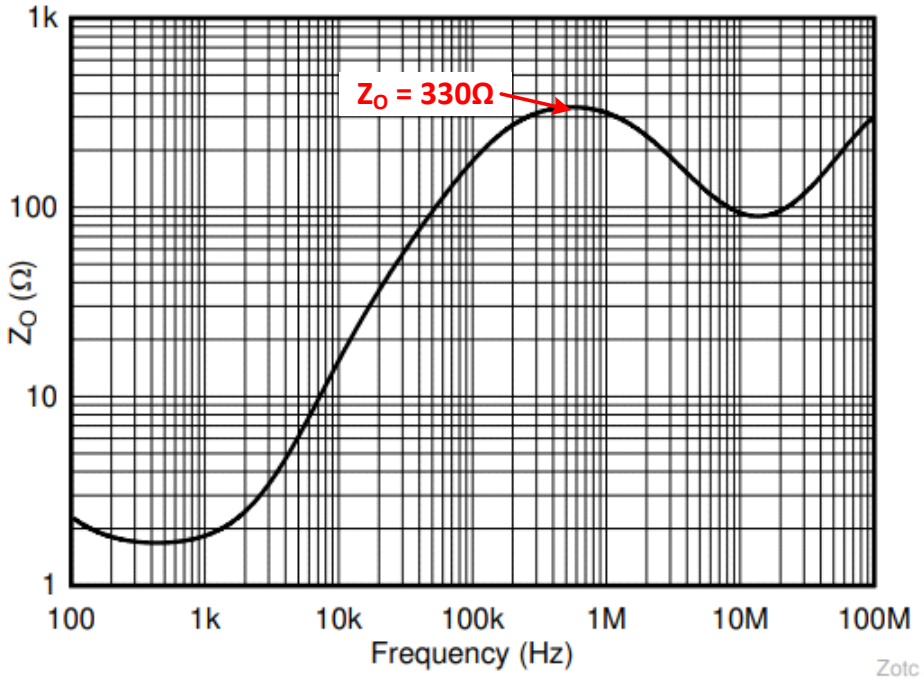


**Figure 6-8. OPA189 Open-Loop Output Impedance**

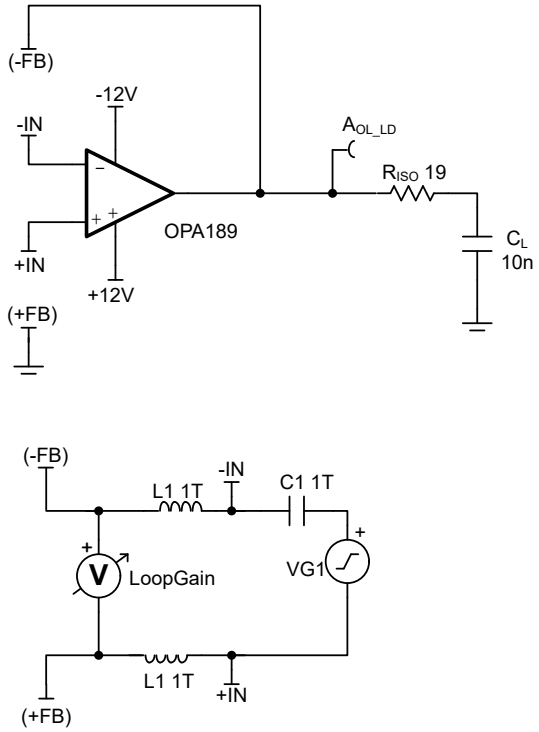


**Figure 6-9. Open-Loop Test Circuit for OPA189 Configuration**

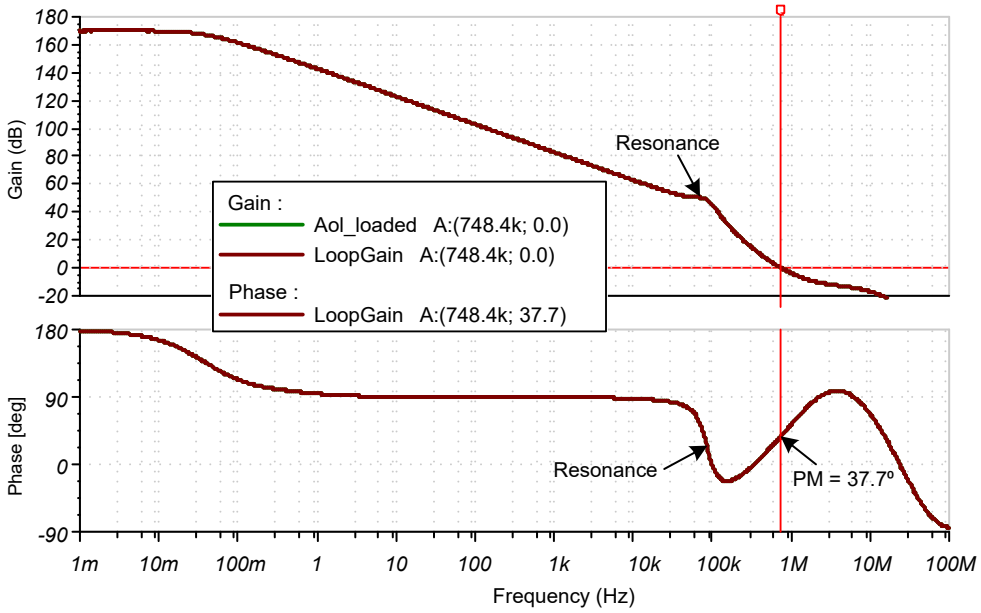


**Figure 6-10. Open-Loop AC Response for OPA189 Circuit**

Figure 6-11 illustrates the closed-loop small-signal step response for the OPA189 example. The response has 8.6mV (43% on a 20mVpp step) of overshoot which corresponds to 29.0° of phase margin (see Figure 2-14). In this example, the open-loop test indicated a phase margin of 37.7°, and the closed-loop indicates 29.0°. The reason for the discrepancy is that the circuit has an instability due to a resonance at 90kHz, as well as a rate of closure issue where loop gain goes to zero. The resonance is due to the complex nature of the output impedance.

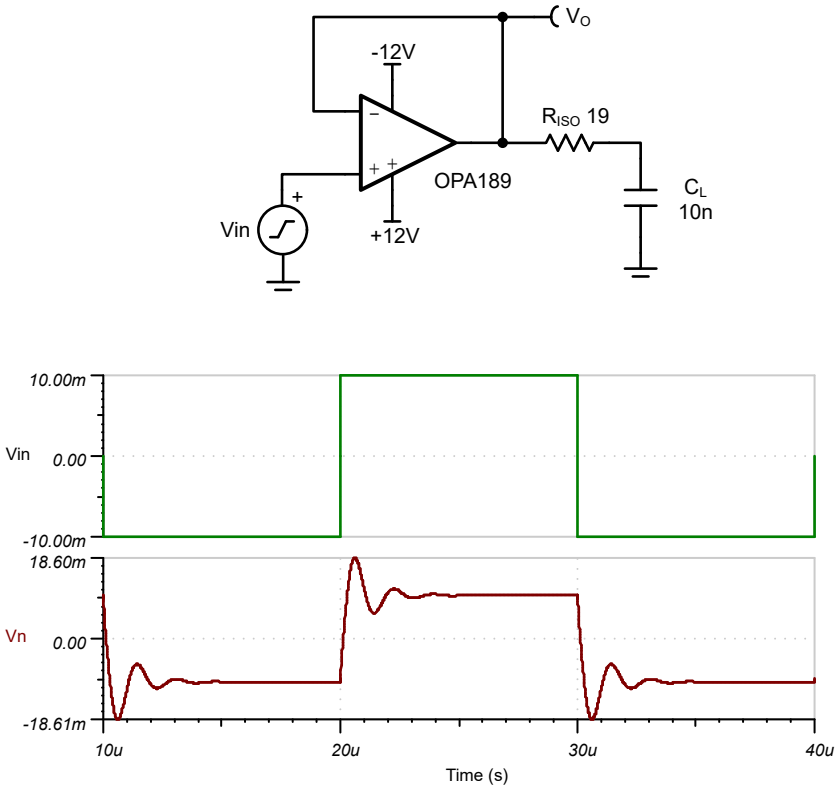


**Figure 6-11. Closed-Loop Small-Signal Step Response for OPA189**

In Figure 6-10, there is a resonance at 90kHz which is largely responsible for the amplifier instability. This resonance results from the load ($C_L$) interacting with the complex closed-loop output impedance ($R_O$). One way to understand the source of the resonance is to plot the load impedance versus the op amp closed-loop output impedance and use the rate of closure rule. Figure 6-12 illustrates the SPICE method for graphing the load-impedance. The closed-loop output impedance can be tested using the method illustrated in Figure 6-11. The closed-loop output impedance and the load impedance are both graphed on Figure 6-13. Notice that the load impedance ($Z_{LOAD}$) intersects the open-loop output impedance in the inductive region. Also notice that the slope of $Z_{LOAD}$ is 20dB/dec (10x/dec) where the two curves intersect. Thus, the rate-of-closure is 40dB/decade. Based on the curve, you can see that moving the $Z_L$ curve to the left changes the rate of closure to 20dB/dec because the resistive part of the $Z_L$ curve intersects $Z_{OUT}$ instead of the capacitive part. Figure 6-14 illustrates how increasing $C_L$ shifts the load curve to the left and improves stability. Increasing $C_L$ to help with stability can seem counter intuitive, but stability can improve or compensating for some stability cases can be easier. Figure 6-14 also shows the transient response for the circuit with a 10nF and 100nF load capacitance. The 10nF has more overshoot and worse phase margin than the 100nF (10nF phase margin 28° and the 100nF has phase margin of 40°).

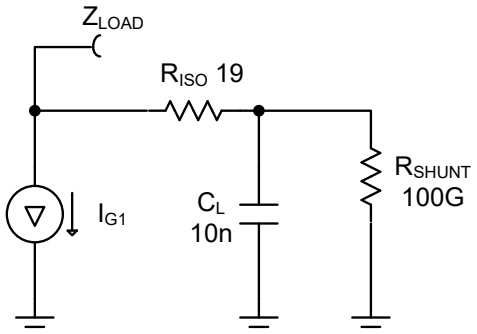


**Figure 6-12. Simulate and Graph Load Impedance $Z_{LOAD}$**

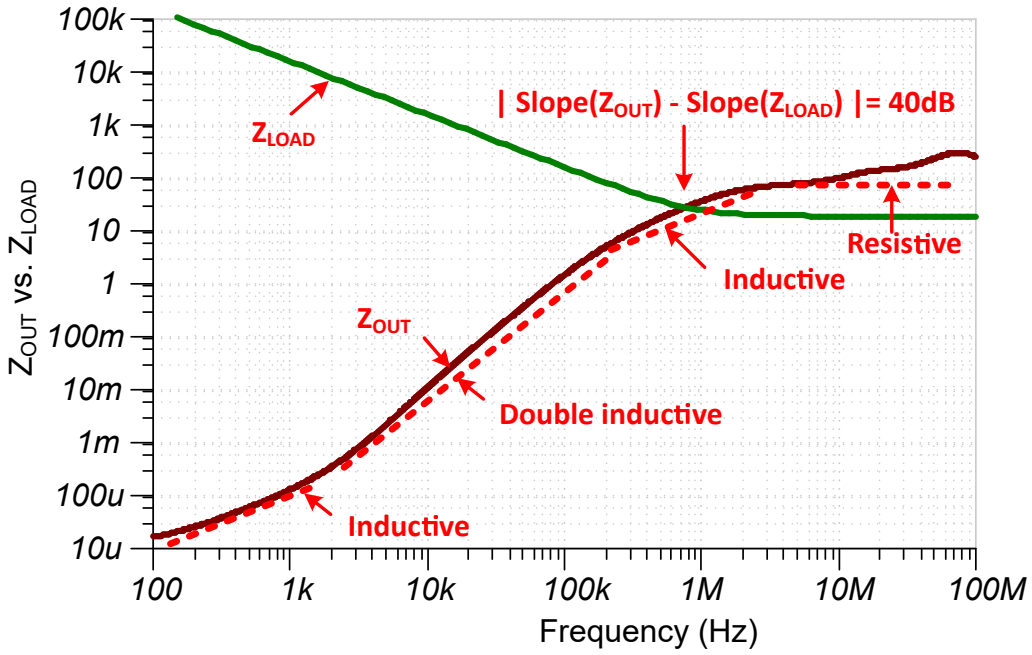


**Figure 6-13. Load Impedance ($Z_{LOAD}$) and Output Impedance ($Z_{OUT}$) Rate-of-Closure Test**

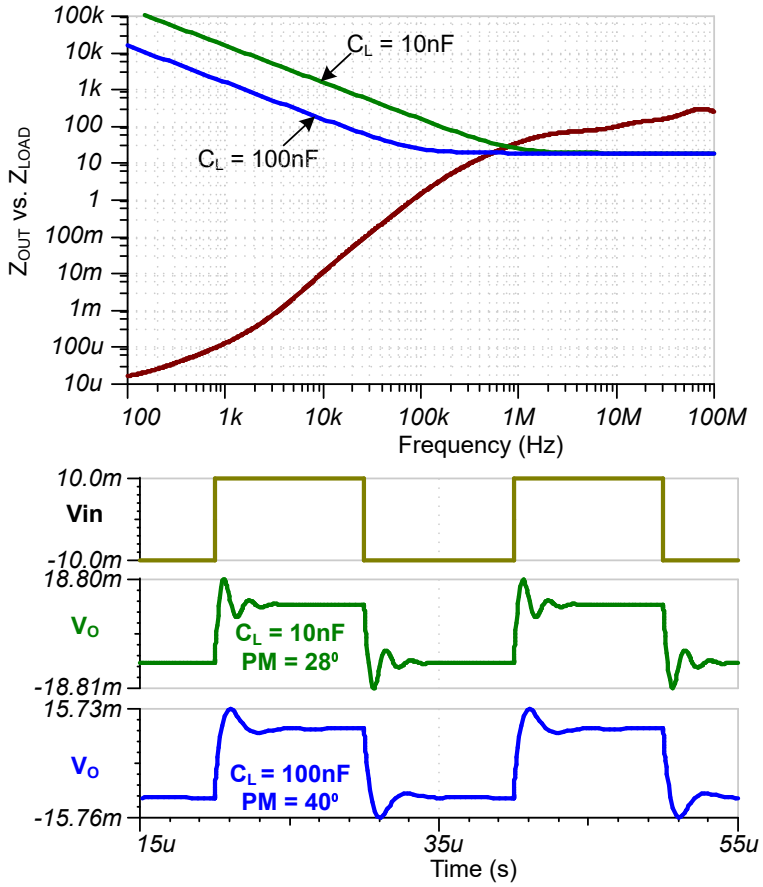


**Figure 6-14. Increasing $C_L$ Improves Stability in this Case**

Figure 6-15 illustrates how increasing $R_{ISO}$ changes the rate-of closure from approximately 40dB/decade to 20dB/decade. Here the term *approximately* is used because the slope of $Z_{OUT}$ is changing continuously in the region where $Z_{LOAD}$ intersects. The important point is that the rate-of-closure improves with increasing resistance. The transient small-signal step also shows that the stability improves with the larger value of $R_{ISO}$.

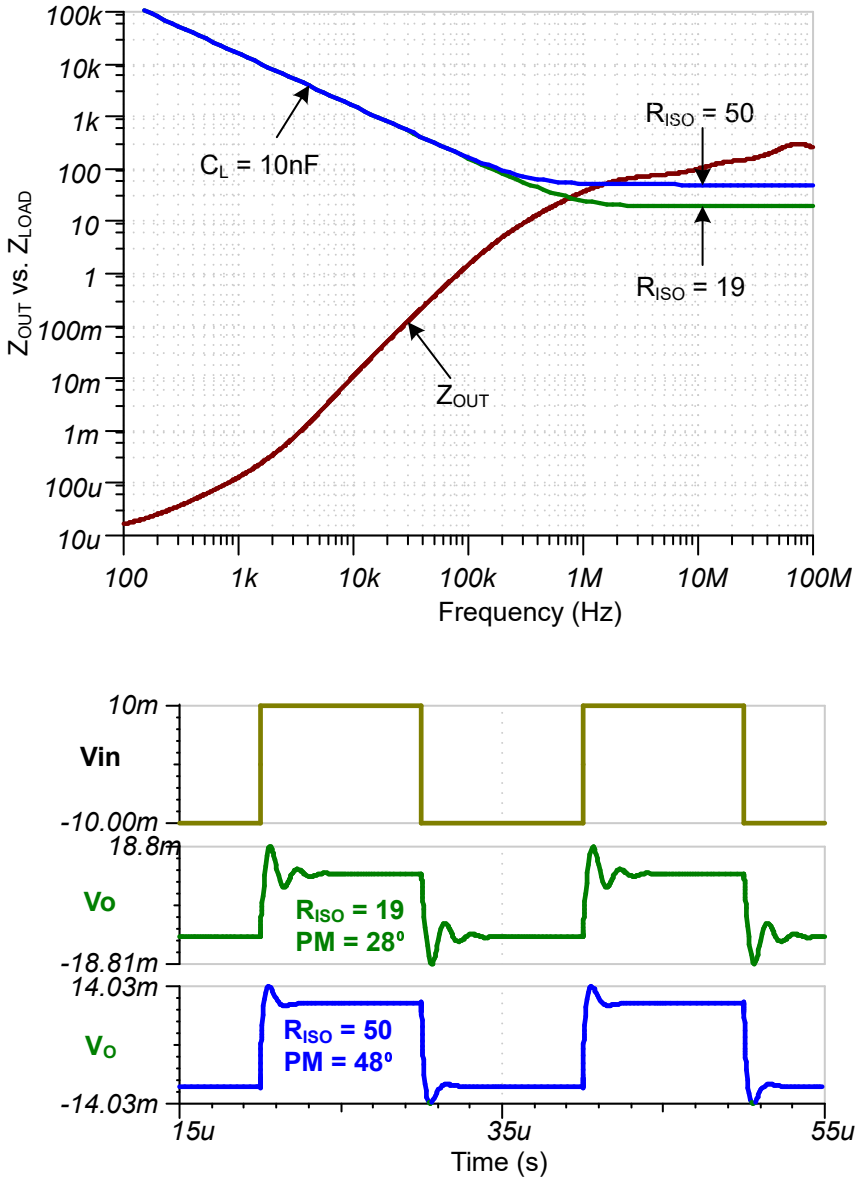


**Figure 6-15. Increasing $R_{ISO}$ Improves Stability**

Since $Z_{OUT}$ has a slope of 40dB/decade from about 2kHz to about 200kHz, the amplifier can potentially be unstable with a resistive load (see Figure 6-13). In Figure 6-16, notice how the low values of load resistance intersect the output impedance curve at a higher rate-of-closure. Also, notice that the overshoot increases for the smaller values of load resistance. The fact that the op amp can be unstable with a resistive load is potentially concerning, but in reality the circuit is stable for practical load resistances and the load must be very small to have stability issues ($R_{ISO}$ ≤ 25Ω in this example).

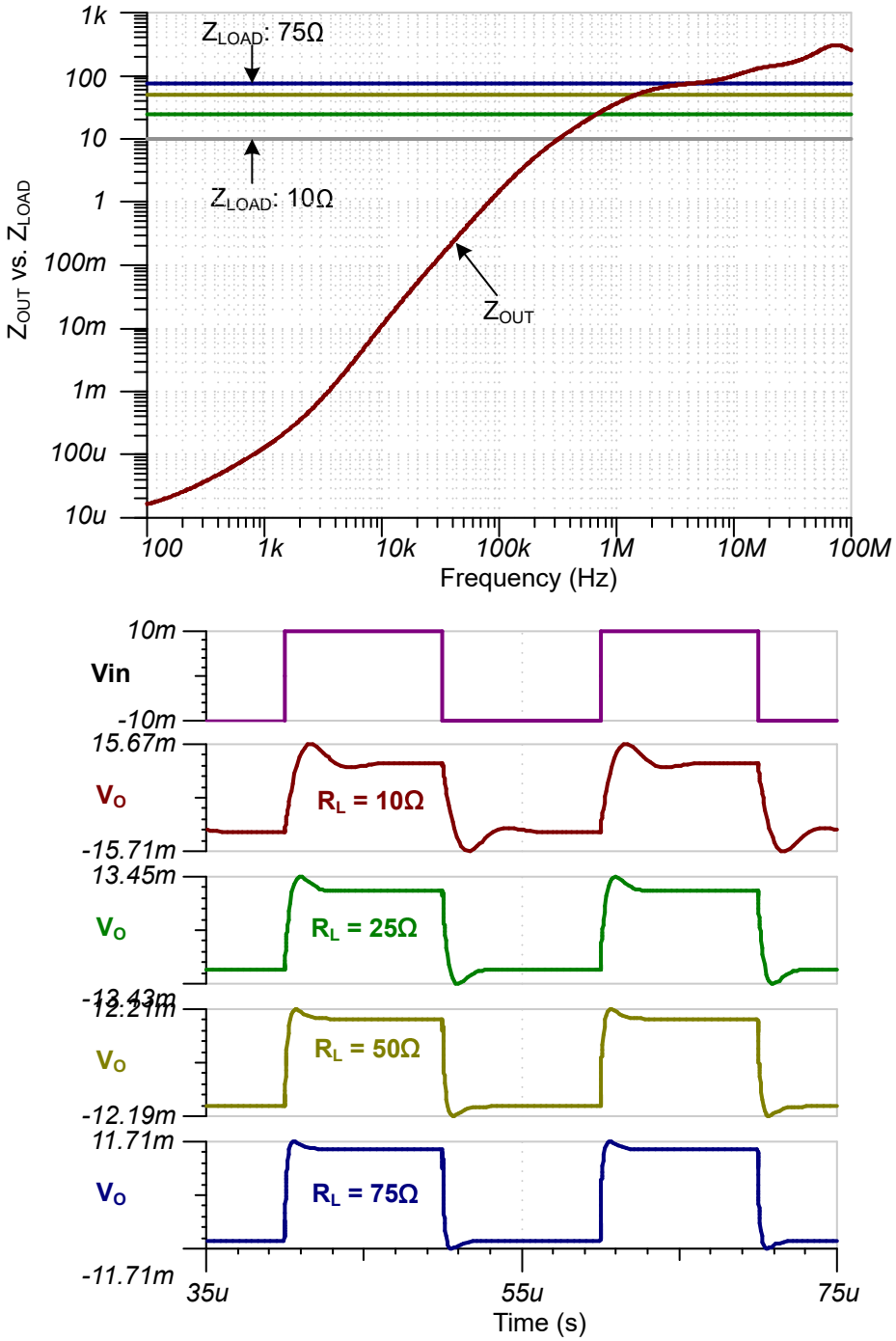


**Figure 6-16. Low Value Resistive Loads Can be Unstable**

As the OPA189 stability example illustrates, circuits with complex open-loop output impedance can be challenging to stabilize. Equation 90 can be used to choose $R_{ISO}$ for circuits with resistive open-loop output impedance ($R_O$) but does not work well for circuits with complex $Z_O$. One possible method for choosing $R_{ISO}$ for circuits with complex $Z_O$ is to plot $Z_{OUT}$ and $Z_{LOAD}$ and graphically choose values to get a 20dB/decade rate of closure. However, this method is time consuming and the value of the precise $Z_{OUT}$ slope is not obvious. Really, the $Z_{OUT}$-$Z_{LOAD}$ curves are most useful in explaining the theory behind instability due to complex $Z_O$, but the curves are not the easiest way to choose components for high stability. A simple approach to choosing $R_{ISO}$ for circuits with complex $Z_O$ is to use parameter stepping.

Parameter stepping is a SPICE analysis method that runs multiple simulations based on sweeping a particular component value. In this case, the value that is varied is $R_{ISO}$. You can find a starting point for $R_{ISO}$ using Equation 90. A good choice for the maximum $R_{ISO}$ is 100 to 1000 times the initial value. Using a logarithmic sweep is a good approach to cover wide ranges. Apply a small-signal input step and look at how the percentage overshoot changes for different values of $R_{ISO}$. The initial sweep potentially does not find the exact desired response, so refine the range as needed and rerun the simulation. Figure 6-17 and Figure 6-18 illustrate the parameter step method on TINA™SPICE, but a similar approach can be followed for most SPICE simulators.

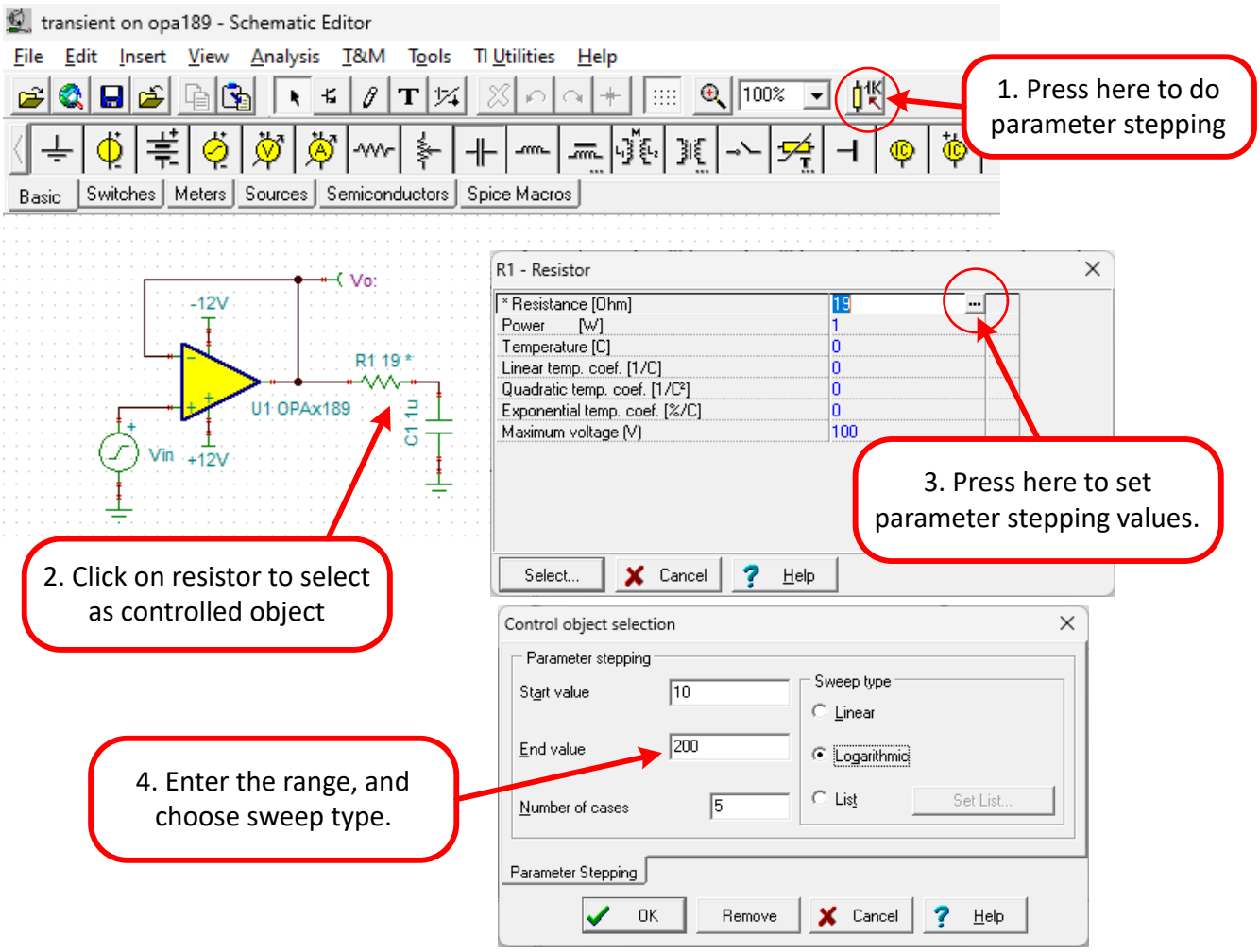


**Figure 6-17. Find the Best $R_{ISO}$ Using TINA™ SPICE Parameter Stepping**

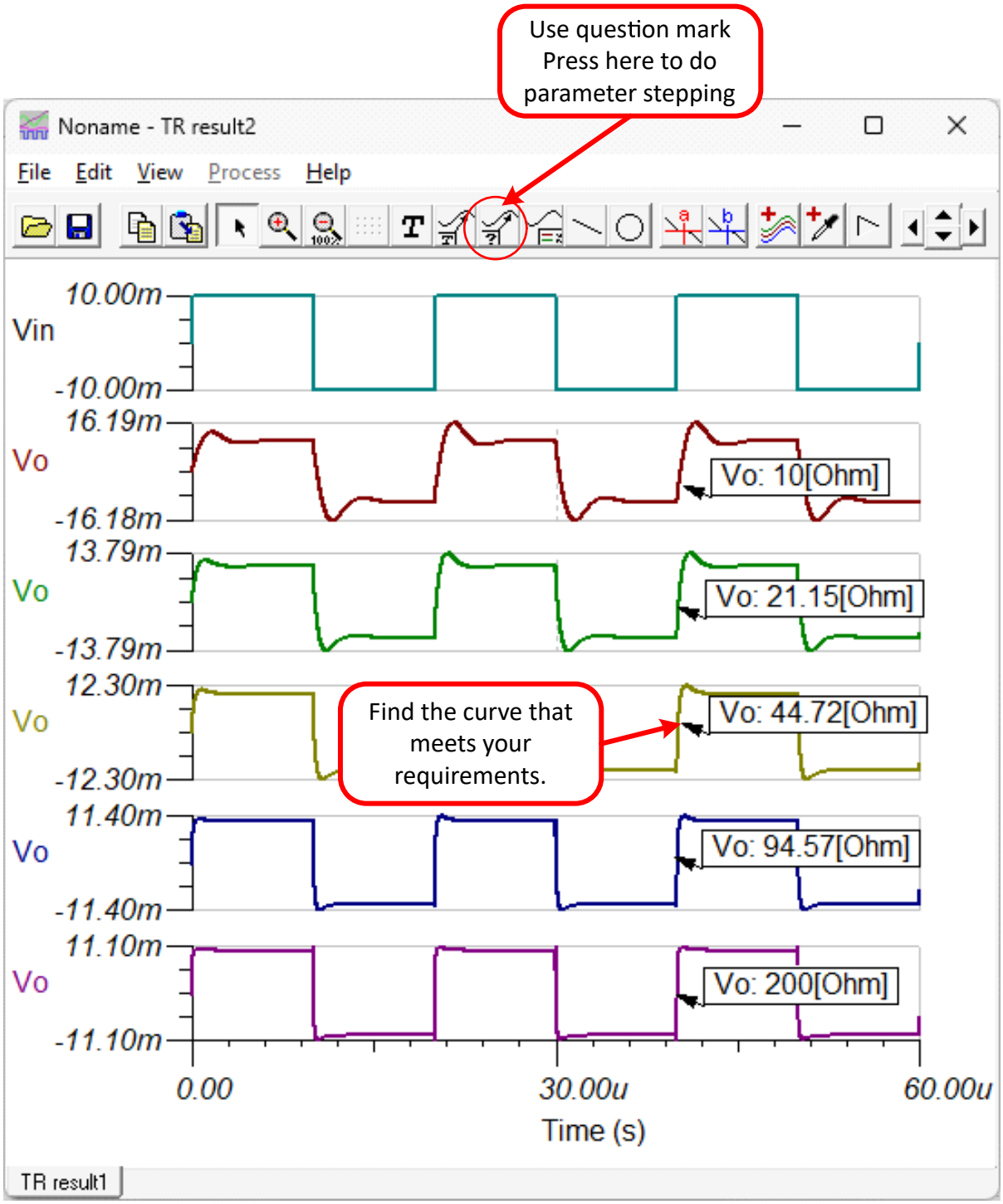


**Figure 6-18. Parameter Stepping $R_{ISO}$ Transient Results**

## 6.4 Impact of Internal Op Amp Topology on Output Impedance Versus Frequency

In Figure 6-19, the low value, resistive open-loop output impedance is the easiest to understand, predict, and compensate. If the value of $Z_O$ is large, then the value of the isolation resistance must be larger than what is required for a low value of $Z_O$. If $Z_O$ is complex, then $Z_L$ can interact with $Z_{OUT}$ to create a resonance. A common question is—why do IC designers not *always* design op amps with low value resistive $Z_O$? The answer is simply that there are design tradeoffs that lead to output impedances that are not adequate from a stability perspective. This section provides insight into what these tradeoffs are. From a board-and-system level design perspective, understanding the tradeoffs is not critical because as long as $Z_O$ is known, engineers can choose the external

compensation components to correct the stability issue. Nevertheless, some understanding of the IC design tradeoffs provides insight into the op amp selection process.

Figure 6-19 illustrates the bipolar emitter follower output stage and the associated $Z_O$ curve. This internal output stage design is used in many older generations op amps and some modern op amps. The topology provides a low and flat output impedance curve, from a stability perspective, this topology is better. The output impedance is $Z_O = (1/g_m)||(1/g_m)$ for the output transistors. The disadvantage of this approach is that the output swing-to-supply-rail is limited by 1V or more. Modern amplifiers generally use a rail-to-rail output structure, which does not have a flat response over frequency (see Figure 6-20).

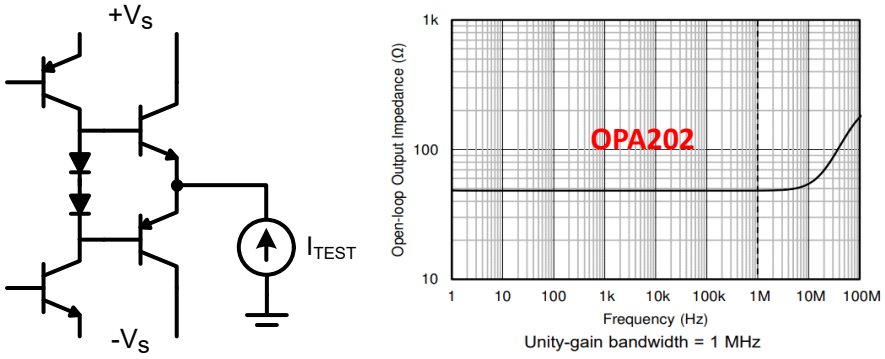


**Figure 6-19. Bipolar Emitter Follower Output**

Figure 6-20 shows the two-stage Miller compensated amplifier. This topology uses a rail-to-rail output stage. The output impedance of the rail-to-rail topology ($R_2$) is higher than the emitter follower, and this impedance dominates at low frequency. At higher frequency, the test signal $I_{TEST}$ applied to output feeds back through the Miller capacitance ($C_m$) to the input of the output stage which is then amplified by $g_{m2}$. This feedback causes $Z_O$ to drop to $1/g_{m2}$. Equation 91 illustrates a simplified equation for $Z_O$ of Figure 6-20. Note that the increase in $Z_O$ at low frequency is not generally a problem as the rate-of-closure issues associated with $Z_{OUT}$ normally happen at high frequencies (see Impact of Internal Op Amp Topology on Output Impedance Versus Frequency).

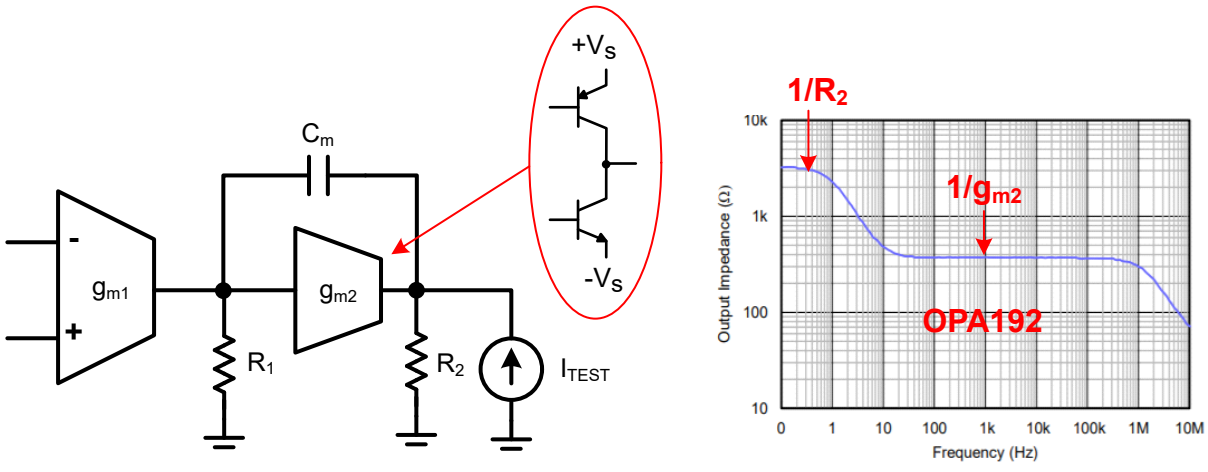


**Figure 6-20. Two-Stage Miller Compensated Amplifier**

$$Z_O \cong \frac{R_2(1 + s \times C_m \times R_1)}{1 + s \times C_M(R_1 + R2 + g_{m2} \times R_1 \times R_2)} \quad (91)$$

Figure 6-21 illustrates the three-stage cascaded Miller with feed-forward. Most chopper amplifiers use this internal topology due to the separate high frequency path and chopped path. This topology has multiple poles and zeros due to the multiple feedback paths. Equation 92 is an approximation for the output impedance of Figure 6-21. As discussed in Instability Due to Resonance From Complex Output Impedance, this is the most challenging $Z_O$ to stabilize. Chopper amplifiers have many excellent benefits related to the calibration of input

offset voltage ($V_{OS}$). One disadvantage is that chopper amplifiers are more challenging to stabilize and often require large values of $R_{ISO}$ for good stability. See Optimizing Chopper Amplifier Accuracy for details on chopper amplifiers.

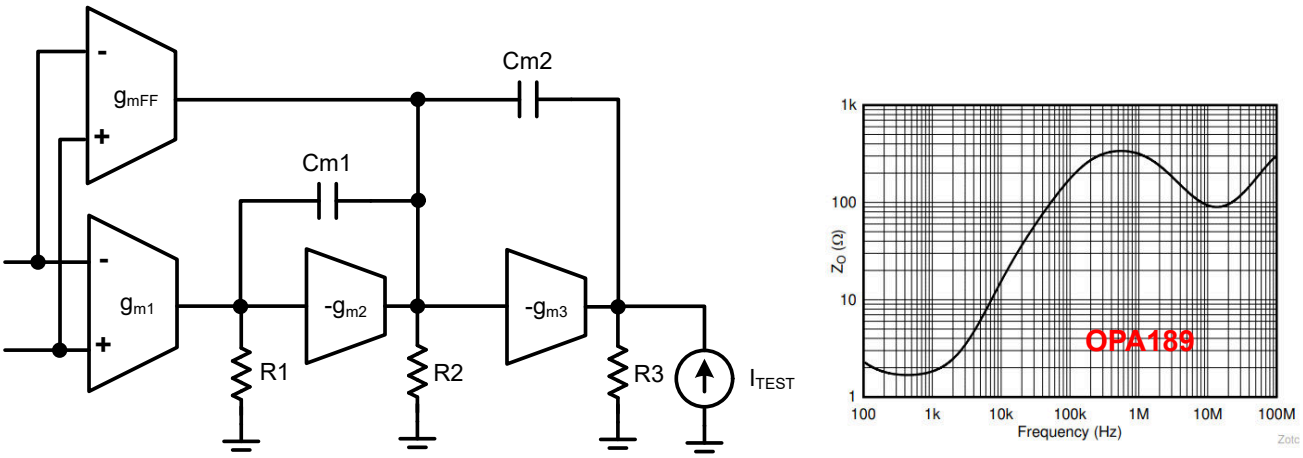


**Figure 6-21. Three-Stage Cascaded Miller With Feed-Forward**

$$Z_O \cong \frac{R_3(1 + s \times C_{m2} \times R_2)(1 + s \times C_{m1}(R_1 + R_3))}{\left(1 + s \times C_{m1} \times R_1 \times g_{m2} \times R_2 \times g_{m3} \times R_3\right)\left(1 + \frac{s \times C_{m2}}{g_{m2}}\right)} \quad (92)$$

There are other amplifier output topologies beyond what is shown in this section. One key point of this section is that emitter follower and source follower amplifiers with output swing limitations are generally the better choice from a stability perspective. Another point is that when selecting op amps to drive capacitive loads, inspect the $Z_O$ curve for impedance flatness and magnitude. Ultimately, any amplifier can be stabilized, but the magnitude of $R_{ISO}$ can be unacceptable for some complex output impedances.

## 6.5 Other Factors Effecting Output Impedance

The open-loop output impedance curve given in most op amp datasheets is a typical value. The datasheet typical value is also used in the op amp model. The $Z_O$ typical measurement was made at room temperature, with typical power supplies and load conditions. Factors such as output current, temperature, supply voltage, and process variations can cause $Z_O$ to change. Most datasheets do not provide estimates for worst case $Z_O$, so targeting a conservative phase margin that remains stable even with some variation in $Z_O$ is advisable. This is why TI generally recommends a minimum phase margin of 45° even though 35° can potentially provide an acceptable transient response. Thus, if you design the circuit to a phase margin of 45°, across process and temperature the phase margin can potentially vary from 40° to 50°, which is generally acceptable.

Figure 6-22 illustrates how load current (amplifier output current) shifts $Z_O$ for OPA376. In general, $Z_O$ decreases for higher load current. Generally, the $Z_O$ curve in the datasheet is measured with minimal load current (large $R_L$). For heavy loads (small $R_L$), $Z_O$ decreases, which generally improves stability. Some amplifier datasheets, such as OPA376, show $Z_O$ for multiple different loads to show how $Z_O$ changes with load current.

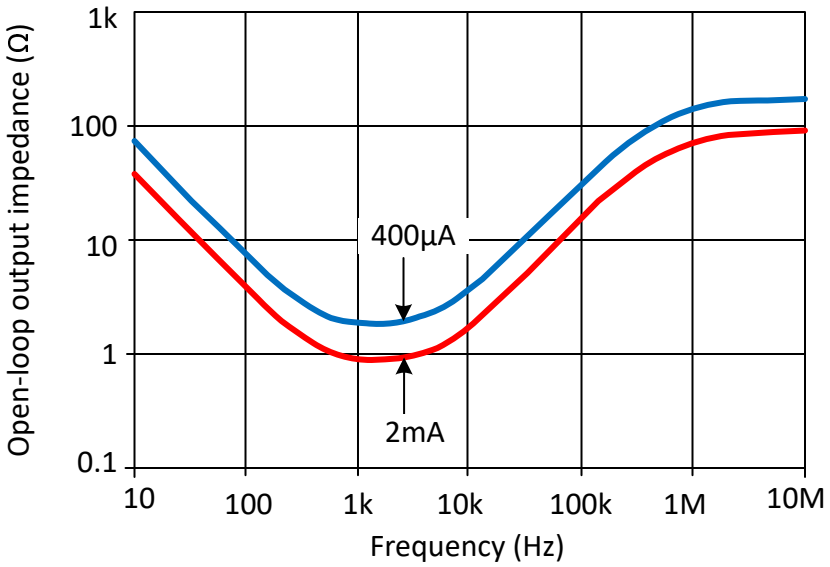


**Figure 6-22. Open-Loop Output Impedance Versus Load Current for OPA376**

Figure 6-23 illustrates an example of how $Z_O$ changes across temperature for PGA900. The PGA900 is used in the next few examples because the open-loop output impedance of PGA900 is characterized over a wide range of conditions that most devices are not tested under. While each amplifier has different characteristics and sensitivities, the PGA900 data provides a rough idea of what to expect. Figure 6-23 shows that temperature has a more significant effect at lower frequencies. In most circuits with stability concerns, the high frequency $Z_O$ determines the amplifier stability and low frequency $Z_O$ is not important. In this example, the curves are relatively tightly grouped past 10kHz ($\Delta Z_O$(1MHz) ≅ ±20%).

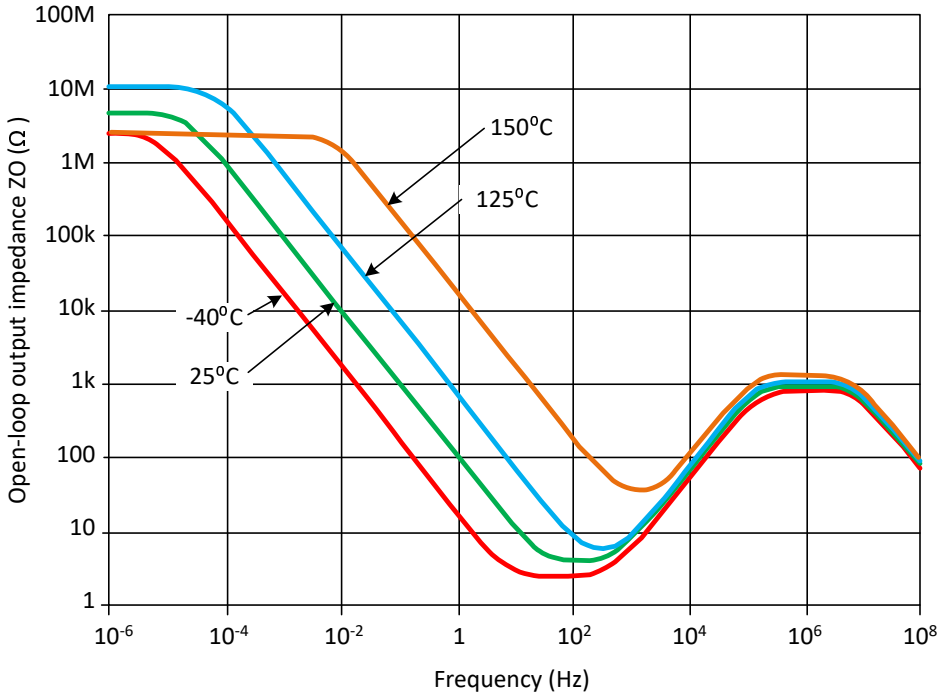


**Figure 6-23. Open-Loop Output Impedance Versus Temperature for PGA900**

The variation in $Z_O$ versus power supply voltage for PGA900 is really negligible (see Figure 6-24). This makes sense as op amps use internal biasing schemes that keep the bias current for the different internal blocks constant versus power supply voltage.

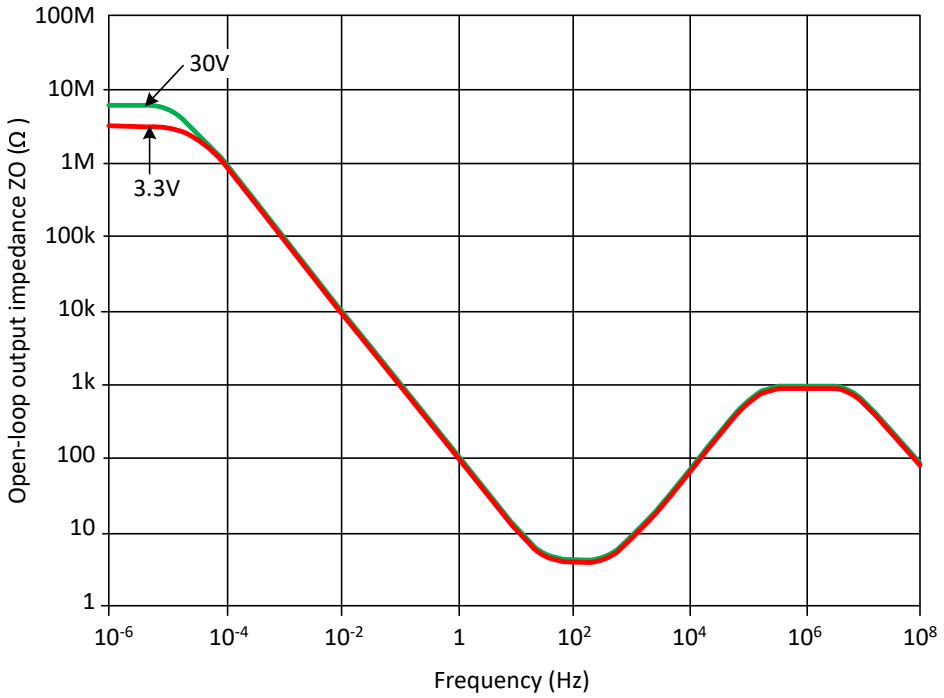


**Figure 6-24. Open-Loop Output Impedance Versus Supply Voltage for PGA900**

Figure 6-25 shows the process variation of $Z_O$ for PGA900. The data was collected for multiple different devices across multiple lots and the curves represent the worst-case deviations. As with other curves in this section, the variations at high frequency are not that significant, so the overall impact on stability is not that significant.

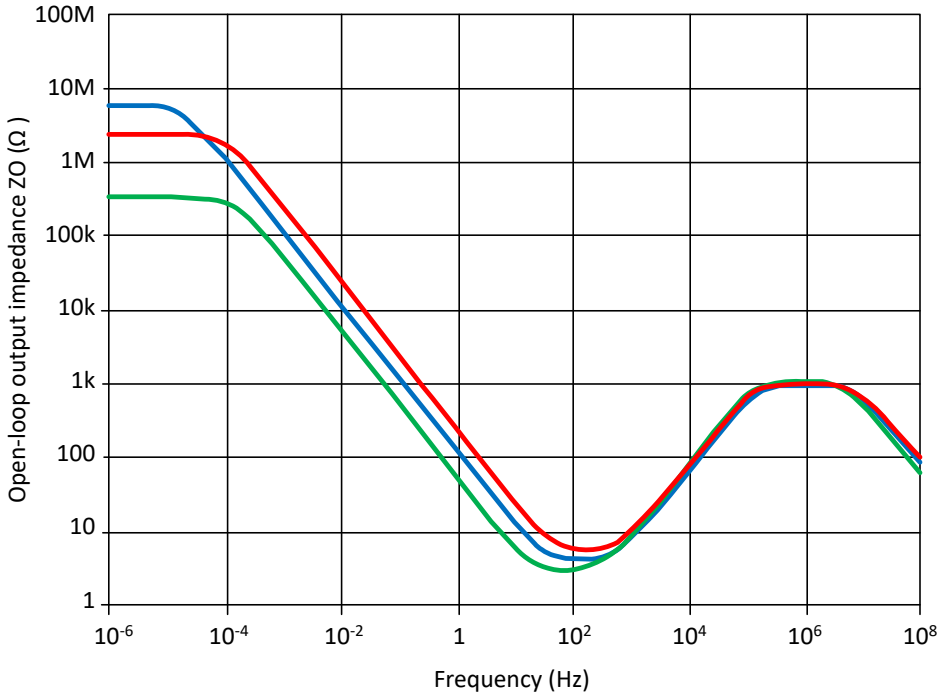


**Figure 6-25. Open-Loop Output Impedance Versus Process for PGA900**

Figure 6-26 and Figure 6-27 illustrate the importance of decoupling for stability of op amps. Figure 6-26 shows the test circuit for measuring $Z_O$. The circuit has a source impedance in the amplifier power supplies labeled $R_{PS}$. This can be an inductive reactance, but for simplicity a resistance was used. With decoupling capacitors $C_2$ and $C_3$ installed, the power supply resistance is effectively shorted out from an AC perspective. If the decoupling

is omitted, the resistance $R_{PS}$ effectively adds to the open-loop output impedance $Z_O$. This is why improper decoupling or lack of decoupling often leads to op amp instability. Figure 6-27 illustrates measured $Z_O$ for OPA827 with the decoupling removed and resistor $R_{PS}$ added to the supply. Inspecting the graph shows that the source resistance increases the open-loop output impedance. The key point here is that this measurement was made without decoupling capacitors. Adding the decoupling effectively shorts out RPS so that all the $Z_O$ values match the original $Z_O$ regardless of $R_{PS}$. Thus, decoupling capacitors are very important from a stability perspective. Use a minimum of 0.1µF decoupling with short connections between the amplifier supply pins and ground for good stability.

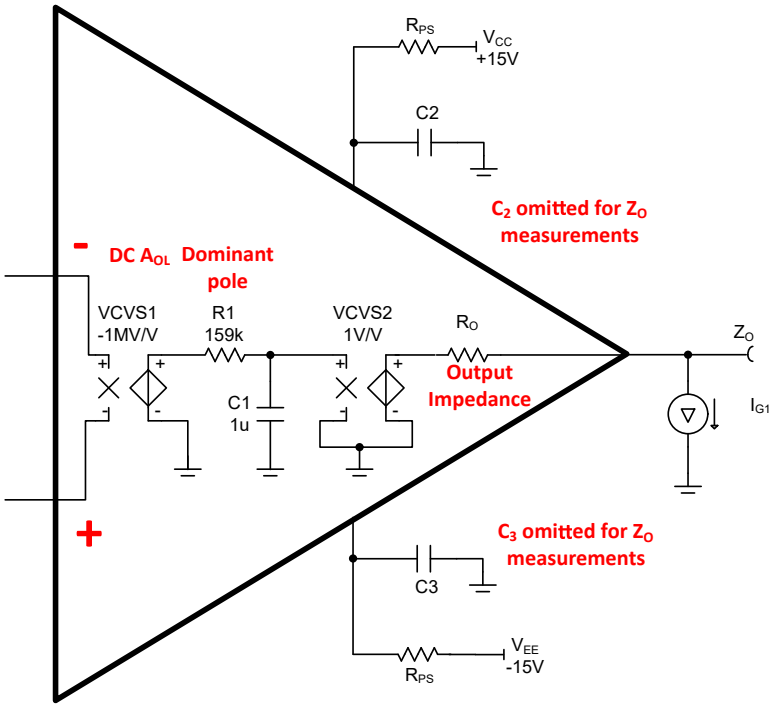


**Figure 6-26. Open-Loop Output Impedance Test Versus Source Impedance and Decoupling**

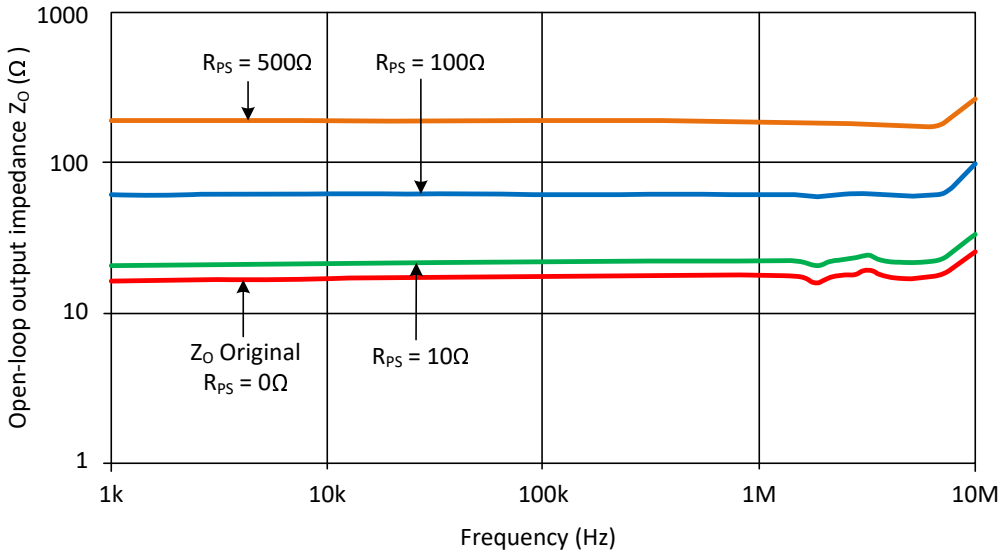


**Figure 6-27. Open-Loop Output Impedance Versus Supply Impedance for OPA827**

The intention of this section is to emphasize that process, load, temperature, and decoupling all impact $Z_O$ and stability. Since most amplifier data sheets and associated SPICE models use the typical value for $Z_O$, having a

design target for phase margin that is conservative is important so that the circuit remains stable across process and temperature. This is really the motivation behind the 45° general guidance.

# 7 $A_{OL}$ Impact on Stability

This section covers details on how the internal compensation of op amps can shape the $A_{OL}$ transfer function versus frequency. The section also introduces the decompensated op amp, and explains the minimum closed-loop gain requirements. Finally, the section explains how op amps generally tend to be more stable for higher closed-loop gain.

## 7.1 $A_{OL}$ Secondary Poles and Zeros

This section shows how the $A_{OL}$ phase droop, due to secondary poles and zeros, can degrade the overall phase margin. Figure 7-1 shows the open-loop gain specification for OPA320. Notice that the phase drops by 90° due to the dominant pole and begins to droop below 90° at about 2MHz. The reason phase droop is below 90° is because of secondary poles and zeros from the internal op amp topology. Technically, the poles cause the phase to go below 90° and the zeros actually cause the phase to increase. However, there are more poles than zeros, which cause phase to decrease below 90° near the unity gain bandwidth. The exact placement and number of poles and zeros depend on the op amp internal topology, and these details are not published. Fortunately, op amp models released by Texas Instruments include the poles and zeros in the model so that the $A_{OL}$ gain and phase response accurately models the real device.

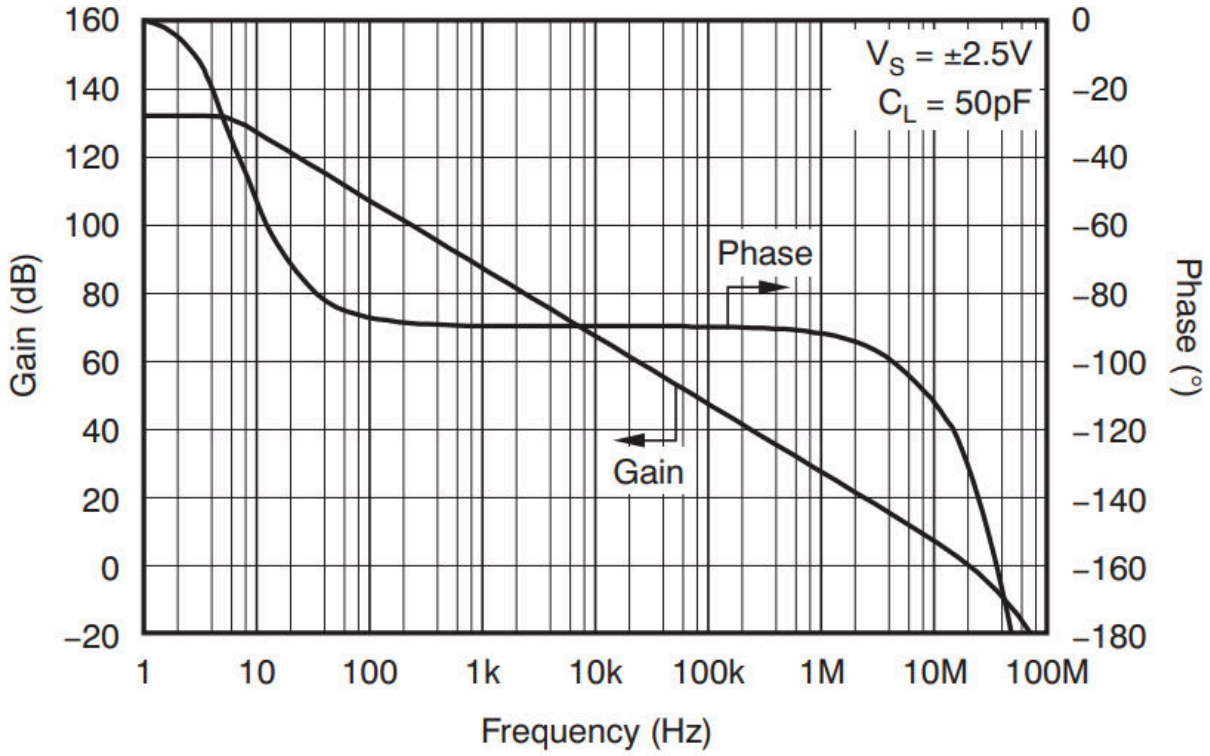


**Figure 7-1. Open-Loop Gain Specification From OPA320 Datasheet**

As mentioned, the TI models accurately model the phase droop near the unity gain bandwidth of the op amp. A good practice is for engineers to practice using the released model for stability analysis. However, for illustrative purposes a simplified single-pole model is used. In this instance, single-pole means that the model only models the dominant pole and ignores the secondary poles and zeros. Figure 7-2 shows the open-loop gain and phase response for the single pole model with no capacitive load (for example, $C_L$ = 0F). Notice that the phase drops to 90° because of the dominant pole but does not drop below 90° as this model does not have the secondary poles and zeros.

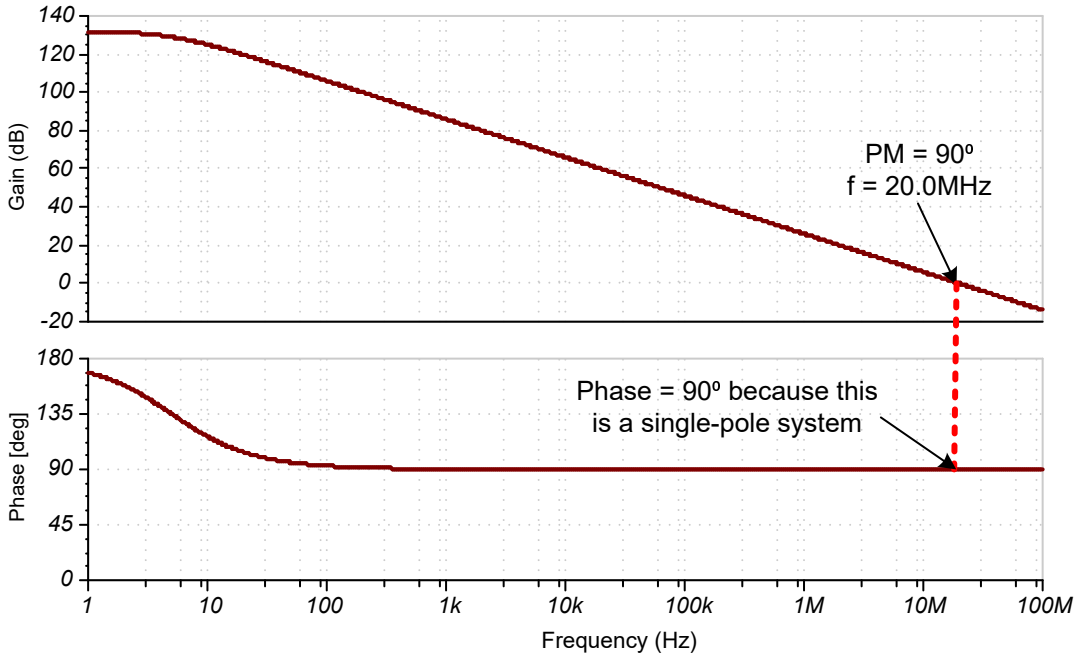


**Figure 7-2. $A_{OL}$ on Single-Pole Model of OPA320 With $C_L$ = 0pF**

Figure 7-3 illustrates the single-pole OPA320 model with a 100pF load. In this case, the capacitive load adds a second pole in $A_{OL}$, as was discussed in Isolation Resistor ($R_{ISO}$) Method. The phase margin drops from 90° to 49.4° due to the capacitive load. The results for the single-pole model are compared to the Texas Instruments' OPA320 released model to illustrate the impact the secondary poles have on stability.

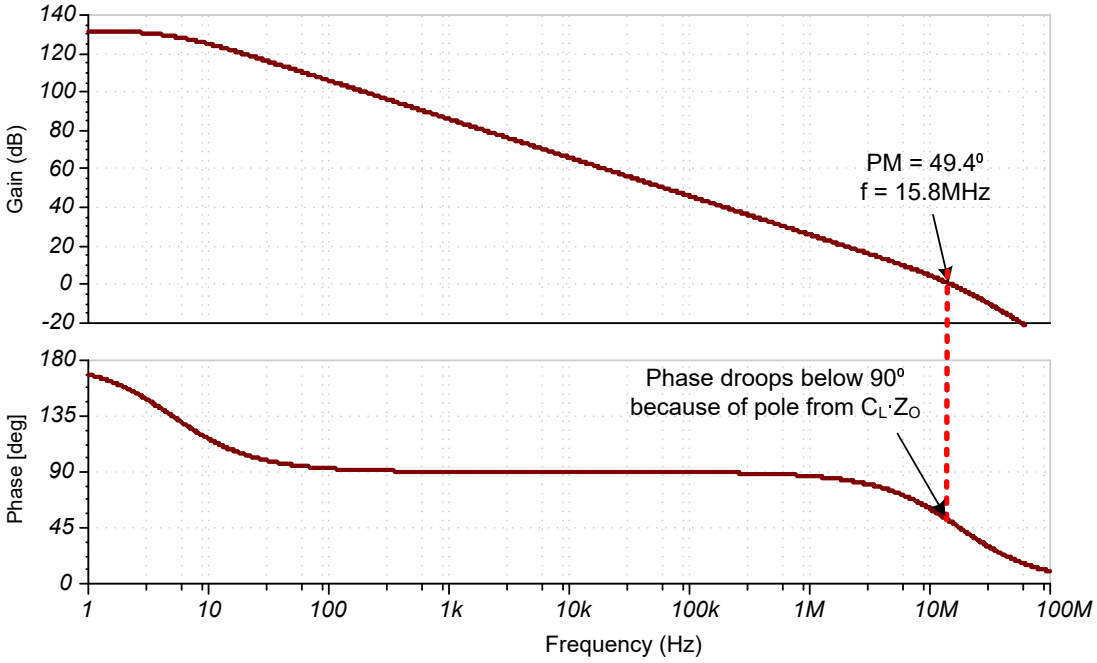


**Figure 7-3. $A_{OL}$ on Single-Pole Model of OPA320 With $C_L$ = 100pF**

Figure 7-4 illustrates the Texas Instruments' released OPA320 model $A_{OL}$ response with $C_L$ = 0pF. Inspecting the $A_{OL}$ response shows the phase roll-off at high frequency due to the secondary poles. The phase margin is 80.9°, so approximately 9.1° of phase is lost due to the secondary poles. When the capacitive load is added, this phase loss adds to the phase loss due to the capacitive load.

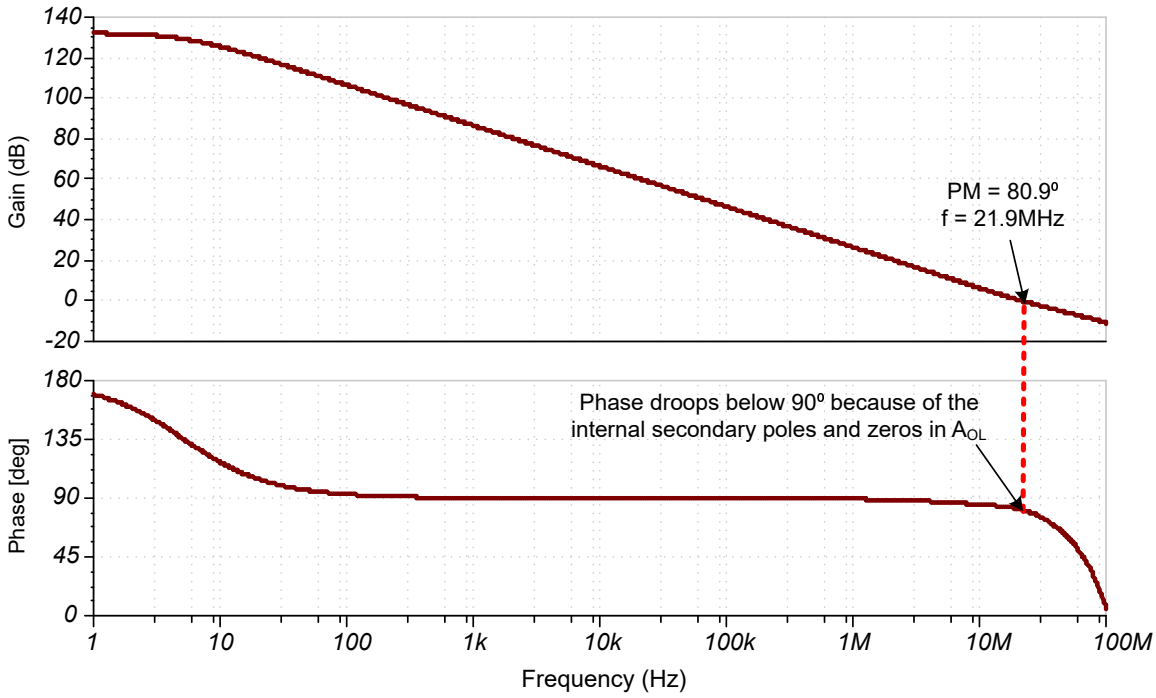


**Figure 7-4. $A_{OL}$ on Texas Instruments' Released OPA320 Model With $C_L$ = 0pF**

Figure 7-5 shows the OPA320 model $A_{OL}$ response with $C_L$ = 100pF. The phase margin in this case is 36.1°, whereas the single-pole model under the same circumstance has a phase margin of 49.4°. The reason for the difference between the single-pole and released models is the secondary poles and zeros in the released model. Recall that the single pole has a phase margin of 90° and the released model has a phase margin of 80.9º with $C_L$ = 0F. The phase droop of 9.1° degrees approximately added with the phase droop from the capacitive load to further degrade the phase margin. The phase margin is a factor of the secondary poles and zeros in AOL as well as the capacitive load. In fact, the open-loop output impedance also impacts phase margin as was discussed in Complex Open-Loop and Closed-Loop Output Impedance. Ultimately, the point here is to emphasize the importance of using an op amp model that properly models $A_{OL}$. Also, this section shows why the phase margin is sometimes less than expected based on a theory that assumes a single-pole op amp response.

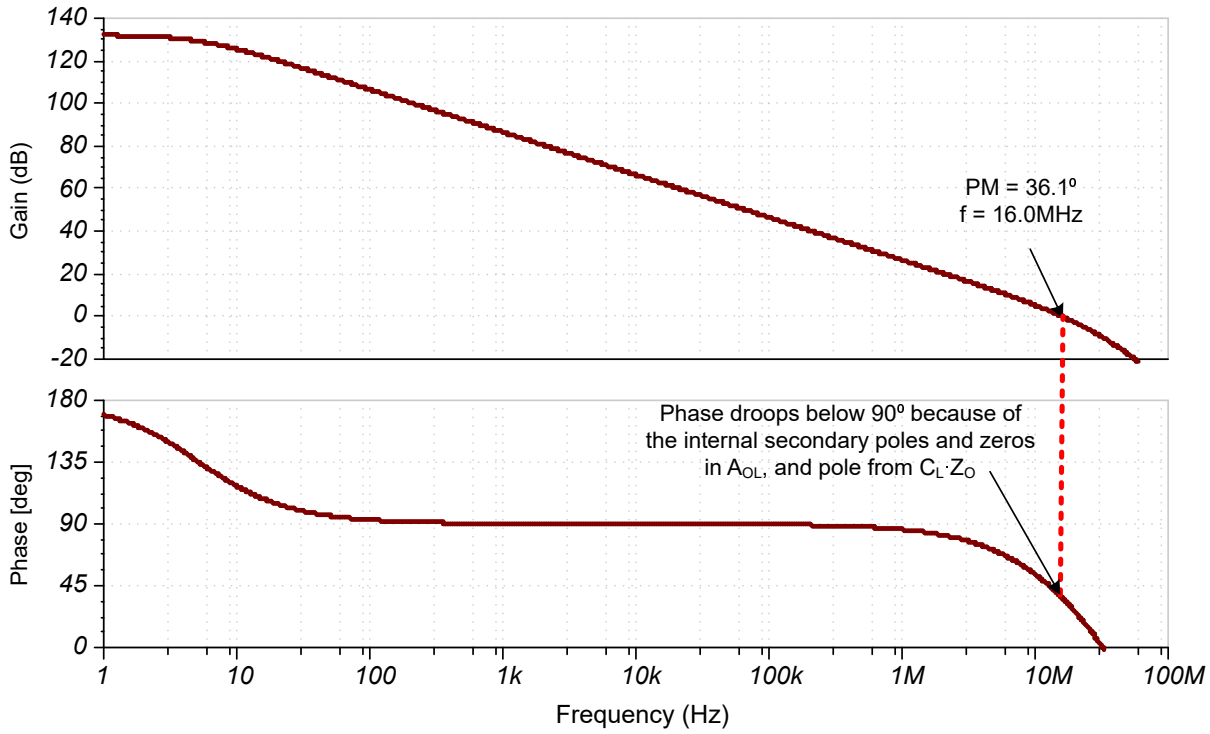


**Figure 7-5. $A_{OL}$ on Texas Instruments' Released OPA320 Model With $C_L$ = 100pF**

## 7.2 Modeling the $A_{OL}$ Secondary Poles and Zeros and Input Capacitance

Figure 7-6 shows an op amp model that covers the input capacitance, DC $A_{OL}$, the dominant pole, a secondary pole, and output impedance for OPA320. Notice that a voltage-controlled-voltage source in a gain of 1V/V is used between the different filter stages to isolate the stages from each other. The DC AOL is calculated based on data sheet information using Equation 93. The dominant pole frequency is calculated with Equation 94, and the resistance is calculated with Equation 95. The secondary pole frequency is calculated by looking at the phase response in the data sheet AOL plot (see Figure 7-1). Recall that a pole causes phase to start shifting about one decade before the pole and stop shifting one decade after the pole. Inspecting Figure 7-1 shows that phase is starting to shift at about 2.5MHz, so the pole is located at about 25MHz. Equation 96 selects the components for the second pole. The output impedance for OPA320 is a flat 90Ω across frequency so a simple 90Ω can be used for the model.

$$A_{OL(DC)} = 10^{(A_{OL}/20)} = 10^{(132/20)} = 3.981 \times 10^{6} \quad (93)$$

$$f_{DOM} = \frac{GBW}{10^{(A_{OL}/20)}} = \frac{20MHz}{10^{(132/20)}} = 5.024Hz \quad (94)$$

$$R_1 = \frac{1}{2 \times \pi \times f_{DOM} \times C_1} = \frac{1}{2 \times \pi \times (5.024Hz) \times (10\mu F)} = 3.168k\Omega \quad (95)$$

$$R_2 = \frac{1}{2 \times \pi \times f_{SEC} \times C_2} = \frac{1}{2 \times \pi \times (25MHz) \times (2pF)} = 3.183k\Omega \quad (96)$$

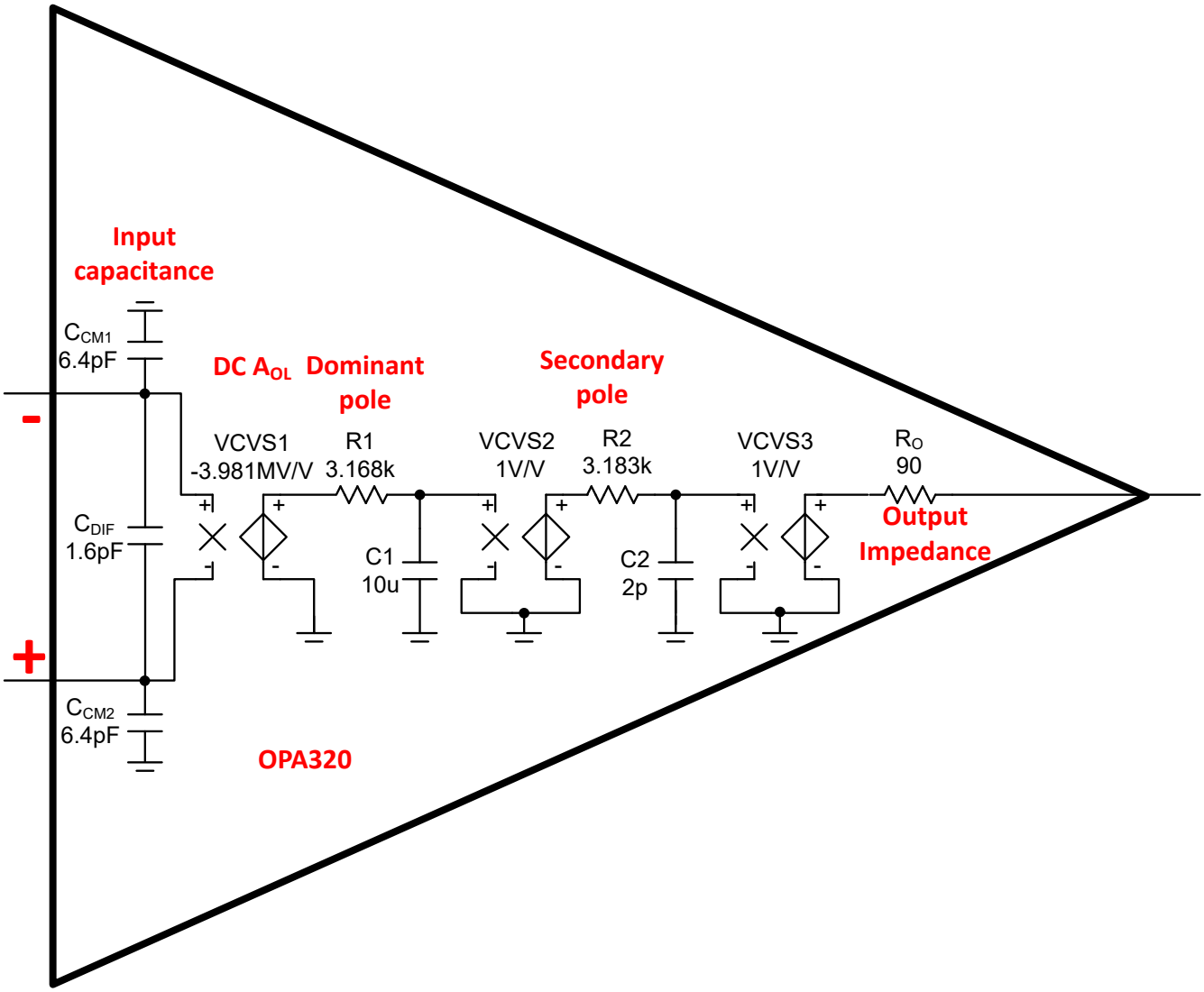


**Figure 7-6. Op Amp Model With Secondary Pole and Input Capacitance (OPA320)**

Figure 7-7 illustrates the open-loop response for Figure 7-6. Notice that the dominant pole introduces a 90° phase shift and the second pole introduces additional phase shift near the unity gain bandwidth. This model is really an approximation as the actual device has multiple poles and a zero at high frequencies, but the specific details on the poles and zeros is not published. Ultimately, using the published models is better because these models accurately model these secondary effects. However, in cases where the model is not available this approach can be used.

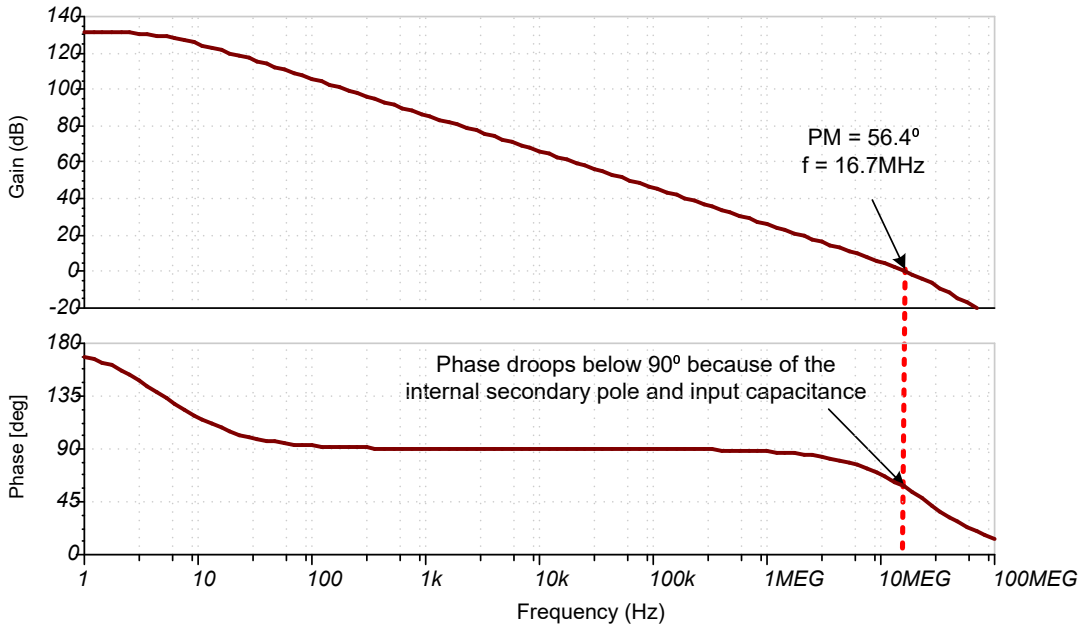


**Figure 7-7. Open-Loop Response for Two-Pole OPA320 Model**

## 7.3 Decompensated Op Amps and Stability

Some operational amplifiers are not stable in unity gain. That is, the op amps oscillate if configured in a buffer configuration (G = 1V/V). The reason for this instability at low gains is that there is a second pole in $A_{OL}$ below the unity-gain bandwidth. This second-pole is internal and behaves the same way as the second pole introduced from a capacitive load (see Isolation Resistor ($R_{ISO}$) Method). These types of amplifiers are called decompensated amplifiers, because these amplifiers lack the internal compensation required for unity gain stability. The reason that decompensated op amps are developed is because these op amps have higher gain bandwidth products than comparable compensated amplifiers with equivalent power consumption. For this reason, decompensated amplifiers are generally high-speed amplifiers with bandwidths beyond 50MHz.

Figure 7-8 illustrates the open-loop response for a typical decompensated amplifier (OPA892). The secondary pole is located at approximately 200MHz. The OPA892 has a minimum gain requirement of 10V/V (20dB). The stability requirement can be understood by inspecting the AOL curve. In this example, the rate-of-closure for a gain of 1V/V is 40dB/decade and for 10V/V is 20dB/decade.

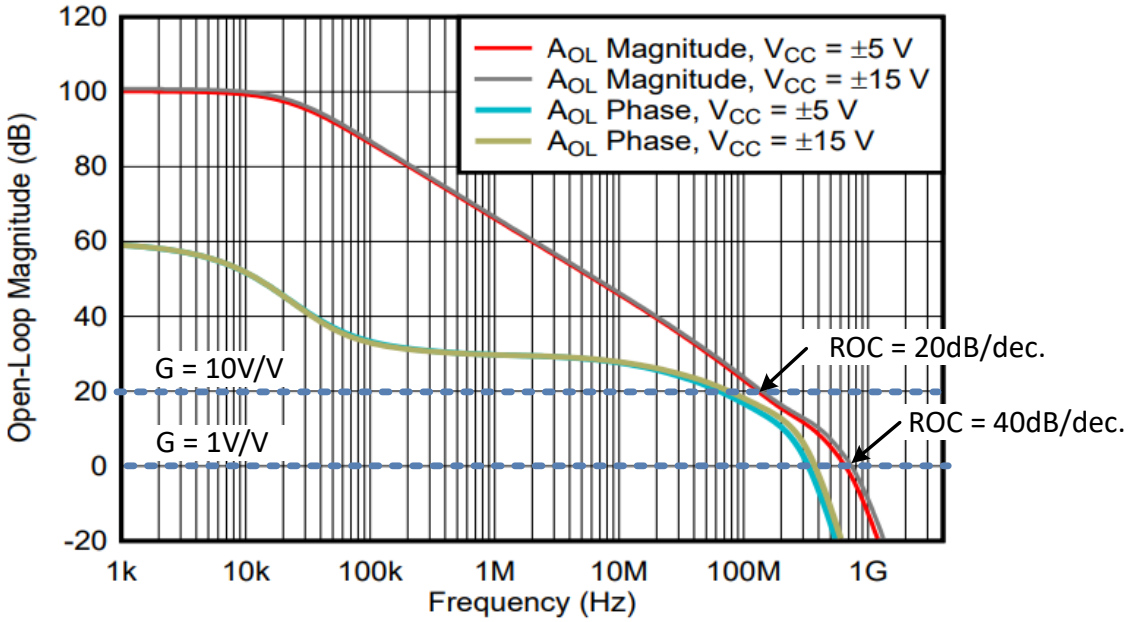


**Figure 7-8. Open-Loop Response for Decompensated Op Amp Example (OPA892)**

## 7.4 The Impact of Closed-Loop Gain on Stability

The reason capacitive load causes instability is because the $Z_O$ and $C_L$ create a second pole in $A_{OL}$ and the closed-loop gain (1/β) intersects the $A_{OL}$ curve at a rate-of-closure of 40dB/decade. For higher closed-loop gain, the 1/β curve intersects the $A_{OL}$ curve above the secondary pole for a rate of closure of 20dB/decade (see Figure 7-9). Thus, for stability issues due to capacitive load, higher gains generally improve stability.

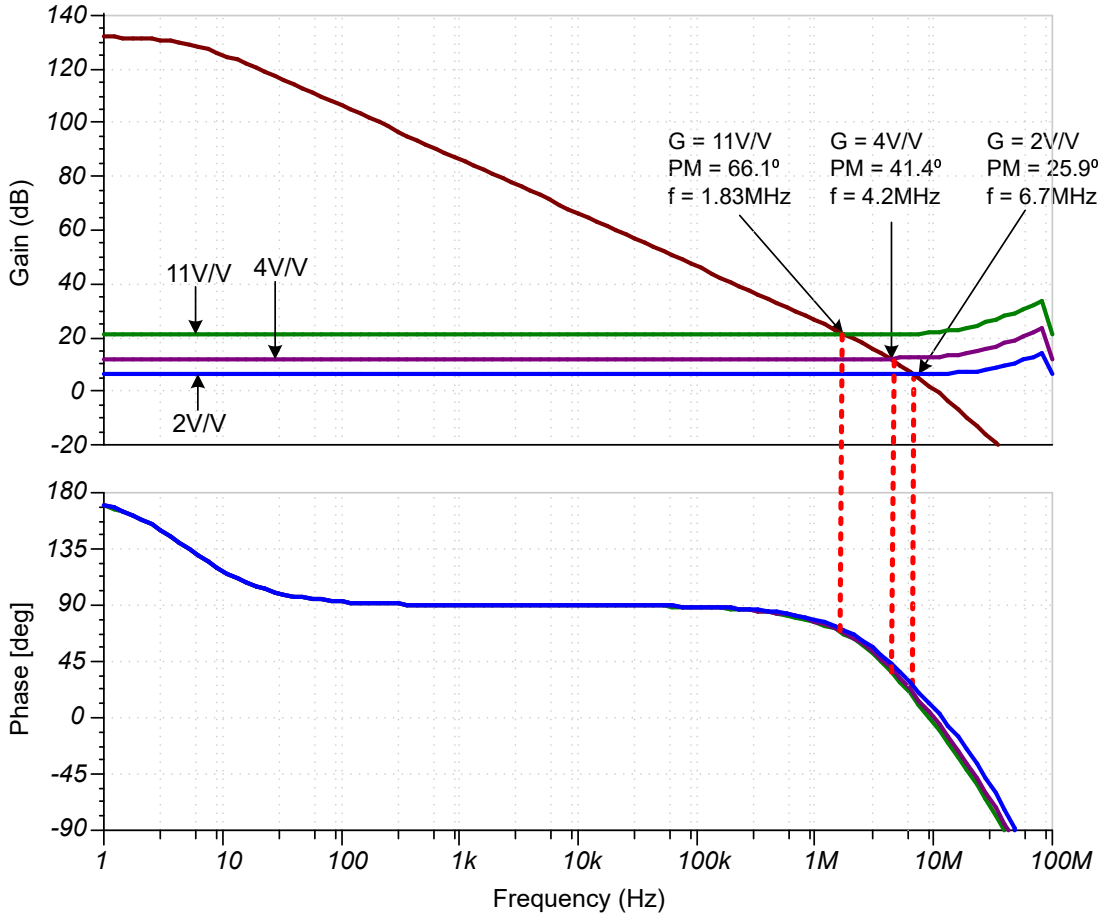


**Figure 7-9. Phase Margin Versus 1/β (gain) for Open-Loop Response (OPA320)**

Figure 7-10 illustrates the closed-loop step response for different gains. Notice that the lower gains have significantly higher overshoot. The measured overshoot versus capacitive load and closed-loop gain is frequently given in the op amp datasheet also (see Figure 7-10). The point of this section is that amplifiers in higher gain generally have a wider capacitive load range than lower gains. In fact, keeping gain low for most of the amplifier frequency range is possible, but boost gain before $A_{OL}$ intersects 1/β (see Section 4.4 for details on this method). Circuits with higher gain can also be compensated using $C_F$ compensation, as explained in Section 4.5.

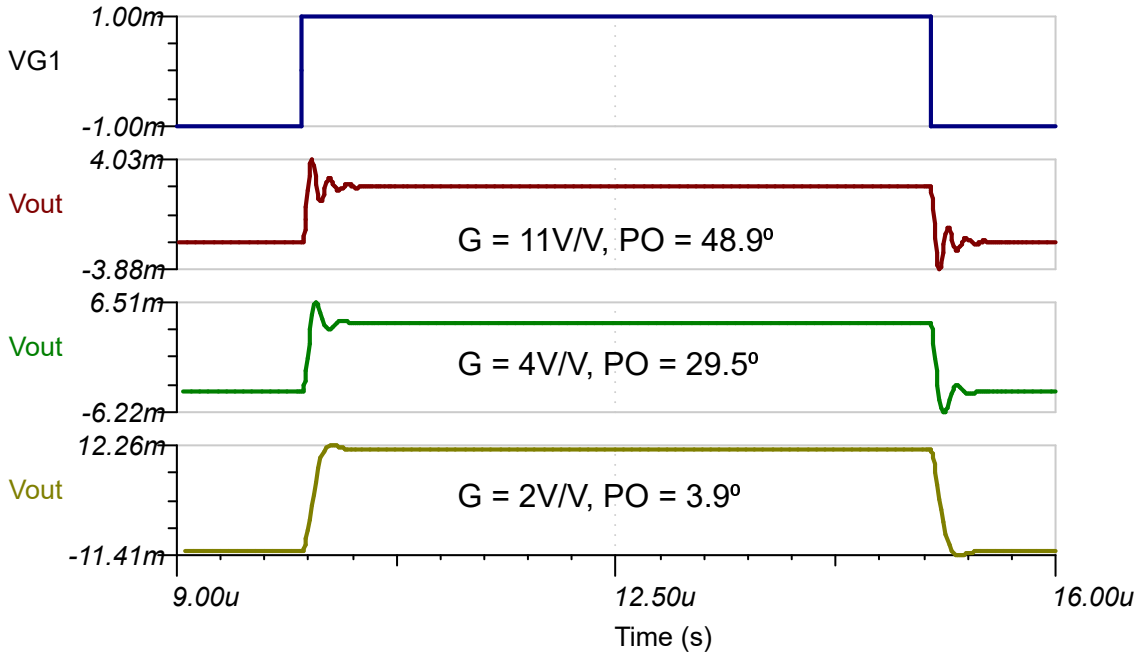


**Figure 7-10. Percentage Overshoot Versus Closed-Loop Gain for OPA320**

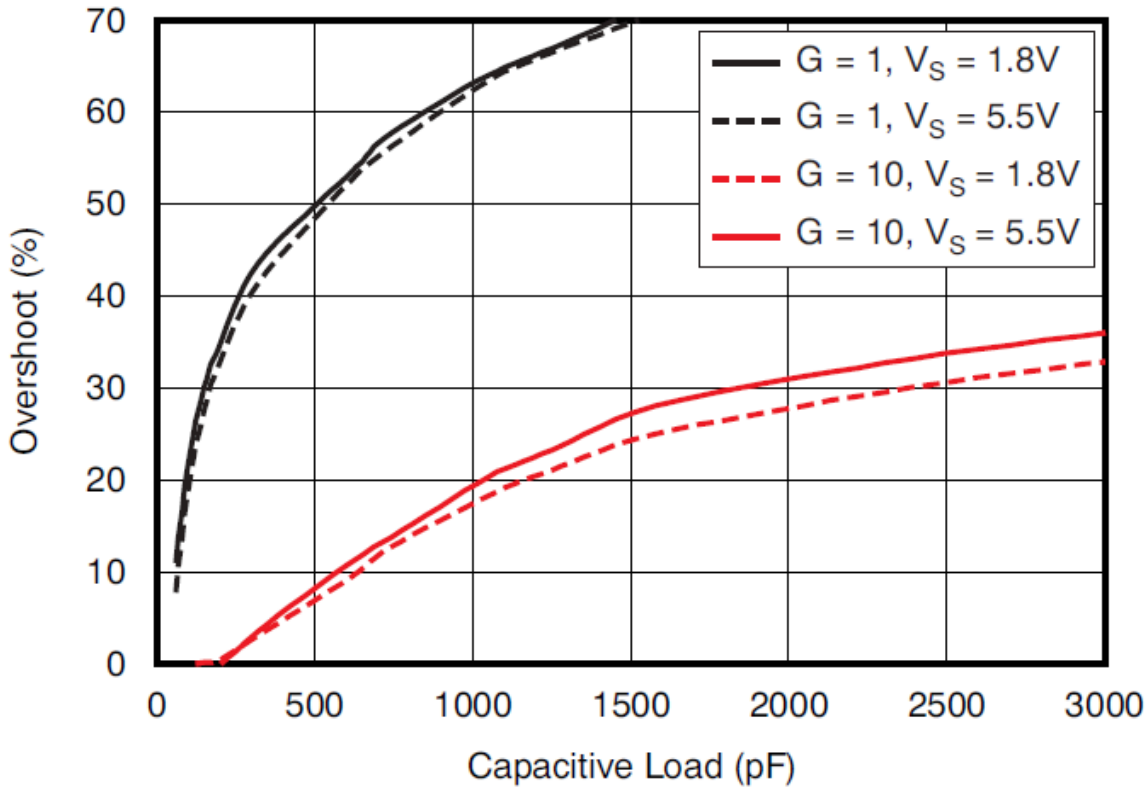


**Figure 7-11. Overshoot Versus Capacitive Load and Gain From OPA320 Datasheet**

## 8 Common Problems in Stability Analysis

Often, engineers who are new to stability analysis learn the theory and methods, but when these engineers try to apply the theory, these same individuals have issues and discrepancies that produce unexpected and incorrect results. Fortunately, many of the problems experienced by new engineers are common issues that can easily be

explained and avoided. This section covers the common stability analysis discrepancies and the way to avoid these issues.

Stability for an op amp must be tested on the amplifier output, and not at the load. A common mistake is to check the transient response at the load rather than at the amplifier output. Figure 8-1 illustrates how a small-signal step can respond with significant overshoot at the amplifier output, but can have essentially no overshoot at the load. This is because the RC load circuit has a long time constant and filters out the overshoot pulse. This problem is avoided by checking both open and closed-loop stability at the amplifiers output and not at the load.

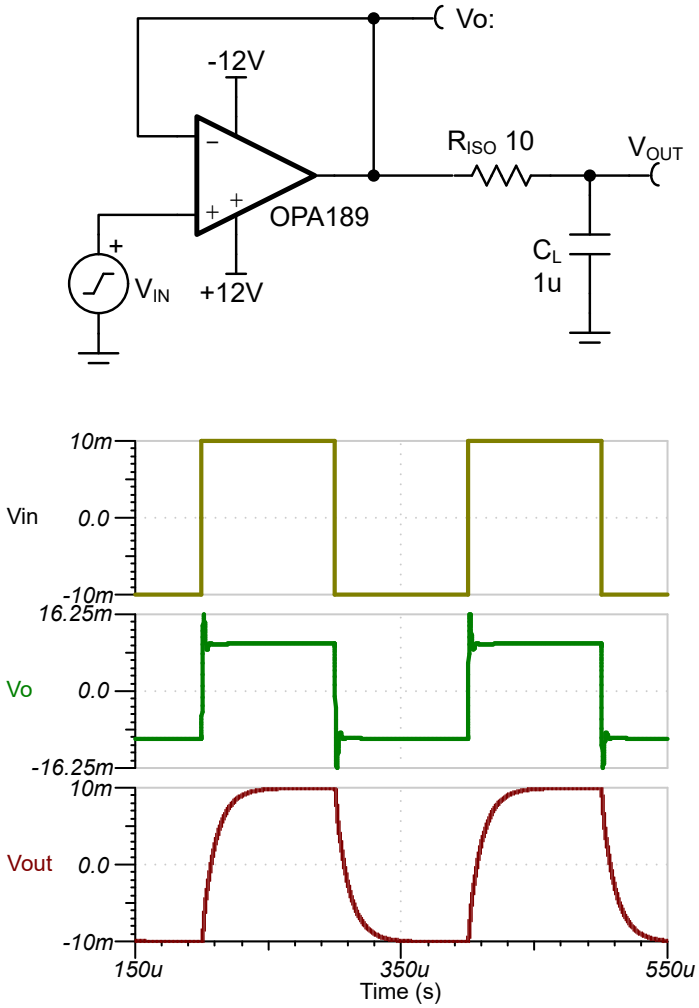


**Figure 8-1. Check the Op Amp Output for Stability, Not the Load Signal**

The most common stability test applies a small signal step to the input of the op amp. This method assumes that the input does not smooth out or filter the amplifiers input signal. The input to all op amps has common mode and differential capacitors in the picofarad range. Depending on the source impedance this input capacitance can create an RC filer that smooths out the input step. If the input step does not have the abrupt square wave rise time, the output does not respond as expected. Figure 8-2 compares an op amp circuit with a large source impedance to one with 0Ω source impedance. Note that the example device (OPA192) has 6.4pF of input capacitance. This input capacitance in conjunction with the 100kΩ source impedance smooths the edges of the input square wave. The output of the circuit with the 100kΩ source impedance does not show any overshoot, whereas, the circuit with the 0Ω source impedance shows 17.5% overshoot. The point is that applying an input step through a source impedance can smooth the edges of the step and product a transient response that implies the circuit is stable when the circuit is not. One way to avoid this issue is to always apply the step directly to the input and bypass any source impedance. Another approach is to check the output load response as in Figure 8-3.

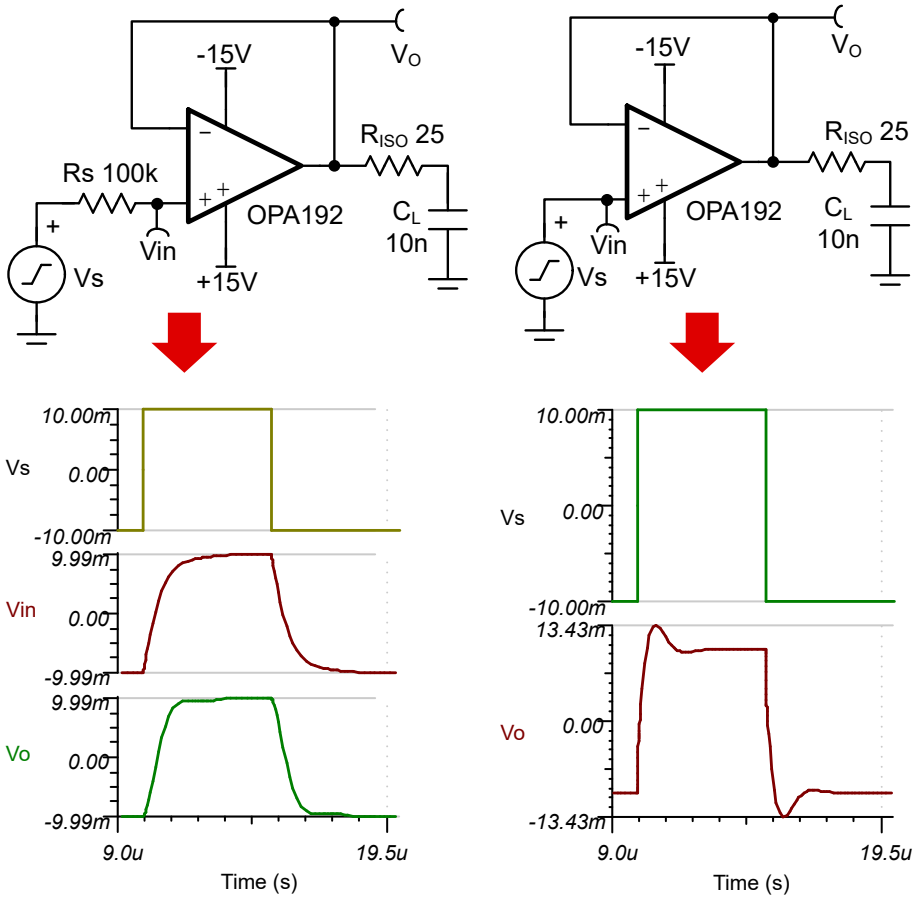


**Figure 8-2. Do Not Test Step Response Through a Large Series Resistor**

A step in the output load current can be used to test the amplifier stability the same way a small signal input step can be used. For the output step, a load current step of ±1mA is a good starting point for checking stability. Depending on the response, the step can be adjusted to be larger or smaller. The load step produces an initial large transient that corresponds to the step size and a smaller dampened oscillation that corresponds to the overshoot. The example shown in Figure 8-3 has a 21mV step size, and a corresponding 6.7mV overshoot to a ±1mA step. When choosing the load step magnitude, look for a 10mV to 20mV output step response similar to this example. The example compares the output step to an input step. While the two cases have similar results, the cases are not exactly the same. Most amplifiers have a somewhat different input and output step response. This is in part due to the fact that the circuits are not simple second order systems as the step response assumes. Rather, the circuits have complex higher order responses that have path dependencies. Since the input and output step response can be different, checking the circuit according to the expected application can be useful. For example, a SAR ADC generates a load step response, so if the circuit is used to drive a SAR ADC, look at the output step response.

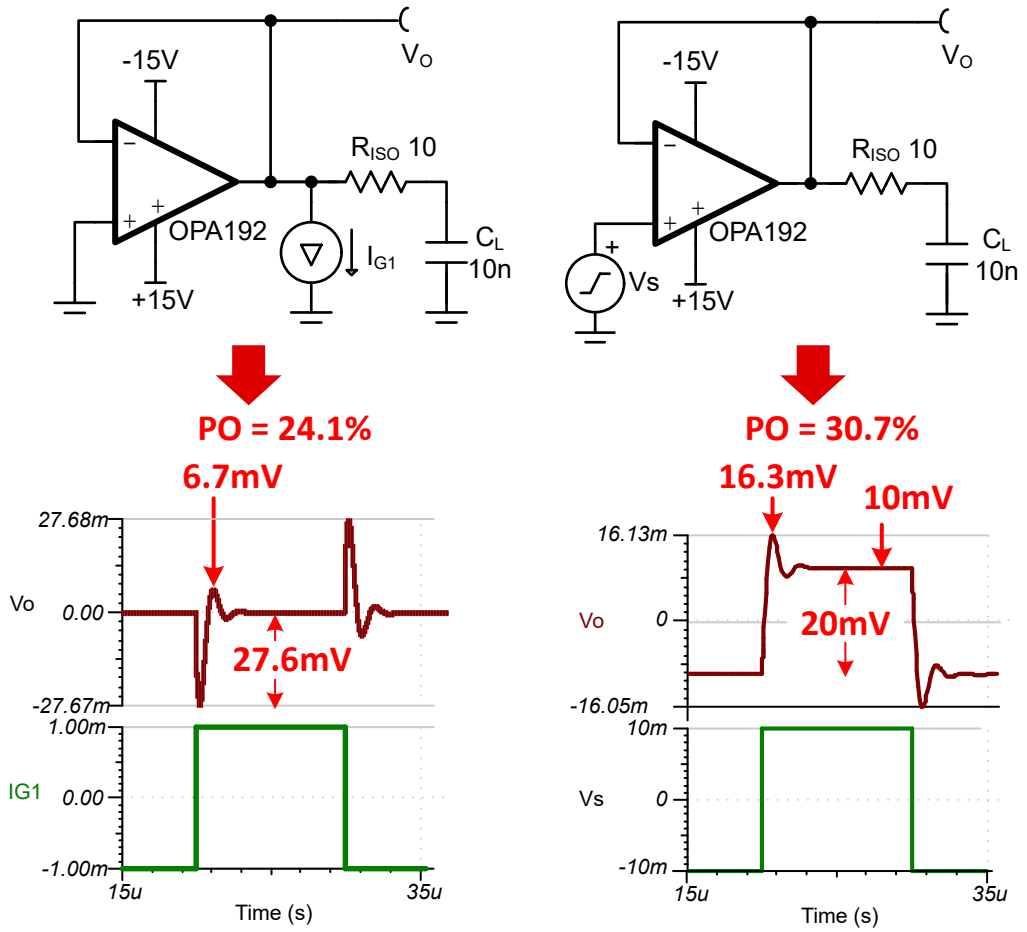


**Figure 8-3. Output Load Step for Stability Testing**

When the terms small-signal and large-signal are used in conjunction with op amps, these terms really describe the difference between linear operation and slew-rate operation. For small-signal operation, the amplifier acts like a linear system. That is, the amplifier has a small input offset voltage and the output is a linear multiple of the input signal. For large-signal operation, the amplifier is slewing so the offset is very large and the output is not a linear multiple of the input. When the amplifier slews, the output is moving at the maximum rate until the output is near the target value and then the amplifier transitions to small signal operation. A small signal step is generally considered to be 100mVpp or less. A large signal step is generally considered to be 1Vpp or more. In reality, the transition point between a large and small signal varies from device to device, so assuming a small signal is 10mVpp or less is best.

When doing stability testing, the amplifier must be in a linear operating condition (small signal). When a large signal step is applied to an op amp, most of the step response is a slew-rate or nonlinear response. At the end of the large signal step, the op amp reverts to a small signal operation. Figure 8-4 shows a ±5V large signal step and a ±10mV small signal step. For most of the large-signal step, the output is slewing, so the amplifier is not in a linear condition. At the end of the large signal step, the amplifier reverts to a small signal operation and there is an overshoot response. However, the overshoot only corresponds to the small signal portion of the step, and the percentage overshoot calculation does not reflect the system stability. In Figure 8-4, the small large-step has a PO of 2%, whereas, the small-signal has a PO of 41.9%.

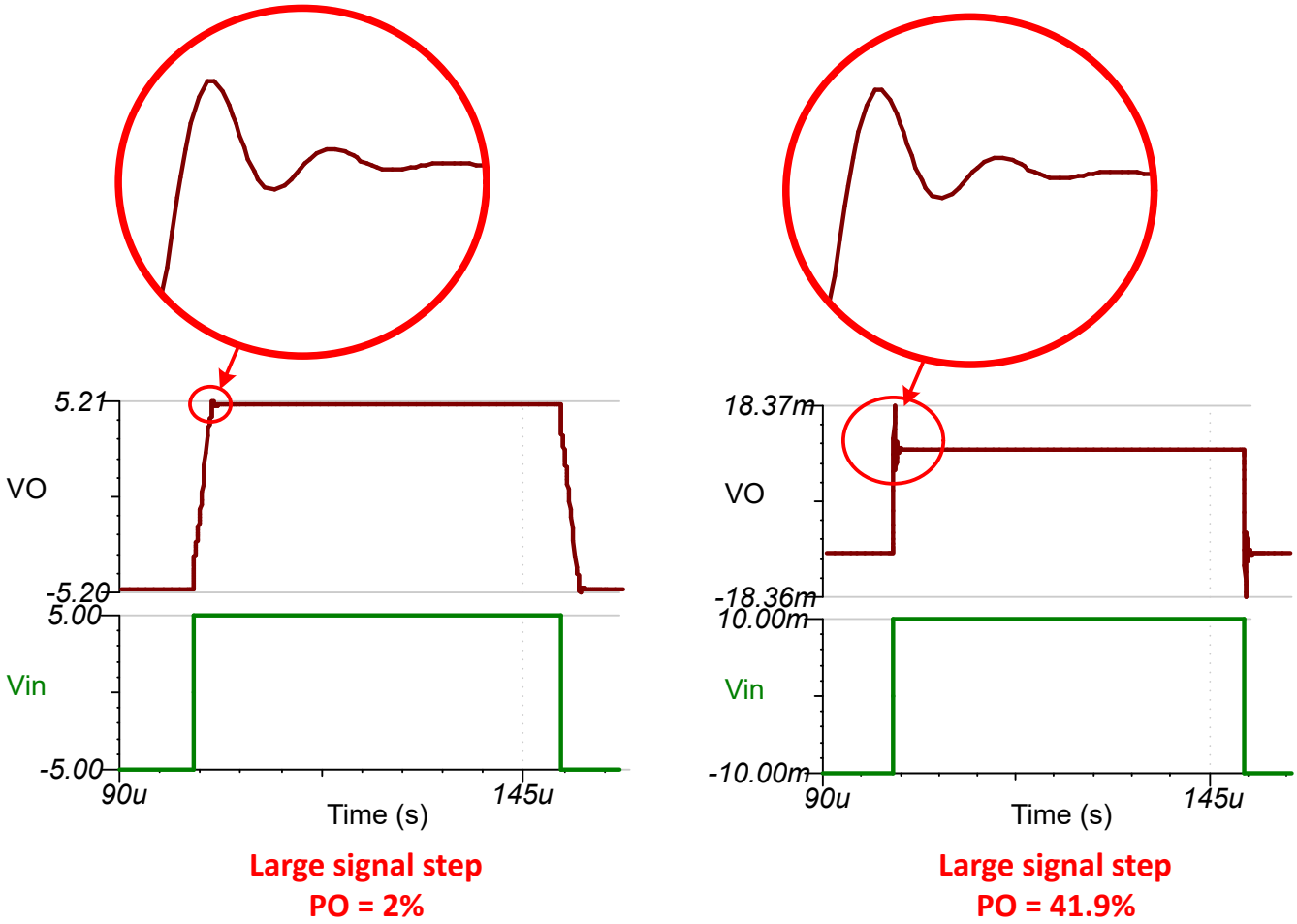


**Figure 8-4. Large Signal Versus Small Signal Step Testing**

The typical way a small signal step response is tested is to apply a small-signal repetitive square wave to the amplifier input or load. In simulation, the very first transient response is not necessarily representative of the steady state response. Most SPICE simulators allow for setting initial conditions by calculating operating point, using predefined initial conditions, or using zero initial conditions. Also, a bipolar waveform can start at zero rather than starting at the negative state. Thus, the first transient has many variables that determine the overshoot response. For accurate overshoot calculations, ignore first transient overshoot and subsequent responses. In Figure 8-5, the first transient response is significantly smaller than subsequent responses.

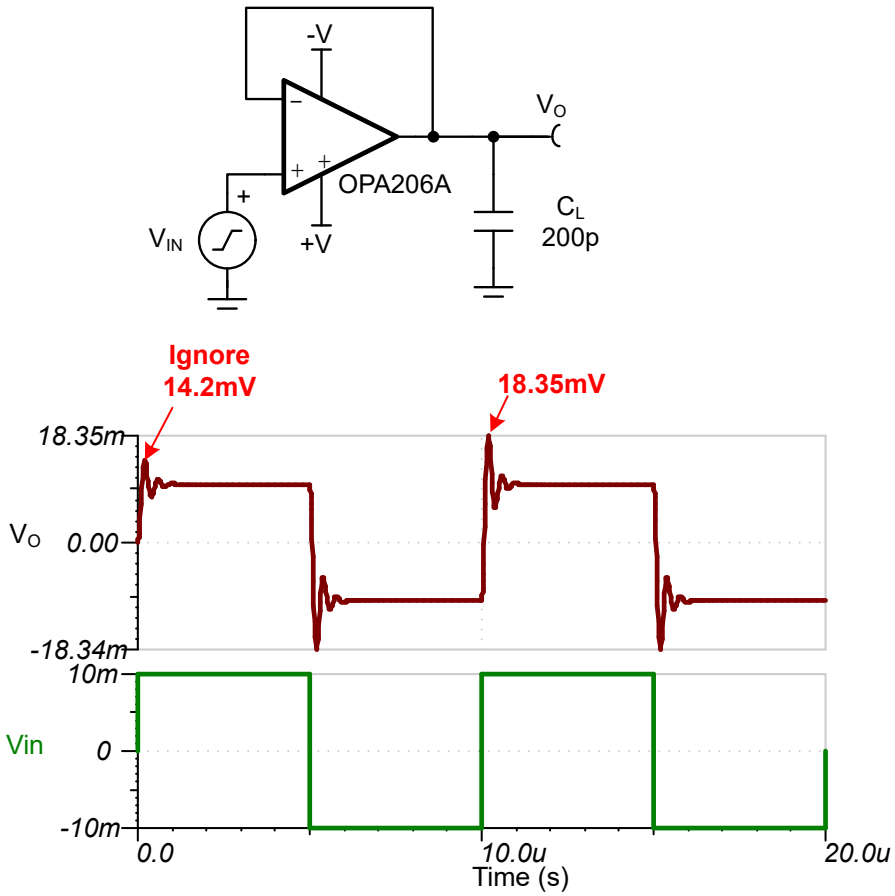


**Figure 8-5. Ignore the Initial Transient Response**

As discussed previously, the open-loop response of an op amp can be simulated by breaking the loop with very large test inductors and capacitors (1TF and 1TH). These large components allow for a valid closed-loop operation a DC and valid open-loop responses from millihertz and above. This method generally works well, but in some cases, there is a mathematical error that happens at low frequency where the $A_{OL}$ is very high. The reason for this error is basically a numerical truncation or overflow error. For example, subtracting a very small number from a very large number can cause this kind of numerical analysis error due to the finite precision of computer calculations. Figure 8-6 illustrates what this kind of mathematical error looks like in simulation. In reality, this error is normally confined to very low frequencies and at the frequency of interest, the stability simulation is accurate. Nevertheless, minimizing this error by reducing the test inductor and capacitor values from tera to giga or even mega values is possible. At some point, this reduction can limit the simulation accuracy at low frequency. Ultimately, this math error generally does not effect the overall accuracy of the simulation so the error can be ignored.

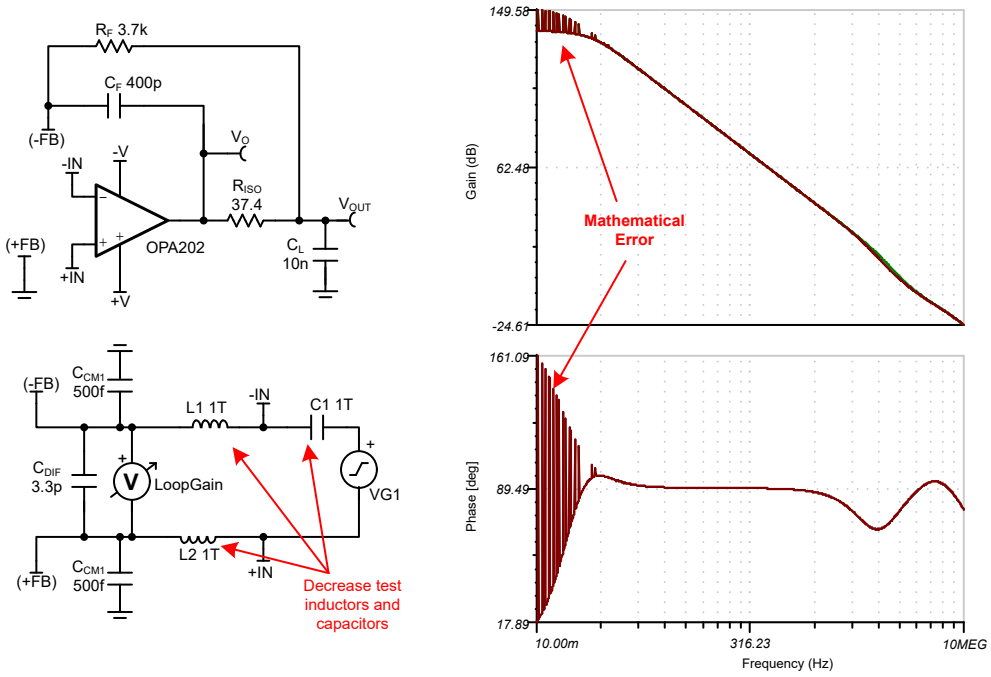


**Figure 8-6. Mathematical Error Common to Open-Loop Stability Analysis**

## 9 References


- Claycomb, Tim and Wells, Collin (2021). *Optimizing Input and Output Transient Settling Times in Amplifier Circuits*. Q3. Optimizing Input and Output Transient Settling Times in Amplifier Circuits.
- Curtis, Alex and Featherstone, Chris (March, 2025). Interview and discussions on complex mathematics.
- Franco, Sergio (August, 2013). *Demystifying Pole-Zero Doublets*. EDN. Demystifying Pole-Zero Doublets.
- Green, Tim (2006–2008). *EN-Genius: 12 Part Stability Series*. Stability Article Series.
- Green, Tim and Wells, Collin (2013). *Op Amp Precision Labs Stability Series*. Op Amp Precision Labs.
- Green, Tim, Oljaca, Miro and Wells, Collin (May, 2015). *Understanding Open-Loop Output Impedance of the PGA900 DAC Gain Amplifier*. Understanding Open-Loop Output Impedance of the PGA900 DAC Gain Amplifier.
- Green, Tim and Wells, Collin (2015). *15 Ways to Stabilize an Op Amp*. 15 Ways to Stabilize an Op Amp.
- Lis, Marek (November 2022). *Reference-Buffer, ADC-Driver and Transimpedance Applications for OPAx328*. Reference-Buffer, ADC-Driver and Transimpedance Applications for OPAx328.
- Olsen, Zach (July 2023). *Determine Optimal Isolation Resistance for Driving Capacitive Load*. Determine Optimal Isolation Resistance for Driving Capacitive Load.
- Varier, Vivek (March, 2025). Interview and discussions on op amp output impedance.
- Wells, Collin (August, 2018). *The Basics of Op Amp Loop-Stability Analysis: A Tale of Twin Loop-Gains*. The Basics of Op Amp Loop-Stability Analysis: A Tale of Twin Loop-Gains.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.



Last updated 10/2025