Functional Safety Information

TPS7B84-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for TPS7B84-Q1 (VSON and SOT223 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

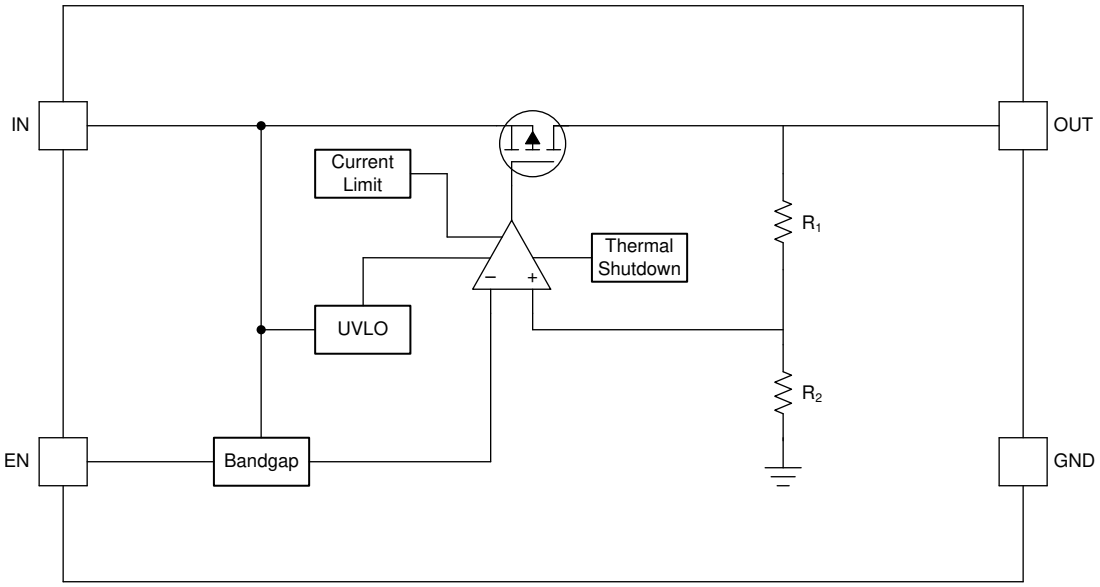

Figure 1-1. Functional Block Diagram

TPS7B84-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 VSON Package

This section provides functional safety failure in time (FIT) rates for the VSON package of TPS7B84-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	10
Die FIT rate	6
Package FIT rate	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 500mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs analog and mixed ≤ 50 V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 SOT223 Package

This section provides functional safety failure in time (FIT) rates for the SOT223 package of TPS7B84-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	14
Die FIT rate	6
Package FIT rate	8

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 500mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs analog and mixed ≤ 50 V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS7B84-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
V_{OUT} high (following V_{IN})	15
V_{OUT} not in specification - voltage or timing	60
V_{OUT} low (no output)	25

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS7B84-Q1 (VSON and SOT223 packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device contains the 8-Pin VSON or the 4-Pin SOT-223 pin configurations.
- Device operates at free-air temperatures between -40°C and 150°C.
- Device operates at an input voltage less than 40V and output current less than 150mA.
- Device operates according to all recommended operating conditions and does not exceed the absolute maximum ratings.

4.1 VSON Package

Figure 4-1 shows the TPS7B84-Q1 pin diagram for the VSON package. For a detailed description of the device pins refer to the *Pin Configuration and Functions* section in the TPS7B84-Q1 data sheet.

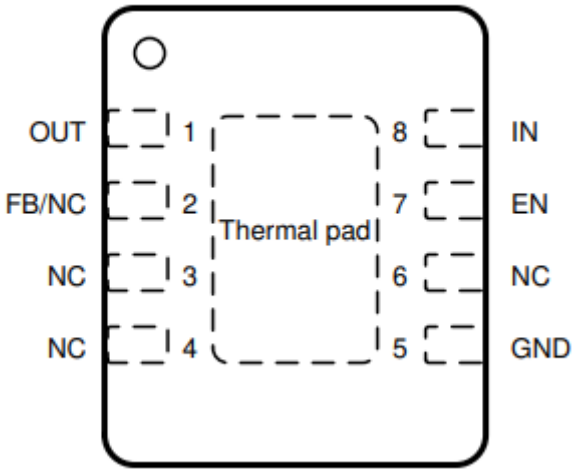

Figure 4-1. Pin Diagram (VSON Package)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
NC, FB	2	(Fixed) No effect. Normal operation.	D
		(Adjustable) The device operates as a switch in dropout mode. The output tracks V_{IN} - V_{DO}.	B
NC	3, 4, 6	No effect. Normal operation.	D
GND	5	No effect. Normal operation.	D
EN	7	The device is disabled, resulting in no output voltage.	B
IN	8	Power is not supplied to the device.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device output is disconnected from the load.	B
NC, FB	2	(Fixed) No effect. Normal operation.	D
		(Adjustable) The device state is unknown. If the device is on, the output voltage is indeterminate.	B
NC	3, 4, 6	No effect. Normal operation.	D
GND	5	There is no current loop for the supply voltage. The device does not regulate and is at risk of exceeding absolute maximum conditions.	A
EN	7	Device not turning on is possible.	B
IN	8	Power is not supplied to the device.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to (1)	Description of Potential Failure Effects	Failure Effect Class
OUT	1	NC, FB	(Fixed) No effect. Normal operation.	D
			(Adjustable) Normal operation if using the device in unity gain.	D
			(Adjustable) If not using the device in unity gain, connecting OUT to FB results in a low output voltage.	B
NC, FB	2	NC	No effect. Normal operation.	D
NC	3	NC	No effect. Normal operation.	D
GND	5	NC	No effect. Normal operation	D
NC	6	EN	No effect. Normal operation.	D
EN	7	IN	The device remains on. Regulation is possible.	C

(1) In the event of a 10kΩ short between adjacent pins, there is no change in the potential failure effect or class.

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible. $V_{OUT} = V_{IN}$. If V_{IN} exceeds 20V, damage is possible.	A
NC, FB	2	(Fixed) No effect. Normal operation.	D
		(Adjustable) The device having no output voltage is possible.	B
NC	3, 4, 6	No effect. Normal operation.	D
GND	5	Power is not supplied to the device.	B
EN	7	The device remains on. Regulation is possible.	C
IN	8	No effect. Normal operation.	D

4.2 SOT223 Package

Figure 4-2 shows the TPS7B84-Q1 pin diagram for the SOT223 package. For a detailed description of the device pins refer to the *Pin Configuration and Functions* section in the TPS7B84-Q1 data sheet.

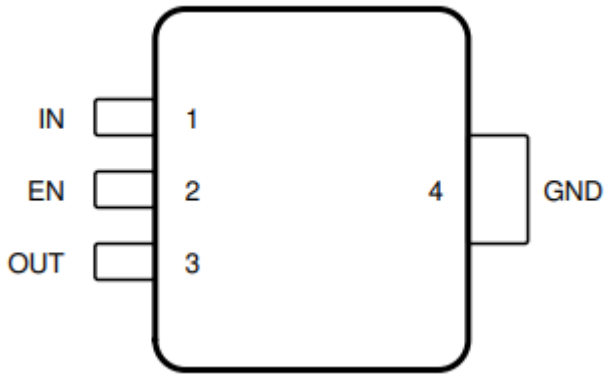

Figure 4-2. Pin Diagram (SOT223 Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Power is not supplied to device.	B
EN	2	The device is disabled, resulting is no output voltage.	B
OUT	3	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
GND	4	No effect. Normal operation.	D

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Power is not supplied to the device	B
EN	2	The device not turning on is possible.	B
OUT	3	The device output is disconnected from the load.	B
GND	4	There is no current loop for the supply voltage. The device does not regulate and is at risk of exceeding absolute maximum conditions.	A

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to (1)	Description of Potential Failure Effects	Failure Effect Class
IN	1	EN	The device remains on. Regulation is possible.	C
EN	2	OUT	The device state is unknown. The device not turning on is possible.	B

(1) In the event of a 10kΩ short between adjacent pins, there is no change in the potential failure effects or class.

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No effect. Normal operation.	D
EN	2	The device remains on. Regulation is possible.	C
OUT	3	Regulation is not possible. $V_{OUT} = V_{IN}$. If V_{IN} exceeds 20V, damage is possible.	A
GND	4	Power is not supplied to the device.	B

5 Revision History

Changes from Revision * (June 2020) to Revision A (August 2024)	Page
• Added the *Pin Failure Mode Analysis (Pin FMA)* section and information	6

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