Application Note

AM62Px Maximum Current Ratings

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This document summarizes the maximum current ratings at the AM62Px power terminals. The current ratings are worst-case estimates for each power supply group, and actual power supply currents for specific applications are typically lower. Table 1-1 serves as a guide for power supply sizing when designing a custom power solution instead of using the TI recommended PMIC. The average active power consumption for a specific use case can be estimated using the AM62P Power Estimation Tool (PET). Actual power consumption must be verified in the real system.

Table 1-1. Maximum Current Ratings at Power Terminals

POWER SUPPLY GROUP	SUPPLY NAME	CONDITION					MAX	UNIT
		CORE Voltage	Operating Junction Temperature Range	Cortex -A53 # of cores and Performance	GPU BXS-4-64 Performance	Video CODEC Wave521CL Performance		
CORE (0.75V/0.85V)	VDD_CORE VDDA_CORE_CSI_DSI VDDA_CORE_DSI_CLK VDDA_CORE_USB VDDA_DDR_PLL0	0.85V	Automotive	Quad, 1400MHz	51 GFLOPS, 800MHz	300Mbps, 500MHz	6555	mA
		0.75V	Automotive	Quad, 1250MHz	42 GFLOPS, 720MHz	300Mbps, 500MHz	5415	mA
		0.85V	Automotive	Dual, 1400MHz	35 GFLOPS, 550MHz	60Mbps, 100MHz	5415	mA
		0.75V	Automotive	Dual, 1250MHz	35 GFLOPS, 550MHz	60Mbps, 100MHz	4560	mA
		0.85V	Extended Industrial	Quad, 1400MHz	51 GFLOPS, 800MHz	300Mbps, 500MHz	5605	mA
		0.75V	Extended Industrial	Quad, 1250MHz	42 GFLOPS, 720MHz	300Mbps, 500MHz	4560	mA
		0.85V	Extended Industrial	Dual, 1400MHz	35 GFLOPS, 550MHz	60Mbps, 100MHz	4560	mA
		0.75V	Extended Industrial	Dual, 1250MHz	35 GFLOPS, 550MHz	60Mbps, 100MHz	3800	mA
CANUART CORE (0.75V/0.85V)	VDD_CANUART(1)						10	mA
0.85V fixed rails (RAM and MMC0)	VDDR_CORE(2) VDD_MMC0(5) VDDA_0P85_DLL_MMC0(5)						300	mA
DDR	VDDS_DDR VDDS_DDR_C						400	mA

Table 1-1. Maximum Current Ratings at Power Terminals (continued)

POWER SUPPLY GROUP	SUPPLY NAME	CONDITION					MAX	UNIT
		CORE Voltage	Operating Junction Temperature Range	Cortex -A53 # of cores and Performance	GPU BXS-4-64 Performance	Video CODEC Wave521CL Performance		
1.8V Analog Supply	VDDA_PLL0 VDDA_PLL1 VDDA_PLL2 VDDA_PLL3 VDDA_PLL4 VDDA_1P8_CSI_DSI VDDA_1P8_OLDI0 VDDA_1P8_USB VDDA_TEMP0 VDDA_TEMP1 VDDA_TEMP2 VDDA_MCU(4)						250	mA
1.8V Digital Supply	VDDS_OSC0 VDDS_MMC0						60	mA
3.3V Supply	VDDA_3P3_USB						50	mA
Dual voltage IO Supplies	VDDSHV0 VDDSHV1 VDDSHV2 VDDSHV3 VDDSHV6						200	mA
SD Interface IO Supply	VDDSHV5(3)						30	mA
MCU IO Supply	VDDSHV_MCU(4)						30	mA
CANUART IO Supply	VDDSHV_CANUART(1)						10	mA
VPP	VPP						400	mA

(1) VDD_CANUART shall be combined with the VDD_CORE power supply group and VDDSHV_CANUART shall be combined with the I/O Power Supply group when not using Partial IO low power mode.
(2) The potential applied to VDDR_CORE must never be greater than the potential applied to VDD_CORE + 0.18V during power-up or power-down. This requires VDD_CORE to ramp up before and ramp down after VDDR_CORE when VDD_CORE is operating at 0.75V. VDD_CORE and VDDR_CORE are expected to be powered by the same source so they ramp together when VDD_CORE is operating at 0.85V.
(3) VDDSHV5 shall be combined with the I/O Power Supply group when a separate power supply is not required for voltage scaling for a high-speed SD card.
(4) VDDA_MCU shall be combined with the same power supply group with the 1.8-V Analog Power Supply and VDDSHV_MCU shall be combined with the I/O Power Supply Group when not isolating MCU channel IO from other IO groups.
(5) AM62Px Errata - i2496 Package Pin Assignment Difference between SR1.0/SR1.1 and SR1.2: Two AMH package terminals previously assigned to VDD_MMC0 and VDDA_0P85_DLL_MMC0 power rails have been assigned to a new signal function, VDDR_CORE, and the connectivity was merged with the VDDR_CORE power rail inside of the package as the device transitions from Device Revision A/B (SR1.0/SR1.1) to Device Revision C (SR1.2) and newer devices.

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Last updated 10/2025