Application Note

TAS278X Schematic and Layout Guidelines

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ABSTRACT

In audio applications it is always important to minimize the noise effects that can be introduced to the device by external conditions. All the audio amplifiers require a clean and stable power supply, isolated and impedance controlled digital inputs, and a clean low impedance ground return path. Otherwise issue of device stability, high THD+N or poor PSRR can occur. In modern integrated DSP smart amplifiers that combine high current switching Class-D amplifiers and low voltage complex digital signal processers it is important that care is taken in component selection and PCB Layout to achieve performance.

This document describes a practical optimized PCB design and layout for the TAS2781, TAS2783A, and TAS2785. The goal is that by following this document, noise issues, output power, and device stability can be optimized regardless of system specific requirements.

Table of Contents

Trademarks

1 Introduction

The following sections describe all critical design considerations for the TAS2781, TAS2783A, and TAS2785. These 3 devices share the same pinout, BOM Requirement, and Layout considerations. The only difference between these devices are DSP features, Soundwire (SNDW) SDCA support in TAS2783A and TAS2785, and of course, part number. For simplicity the name TAS278X is used as a catch-all term to refer to all three of these devices, TAS2781, TAS2783A, and TAS2785 unless it is necessary to differentiate the devices.

2 Detailed Description

2.1 Typical Application Block Diagrams

Figure 2-1 shows a typical application block diagram for TAS278X in a mono configuration. An optional external boost converter, and low-pass filter can be used. The TAS278X can provide an external PWM control signal (PWM_CTRL) to modulate the boost voltage for improved efficiency.

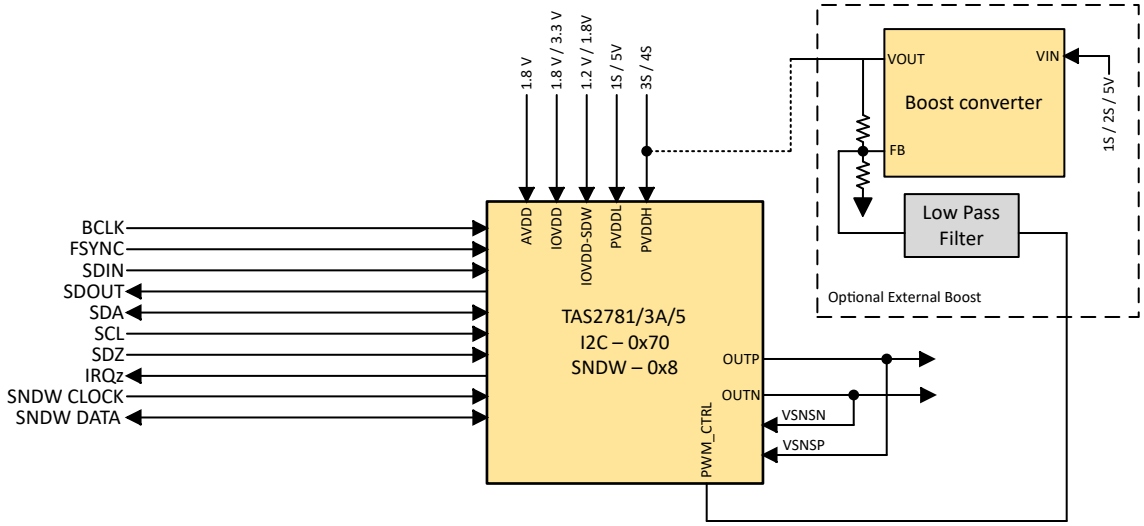

Figure 2-1. Typical Mono Application Block Diagram

Figure 2-2 shows a typical application block diagram in a stereo system. In a 2-or-more channel configuration the digital control data, I2C or SPI, and digital audio data, I2S or TDM, will typically be a shared connection between the devices. The hardware shutdown pin, SDz, and active low interrupt pin, IRQz, can be a shared connection or separated depending on the system requirements. In the SNDW devices, TAS2783A or TAS2785, the SNDW clock and data signals can be connected as required based on bandwidth, SOC vendor recommendation, or PCB layout restrictions. When operating in a non-SNDW mode. The gainsharing pin, ICC, is recommended to be shorted between the two channels. In a 4-way speaker design, such as a stereo woofer-tweeter configuration, the ICC must be shorted between left woofer and right woofer. And then left tweeter and right tweeter.

When the external Class-H boost converter Is used. The PWM_CTRL signal of the 2 devices must be shorted and then connected to the low pass filter (LPF) feedback circuit.

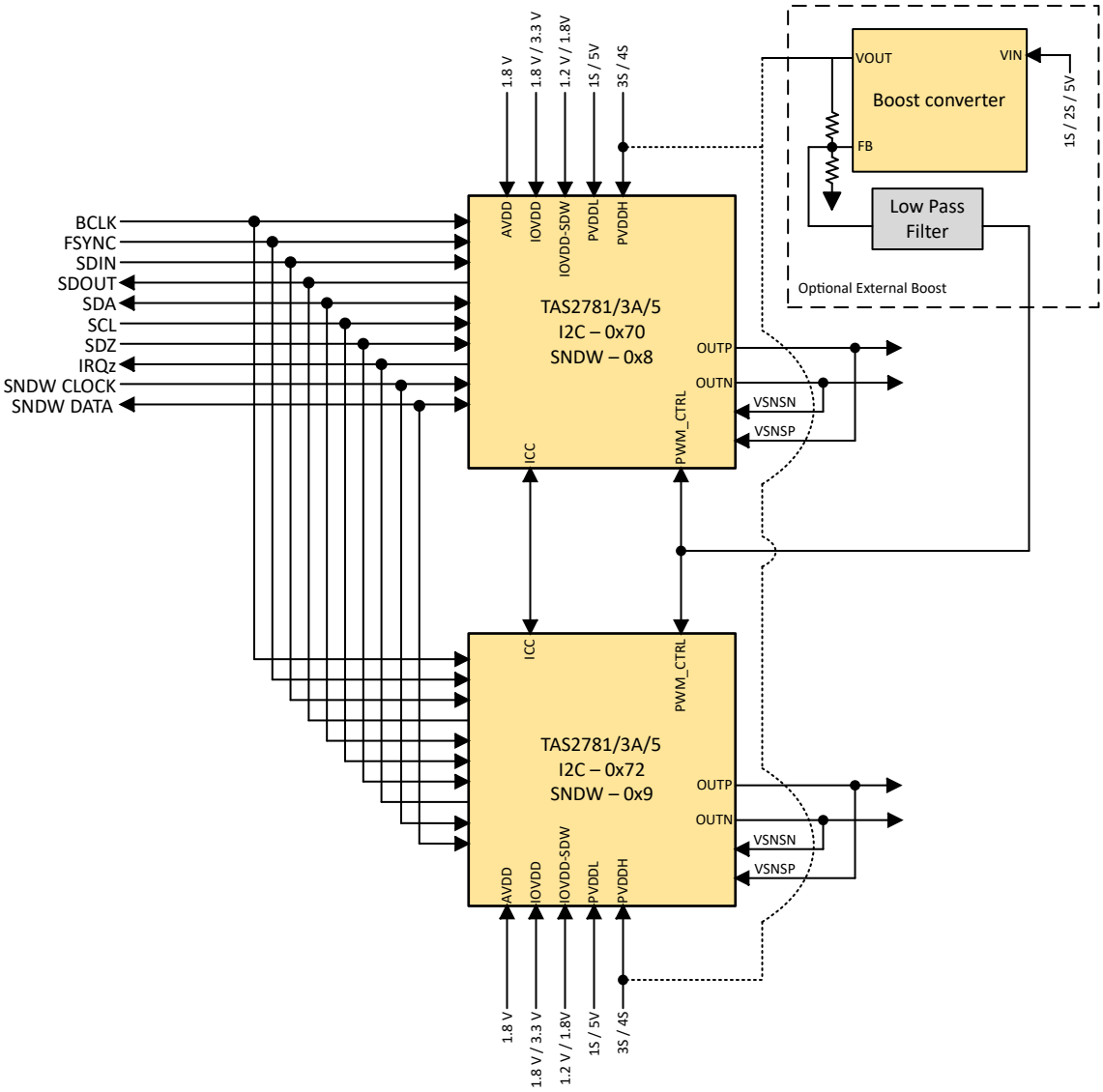

Figure 2-2. Typical Stereo Application Block Diagram

2.2 Typical Schematics

Figure 2-3 shows a typical application schematic in a mono configuration.

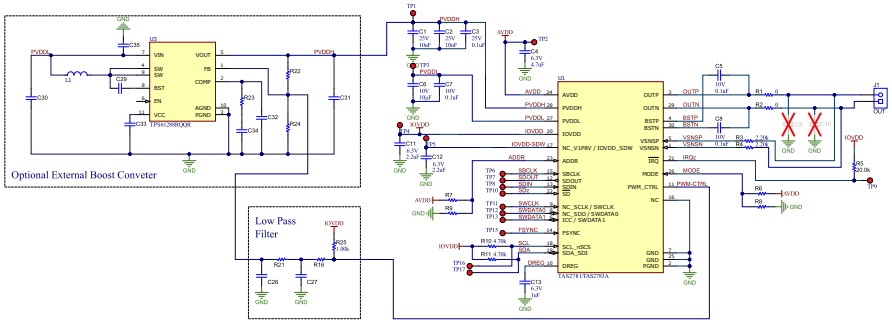

Figure 2-3. Typical Mono Application Schematic

Table 2-1 shows the recommended passive components for the TAS278x.

Table 2-1. TAS278X Recommended Passive Components

Item	Details	Ref Designator	Recommended Value	Comment
Smart Amp		U1	TAS278X	25W Mono Smart Amp
Power Supplies	PVDDH	C1	10uF 25V	Bulk Decoupling
		C2	10uF 25V	Bulk Decoupling
		C3	100nF 25V	Low ESL Decoupling
	PVDDL	C6	PWR_MODE0, 1, and 3 10uF 10V	C6 should be 10uF only in PWR_MODE0, 1 , and 3
			PWR_MODE2 1uF 10V	C6 should be 1 uF only in PWR_MODE2
		C7	100nF 10V	Low ESL Decoupling
	AVDD	C4	4.7uF 6.3V	
	IOVDD	C11	2.2uF 6.3V	IOVDD for all digital pins except 6,8,9
	IOVDD-SDW	C12	2.2uF 6.3V	IOVDD for Pins 6,8,9
	Dreg	C13	1uF 6.3V	DSP LDO output
Class-D	V-Sense	R3	2.2kΩ	Damping reisistor
		R4	2.2kΩ	Damping reisistor
	LC Filter	R1	if needed - 120 Ohm FB Isat > 5A	Saturation current should be higher than the peak output current. Peak current can be approximated as (PVDDH/ Speaker Re)
		R2	if needed - 120 Ohm FB Isat > 5A	
		C9	If needed - 1nF 25V	
		C10	If needed - 1nF 25V	
	Boot Strap Caps	C5	100nF 10V	
		C8	100nF 10V	

Table 2-1. TAS278X Recommended Passive Components (continued)

Item	Details	Ref Designator	Recommended Value	Comment
Device Configuration	Mode Selection	R6 & R8	Short to AVDD	Soudwire Mode
			Short to GND	I2C Mode
			470Ω to GND	SPI Mode
	Address selection	R7 & R9	Short to GND	UID 0x08 **OR** I2C Address 0x70
			470Ω to GND	UID 0x09 **OR** I2C Address 0x72
			470Ω to AVDD	UID 0x0A **OR** I2C Address 0x74
			2.2kΩ to GND	UID 0x0B **OR** I2C Address 0x76
			2.2kΩ to AVDD	UID 0x0C **OR** I2C Address 0x78
			10kΩ to GND	UID 0x0D **OR** I2C Address 0x7A
			10kΩ to AVDD	UID 0x0E **OR** I2C Address 0x7C
			Short to AVDD	UID 0x0F **OR** I2C Address 0x7E
Interrupt Function	Interrupt Function	R5	20kΩ Pull-Up to IOVDD	
Class-H feedback RC Network	Boost Converter	U3	TPS61288RQQR	
	RC Lowpass Filter	R16, R21, C28, C27	Application Specific	refer to SLOA326 for guidance to calculate these values
	Pull-up resistor	R25	1kΩ	
	Boost Passives	L1, R22, R23, R24, C29, C30, C31, C32, C33, C34, C35	Application Specific	Refer to Boost IC datasheet

Figure 2-4 shows a typical application schematic in a stereo configuration

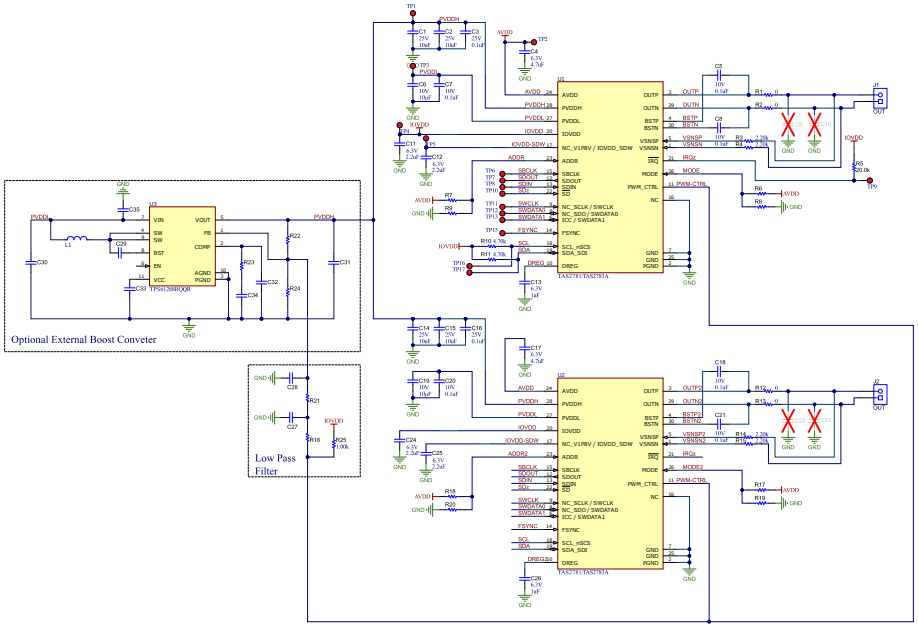

Figure 2-4. Typical Stereo Application Schematic

2.2.1 External PVDDH Mode

TAS278X supports a direct battery connection for the high voltage class-d supply, PVDDH. In a battery powered system the PVDDH rail can supplied directly from a 3S battery, 4S battery, or from any supply less than a nominal 24 VDC. The low voltage supply, PVDDL, can be provided by any 2.7V – 5.5V supply which may already be available in the system, or PVDDL can be generated internally from PVDDH as described in 2.2.3. When PVDDL is generated internally from PVDDH make sure that the PVDDH voltage is not allowed to drop below 7.3V.

The same voltage supply can be used for PVDDL and PVDDH if the nominal voltage of that supply is less than 5.5V.

2.2.2 Class-H Boosted Mode

In systems powered by a 1S battery, 2S battery, or a DC supply of an equivalent voltage. an external class-h boost, such as the TI TPS61288, can be used for the high voltage class-d supply, PVDDH. The low voltage supply, PVDDL, can be directly connected to a 1S battery, It can be provided by any 2.7V – 5.5V supply which can already be available in the system, or PVDDL can be generated internally from PVDDH as described in 2.2.3. When PVDDL is generated internally from PVDDH make sure that the PVDDH voltage is not allowed to drop below 7.3V.

More information and design guidance on the TAS278X class-H boost can be found in TAS2781 and TAS2783 Hybrid-Pro Boost Controller.

2.2.3 TAS278X Power Modes

The TAS278X supports 4 different power supply modes for the class-d. These power modes describe how and when the class-d will be powered from PVDDH and PVDDL.

Most systems designers must choose either PWR_MODE1 or PWR_MODE2. If a sufficiently high current 2.7V – 5.5V power rail exists, then it must be connected to PVDDL, and PWR_MODE1 must be used. This gives the best efficiency by using the Y-bridge. If no supply rail is available for PVDDL then only 1uF + 0.1uF decoupling is required on PVDDL and no external connection is required. This saves some BOM at the cost of efficiency. When using PWR_MODE1 or PWR_MODE2 ensure that the PVDDH voltage is not allowed to drop below PVDDL+2.5V, otherwise the Y-bridge cannot be utilized and the class-d will only be supplied from PVDDH.

PWR_MODE0 is typically not recommended. This requires both PVDDL and PVDDH to be provided to the device, but it will not utilize the Y-bridge. This power mode exists for the system designer who thinks the Y-bridge architecture introduces audible distortion or audio artifacts – this is not the case.

PWR_MODE3 is not a primary operational mode of the device. any system which uses PWR_MODE3 for a purpose like ultrasonic presence detection is recommended to return to a full power mode like PWR_MODE1, 2 or 0.

PWR_MODE0, PWR_MODE1, PWR_MODE3 all require identical BOM components. In PWR_MODE2 PVDDL ***requires*** that only 1uF + 0.1uF decoupling capacitors are used. PWR_MODE0, PWR_MODE1, PWR_MODE3 ***require*** that 10uF + 0.1uF decoupling capacitors are used on PVDDL.

For more information on the Y-bridge and power modes refer to Y-Bridge in TAS278x Class-D Amplifiers for Improving Efficiency .

Table 2-2 shows the possible power mode configurations in TAS278X.

Table 2-2. TAS278x Power Mode Configurations

Supply Power Mode	Output Switching Mode	Supply Condition	PVDDL Mode	Device Configurations	Use Case and Device Functionality
PWR_MODE0	High Power on PVDDH	PVDDH>PVDDL	External	PVDDL_MODE=0 CDS_MODE[1:0]=10	PVDDH is the only supply used to deliver output power.
PWR_MODE1	Y Bridge - High Power on PVDDL	PVDDH	External	PVDDL_MODE=0 CDS_MODE[1:0]=00	PVDDL is used to deliver output power based on level and headroom configured. When audio signal crosses a programmed threshold Class-D output is switched over PVDDH.
PWR_MODE2	Y Bridge - Low Power on PVDDL	PVDDH	Internal	PVDDL_MODE=1 CDS_MODE[1:0]=11	PVDDH is the only supply. PVDDL is delivered by an internal LDO and used to supply at signals close to idle channel levels. When audio signal levels crosses -100dBFS (default), Class-D output switches to PVDDH.
PWR_MODE3	PVDDL	PVDDL	External	PVDDL_MODE=0 CDS_MODE[1:0]=01	The device can be forced to work out of a low power rail mode of operation. For example this can be used for a low power ultrasonic chirp when audio is not played.

2.2.4 TAS278X Operational Modes

The TAS278X operational mode is selected based on the MODE pin configuration.

Table 2-3 shows a list of the TAS2781 Device operational modes.

Table 2-3. TAS2781 Device Operational Modes

Amplifier Mode	Control Interface	Pin 26 (MODE)
Smart Amp	I2C	Connected to GND
Smart Amp	SPI	470Ω to GND

Table 2-4 shows a list of the TAS2783A and TAS2785 operational modes.

Table 2-4. TAS2783A and TAS2785 Operational Modes

Amplifier Mode	Control Interface	Pin26 (MODE)	Pin20 (IOVDD)	Pin17 (IOVDD_SDW)
SoundWire	SoundWire (optional I2C)	Connected to AVDD	1.8	1.8
	SoundWire	Connected to AVDD	1.2	1.2
	SoundWire (optional I2C)	Connected to AVDD	1.8	1.2
I2S/TDM	I2C	Connected to GND	1.8	0
	I2C	Connected to GND	3.3	0
	SPI	470Ω Connected to GND	1.8	1.8

The TAS278X address is selected based on the ADDR pin configuration. Table 2-5 lists the addresses available in TAS278x.

Table 2-5. TAS278x Addresses

SDW Peripheral Unique ID	I2C Address	ADDR PIN
0x8	0x70	Short to GND
0x9	0x72	470Ω to GND
0xA	0x74	470Ω to AVDD
0xB	0x76	2.2kΩ to GND
0xC	0x78	2.2kΩ to AVDD
0xD	0x7A	10kΩ to GND
0xE	0x7C	10kΩ to AVDD
0xF	0x7E	Short to AVDD

2.3 Layout Best Practices

The following sections outline the layout best practices for each pin. The sample layout provided is intended to be practical for all systems. For this reason, the design is not using blind vias, vias on pins, vias on pads, or a solid ground pour on the top layer.

2.3.1 DREG

Pin 10, DREG is an LDO output generated from the AVDD supply. This LDO is used to power the DSP and digital portions of the TAS278X. DREG capacitor placement is critical. the DREG capacitor must be placed directly next to the pin 10. and the ground side of the capacitor is connected to the pin 7 GND on the top layer. For systems which are not using SNDW or SPI this is possible – the GND can be returned on the top layer. For SNDW systems which are using pins 8 and 9, it may not be possible to return the ground on the top layer. Use a via directly next to the ground side of the DREG capacitor and make sure that there is a short path through the layer 2 ground to the pin 7 exists. The parasitic inductance seen by the DREG pin should not exceed 500 pH.

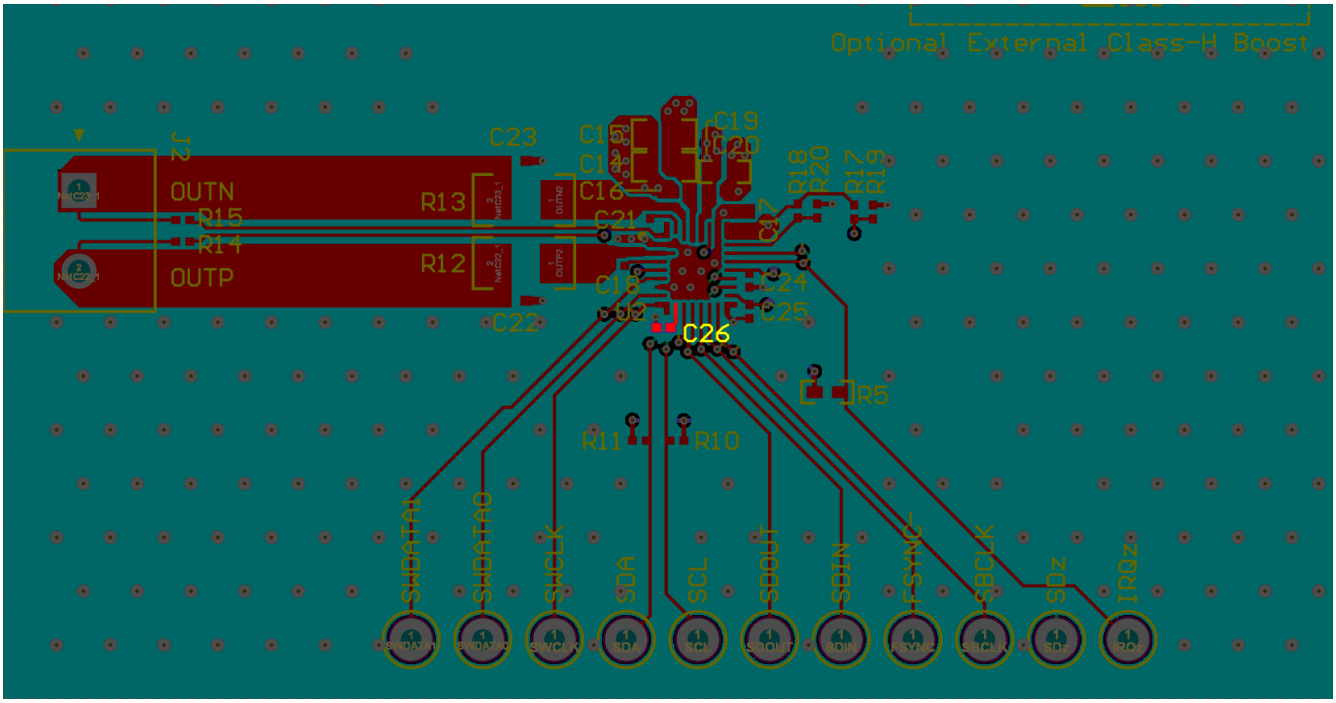

Figure 2-5. DREG

2.3.2 IOVDD and IOVDD-SDW

Pin 17 (IOVDD-SDW or NC_V1P8V) is the IO Supply for the Pins 6,8,9. When SPI, ICC, or SNDW modes are used place a capacitor near this pin and short the ground side of the capacitor to layer 2 GND through a via.

Pin 20 IOVDD is the IO supply for all other digital IO pins. Place a capacitor near this pin and short the ground side of the capacitor to layer 2 GND through a via.

The parasitic inductance seen by the IOVDD, and IOVDD-SDW pin must not exceed 200 pH.

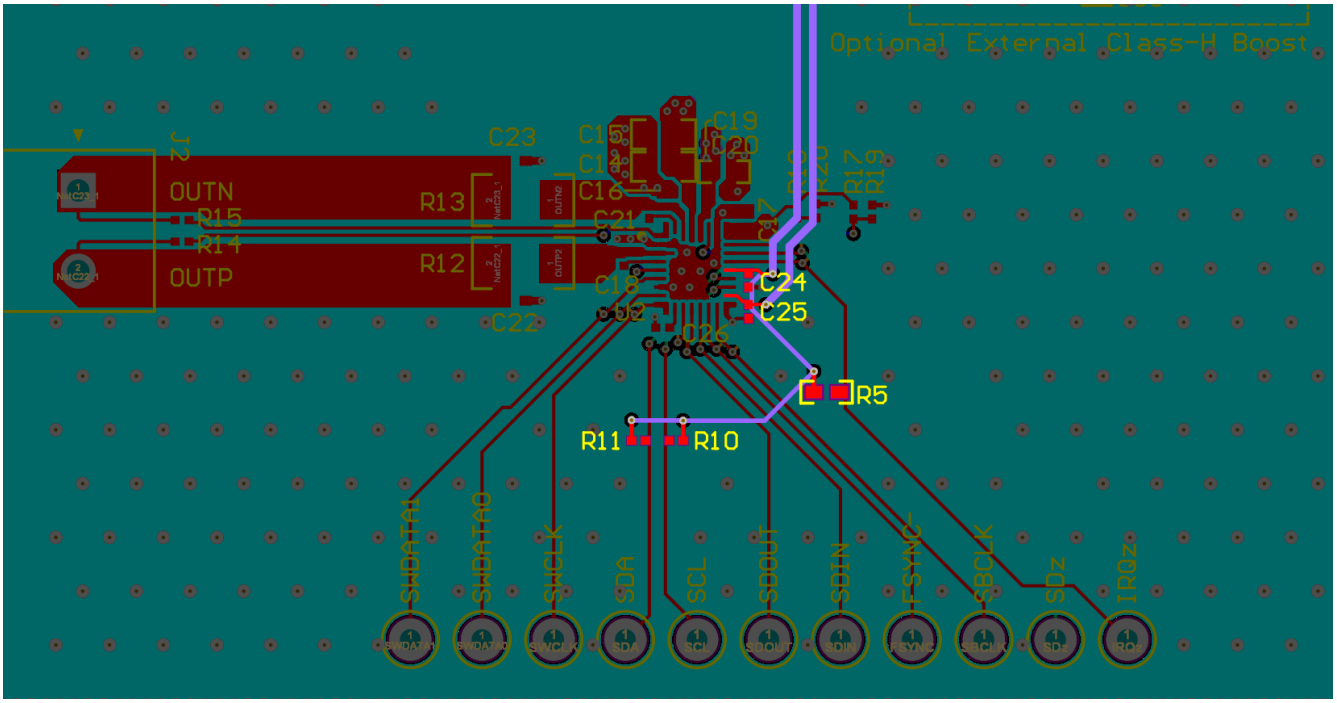

Figure 2-6. IOVDD and IOVDD-SDW

2.3.3 AVDD

Pin 24, AVDD, powers all non-class-D, analog and digital portions of the device. The placement is critical to device performance. In all systems it must be possible to place the AVDD capacitor directly next to the device pin 24, and the GND side of the capacitor can connect to pin 25 GND on the top layer. The parasitic inductance seen by the AVDD pin must not exceed 200pH.

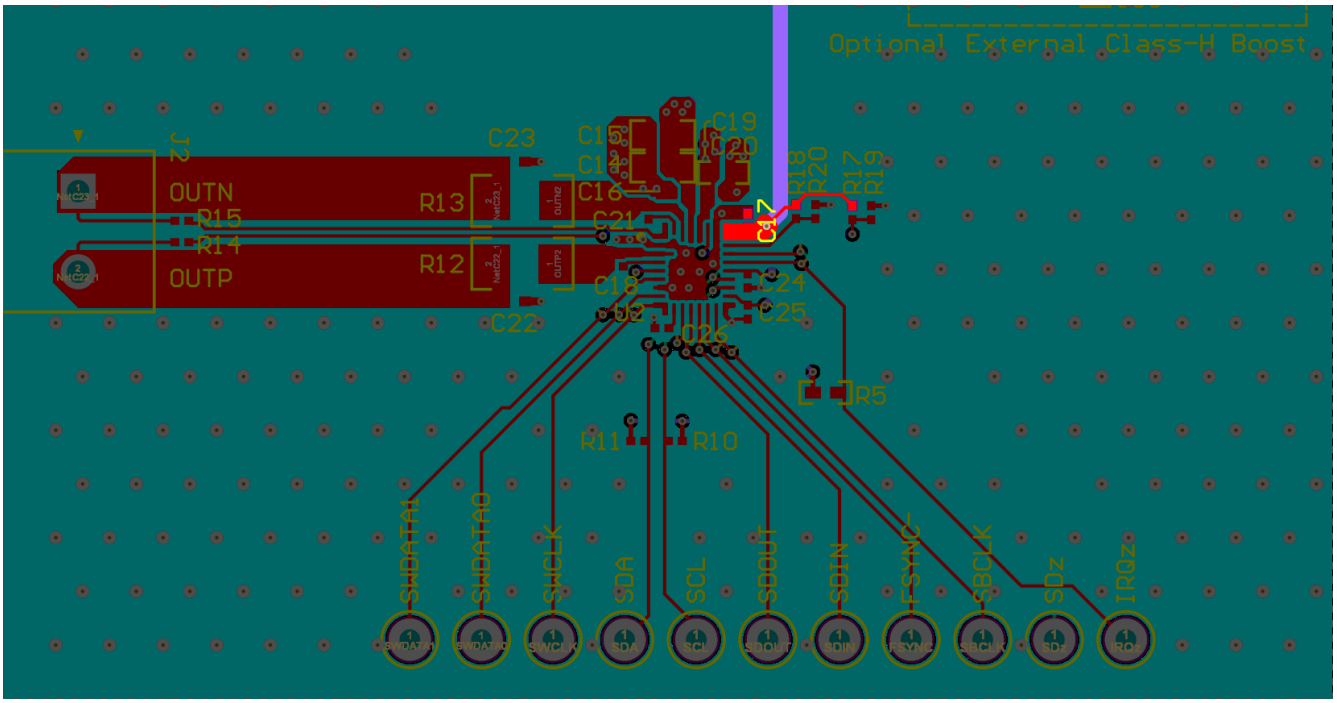

Figure 2-7. AVDD

2.3.4 PVDDH

Pin 28, PVDDH, is the high voltage class-D supply. High parasitic inductance between the PVDDH decoupling capacitor and the device pin can cause THD+N to degrade or device stability issues. the low ESL 0.1uF capacitor should be placed as close to the device pin as possible. And the bulk 10uF capacitors should be placed as close to the low ESL capacitor as possible. Use a wide polygon or trace to provide the PVDDH to the device pin. In the layout the ground side of the PVDDH decoupling capacitors should return to the pin 2 PGND Pin on the top layer. In systems where this is not feasible a ground polygon should be used on the top layer with many vias to the layer 2 GND. It is critical that the ground return path to pin2 is short and low inductance. The parasitic inductance seen by the PVDDH pin should not exceed 100 pH.

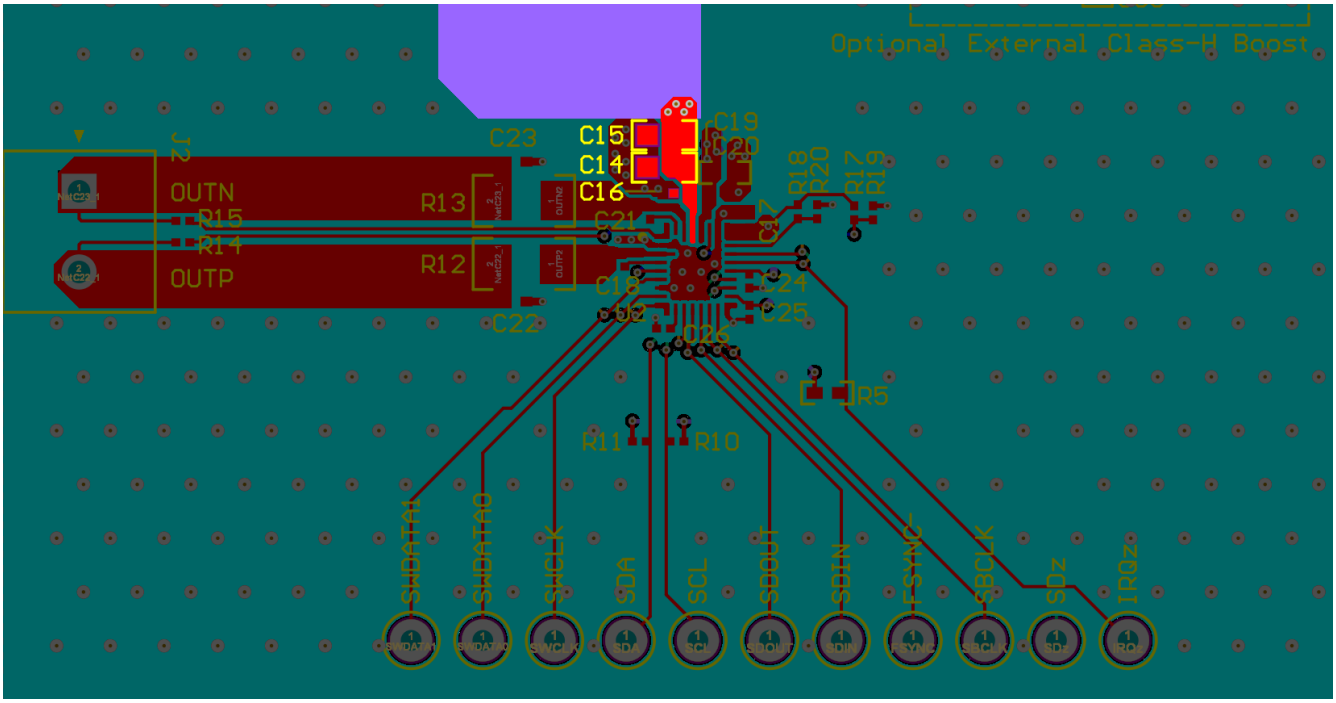

Figure 2-8. PVDDH

2.3.5 PVDDL

Pin 27, PVDDL, is the low voltage supply for the class-D. The layout requirements are the same as for PVDDH. Place the low ESL capacitor as close to the device pin as possible. And place the bulk capacitor as close to the low ESL capacitor as possible. Use a wide polygon to supply PVDDL to the device pin and make sure that there is low impedance path from the ground side of the decoupling capacitors to the pin 2 PGND pin, either through the top layer or through the layer 2 GND using multiple vias. The parasitic inductance seen by the PVDDL pin should not exceed 100 pH.

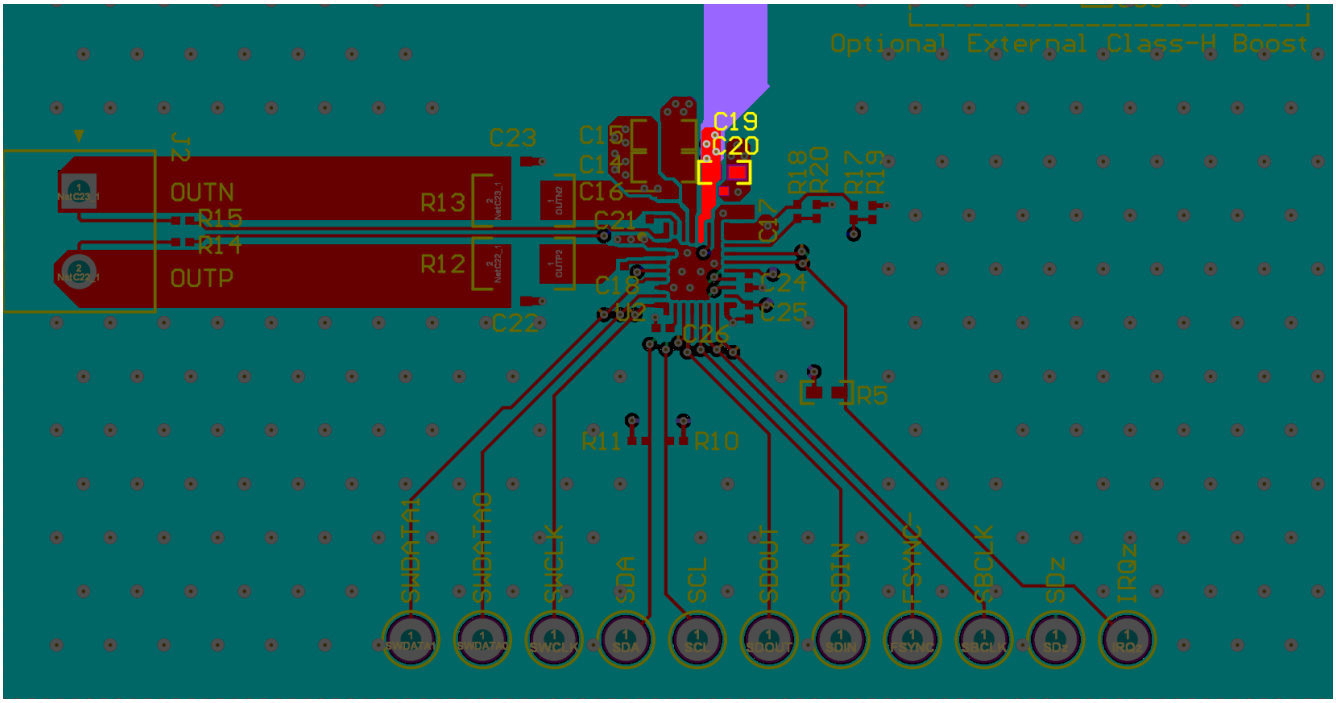

Figure 2-9. PVDDL

2.3.6 Class-D Outputs (OUTP and OUTN)

Pin 3 and pin 29, OUTP and OUTN are the positive and negative outputs of the class-d respectively. Due to the switching nature of these traces, TI recommends keeping the routing as short as possible to minimize the parasitics and emissions.

To optimize the current flow the traces must be widened close to the output pins.

When using an EMI filter, consider the following:

- The inductor or ferrite bead must be the first element in the filter.
- Capacitance to GND pulls high current spikes and risk the overcurrent protection being triggered
- The filter must be placed relatively close to the device to minimize emissions.

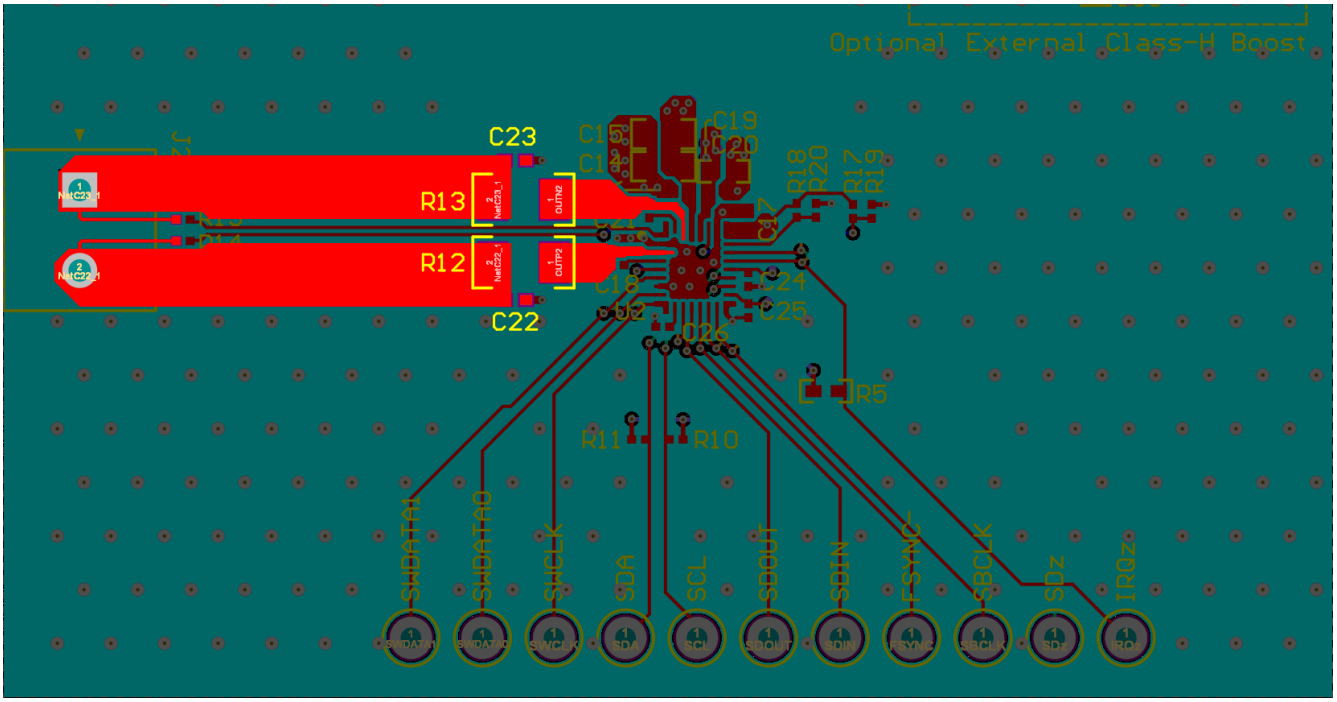

Figure 2-10. OUTP and OUTN

2.3.7 VSNSP and VSNSN

Pin 5 and pin 1, VSNSP and VSNSN are the voltage sense positive and negative inputs respectively. These inputs are relatively high impedance and can be made arbitrarily thin. These inputs must be routed differentially and connected to the output traces (VSNSP for OUTP, and VSNSN for OUTN). The VSNS traces must connect after the ferrite bead or LC filter near the speaker terminals. Do not connect them near the device pin or output trace. TI also recommends including a 2.2kOhm resistor in series with both VSNSP and VSNSN. This practice helps to damp any ringing on the VSNS traces to minimize emissions and prevent any over voltage stress to the VSNS pins.

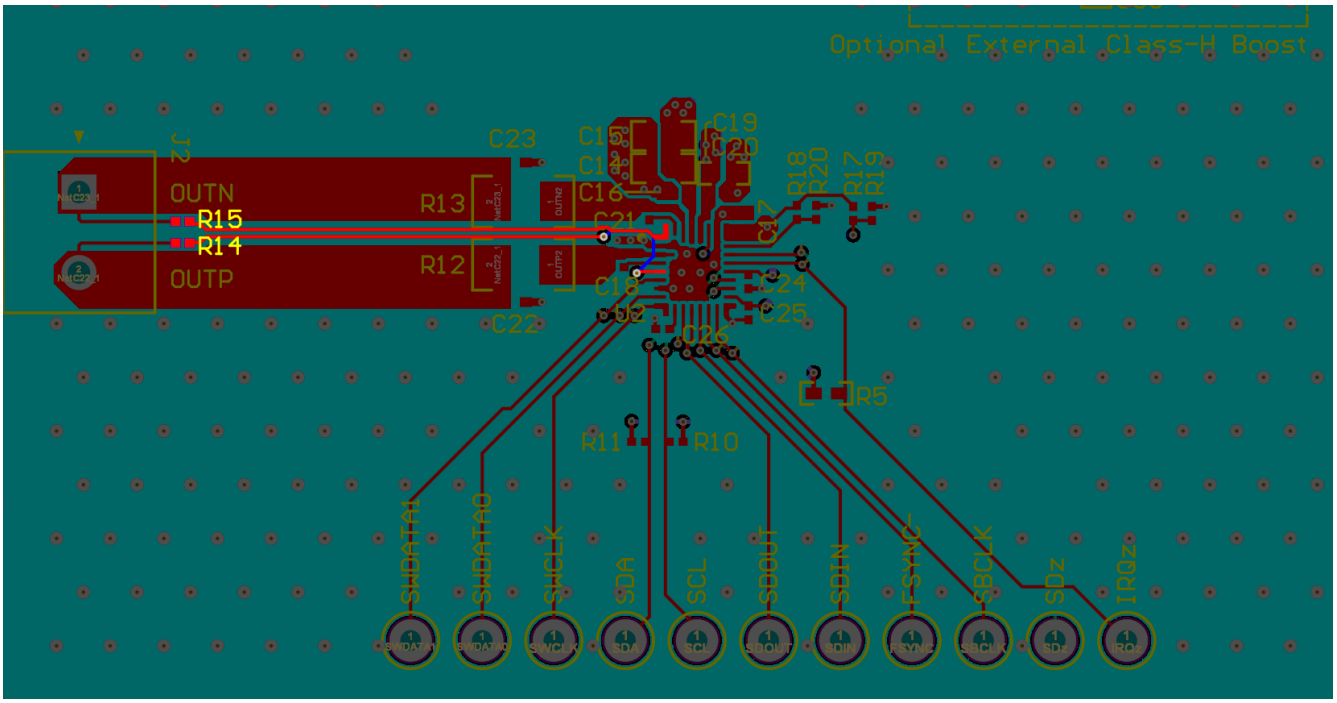

Figure 2-11. VSNSP and VSNSN

2.3.8 BSTP and BSTN

Pin 4 and pin 30 BSTP and BSTN are the bootstrap pins for the OUTP and OUTN respectively. There must be a single 0.1uF capacitor placed between the output traces and the respective bootstrap pin (BSTP for OUTP and BSTN for OUTN) the boot strap capacitor must be connected directly to the output signal before any of the filter components. These capacitors can be placed on the bottom layer if needed. The parasitic inductance seen by the BSTP and BSTN pins can be as high as 1nH.

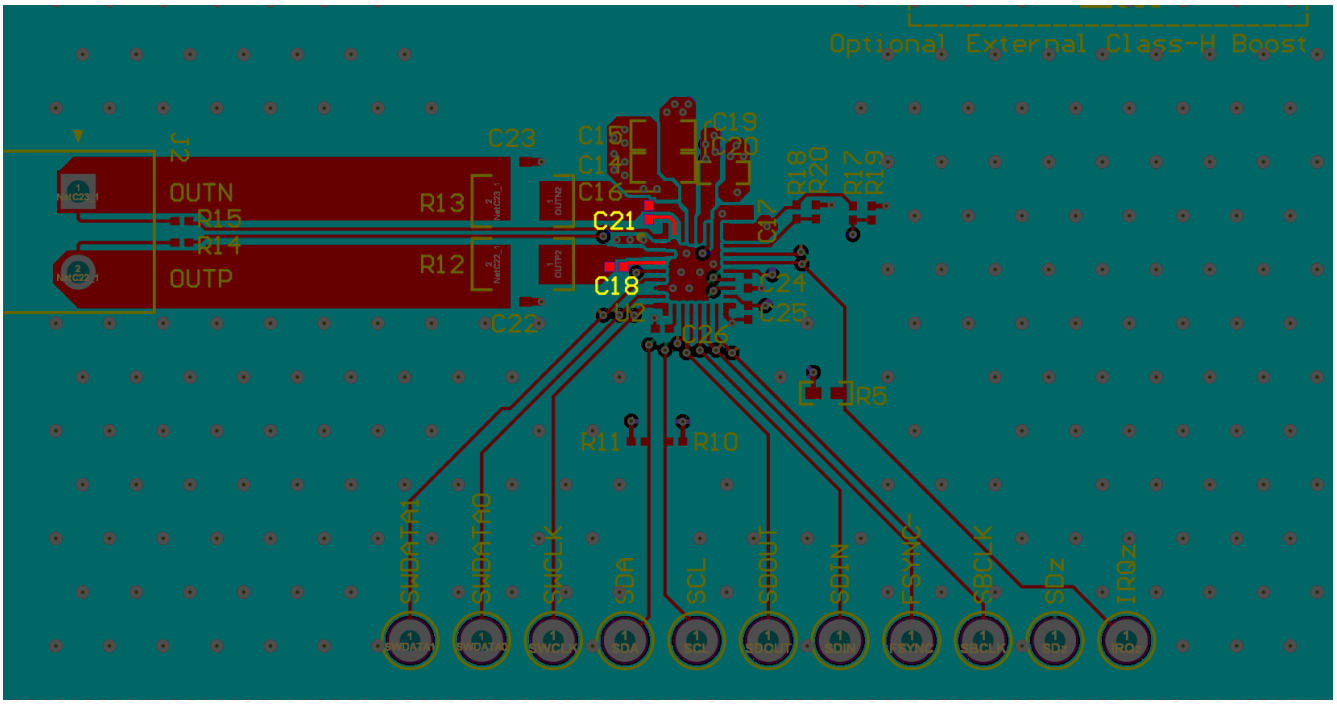

Figure 2-12. BSTP and BSTN

2.3.9 Ground Pins

Ground routing is important when designing the PCB Layout. The ground pins need to have a low impedance electrical and thermal path to the board ground plane, and minimal parasitic inductance. The parasitic inductance between any ground pin and the board ground plane should not exceed 100nH. Design tips for the different ground pins are listed here.

- Pin 2 PGND is the class-D Ground pin. This carries the highest current of the three ground pins. Multiple vias under the package and outside the package must be used to give a low impedance connection to the PCBs ground plane
- Place a ground polygon under the device package on the top layer. Short pins 2,7, and 25 to this polygon, and use multiple vias to short that polygon to the Layer 2 GND plane
- The layer directly under the top layer must be dedicated to ground.

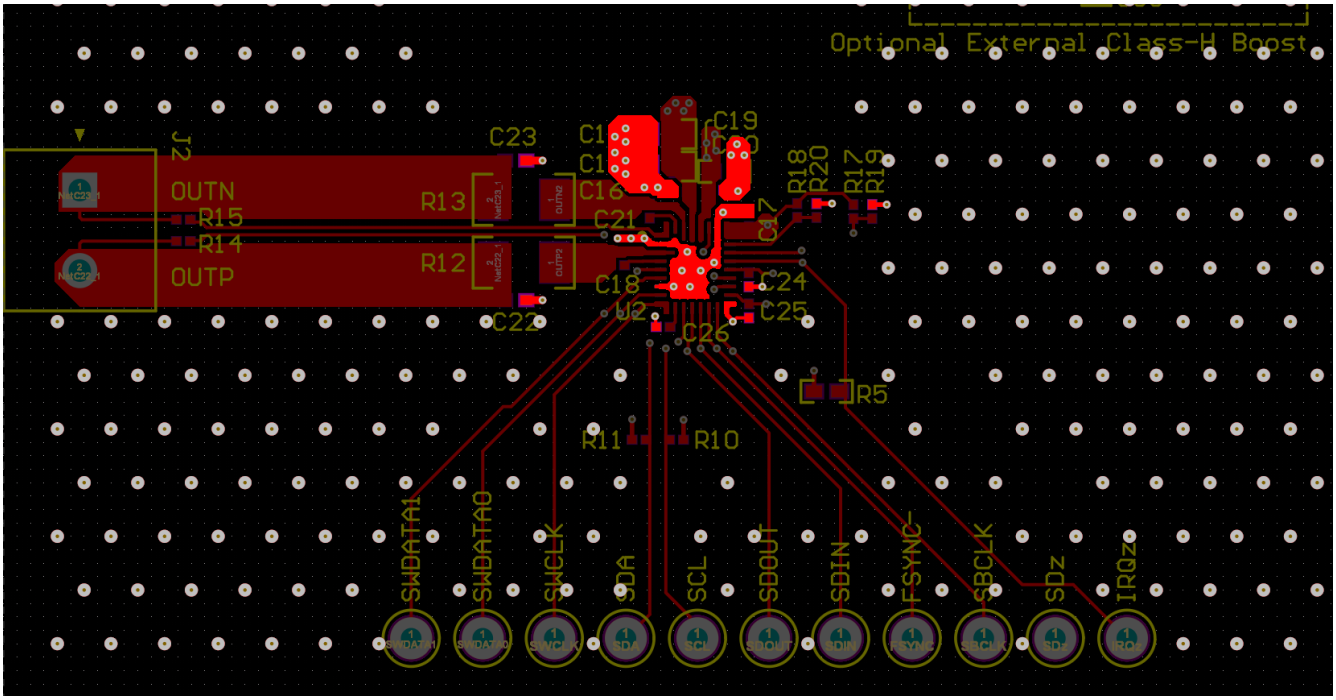

Figure 2-13. Grounding

2.3.10 Non-Soundwire Digital IO

The I2S, I2C, SPI, interrupt and shutdown signals are not significantly sensitive to layout. Avoid routing any of these signals near any high current or switching signals, such as PVDDH, PVDDL, OUTP, OUTN, BSTP, BSTN, VSNSP, VSNSN. Avoid long un-terminated trace segments on the I2S Signals.

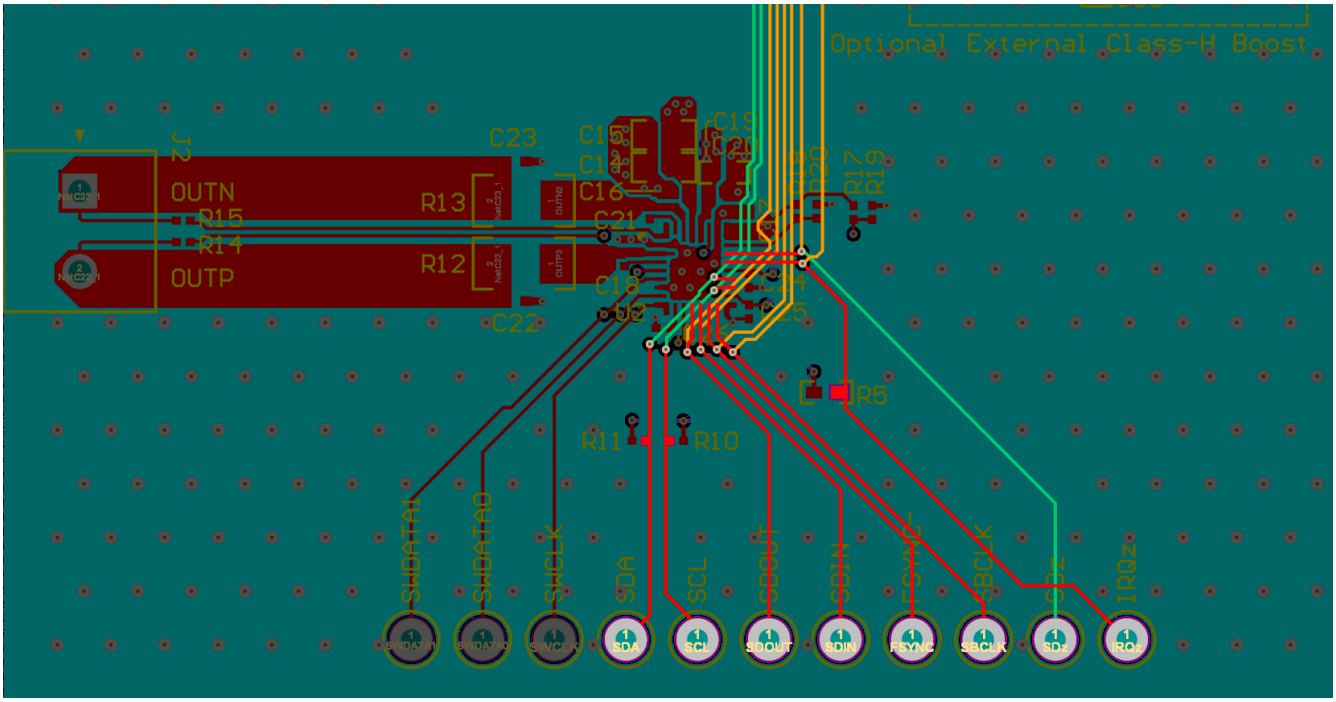

Figure 2-14. Non-Soundwire Digital IO

2.3.11 Soundwire IO

Control the characteristic impedance of all the Soundwire signals to 50 ohms. Length match all bus segments between Host and device, as well as segments daisy chaining between device and device. Avoid routing any of these signals near any high current or switching signals, such as PVDDH, PVDDL, OUTP, OUTN, BSTP, BSTN, VSNSP, VSNSN. Avoid long un-terminated trace segments on the Soundwire Signals.

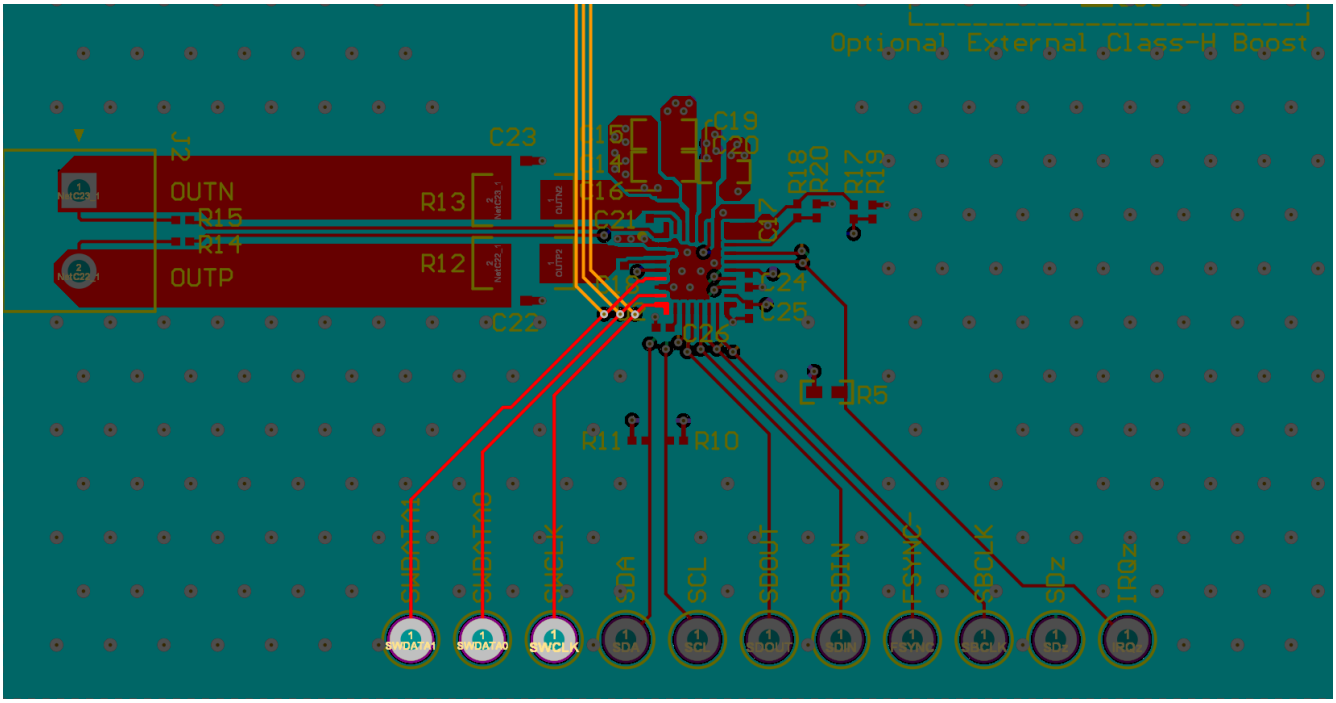

Figure 2-15. Soundwire

3 PCB Layers

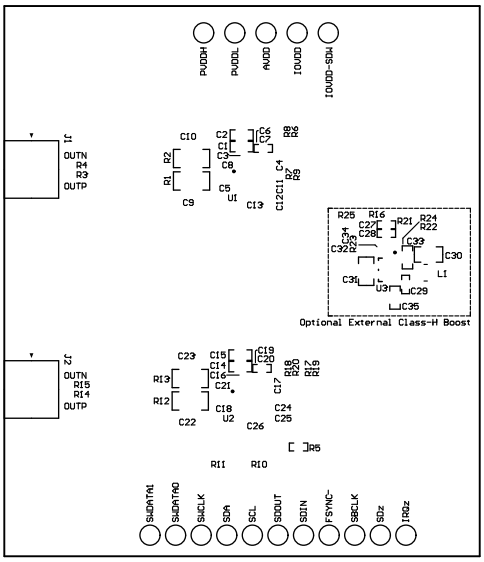

Figure 3-1. Top Overlay

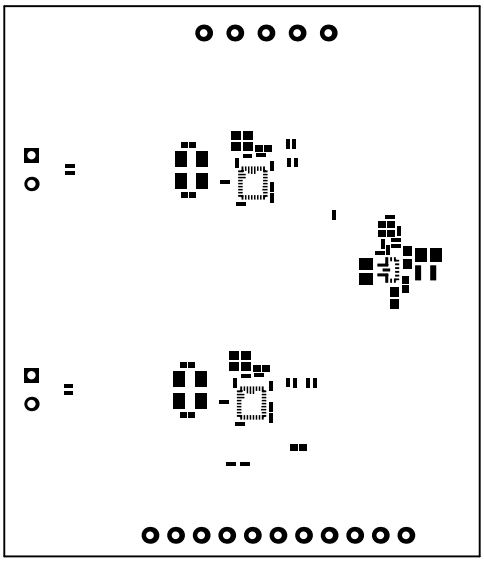

Figure 3-2. Top Solder

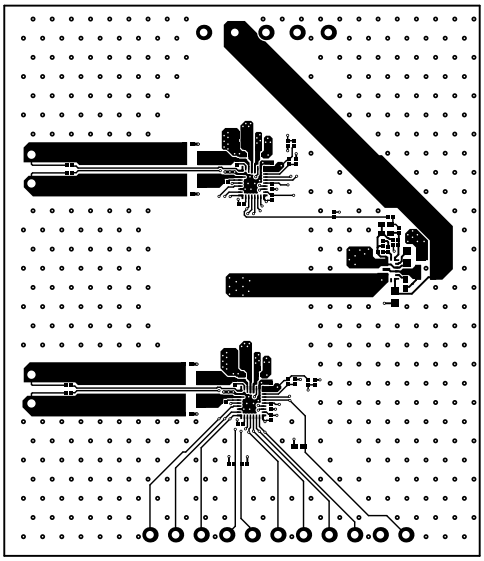

Figure 3-3. Top Layer

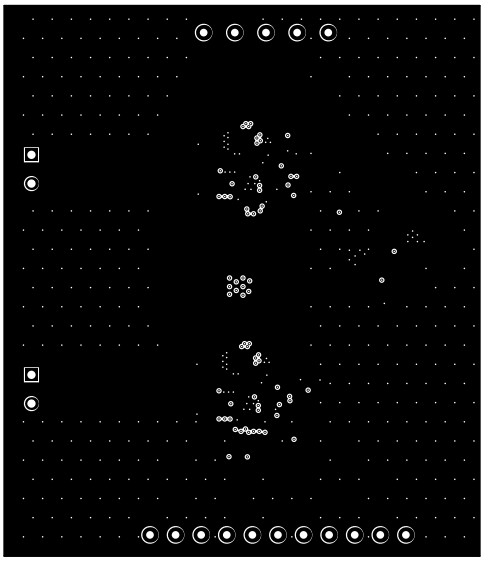

Figure 3-4. Layer 2 Ground

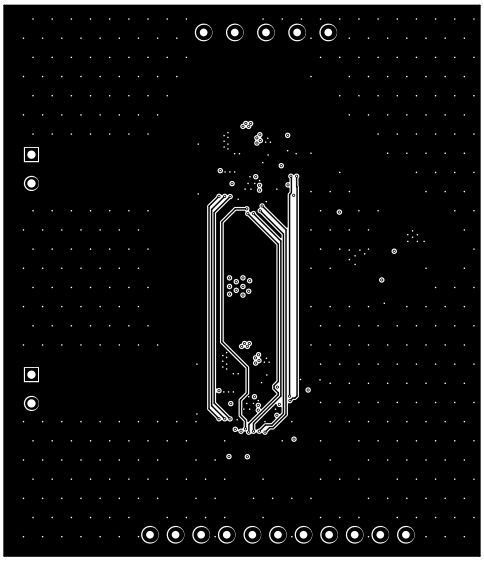

Figure 3-5. Layer 3 Signal

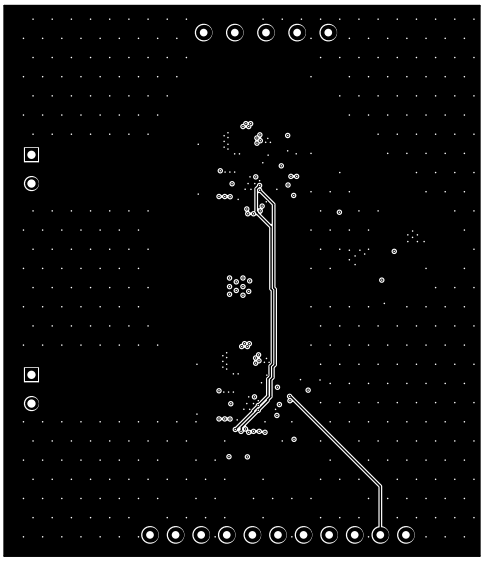

Figure 3-6. Layer 4 Signal

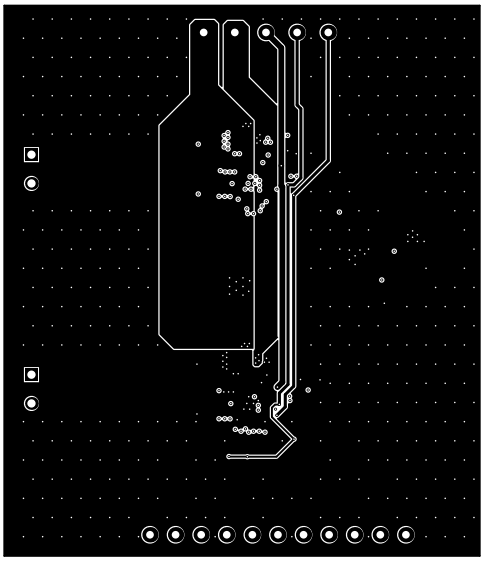

Figure 3-7. Layer 5 Power

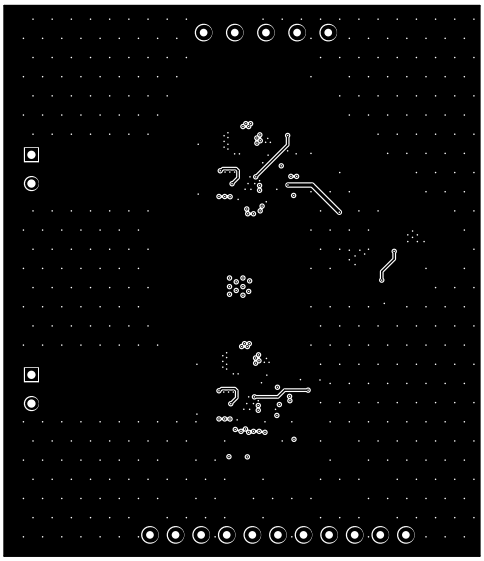

Figure 3-8. Bottom Layer

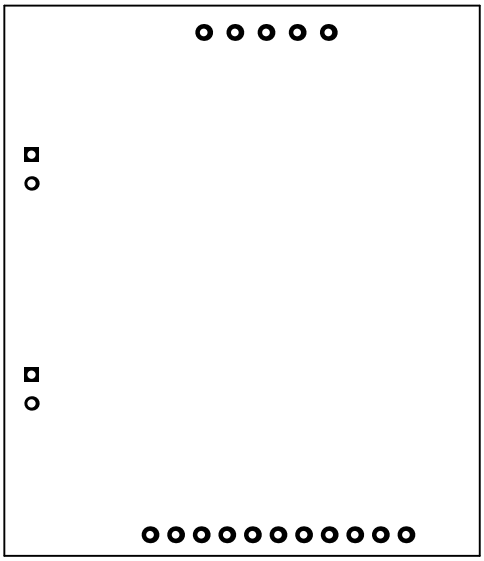

Figure 3-9. Bottom Solder

4 Summary

Table 4-1. Design Guidelines Summary

Pin Number	Pin Name		Schematic Considerations		Layout Considerations
	TAS2783A/ TAS2785	TAS2781			
28	PVDDH	PVDDH	Connect to 3s, 4s battery or boost converter output Decouple to GND with 10uF+10uF+0.1uF at 25V		Use a wide trace to handle the high current Place the capacitors as close to the device pin as possible Make sure there is a short ground return path to pin 2, PGND. if no top layer GND plane is used. Pour a polygon around the ground side of the capacitors and use many vias to give a low impedance ground return path through layer 2.
27	PVDDL	PVDDL	PWR_MODE0,1,3 connect to 1s battery, or 2.7V5.5V DC-DC Decouple to GND with 10uF+0.1uF at 10 PWR_MODE2 Do not connect externally to a voltage Decouple to GND with 1uF+0.1uF at 6.3V		
24	AVDD	AVDD	Connect to 1.8V Decouple to GND with 4.7uF at 6.3V		Place the capacitor as close to the pin 24 as possible. Connect the ground side of the capacitor to pin 25 on the top layer
20	IOVDD	IOVDD	TAS2781 Connect to 1.8V or 3.3V Decouple to GND with 1uF at 6.3V Rated. TAS2783A/TAS2785 Connect to 1.2V, 1.8V or 3.3V Decouple to GND with 2.2uF at 6.3V	Note: if Pin 17 and Pin 20 are sharing a supply voltage, the pins can be shorted together and a single 2.2uF capacitor can be used. This applies to TAS2781 and TAS2783A and TAS2785	Place decoupling capacitors near device pin. Short ground side of the cap to the layer 2 ground plane with a via
17	IOVDD-SDW	NC_V1P8V	If pin 6,8,9 are used, ICC, SPI or Soundwire are used TAS2781 Connect to 1.8V Decouple to GND with 1uF at 6.3V. TAS2783A/TAS2785 Connect to 1.2V or 1.8V Decouple to GND with 2.2uF at 6.3V		
10	DREG	DREG	Decouple to GND with 1uF at 6.3V Do not connect externally to a supply or load		Place directly next to the device pin. There must be a short, direct, and low impedance path to pin 7 GND. Use vias on the ground side of the capacitor to layer 2 GND
1, 5	VSNSN & VSNSP	VSNSN & VSNSP	Short to the speaker output after any LC Filter. Use 2.2kΩ 1% resistor in series		Route differentially and connect to the speaker connector. The 2.2kΩ resistor placement is not critical. This trace carries no current. It can be as thin as allowed by the PCB fab.
3,29	OUTP and OUTN	OUTP and OUTN	This is a filter less class-D. LC filter is optional and only for EMI purposes. Use 120Ω ferrite bead and shunt 1nF capacitor if a filter is required.		Route with wide traces to the speaker connection. Make VSNS connections as close to the speaker as possible. Keep the route short and place the EMI filter near the device to limit emissions.
4,30	BSTP and BSTN	BSTP and BSTN	Place a 100nF 10V capacitor between BSTP<->OUTP and BSTN<->OUTN. Connect the capacitor before any LC Filter.		Both sides of this capacitor must have a low impedance connection. The capacitors can be placed on the bottom side of the PCB.

Table 4-1. Design Guidelines Summary (continued)

Pin Number	Pin Name		Schematic Considerations	Layout Considerations
	TAS2783A/ TAS2785	TAS2781		
26	MODE	MODE	Short to AVDD - Soundwire Mode Short to GND - I2C Mode 470 to GND - SPI Mode	Not critical. Do not allow mode pin connection to affect the AVDD routing.
23	ADDR	ADDR	Short to GND - SNDW UID 0x08 OR I2C Address 0x70 470Ω to GND - SNDW UID 0x09 OR I2C Address 0x72 470Ω to AVDD - SNDW UID 0x0A OR I2C Address 0x74 2.2kΩ to GND - SNDW UID 0x0B OR I2C Address 0x76 2.2kΩ to AVDD - SNDW UID 0x0C OR I2C Address 0x78 10kΩ to GND - SNDW UID 0x0D OR I2C Address 0x7A 10kΩ to AVDD - SNDW UID 0x0E OR I2C Address 0x7C Short to AVDD - SNDW UID 0x0F OR I2C Address 0x7E	Not Critical. Do not allow ADDR pin connection to affect the AVDD routing.
11	PWM_CTRL	PWM_CTRL	Connect to LC filter then boost feedback pin. Refer to {link to sloa326} for design guidance on the Class-H boost. Leave floating if unused	Not critical
21	IRQz	IRQz	In I2C or SPI Modes Pull up to IOVDD with 20kΩ . Connect to SoC GPIO to monitor device interrupt In SNDW Mode Pull up to IOVDD with 20kΩ even if unused.	Not critical
22	SDz	SDz	Connect to the SoC GPIO	Not critical
25,2,7	DGND, PGND, GND	DGND, PGND, GND	Short to board ground	Place a ground polygon under the device package on the top layer. Short pins 2,7, and 25 to this polygon, and use multiple vias to short that polygon to the Layer 2 GND plane The Layer directly under the top layer must be dedicated to ground.
16	NC	NC	Short to board ground	Not critical
6	SWDATA1	ICC	I2C/SPI Modes Short ICC between two L and R channel devices Float if unused Soundwire mode (TAS2783A/TAS2785) Connect to the host data lane 1 Short to GND if unused	In Soundwire mode Control the impedance to 50Ω Length match the trace segments of clock and data between Host <-> Device, and Device <-> Device Do not route near any high current or switching signals, such as PVDDH, PVDDL, OUTP, OUTN, BSTP, BSTN,VSNSP,VSNSN
8	SWDATA0	NC_SDO	SPI Mode Connect to host SPI data in Soundwire mode Connect to the host data lane 0Short to ground if unused	
9	SWCLK	NC_SCLK	SPI Mode Connect to host SPI clock output Soundwire mode Connect to host Soundwire clock output	

Table 4-1. Design Guidelines Summary (continued)

Pin Number	Pin Name		Schematic Considerations	Layout Considerations
	TAS2783A/ TAS2785	TAS2781		
18	SCL	SCL_nSCS	I2C Mode Pull up to IOVDD with resistor SPI Mode Connect to host SPI chip select Soundwire Mode Pull up to IOVDD even if unused	Do not route near any high current or switching signals, such as PVDDH, PVDDL, OUTP, OUTN, BSTP, BSTN, VSNSP,VSNSN
19	SDA	SDA_SDI	I2C Mode Pull up to IOVDD with resistor SPI Mode Connect to host SPI data output Soundwire Mode Pull up to IOVDD even if unused	
12	SDOUT	SDOUT	Connect to host Leave floating if unused	
13,14,15	SDIN, FSYNC, SBCLK	SDIN, FSYNC, SBCLK	Connect to host Connect to ground if unused	

5 References

1. Texas Instruments, Y-Bridge in TAS278x Class-D Amplifiers for Improving Efficiency, application note.
2. Texas Instruments, *TAS2781 and TAS2783 Hybrid-Pro Boost Controller*, application note.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2026) to Revision A (May 2026)	Page
• Minor grammar improvements	22

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