Application Note

Extending Output Voltage Beyond 5.5V with the TPS546x24y Family

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ABSTRACT

The TPS546x24y family uses the VOSNS pin to sense output voltage for closed-loop regulation. Since the VOSNS pin is limited to 5.5V, applications requiring higher output voltages must use an external resistor divider to scale the feedback signal. This application note describes how to design the VOSNS resistor divider for output voltages exceeding 5.5V, the effects on telemetry, fault management, and design limitations.

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Trademarks

1 Introduction

The TPS546x24y family of synchronous buck converters uses the VOSNS pin to sense output voltage for closed-loop regulation. Output voltage is set digitally by adjusting an internal feedback divider, eliminating the need for external feedback resistors. The VOSNS pin has an absolute maximum rating of 5.5V, and the device does not allow the output voltage to be programmed above this limit. Applications requiring output voltages above 5.5V must use an external resistor divider between the V_{out} net and the VOSNS pin to scale the sensed voltage within the pin's operating range, allowing the internal feedback comparator to regulate higher output voltages correctly. This application note describes how to design the VOSNS resistor divider for output voltages exceeding 5.5V, the divider's impact on regulation accuracy, telemetry, fault handling, and practical layout considerations. Table 1-1 shows a list of all part numbers that this application note applies to.

Table 1-1. Applicable Part Numbers

Part Numbers
SN546D24A
TPS546A24A
TPS546A24S
TPS546B24A
TPS546B24S
TPS546D24A
TPS546D24S
TPS546D24Z
TPSM8D6B24
TPSM8D6C24
TPSM8S6B24S
TPSM8S6C24S

2 Theory

When the desired output voltage exceeds 5.5V, an external resistor divider must be placed between the V_{OUT} net and VOSNS pin to scale the feedback signal within the pin's operating range. The divider follows the standard voltage divider equation:

$$V_{VOSNS} = V_{OUT} \times \frac{R_{BOTTOM}}{R_{TOP} + R_{BOTTOM}} \quad (1)$$

where R_{TOP} connects from V_{OUT} to the VOSNS pin and R_{BOTTOM} connects from the VOSNS pin to GND.

The TPS546x24y includes an internal resister divider from VOSNS to GOSNS that has a nominal 130kΩ resistance (85kΩ - 165kΩ) that loads any external resistor divider. For this reason, feedback divider resistors are required to have a resistance of less than 1kΩ to avoid large deviations in expected V_{OUT}. The example design in Section 3 uses a 255Ω resistor as R_{TOP} and a 1.02kΩ resistor as $R_{BOTTOM.}$. Due to the sensitivity of this circuit, resistors with a tolerance of less than ±0.5% are recommended for use in any design utilizing a resistor divider on the VOSNS pin.

Once R_{TOP} and R_{BOTTOM} are chosen, verify that the scaled VOSNS pin voltage remains within the device's programmable output voltage range of 0.25V to 5.5V across the full intended output voltage range. At the maximum programmed output voltage, V_{VOSNS} must not exceed 5.5V. At the minimum programmed output voltage, V_{VOSNS} must not fall below 0.25V.

To find R_{TOP} given a target $V_{OUT(max)}$ and a chosen R_{BOTTOM}:

$$V_{VOSNS} = V_{OUT} \times \frac{R_{BOTTOM}}{R_{TOP} + R_{BOTTOM}} \quad (2)$$

where $V_{VOSNS(max)}$ = 5.5V

Conversly, the formula for calculating V_{OUT} with a given V_{VOSNS} is:

$$V_{OUT} = V_{VOSNS} \times \left(\frac{R_{TOP}}{R_{BOTTOM}} + 1 \right) \quad (3)$$

where V_{VOSNS} is equal to VOUT_COMMAND in addition to VOUT_TRIM, if any.

3 Design Example

3.1 Design Requirements

This design uses the parameters listed in the following table.

Table 3-1. Design Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage		11	12	13	V
I_{IN}	Input Current	V_{IN} = 12V, I_{OUT} = 25A		13		A
V_{OUT}	Output Voltage	VOUT_COMMAND = 4.8V selected by VSEL, attenuated to 6V by external resistor divider.		6.02		V
I_{OUT}	Output Current Range	11V ≤ V_{IN} ≤ 13V	0		25	A
$\eta_{HALF\ LOAD}$	Half Load Efficiency	V_{IN} = 12V, I_{OUT} = 12.5A		97.1		%
$\eta_{FULL\ LOAD}$	Full Load Efficiency	V_{IN} = 12V, I_{OUT} = 25A		96.2		%
$\Delta V_{TRANSIENT}$	Load Transient Response	ΔI_{OUT} = 10A, I_{OUT} slew rate = 1A/µs V_{IN} = 12V		323.9		mV
$\Delta V_{STEADY\text{-}STATE\ NO\ LOAD}$	No Load Steady State Output Ripple Voltage	I_{OUT} = 0A		3.45		mV
$\Delta V_{STEADY\text{-}STATE\ FULL\ LOAD}$	Full Load Steady State Output Ripple Voltage	I_{OUT} = 25A		3.30		mV
F_{SW}	Switching Frequency	V_{IN} = 12V		650		kHz
T_{CASE}	Operating Case Temperature	I_{OUT} = 25A, 30 Minute Soak		69.2		°C
$T_{INDUCTOR}$	Operating Inductor Temperature	I_{OUT} = 25A, 30 Minute Soak		67.7		°C

Note

The TPS546x24A Compensation and Pin-Strap Resistor Calculator supports calculating compensation settings for voltages greater than 5.5V. First, set the pinstrap settings to pre-attenuated V_{OUT}, then change the V_{OUT} cell to reflect your actual V_{OUT}. The V_{REF} cell shows a warning when setting V_{OUT} higher than the recommended maximum value, but the V_{REF} value is not used for any calculations later in the design sheet.

Note

V_{OUT} accuracy is dependent on the accuracy of your external resistor dividers compounded with the specified accuracy listed in the device data sheet. For fine-tuning V_{OUT} accuracy, altering VOUT_COMMAND or VOUT_TRIM is recommended.

3.2 Schematic

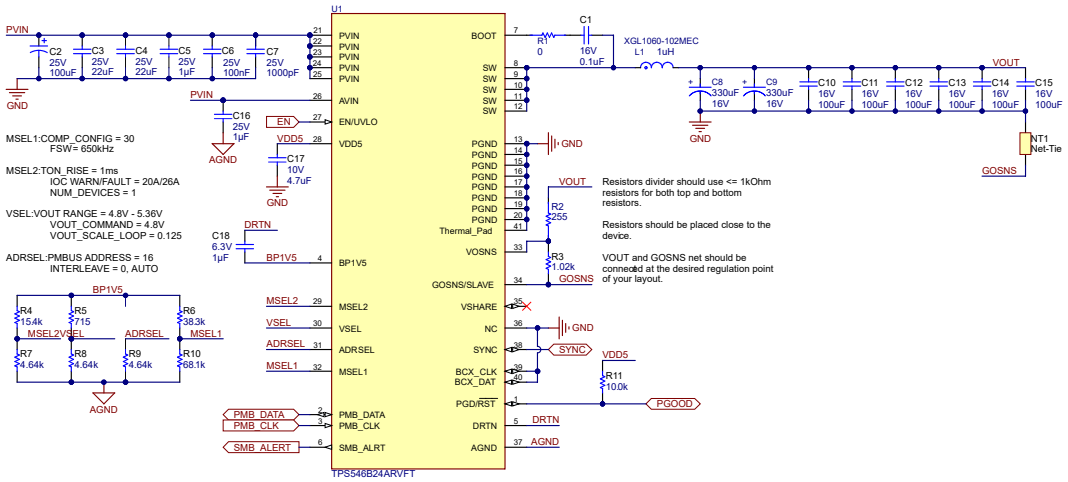
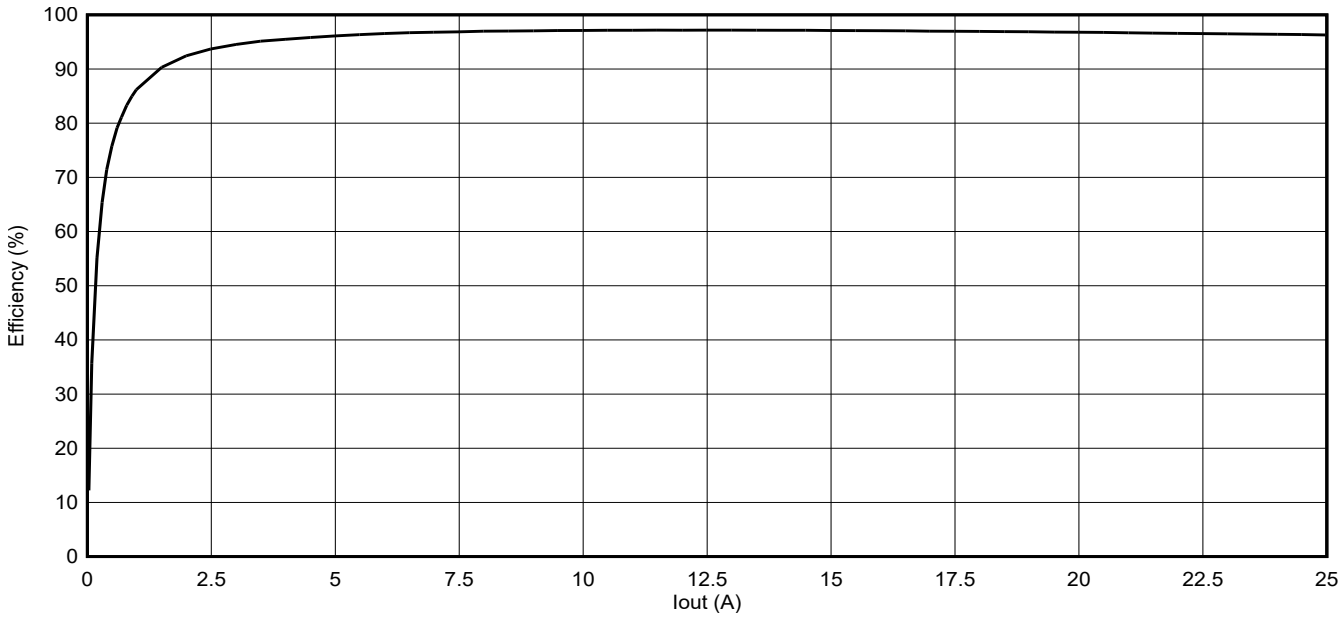


Figure 3-1. 6V$_{out}$ Application Circuit Diagram

Note

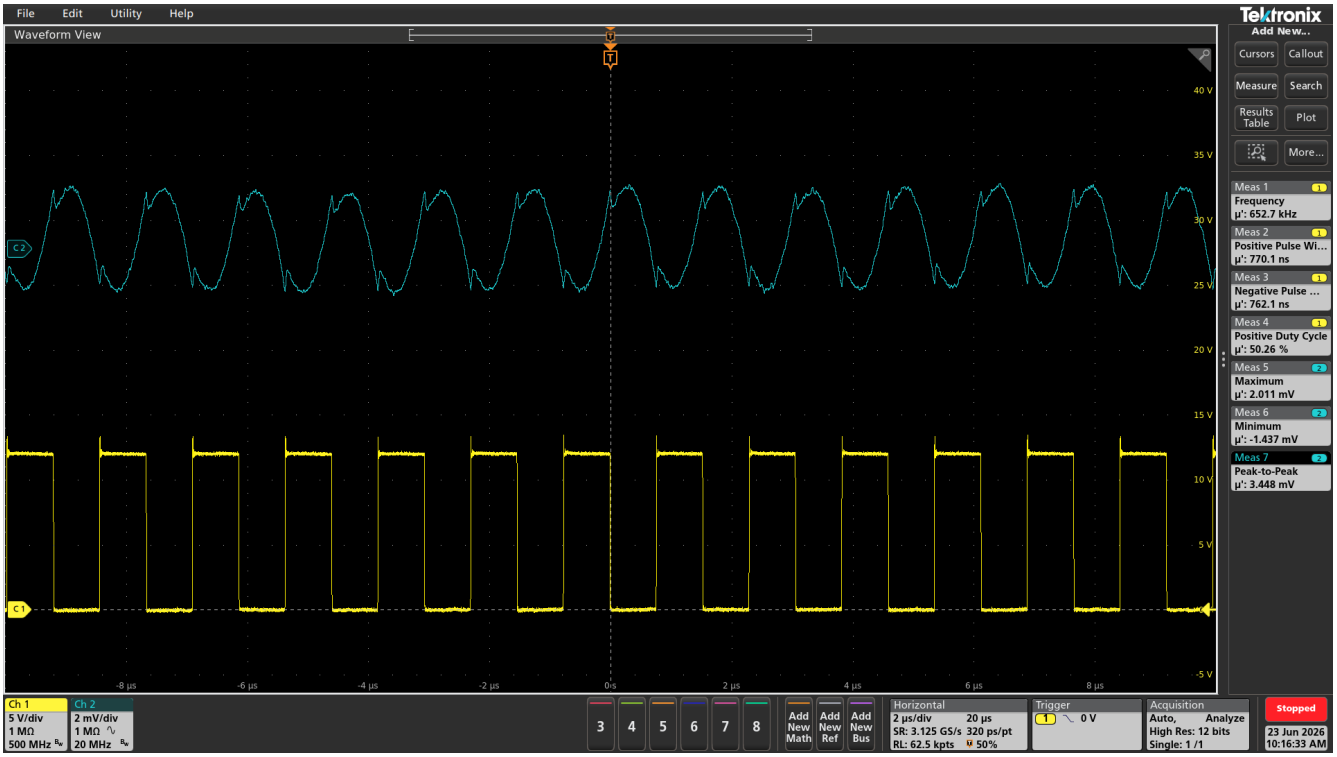
Similar to a design where there is no resistor divider on the VOSNS pin, a kelvin trace must be used to connect the input of the feedback divider network to the desired regulation point of the V_{OUT} plane.

3.3 Performance Plots



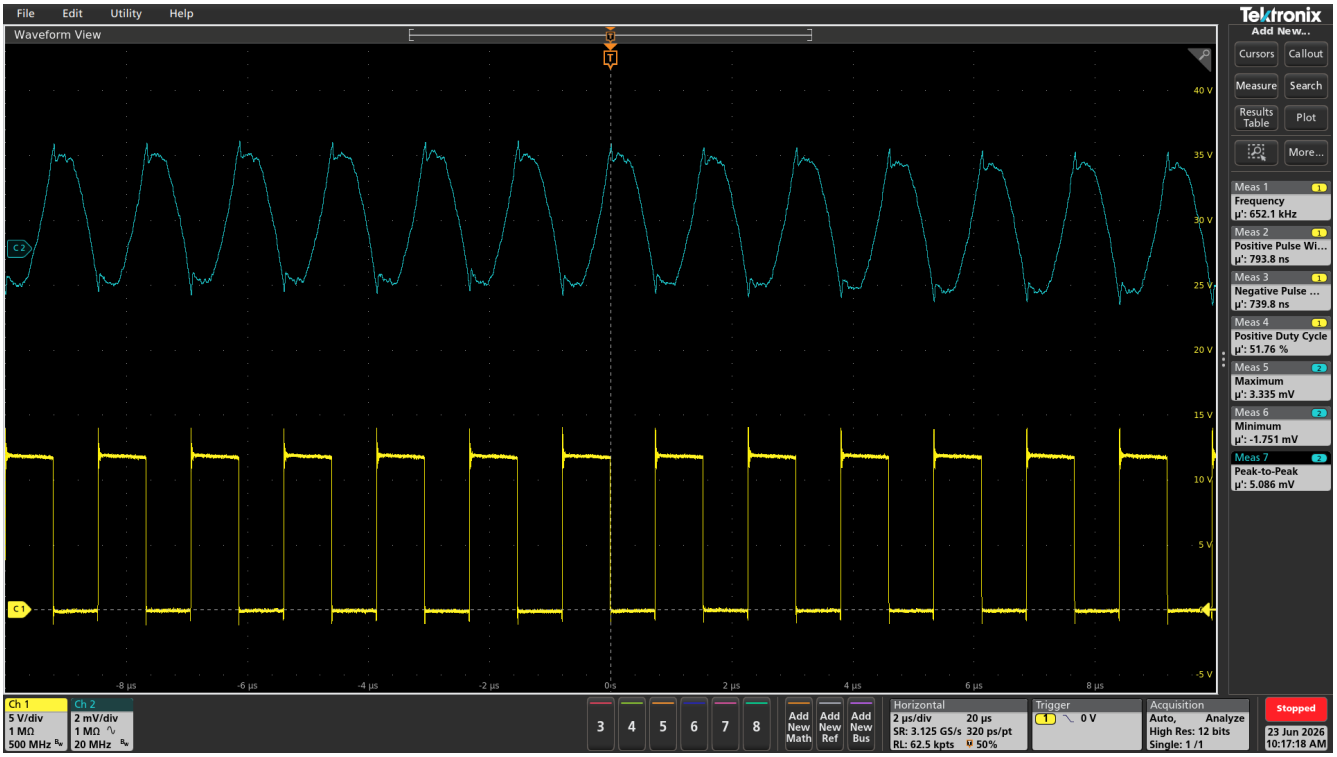
L = 1µH	V_{OUT} = 6V	C_{OUT} = 6 × 100µF Ceramic, 2 x 330µF Polymer
V_{IN} = 12V	Fsw = 650kHz	Internal Bias

Figure 3-2. Efficiency



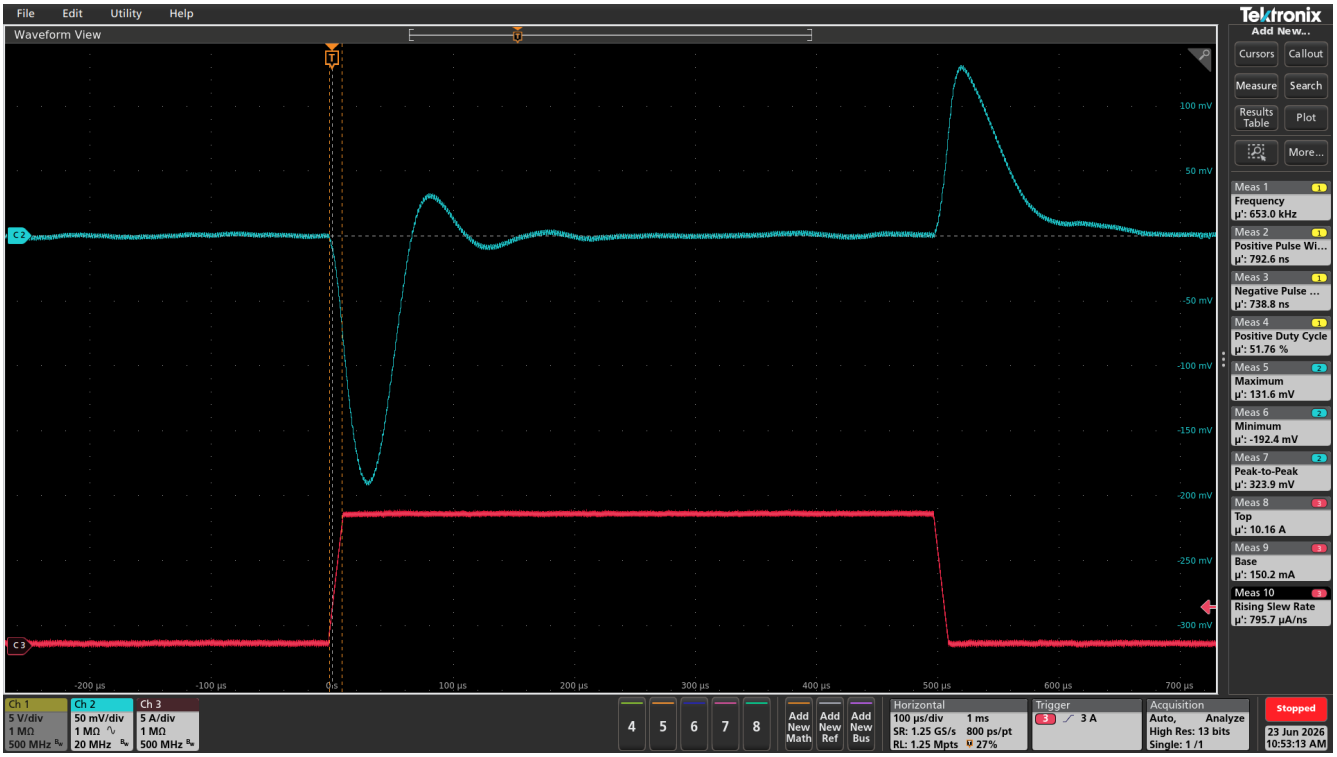
L = 1μH	V_{OUT} = 6V	C_{OUT} = 6 × 100μF Ceramic, 2 x 330μF Polymer
V_{IN} = 12V	Fsw = 650kHz	Internal Bias
CH1 = SW	CH2 = V_{OUT}	

Figure 3-3. Output Voltage Ripple - 0A



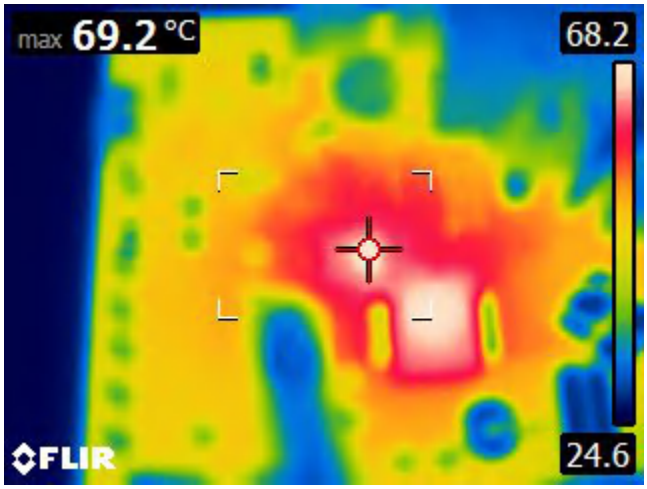
L = 1μH	V_{OUT} = 6V	C_{OUT} = 6 × 100μF Ceramic, 2 x 330μF Polymer
V_{IN} = 12V	Fsw = 650kHz	Internal Bias
CH1 = SW	CH2 = V_{OUT}	

Figure 3-4. Output Voltage Ripple - 25A



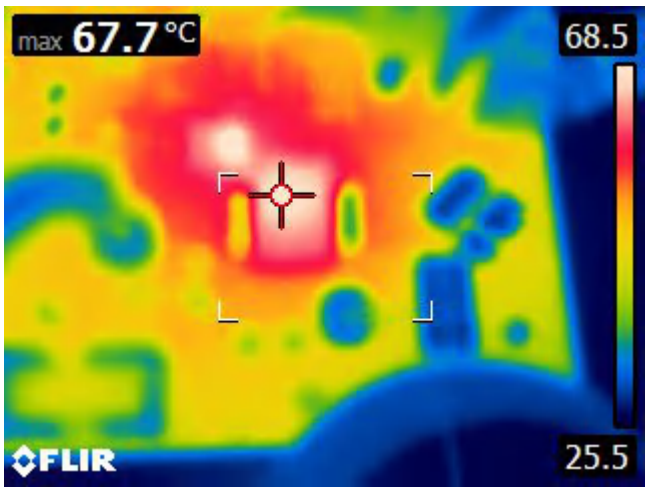
L = 1μH	V_{OUT} = 6V	C_{OUT} = 6 × 100μF Ceramic, 2 x 330μF Polymer
V_{IN} = 12V	Fsw = 650kHz	Internal Bias
CH2 = V_{OUT}	CH3 = I_{LOAD}	5A being sunk by external DC load.

Figure 3-5. Load Transient - 5A to 15A @ 1A/μs



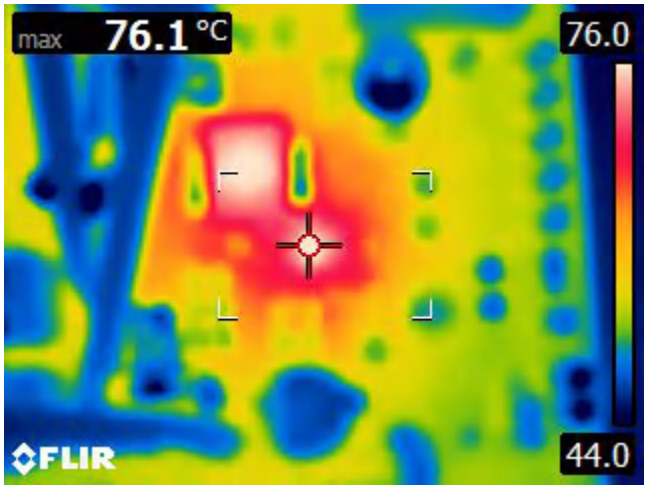
L = 1µH	V_{OUT} = 6V	C_{OUT} = 6 × 100µF Ceramic, 2 x 330µF Polymer
V_{IN} = 12V	Fsw = 650kHz	Internal Bias
I_{OUT} = 25A	Air Velocity = 0 LFM	

Figure 3-6. IC Thermal Performance - $T_{AMBIENT}$ = 25°C



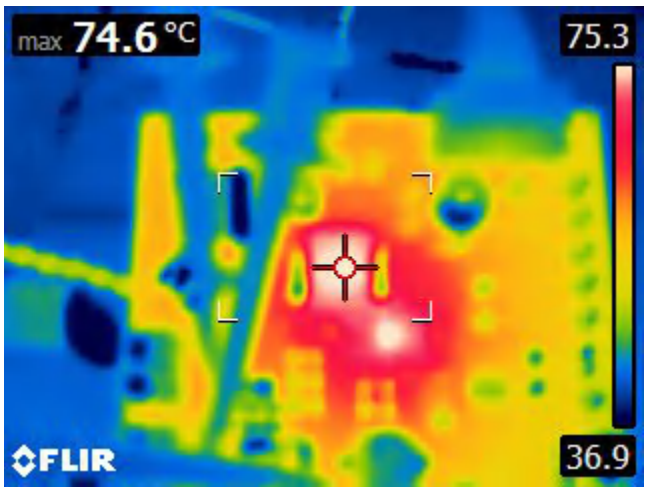
L = 1µH	V_{OUT} = 6V	C_{OUT} = 6 × 100µF Ceramic, 2 x 330µF Polymer
V_{IN} = 12V	Fsw = 650kHz	Internal Bias
I_{OUT} = 25A	Air Velocity = 0 LFM	

Figure 3-7. Inductor Thermal Performance - $T_{AMBIENT}$ = 25°C



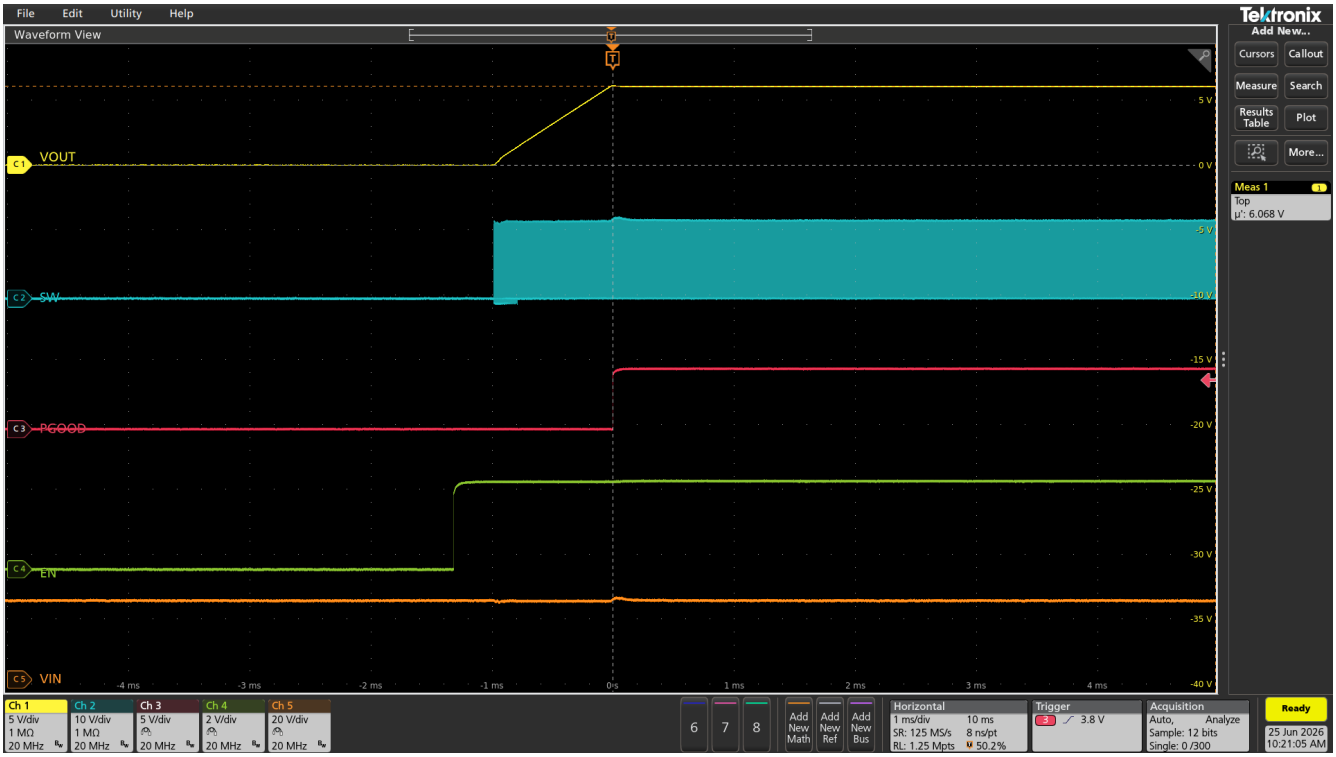
Note		
L = 1µH	V_{OUT} = 6V	C_{OUT} = 6 × 100µF Ceramic, 2 x 330µF Polymer
V_{IN} = 12V	Fsw = 650kHz	Internal Bias
I_{OUT} = 25A	Air Velocity = 0 LFM	

Figure 3-8. IC Thermal Performance - $T_{AMBIENT}$ = 45°C



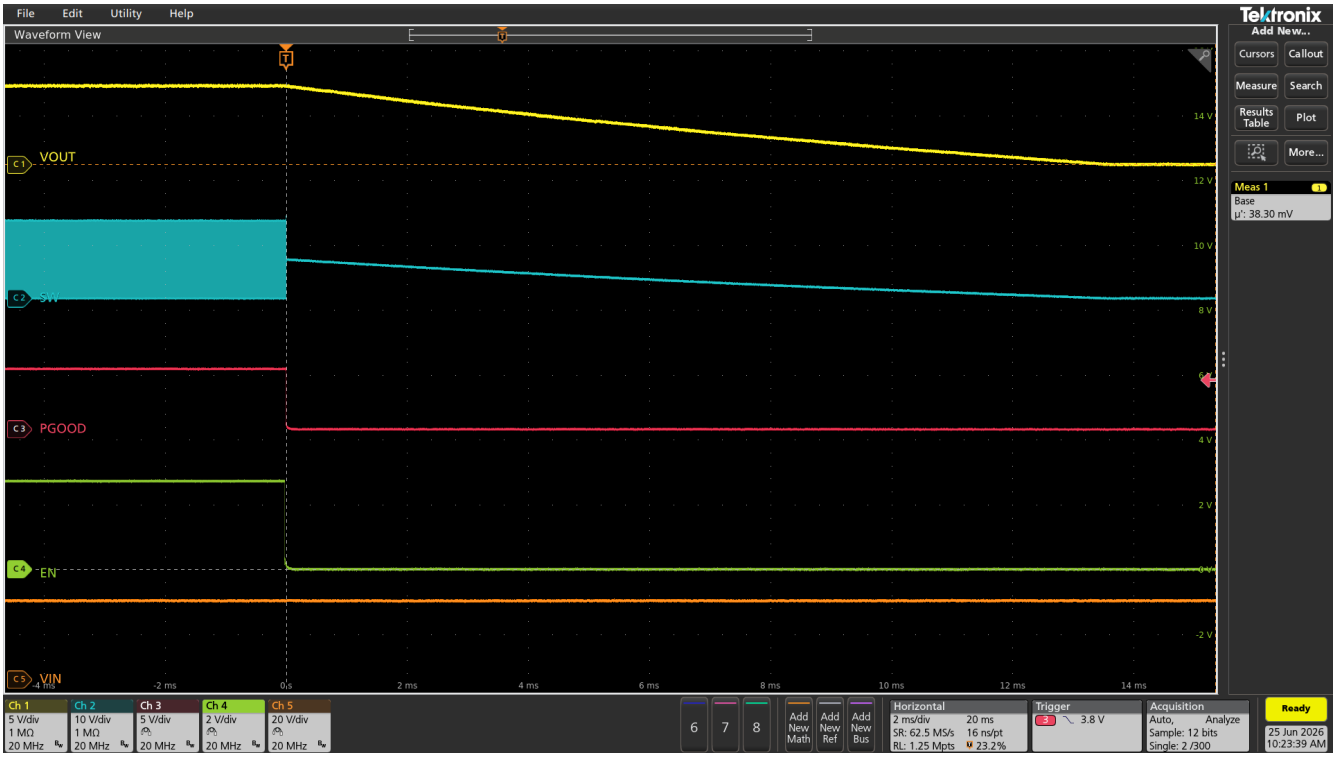
Note		
L = 1µH	V_{OUT} = 6V	C_{OUT} = 6 × 100µF Ceramic, 2 x 330µF Polymer
V_{IN} = 12V	Fsw = 650kHz	Internal Bias
I_{OUT} = 25A	Air Velocity = 0 LFM	

Figure 3-9. Inductor Thermal Performance - $T_{AMBIENT}$ = 45°C



L = 1μH	V_{OUT} = 6V	C_{OUT} = 6 × 100μF Ceramic, 2 x 330μF Polymer
V_{IN} = 12V	Fsw = 650kHz	Internal Bias

Figure 3-10. Startup Using Enable Signal



L = 1μH	V_{OUT} = 6V	C_{OUT} = 6 × 100μF Ceramic, 2 x 330μF Polymer
V_{IN} = 12V	Fsw = 650kHz	Internal Bias

Figure 3-11. Shutdown Using Enable Signal

4 Telemetry

Output voltage telemetry data on the TPS546x24y family of devices is measured on the VOSNS pin. Since this application requires an external divider on the VOSNS pin, the voltage reported is not the actual output voltage of the device. Instead, the voltage reported by the telemetry is the divided voltage on the VOSNS pin. In this design example, the telemetry register is reporting 4.79V.

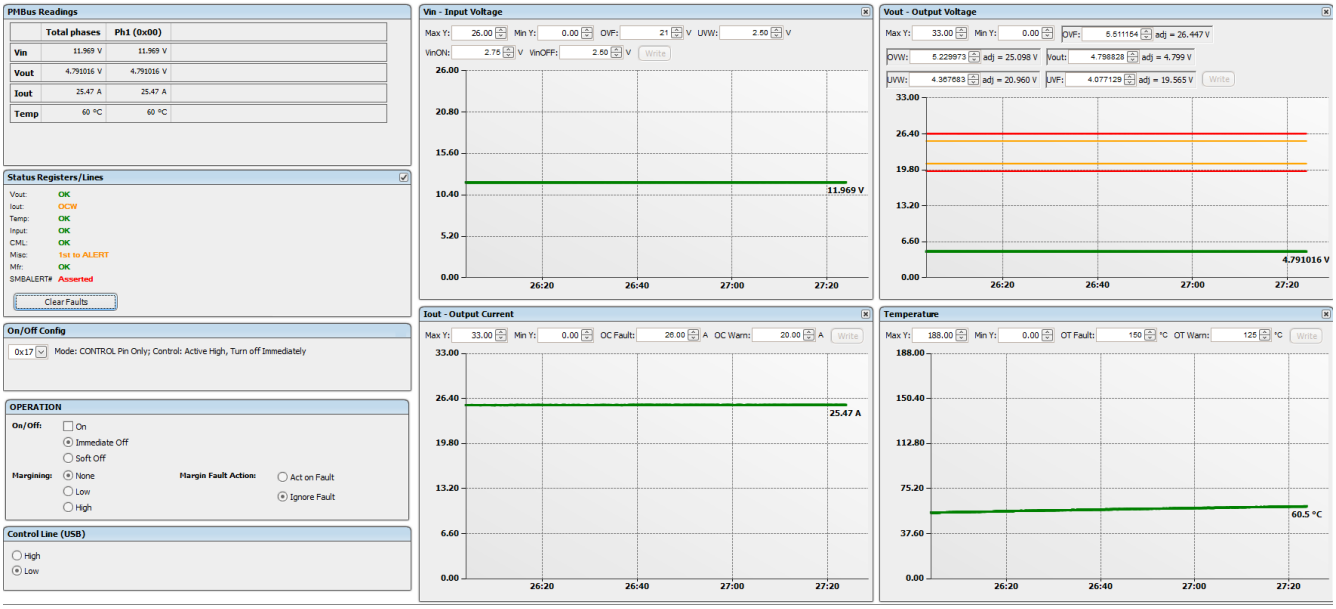


Figure 4-1. TPS546x24y Telemetry Page of Fusion Digital Power Designer GUI

To calculate the actual output voltage, you must multiply the value reported by the telemetry register by the divider ratio, which can be calculated using Equation 9.

Using the reported value of 4.79V from Figure 4-1:

$$V_{OUT\_ACTUAL} = V_{OUT\_TELEMETRY} \times \left(\frac{R_{TOP}}{R_{BOTTOM}} + 1\right) = 4.79V \times \left(\frac{255\Omega}{1020\Omega} + 1\right) = 5.99V \quad (4)$$

All other telemetry values remain the same, even when using an external divider on the VOSNS pin.

5 Overvoltage and Undervoltage Protection

The TPS546x24y family utilizes a programmable overvoltage and undervoltage protection through the PMBus™ register (40h)VOUT_OV_FAULT_LIMIT, and (44h)VOUT_UV_FAULT_LIMIT, respectively. The voltage on the VOSNS pin is monitored to provide overvoltage (OV) and undervoltage (UV) protection.

The circuit for (40h)VOUT_OV_FAULT_LIMIT is implemented as a fixed percentage of the current output voltage target. The circuit supports values from 105% to 140% of VOUT_COMMAND in 2.5% steps. When output conversion is disabled, the circuit supports values from 110% to 140% of VOUT_COMMAND in 10% steps.

The circuit for (44h)VOUT_UV_FAULT_LIMIT is implemented as a fixed percentage relative to the current output voltage target. The circuit supports values from 60% to 95% of VOUT_COMMAND in 2.5% steps.

The percent limit programmed for both the overvoltage and undervoltage fault limit still apply to this application, where the voltage on the VOSNS pin is stepped down through a voltage divider. The default programmed overvoltage and undervoltage limit for a TPS546x24y is 115% and 85%, respectively.

In the example application, we set VOUT_COMMAND to 4.8V at startup using our pin-strap network on the VSEL pin. Using our default programmed OV/UV limits, the calculated voltage required on the VOSNS pin to trigger overvoltage protection (OVP) is:

$$V_{VOSNS\_OVP} = \text{VOUT\_COMMAND} \times \text{PROGRAMMED OVP THRESHOLD} \quad (5)$$

$$V_{VOSNS\_OVP} = 4.8V \times 115\% = 5.52V \quad (6)$$

and the calculated voltage required on the VOSNS pin to trigger the undervoltage protection (UVP) is:

$$V_{VOSNS\_UVP} = \text{VOUT\_COMMAND} \times \text{PROGRAMMED UVP THRESHOLD} \quad (7)$$

$$V_{VOSNS\_UVP} = 4.8V \times 85\% = 4.08V \quad (8)$$

We can now apply the voltage division factor of the external feedback divider placed on the VOSNS pin:

$$V_{OUT} = V_{VOSNS} \times \left(\frac{R_{TOP}}{R_{BOTTOM}} + 1\right) \quad (9)$$

Plugging in the calculated V_{VOSNS_OVP} into the V_{VOSNS} term of Equation 9, we can solve for the required V_{OUT} voltage required to trigger an OVP:

$$V_{OUT\_OVP} = V_{VOSNS\_OVP} \times \left(\frac{R_{TOP}}{R_{BOTTOM}} + 1\right) = 5.52V \times \left(\frac{255\Omega}{1020\Omega} + 1\right) = 6.9V \quad (10)$$

The required V_{OUT} to trigger a UVP is:

$$V_{OUT\_UVP} = V_{VOSNS\_UVP} \times \left(\frac{R_{TOP}}{R_{BOTTOM}} + 1\right) = 4.08V \times \left(\frac{255\Omega}{1020\Omega} + 1\right) = 5.1V \quad (11)$$

To simplify this calculation, we can observe that the calculated V_{OUT_OVP} is 115% of the set V_{OUT} = 6V. The calculated V_{OUT_UVP} is 85% of the set V_{OUT} = 6V.

From this, we can conclude that the percentage limit set for OVP/UVP scales to the V_{OUT} voltage, even with a resistor divider on the VOSNS pin.

Note

Although the absolute maximum rating of the VOSNS pin is 5.5V, the VOSNS pin has enough margin to support up to 6V_{OUT} through a VOUT_COMMAND change without using any external dividers. The caveat to this method is the delay involved from having to boot the system to 5.5V, and then programming V_{OUT} to 6V using VOUT_COMMAND after the system has initialized.

6 Limitations

So long as V_{VOSNS} stays below it's absolute maximum rating of 5.5V, the device can regulate to a given V_{out} given that the difference between V_{in} and V_{out} has enough overhead to account for efficiency losses due to conversion, and does not violate the minimum T_{on} and minimum T_{off} of the PWM controller that controls the high-side FET and low-side FET. Below are equations that you can use to determine the limits of your design:

$$f_{SW(MAX)} = \frac{V_{OUT}}{V_{IN(MAX)} \times t_{OFF(MIN)} \times \eta} \quad (12)$$

$$V_{OUT(MAX)} = V_{IN(MAX)} \times \left(1 - f_{sw} \times t_{OFF(MIN)}\right) \times \eta \quad (13)$$

where the $t_{OFF(MIN)}$ of the TPS546x24y is 400ns nominal and 500ns maximum. We recommend the reader use the 500ns maximum $t_{OFF(MIN)}$ in any maximum V_{OUT} and f_{SW} calculations.

For higher values V_{OUT}, a safe assumption for efficiency, assuming a low DCR inductor, is >= 90%. Proper conversion must be verified on an evaluation board before being implemented in mass production.

7 Summary

The TPS546x24y family supports output voltages above 5.5V by placing an external resistor divider between V_{OUT} and the VOSNS pin, scaling the feedback signal within the pin's 0.25V–5.5V operating range.

Divider resistors must be 1kΩ or below to avoid loading errors from the TPS546D24A's internal VOSNS to GOSNS resistance.

If the designer chooses to use VOUT_TRIM to fine-tune V_{OUT}, the value programmed into VOUT_TRIM can be added to V_{OUT} in Equation 3 to calculate the new V_{OUT}

A 6V output design using the TPS546B24A (12V input, 25A, 650kHz) with R_{TOP} = 255Ω and R_{BOTTOM} = 1.02kΩ achieves 96.2% full-load efficiency, 3.30mV output ripple at full load, and a 323.9mV transient at a 10A step with a slew rate of 1A/µs.

Telemetry reports the attenuated VOSNS voltage, not the actual output; use Equation 4 to calculate the actual V_{OUT}.

Overvoltage and undervoltage fault thresholds (default 115%/85% of VOUT_COMMAND) apply to the VOSNS pin voltage and scale correctly to V_{OUT} even with the external divider in place.

Maximum output voltage and switching frequency are constrained by the 500ns minimum t_{OFF} of the PWM controller; use the provided equations in Section 6 to verify headroom before production.

For output voltages at or just above 5.5V, an alternative approach is to boot the device to 5.5V and then program V_{OUT} via VOUT_COMMAND over PMBus, avoiding the need for an external divider entirely.

The designer can still use the TPS546x24A Compensation and Pin-Strap Resistor Calculator to determine compensation settings, even when plugging in V_{OUT} values higher than 5.5V.

8 References

- Texas Instruments, TPS546B24A 2.95-V to 18-V, 20-A, Up to 4× Stackable, PMBus® Buck Converter, datasheet.

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