Functional Safety Information

TMP175-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TMP175-Q1 (SOIC-8 and VSSOP-8 packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

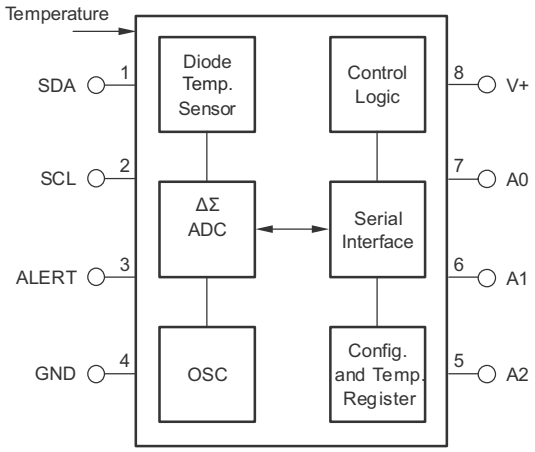

Figure 1-1. Functional Block Diagram

The TMP175-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SOIC-8 Package

This section provides functional safety failure in time (FIT) rates for the SOIC-8 package of the TMP175-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	9
Die FIT rate	2
Package FIT rate	7

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 3mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 VSSOP-8 Package

This section provides functional safety failure in time (FIT) rates for the VSSOP-8 package of the TMP175-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	6
Die FIT rate	2
Package FIT rate	4

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 3mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TMP175-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Serial communication error	20
VOUT out of specification	55
VOUT stuck high	5
VOUT stuck low	5
ALERT false trip, fails to trip	15

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TMP175-Q1 (SOIC-8 and VSSOP-8 packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TMP175-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TMP175-Q1 datasheet.

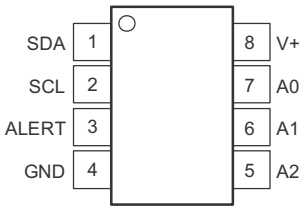

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- A bypass capacitor of 0.1µF on the input voltage pin is implemented.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SDA	1	The SDA pin is stuck low. I2C communication is not possible.	B
SCL	2	The SCL pin is stuck low. I2C communication is not possible.	B
ALERT	3	The ALERT pin is stuck low. The functionality of the ALERT pin is not available.	B
GND	4	There is no effect on the device. The device operates as normal.	D
A2	5	The I2C address selection is limited. I2C communication is potentially corrupted.	B
A1	6	The I2C address selection is limited. I2C communication is potentially corrupted.	B
A0	7	The I2C address selection is limited. I2C communication is potentially corrupted.	B
V+	8	The device is not functional and potentially damaged.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SDA	1	The state of the SDA pin is undetermined. I2C communication is not possible.	B
SCL	2	The state of the SDA pin is undetermined. I2C communication is not possible.	B
ALERT	3	The functionality of the ALERT pin is not available.	B
GND	4	The functionality of the device is undetermined.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
A2	5	The I2C address selection is limited. I2C communication is potentially corrupted.	B
A1	6	The I2C address selection is limited. I2C communication is potentially corrupted.	B
A0	7	The I2C address selection is limited. I2C communication is potentially corrupted.	B
V+	8	The functionality of the device is undetermined.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
SDA	1	SCL	I2C communication is not possible.	B
SCL	2	ALERT	The functionality of the ALERT pin is not available.	B
ALERT	3	GND	The ALERT pin is stuck low. The functionality of the ALERT pin is not available.	B
GND	4	A2	The I2C address selection is limited. I2C communication is potentially corrupted.	B
A2	5	A1	The I2C address selection is limited. I2C communication is potentially corrupted.	B
A1	6	A0	The I2C address selection is limited. I2C communication is potentially corrupted.	B
A0	7	V+	The I2C address selection is limited. I2C communication is potentially corrupted.	B
V+	8	SDA	The SDA pin is stuck high. I2C communication is not possible.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SDA	1	The SDA pin is stuck high. I2C communication is not possible.	B
SCL	2	The SCL pin is stuck high. I2C communication is not possible.	B
ALERT	3	The ALERT pin is stuck high. The functionality of the ALERT pin is not available.	B
GND	4	The functionality of the device is undetermined. The device is potentially damaged.	A
A2	5	The I2C address selection is limited. I2C communication is potentially corrupted.	B
A1	6	The I2C address selection is limited. I2C communication is potentially corrupted.	B
A0	7	The I2C address selection is limited. I2C communication is potentially corrupted.	B
V+	8	There is no effect on the device. The device operates as normal.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

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