Analog Engineer's Circuit

Laser and Modulator Biasing Power Circuit for Optical Module Systems

Data Converters

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Design Objective

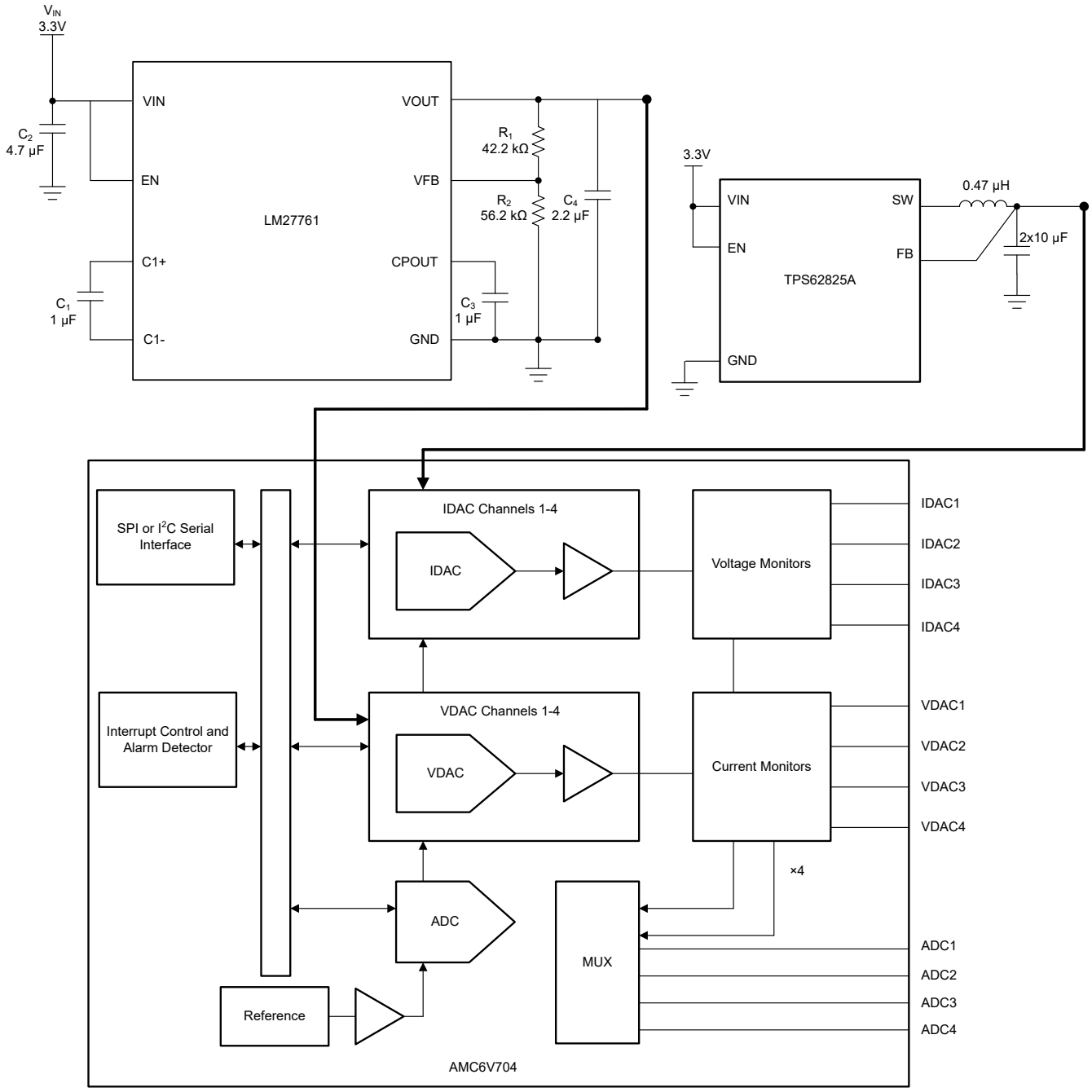
Design a cost-effective, efficient, small, competitive circuit to consolidate AMC60704 power supply rails for biasing *current output digital-to-analog converters* (IDAC) and *voltage output digital-to-analog converters* (VDAC).

Input Supply	Operating Range		Recommended Device
	Minimum	Maximum	
PVDD	1.5V	2.2V	TPS62825A
VSS	–5.5V	–2.5V	LM27761

Design Description

This circuit design creates a method to allow one main 3.3V power supply to supply multiple AMC60704 inputs. Important supplies are PVDD which supplies the IDAC that biases the lasers in an electro-absorption modulated laser (EML). Another important supply is VSS which is the input that supplies the VDAC in the negative range because VSS is used for biasing the electro-absorption modulator (EAM) in an EML.

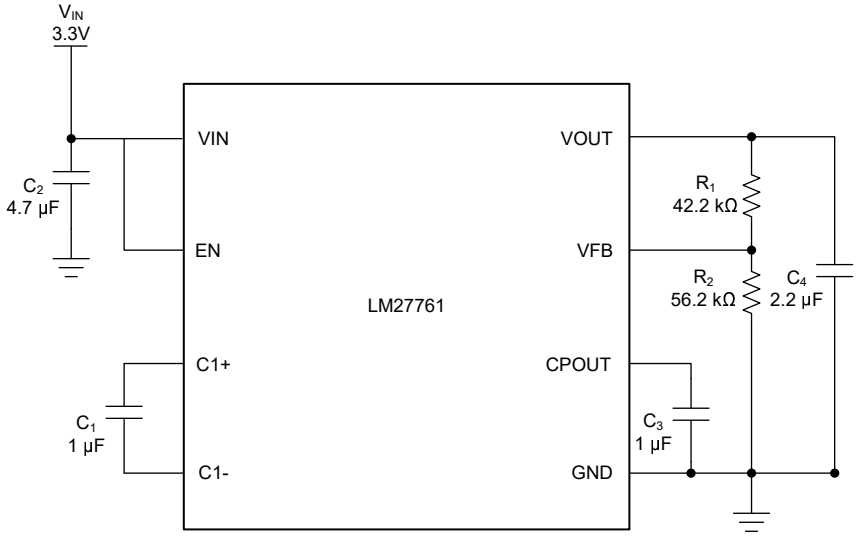
Placing DC/DC converters on the PVDD and VSS rails allow the designers to provide a 3.3V supply and the converters step down and invert the input voltage to the desired value in range for PVDD and VSS. The suggested TPS6285A and LM27761 devices are small, low-cost, and efficient DC/DC converters that can step down and invert input voltages for PVDD and VSS. This design can be used in optical module applications for 400G. Additionally, 800G designs can be created but the 800G design requires an extra AMC60704 and LM27761 device.



Application Block Diagram

Design Notes

1. This design focuses on EML applications, thus VCC, the positive rail is grounded.
2. This design can be used in 400G applications. Additionally, an 800G design can be created but the 800G design requires an extra AMC60704 and LM27761.
3. For biasing the VDACs in an EML application, the operating range for the VSS is rail is –2.5V to –5.5V. This circuit design uses –3.3V to supply the VDACs.
4. The AMC60704 has four VDAC channels each capable of a 50mA output. In 400G applications, all 4 channels are used. This circuit design uses all four VDAC channels.
5. The LM27761 has a maximum output current of 250mA and a configurable output range of –1.5V to –5V making the device a good fit for the VSS rail. The following *image* shows a typical LM27761 schematic.

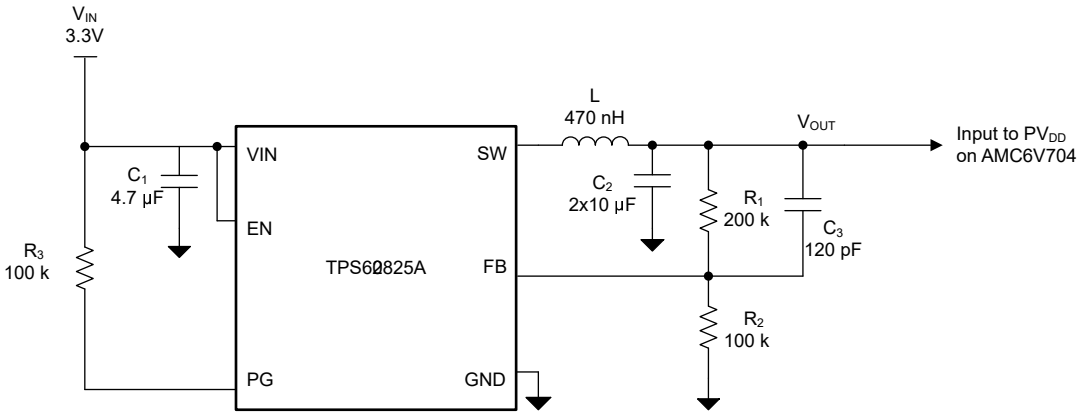


LM27761

6. The output voltage of the LM27761 is externally configurable. The values of R_1 and R_2 determine the output voltage setting. Use Equation to calculate the output voltage. The value for R_2 must be no less than 50kΩ.

$$V_{OUT} = -1.22V \times \left(\frac{R_1 + R_2}{R_1}\right)$$

   - This design operates at –2.85V VSS, thus R_1= 30.1kΩ and R_2 = 39kΩ, to allow enough headroom for current sourcing.
7. Different output capacitance values can be used to reduce charge pump ripple, shrink the design size, or cut the cost of the design. In typical applications, a 4.7µF low-ESR ceramic charge-pump output capacitor (C_3) is recommended.
8. Increasing the input capacitance results in a proportional decrease in input voltage ripple. Input voltage, output current, and flying capacitance also affect input ripple levels to some degree. A 4.7µF low-ESR ceramic capacitor is recommended on the input.
9. Flying capacitance can impact both output current capability and ripple magnitudes. In typical high-current applications, 0.47µF or 1µF 10V low-ESR ceramic capacitors are recommended for the flying capacitors.
10. The LDO output capacitor (C_4) value and the ESR affect stability, output ripple, output noise, PSRR and transient response. The LM27761 only requires the use of a 2.2µF ceramic output capacitor for stable operation.
11. For biasing the IDACs in an EML application, the operating range for the PVDD rail is 1.5V to 2.2V. This circuit design uses 1.8V to supply the IDACs.
12. The AMC6V704 has four IDAC channels each with a 200mA full scale output. The maximum output current for the IDACs is 800mA.
13. The TPS62825A is selected for this design because the device has a maximum output current of 2A and adjustable output voltage range from 0.6V to 4V. These converters maintain a continuous conduction mode operation and keep the output voltage ripple very low across the whole load range. The following *image* shows a typical TPS62825A schematic.



TPS62825A Schematic

14. Use the following equation to set the output voltage on the TPS62825A.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

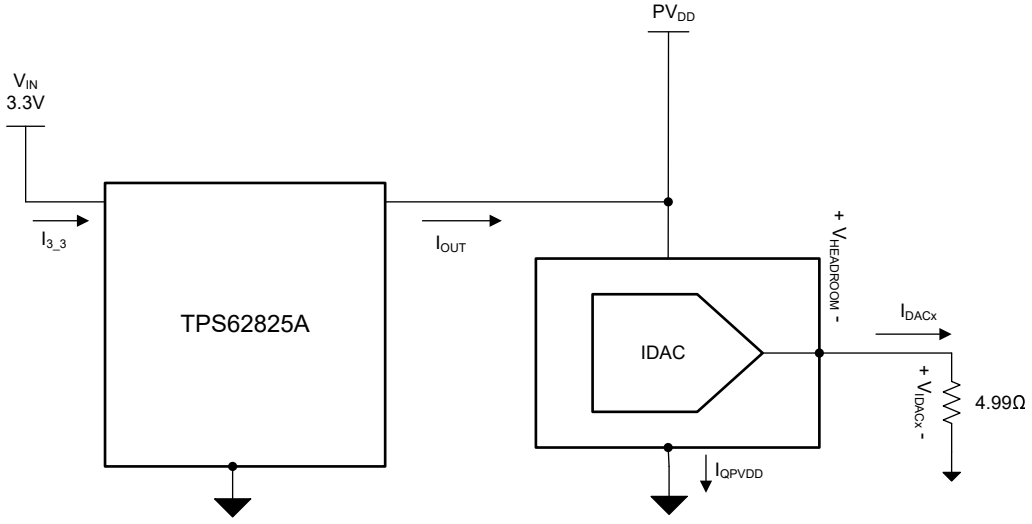
where

- V_{FB} is 0.6V

15. R_2 must not be greater than 100kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity. The following equation shows how to compute the value of the feedforward capacitor, C_3 for a given R_2 value. For the recommended 100kΩ value for R_2, a 120pF feedforward capacitor is used.

$$C_3 = \frac{12\mu}{R_2}$$

16. Considering the DC-bias derating the capacitance, the minimum effective output capacitance, C_2, is 10µF for the TPS62825A.
17. A minimum effective input capacitance, C_1, of 3µF must be present, though a larger value reduces input current ripple. A 4.7µF input capacitor is used for the TPS62825A.
18. Adding the TPS62825A to the system, the power dissipation of the IDACs is now a function of the TPS62825A output voltage and current output, PVDD supply voltage, the current output, and the voltage of the IDAC pin. The power dissipation is calculated using this equation. The $V_{HEADROOM}$ voltage is calculated as the difference between PVDD and V_{IDACx}.



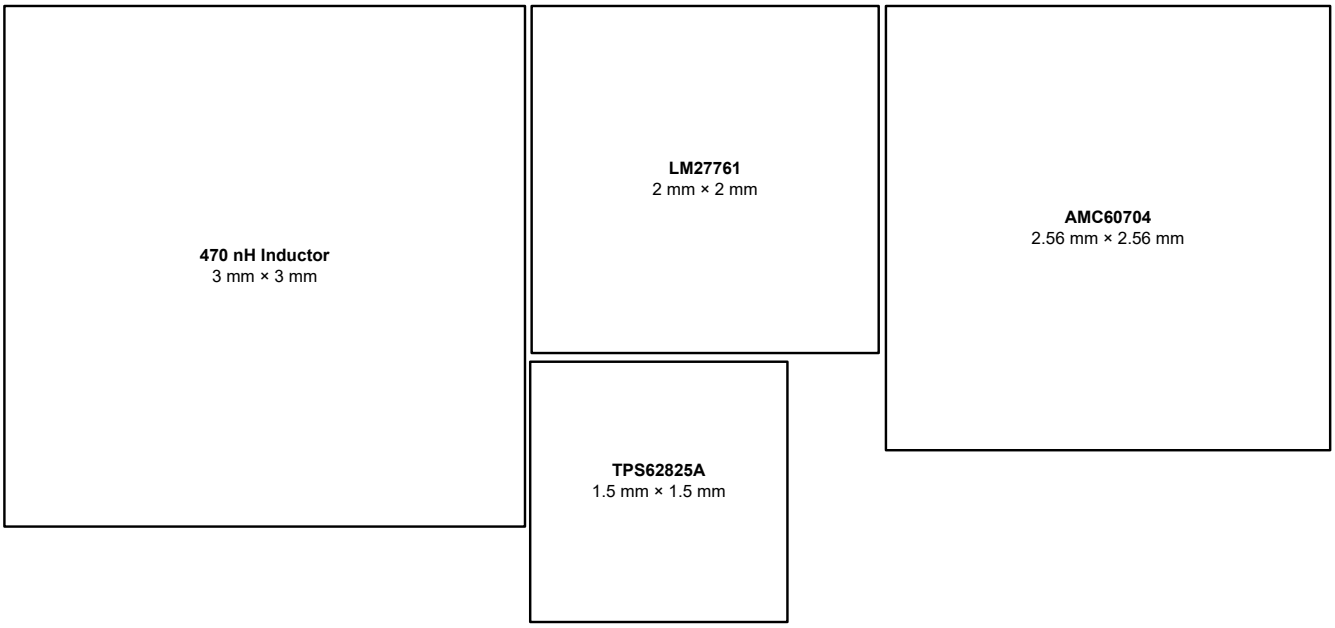
PVDD Power Dissipation

19. $P_{TPS62825A} = 3.3V \times I_{3\_3} - \left[P_{VDD} \times I_{OUT} + P_{VDD} \times I_{QPVDD} + \Sigma_{IDAC0-3}\{V_{HEADROOM} \times I_{DACx}\}\right]$

    a. The power dissipation can be reduced by minimizing the voltage difference, $V_{HEADROOM}$, between PVDD supply and V_{IDAC}. The minimum PVDD is 1.5V.
    b. The output load can be calculated using the following equation.

$$LOAD = \frac{V_{IDAC}}{I_{DAC}}$$

20. *Package Size Comparison* shows the products used in this design. Selecting the key passive components was previously discussed. For more complete details, see the product data sheet. A key requirement for this design is small package size due to high channel density within an optical module. The following *image* shows the package size comparison.



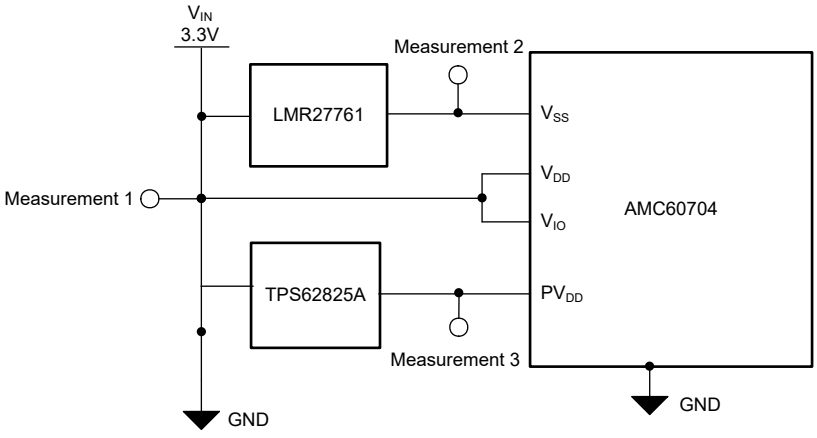
Package Size Comparison

21. To compete in this market, this design creates a low-cost answer against integrated devices.

Design Measurements

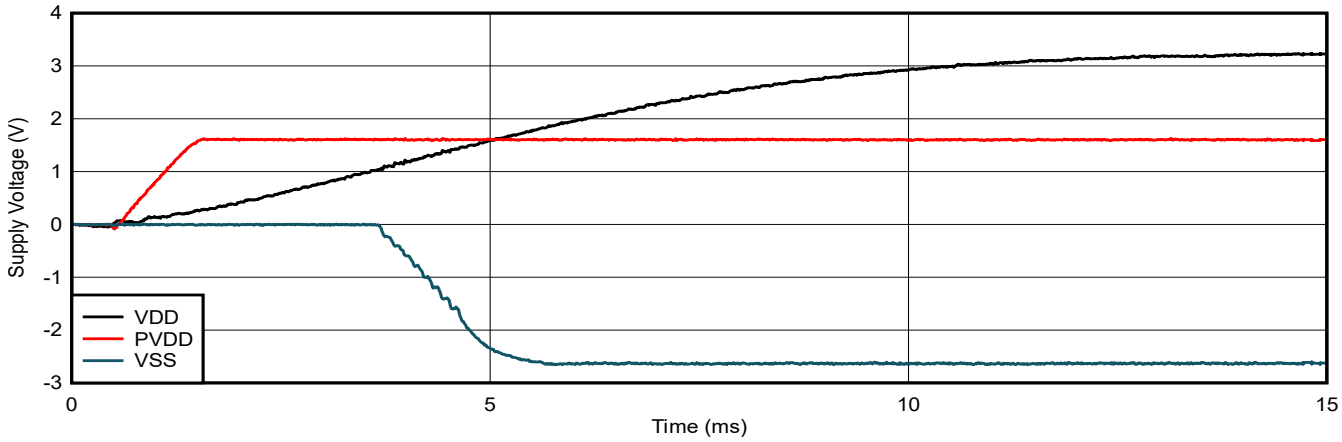
Test 1: Power Supply Ramp-Up Response

Power Supply Ramp-Up Response shows the power supply ramp-up response test setup and test points.



Power Supply Ramp-Up Response

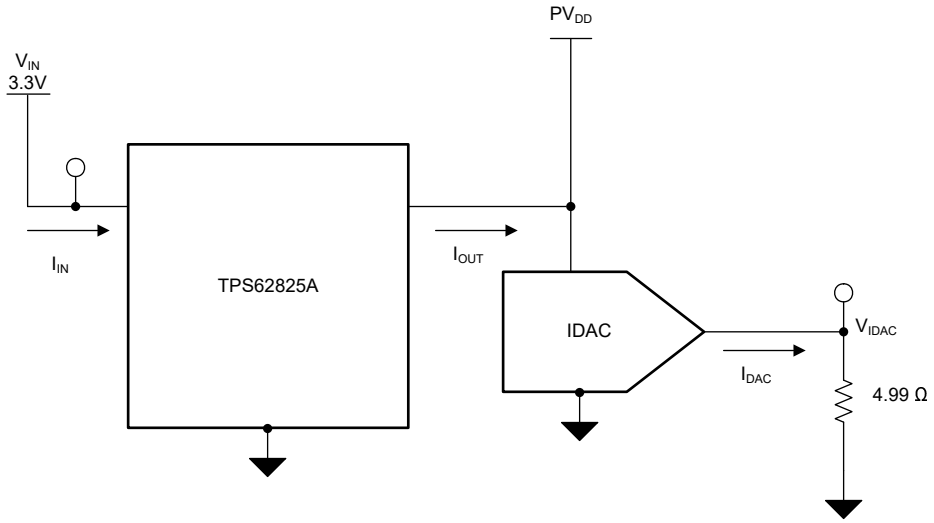
The *Power Supply Ramp-Up Response* graph shows the time required after a power-on trigger occurs for the power supplies in the system to respond. The Tektronix TBS 2000B oscilloscope was used to probe each power supply input to measure the ramp-up for this test.



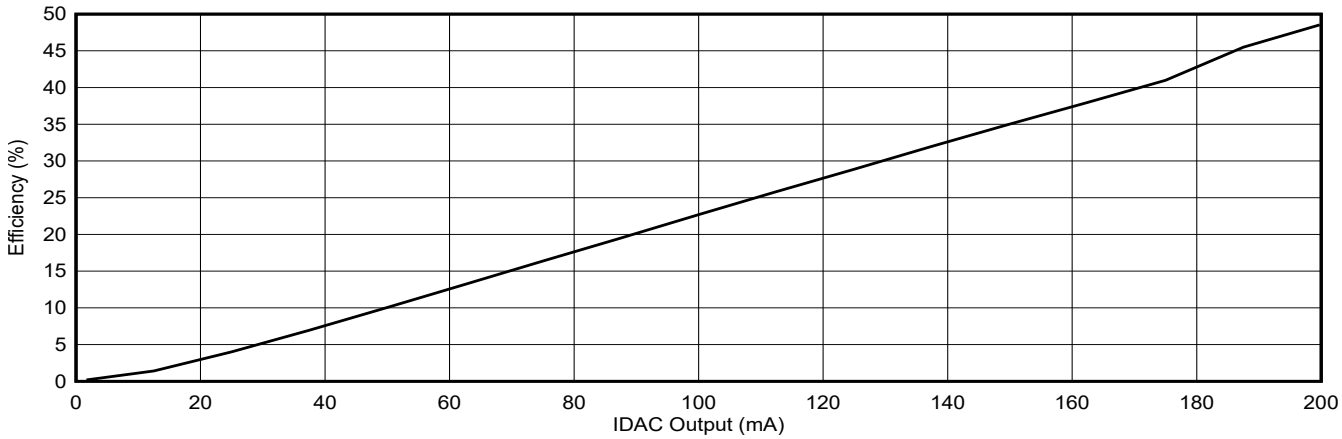
Power Supply Ramp-Up Response

Test 2: Power Efficiency of System vs IDAC

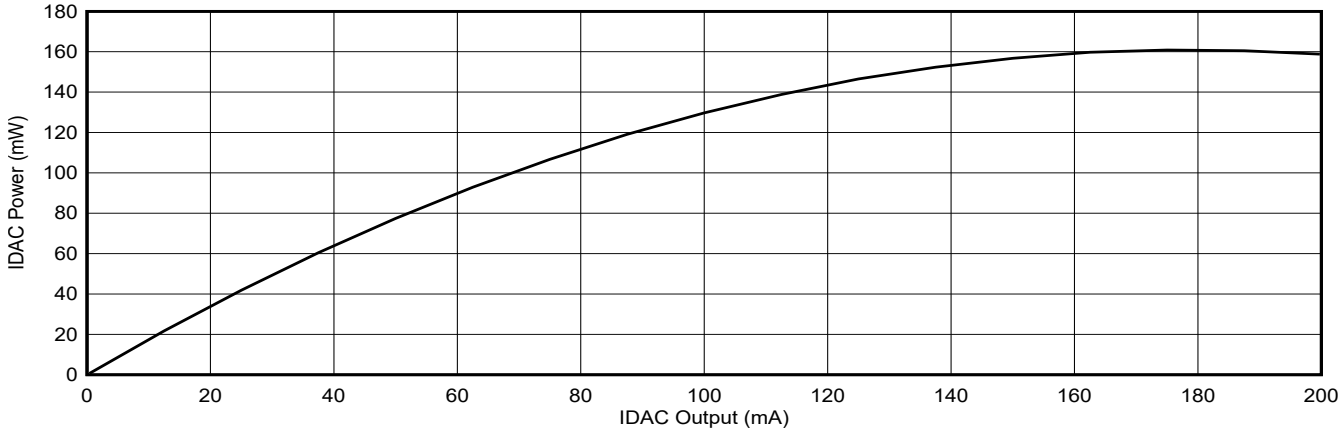
This efficiency test measures the power dissipation at the input supply of the TPS62825A against the power dissipation of the IDAC with a 4.99Ω load. As the IDAC codes change, the output of the IDAC as well as the input power changes. *IDAC Test Setup* shows the setup for this test.



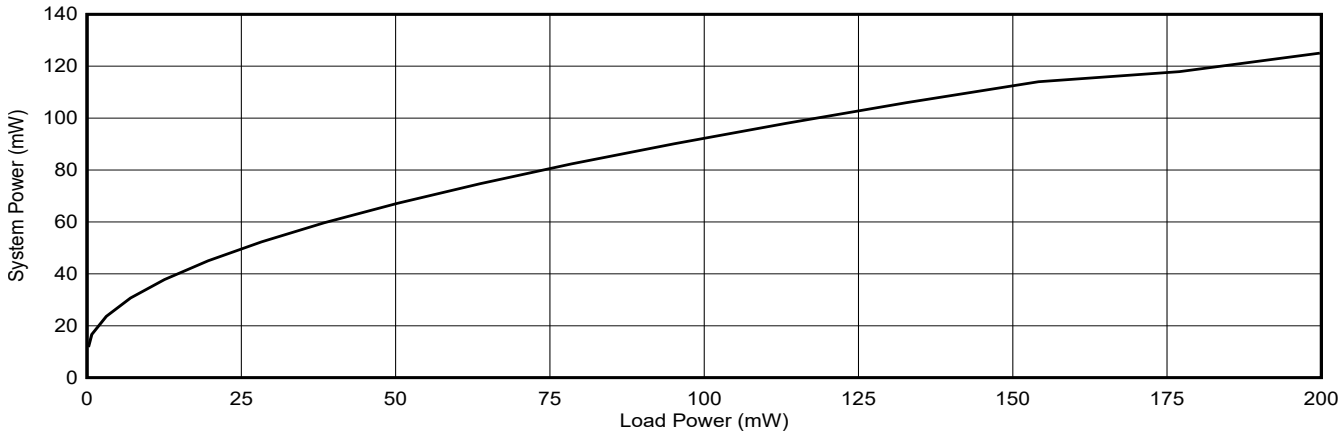
IDAC Test Setup



IDAC Efficiency vs IDAC Output



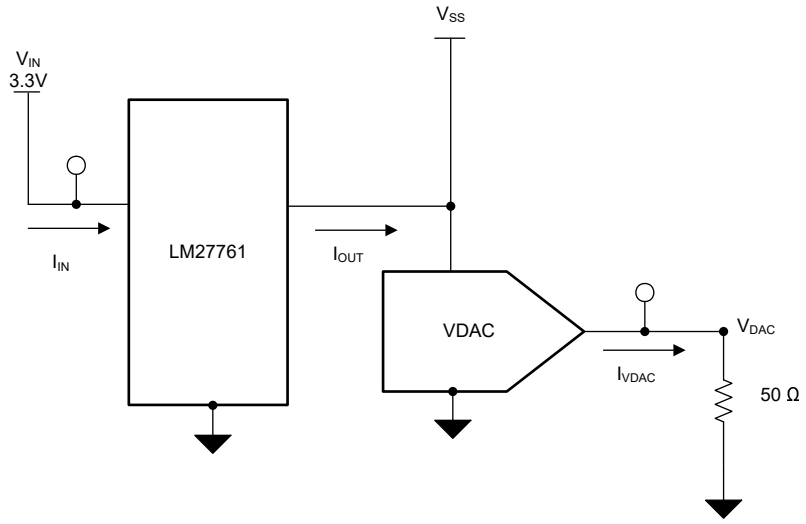
IDAC Power vs IDAC Output



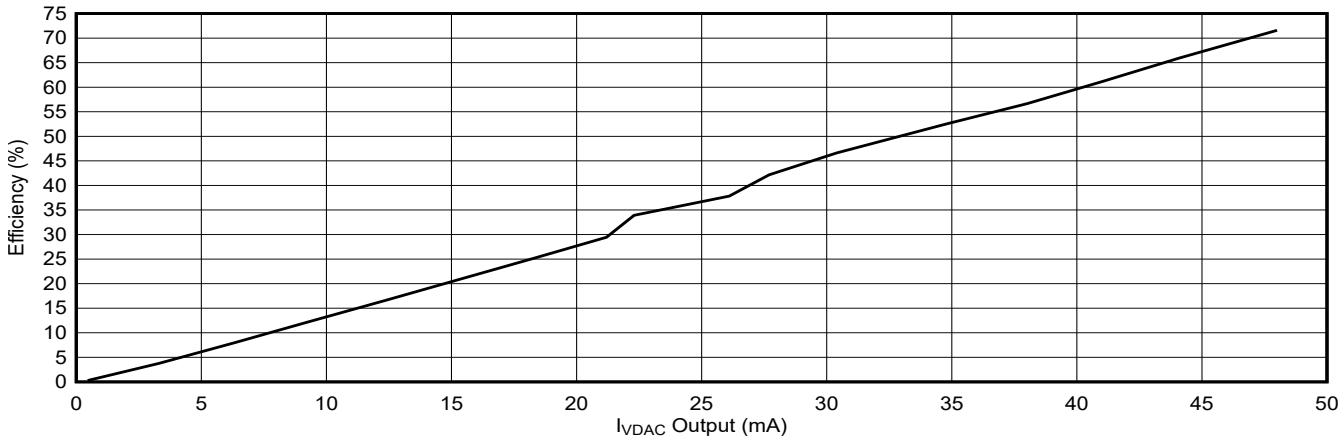
IDAC System Power vs IDAC Output

Test 3: Power Efficiency of System vs VDAC

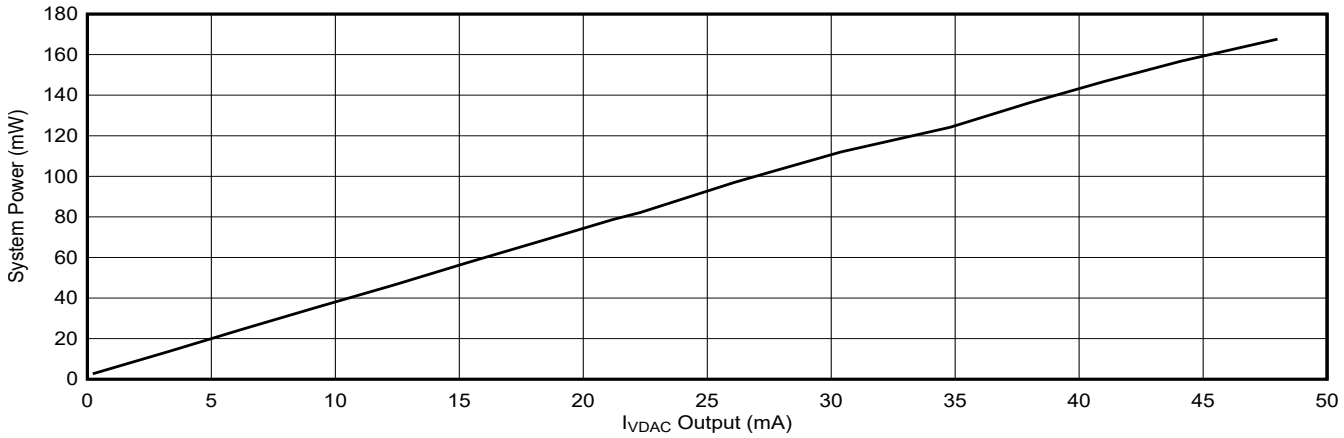
This test shows the power dissipation of the input supply from the LM27761 and the output of the VDAC. The following *image* shows the setup and test points. Using a DMM in a current measurement configuration, measuring the input current of the LM27761 can be used to calculate the power of the system. By changing the VDAC codes, the output of the VDAC changes as well as the system current. Placing a load resistor at the output allows for the calculation of the current flowing through the load. For a maximum output current of 50mA at full scale voltage output of –2.5V, the maximum resistive load is 50Ω.



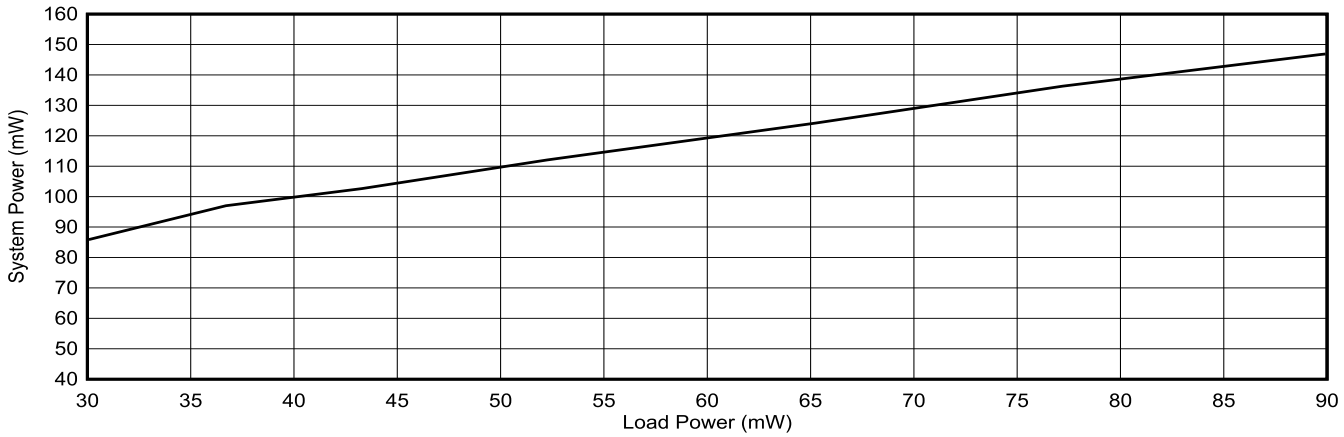
VDAC Test Setup



VDAC Efficiency vs VDAC Current Drive Output



VDAC System Power vs VDAC Current Drive Output



VDAC System Power vs Load Power

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
AMC6V704	Optical controller with four 200mA current DACs, four voltage-output DACs and a multichannel ADC	AMC6V704	AMC60704
TPS62825A	2.4V to 5.5V input, 2A step-down converter with forced PWM in 1.5mm × 1.5mm VSON-HR package	TPS62825A	TPSM82822
LM27761	Low-noise regulated inverter with integrated LDO for an input voltage in the range of 2.7V to 5.5V	LM27761	LM27762

Additional Resources

- Texas Instruments, *TPS6282xAEVM-126 Evaluation Module User's Guide*
- Texas Instruments, *LM27761EVM User's Guide*
- Texas Instruments, *Low-noise charge pumps make it easy to create negative voltages technical article*
- Texas Instruments, *AMC6V704 Evaluation Module User's Guide*
- Texas Instruments, *AMC6V704 4-Channel Optical Monitor and Controller With Current and Voltage Output DACs and Multichannel ADC Data Sheet*
- Texas Instruments, *AMC6V704EVM Evaluation Board Tool Page*

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