Application Note

TDP142 Configuration Guide

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ABSTRACT

The TDP142 is a linear redriver that supports DisplayPort 1.4 up to HBR3 (8.1Gbps). At these higher data rates, signal integrity issues place limitations on system trace length. The TDP142 provides 16 levels of receive linear equalization to compensate for board loss due to inter-symbol interference (ISI). This document is intended to provide general guidelines on how to use the TDP142 in a source/sink application.

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1 Introduction

The TDP142 is a DisplayPort™ linear redriver intended to support up to HBR3 (8.1Gbps) for each lane. Additionally, the transparency to the DP link training makes TDP142 a position independent device, designed for source or sink application. DisplayPort standards define a minimum eye height and width at the end of a channel in which a compliant receiver must operate. Longer trace lengths add ISI contributing to the loss of the channel which closes the eye such that the eye height and width are no longer compliant and the receiver cannot reliably recover the data on that channel. The TDP142 provides equalization gain to compensate for the board trace loss due to ISI and restore to a compliant eye.

2 Device Configuration

The TDP142 supports configuration modes in GPIO and I2C Mode. Table 2-1 details 4-level control pin settings of TDP142. Table 2-2 details TDP142 mode configurations based on the pin setting. If the device is configured in GPIO mode, please refer to Table 2-2 for pin configurations to enable DisplayPort and AUX Snoop feature and Table 3-1 for DPEQ1 and DPEQ0 pin configuration to change equalization setting. Please refer to *TDP142 DisplayPort™ 8.1 Gbps Linear Redriver*, data sheet for configuration details and register mapping over I2C.

Table 2-1. 4-Level Control Pin Settings

Level	Settings
0	Option 1: Tie 1kΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20kΩ 5% to GND.
F	Float (Leave pin open)
1	Option 1: Tie 1kΩ 5% to VCC. Option 2: Tie directly to VCC

Table 2-2. TDP142 Mode Configuration

I2C_EN	Configuration
F	I2C Enabled at 1.8V
1	I2C Enabled at 3.3V
0	GPIO Mode

Table 2-3. TDP142 GPIO Mode Configuration

DPEN/HPDIN	SNOOPENZ/RSVD8	Configuration
1	-	DisplayPort Enabled
0	-	DisplayPort Disabled
-	1	AUX Snoop Enabled
-	0	AUX Snoop Disabled

3 Equalization Selection

The TDP142 used in a source/sink application enables the system to pass both transmitter electrical compliance for DisplayPort 1.4 and receiver jitter tolerance compliance testing for DisplayPort 1.4. The TDP142 recovers incoming data from the source and to the sink by applying equalization that compensates for the channel insertion loss. The equalization can be set based on the amount of insertion loss of the channel before the TDP142 receivers (Pre-Channel) and some insertion loss of the channel after the TDP142 (Post-Channel). In the GPIO or pin strap mode, the EQ value of each lane is set globally by configuring the DPEQ[1:0] pins. In the I2C mode, the EQ value of each channel is set independently based on the loss of the individual channel by programming the equivalent registers. The equalization values are detailed in Table 3-1. Typical FR4 trace losses are given in Table 3-2.

Table 3-1. TDP142 Equalization

Equalization Setting Number	All DisplayPort Lanes		
	DPEQ1 Pin Level	DPEQ0 Pin Level	EQ GAIN at 4.05GHz (dB)
0	0	0	1.0
1	0	R	3.3
2	0	F	4.9
3	0	1	6.5
4	R	0	7.5
5	R	R	8.6
6	R	F	9.5
7	R	1	10.4
8	F	0	11.1
9	F	R	11.7
10	F	F	12.3
11	F	1	12.8
12	1	0	13.2
13	1	R	13.6
14	1	F	14.0
15	1	1	14.4

Table 3-2. Example FR4 Trace Loss

4-mil Wide FR4 PCB Trace Length (Inches)	Loss at 2.5GHz (0.49dB/inch) (dB)	Loss at 4.05GHz (0.73dB/inch) (dB)	Loss at 5GHz (0.87dB/inch) (dB)
1	0.5	0.7	0.9
2	1	1.5	1.7
3	1.5	2.2	2.6
4	2	2.9	3.5
5	2.5	3.7	4.3
6	2.9	4.4	5.2
7	3.4	5.1	6.1
8	3.9	5.9	7
9	4.4	6.6	7.8
10	4.9	7.3	8.7

4 Equalization Selection Example

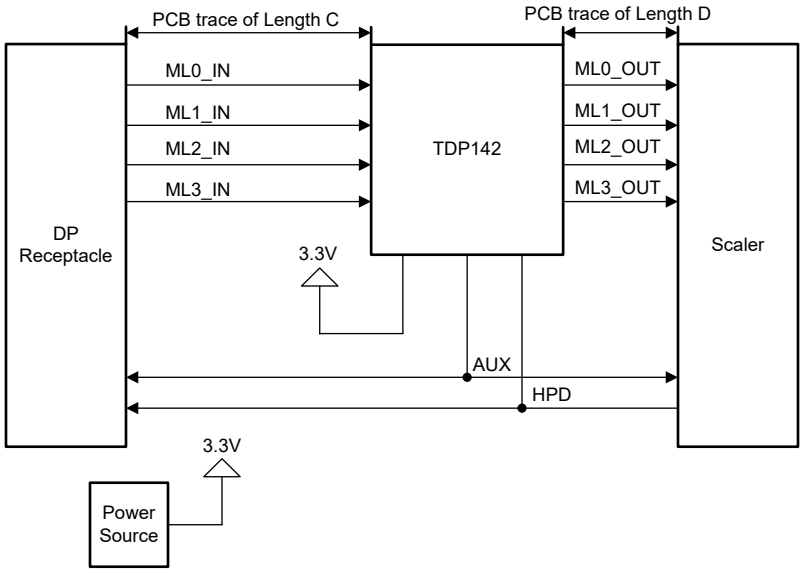

Figure 4-1. TDP142 Sink Side Equalization Example

This section discusses an example to select equalization for different trace length. Figure 4-1 shows an example sink side application of TDP142. The following method is used to select equalization value for this sink side application:

- PCB Trace of Length C = 8 inches FR4 PCB Trace (5.9dB Loss at 4.05GHz). DPEQ setting used = Setting Number 5 (6.5dB).

Other factors such as layout quality and DP driver and receiver quality can require the equalization settings to be adjusted higher or lower for best performance. The previous method is recommended to be used for selecting initial configuration settings based on system board trace lengths.

5 AUXP/N and SNOOPENZ Configuration

TDP142 uses AUXp and AUXn pins to snoop AUX. AUX snooping enables TDP142 to monitor the native AUX traffic as the traffic traverses between DisplayPort source and DisplayPort sink. The TDP142 snoops native AUX writes to DisplayPort sink's DPCD registers 0x00101 (LANE_COUNT_SET) and 0x00600 (SET_POWER_STATE). TDP142 disables/enables lanes based on value written to LANE_COUNT_SET. The TDP142 disables all lanes when SET_POWER_STATE is in the D3. Otherwise, active lanes is based on value of LANE_COUNT_SET.

In GPIO mode, AUX snooping is enabled by strapping SNOOPENZ pin low either pulling down to GND directly or to GND with 1k pull down resistor. In I2C mode, AUX snooping is enabled by default. AUX snooping can be disabled by writing 1 to bit 7 of the register 0x13.

When AUX snooping is disabled, all four DisplayPort lanes is active in GPIO mode. In I2C mode, each lane can be enabled or disabled by writing to bit [3:0] of the register 0x13.

AUXP needs to have a 100kΩ pull-down resistor and AUXN needs to have a 100kΩ pull-up resistor for the source. For sink, AUXp has 1M pullup to 3.3V and AUXn has 1M pulldown to GND. These resistors must be on the TDP142 side of the 100nF capacitors.

For the application supporting Dual mode DisplayPort: SNOOPENZ pin must be connected to the CONFIG1 on DisplayPort Receptacle through a buffer like the SN74AHC125. The buffer is needed because the internal pulldown on SNOOPENZ pin is too strong to register a valid VIH when a Dual mode adapter is plugged into the DisplayPort receptacle.

6 Layout Guidelines

The following layout guidelines needs to be used in routing the high-speed DisplayPort signals to and from the TDP142.

- INDP and OUTDP pairs must be routed with controlled 100Ω differential impedance (±10%).
- Keep differential pairs away from other high-speed signals.
- Intra-pair routing needs to be kept to within 5 mils.
- DisplayPort lane inter-pair routing needs to be kept to within 2 UI according to the DisplayPort Design Guide.
- Differential pair length matching needs to be near the location of mismatch.
- Each pair needs to be separated by at least 3 times the signal trace width.
- The use of bends in differential traces needs to be kept to a minimum. When bends are used, the number of left and right bends needs to be as equal as possible and the angle of the bend needs to be ≥ 135°. This can minimize any length mismatch caused by the bends and minimize the impact bends have on EMI.
- Route all differential pairs on the same layer.
- Minimize the number of vias, this is recommended to keep the via count to 2 or less.
- The layout can face signal crossing on OUTDP2 and OUTDP3 due to mismatched order between the output pins of the device and the connector. One of the designs is to do polarity swap on the input of the device when GPU is BGA package. This can minimize the number of VIAS being used. Please refer to Figure 6-1 and Figure 6-2.

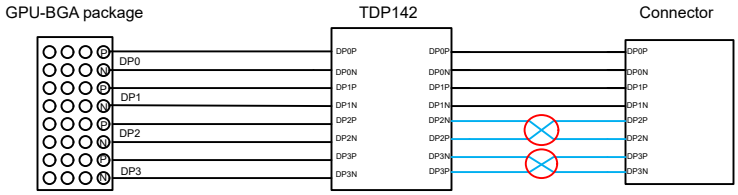

Figure 6-1. Signal Crossing on the Output

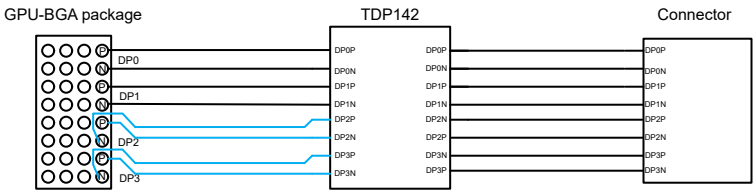

Figure 6-2. INDP2 and INDP3 Polarity Swap

- Keep differential traces on layers adjacent to a ground plane.
- Do not route differential pairs over any split plane.
- If using a through-hole connector, route the high-speed signals on opposite side of the connector such that the connector pin does not create a stub in the transmission line.
- Test points needs to be placed in series and in symmetry to avoid impedance discontinuity.

6.1 GND Stitching

The entirety of any high-speed signal trace needs to maintain the same GND reference plane from origination to termination. If the same GND reference plane is not maintained, via-stitch both GND planes together to make sure continuous grounding and uniform impedance. Place these stitching vias symmetrically within 200mils (Center-to-center, closer is better) of the signal transition vias. See Figure 6-3 for an example of GND stitching vias.

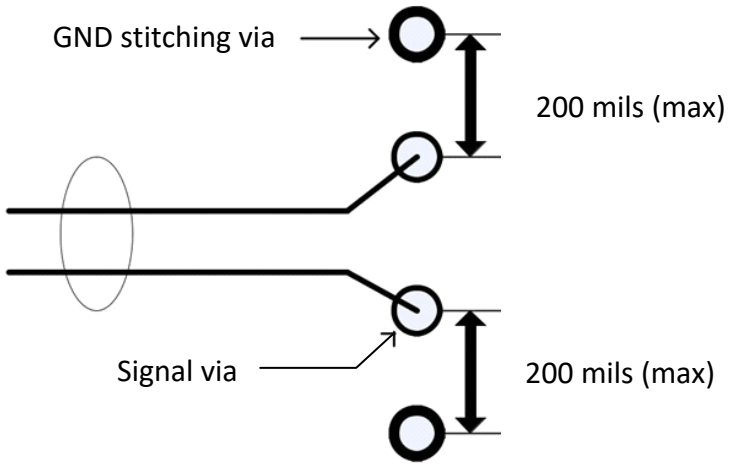

Figure 6-3. GND Stitching Vias Example

6.2 AC-Coupling Capacitors

When placing AC-Coupling capacitors, the recommended component size is 0201. The maximum component size used needs to be 0402. During layout, the AC-Coupling capacitors needs to be placed close to the transmitter pins of the device with symmetrical placement to make sure optimum signal quality and to minimize reflections. Place AC-Coupling capacitors as close to the device as possible or on the transmitter side. Figure 6-4 for AC-Coupling capacitor layout symmetry.

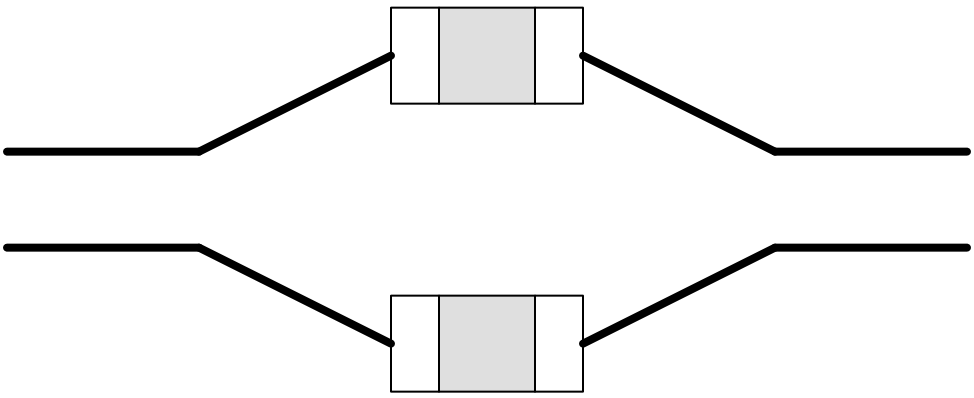

Figure 6-4. AC-Coupling Capacitor Layout Symmetry Example

Note

Adding test points to the high-speed traces can cause impedance discontinuity which negatively impacts signal performance. If test points are used, the test points need to be placed in series and symmetrically. The test points must not be placed in a manner that causes a stub on the differential pair.

6.3 Layout Example

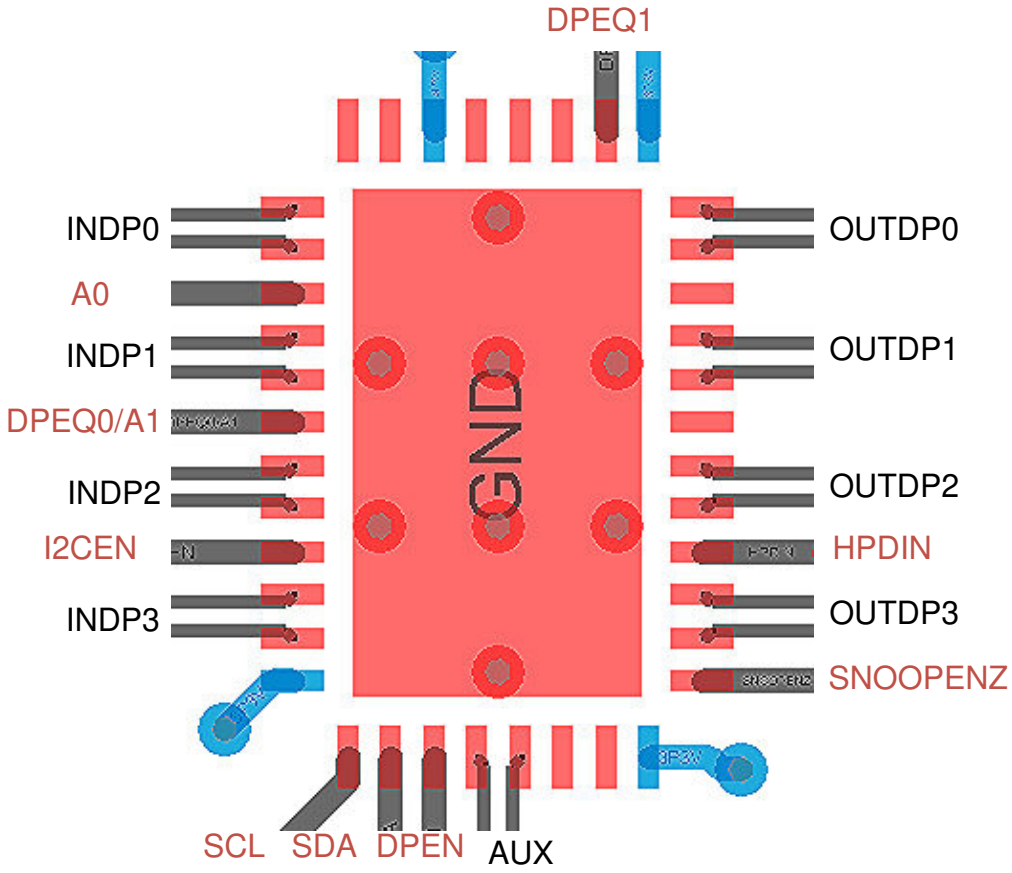

Figure 6-5. Layout Example

7 Summary

This document provides the tools needed to setup and configure the TDP142 in your system. Please refer to this documentation along with the *TDP142 DisplayPort™ 8.1 Gbps Linear Redriver* and *TDP142 Schematic Checklist* for further information.

8 References

- Texas Instruments, *TDP142 DisplayPort™ 8.1 Gbps Linear Redriver*, data sheet

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