Application Report

Common-Anode Power Supply Solution for Common-Cathode LED Display

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ABSTRACT

Due to the increasing popularity of the outdoor video advertising industry, more full-color LED displays appear in areas such as shopping centers, office buildings, exhibition centers, and rail stations. LED display is gradually replacing traditional large-format print advertisement and mechanical flip-type display. The typical size of an outdoor LED display is large, which yields a better visual experience, but inevitably introduces new problems, which can include high-heat generation and high-power consumption. A new common-cathode LED display driving solution recently proposed by the industry significantly reduces the power consumption of LED display.

The key technology of the common-cathode LED display is the innovation of the power supply method. With this method, individual LED colors operate at different power supply voltages to improve system efficiency. The traditional approach is common-cathode (ground) power supply using dual outputs with a flyback or LLC topology. However, this approach has the problems of high cost, large size, and also output cross-regulation issues. This application report provides details about a new common-anode power supply circuit implementation of single output flyback or LLC and synchronous buck converter with sinking current based on the TI device TPS548D22. This is a simple feasible solution to achieve low cost and small size.

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1 Introduction

A LED display (LED matrix display system, LED signage) is a flat-panel display that uses an array of light-emitting diodes as pixels for a video display. The resolution of LED displays continues to increase as pixel pitch becomes smaller to achieve better visual effects. Higher pixel density requires higher power consumption and introduces thermal issues. The traditional common-anode LED display can no longer meet the energy-saving requirements in high-resolution LED displays. In response, the industry has recently proposed a new common-cathode LED display technology suitable for high-resolution LED display.

1.1 LED Driver Methods

The LED forward voltage varies by color. Typically, 1.8 V to 2.2 V for red LED and 2.8 V to 3.4 V for both blue and green LEDs. Figure 1-1, Figure 1-2, and Figure 1-3 show three types of LED driver solutions:

- traditional common-anode
- traditional common-cathode
- new common-cathode

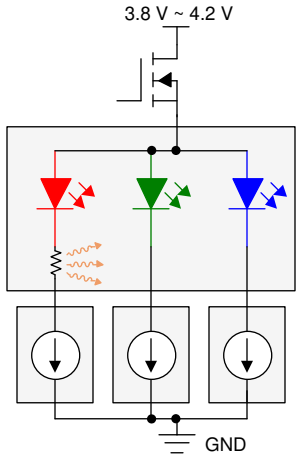

Figure 1-1. Traditional Common-Anode LED Display

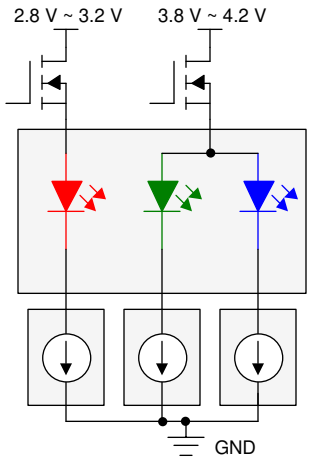

Figure 1-2. Traditional Common-Cathode LED Display

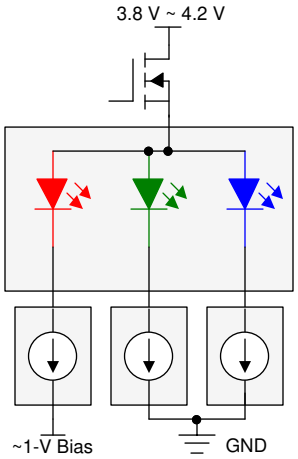

Figure 1-3. New Common-Cathode LED Display

The traditional common-anode LED display (shown in Figure 1-1) uses a single power rail for all three LED colors. The red LED required an additional external resistor in series to limit the voltage across the red LED. The disadvantage is extra power loss due to the resistor. An approach to eliminate the resistor is using common-cathode LED display with red, blue, and green LEDs powered by separate rails, as shown in Figure 1-2 and Figure 1-3.

The traditional common-cathode LED display (drive common-cathode LEDs) shown in Figure 1-2 has two power supplies. One is dedicated to the red LED. The other is for both the blue and green LEDs with ground as a common reference. This power supply is called a common-cathode power supply since the reference is ground (cathode).

The new common-cathode LED display (drive common-anode LEDs) shown in Figure 1-3 uses one supply connected to a common anode for all three LEDs and a second supply that generates a bias voltage for the red LED. This power supply is called a common-anode power supply because the reference is positive to the supply (anode). The key challenge is to generate the 1-V bias supply for the red LED.

Common-anode RGB LEDs share a single electrical connection for the anode of all three LEDs and are powered by a single power supply. Common-cathode RGB LEDs have two power supplies – one for the red LED and one for the blue and green LEDs with ground as a common reference. One supply is dedicated to the red LED and the other supply powers both the blue LED and the green LED. The improved common-cathode LED display uses one supply connected to a common anode for all three LEDs and a second supply that generates a bias voltage for the red LED. The key challenge is to generate the 1-V bias supply for the red LED.

For a video or image display application, red LEDs can typically occupy between 40% and 50% of the driver current. With the common-cathode LED driving method, the LED display surface temperature can be significantly reduced by more than ten degrees. This method enables color uniformity and improved LED life. In addition, power consumption can be reduced between 30% and 75%.

1.2 Power Supply Solutions for Common-Cathode LED Display

Because of their modularized design, LED displays scale easily.

Each LED module consists of one power module board, an LED controller board and one or more LED panels. For more information, see LED signage. For common-cathode LED driving displays that use dual power supplies, the common approach is dual outputs flyback or LLC. Figure 1-4 and Figure 1-5 show power solutions corresponding to Figure 1-2 and Figure 1-3.

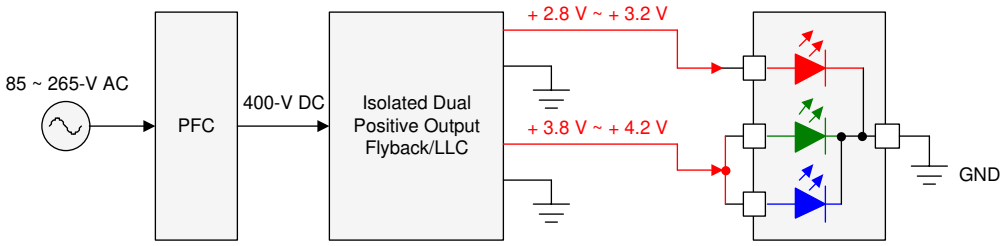

Figure 1-4. Power System to Drive Common-Cathode LEDs

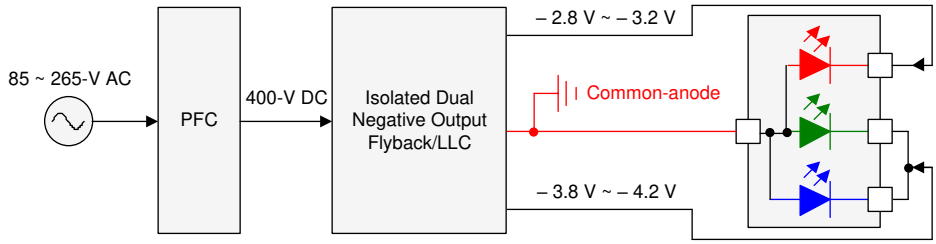

Figure 1-5. Power System to Drive Common-Anode LEDs

Both methods described in in Figure 1-4 and Figure 1-5 are widely used for common-cathode LED driving displays. However, both have the disadvantage of high cost and large size as a result of large magnetics requirements (dual outputs transformer). In addition, dual outputs have cross-regulation challenges for wide dynamic load adjustment in LED display. To solve these problems, the new method proposed in Figure 1-6 shows a flyback or LLC and synchronous buck converter structure to drive common-anode LEDs.

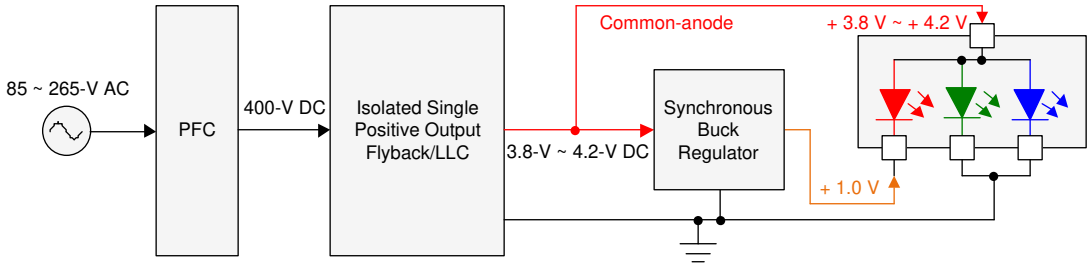

Figure 1-6. Flyback or LLC and Synchronous Buck Converter Solution

In Figure 1-6, the output that comes directly from the flyback or LLC drives the blue and green LEDs. Another output crossing between the flyback or LLC output and the buck output drives the red LED. This approach uses a synchronous buck topology to generate a 1-V floating ground for the red LED. The buck converter operates only to sinki current instead of to source current in steady state. The sinking current converter has been widely used in some applications, such as the TEC driver. Refer to the Low-Power TEC Driver Application Note and the TEC driver reference design for 3.3-V inputs Design Guide.

This application note focuses only on analysis and implementation of the synchronous buck converter topology to design sinking current applications. It discusses some TI devices such as TPS548B22 (synchronous buck converter with integrated switch), TPS548D22 (synchronous buck converter with integrated switch), TPS549D22 (synchronous buck converter with integrated switches and PMBus™), and TPS53819A (synchronous buck controller with external switches and PMBus™) .

Principle of Synchronous Buck with Sinking Current Application analyzes in detail the operations of the synchronous buck topology with sinking current operation. It presents simulations to enable a comparison of the behaviors between sourcing current buck and sinking current buck.

2 Principle of Synchronous Buck with Sinking Current Application

The basic steady state operations of synchronous buck with sourcing current (general use) and sinking current at full load are shown in Figure 2-1 and Figure 2-2. The behaviors of the sinking current case are opposite that of the sourcing current case. The inductor current flows in reverse. The currents of both the high-side and low-side MOSFET flow from source to drain. In addition, the inductor is charged when the low-side MOSFET is ON and the high-side MOSFET is OFF. The inductor is discharged and freewheeling when the low-side MOSFET is OFF and high-side MOSFET is ON.

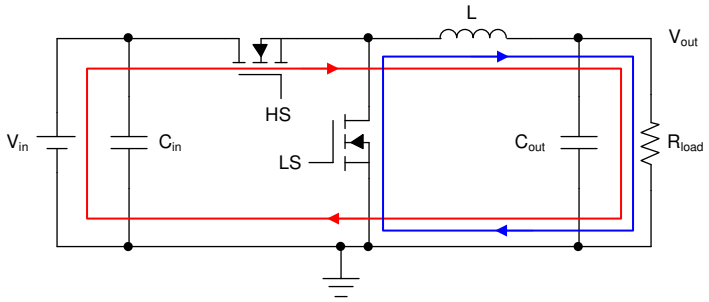

Figure 2-1. Steady State Operation of Sourcing Current

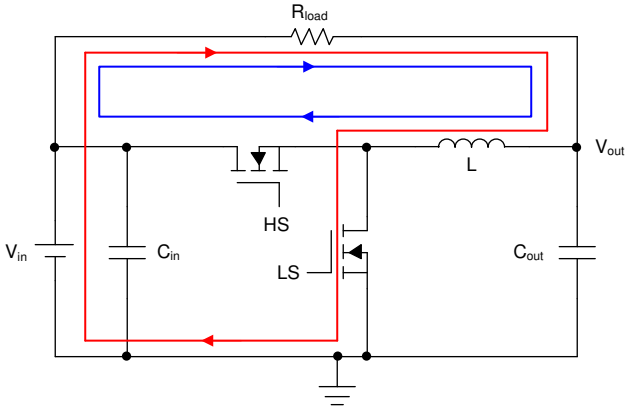

Figure 2-2. Steady State Operation of Sinking Current

Figure 2-3 and Figure 2-4 show simulation circuits of a synchronous buck converter (ideal open-loop) with sourcing current and sinking current. Figure 2-5 and Figure 2-6 show their steady state waveforms. Both converters regulate 12-V input to 5-V 1-A output with the same components value but with a different load so that both load current equals 1 A. The real-time simulation shows both converters have the same duty cycle (for example 41.67%) which conforms to the output-input relation (V_{OUT} = D × V_{IN}) of a buck converter.

It also can be seen from Figure 2-5 and Figure 2-6 that all waveforms, except for the input capacitor waveform, are symmetrical to each other. The differences in input capacitor waveform are due to load difference. The load power in Figure 2-3 is 7 W, which requires a larger input capacitor to supply the higher switching current demanded when the MOSFET turns on than the load power in Figure 2-4 which is 5 W for the same input ripple requirement.

In conclusion, for the same input and output conditions, sourcing current use and sinking current use of synchronous buck converter have the same power stage (except for the input capacitor), as well as the same design methods and formulas.

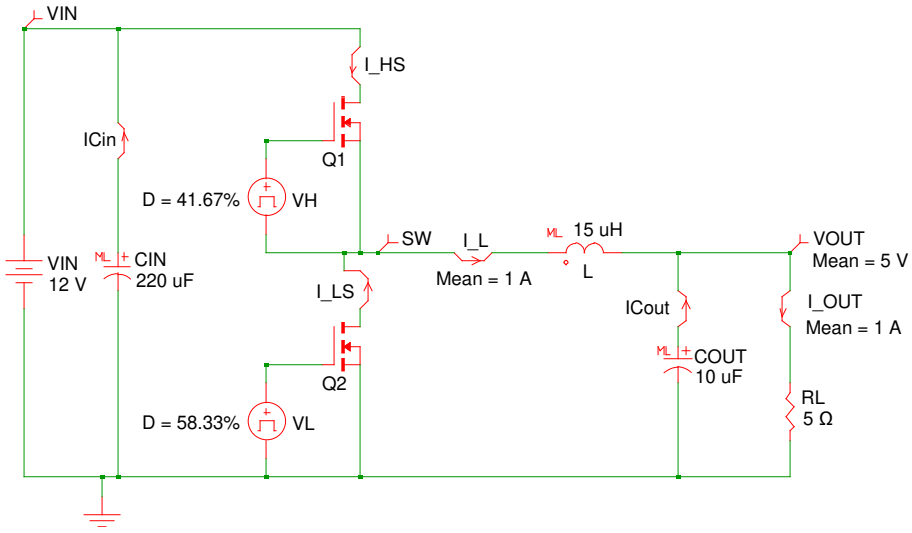

Figure 2-3. Synchronous Buck Sourcing Current Simulation

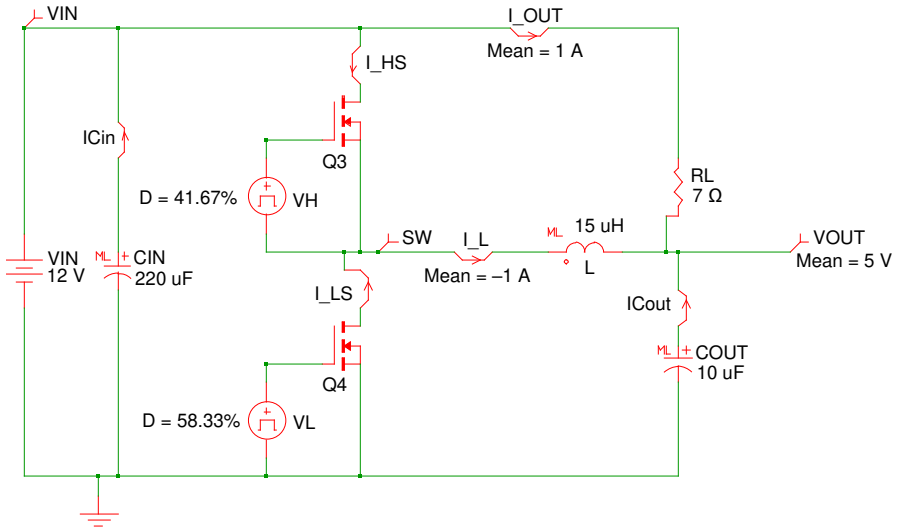

Figure 2-4. Synchronous Buck Sinking Current Simulation

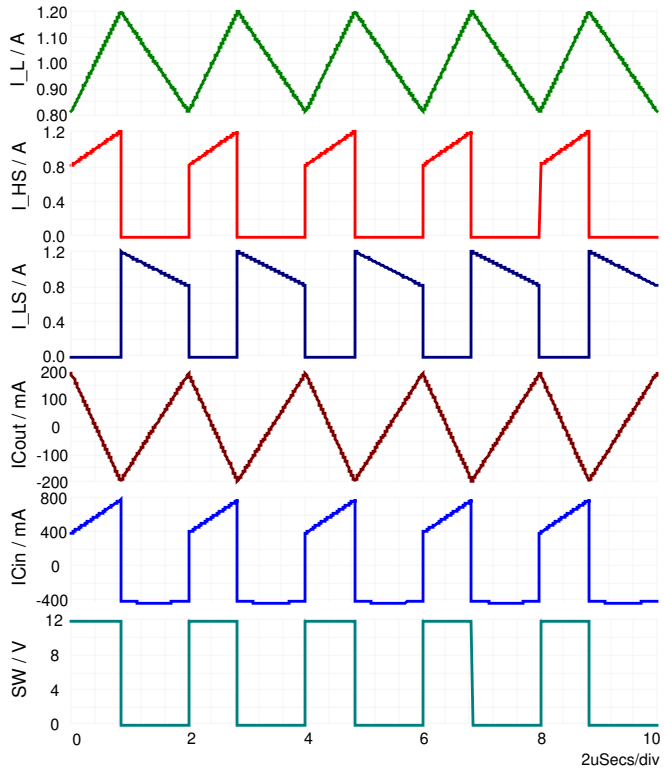

Figure 2-5. Steady State Waveforms Sourcing Current

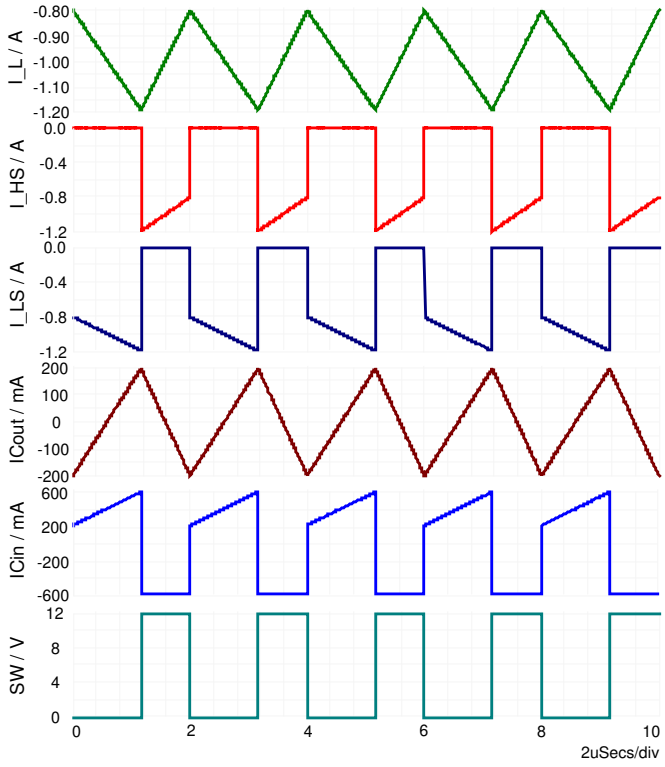

Figure 2-6. Steady State Waveforms Sinking Current

3 Design Considerations and Analysis

The analysis in the previous section is limited to the steady state in open-loop. But other situations, such as start up, close-loop control and transients should also be considered. Converters are generally designed for sourcing current - not sinking current applications. From IC and system perspectives, there are four design challenges:

- Does the controller allow sufficiently large negative current flow?
- Does the controller support negative overcurrent protection (OCP)?
- Does the controller support pre-bias startup?
- Does the system start up normally?

3.1 Choose an IC with Sufficient Current Sinking

Synchronous buck allows for FPWM operation. Normally it is desired to have FPWM only in light load mode - not in full load mode. Hence, most synchronous buck converters have a much smaller negative inductor current limit than a positive inductor current limit. If an IC is chosen without sufficiently large negative inductor current limit for a sinking current application, the output power will be limited by the small negative inductor current limit.

Fortunately, some TI devices such as TPS548B22 and TPS548D22 perform both positive and negative inductor current limits with the same magnitudes, allowing the sinking current application the same large output current as the sourcing current application.

3.2 Choose IC Supporting Negative OCP

Negative OCP functionality allows a circuit to have the ability to react to an OCP event in a sinking current case as a positive OCP in a sourcing current case. Most TI devices based on low-side MOSFET on-resistance ($R_{DS\ (on)}$) sensing have negative OCP levels with the same magnitude as positive OCP. This is realized by OCP comparator and zero crossing detection circuits as discussed in Negative OCP Functionality.

3.3 Choose an IC Supporting Pre-Bias Startup

The pre-bias start-up condition occurs as a result of an external voltage present at the output of the power supply prior to its start up. This could be an issue for a synchronous converter because during start up the output will deliver power into the converter. The pre-bias start-up condition of buck with sinking current is shown in Figure 3-1.

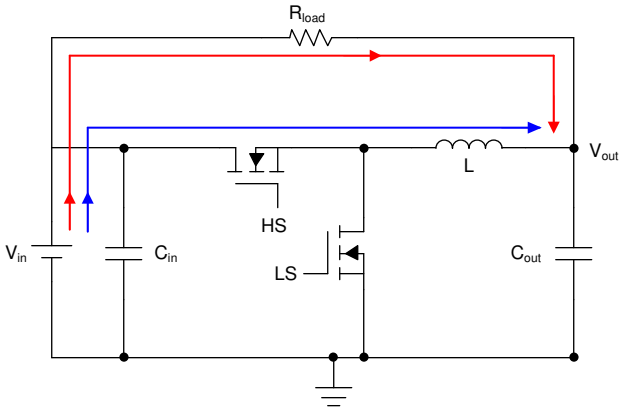

Figure 3-1. Pre-Bias Start-up Condition of Buck with Sinking Current

Due to the fact that the load is connected between the input and output, at the moment of powering on the circuit, the input voltage ramps up first. It presents at the output through the load path (output capacitor is charged through the load, shown in red) before the converter is enabled to switch (output capacitor is charged through the high-side MOSFET, as shown in blue). The output voltage ramps up at the same time as the input voltage until it equals the input voltage (if the converter is not enabled during this period). Suppose that the

converter is enabled and finishes start-up before the output voltage is higher than the OVP threshold. What will happen if the converter does not support pre-bias start up?

Due to the soft-start logic of gradually increasing the duty cycle from zero to that required for regulation, the duty cycle is very small at the early time of soft-start. This means that the low-side MOSFET on time is much larger than the high-side MOSFET on time. When the low-side MOSFET turns on, it could sink large current from the output through the inductor path. This would result in a voltage drop on both the output and the input. If the input cannot provide a large inrush current the converter may go into UVLO and attempt to restart after release from UVLO. Finally, the converter may hiccup and get stuck in the start-up state. In the worst case, the system never starts at all.

Due to the soft-start logic of gradually increasing the reference voltage from zero to the target level, the feedback voltage at the inverting error amp input is much higher than the slow start reference voltage at the non-inverting input. This is because there already exists a voltage at the output. Hence, the control logic will try to decrease the duty cycle to discharge the pre-bias voltage at the output. This causes the low-side MOSFET to constantly turn on and the inductor current to negatively ramp up to a very large value. The constant large current may destroy the low-side MOSFET. Even with negative OCP, an OCP event could bring the converter into hiccup mode or latch-off mode. This means the converter still cannot escape from the start-up dilemma. Again, in the worst case, the system never starts at all.

To ensure the converter can start up normally, select devices such as TPS548B22 and TPS548D22 that support pre-bias start up. The principle behind pre-bias start up is that the device inhibits both high-side and low-side MOSFETs switching until the soft-start reference voltage ramps up and exceeds the feedback voltage. Inhibiting switching during the pre-bias start up condition gives no path for the output to discharge and conduct excessive large current. When the soft-start reference voltage exceeds the feedback voltage, the device begins to switch and start up from the pre-bias level.

3.4 Analysis of System Startup

This section discusses the pre-bias start up with a presupposed condition that OVP is not triggered during start up. This could occur if the output voltage ramps up slowly, such as when the output capacitor is charged through the load path. This could also happen if the target output voltage is higher than the minimum required input voltage and the converter finishes start up before the OVP is triggered.

However, if the load resistance is very small, the output voltage ramps up very fast as the input voltage ramps up and finally equals to the input voltage before the converter is enabled. This results in an OVP event once the converter is enabled. Then, the converter will discharge the output voltage and restart again. Next, the output capacitor is charged through the load path and OVP will be triggered again. In the worst case, OVP events repeatedly appear. This causes the converter to hiccup and get stuck in the start-up state.

The following sections will analyze the behaviors of the TPS548D22 during start up based on bench test waveforms. Also, a solution to solve start up stuck issue will be also discussed.

4 TI Devices and Functionalities

The power level of an LED display module varies from 100 W to 300 W by different pixel pitches. The common power levels for small pixel pitch LED signage in the market are 110 W, 150 W and 220 W. Design parameters and recommended devices are listed in Table 4-1 based on different power levels.

TPS548B22 and TPS548D22 are pin-to-pin, 25 A and 40 A, synchronous buck converter devices. TPS549B22 and TPS549D22 are the same series devices with an additional PMBus™ function for programming. For powering an LED display, the output voltage can be set or dynamically adjusted through PMBus™ to further optimize the design by adjusting the cathode voltage to more precisely match the red LED forward voltage. Since a voltage drop on the path varies in current (as determined by brightness), the red LED forward voltage may drop or increase if a fixed output voltage is applied.

Table 4-1. Design Parameters and Recommended Devices

Design Parameters	Specifications		
	110 W	150 W	220 W
Input Voltage	4.2 V	4.2 V	4.2 V
Output Voltage	1 V	1 V	1 V
Red LED Forward Voltage	3.2 V	3.2 V	3.2 V
Red LED Total Load Current	15 A	20 A	30 A
Blue and Green LED Forward Voltage	4.2 V	4.2 V	4.2 V
Blue and Green Total Load Current	15 A	20 A	30 A
Recommended Device	TPS548B22	TPS548B22	TPS548D22
Recommended Device With PMBus™	TPS549B22	TPS549B22	TPS549D22

This series of devices support soft-start, pre-bias start up, UVLO protection with external adjustment by precise enable hysteresis, and fault protection (OVP, UVP, OCP, OTP). In addition, hiccup mode or latch-off mode can be chosen by external resistor setting. The next sections will discuss some key functionality with TPS548D22. For more details, refer to the TPS548D22 1.5-V to 16-V VIN, 4.5-V to 22-V VDD, 40-A SWIFT™ Synchronous Step-Down Converter with Full Differential Sense Data Sheet.

4.1 Negative OCP Functionality

TPS548D22 has cycle-by-cycle overcurrent limit control. The inductor current is monitored by the voltage across low-side MOSFET $R_{DS\ (on)}$ during the OFF state. The controller maintains the OFF state during the period when the inductor current is larger than the overcurrent trip level. The device uses the GND pin as the positive current sensing node. As the comparison occurs during the OFF state, V_{ILIM} sets the valley level of the inductor current. Also, this device performs both positive and negative OCP with the same magnitudes. Positive current limit is normally used to protect the inductor from saturation which causes damage to MOSFETs. Negative current limit is normally used to protect the low-side MOSFET during OVP discharge. While in a synchronous buck converter with sinking current application, a negative current limit is also used to protect the inductor from saturation, just as the positive current limit does.

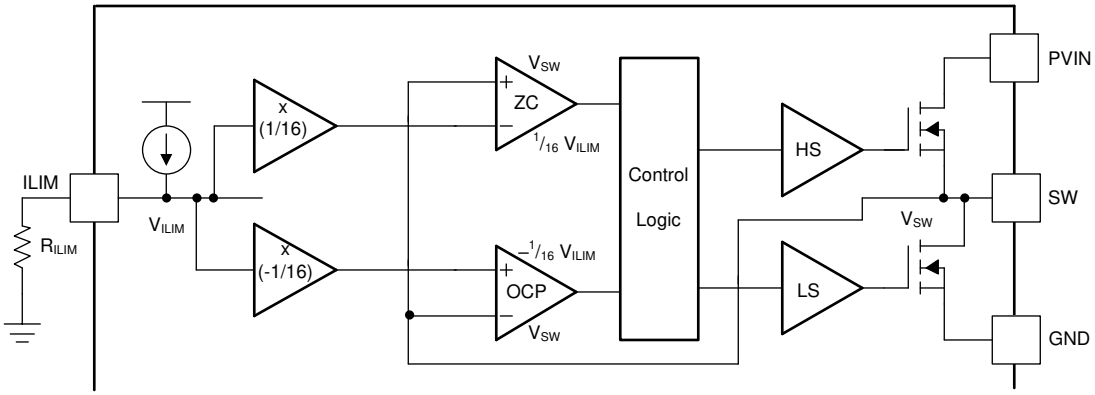

Figure 4-1. OCP Functionality Block Diagram of TPS548D22

Figure 4-1 shows the OCP functionality block diagram of TPS548D22. The resistor R_{ILIM} is connected between ILIM pin and GND to set OCP level. The current coming out from the internal current source flows through R_{ILIM} and determines the voltage V_{ILIM} on the ILIM pin. V_{ILIM} is attenuated to 1/16 of the original value and then connected to the inverting input of the zero-crossing detector. V_{ILIM} is also attenuated to -1/16 of the original value and then connected to the non-inverting input of the OCP detector. The switching node is connected to the non-inverting input of zero-crossing detector and the inverting input of OCP detector.

For positive OCP, once the magnitude of sensing voltage V_{SW} (V_{SW} is negative, since current follows from source to drain) exceeds -1/16 V_{ILIM}, the OCP comparator outputs high and a positive OCP event is recorded. For negative OCP, the detect threshold is set at the same absolute value as positive OCP but with negative polarity. Once the magnitude of sensing voltage V_{SW} (V_{SW} is positive, since current follows from drain to source) exceeds 1/16 V_{ILIM}, the ZC comparator outputs high and a negative OCP event is recorded.Note that the negative OCP threshold still represents the valley value of the inductor current.

4.2 Hiccup Mode and Latch-off Mode

TPS548D22 supports latch-off mode or hiccup mode when an OVP or UVP event are triggered. Normally when an OVP event occurs, the output discharge could lead to an undervoltage condition and trigger an UVP event. Then the OVP event will be reset by the UVP event. When an OCP event occurs, it results in the output voltage falling which causes the UVP event.

For latch-off mode, the device will shut down if an OVP or UVP event occurs. It will restart again only if the EN pin is toggled or the VDD pin is power cycled. For hiccup mode, the device will restart after a hiccup delay when OVP or UVP are triggered. The hiccup blanking time depends on the soft-start ramp time setting. For a typical 1-ms soft-start, the hiccup blanking time is 16 ms. During the hiccup blanking time, the soft-start logic takes 1 ms to gradually increase the reference voltage from zero to the target level.

4.3 UVP and OVP Functionality

TPS548D22 monitors the feedback voltage to detect overvoltage and undervoltage conditions. When the feedback voltage becomes lower than 68% of the target voltage, the UVP comparator output goes high and an internal UVP delay time counter begins counting. After 1 ms, the device turns OFF both high-side and low-side MOSFETs drivers. If the hiccup mode is selected, then the device restarts after a hiccup delay time. UVP function is only enabled after the soft-start operation is completed.

When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the device latches OFF the high-side MOSFET driver and latches ON the low-side MOSFET driver until reaching the negative current limit to discharge the output. If the sensed inductor current reaches the negative current limit (negative OCP), the low-side MOSFET driver is turned OFF and the high-side MOSFET driver is turned ON for a minimum on-time to limit the inductor current exceed the negative limit to protect the low-side MOSFET during OVP discharge. With high-side MOSFET turning on for a minimum on-time, the inductor current is flowing in the positive direction but still in the negative region. After the minimum on-time, the low-side MOSFET turns on and the high-side MOSFET turns off. The inductor current continues following in the negative

direction and reaches the negative current limit again. This cycle will continue until the negative OCP is not triggered anymore. At that time, the output voltage is close to being completely discharged. The high-side MOSFET stays turned off and the low-side MOSFET stays turned on until 1 ms UVP delay is completed. After the 1 ms UVP delay is completed, the device turns OFF both high-side and low-side MOSFETs drivers. If the hiccup mode is selected, then the device restarts after a hiccup delay time.

5 TI Solution

Taking 220 W power supply with hiccup mode as an example, the buck converter is designed for 1-V 30-A output at 4.2-V input. For the component parameters design, it was shown in Principle of Synchronous Buck with Sinking Current Application that sourcing current and sinking current use of a synchronous buck converter have the same power stage (except for the input capacitor), as well as design methods and formulas. Fortunately, TPS548D22EVM-784 provides a fixed 1-V output at up to 40 A from a 12-V input bus. It is possible to use it to verify this common-anode power solution with just some minor changes as shown in Figure 5-1.

The first change is the VDD supply voltage. Note that the VDD UVLO rising threshold of TPS548D22 is typically 4.25 V. With 4.2-V input connecting to VDD, the device will be in UVLO state and cannot start. A boost circuit or an external power supply of 12 V should be used to make sure the device is properly powered and enabled. The second change is the resistor divider network of reference voltage. The EVM is set in latch-off mode. So, R_{sel} (R23 in EVM) should be changed to 33.2 kΩ for hiccup mode. The hiccup time is 16 ms (with 1 ms soft-start option).

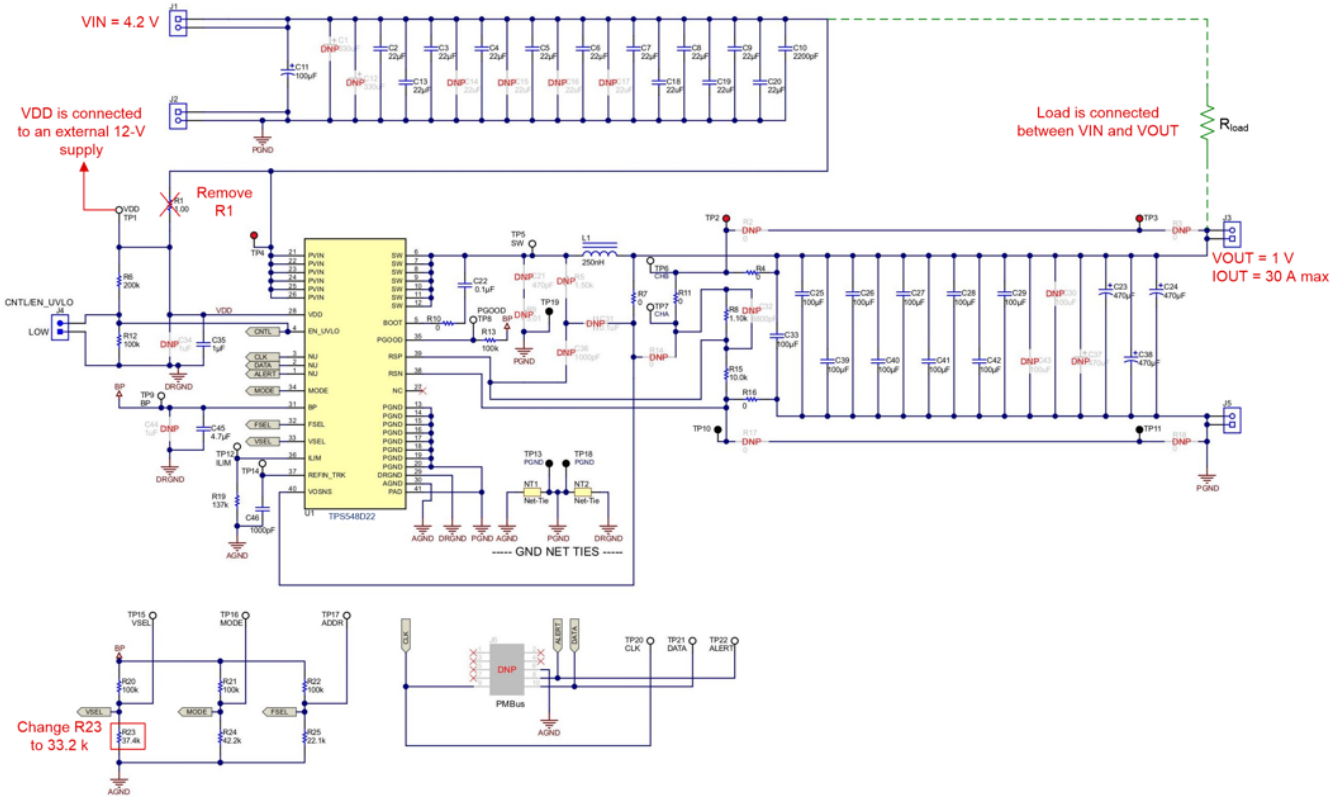

Figure 5-1. Schematic of TPS548D22 with Sinking Current Application

A question is left in Analysis of System Start Up - how does one ensure that the converter does not get stuck during the start-up state? Since a small load resistance will charge the output capacitor quickly, causing an OVP to occur, one approach is to start up with a light load that slows down the charging speed of the output capacitor. Then the OVP may not be triggered after the device is enabled and the device could start up from a pre-bias condition. Or a simpler approach is to start up with no load. With no load condition, the path charging the output capacitor through the load resistor does not exist anymore. Then the device can start up normally and an OVP event will not occur. Once the start-up is finished, the PGOOD signal could be used as an enable signal to add the load. Finally, the synchronous buck converter with sinking current can work fine in steady state, as well as in transient conditions.

Bench Test and Result analyzes start-up behaviors of this synchronous buck converter with sinking current application based on bench test waveforms. Also, a lazy loading solution, which means to start up with no load and then add the load after start up is complete, will be analyzed.

6 Bench Test and Result

This section analyzes the startup behaviors and waveforms of the synchronous buck converter with sinking current application. The lazy loading solution is also covered.

6.1 Bench Test Configuration

Figure 6-1 shows the bench test configuration of TPS548D22 with sinking current application. The power supply used in this configuration was limited to 8-A current. Therefore this test is not able to validate the 30 A full load (R_{load} = 3.2 V/30 A = 0.107 ohm) condition. However, an approximate 9.3-A load (R_{load} = 3.2 V/0.34 ohm = 9.3 A) is sufficient to verify the feasibility of TPS548D22 with a current sink application. Note that the output voltage of the DC power supply is set at 4.7 V. This is higher than the 4.2-V input voltage due to resistive loss in the cabling.

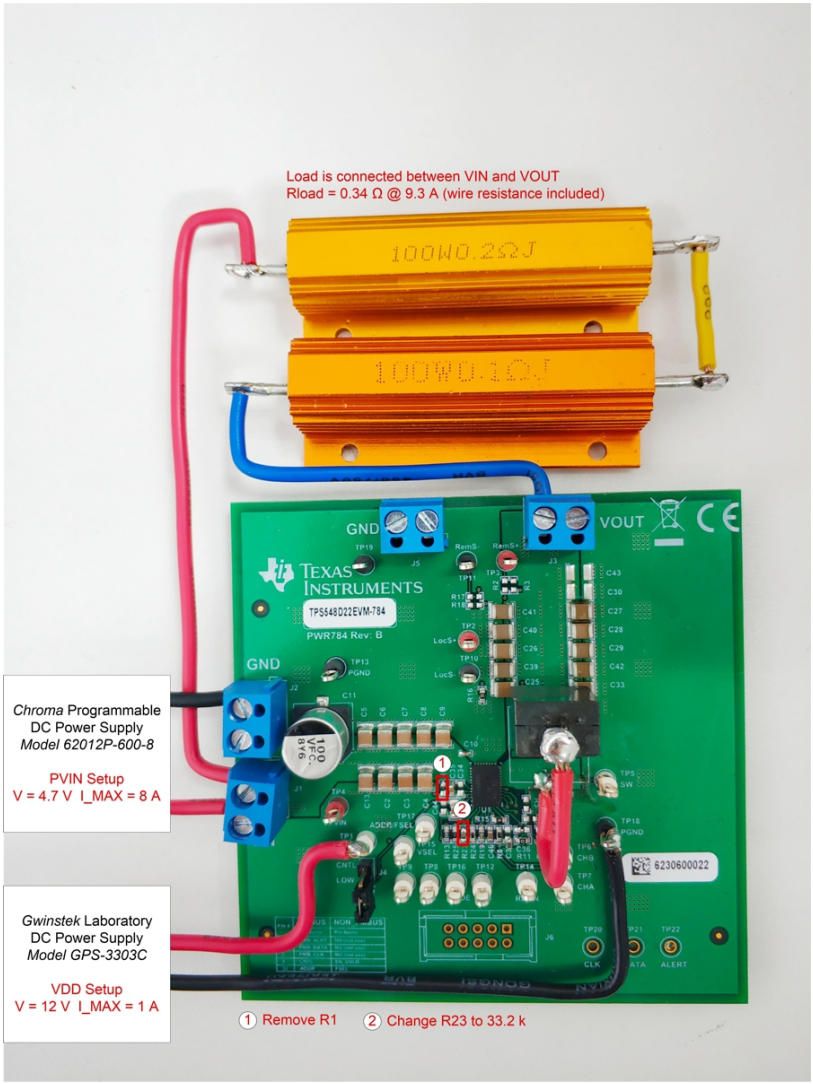

Figure 6-1. Bench Test Configuration of TPS548D22 with Sinking Current Application

6.2 Startup Waveforms and Behaviors Analysis Overview

Figure 6-2 shows the start-up waveforms of TPS548D22 with 9.3-A load added before power up.

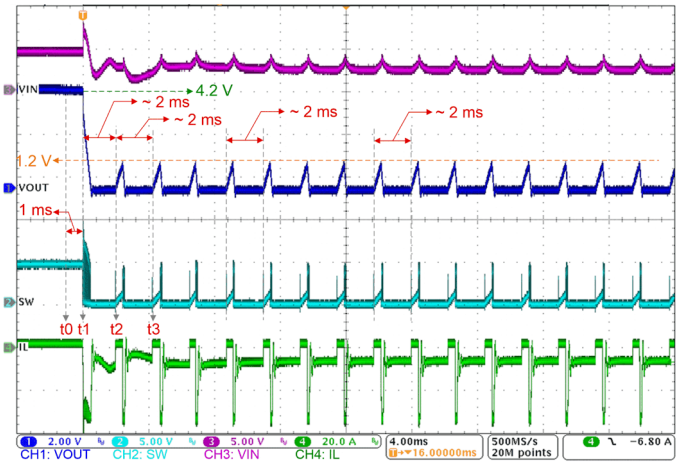

Figure 6-2. Start-up Waveforms with 9.3-A Load

At some moment before t0, PVIN power and VDD power are turned on but the device is not enabled. It can be seen that the output voltage equals the input voltage of 4.2 V. This means the output capacitor is fully charged to the input voltage through the load path. The output voltage is 4.2 V higher than the OVP trip level 1.2 V (120% threshold) but OVP is not triggered before t0 because the device is not enabled.

At t0, the device is enabled. t1 occurs after about 1 ms of the Power-on delay time, t_{PODLY}. At t1, the device's function modules, such as soft-start and protection functionality, start working. The soft-start begins from t1 for 1 ms with reference voltage ramping up from 0 V to the final defined level. The device does not start up because an OVP event also occurs at t1 and the output begins discharging to 0 V.

At t2, around 2 ms after t1, the output voltage begins ramping up to the OVP trip level of 1.2 V and then discharges to 0 V. At t3, the output voltage begins ramping up to the OVP level and discharges again, similar to at t2. The OVP event is periodically triggered every 2 ms. Hence, the device hiccups every 2 ms and gets stuck during the start-up state.

This may result in a number of questions. Why is the duration between t1 and t2 around 2 ms? Why does the device *hiccup* every 2 ms after t2? It is known that the hiccup time should be 16 ms for 1 ms soft-start. Here, a 2 ms hiccup time looks quite different. What about the behaviors of waveforms? How does the output ramp up and decay? Why does the software voltage ramp up following output and also have some pulses?

It can be seen from the inductor current and input voltage waveforms that when large inductor current transients occur, the input voltage changes sharply. This is not good for the input stage and should be avoided in the power supply design.

To address the questions listed above, the internal soft-start operation should be taken into account. Note that it is mentioned in Hiccup Mode and Latch-off Mode that when an OVP event occurs, the discharge of output could lead to an undervoltage condition and trigger the UVP. Then the OVP event will be reset by the UVP event. In addition, it is specified in UVP and OVP Functionality that UVP function is only enabled after the soft-start operation is completed.

To better understand the relations between output behavior and internal soft-start operation. Figure 6-3 shows output voltage and critical time nodes in detail.

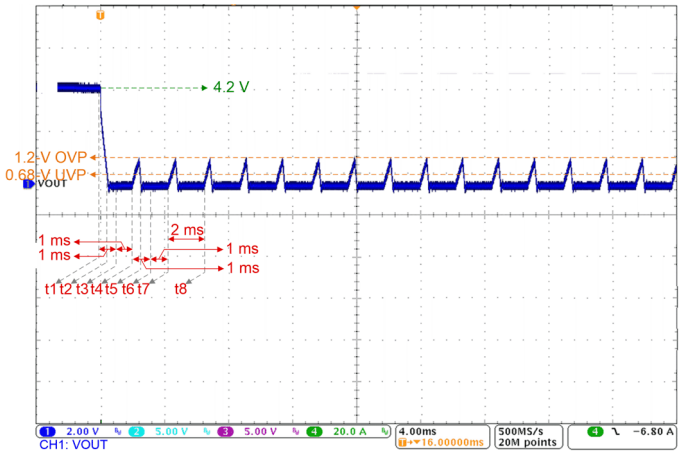

Figure 6-3. Start-up Output Waveforms with 9.3-A Load

At t1, OVP is triggered and the output begins discharging. At t2, the feedback voltage (the same as output voltage) becomes lower than 68% (0.68 V) of the target voltage. The UVP comparator output goes high but the internal UVP delay time counter won't begin counting since the soft-start operation is not completed. The output continues discharging from t2 to t3. At t3 when the soft-start operation is completed, the internal UVP delay time counter begins counting for 1 ms from t3 to t4. At t4, the device turns OFF both high-side and low-side MOSFETs drivers. Then the device enters hiccup mode with 16 ms delay due to UVP (the OVP at t1 is reset by the UVP). After 1 ms UVP delay at t4, there is an internal 1 ms soft-start timer that begins counting from t4 to t6 (1 ms, 16 times). At t4, the output ramps up resulting in OVP being triggered. Further details on why the output ramps up at t4 to the 1.2-V OVP level will be provided in Start-up Waveforms and Behaviors Analysis after the First OVP. At t5, the output decays to the UVP trip level. But the 1 ms UVP delay counter doesn't count until t6 when the soft-start operation is completed, similar to what happens from t2 to t3. After 1 ms UVP delay at t7 (repeat as t4) , the internal 1 ms soft-start timer begins counting, similar to what happens at t4.

The OVP and UVP event occur cyclically. This results in a 2 ms hiccup time, consisting of 1 ms UVP delay and 1 ms soft-start time. If the circuit is configured with 2 ms soft-start time (by changing R24 to 47.5 kΩ), then the cycle is 3 ms hiccup time, consisting of 1 ms UVP delay and 2 ms soft-start time.

6.3 Startup Waveforms and Behaviors Analysis at the First OVP

Figure 6-4 and Figure 6-5 show waveforms at the first OVP with details.

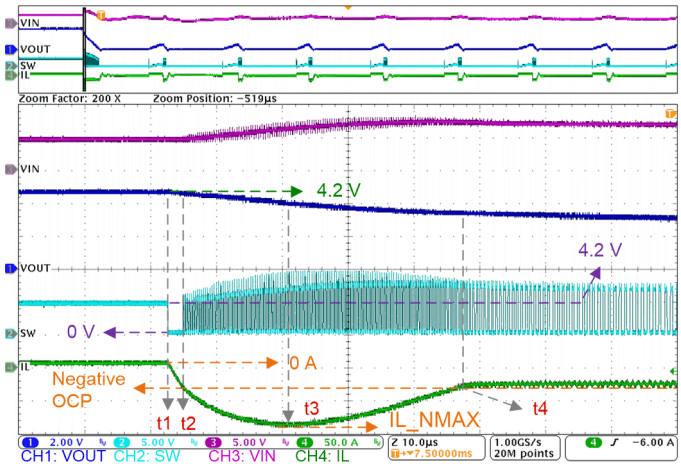

Figure 6-4. Start-up Waveforms at the First OVP with Details: 1

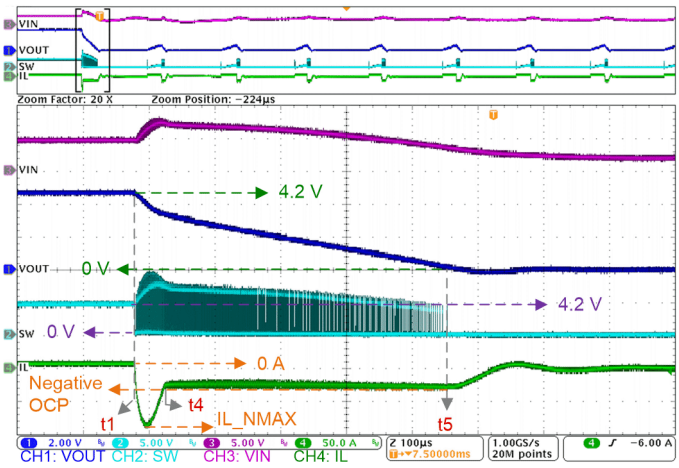

Figure 6-5. Start-up Waveforms at the First OVP with Details: 2

At t1 , when OVP occurs, the high-side MOSFET keeps turning OFF and the low-side MOSFET keeps turning ON to discharge the output until t2, at which time negative OCP is reached. Correspondingly, the output voltage drops, the SW voltage stays at 0 V and the inductor current increases in the negative direction during t1 to t2.

At t2, normally, the device is supposed to turn on the high-side MOSFET for a minimum on-time to limit the inductor current exceeding the negative OCP level to protect the low-side MOSFET during OVP discharge. But from t2 to t3, it looks like that inductor current exceeds the negative OCP level and increases in the negative direction. In the negative direction, the rising speed of the inductor current is faster than the falling speed. The difference gradually becomes smaller and smaller with output discharging. During the minimum on-time of the high-side MOSFET, inductor current falls in the negative direction. During the on-time of the low-side MOSFET, inductor current increases for at least a minimum on-time in the negative direction. As a result, the increment is larger than the decrement and the inductor current increases in the negative direction. The large inductor current could exceed the inductor saturation current and damage the MOSFETs.

At t3, in the negative direction, the rising speed of inductor current becomes equal to the falling speed. From t3 to t4, the rising speed of inductor current is slower than the falling speed and the difference gradually increases with the output continuously discharging. Inductor current decreases in the negative direction and finally goes back to the negative OCP level at t4.

From t4 to t5, the high-side MOSFET continuously turns on for a minimum on-time until the output voltage is close to being completely discharged at t5. In this period, negative OCP is cyclically triggered. More details about OCP behaviors are in the next section.

6.4 Startup Waveforms and Behaviors Analysis after the First OVP

Figure 6-6, Figure 6-7, Figure 6-8 and Figure 6-9 show waveforms after the first OVP with details.

The corresponding circuit behaviors of each stage are shown in Figure 6-10, Figure 6-11, Figure 6-12, Figure 6-13, Figure 6-14, and Figure 6-15.

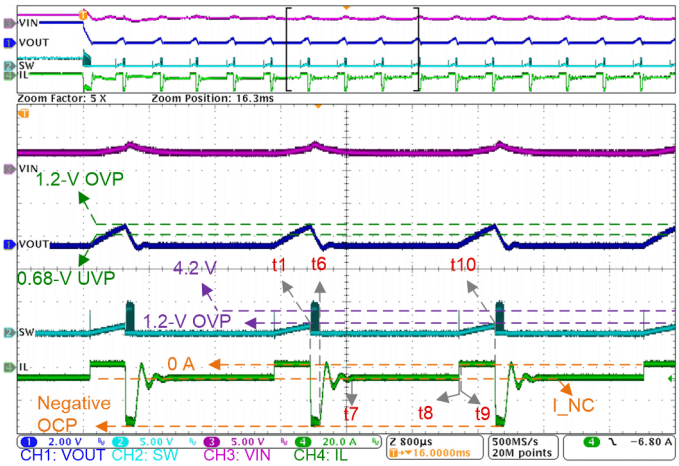

Figure 6-6. Start-up Waveforms after the First OVP with Details: 1

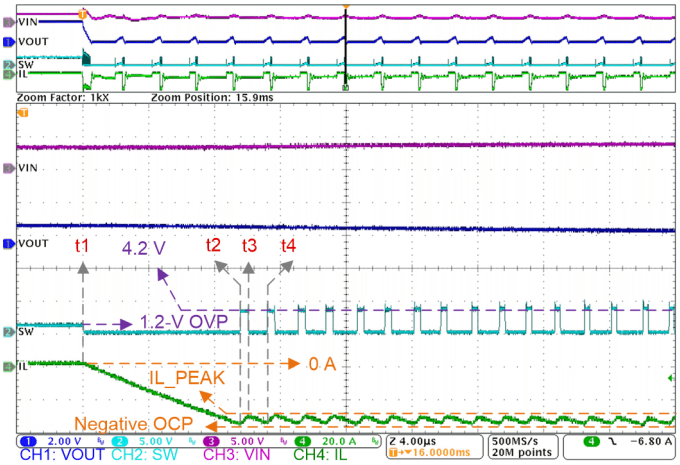

Figure 6-7. Start-up Waveforms after the First OVP with Details: 2

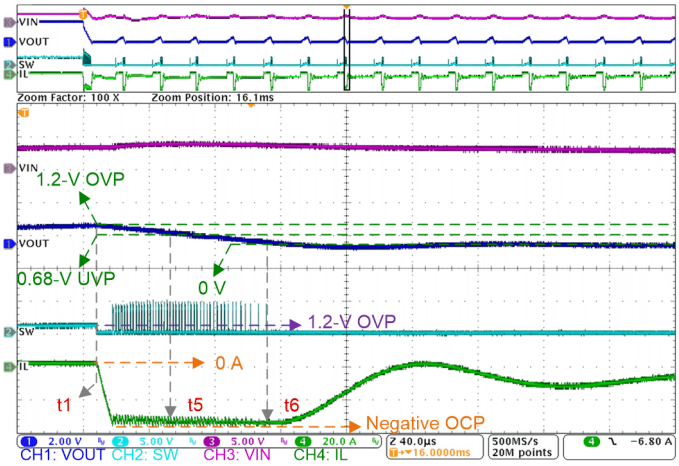

Figure 6-8. Start-up Waveforms after the First OVP with Details: 3

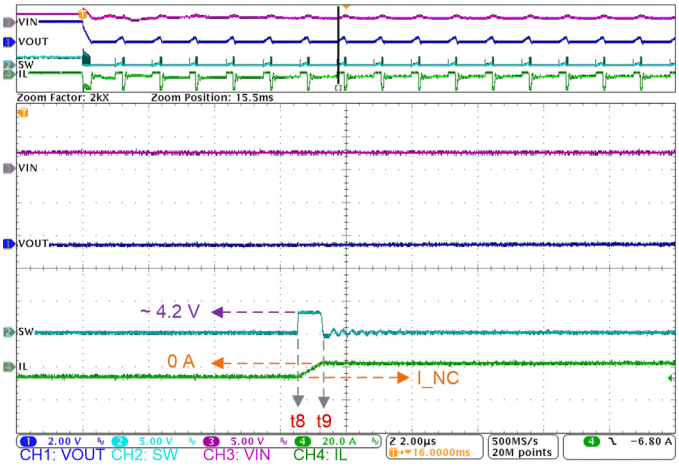

Figure 6-9. Start-up Waveforms after the First OVP with Details: 4

From t1 to t2, OVP is triggered at t1. The high-side MOSFET keeps turning OFF and the low-side MOSFET keeps turning on to discharge the output until t2, at which time the negative current limit (negative OCP) is reached. Correspondingly, the output voltage drops, the SW voltage stays at 0 V and the inductor current increases in the negative direction during t1 to t2.

From t2 to t6, negative OCP is first reached at t2. Then the low-side MOSFET driver is turned off, and the high-side MOSFET driver is turned on for a minimum on-time to limit the inductor current so that it does not exceed the negative limit level. With the high-side MOSFET turning on for a minimum on-time (t2 to t3), the inductor current flows in the positive direction but still in the negative region. After the minimum on-time, the low-side MOSFET turns on and the high-side MOSFET turns off. The inductor current continues flowing in the negative direction (t3 to t4) and reaches the negative current limit again (negative OCP is triggered again) at t4. This cycle will continue until negative OCP is not triggered anymore at t6. At this time, the output voltage is close to being completely discharged. The high-side MOSFET stays turned off and the low-side MOSFET stays turned on until the 1 ms UVP delay is completed. Note that at t5, UVP is reached, but the internal 1 ms UVP delay time counter does not begin counting since the soft-start operation is not completed. This is discussed in Start-up Waveforms and Behaviors Analysis Overview.

From t6 to t7, the output capacitor is completely discharged and voltage across the inductor is zero at t6. As there is no voltage across the inductor to maintain the current, it starts to fall but still keep flowing in the original direction to charge the output capacitor with the opposite polarity. Then, the capacitor starts to discharge again back through the coil and the whole process is repeated. The polarity of the voltage changes as the energy is passed back and forth between the capacitor and inductor producing a LC oscillator and finally decays the oscillations to zero at t7 due to some energy losses.

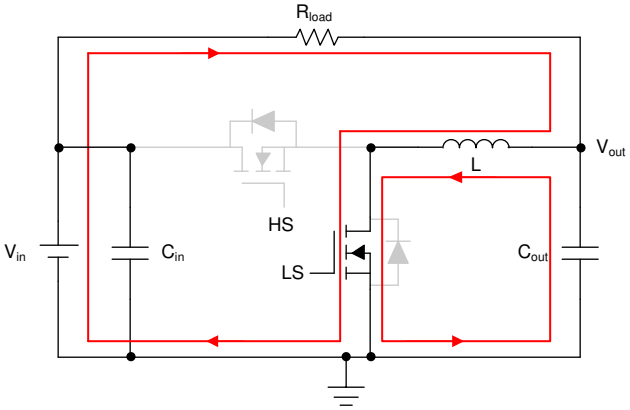

Figure 6-10. t1~t2: OVP triggers, output discharge until reaching negative OCP

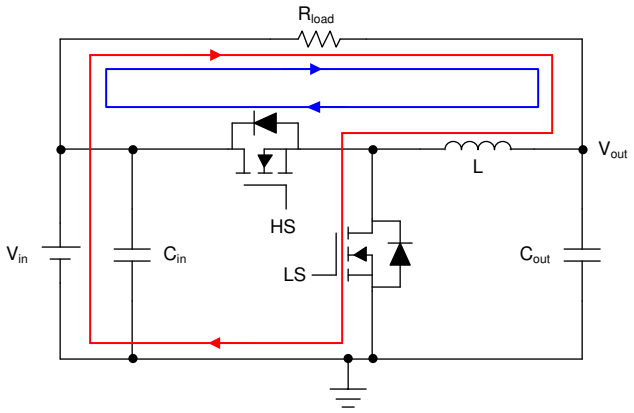

Figure 6-11. t2~t6: High-side MOSFET turns on for a minimum on-time

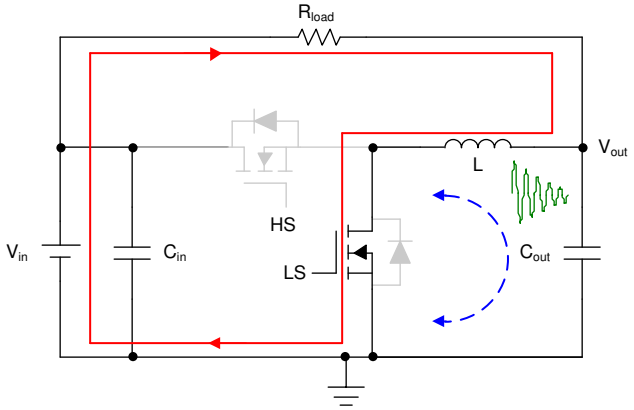

Figure 6-12. t6~t7: LC resonating, output voltage follows resonating

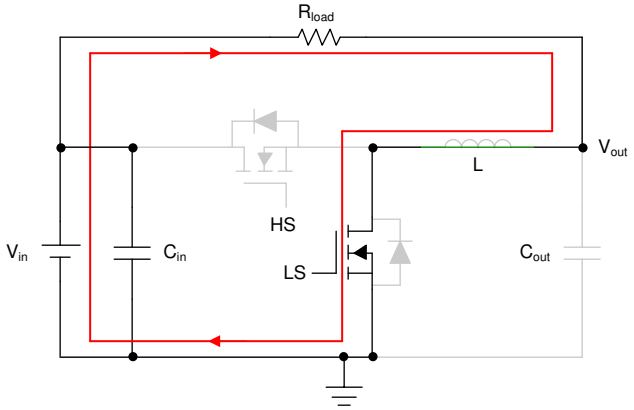

Figure 6-13. t7~t8: Output voltage is 0V, inductor behaves as a pure wire

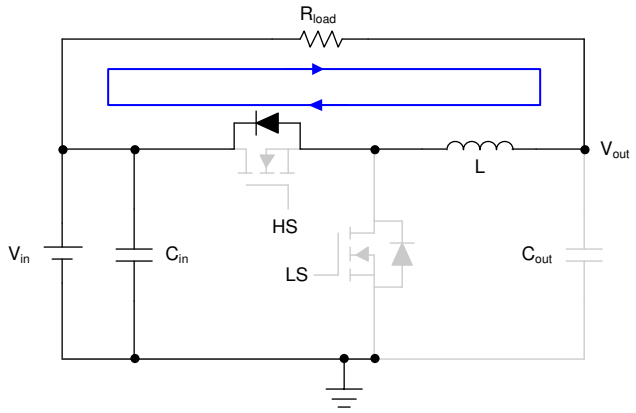

Figure 6-14. t8~t9: Inductor current is freewheeling through high-side body diode

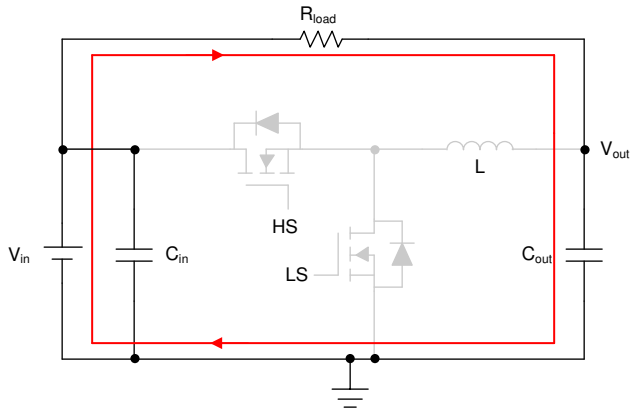

Figure 6-15. t9~t10: Output capacitor charging and OVP is triggered again

From t7 to t8, energy stored in the LC oscillator is fully discharged at t7. The inductor is equivalent to a short circuit. The whole circuit is a pure resistance circuit with a constant negative current with V_{out}/R_{load} through the inductor.

From t8 to t9, the 1 ms UVP delay is completed at t8, the device turns OFF both high-side and low-side MOSFETs drivers. However, there still is current left in the inductor and the current cannot suddenly change. The freewheeling current of the inductor continues to flows through the body diode of the high-side MOSFET and decays to zero. The corresponding SW node voltage roughly equals to the input voltage.

From t9 to t10, the output capacitor is charged again only through the load path. This results in the output voltage ramping up and OVP being triggered again at t10 (repeat as t1). A new OVP cycle begins. Also note that the SW voltage exactly follows the output voltage since there has no current flowing in the inductor.

The waveform analysis explains why the OVP event is cyclically triggered and yields a system start-up issue. Apart from that, some other behaviors, such as intense fluctuation of the input voltage, possible inductor saturation and MOSFET damage cannot be accepted for actual power supply application.

6.5 Waveforms and Behaviors Analysis of Startup Solution with Lazy Loading

Figure 6-16, Figure 6-17, and Figure 6-18 show the startup waveforms of the lazy loading solution. The inductor current gradually increases in the negative direction and then goes into steady state. The shape of the inductor waveform looks like the normal startup of buck with sourcing current but is horizontally symmetrical. The output voltage before the startup of buck with sourcing current application is 0 V ground. Similarly, for buck with sinking current application, the output needs to be pre-biased to the target level before startup since the output is regarded as the floating ground for the load.

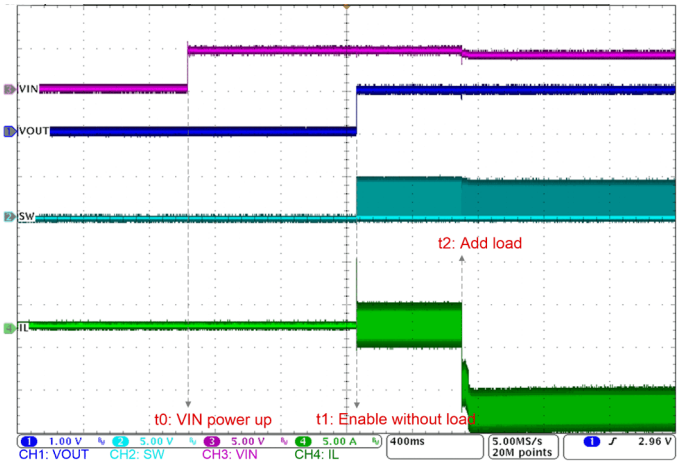

Figure 6-16. Startup Waveforms with Lazy Loading: 1

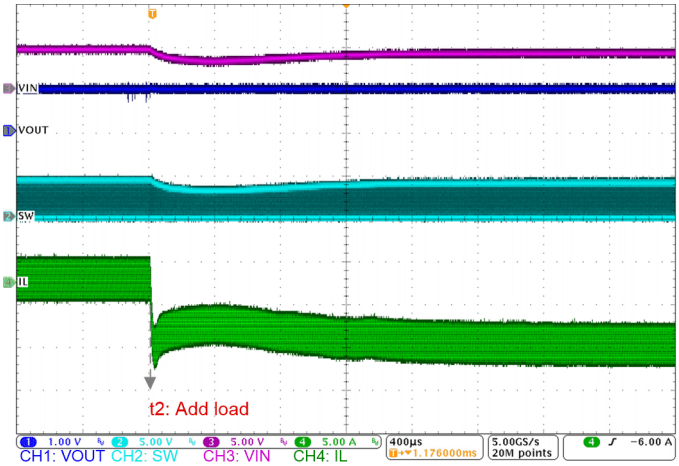

Figure 6-17. Startup Waveforms with Lazy Loading: 2

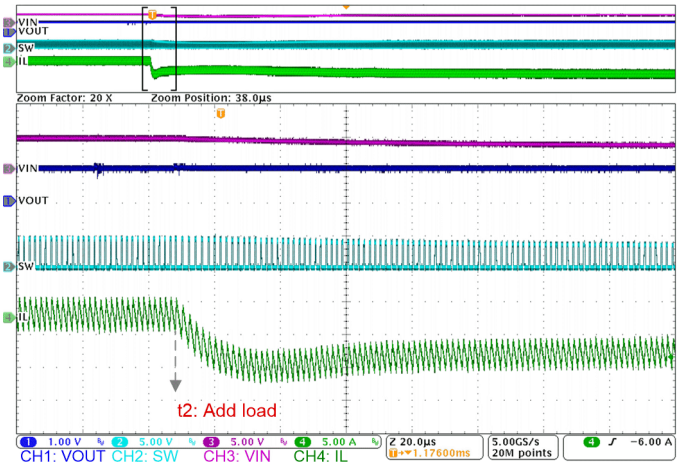

Figure 6-18. Startup Waveforms with Lazy Loading: 3

Figure 6-19, Figure 6-20, Figure 6-21, and Figure 6-22 show steady state, output ripple, transient response, and shutdown waveforms.

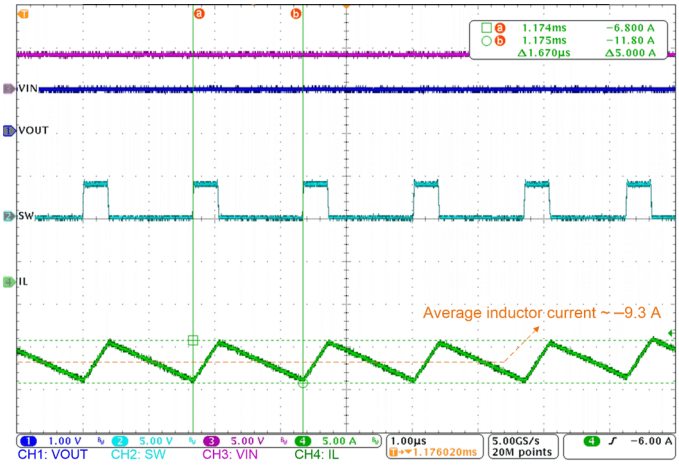

Figure 6-19. Steady State Waveforms of 4.2-V Input, 1-V 9.3-A Output

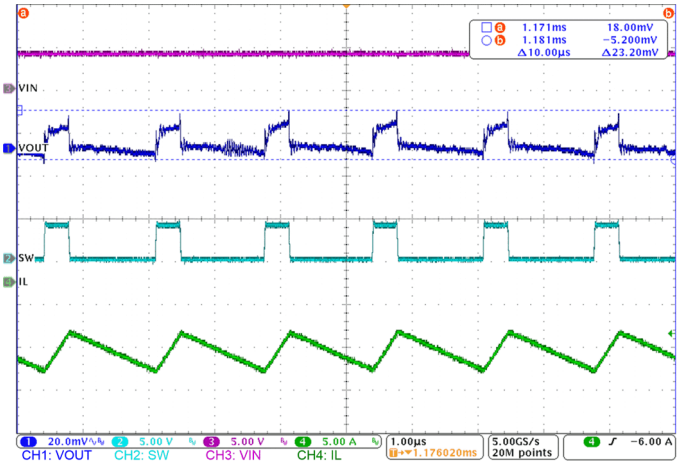

Figure 6-20. Output Ripple Waveforms of 4.2-V Input, 1-V 9.3-A Output

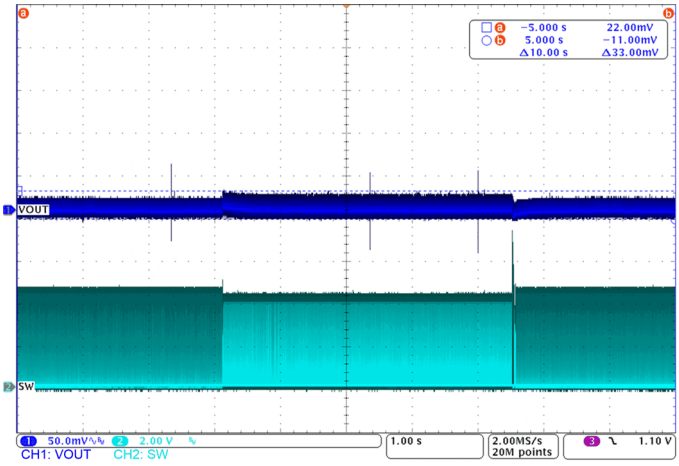

Figure 6-21. Transient Response of 4.2-V Input, 1-V Output, 0 A to 9.3 A, 2.5 A/µs Transient

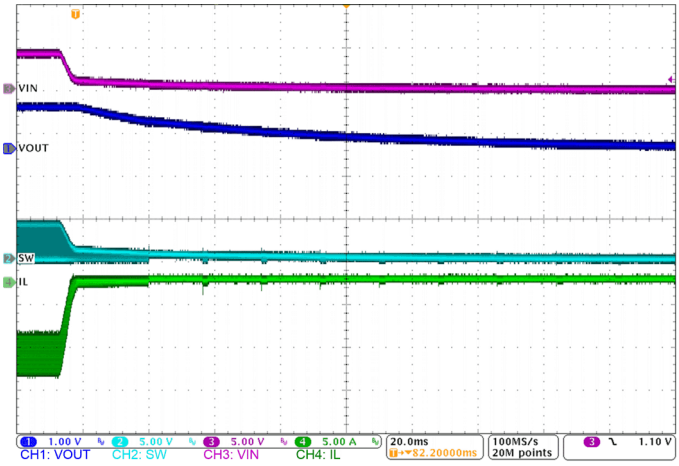

Figure 6-22. Shutdown Waveforms

7 Conclusion

This application report discusses a common-anode power supply circuit implementation of synchronous buck converter with sinking current based on TI device TPS548D22 for common-cathode LED display driving. The principle of the buck topology with sinking current is analyzed and concluded to have the same power stage (except for the input capacitor), design methods and formulas as buck with sourcing current use, for the same input and output conditions. Then, this report presents design considerations and analyses to help select the devices which are most suitable for a sinking current application. In addition it offers a detailed analysis of the startup stuck issue of sinking current circuit. In conclusion, it proposes a solution of lazy loading to solve the startup stuck issue which works well.

8 References

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5. Texas Instruments, TEC driver reference design for 3.3-V inputs Design Guide
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