Application Note

Understanding BQ76905, BQ76907 Voltage Sampling Measurement Loop

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ABSTRACT

BQ76905, BQ76907 is a BMS analog front-end device, supporting 2-7S battery packs. The device has many advantages such as high-sampling accuracy, low-power consumption, rich-protection functions, support for out-of-order power-on, integrated low-side driver, integrated LDO and internal balancing circuit, and is widely used in BMS designs for vacuum cleaners, power tools, drones, and other applications. However, many are often confused about our internal voltage sampling cycle when first using the device. To improve the efficiency of designing designs using this device, this article uses a combination of pictures and text to help understand the voltage sampling logic of BQ76905, BQ76907 more clearly and intuitively.

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Trademarks

1 Introduction

Figure 1-1 shows the functional block diagram of BQ76907. This can be seen from the figure that BQ76907 has a Δ-Σ ADC for each battery cell, TS Pin voltage, internal LDO output voltage and VREF1 voltage, and so on. The sampling accuracy can reach 4mV. Because battery cells share an ADC through MUX, some specific scheduling is necessary to realize voltages sampling.

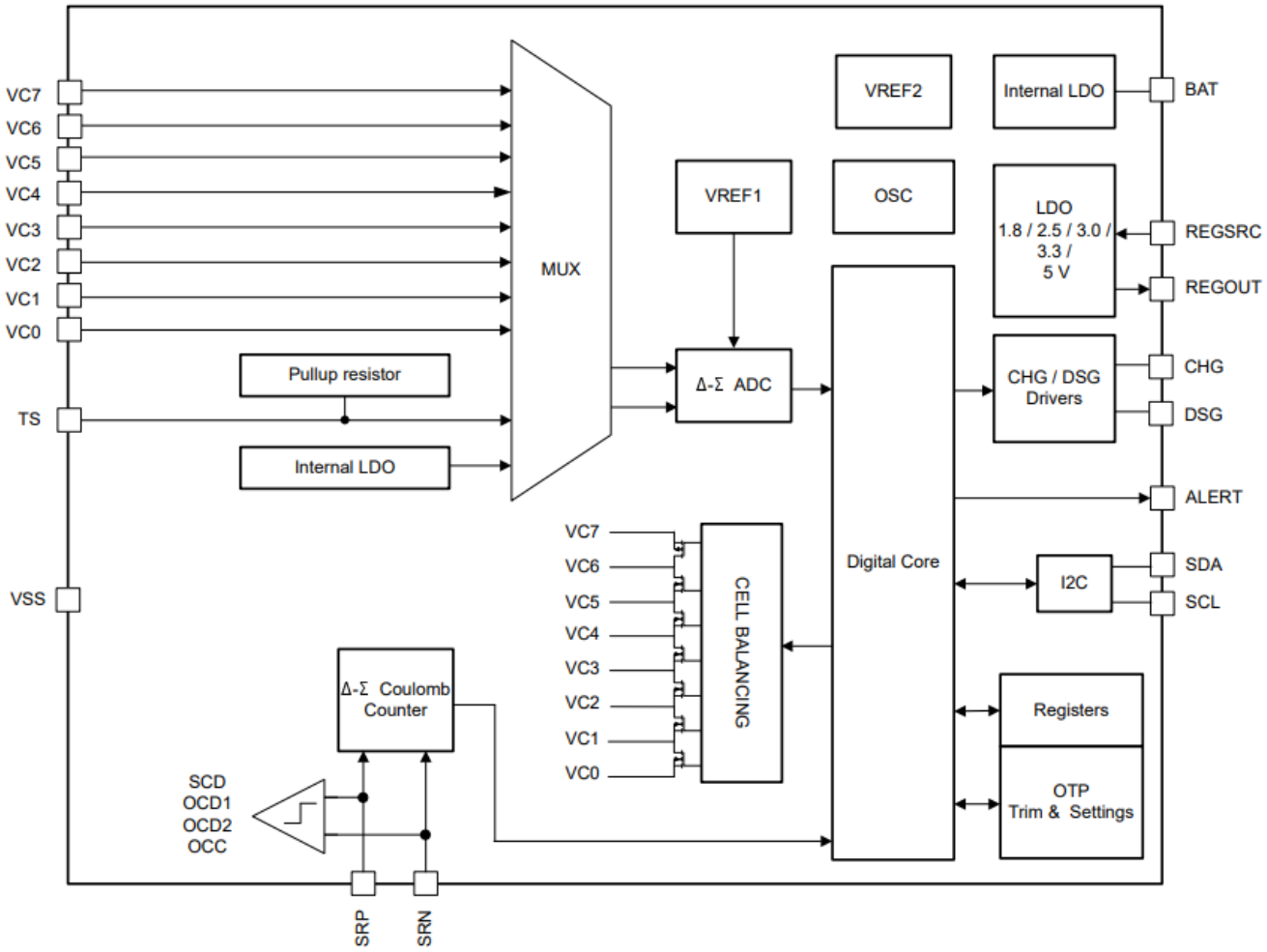

Figure 1-1. BQ76907 Block Diagram

However, considering the different working scenarios, different numbers of battery cells, different requirements for sampling accuracy and speed, and different device power consumption, the implementation methods can be different. The following chapters describe the implementation in detail using BQ76907 as an example.

2 Normal Mode

2.1 For 7 Cell Battery Pack

This section introduces the sampling logic of 7S battery pack and battery pack smaller than 7S in Normal Mode. For the 7S battery pack, as shown in Figure 2-1, the BQ76907 performs voltage sampling as ADSCAN LOOP.

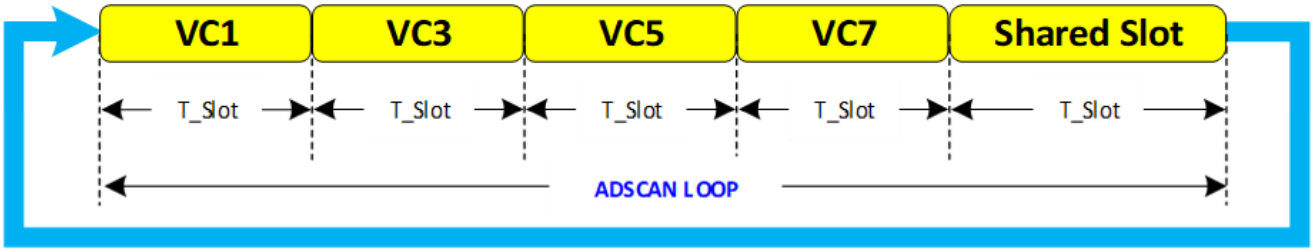

Figure 2-1. ADSCAN LOOP for 7S Pack

Each ADSCAN LOOP contains 8 slots, of which the first 7 slots continuously collect the voltage of 7 cells, and the last slot is a shared slot.

The time T_Slot of each slot can be configured through [CVADCSPEED_1, CVADADCSPEED_0]. As shown in Table 2-1. The smaller the T_Slot, the higher the sampling rate, but the lower the accuracy. On the contrary, the larger the T_Slot, the lower the sampling rate, but the higher the accuracy. Therefore, users need to compromise between the speed and accuracy of BQ76907 sampling when configuring T_Slot.

Table 2-1. T_Slot

CVADCSPEED_1	CVADCSPEED_0	T_Slot
0	0	2.93ms
0	1	1.46ms
1	0	732us
1	1	366us

The Shared Slot is shared by (TS Pin voltage, internal temperature, VC7 Pin voltage, VREF voltage and VSS voltage). Because these voltages do not require a fast sampling rate compared to the cell voltage, each ADSCAN LOOP can only sample one of the voltages. This process takes every 5 ADSCAN LOOPs to complete the sampling of all voltages. Therefore, every 5 ADSCAN LOOPs is called a FULLSCAN LOOP, as shown in Figure 2-2.

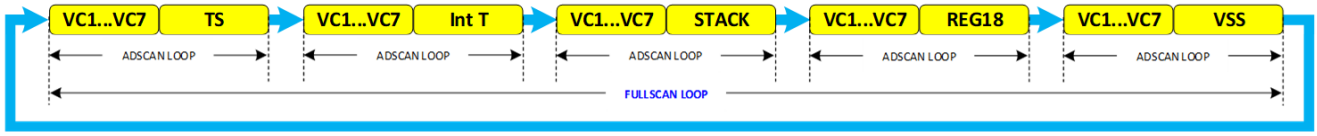

Figure 2-2. FULLSCAN LOOP

In many application scenarios, customers do not have very high requirements for the sampling rate, but have high requirements for power consumption, and hope to maintain a relatively low power consumption level in Normal Mode. For this reason, BQ76907 opens a register: LOOP_SLOW [1, 0]. By configuring this register, users can insert several IDLE Slots after each Active Slot, and use this method to reduce the sampling rate and achieve lower power consumption. As shown in Figure 2-3.

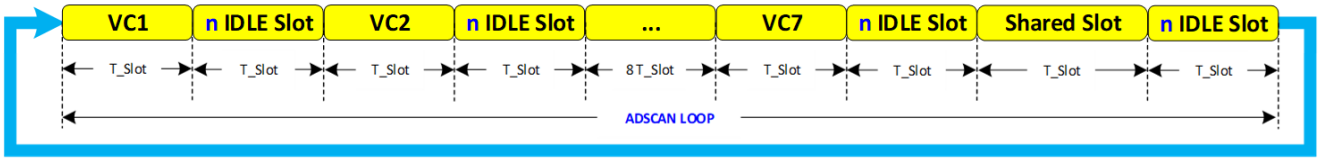

Figure 2-3. ADSCAN LOOP with LOOP_SLOW Speed Control

$$n = 2^{Loop\_SLOW[1:0]} - 1 \quad (1)$$

Where: relationship between n and the number of IDLE slots can also be directly referred to in Table 2-2.

Table 2-2. LOOP_SLOW Speed Control

LOOP_SLOW [1]	LOOP_SLOW [0]	Loop Speed
0	0	Full Speed (0 Idle Slot after 1 Active Slot)
0	1	Half Speed (1 Idle Slot after 1 Active Slot)
1	0	Quarter Speed (3 Idle Slots after 1 Active Slot)
1	1	Eighth Speed (7 Idle Slots after 1 Active Slot)

2.2 Less Than 7 Cell Battery Pack

For battery packs less than 7S, the cells must be connected in accordance with the connection method specified in Table 2-3, and Settings:Configuration:Vcell Mode must also be configured to the actual number of cells.

Table 2-3. Cell Usage and Connection

Number of Cell Used	Connected Cells	Shorted Cells
6	VC7, VC6, VC5, VC3, VC2, VC1	VC4
5	VC7, VC5, VC3, VC2, VC1	VC6, VC4
4	VC7, VC5, VC3, VC1	VC6, VC4, VC2
3	VC7, VC5, VC1	VC6, VC4, VC3, VC2
2	VC7, VC1	VC6, VC5, VC4, VC3, VC2

In the sampling cycle of BQ76907, to save sampling resources and improve sampling efficiency, BQ76907 can automatically skip channels that are not actually connected to cells. Taking the 4S battery pack as an example, as shown in Figure 2-4, BQ76907 automatically skips the sampling of the 2nd, 4th, and 6th channels. In this way, the number of slots in an ADSCAN LOOP is reduced from 8 to 5, greatly improving the sampling efficiency.

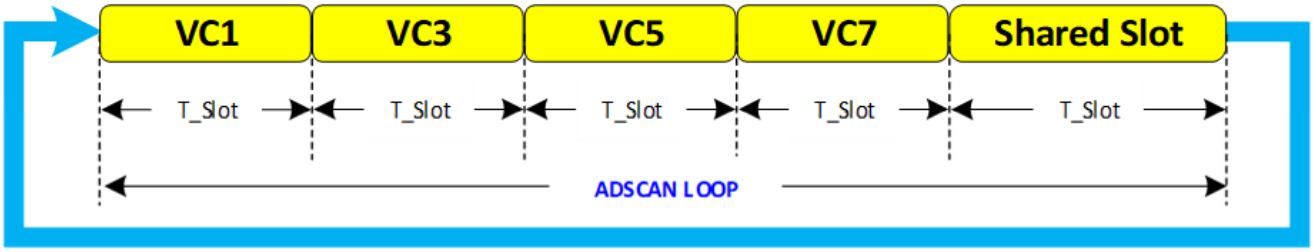

Figure 2-4. ADSCAN LOOP for 4S Pack

The LOOP_SLOW Speed Control described in the previous section still applies here.

3 Sleep Mode

When the device is in Sleep Mode, to save power, BQ76907 does not perform sampling all the time like in Normal Mode, but can perform sampling intermittently. As shown in Figure 3-1, in Sleep Mode, BQ76907 can maintain the IDLE state for a period of time and then enter the Burst sampling stage. The difference between Burst sampling and the ADSCAN LOOP mentioned previously is that Burst sampling can collect all cell voltages and Shared Slots at one time, to reduce the number of Bursts and save power consumption in Sleep Mode.

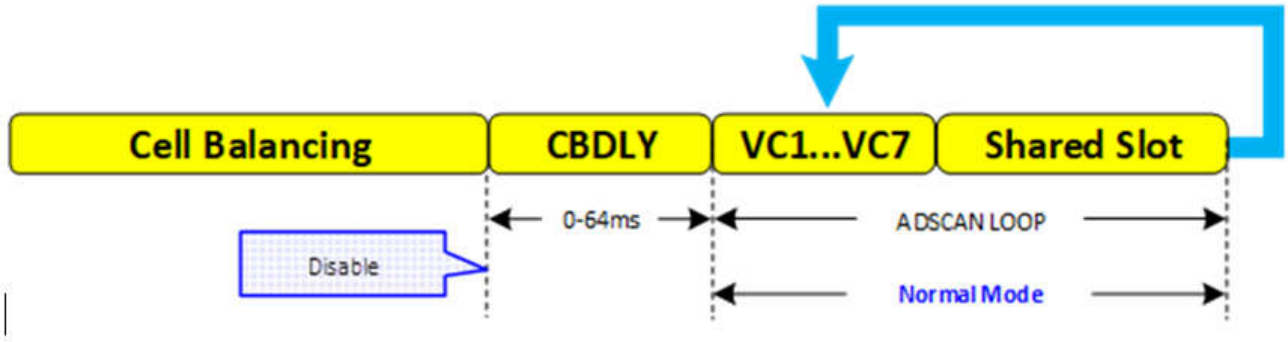

Figure 3-1. Voltage Measurement Loop in Sleep Mode (7S version)

The IDLE state time can be configured through the register Power:Sleep:Voltage Time. However, if the BQ76907 exits Sleep Mode during the Power:Sleep:Voltage Time, this can immediately perform a round of Burst sampling and then enter the Normal Mode sampling mode described previously.

4 Startup Mode

As shown in Figure 4-1, if this wakes up from SHUTDOWN Mode, exits from DEEPSLEEP Mode, or exits from CONFIG_UPDATE Mode, BQ76907 can enter Startup Mode. As shown in Figure 4-1, at the moment of wakeup or exit, BQ76907 can immediately perform Burst sampling similar to Sleep Mode, that is, sampling all cell voltages and Shared Slots. After sampling, if there is no abnormal event such as protection, this can enter Normal Mode normally.

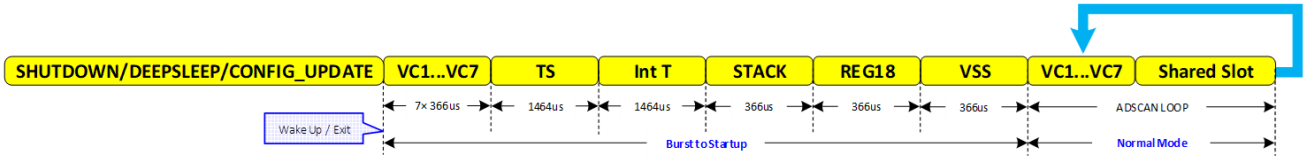

Figure 4-1. Voltage Measurement Loop in Startup Mode (7S version)

Note that in the Burst sampling phase of Startup Mode, all T_Slots are fixed and cannot be configured. In addition, except for temperature-related sampling, all voltage sampling is performed according to the minimum time, to complete the acquisition of all voltages as quickly as possible, speed up the startup time, and optimize the user experience.

5 Cell Balance Mode

BQ76907 integrates a balancing circuit, which uses a passive balancing method and supports a maximum internal balancing current of 50mA. However, the host must send a command to enable balancing. This does not only support simultaneous balancing of non-adjacent cells, but also adjacent cells.

When balancing is turned on, the pin voltages of the corresponding cell and the adjacent cells can change. Figure 5-1 shows the equivalent circuit before and after the balancing of the Cell_n cell is turned on.

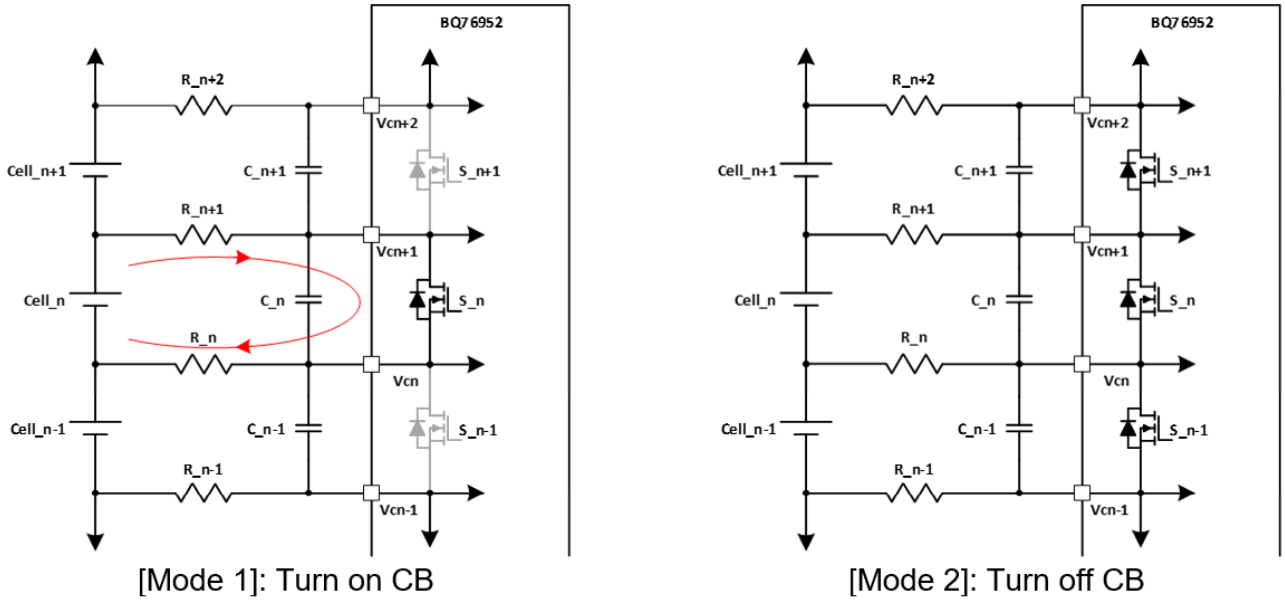

Figure 5-1. BQ76907 Internal Balance Circuit

By Figure 5-1, the corresponding VCx input pin voltage change as follows:

Table 5-1. VCx Pin Voltage Changes Before and After Cell Balance Is Turned On

Voltage	Balance OFF	Balance ON
$V_{(cn+1)} - V_{cn}$	V_{cell_n}	$\frac{V_{cell\_n}}{R_n + R_{n+1} + R_{\_dson}} \times R_{\_dson}$
$V_{(cn)} - V_{(cn-1)}$	V_{cell_n}	$V_{cell\_n-1} + \frac{V_{cell\_n}}{R_n + R_{n+1} + R_{\_dson}} \times R_{\_dson}$
$V_{(cn+2)} - V_{(cn+1)}$	V_{cell_n+1}	$V_{cell\_n+1} + \frac{V_{cell\_n}}{R_n + R_{n+1} + R_{\_dson}} \times R_{\_dson}$

To prevent incorrect sampling voltage due to battery balancing, balancing must be disabled during sampling. To balance the balancing capability (balancing duty cycle) and sampling rate, the BQ76907 can add several IDLE Slots after the normal sampling ADSCAN LOOP

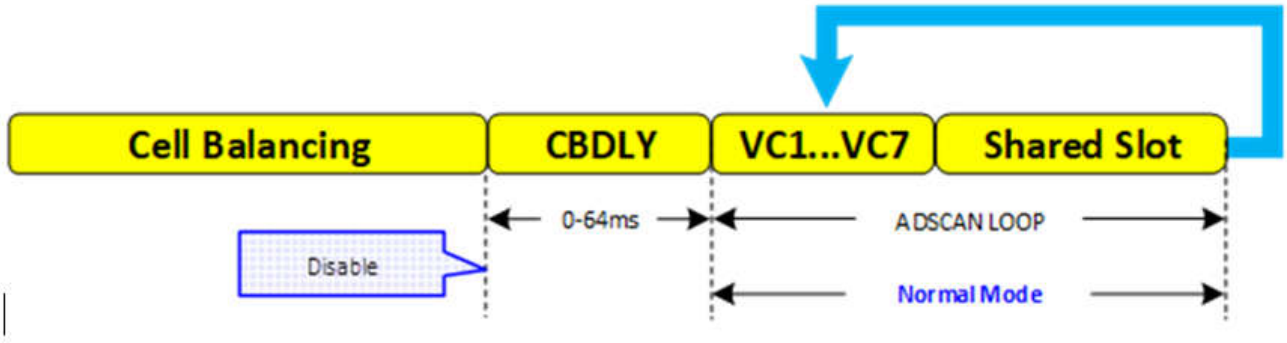

Figure 5-2. Voltage Measurement Loop in Cell Balance Mode (7S version)

$$m = \left(2^{CB\_Loop\_SLOW[1:0]+1} - 1\right) \times 8 \quad (2)$$

The more IDLE Slots are inserted, the greater the balancing duty cycle is, and the stronger the balancing ability of the battery pack is, but the sampling refresh rate can be reduced. Therefore, users need to configure the CB_LOOP_SLOW[1:0] register according to the actual usage scenario.

In addition, when the cell balancing is turned off, due to the existence of the RC network, the voltage recovery takes a certain amount of time, which can cause a large error in several voltage samplings after the cell balancing is turned off. To avoid such errors, BQ76907 opens a delayed sampling register: Settings: Cell Balancing: Balancing Configuration[CBDLY2:0]. Through this register, we can insert a 0-64ms delay between turning off Cell Balance and valid voltage sampling, as shown in Figure 5-3.

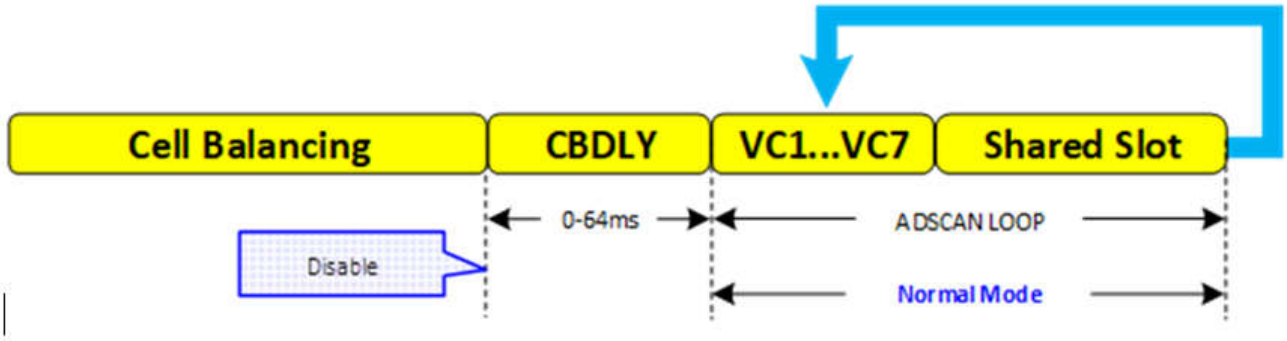

Figure 5-3. Voltage Measurement Loop in Cell Balance Mode (7S version)

6 Summary

This article explains the voltage sampling logic of BQ76905/07 in detail and gives suggestions for settings in different modes to help understand of BQ76905/07 more clearly and intuitively.

7 References

- Texas Instruments, *BQ76907 2-Series to 7-Series High Accuracy Battery Monitor and Protector for Li-Ion, Li-Polymer, LiFePO4 (LFP), and LTO Battery Packs*, data sheet.
- Texas Instruments, *BQ76907 Technical Reference Manual* .
- Texas Instruments, *5s–7s Battery Pack Reference Design With Low-Side MOSFET Control*, design guide.

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