Application Note

Why is short-circuit protection more challenging for high-side driver battery packs than low-side driver?

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ABSTRACT

Depending on where the protection FETs are located, lithium battery packs can be divided into high-side protection and low-side protection solutions. Compared to the low-side protection solution, the high-side protection solution is increasingly adopted in battery packs because AFE and MCU remain grounded together after a fault is triggered, and communication with MCU side can still be achieved. Short-circuit protection, as one of the most stringent test items for battery packs, frequently results in damage to the discharge MOS-DFET during R&D testing. Developers have observed that the high-side driver battery packs often present greater challenges than the low-side driver in practical implementation. This article will explain why the short-circuit protection driver in the high-side protection solution is more challenging than that in the low-side protection solution, and intend to provide insights for readers undertaking the high-side driver design.

Table of Contents

1 Introduction to the low-side/high-side protection solutions

Depending on where the protection FETs are located Figure 1-2, we can divide the battery packs into a low-side Figure 1-1 protection solution and a high-side protection solution.

Figure 1-1 illustrates a diagram of the low-side protection architecture, where both charge tube CFET and discharge tube DFET are positioned between B- and PACK- and situated at the low-side of the battery pack. AFE in TI's BQ769x0 and BQ7690x families integrates a low-side driver.

Figure 1-2 illustrates a diagram of the high-side protection architecture, where both charge tube CFET and discharge tube DFET are positioned between B+ and PACK+ and situated at the high-side of the battery pack. AFE in TI's BQ769x2 family integrates a high-side driver.

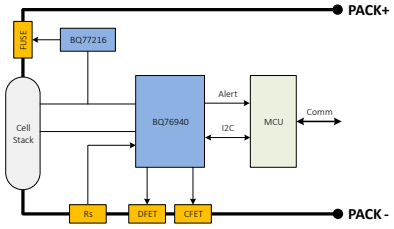

Figure 1-1. Low-side protection solution

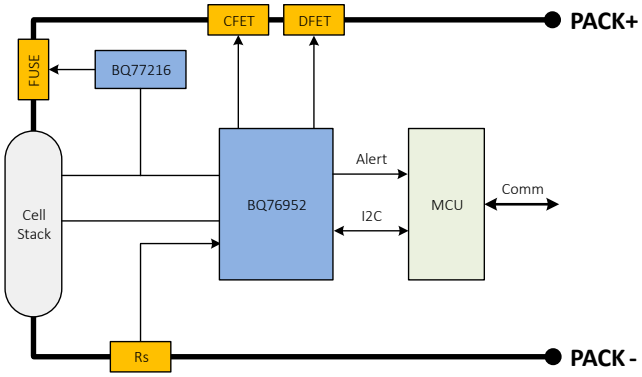

Figure 1-2. High-side protection solution

For the low-side protection solution, when CFET and DFET are turned off, the battery pack ground and system ground are no longer connected. Consequently, once protection is triggered and the charge/discharge FETs are turned off, direct communication between the battery side and the system side is no longer possible. To maintain communication, the isolated communication must be employed. This not only increases cost but also elevates power consumption, particularly during undervoltage protection. Excessive communication power consumption further exacerbates the situation for battery packs already operating under undervoltage conditions. Therefore, the low-side solution is primarily applied in cost-sensitive products without complex communication requirements.

In contrast to the low-side protection, the high-side protection solution maintains a common ground connection between the battery pack and system side even after protection is triggered. Therefore, communication between them can still be achieved without requiring additional isolation measures. Furthermore, the system becomes safer as the battery positive terminal is disconnected upon triggering the protection.

2 Short-circuit protection results in overvoltage damage to DFET

Because real circuits are not ideal ones, there is always some parasitic inductance in the power loop. During short-circuit protection, the short-circuit current becomes extremely high. At the instant of protection, the DFET switches off, and the abrupt change in current induces a very high voltage. Applying this induced voltage to the DFET will cause overvoltage damage to DFET.

2.1 Low-side protection solution

To simplify the analysis, the parasitic inductance on the load side and the battery side are equivalent to L1 and L2 respectively in the article.

Figure 2-1 shows the equivalent circuit of the low-side protection solution after DFET short-circuit protection is turned off.

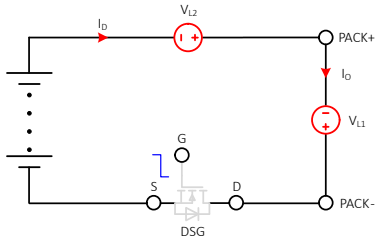

Figure 2-1. Low-side protection solution-the discharge tube DFET shutdown equivalent circuit

After the short-circuit protection, DSG turns off. The current flowing through L1 lacks freewheeling loop, quickly reducing from I_o to zero. Consequently, a substantial induced voltage is generated across L1:

$$V_{L1} = \mathrm{L1}\frac{dI_O}{dt} \quad (1)$$

and the current flowing through L2 also decreases rapidly from I_o to zero because there is no freewheeling loop for the current across L2. Thus, a substantial induced voltage is also generated across L2:

$$V_{L2} = \mathrm{L2}\frac{dI_O}{dt} \quad (2)$$

Therefore, the voltage at two terminals of DS can be expressed by the following equation:

$$V_{DS\_LS} = V_{L1} + V_{L2} + V_{bat} = \mathrm{L1}\frac{dI_O}{dt} + \mathrm{L2}\frac{dI_O}{dt} + V_{bat} \quad (3)$$

2.2 High-side protection solution

Figure 2-2 shows the equivalent circuit of the high-side protection solution after DFET short-circuit protection is turned off.

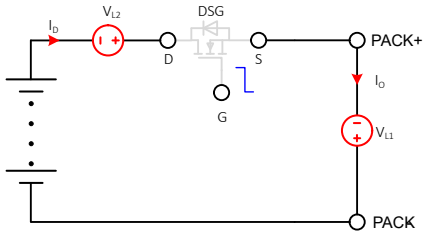

Figure 2-2. High-side protection solution-the discharge tube DFET shutdown equivalent circuit

Similar to the low-side protection solution, the voltage at two terminals of DS can be expressed by the following equation:

$$V_{DS\_HS} = V_{L1} + V_{L2} + V_{bat} = \mathrm{L1}\frac{dI_O}{dt} + \mathrm{L2}\frac{dI_O}{dt} + V_{bat} \quad (4)$$

2.3 Summary

From the above analysis, it is evident that the voltage stress endured by DFET during short-circuit protection is identical in both high-side and low-side protection solutions.

3 Short-circuit protection results in overtemperature damage to DFET

Neglecting the effect of parasitic inductance, the main waveform of DFET during shutdown, as shown in Figure 3-1, can be divided into four distinct modes. And because DS voltage of mode 1 (t_0-t_1) is zero and the current of mode 4 (t_3-t_4) is zero, neither of these modes generates power consumption, so only mode 2 and mode 3 really contribute to actual power consumption. Mode 2 and mode 3 are analyzed separately below.

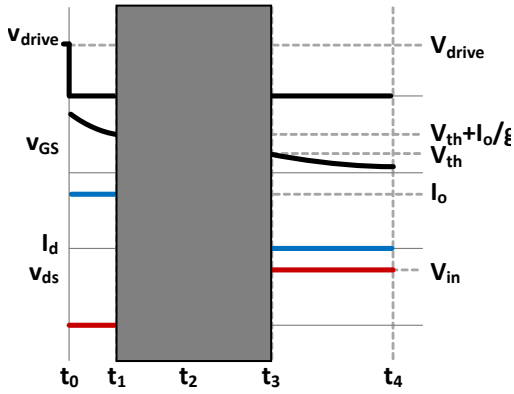

Figure 3-1. Primary waveform during the discharge MOS shutdown

[Mode 2: t_1-t_2]: This phase constitutes the Miller plateau of MOS tube, as shown in Figure 3-2. The junction capacitance Cgd and Cds are charged by the drive resistor R_{drive}, causing v_{DS} voltage to rise. At the moment of t_2, v_{DS}reaches V_{bat}+V_{FD1}, and mode 2 ends. In this mode, the current through the discharge MOS tube is held to Io, and the speed at which the junction capacitance is charged depends on the size of R_{drive}. The smaller R_{drive}, the faster the charge, the shorter the time for mode 2.

[Mode 3: t_2-t_3]: As shown in Figure 3-3, at the moment of t_2, the discharge MOS enters mode 3 and the current flowing through the discharge MOS tube decreases from Io. C_{gs} discharges through R_{drive}, C_{gd} charges through R_{drive}, and v_{GS}begins to decrease. At the moment of t_3, the current flowing through the discharge MOS decreases to zero and v_{GS}decreases to the turn-on voltage V_{th}, ending in mode 3. In this mode, the speed at which the junction capacitance charges and discharges is also dependent on the size of R_{drive}. The smaller the R_{drive}, the faster the charge and discharge, the shorter the mode 3.

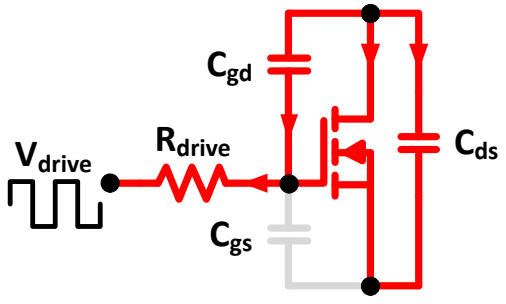

Figure 3-2. Discharge MOS shutdown mode

(a) mode 2 [t_1-t_2]

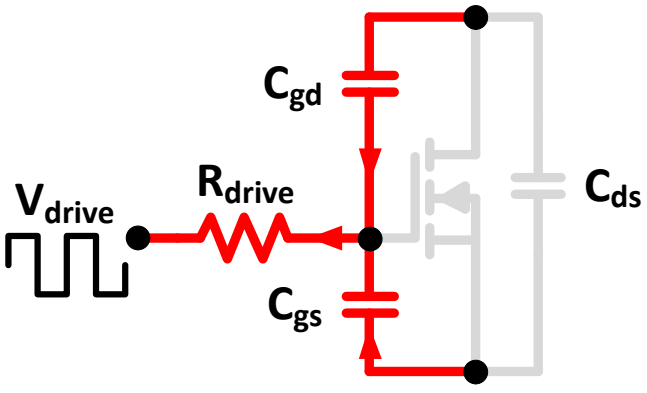

Figure 3-3. Discharge MOS shutdown mode

(b) mode 3 [t_2-t_3]

Based on the above analysis, the losses incurred by the discharge MOS at the shutdown instant can be expressed by the following equation:

$$P_{loss} = \frac{1}{2} \times V_{in} \times I_o \times \left(t_3 - t_1\right) \quad (5)$$

From the above equation, it is evident that the longer the duration of t_3-t_1, the greater the losses generated by the discharge MOS during the protection instant, resulting in more severe heating.

3.1 Low-side protection solution

For the low-side protection solution, taking BQ76940 as an example, G-pole voltage, V_G, is clamped around -0.3V by the built-in diode at the shutdown instant of DFET. S-pole voltage, V_S, is clamped at BAT-, also equal to 0V.

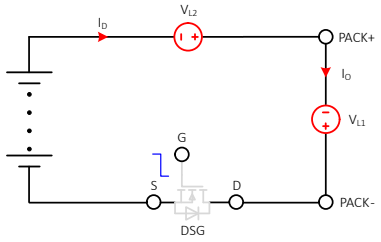

Figure 3-4. Low-side protection solution-the discharge tube DFET shutdown equivalent circuit

Figure 3-5 shows BQ76940 DSG Pin equivalent circuit. When AFE turns off DFET, DSG Pin pulls to ground through R_{DSG_OFF} inside AFE, so the shutdown time depends only on the junction capacitance of DFET and the discharge resistor R_{DSG_OFF}=2.5KOhm.

When G-pole voltage of DFET drops to meet the following conditions, DFET can be turned off completely.

$$V_G < V_{GSth_{DFET}} \quad (6)$$

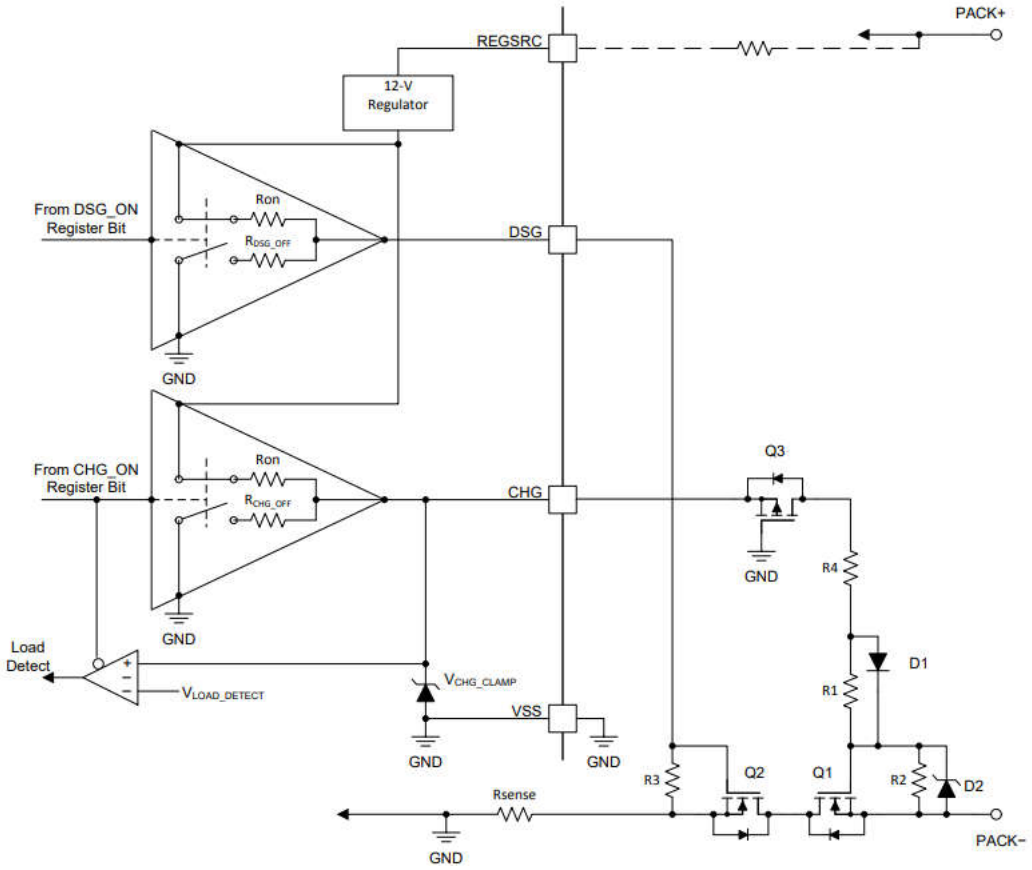

Figure 3-5. BQ76940 DSG pin equivalent diagram

Naturally, the users may further regulate the shutdown speed by placing an additional resistor between DSG pin and G-pole of DFET.

3.2 High-side protection solution

For the high-side protection solution, taking BQ76952 as an example, G-pole discharges to ground when DFET is off. The voltage V_G is clamped around -0.3V by the built-in diode, but S-pole voltage V_S is pulled down to $-V_{L1}$ because of the magnitude of the parasitic inductance. Thus, even if G-pole has already discharged to -0.3V relative to ground, GS voltage V_{GS} is still equal to V_{L1}-0.3V as long as the following conditions are met:

$$\boldsymbol{V_{L1} - 0.3V > V_{GSth_{DFET}}} \quad (7)$$

DFET cannot be fully turned off.

GS voltage cannot discharge the junction capacitance via DSG pin, but must instead discharge through the resistors connected in parallel across two terminals of GS in DFET. This resistor primarily serves to prevent electrostatic accumulation at GS terminals and avoid unintended turn-on. Consequently, the resistor is typically selected to be relatively large, as a smaller GS resistor would increase DC load on BQ76952 charge pump. BQ76952 is not recommended for significant DC load. Therefore, GS resistor is typically of the megohm order, such as 10 MΩ value selected in both Reference 3 and Reference 4. Consequently, the charge and discharge currents of the junction capacitance are in the uA range, resulting in a very slow shutdown time. This generates substantial thermal losses during the shutdown process, leading to overtemperature and damage of DFET.

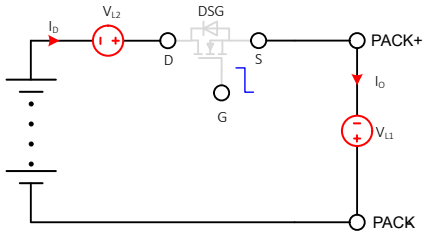

Figure 3-6. High-side protection solution-the discharge tube DFET shutdown equivalent circuit

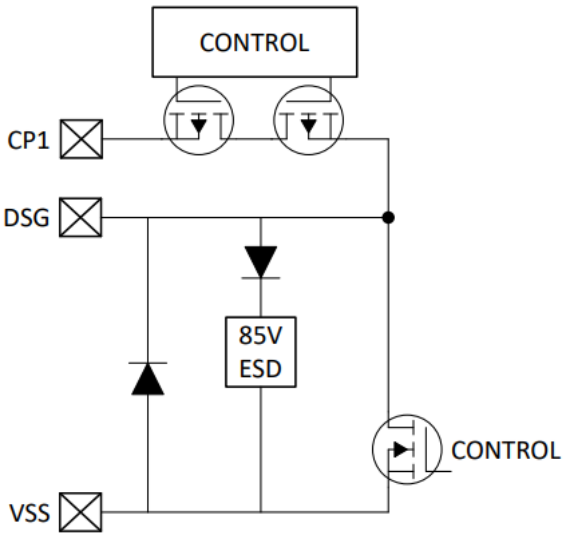

Figure 3-7. BQ76952 DSG pin equivalent diagram

3.3 Summary

In summary, compared to the low-side protection solution, the high-side protection solution is not clamped because S-pole of DFET is tied to P+. This causes DFET to turn off slowly when short-circuit protection is pulled down to a negative voltage by the induced voltage of the parasitic inductance at the load side, which makes it more susceptible to overtemperature damage.

4 Conclusion

Short-circuit protection, as one of the most stringent test items, poses a risk of DFET damage regardless of whether a low-side or high-side protection solution is employed. This risk primarily stems from two causes: overvoltage and overtemperature:

Overvoltage damage: Both low-side and high-side protection solutions subject the DFET to equivalent voltage stress during short-circuit protection.

Overtemperature damage: High-side protection solutions exhibit slower DFET shutdown, more severe heating, and are more susceptible to overtemperature damage during short-circuit protection.

Reference 2 and Reference 5 are available for driver design with short circuit protection.

5 References

1. *Reference Design for 10-Cell to 16-Cell Battery Packs in Series with Precise Battery Measurement and High-Side MOSFET Control Function (TIDA-010208)*
2. *Design and Considerations for Short-Circuit Protection Circuits in High-Series Lithium Battery Packs (ZHCAAJ0)*
3. *BQ76952 3-Series to 16-Series High Accuracy Battery Monitor and Protector for Li-Ion, Li-Polymer, and LiFePO4 Battery Packs dataset (SLUSE13)*
4. *BQ76952 Technical Reference Manual (SLUUBY2)*
5. *Causes of DSG FET Damage in BQ76952-Based Battery Pack Short-Circuit Protection and Optimization Methods (ZHCAB67)*

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Last updated 10/2025