

# Programmer's Guide

## LMK3H2108A11 Configuration Guide

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### ABSTRACT

This document provides the configuration information for the LMK3H2108A11 device. For the default configuration of the LMK3H2108 device, refer to the [LMK3H2108 data sheet](#).

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### Table of Contents

<b>1 Configuration Overview</b> .....	1
1.1 LMK3H2108A11 Configuration Information.....	1
<b>2 Revision History</b> .....	6

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### 1 Configuration Overview

This section provides an overview of the critical device settings of the configurations.

#### 1.1 LMK3H2108A11 Configuration Information

**Table 1-1. LMK3H2108A11 Frequency Configuration**

OTP Page	OUT0 (MHz)	OUT1 (MHz)	OUT2 (MHz)	OUT3 (MHz)	OUT4 (MHz)	OUT5 (MHz)	OUT6 (MHz)	OUT7 (MHz)
OTP Page 0	100	100	100	100	100	100	100	100
OTP Page 1	100	100	100	100	100	100	100	100
OTP Page 2	100	100	100	100	100	100	100	100
OTP Page 3	100	100	100	100	100	100	100	100

**Table 1-2. LMK3H2108A11 I2C Configuration**

OTP Page	I2C Configuration
OTP Page 0	I2C Address: 0x68 1 Byte Register Addressing
OTP Page 1	I2C Address: 0x68 1 Byte Register Addressing
OTP Page 2	I2C Address: 0x68 1 Byte Register Addressing
OTP Page 3	I2C Address: 0x68 1 Byte Register Addressing

**OTP Page 0**

**Table 1-3. LMK3H2108A11 GPI Settings, OTP Page 0**

GPI Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPI0	GPI	Normal	Disabled	Disabled
GPI1	GPI	Normal	Disabled	Disabled
GPI2	GPI	Normal	Enabled	Disabled
GPI3	GPI	Normal	Enabled	Disabled
GPI4	Group OE, OE_GROUP_4	Inverted	Disabled	Enabled
GPI5	Group OE, OE_GROUP_5	Inverted	Disabled	Enabled

**Table 1-4. LMK3H2108A11 GPIO Settings, OTP Page 0**

GPIO Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPIO0	Dynamic OTP	Normal	Enabled	Disabled
GPIO1	Dynamic OTP	Normal	Enabled	Disabled
GPIO2	I2C Bit 0	Normal	Enabled	Disabled
GPIO3	I2C Bit 1	Normal	Enabled	Disabled
GPIO4	GPI	Normal	Disabled	Enabled

**Table 1-5. LMK3H2108A11 Input Settings, OTP Page 0**

Input	Powered Up/Down	Input Format	Input Termination
IN_0	Powered Up	Differential IN0	100 Ω P to N
IN_1	Powered Down	N/A (IN1 Unused)	None, DC
IN_2	Powered Down	N/A (IN2 Unused)	None, DC

**Table 1-6. LMK3H2108A11 Output Settings, OTP Page 0**

Output	Frequency (MHz)	Format	Clock Source	Output State	OE Group	SSC Behavior
OUT0	100	100 Ω LP-HCSL	IN_0	Enabled	OE_GROUP_5	Disabled
OUT1	100	100 Ω LP-HCSL	IN_0	Enabled	OE_GROUP_4	Disabled
OUT2	100	100 Ω LP-HCSL	IN_0	Enabled	OE_GROUP_4	Disabled
OUT3	100	100 Ω LP-HCSL	IN_0	Enabled	OE_GROUP_4	Disabled
OUT4	100	100 Ω LP-HCSL	IN_0	Enabled	OE_GROUP_4	Disabled
OUT5	100	100 Ω LP-HCSL	IN_0	Enabled	OE_GROUP_4	Disabled
OUT6	100	100 Ω LP-HCSL	IN_0	Enabled	OE_GROUP_4	Disabled
OUT7	100	100 Ω LP-HCSL	IN_0	Enabled	OE_GROUP_5	Disabled

**OTP Page 1**

**Table 1-7. LMK3H2108A11 GPI Settings, OTP Page 1**

GPI Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPI0	GPI	Normal	Disabled	Disabled
GPI1	GPI	Normal	Disabled	Disabled
GPI2	GPI	Normal	Enabled	Disabled
GPI3	GPI	Normal	Enabled	Disabled
GPI4	Group OE, OE_GROUP_4	Inverted	Disabled	Enabled
GPI5	Group OE, OE_GROUP_5	Inverted	Disabled	Enabled

**Table 1-8. LMK3H2108A11 GPIO Settings, OTP Page 1**

GPIO Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPIO0	Dynamic OTP	Normal	Enabled	Disabled
GPIO1	Dynamic OTP	Normal	Enabled	Disabled
GPIO2	I2C Bit 0	Normal	Enabled	Disabled
GPIO3	I2C Bit 1	Normal	Enabled	Disabled
GPIO4	GPI	Normal	Disabled	Enabled

**Table 1-9. LMK3H2108A11 Input Settings, OTP Page 1**

Input	Powered Up/Down	Input Format	Input Termination
IN_0	Powered Down	Differential IN0	100 Ω P to N
IN_1	Powered Down	N/A (IN1 Unused)	None, DC
IN_2	Powered Down	N/A (IN2 Unused)	None, DC

**Table 1-10. LMK3H2108A11 Output Settings, OTP Page 1**

Output	Frequency (MHz)	Format	Clock Source	Output State	OE Group	SSC Behavior
OUT0	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_5	Disabled
OUT1	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_4	Disabled
OUT2	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_4	Disabled
OUT3	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_4	Disabled
OUT4	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_4	Disabled
OUT5	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_4	Disabled
OUT6	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_4	Disabled
OUT7	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_5	Disabled

OTP Page 2

**Table 1-11. LMK3H2108A11 GPI Settings, OTP Page 2**

GPI Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPI0	GPI	Normal	Disabled	Disabled
GPI1	GPI	Normal	Disabled	Disabled
GPI2	GPI	Normal	Enabled	Disabled
GPI3	GPI	Normal	Enabled	Disabled
GPI4	Group OE, OE_GROUP_4	Inverted	Disabled	Enabled
GPI5	Group OE, OE_GROUP_5	Inverted	Disabled	Enabled

**Table 1-12. LMK3H2108A11 GPIO Settings, OTP Page 2**

GPIO Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPIO0	Dynamic OTP	Normal	Enabled	Disabled
GPIO1	Dynamic OTP	Normal	Enabled	Disabled
GPIO2	I2C Bit 0	Normal	Enabled	Disabled
GPIO3	I2C Bit 1	Normal	Enabled	Disabled
GPIO4	GPI	Normal	Disabled	Enabled

**Table 1-13. LMK3H2108A11 Input Settings, OTP Page 2**

Input	Powered Up/Down	Input Format	Input Termination
IN_0	Powered Down	Differential IN0	100 Ω P to N
IN_1	Powered Down	N/A (IN1 Unused)	None, DC
IN_2	Powered Down	N/A (IN2 Unused)	None, DC

**Table 1-14. LMK3H2108A11 Output Settings, OTP Page 2**

Output	Frequency (MHz)	Format	Clock Source	Output State	OE Group	SSC Behavior
OUT0	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_5	Enabled, -0.199% Down-spread
OUT1	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_4	Enabled, -0.199% Down-spread
OUT2	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_4	Enabled, -0.199% Down-spread
OUT3	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_4	Enabled, -0.199% Down-spread
OUT4	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_4	Enabled, -0.199% Down-spread
OUT5	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_4	Enabled, -0.199% Down-spread
OUT6	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_4	Enabled, -0.199% Down-spread
OUT7	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_5	Enabled, -0.199% Down-spread

## OTP Page 3

Table 1-15. LMK3H2108A11 GPI Settings, OTP Page 3

GPI Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPI0	GPI	Normal	Disabled	Disabled
GPI1	GPI	Normal	Disabled	Disabled
GPI2	GPI	Normal	Enabled	Disabled
GPI3	GPI	Normal	Enabled	Disabled
GPI4	Group OE, OE_GROUP_4	Inverted	Disabled	Enabled
GPI5	Group OE, OE_GROUP_5	Inverted	Disabled	Enabled

Table 1-16. LMK3H2108A11 GPIO Settings, OTP Page 3

GPIO Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPIO0	Dynamic OTP	Normal	Enabled	Disabled
GPIO1	Dynamic OTP	Normal	Enabled	Disabled
GPIO2	I2C Bit 0	Normal	Enabled	Disabled
GPIO3	I2C Bit 1	Normal	Enabled	Disabled
GPIO4	GPI	Normal	Disabled	Enabled

Table 1-17. LMK3H2108A11 Input Settings, OTP Page 3

Input	Powered Up/Down	Input Format	Input Termination
IN_0	Powered Down	Differential IN0	100 Ω P to N
IN_1	Powered Down	N/A (IN1 Unused)	None, DC
IN_2	Powered Down	N/A (IN2 Unused)	None, DC

Table 1-18. LMK3H2108A11 Output Settings, OTP Page 3

Output	Frequency (MHz)	Format	Clock Source	Output State	OE Group	SSC Behavior
OUT0	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_5	Enabled, -0.3% Down-spread
OUT1	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_4	Enabled, -0.3% Down-spread
OUT2	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_4	Enabled, -0.3% Down-spread
OUT3	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_4	Enabled, -0.3% Down-spread
OUT4	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_4	Enabled, -0.3% Down-spread
OUT5	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_4	Enabled, -0.3% Down-spread
OUT6	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_4	Enabled, -0.3% Down-spread
OUT7	100	100 Ω LP-HCSL	PATH1	Enabled	OE_GROUP_5	Enabled, -0.3% Down-spread

## 2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

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