

Designing a Low Cost Flyback Power Supply Using Boost Converter (TPS61165) for High Frequency Inverter

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ABSTRACT

Inverters are commonly used in residential and industrial applications for AC back up in case of power outages. The function of an inverter is to convert the stored energy in the battery to AC voltage that can be used to provide power to various devices such as fans and lights when AC power is not available.

Depending upon the power output (VA), inverters come in various power ranges ranging from 100 VA to 3.2 kVA. The input of the power inverter may come from a 12 V, 24 V, or 48 V battery. In a high frequency (HF) inverter, AC voltage is converted to an intermediate high voltage before it's converted to an AC waveform using pulse width modulation (PWM).

This application note discusses designing an integrated and low-cost power supply for the most commonly used inverter application that runs from 12-V battery. However, the concept of using a boost converter for a flyback application can be applied across any similar design.

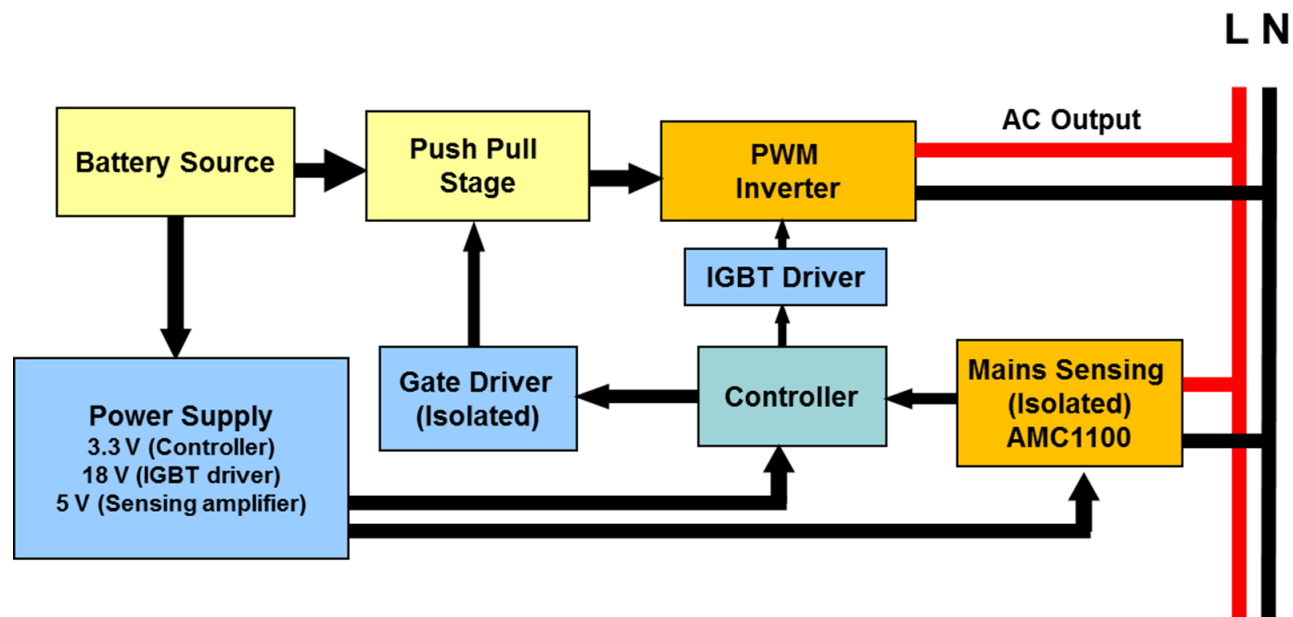


Figure 1. Block Diagram of a Typical HF Inverter

In a conventional 12-V based inverter design, isolated supplies are required between AC mains and battery side of the inverter. The power supply on the AC mains side typically powers the isolated amplifier used for mains current sensing, while the power supply on the battery side provides power to the controller used for generating PWMs for the H-bridge and battery charging. 18 V is required for powering the IGBT driver driving the PWM Inverter stage.

One more design consideration for the power supply is to keep in mind the lowest possible input voltage to the inverter from a standard 12-V lead acid battery. Typically, in an inverter application, the cutoff of the main circuitry is done when the battery voltage reaches approximately 10.8 V. However even after this cutoff, the idle discharge of the lead acid battery may cause its voltage to fall down to 5 V (in cases, when the inverter hasn't been charged for a long time – a common occurrence in places where AC power outages are longer). Under such conditions, the supply must be able to power up the system even at an input voltage of 5 V to enable the charging of the battery.

In addition, isolation is also required between the power supply windings. Generally, isolation voltage of 2.5 kV is sufficient between:

- 5 V on the mains side and any of the other remaining windings
- 18 V on the mains side and any of the other remaining windings.

Keeping all these factors in mind, a power supply with the following specifications must be designed:

- **Input voltage** – 4.5 V to 16 V
- **Output rail-1** – 3.3 V (4 V + linear regulator at 3.3 V)
- **Output rail-2** – 5 V (6 V + linear regulator at 5 V)
- **Output rail-3** – 18 V (main output, we close the loop here)
- **Output current** on each rail is below 60 mA

18 V is used for powering the IGBT driver, 3.3 V is used for driving the microcontroller, and the third supply of 5 V is used for powering the mains side of the sense amplifier.

The most suitable topology to realize this circuit is flyback topology. In order to achieve integration and lowest possible cost, TI used a boost converter in a flyback topology and in particular the TPS61165 fits perfectly to this application since it meets our specifications (see [Design Steps](#)) and is a low-cost part with an integrated FET. For higher input voltages, LM5001 can be considered. By using a couple inductor instead of a single coil used in boost topology and placing an output diode in a configuration such that it conducts when the FET in the boost converter is OFF, we can achieve the flyback action (which is storing energy on one cycle and delivering it to the load on other cycle).

Design Steps

In order to use a boost converter in a flyback configuration, we first must check if the integrated FET present in the boost converter is able to support the peak current and whether the voltage stress on the internal MOSFET is within the limits of the device.

Consider a single main output, 18 V, and calculate the power stage with the total load connected only to this output. Later divide the power into the auxiliary outputs and report the impedances according to the related turn ratios. Now the maximum primary to secondary turn ratio (N_p/N_s) is calculated from [Equation 1](#).

$$\frac{N_P}{N_S} \leq \frac{V_{MOSMAX} - V_{INMAX}}{(V_{OUT} + V_F) \times K_{SPIKE}} \quad (1)$$

Where:

$$\frac{N_P}{N_S} = \text{turns ratio,}$$

V_{MOS_MAX} = maximum allowed MOSFET voltage

V_{INMAX} = maximum input voltage

V_{OUT} = output voltage

V_F = forward voltage of secondary side diode

K_{SPIKE} = spike coefficient

The “spike coefficient” is the ratio between the spike on the reflected voltage due to leakage inductance, and the reflected voltage calculated without parasitic (in an ideal scenario).

Choosing “ K_{SPIKE} close to 1” means that no spike is allowed. This leads to slow demagnetization of the leakage inductance and time is lost during the transition between on and off. During this transition time, we also lose some energy from the main primary inductance, therefore reducing efficiency. $K_{SPIKE} > 1.5$ can put a lot of stress on the MOSFET, and cause it to operate at its absolute maximum rating.

In this particular example the input voltage range is 4.5 V to 16 V, the output voltage is 18 V and the maximum allowed MOSFET voltage is 38 V. If we select $K_{SPIKE} = 1.5$ and supposing $V_F = 0.7$ V we get:

$$\frac{N_p}{N_s} \leq 0.78 \tag{2}$$

If we select this ratio to be 0.5, the reflected voltage becomes $18 \text{ V} \times 0.5 \text{ V} = 9 \text{ V}$ and this adds up to the maximum input voltage of 16 V to give us a total of 25 V in the worst case. We now have plenty of margins for proper MOSFET operation.

From the equation valid for continuous conduction mode (CCM) flyback:

$$V_{OUT} = V_{IN} \frac{N_s}{N_p} \frac{D}{1-D} \tag{3}$$

We derive:

$$D = \frac{1}{1 + \frac{N_s \times V_{IN}}{N_p \times V_{OUT}}} \tag{4}$$

Entering the following values: [Equation 4](#)

$$V_{IN_MIN} = 4.5 \text{ V and } V_{IN_MAX} = 16 \text{ V,}$$

we get:

$$D_{MIN} = 36\% \text{ and } D_{MAX} = 66.7\%$$

Ensure that the peak current rating is within the limit of the integrated FET present in the boost converter. With all outputs (3.3 V, 5 V and 18 V) fully loaded at 60 mA, a total power of $P_{out} = (4 \text{ V} + 6 \text{ V} + 18 \text{ V}) \times 60 \text{ mA} = 1.68 \text{ W}$, since the load is related to the voltage before the linear regulators. Assuming around 80% efficiency, the input power is $P_{in} = 2.1 \text{ W}$.

Knowing the minimum and maximum duty cycle as well as the input power, we can draw how the MOSFET current will be; illustrated in [Figure 2](#).

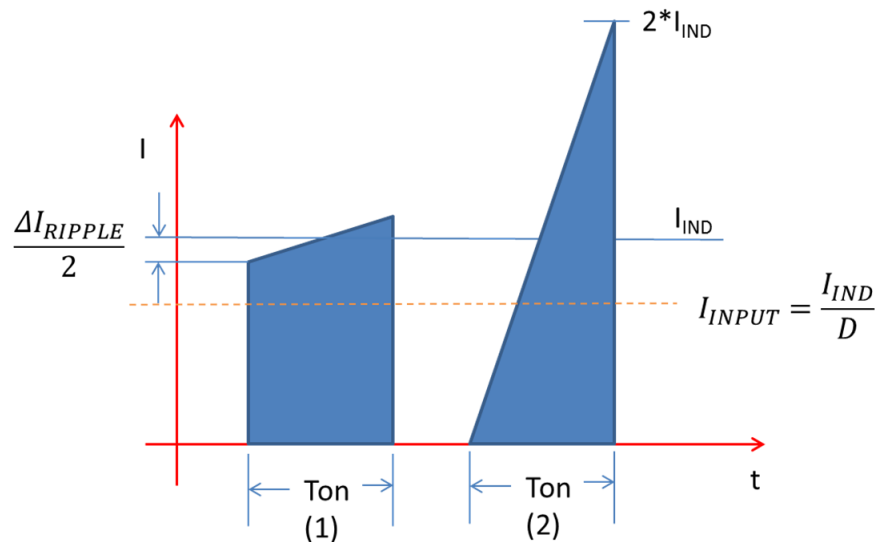


Figure 2. MOSFET Current in CCM and Transition Mode

Here we see two cases, the left blue area defines the switch current in CCM while in the right part the peak-to-peak ripple current is twice the inductor current; this particular working condition is called *transition mode*. If the ripple current continues to increase, the converter works in DCM. The goal is to let the converter work in CCM in the whole input voltage range and at least at full load. This reduces the peak current to minimum value in the MOSFET. The peak-peak inductor current is calculated from:

$$\Delta I_{PP} = \frac{V_{IN}\Delta t}{L_P} = \frac{D \times V_{IN}}{F_{SW} \times L_P} = \Delta I_{RIPPLE} \quad (5)$$

where L_P = primary side inductance, F_{SW} = switching frequency.

In [Figure 2](#), I_{IND} = inductor current, which is the average total inductor current (primary side during Ton and secondary side during Toff) and I_{input} = input current of the converter, which is simply I_{IND} divided by duty cycle D.

The converter always works in CCM, if the following is satisfied:

$$\frac{\Delta I_{RIPPLE}}{2} \leq I_{IND} \quad (6)$$

When combining [Equation 6](#) and [Equation 5](#), the result is:

$$L_P \geq \frac{(V_{IN} \times D)^2}{2P_{IN}F_{SW}} \quad (7)$$

where V_{in} = Vin maximum, and D = Dmin

From [Equation 7](#) a minimum primary inductance value of 6.17 μ H is obtained, since the switching frequency of TPS61165 is fixed and equal to 1.2 MHz.

A new minimum value of inductance is calculated that is needed to keep the maximum peak (average plus half of ripple) below the worst case overcurrent protection of the TPS61165: this value is 0.96 A (see the TPS61165 datasheet, [SLVS790](#)).

The minimum primary inductance in this case must be $L_P \geq 5.85 \mu$ H.

If 10 μ H is chosen, there is plenty of margin to stay in CCM in the whole input voltage range and for most of the output load.

Inverter designers already use linear regulators for 3.3 V and 5 V output such as TLV1117-33 and TLV1117-50. Thus, both of these can be used at the output of the cross-regulated transformer windings.

Transformer Design

In order to design a low-cost transformer, we keep ΔB small to reduce the core losses at the expense of a bigger transformer. We use N49 core (from EPCOS) for the transformer, EFD25 SMD as the coil former. N87 can also be used, however, the core losses for N49 are three times less than N87. 750313527 part number from Würth Electronics was custom designed for this application.

Design Equations

$$V_{OUT} = V_{IN} \frac{N_s D}{N_p (1-D)}; D = \frac{1}{1 + \frac{N_s \times V_{IN}}{N_p \times V_{OUT}}}; F_{RHPZ} = \frac{(1-D)^2 R_{LOAD}}{2\pi D L_{SEC}}; C_{OUT} \geq \frac{I_{OUTmax} D_{MAX}}{2\pi D \times L_{SEC}} \quad (8)$$

Where:

V_{out} = output voltage,

D = Duty cycle,

F_{RHPZ} = Right Half Plane Zero

C_{out} = Equivalent output capacitor on a single output: collect all capacitors reported by the square of the turn ratios

$$ESR \leq \frac{\Delta V_{RIPPLE}}{\frac{\Delta I_{RIPPLE}}{2} + \frac{I_{OUTmax}}{1-D_{MAX}}}; I_{COUT_RMS} = I_{OUT} \sqrt{\frac{D}{1-D}}; \frac{N_p}{N_s} = \frac{V_{MOSMAX} - V_{INMAX}}{(V_{OUT} + V_F) \times K_{SPIKE}} \quad (9)$$

Where:

ESR = series resistance of the electrolytic capacitors,

I_{COUT_RMS} = RMS current on the equivalent electrolytic capacitor,

N_p/N_s = primary to equivalent secondary turns ratio

$$\Delta I_{PP} = \frac{V_{IN} \Delta t}{L_P} = \frac{D \times V_{IN}}{F_{SW} \times L_P} = \Delta I_{RIPPLE}; \quad \frac{\Delta I_{RIPPLE}}{2} \leq I_{IND}; \quad I_{INPUT} = \frac{I_{IND}}{D}; \quad L_P \geq \frac{(V_{IN} \times D)^2}{2P_{IN} F_{SW}} \quad (10)$$

Where:

ΔI_{RIPPLE} = peak-peak ripple,
 I_{INPUT} = Input current

Design Results

Figure 3 illustrates the final schematic of the system. The SW pin of TPS61165 is connected to the primary winding of the transformer T1. The FB pin is shorted because the optocoupler U4 is used to close the loop. Therefore, the collector of U4 is connected directly to the COMP pin, which sources 100 μ A into the optocoupler; this current is seen as a load. The network R1, C8, C100 is reducing the gain of the *inner-loop* in order to have it stable in all conditions. On the secondary side, the two unregulated outputs 4 V and 6 V are followed with two low-drop linear regulators: TLV1117, specialized to supply 3.3 V and 5 V.

The main output is 18 V and the loop is closed to it by means of the network driven by the LMV431. This is a standard feedback network, and instead of employing a TL431, the LMV equivalent part works with a lower cathode current, allowing reduced current consumption.

In order to meet the voltage regulation in a multi-output flyback topology when cross-windings are fully loaded, there must be a minimum load (in this case, around 8 mA on 18-V output) on the voltage output regulated with the feedback circuitry. The converter goes out of regulation on the 3.3 V and 5 V rails if the 18-V output is not loaded with a minimum amount of current. The Zener diode D2 and D6 are needed in case the 18 V is fully loaded and the 3.3 V and 5 V are unloaded. The unavoidable spikes present on the unloaded output will integrate the voltage on C1 and C6 capacitors, which can overstress the inputs of the linear regulators.

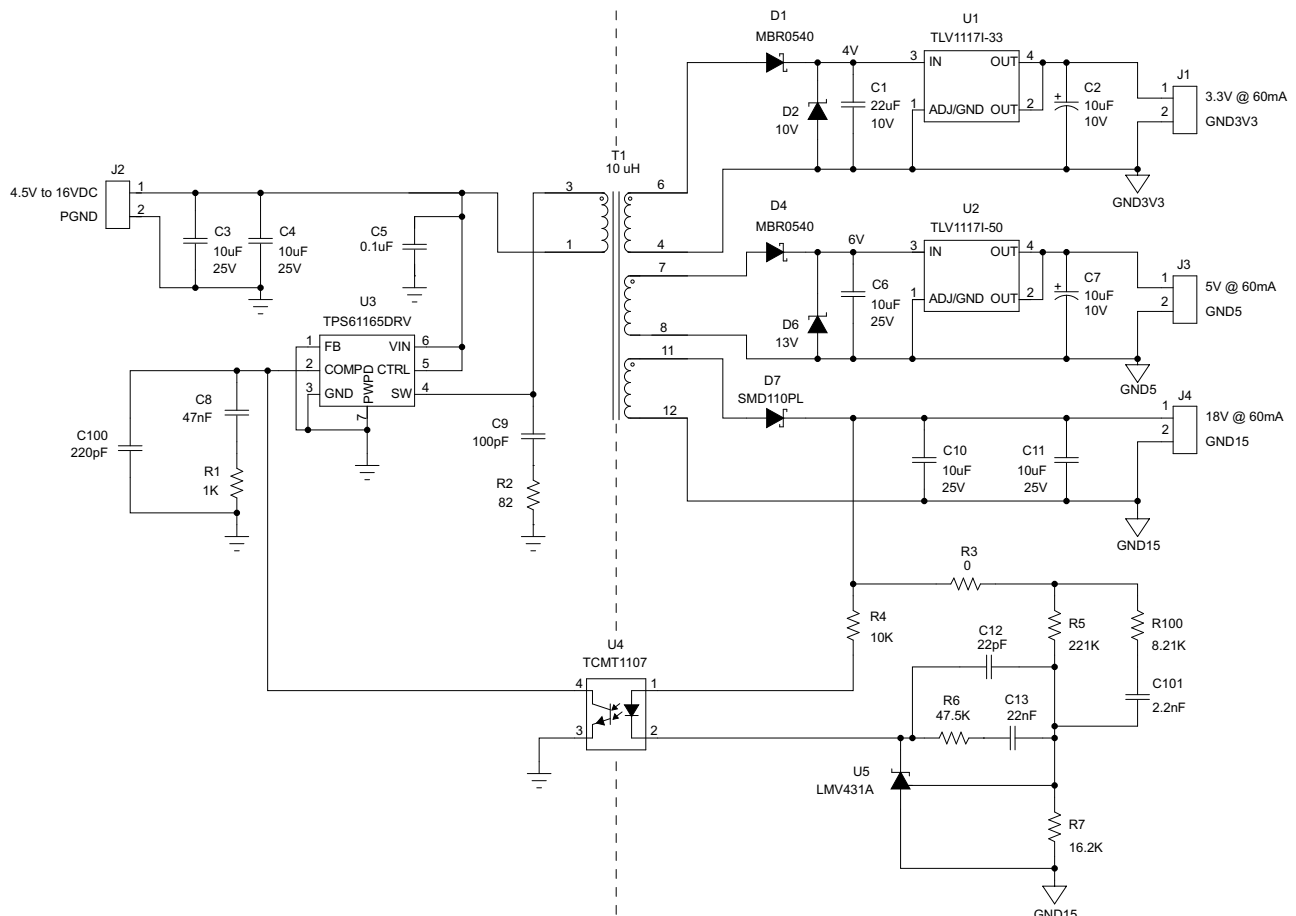


Figure 3. Complete Schematic of the Flyback Converter

Figure 4, Figure 5 and Figure 6 illustrate the output voltages during the startup phase, taken at full load and 4.5 Vin, the voltage on SW pin of U3, at full load and 16 Vin, as well as the transient response, measured when the load on 18 V has been switched between 6 mA and 60 mA and the input voltage kept at 4.5 V.

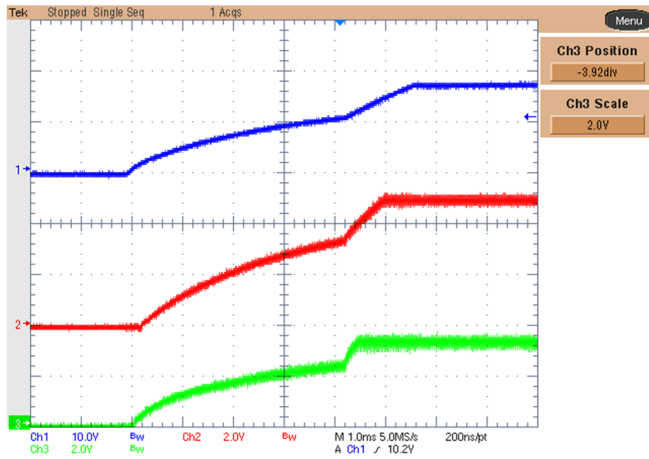


Figure 4. Output Voltages During the Startup Phase, Full Load, Vin = 4.5 V

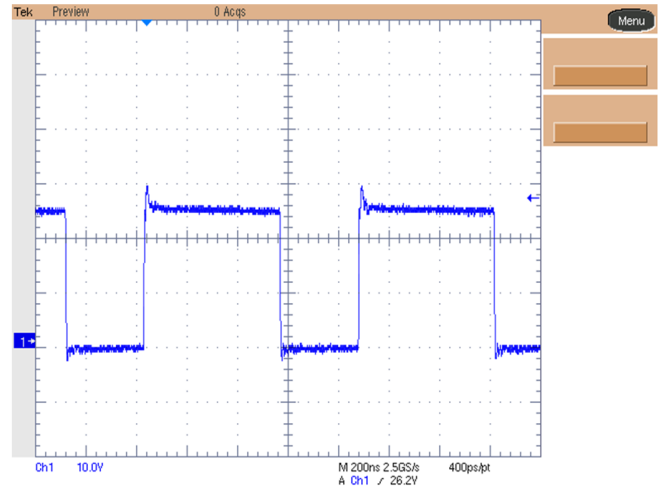


Figure 5. SW Pin Voltage, Full Load, Vin = 16 V

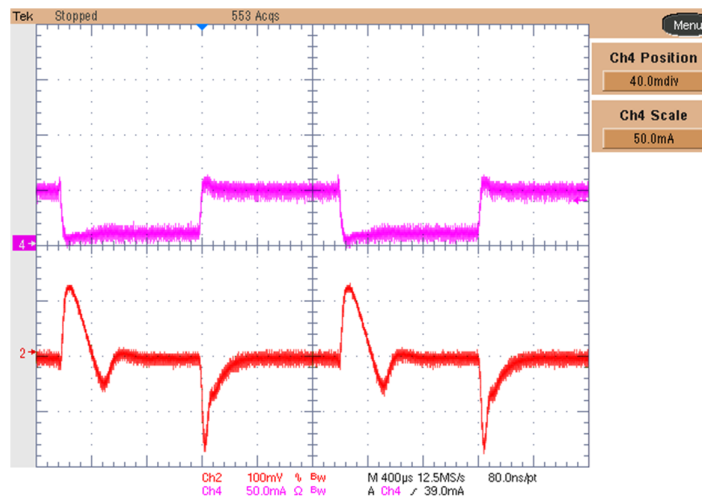


Figure 6. Transient Response, Load on 18 V Switched Between 6 mA and 60 mA, Vin = 4.5 V

Figure 7 shows the photo of the prototype.

The complete design detail including the schematic, test detail, and layout is available as PMP7223 design on the Power Lab TI page:

http://www.ti.com/lscds/ti/analog/powermanagement/reference_design.page?DCMP=pmp-reference-designs&HQS=powerlab-sig

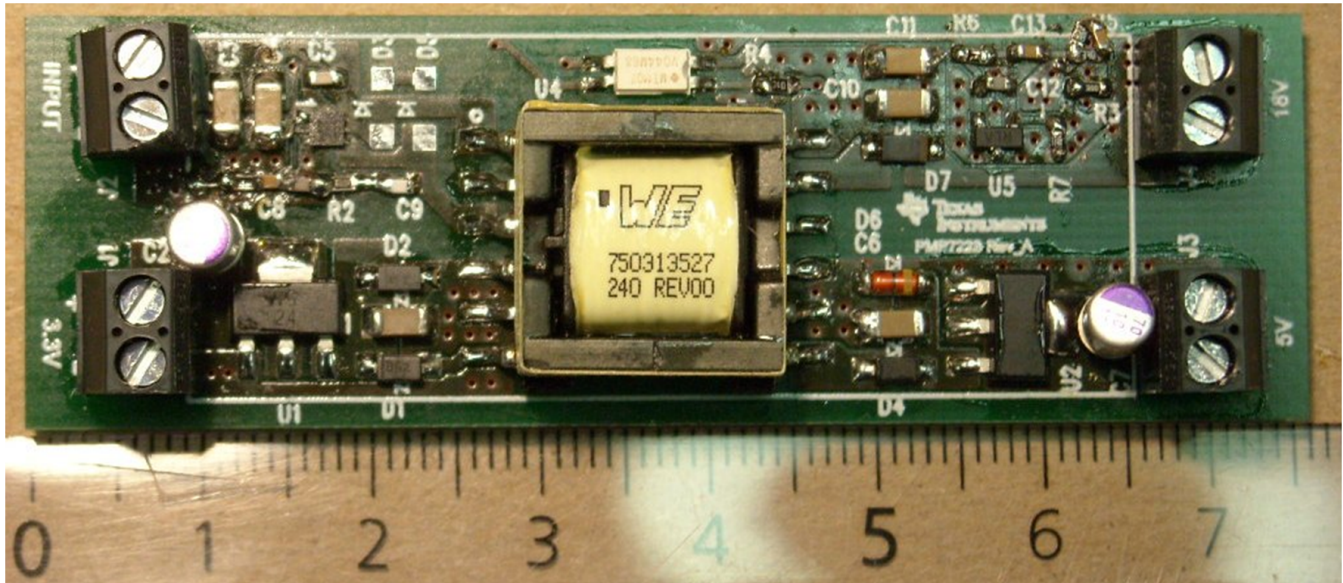


Figure 7. Photo of the Prototype

Conclusion

The entire approach to designing an integrated and low-cost power supply for 12-V based high frequency inverter was discussed step by step in this application note. The concept of using the boost converter, TPS61165 in this case, for the flyback application can be applied across any such design.

We would like to cover how power management solutions can be generated for a 24-V based inverter system. In this case, a standard buck converter with an isolated coupled winding taken from the output inductor is a good option. Low-cost devices such as LMR14206 or TPS5401 can be used for implementation, provided these controllers run in CCM mode and output load is constant. With unbalanced loads and under the condition when the load is concentrated mainly on the isolated output, they may lose regulation because of DCM operation. Using other controllers such as LM5017 that work in forced CCM mode can be other option. The main output from these DC-DC converters is used for powering the controller and AMC1100 primary while the Zener-regulated bias supply taken from the coupled winding can be used for powering AMC1100 secondary side.

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