User's Guide

TPS54233 Step-Down Converter Evaluation Module User's Guide

Table of Contents

List of Figures

List of Tables

Trademarks

SWIFT™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

1 Introduction

This user's guide contains background information for the TPS54233 as well as support documentation for the TPS54233EVM-373 evaluation module (HPA373). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54233EVM-373.

1.1 Background

The TPS54233 dc/dc converter is designed to provide up to a 2 A output from an input voltage source of 3.5 V to 28 V. Rated input voltage and output current range for the evaluation module are given in Table 1-1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS54233 regulator. The switching frequency is internally set at a nominal 300 kHz. The high-side MOSFET is incorporated inside the TPS54233 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFET allows the TPS54233 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54233 provides adjustable slow start and undervoltage lockout inputs. The absolute maximum input voltage is 30 V for the TPS54233EVM-373.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54233EVM-373	VIN = 8 V to 18 V	0 A to 2 A

1.2 Performance Specification Summary

A summary of the TPS54233EVM-373 performance specifications is provided in Table 1-2. Specifications are given for an input voltage of V_{IN} = 15 V and an output voltage of 3.3 V, unless otherwise specified. The TPS54233EVM-373 is designed and tested for V_{IN} = 7 V to 28 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 1-2. TPS54233EVM-373 and Performance Specification Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range			7	15	18	V
Output voltage set point				3.3		V
Output current range	V_{IN} = 8 V to 18 V		0		2	A
Line regulation	I_O = 1 A, V_{IN} = 8V to 18 V			±0.025%		
Load regulation	V_{IN} = 15 V, I_O = 0 A to 2 A			±0.03%		
Load transient response	I_O = 0.5 A to 1.5 A	Voltage change		–20		mV
		Recovery time		400		µs
	I_O = 1.5 A to 0.5 A	Voltage change		20		mV
		Recovery time		400		µs
Loop bandwidth	V_{IN} = 15 V, I_O = 1 A			9.0		kHz
Phase margin	V_{IN} = 15 V , I_O = 1 A			70		°
Input ripple voltage	I_O = 2 A			250		mVpp
Output ripple voltage	I_O = 2 A			70		mVpp
Output rise time				3.5		ms
Operating frequency				300		kHz
Maximum efficiency	TPS54233EVM-373, V_{IN} = 8 V, I_O = 0.4 A			91.2%		

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54233. Some modifications can be made to this module.

1.3.1 Output Voltage Set Point

To change the output voltage of the EVM, it is necessary to change the value of resistor R_6. Changing the value of R_6 can change the output voltage above 0.8 V. The value of R_6 for a specific output voltage can be calculated using Equation 1.

$$R_6 = 10.2\ k\Omega \times \frac{0.8\ V}{V_{Out} - 0.8\ V} \quad (1)$$

Table 1-3 lists the R_6 values for some common output voltages. Note that V_{IN} must be in a range so that the minimum on-time is greater than 160 ns, and the maximum duty cycle is less than 90%. The values given in Table 1-3 are standard values, not the exact value calculated using Equation 1.

Table 1-3. Output Voltages Available

Output Voltage (V)	R_6 Value (kΩ)
1.8	8.25
2.5	4.75
3.3	3.24
5	1.96

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54233EVM-373 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input / Output Connections

The TPS54233EVM-373 is provided with input/output connectors and test points as shown in Table 2-1. A power supply capable of supplying 2 A must be connected to J1 through a pair of 20 AWG wires. The load must be connected to J4 through a pair of 20 AWG wires. The maximum load current capability must be 2 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP5 is used to monitor the output voltage with TP6 as the ground reference.

Table 2-1. EVM Connectors and Test Points

Reference Designator	Function
J1	V_{IN} (see Table 1-1 for V_{IN} range)
J2	2-pin header for enable. Connect EN to ground to disable, open to enable.
J3	2-pin header for slow start monitor and GND.
J4	V_{OUT}, 3.3 V at 2 A maximum
TP1	V_{IN} test point at V_{IN} connector
TP2	GND test point at V_{IN}
TP3	PH test point
TP4	Test point between voltage divider network and output. Used for loop response measurements.
TP5	Output voltage test point at OUT connector
TP6	GND test point at OUT connector

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 0.5 A - 1 A and then decreases as the load current increases towards full load. Figure 2-1 shows the efficiency for the TPS54233EVM-373 at an ambient temperature of 25°C.

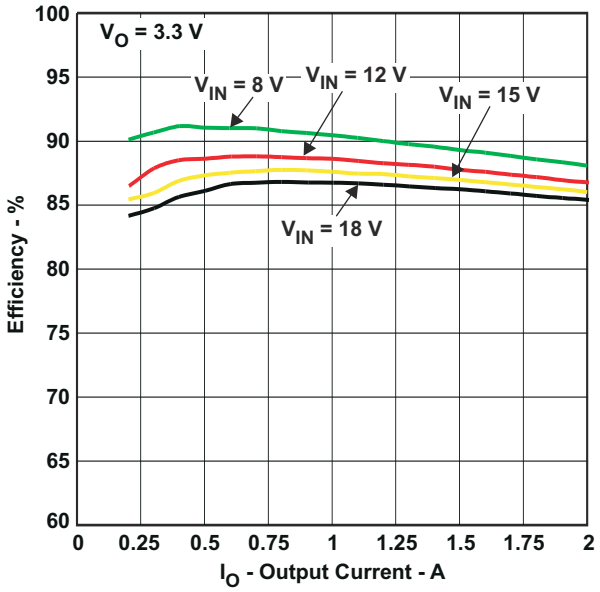

Figure 2-1. TPS54233EVM-373 Efficiency

Figure 2-2 shows the efficiency for the TPS54233EVM-373 at lower output currents between 0.01 A and 0.20 A at an ambient temperature of 25°C.

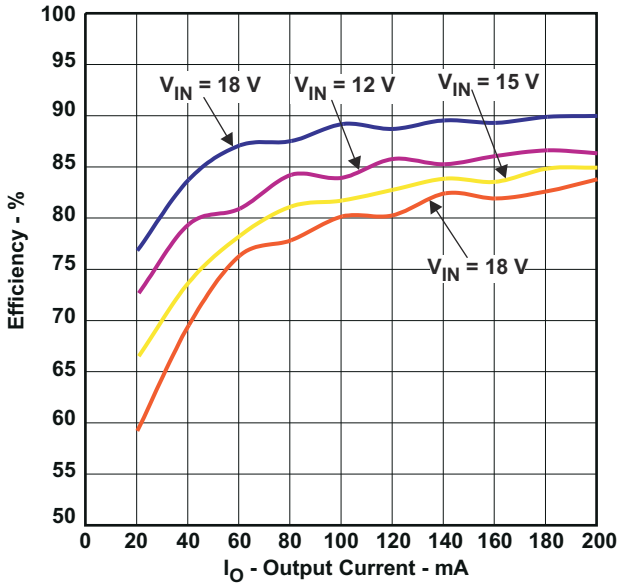

Figure 2-2. TPS54233EVM-373 Low Current Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Output Voltage Load Regulation

The load regulation for the TPS54233EVM-373 is shown in Figure 2-3.

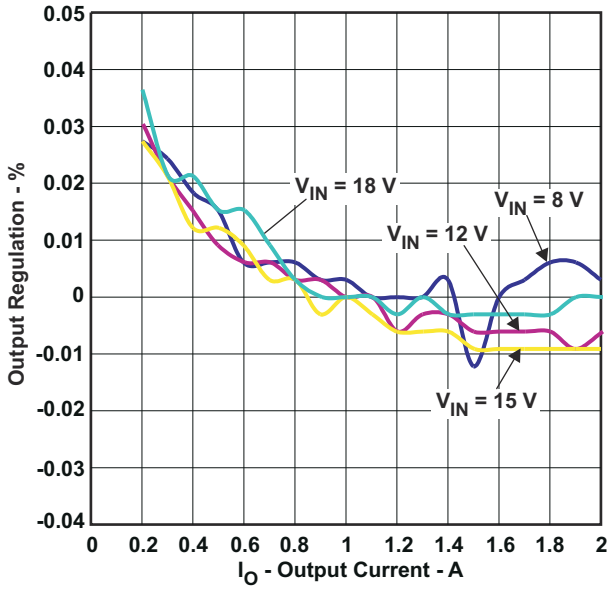

Figure 2-3. TPS54233EVM-373 Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

The line regulation for the TPS54233EVM-373 is shown in Figure 2-4.

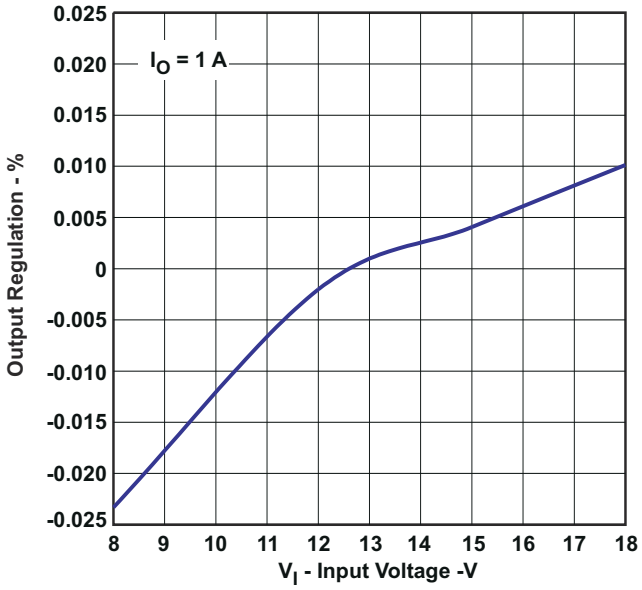

Figure 2-4. TPS54233EVM-373 Line Regulation

2.5 Load Transients

The TPS54233EVM-373 response to load transients is shown in Figure 2-5. The current step is from 25% to 75% of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

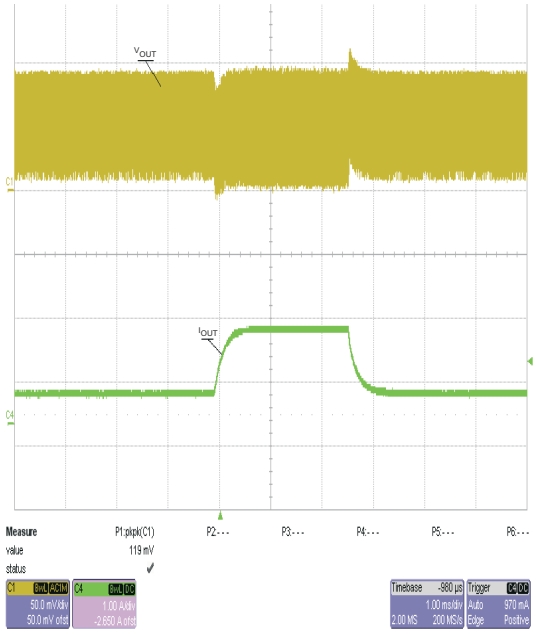

Figure 2-5. TPS54233EVM-373 Transient Response

2.6 Loop Characteristics

The TPS54233EVM-373 loop-response characteristics are shown in Figure 2-6. Gain and phase plots are shown for V_{IN} voltage of 15 V. Load current for the measurement is 1 A.

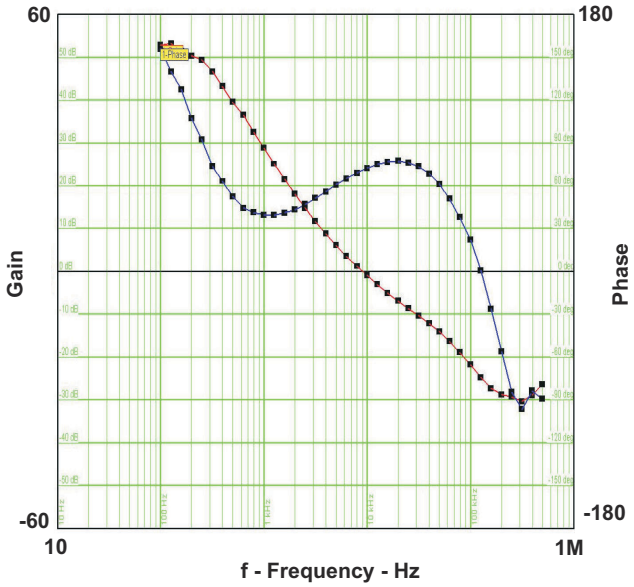

Figure 2-6. TPS54233EVM-373 Loop Response

2.7 Output Voltage Ripple

The TPS54233EVM-373 output voltage ripple is shown in Figure 2-7 . The output current is the rated full load of 2 A. Voltage is measured directly across the output capacitors.

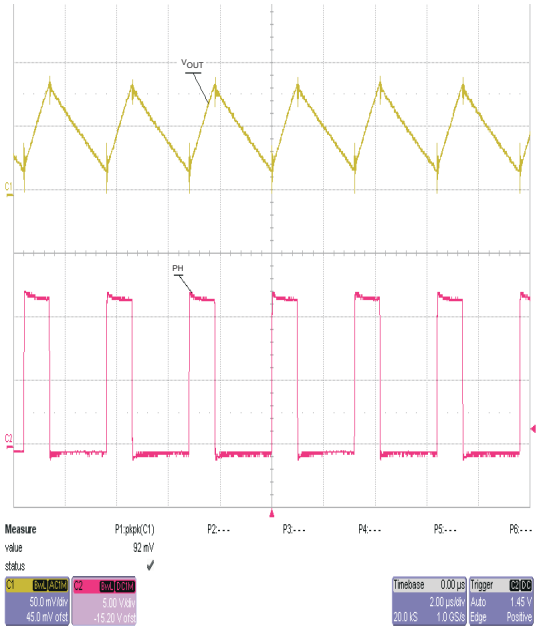

Figure 2-7. TPS54233EVM-373 Output Ripple

2.8 Input Voltage Ripple

The TPS54233EVM-373 input voltage ripple is shown in Figure 2-8 . The output current is the rated full load of 2 A. Voltage is measured directly across the input capacitors.

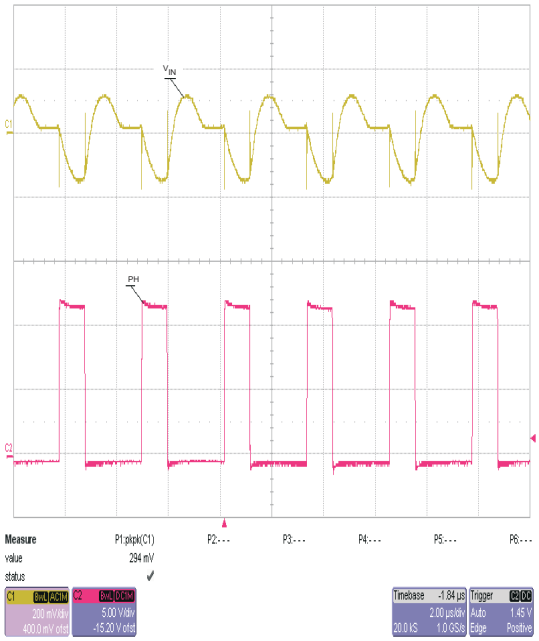

Figure 2-8. TPS54233EVM-373 Input Ripple

2.9 Powering Up

The start-up waveforms are shown in Figure 2-9 and Figure 2-10. In Figure 2-9, the top trace shows V_{IN}, and the bottom trace shows V_{OUT}. In Figure 2-10, the top trace shows EN (enable) whereas the bottom trace shows V_{OUT}. In Figure 2-10, the input voltage is initially applied and the output is inhibited by using a jumper at J2 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage of 1.25 V, the start-up sequence begins and the internal reference voltage begins to ramp up at the internally set rate toward 0.8 V and the output voltage ramps up to the externally set value of 3.3 V. The input voltage for these plots is 15 V and there is no load.

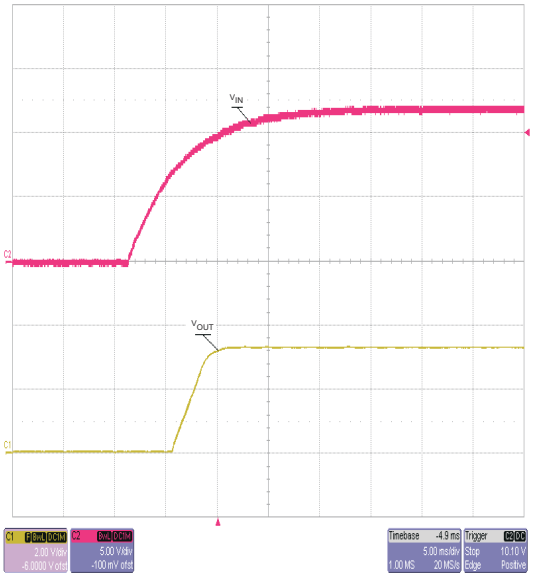

Figure 2-9. TPS54233EVM-373 Start-Up Relative to V_{IN}

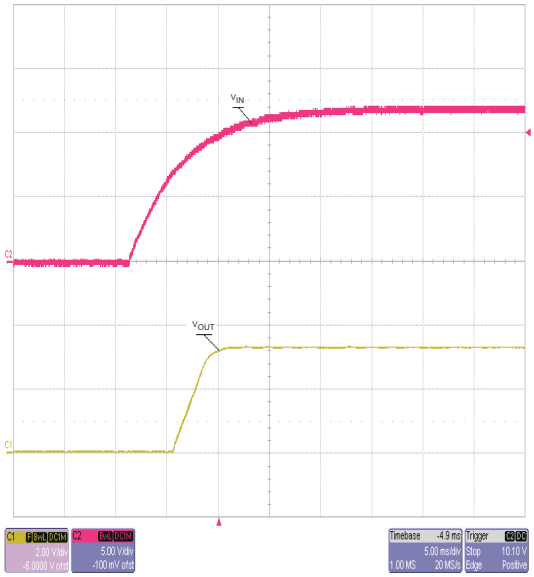

Figure 2-10. TPS54233EVM-373 Start-up Relative to Enable

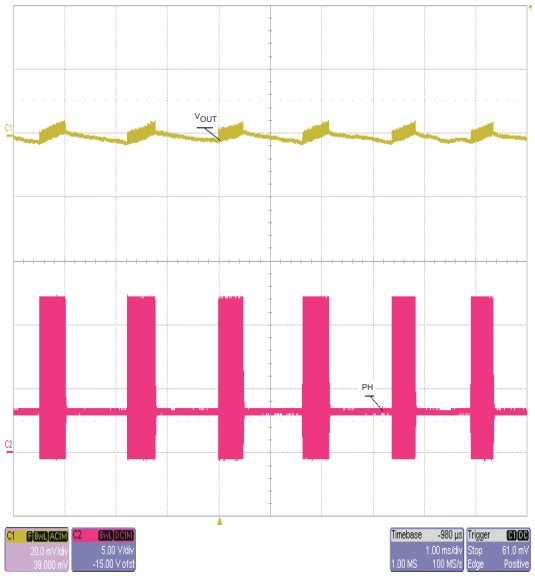

Figure 2-11. TPS54233EVM-373 Eco-Mode Operation

3 Board Layout

This section provides a description of the TPS54233EVM-373, board layout, and layer illustrations.

3.1 Layout

The board layout for the TPS54233EVM-373 is shown in Figure 3-1 through Figure 3-3. The topside layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz. copper.

The top layer contains the main power traces for V_{IN}, V_{OUT}, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54233 and a large area filled with ground. The bottom layer contains ground and a signal route for the BOOT capacitor. The top and bottom and internal ground traces are connected with multiple vias placed around the board including ten vias directly under the TPS54233 device to provide a thermal path from the top-side ground plane to the bottom-side ground plane.

The input decoupling capacitors (C1, C2, and C3) and bootstrap capacitor (C4) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace past the output capacitor C9. For the TPS54233, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply.

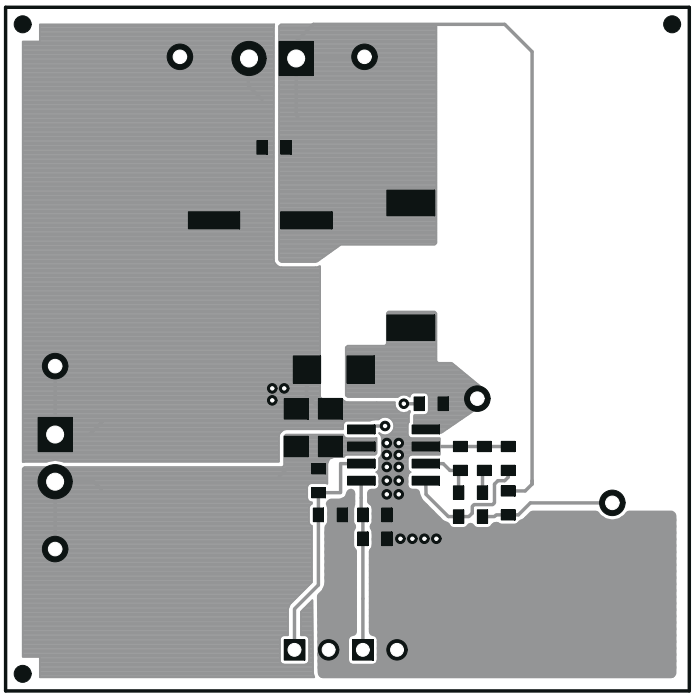

Figure 3-1. TPS54233EVM-373 Top-Side Layout

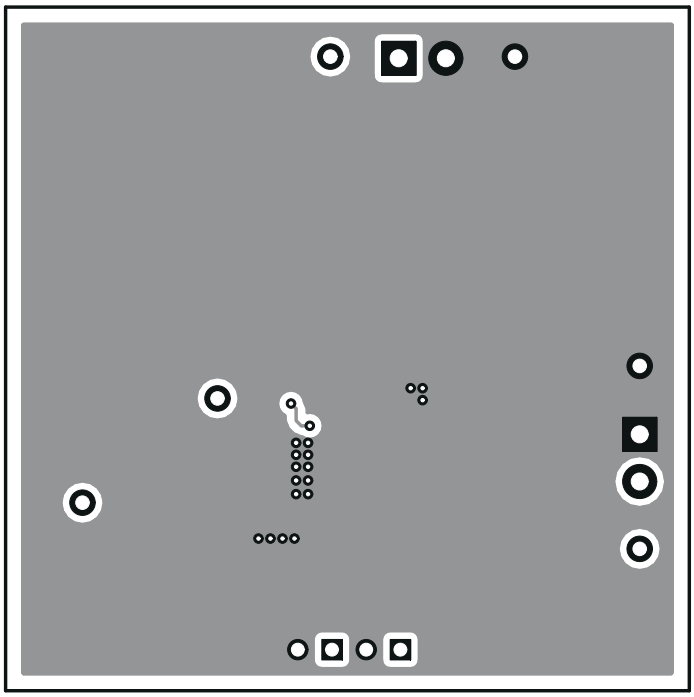

Figure 3-2. TPS54233EVM-373 Bottom-Side Layout

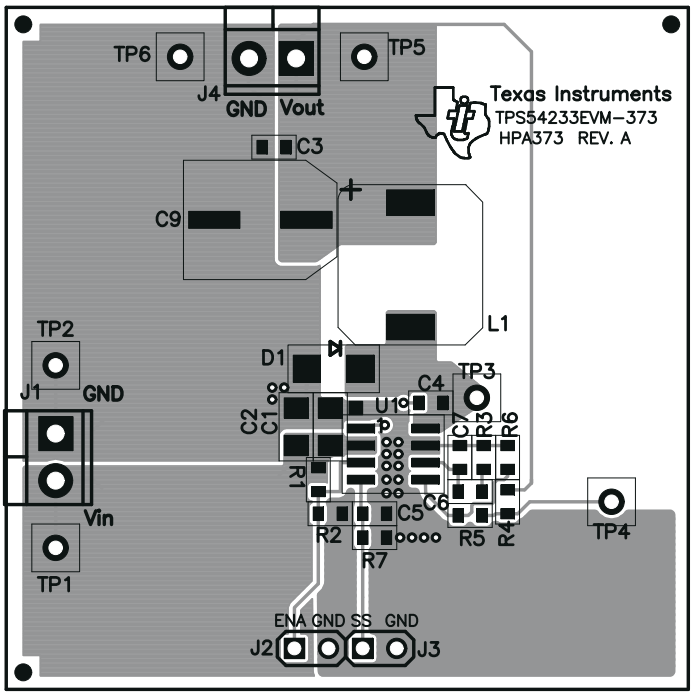

Figure 3-3. TPS54233EVM-373 Top-Side Assembly

3.2 Estimated Circuit Area

The estimated printed circuit board area for the components used in the design of this circuit is 0.72 in^2. This area does not include test points or connectors.

4 Schematic and Bill of Materials

This section presents the TPS54233EVM-373 schematic and bill of materials.

4.1 Schematic

Figure 4-1 is the schematic for the TPS54233EVM-373.

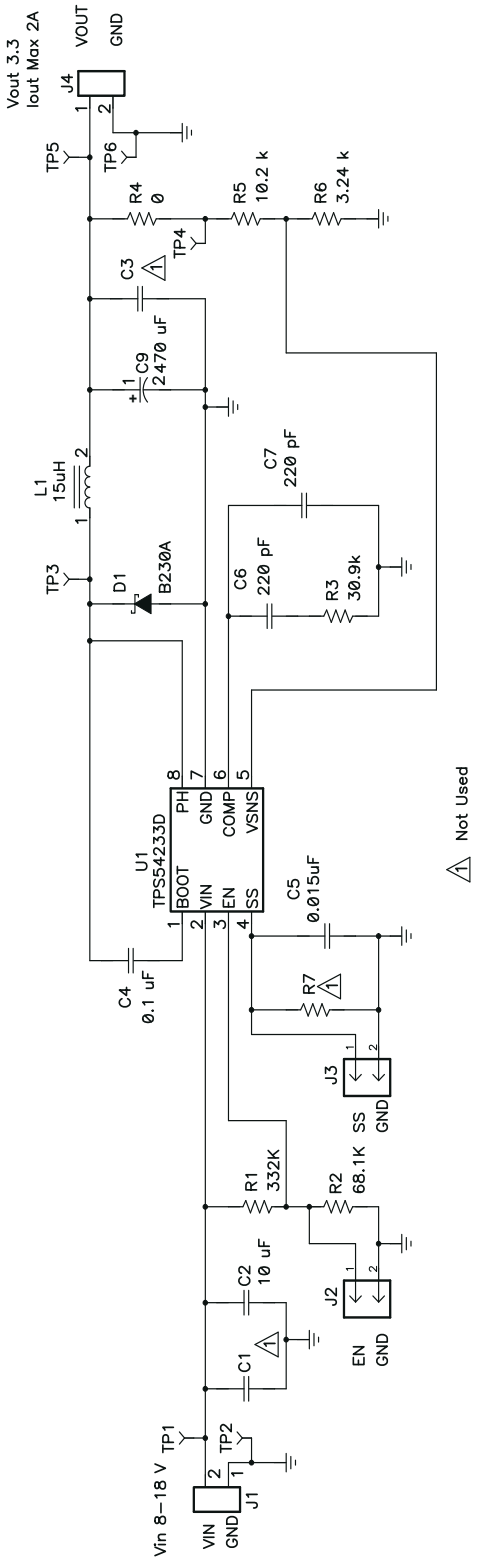

Figure 4-1. TPS54233EVM-373 Schematic

4.2 Bill of Materials

Table 4-1 presents the bill of materials for the TPS54233EVM-373.

Table 4-1. TPS54233EVM-373 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
0	C1	Open	Capacitor, Ceramic	1206		
1	C2	10 µF	Capacitor, Ceramic, 25V, X5R, 10%	1206	GRM31CR61E106KA12	muRata
0	C3	Open	Capacitor, Ceramic	0603		
1	C4	0.1 µF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
1	C5	0.015 µF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
2	C6, C7	220 pF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
1	C8	470 µF	Capacitor, Aluminum, 10V, ±20%	0.328 x 0.328 inch	EEVFK1A471P	Panasonic
1	D1	B230A	Diode, Schottky, 2A, 40V	SMA	B240A	Diodes Inc
2	J1, J4	ED1514	Terminal Block, 2-pin, 6-A, 3,5mm	0.27 × 0.25 inch	ED1514	OST
2	J2, J3	PTC36SAAN	Header, 2-pin, 100mil spacing, (36-pin strip)	0.100 × 2	PTC36SAAN	
1	L1	15 µH	Inductor, SMT, 3.7A, 41 mΩ	0.402 × 0.394 inch	MSS1038-273NL	Coilcraft
1	R1	332k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	68.1k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	30.9k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	10.2k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	3.24k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R7	Open	Resistor, Chip, 1/16W, 1%	0603	Std	Std
3	TP1, TP3, TP5	5000	Test Point, Red, Thru Hole Color Keyed	0.100 × 0.100 inch	5000	Keystone
3	TP2, TP4, TP6	5001	Test Point, Black, Thru Hole Color Keyed	0.100 × 0.100 inch	5001	Keystone
1	U1	TPS54233D	IC, DC-DC Converter, 28V, 2A	SO-8	TPS54233D	TI
1	—		PCB	2.0" x 2.0" x 0.062"	HPA373	Any
1	—		Shunt, 100-mil, Black	0.100	929950-00	3M

Note

1. These assemblies are ESD sensitive, ESD precautions shall be observed
2. These assemblies must be clean and free from flux and all contaminants. Use of unclean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2008) to Revision A (October 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
• Updated the user's guide title.	2

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025