User's Guide
SLVU352G–March 2010–Revised April 2019

UCD90xxx Sequencer and System Health Controller PMBus Command Reference

The UCD90xxx Power Supply Sequencer and Monitor supports a wide range of commands that allow an external host to configure, control, and monitor voltage rails and fans. Communication between the sequencer and the host is via an I^2C electrical interface using the PMBus™ command protocol.

The PMBus specification describes the command protocol in general terms. This document describes implementation details that are specific to the UCD90xxx Power Supply Sequencer and Monitor. If a command is not described in this document and it is supported by a UCD90xxx device (see Table 3), it functions exactly as described in the PMBus specification. In which case, refer to PMBus specification for more details.

See the device-specific data sheet for a complete description of the features.

This document makes reference to *Fusion*. The TI Fusion Digital Power Designer (SLVC223) is provided for device configuration. This Microsoft® Windows® based, graphical user interface (GUI) offers an intuitive interface for configuring, storing, and monitoring all system operating parameters.

Note: This document does not apply to the UCD9080 and UCD9081 devices.

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1 PMBus Specification

This document makes frequent mention of the PMBus specification, specifically, the *PMBus Power System Management Protocol Specification Part II – Command Language*, Revision 1.1, dated 5 February 2007 (UCD90240 is Revision 1.2 Compliant). The specification is published by the Power Management Bus Implementers Forum and is available from http://pmbus.org.

The types of status supported by the UCD90xxx are shown in Figure 1, Figure 3, Figure 5, and Figure 6. Whenever any of these bits are set, the PMBALERT# line is asserted. Unsupported types are denoted with grayed-out text.

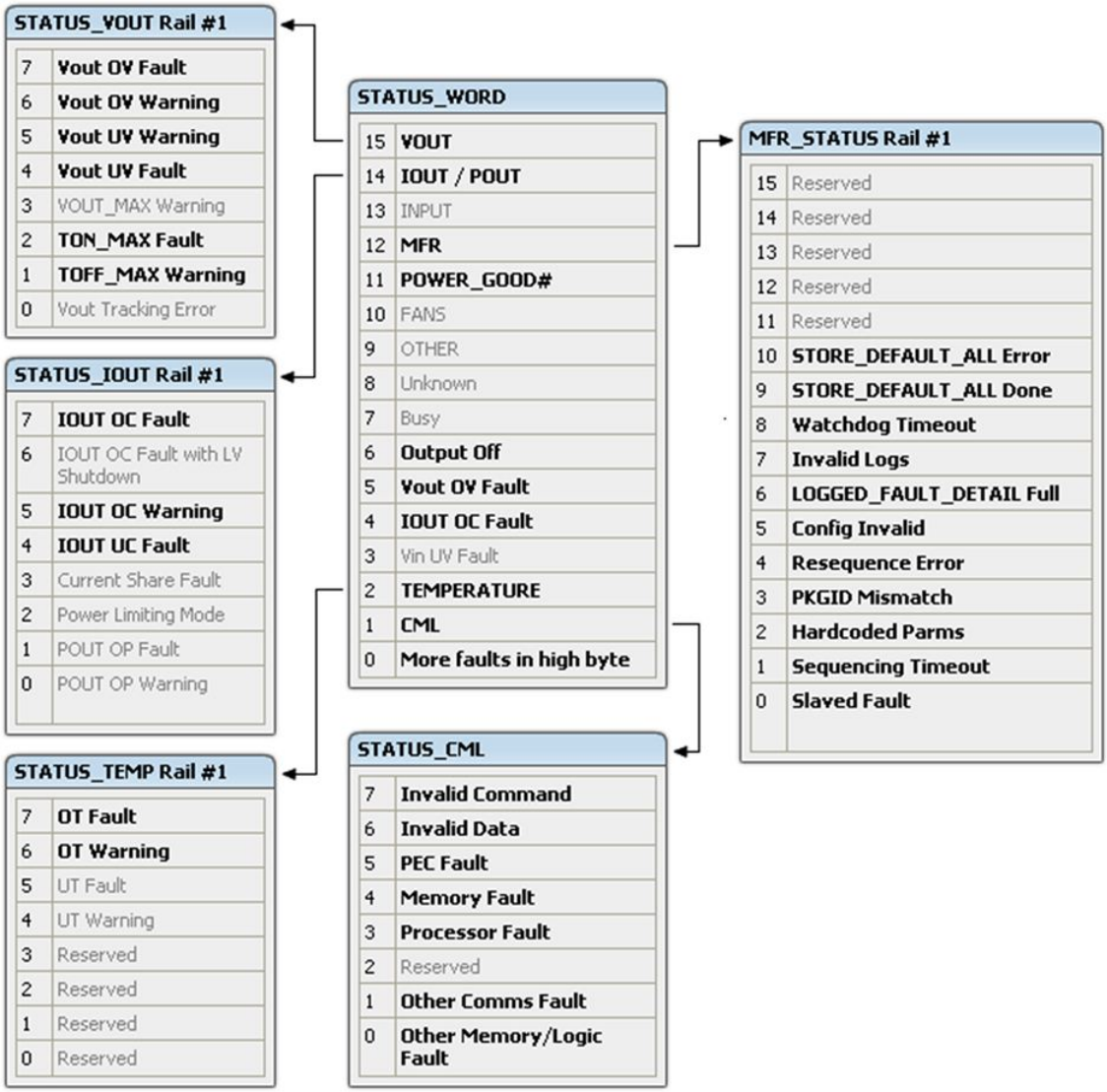


Figure 1. PMBus Status Supported by the UCD90120

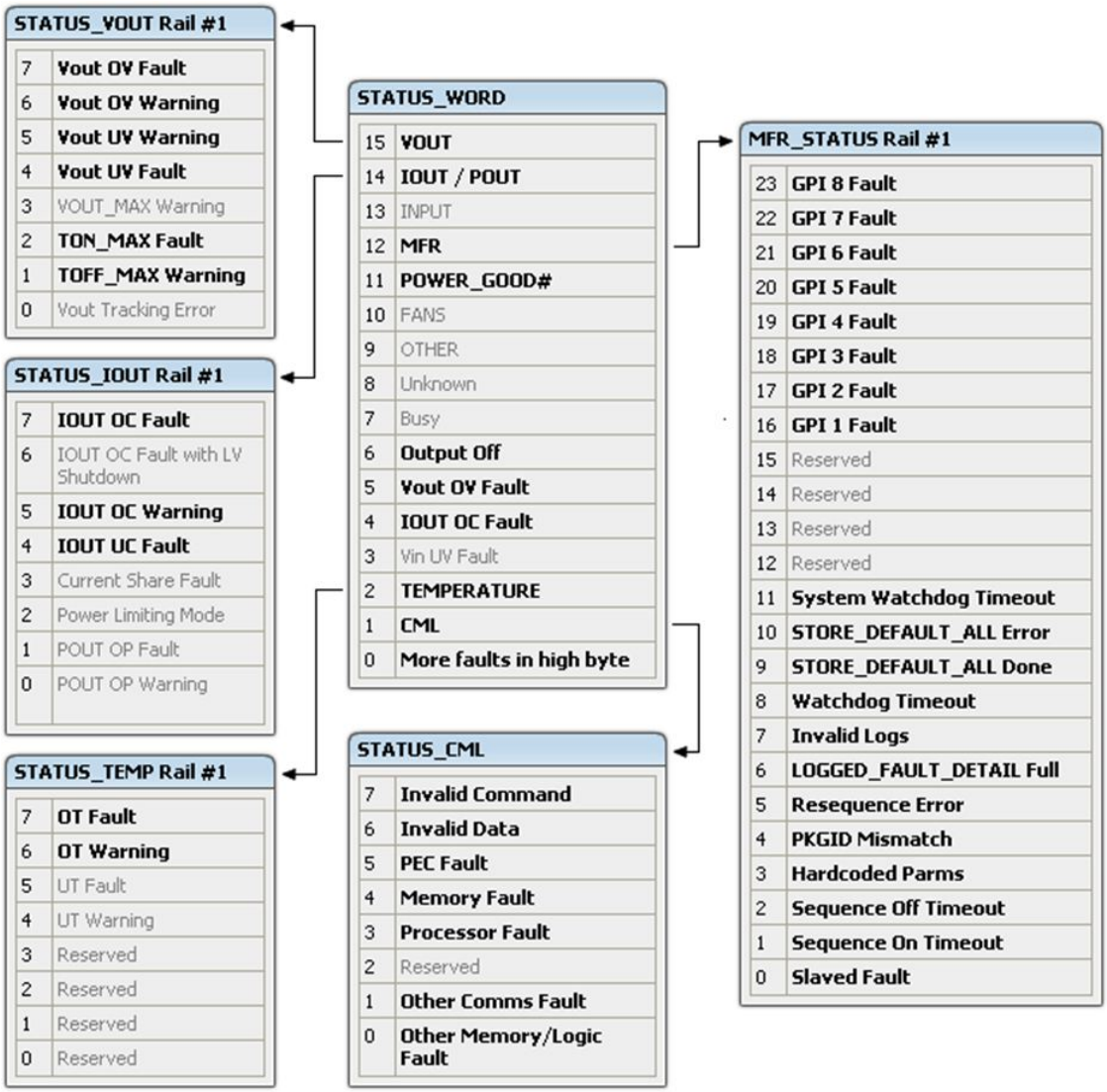


Figure 2. PMBus Status Supported by the UCD90120A, UCD9090, and UCD9090A

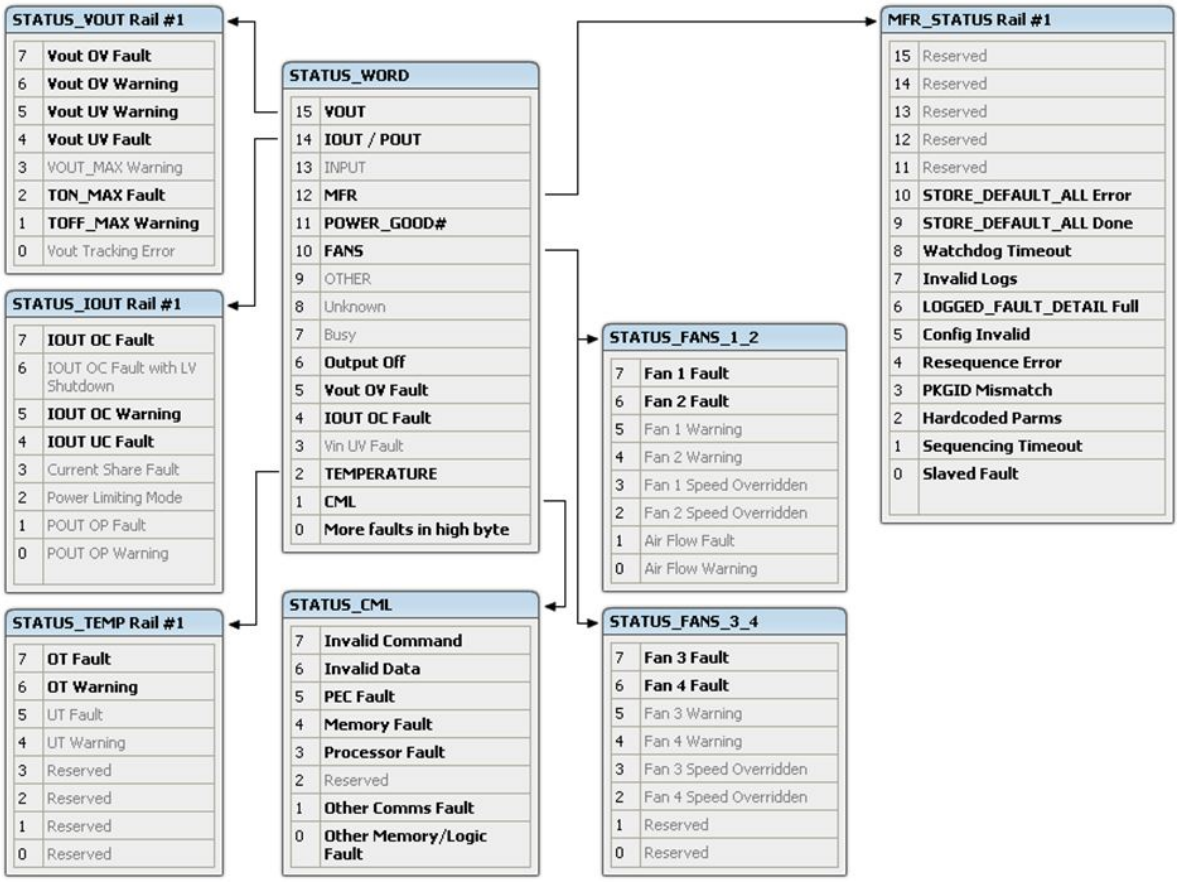


Figure 3. PMBus Status Supported by the UCD90124

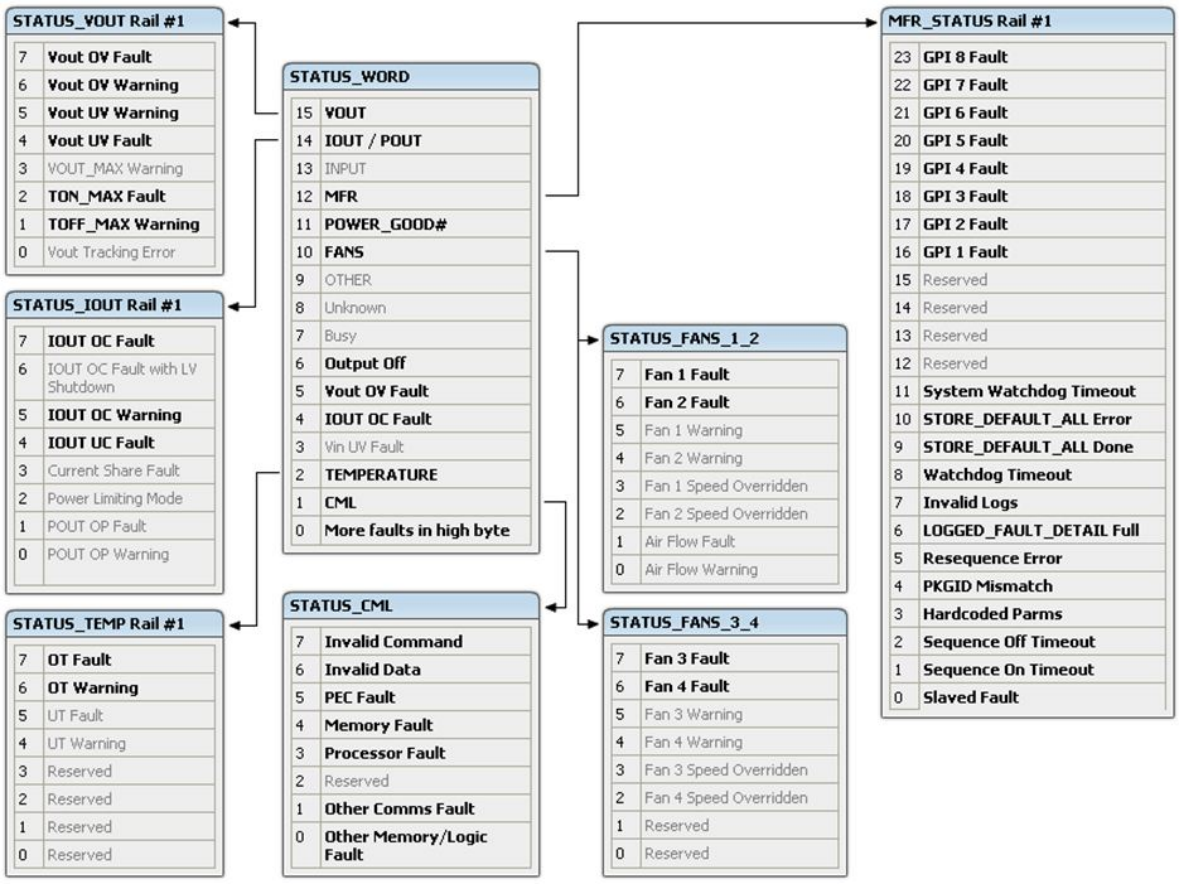


Figure 4. PMBus Status Supported by the UCD90124A

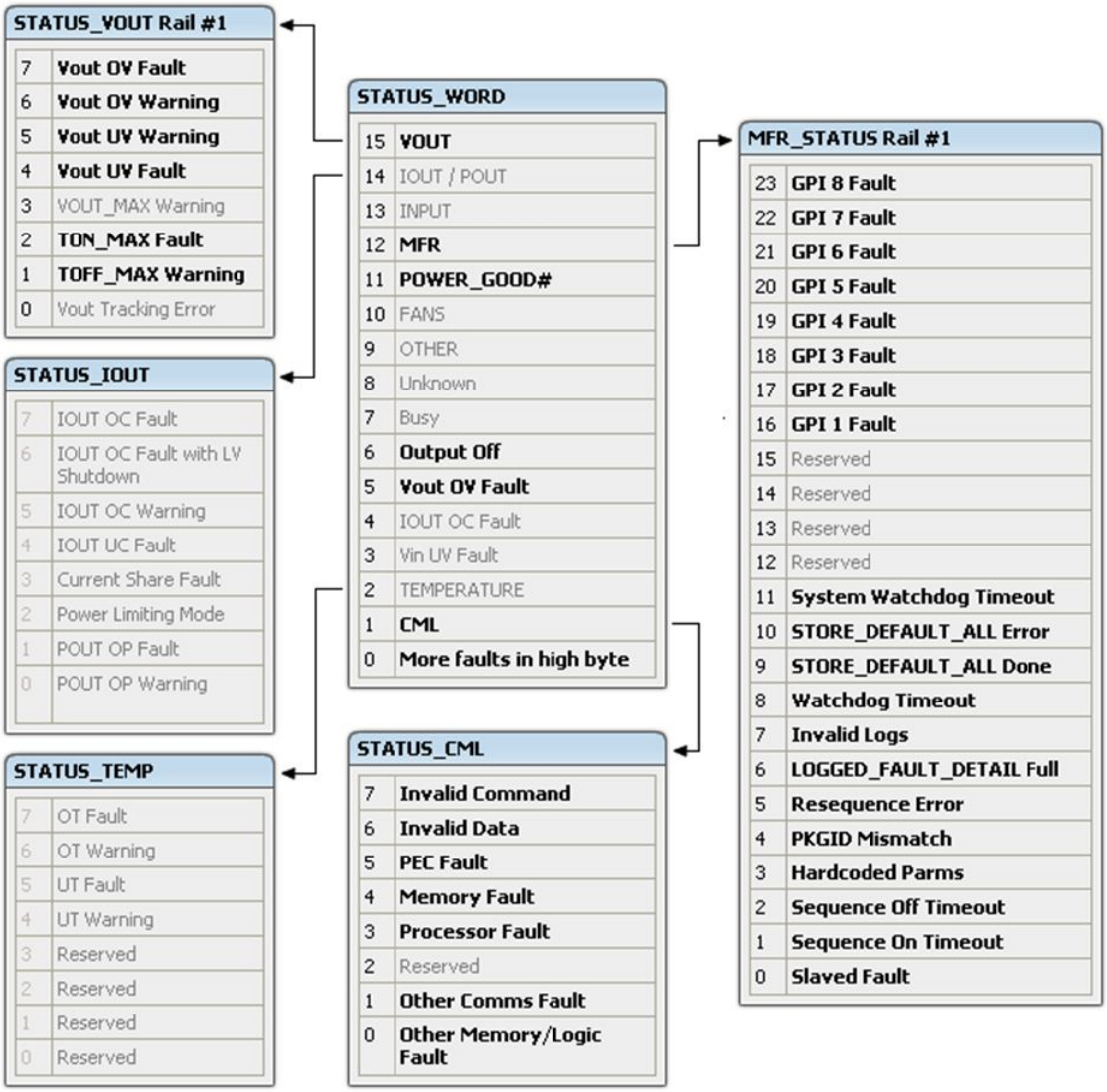


Figure 5. PMBus Status Supported by the UCD90160 and UCD90160A

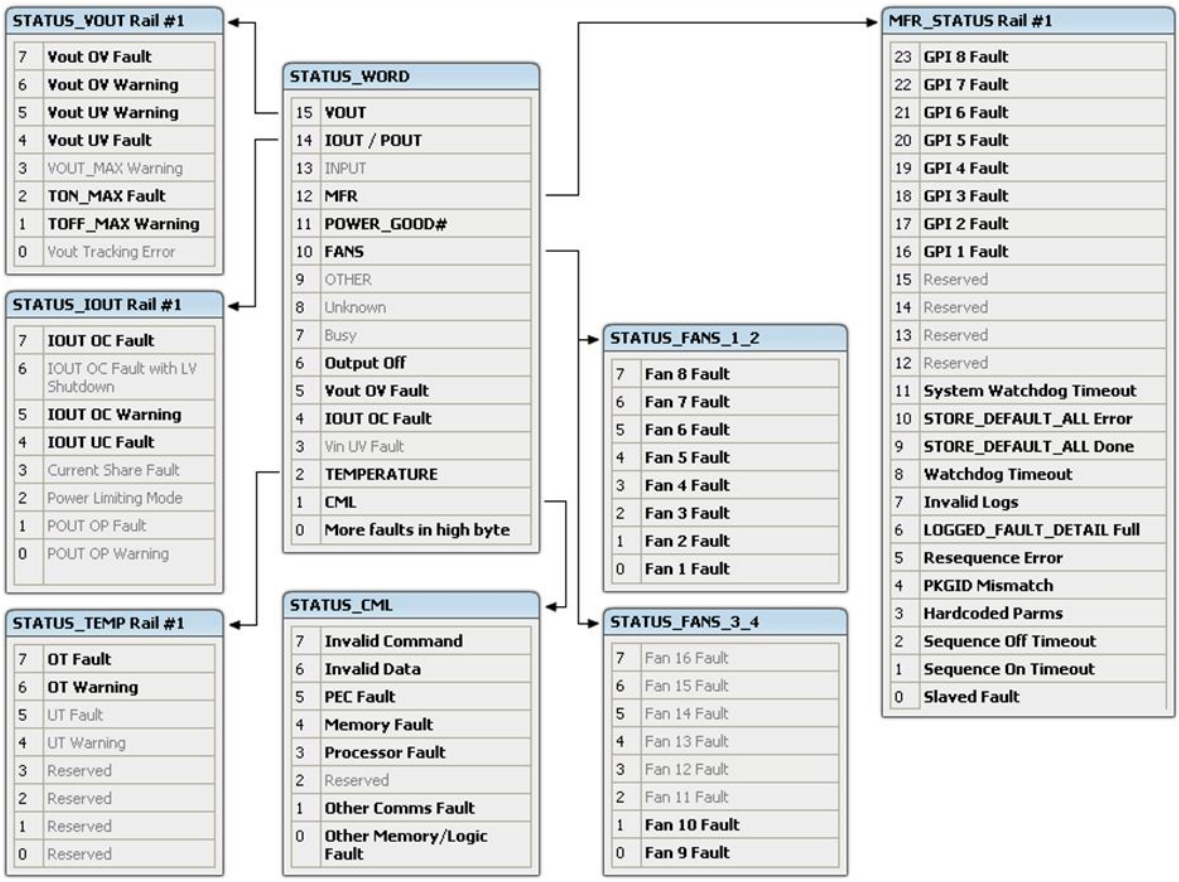


Figure 6. PMBus Status Supported by the UCD90910

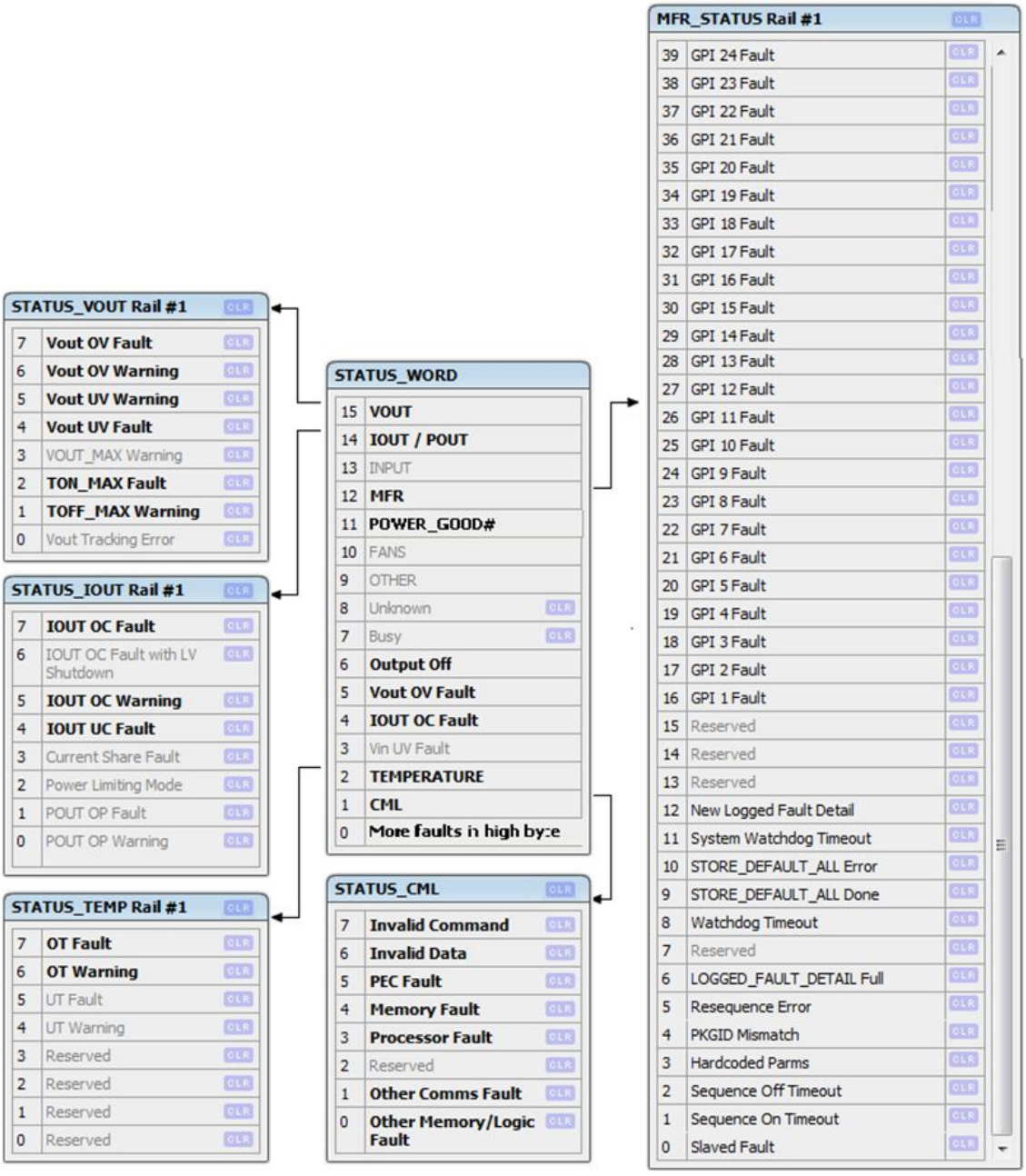


Figure 7. PMBus Status Supported by the UCD90240

1.1 Manufacturer Specific Status (STATUS_MFR_SPECIFIC)

The standard STATUS_MFR_SPECIFIC command does not have enough bits to implement UCD90xxx's functionalities. This command has been replaced by the MFR_STATUS command (see Section 10.35).

2 Data Formats

Sections 7 and 8 of the PMBus standard provides for five different data formats: three for parameters related to output voltage and two for all other commands. Each PMBus device is expected to support only one of these formats.

2.1 Data Format for Output Voltage Parameters

For parameters related to output voltage, the UCD90xxx supports the linear format defined in Section 8.3.1 of the PMBus specification. The linear format uses a 16-bit unsigned mantissa for each parameter, along with an exponent that is shared by all the voltage-related parameters. The exponent is reported in the bottom 5 bits of the VOUT_MODE parameter.

The voltage value is calculated using the equation

$$\text{Voltage} = V \times 2^{X} \quad (1)$$

Where:

Voltage is the parameter of interest, in volts,
V is a 16-bit unsigned binary integer mantissa, and
X is the signed 5-bit twos-complement binary integer exponent from VOUT_MODE.

Exception: The PMBus standard assumes that all output voltages are expressed as positive numbers; therefore, all parameters related to output voltage are unsigned integers, with a few notable exceptions. The VOUT_CAL_OFFSET, and VOUT_CAL_MONITOR values are intended for making fine adjustments to the output voltage and may take on small negative values. As such, these parameters are treated as signed twos-complement binary integers.

2.2 Data Format for Other Parameters

For parameters not directly related to output voltage, the UCD90xxx supports the linear data format described in section 7.1 of the PMBus specification. This linear format is a two-byte value that contains an 11-bit, twos-complement mantissa and a 5-bit, twos-complement exponent.

The relationship between the PMBus parameter and the real-world value is given by the formula:

$$R = Y \times 2^{X} \quad (2)$$

Where:

R is the real-world value,
Y is an 11-bit, signed twos-complement binary integer mantissa, and
X is the signed 5-bit, `twos-complement binary integer exponent.

This pseudo floating-point notation allows values as large as ≈33E6 down to ≈15E-6 to be sent over the PMBus. The internal variables used by the UCD90xxx firmware are mostly 16 bits wide and do not support such a wide range of values. The resolution of a PMBus setting depends strongly on both the exponent of the PMBus value (larger values have coarser resolution) and the scaling of the internal variables.

2.3 Distinguishing Between Linear Data Formats

The PMBus specification uses the same term, linear, to describe both the 16-bit+exponent format used for the voltage-related parameters as well as the 11-bit+exponent format used for other parameters. In cases where it is necessary to distinguish between these two data formats, this document uses the term LINEAR16 or LINEAR11.

2.4 Translation, Quantization, and Truncation

The internal variables used by the UCD90xxx are often scaled to take optimal advantage of the hardware's native units such as ADC or DAC counts rather than volts or amperes. As a result, values that are written and read via PMBus must undergo mathematical translations. These translations, with their inherent quantization, may result in very slight differences between the setting that was written to the UCD90xxx and the value that was later read back from it. This is normal and compliant, described in section 7.4 of the PMBus specification.

In some cases, a value written to the device may cause it to exceed the range of its internal variable. In some cases, the device reports this as an error; in other cases it saturates the variable at a safe value. In all cases, the value read back via the PMBus reflects as accurately as possible the internal variable actually being used by the UCD90xxx.

2.5 8-Bit Time Encoding

To save memory when precision is not needed, several commands will encode a time parameter in 8-bits. The 8 bits are separated into two fields. Bits 6 and 7 are the index for the multiplier field and bits 0 to 5 are the mantissa (0x00 to 0x3F). The two are multiplied together to derive the time. A mantissa of 0 will result in a time of 0 regardless of the multiplier value.

Table 1. 8-Bit Time Encoding

Multiplier Index	Multiplier (ms)	Resulting Range
b'00	1	0 to 63 ms
b'01	8	8 to 504 ms
b'10	64	64 ms to 4.032 s
b'11	512	512 ms to 32.256 s

2.6 16-Bit Time Encoding

The 16 bits are separated into two fields. Bits 14 and 15 are the index for the multiplier field and bits 0 to 13 are the mantissa (0x00 to 0x3FFF). The two are multiplied together to derive the time. A mantissa of 0 results in a time of 0, regardless of the Increment value.

Table 2. 16-Bit Time Encoding

Multiplier Index	Multiplier (ms)	Resulting Range
b'00	1	1 to 16384 ms
b'01	8	8 to 131.72 s
b'10	64	64 ms to 1048.576 s
b'11	512	512 ms to 8388.608 s

3 Memory Model

Section 6 of the PMBus specification describes the memory model for PMBus devices. Values used by the PMBus device are loaded into volatile Operating Memory from one or more of the following places:

- Values hard coded into an integrated circuit (IC) design (if any)
- Values programmed from hardware pins (if any)
- A nonvolatile memory called the Default Store
- A nonvolatile memory called the User Store (not supported by the UCD90xxx)
- Communications from PMBus

The UCD90xxx contains RAM that is used as Operating Memory. Embedded Data Flash memory is used to implement the hard-coded values and the Default Store values. Hard-coded values require a new firmware revision. Values in the Default Store may be changed using the STORE_DEFAULT_ALL command described in Section 6.3.

Section 6.1 of the PMBus specification describes the ordering of memory loading and precedence. In general, the hard-coded parameters are loaded into Operating Memory first. Second, any pin-programmable settings take effect. Third, values from the Default Store are loaded. Later, commands issued from the PMBus take effect. In all cases, an operation on a parameter overwrites any prior value that was already in the Operating Memory.

4 Alert Response Address Support

The UCD90xxx supports using the PMBALERT# line to notify the host of warning or fault conditions and also supports the Alert Response Address protocol with the following exception.

After UCD90xxx loses arbitration during an Alert Response Address event, it does not respond to its address on the PMBus or another Alert Response Address event. Sending any other PMBus command on PMBus will clears this state, including commands addressed to other devices. Then, UCD90xxx will respond to subsequent commands and Alert Response Address events normally.

UCD90240 has restriction on the Alert Response Address Support. The device does not support slave arbitration lost. Multiple PMBus devices including the UCD90240 can work on the same PMBus if all the PMBus addresses meet the following requirement: when performing binary AND operation to any two of the addresses on the bus, the result must always be the lowest address. Please refer to UCD90240 datasheet (SLVSCW0) and corresponding application notes for details.

5 Supported PMBus Commands

Table 3 lists the PMBus commands. Commands 00h through CFh are defined in the PMBus specification and are considered to be core commands that are standardized for all manufacturers and products. Commands D0h through FEh are manufacturer specific and may be unique for each manufacturer and product.

The device columns (UCD90120, and so forth) indicate if a command is supported by a given device. The command is supported if a check mark (√) appears in that column. Commands that are not supported by any device are grayed out.

Most commands support writing and reading. Exceptions are indicated in the Comments column.

The Data Format column indicates the format of the data:

Byte	8-bit binary value. See the PMBus specification for details for each command.
LINEAR16	16-bit linear format used for output voltage parameters. Described in Section 2.1.
LINEAR11	11-bit linear format used for parameters other than output voltage. Described in Section 2.2.
n/a	Command does not have a data field.
String	ASCII string. Described in Section 22.2 of the PMBus specification.
Byte Array	A block of data in binary format.

The Scope column indicates how each command is affected by the PAGE setting.

Common	This command does not depend on the PAGE setting. It is a common variable used by all pages.
PAGE	This command applies to the page(s) set by the most recent PAGE command. See Section 6.1 for details.

The Page column in Table 3 points to additional detail about the command. A number that is not in parenthesis corresponds to the page in the *PMBus Power System Management Protocol Specification Part II – Command Language*, Revision 1.1, dated 5 February 2007. The number in parenthesis is the page number in this document.

The Data Flash column indicates if the parameter is stored in the Default Store in Data Flash. If an x appears in that column, it is not stored. See Section 6.3 for more information.

Most commands are used for device configuration which is often only done once with the assistance of the TI provided GUI (Fusion). In normal operation, only a subset of the commands are used frequently. Those commands are highlighted in **bold** font.

Table 3. PMBus Commands

Code (hex)	Command	Transaction Type	Data Format [Units]	Scope	UCD90120	UCD90124	UCD9090/A	UCD90910	UCD90160/A	UCD90120A	UCD90124A	UCD90240	Data Flash	Comments
00	PAGE	R/W Byte	Byte	Common	√	√	√	√	√	√	√	√	X	
01	OPERATION	R/W Byte	Byte	PAGE	√	√	√	√	√	√	√	√	X	
02	ON_OFF_CONFIG	R/W Byte	Byte	PAGE	√	√	√	√	√	√	√	√		
03	CLEAR_FAULTS	Send Byte	n/a	Common	√	√	√	√	√	√	√	√		Write Only
04	PHASE													
05-0F	Reserved													
10	WRITE_PROTECT													
11	STORE_DEFAULT_ALL	Send Byte	n/a	Common	√	√	√	√	√	√	√	√		Write Only(1)
12	RESTORE_DEFAULT_ALL	Send Byte	n/a	Common	√	√						√		Write Only
13	STORE_DEFAULT_CODE													
14	RESTORE_DEFAULT_CODE													
15	STORE_USER_ALL													
16	RESTORE_USER_ALL													
17	STORE_USER_CODE													
18	RESTORE_USER_CODE													
19	CAPABILITY	Read Byte	Byte	Common	√	√	√	√	√	√	√	√		Read Only
1A	QUERY													
1B-1F	Reserved													
20	VOUT_MODE	R/W Byte	Byte	PAGE	√	√	√	√	√	√	√			The mode is fixed at 000 (Linear Mode), but the exponent may be modified. See Section 2.1 and Section 6.5 for details.
21	VOUT_COMMAND	R/W Word	LINEAR16 [V]	PAGE	√	√	√	√	√	√	√	√		
22	VOUT_TRIM													√
23	VOUT_CAL_OFFSET													
24	VOUT_MAX													
25	VOUT_MARGIN_HIGH	R/W Word	LINEAR16 [V]	PAGE	√	√	√	√	√	√	√			
26	VOUT_MARGIN_LOW	R/W Word	LINEAR16 [V]	PAGE	√	√	√	√	√	√	√	√		
27	VOUT_TRANSITION_RATE											√		
28	VOUT_DROOP													
29	VOUT_SCALE_LOOP													
2A	VOUT_SCALE_MONITOR	R/W Word	LINEAR11 [V/V]	PAGE	√	√	√	√	√	√	√			
2B-2F	Reserved											√		

(1) There is a chance that a write to this command will receive a NACK. Once the firmware starts a periodic or commanded update of data flash, it may take up to 100 ms to complete. During that time, writes to these commands will receive a NACK. If this occurs, wait 100 ms and retry the command. This note only applies if the brownout feature is not enabled (see brownout enable mode in MISC_CONFIG).

Table 3. PMBus Commands (continued)

Code (hex)	Command	Transaction Type	Data Format [Units]	Scope	UCD90120	UCD90124	UCD9090/A	UCD90910	UCD90160/A	UCD90120A	UCD90124A	UCD90240	Data Flash	Comments
30	COEFFICIENTS													
31	POUT_MAX													
32	MAX_DUTY													
33	FREQUENCY_SWITCH													
34	Reserved													
35	VIN_ON													
36	VIN_OFF													
37	INTERLEAVE													
38	IOUT_CAL_GAIN	R/W Word	LINEAR11 [mV/A = mΩ]	PAGE	√	√	√	√		√	√			Current Sense Gain
39	IOUT_CAL_OFFSET	R/W Word	LINEAR11 [A]	PAGE	√	√	√	√		√	√	√		
3A	FAN_CONFIG_1_2											√		See FAN_CONFIG command, E8h
3B	FAN_COMMAND_1	R/W Word	LINEAR11 [%]	Common		√		√			√		X	% Duty cycle (0-100%) RPM Command mode
3C	FAN_COMMAND_2	R/W Word	LINEAR11 [%]	Common		√		√			√		X	See FAN_COMMAND_1
3D	FAN_CONFIG_3_4													See FAN_CONFIG command, E8h
3E	FAN_COMMAND_3	R/W Word	LINEAR11 [%]	Common		√		√			√		X	See FAN_COMMAND_1
3F	FAN_COMMAND_4	R/W Word	LINEAR11 [%]	Common		√		√			√		X	See FAN_COMMAND_1
40	VOUT_OV_FAULT_LIMIT	R/W Word	LINEAR16 [V]	PAGE	√	√	√	√	√	√	√			
41	VOUT_OV_FAULT_RESPONSE	R/W Byte	Byte	PAGE								√		See FAULT_RESPONSES command
42	VOUT_OV_WARN_LIMIT	R/W Word	LINEAR16 [V]	PAGE	√	√	√	√	√	√	√			
43	VOUT_UV_WARN_LIMIT		R/W Word	LINEAR16 [V]	61	√	√	√	√	√	√	√	√	
44	VOUT_UV_FAULT_LIMIT		R/W Word	LINEAR16 [V]	62	√	√	√	√	√	√	√	√	
45	VOUT_UV_FAULT_RESPONSE	R/W Byte	Byte	PAGE								√		See FAULT_RESPONSES command
46	IOUT_OC_FAULT_LIMIT	R/W Word	LINEAR11 [A]	PAGE	√	√	√	√		√	√			
[(2)]47	IOUT_OC_FAULT_RESPONSE	R/W Byte	Byte	PAGE								√		See FAULT_RESPONSES command
48	IOUT_OC_LV_FAULT_LIMIT													
49	IOUT_OC_LV_FAULT_RESPONSE													
4A	IOUT_OC_WARN_LIMIT	R/W Word	LINEAR11 [A]	PAGE	√	√	√	√		√	√			[(2)]
4B	IOUT_UC_FAULT_LIMIT	R/W Word	LINEAR11 [A]	PAGE	√	√	√	√		√	√	√		[(2)]

(2) These values are only applied when associated voltage is in regulation. If there is not an associated voltage monitor, these values are applied after the rail is enabled and after TON_DELAY.

Table 3. PMBus Commands (continued)

Code (hex)	Command	Transaction Type	Data Format [Units]	Scope	UCD90120	UCD90124	UCD9090/A	UCD90910	UCD90160/A	UCD90120A	UCD90124A	UCD90240	Data Flash	Comments
4C	IOUT_UC_FAULT_RESPONSE	R/W Byte	Byte	PAGE								√		See FAULT_RESPONSES command
4D	Reserved													
4E	Reserved													
4F	OT_FAULT_LIMIT	R/W Word	LINEAR11 [°C]	PAGE	√	√	√	√		√	√			
50	OT_FAULT_RESPONSE	R/W Byte	Byte	PAGE								√		See FAULT_RESPONSES command
51	OT_WARN_LIMIT		R/W Word	LINEAR11 [°C]	64	√	√	√	√		√	√		
52	UT_WARN_LIMIT												√	
53	UT_FAULT_LIMIT													
54	UT_FAULT_RESPONSE													
55	VIN_OV_FAULT_LIMIT													
56	VIN_OV_FAULT_RESPONSE													
57	VIN_OV_WARN_LIMIT													
58	VIN_UV_WARN_LIMIT													
59	VIN_UV_FAULT_LIMIT													
5A	VIN_UV_FAULT_RESPONSE													
5B	IIN_OC_FAULT_LIMIT													
5C	IIN_OC_FAULT_RESPONSE													
5D	IIN_OC_WARN_LIMIT													
5E	POWER_GOOD_ON	R/W Word	LINEAR16 [V]	PAGE	√	√	√	√	√	√	√			
5F	POWER_GOOD_OFF	R/W Word	LINEAR16 [V]	PAGE	√	√	√	√	√	√	√	√		
60	TON_DELAY	R/W Word	LINEAR11 [ms]	PAGE	√	√	√	√	√	√	√	√		This does not apply to retries
61	TON_RISE											√		
62	TON_MAX_FAULT_LIMIT	R/W Word	LINEAR11 [ms]	PAGE	√	√	√	√	√	√	√			Maximum time to reach POWER_GOOD_ON
63	TON_MAX_FAULT_RESPONSE	R/W Byte	Byte	PAGE								√		See FAULT_RESPONSES command
64	TOFF_DELAY	R/W Word	LINEAR11 [ms]	PAGE	√	√	√	√	√	√	√			
65	TOFF_FALL											√		
66	TOFF_MAX_WARN_LIMIT	R/W Word	LINEAR11 [ms]	PAGE	√	√	√	√	√	√	√			
67	Reserved											√		
68	POUT_OP_FAULT_LIMIT													
69	POUT_OP_FAULT_RESPONSE													
6A	POUT_OP_WARN_LIMIT													

Table 3. PMBus Commands (continued)

Code (hex)	Command	Transaction Type	Data Format [Units]	Scope	UCD90120	UCD90124	UCD9090/A	UCD90910	UCD90160/A	UCD90120A	UCD90124A	UCD90240	Data Flash	Comments
6B	PIN_OP_WARN_LIMIT													
6C-77	Reserved													
78	STATUS_BYTE	Read Byte	Byte	Common	√	√	√	√	√	√	√		X	Read Only
79	STATUS_WORD	Read Word	Word	Common	√	√	√	√	√	√	√	√	X	Read Only
7A	STATUS_VOUT	Read Byte	Byte	PAGE	√	√	√	√	√	√	√	√	X	Read Only
7B	STATUS_IOUT	Read Byte	Byte	PAGE	√	√	√	√		√	√	√	X	Read Only
7C	STATUS_INPUT											√		
7D	STATUS_TEMPERATURE	Read Byte	Byte	PAGE	√	√	√	√		√	√		X	Read Only
7E	STATUS_CML	Read Byte	Byte	Common	√	√	√	√	√	√	√	√	X	Read Only
7F	STATUS_OTHER											√		
80	STATUS_MFR_SPECIFIC													See MFR_STATUS on page 79
81	STATUS_FANS_1_2	Read Byte	Byte	Common		√		√			√		X	Read Only
82	STATUS_FANS_3_4	Read Byte	Byte	Common		√		√			√		X	Read Only
83-87	Reserved													
88	READ_VIN													
89	READ_IIN													
8A	READ_VCAP													
8B	READ_VOUT	Read Word	LINEAR16 [V]	PAGE	√	√	√	√	√	√	√		X	Read Only
8C	READ_IOUT	Read Word	LINEAR11 [A]	PAGE	√	√	√	√		√	√	√	X	Read Only
8D	READ_TEMPERATURE_1	Read Word	LINEAR11 [°C]	Common	√	√	√	√		√	√	√	X	Read Only
8E	READ_TEMPERATURE_2	R/W Word	LINEAR11 [°C]	PAGE	√	√	√	√		√	√	√	X	UCD90120 and UCD90124: Read Only
8F	READ_TEMPERATURE_3											√		
90	READ_FAN_SPEED_1	Read Word	LINEAR11 [RPM]	Common		√		√			√		X	Read Only (Only valid when the fan is enabled.)
91	READ_FAN_SPEED_2	Read Word	LINEAR11 [RPM]	Common		√		√			√		X	Read Only (Only valid when the fan is enabled.)
92	READ_FAN_SPEED_3	Read Word	LINEAR11 [RPM]	Common		√		√			√		X	Read Only (Only valid when the fan is enabled.)
93	READ_FAN_SPEED_4	Read Word	LINEAR11 [RPM]	Common		√		√			√		X	Read Only (Only valid when the fan is enabled.)
94	READ_DUTY_CYCLE													
95	READ_FREQUENCY													
96	READ_POUT													
97	READ_PIN													

Table 3. PMBus Commands (continued)

Code (hex)	Command	Transaction Type	Data Format [Units]	Scope	UCD90120	UCD90124	UCD9090/A	UCD90910	UCD90160/A	UCD90120A	UCD90124A	UCD90240	Data Flash	Comments
98	PMBUS_REVISION	Read Byte	Byte	Common	√	√	√	√	√	√	√			Read Only
99	MFR_ID	R/W Block (18 bytes)	String	Common	√	√	√	√	√	√	√	√		
9A	MFR_MODEL	R/W Block (12 bytes)	String	Common	√	√	√	√	√	√	√	√		
9B	MFR_REVISION	R/W Block (12 bytes)	String	Common	√	√	√	√	√	√	√	√		
9C	MFR_LOCATION	R/W Block (12 bytes)	String	Common	√	√	√	√	√	√	√	√		
9D	MFR_DATE	R/W Block (6 bytes)	String	Common	√	√	√	√	√	√	√	√		
9E	MFR_SERIAL	R/W Block (12 bytes)	String	Common	√	√	√	√	√	√	√	√		
9F	Reserved											√		
A0	MFR_VIN_MIN													
A1	MFR_VIN_MAX													
A2	MFR_IIN_MAX													
A3	MFR_PIN_MAX													
A4	MFR_VOUT_MIN													
A5	MFR_VOUT_MAX													
A6	MFR_IOUT_MAX													
A7	MFR_POUT_MAX													
A8	MFR_TAMBIENT_MAX													
A9	MFR_TAMBIENT_MIN													
AA-AF	Reserved													
B9	RAIL_STATE(USER_DATA_09)	R Block	Byte Array	PAGE			√		√					UCD9090A/UCD90160A support.
B0-BF	USER_DATA_00 - USER_DATA_15											√		
C0-CF	Reserved											√		
D0	SEQ_TIMEOUT (MFR_SPECIFIC_00)	R/W Word	LINEAR11 [ms]	PAGE	√	√								Must be configured along with GPI_CONFIG which selects the external pin to use for the input source
D1	VOUT_CAL_MONITOR (MFR_SPECIFIC_01)	R/W Word	LINEAR16 [V]	PAGE	√	√	√	√	√	√	√	√	X	Offset calibration value for the sensor used in READ_VOUT. Signed.
D2	SYSTEM_RESET_CONFIG (MFR_SPECIFIC_02)	R/W Block (4, 6, or 9 bytes)	Byte Array	Common	√	√	√	√	√	√	√	√	X	Configures the System Reset function
D3	SYSTEM_WATCHDOG_CONFIG (MFR_SPECIFIC_03)	R/W Block (4 bytes)	Byte Array	Common	√	√	√	√	√	√	√	√		Configures the System Watchdog function
D4	SYSTEM_WATCHDOG_RESET (MFR_SPECIFIC_04)	Send Byte	n/a	Common	√	√	√	√	√	√	√	√		Resets the System Watchdog timeout counter

Table 3. PMBus Commands (continued)

Code (hex)	Command	Transaction Type	Data Format [Units]	Scope	UCD90120	UCD90124	UCD9090/A	UCD90910	UCD90160/A	UCD90120A	UCD90124A	UCD90240	Data Flash	Comments
D5	MONITOR_CONFIG (MFR_SPECIFIC_05)	R/W Block	Byte Array	Common	√	√	√	√	√	√	√			Configure pins for monitoring (voltage, temperature, and so forth)
D6	NUM_PAGES (MFR_SPECIFIC_06)	Read Byte	Byte	Common	√	√	√	√	√	√	√			Read Only Returns the number of active pages
D7	RUN_TIME_CLOCK (MFR_SPECIFIC_07)	R/W Block	Byte Array	Common	√	√	√	√	√	√	√	√		Time in milliseconds and days (4 bytes each)
D8	RUN_TIME_CLOCK_TRIM (MFR_SPECIFIC_08)	R/W Word	LINEAR11 [%]	Common	√	√	√	√	√	√	√	√		Percent adjustment for calibrating the run-time clock
D9	ROM_MODE (MFR_SPECIFIC_09)	Send Byte	n/a	Common	√	√	√	√	√	√	√	√		Write Only This command sends the device back into ROM mode
DA	USER_RAM_00 (MFR_SPECIFIC_10)	R/W Byte	Byte	Common	√	√	√	√	√	√	√	√		RAM value that is set to 0 during device reset. By writing a nonzero value to this variable and then monitoring its value, a host may determine that a device reset has occurred.
DB	SOFT_RESET (MFR_SPECIFIC_11)	Send Byte	n/a	Common	√	√	√	√	√	√	√	√		Write Only This command restarts the controller firmware
DC	RESET_COUNT (MFR_SPECIFIC_12)	R/W Word (1)	2 Bytes (1)	Common	√	√	√	√	√	√	√	√		The number of times that the device has been reset.(1) This is a single byte in the UCD90120, UCD90124, and UCD90910 devices.
DD	PIN_SELECTED_RAIL_STATES (MFR_SPECIFIC_13)	Read Block (18 bytes)	Byte Array	Common			√		√	√	√	√		Allows encoding on input pins to decide into what state each of the rails should be.
DE	RESEQUENCE (MFR_SPECIFIC_14)	Write Word	2 Bytes	Common			√	√	√	√	√	√	X	Commands selected rails to resequence. (Write Only)
DF	CONSTANTS (MFR_SPECIFIC_15)	Read Block (8 bytes)	Byte Array	Common	√	√	√	√	√	√	√			Fixed information about the device
E0	PWM_SELECT (MFR_SPECIFIC_16)	R/W Byte	Byte	Common	√	√	√	√	√	√	√	√	X	Determines which PWM the PWM_CONFIG command applies to
E1	PWM_CONFIG (MFR_SPECIFIC_17)	R/W Block (8 bytes)	Byte Array	Common	√	√	√	√	√	√	√	√		Configures a PWM (frequency, duty cycle, and phase)

Table 3. PMBus Commands (continued)

Code (hex)	Command	Transaction Type	Data Format [Units]	Scope	UCD90120	UCD90124	UCD9090/A	UCD90910	UCD90160/A	UCD90120A	UCD90124A	UCD90240	Data Flash	Comments
E2	PARM_INFO (MFR_SPECIFIC_18)	R/W Block (5 bytes)	Byte Array	Common	√	√	√	√	√	√	√	√	X	Parm Info: <parm base> <parm offset low byte> <parm offset high byte> <parm count> <parm size> This command sets the parameters used by the Parm Value command
E3	PARM_VALUE (MFR_SPECIFIC_19)	R/W Block	Byte Array	Common	√	√	√	√	√	√	√	√	X	Value transferred to memory location chosen by the PARM_INFO command
E4	TEMPERATURE_CAL_GAIN (MFR_SPECIFIC_20)	R/W Word	LINEAR11 [°C/V]	PAGE	√	√	√	√		√	√	√		Gain calibration for the external sensors used by the READ_TEMPERATURE_2 command
E5	TEMPERATURE_CAL_OFFSET (MFR_SPECIFIC_21)	R/W Word	LINEAR11[°C]	PAGE	√	√	√	√		√	√	√		Offset calibration for the external sensors used by the READ_TEMPERATURE_2 command
E6	(MFR_SPECIFIC_22)											√		
E7	FAN_CONFIG_INDEX (MFR_SPECIFIC_23)	R/W Byte	Byte	Common		√		√			√	√	X	Selects to which fan the FAN_CONFIG command applies
E8	FAN_CONFIG (MFR_SPECIFIC_24)	R/W Block (15 Bytes)	Byte Array	Common		√		√			√	√		Fan configuration – fault detection, auto adjust, etc
E9	FAULT_RESPONSES (MFR_SPECIFIC_25)	R/W Block (9 Bytes)	Byte Array	PAGE	√	√	√	√	√	√	√	√		Defines the response to all supported faults
EA	LOGGED_FAULTS (MFR_SPECIFIC_26)	R/W Block	Byte Array	Common	√	√	√	√	√	√	√	√		Flags in Data Flash that are set when each fault type occurs on each page (1)
EB	LOGGED_FAULT_DETAIL_INDEX (MFR_SPECIFIC_27)	R/W Word	2 bytes	Common	√	√	√	√	√	√	√	√	X	Number of LOGGED_FAULT_DETAIL entries and a read/write index into those entries
EC	LOGGED_FAULT_DETAIL (MFR_SPECIFIC_28)	Read Block	Byte Array	Common	√	√	√	√	√	√	√	√		Detail information about the faults that have occurred
ED	LOGGED_PAGE_PEAKS (MFR_SPECIFIC_29)	R/W Block	Byte Array, Byte [°C], LINEAR16 [V], LINEAR11 [amp]	PAGE	√	√	√	√	√	√	√			Peak temperature, voltage, and current for a given page, stored in Data Flash (1)
EE	LOGGED_COMMON_PEAKS (MFR_SPECIFIC_30)	R/W Byte	Byte [°C]	Common	√	√	√	√		√	√			Peak internal temperature (1)
EF	LOGGED_FAULT_DETAIL_ENABLES (MFR_SPECIFIC_31)	R/W Block	Byte Array	Common	√	√	√	√	√	√	√			Selectable fault logging by rail and by fault type

Table 3. PMBus Commands (continued)

Code (hex)	Command	Transaction Type	Data Format [Units]	Scope	UCD90120	UCD90124	UCD9090/A	UCD90910	UCD90160/A	UCD90120A	UCD90124A	UCD90240	Data Flash	Comments
F0	EXECUTE_FLASH (MFR_SPECIFIC_32)	Send Byte	n/a	Common	√	√	√	√	√	√	√	√		If in ROM mode, starts the device executing in FLASH mode. If already in FLASH mode, command has no effect.
F1	SECURITY (MFR_SPECIFIC_33)	R/W Block (6 bytes)	Binary Array	Common			√		√	√	√	√		Sets the password used to secure the unit against unauthorized modification of its settings
F2	SECURITY_BIT_MASK (MFR_SPECIFIC_34)	R/W Block (32 bytes)	Binary Array	Common			√							Configures which commands are password protected.
F3	MFR_STATUS (MFR_SPECIFIC_35)	Read Block (2 or 4 bytes)	Byte Array	PAGE	√	√	√	√	√	√	√	√	X	Replaces the STATUS_MFR_SPECIFIC command
F4	(MFR_SPECIFIC_36)											√		
F5	MARGIN_CONFIG (MFR_SPECIFIC_37)	R/W Byte	Byte	PAGE	√	√	√	√	√	√	√	√		Selects the margining pin and other margining configuration
F6	SEQ_CONFIG (MFR_SPECIFIC_38)	R/W Block (6-12 bytes)	Byte Array	PAGE	√	√	√	√	√	√	√	√		Configures sequencing dependencies and enable pin
F7	GPO_CONFIG_INDEX (MFR_SPECIFIC_39)	R/W Byte	Byte	Common	√	√	√	√	√	√	√		X	Selects to which GPO the GPO_CONFIG command applies
F8	GPO_CONFIG (MFR_SPECIFIC_40)	R/W Block (20 or 29 bytes)	Byte Array	Common	√	√	√	√	√	√	√	√		Configures output pins and their dependencies
F9	GPI_CONFIG (MFR_SPECIFIC_41)	R/W Block (13 bytes)	Byte Array	Common	√	√	√	√	√	√	√	√		Configures input pins
FA	GPIO_SELECT (MFR_SPECIFIC_42)	R/W Byte	Byte	Common	√	√	√	√	√	√	√	√	X	Determines to which GPIO the GPIO_CONFIG command applies
FB	GPIO_CONFIG (MFR_SPECIFIC_43)	R/W Byte	Byte	Common	√		√	√	√	√	√	√		Set or get the state of a GPIO
FC	MISC_CONFIG (MFR_SPECIFIC_44)	R/W Block	2 Bytes	Common	√	√	√	√	√	√	√	√		Miscellaneous configuration settings
FD	DEVICE_ID (MFR_SPECIFIC_45)	Read Block (up to 32 bytes)	String	Common	√	√	√	√	√	√	√	√		Returns ASCII string with hardware and firmware version information of the controller
FE	Mfr_Specific_Extended_Command											√		
FF	PMBUS_Extended_Command											√		

6 Implementation Details for PMBus Core Commands

The following PMBus core commands are defined in the PMBus specification. This section describes details that are unique to the UCD90xxx implementation.

6.1 (00h) PAGE

The PAGE command provides the ability to configure, control, and monitor multiple outputs on one unit using a single PMBus physical address. When the PAGE command is sent, all subsequent commands are applied to settings for the rail selected by the PAGE command.

The Fusion Digital Power Designer software uses the term Rail to refer to a voltage output. Rails are numbered starting with one, whereas pages are numbered starting at zero. The relationship between the PMBus PAGE value and the Rail number is shown in Table 4.

Setting PAGE = 0xFF means that the following write commands are to be applied to all outputs. A page setting of 0xFF is invalid for all read commands, with the exception of the PAGE command.

Table 4. Relationship Between PAGE and Rail (UCD90120 Example)

Page	Output Rail
0	1
1 (1)	2
2 (1)	3
...	...
11 (1)	12
12 – 254	Invalid
255 (0xFF)	All

(1) The maximum number of rails on the UCD90120 is 12.

Section 11.10 of the PMBus specification describes the PAGE command in more detail.

6.2 (01h) OPERATION

This command is used to turn outputs on and off along with input from the CONTROL pin. Section 12.1 of the PMBus specification describes this command in more detail.

The UCD90xxx supports the following modes for the Operation command:

- Immediate Off (No Sequencing)
- Soft Off (With Sequencing)
- On Nominal (No Margining)
- On Margin High (Ignore Faults)
- On Margin High (Act on Fault)
- On Margin Low (Ignore Faults)
- On Margin Low (Act on Fault)

6.3 (11h) STORE_DEFAULT_ALL

The STORE_DEFAULT_ALL command saves the PMBus parameters from Operating Memory into the Default Store in Data Flash. The UCD90xxx uses the most recently written set of Default Store values at startup or after a RESTORE_DEFAULT_ALL command. If the Default Store has never been written, values from the hard-coded memory are used.

NOTE: The device configuration will be corrupted if a power cycle or a reset occurs before this save operation is completed. To ensure a successful save operation, after writing the STORE_DEFAULT_ALL command, wait for the STORE_DEFAULT_ALL_DONE bit to be set (see the MFR_STATUS). Once that bit is set, check the STORE_DEFAULT_ALL_ERROR bit. If the STORE_DEFAULT_ALL_DONE bit is set and the STORE_DEFAULT_ ALL_ERROR is not set, the operation was successful.

NOTE: Monitoring and other tasks (including PMBus communication) are not performed during this save operation which may take up to 100 milliseconds.

6.4 (12h) RESTORE_DEFAULT_ALL

The RESTORE_DEFAULT_ALL command restores the PMBus parameters from the Default Store into Operating Memory. If the Default Store has never been written, values from the hard-coded memory are used

NOTE: Resetting the device is a better (more thorough) way to perform this operation.

6.5 (1Bh) SMBALERT_MASK

This command is added in PMBUS specification 1.2 and is described in section 15.38. It is used to block a status bit(s) from causing the SMBALERT# signal to be asserted. Refer to PMBUS specification document for format details. This command has to be used together with status command codes in order to write or read the mask of a specific status bit. The status command codes that can be used with this command include:

- STATUS_VOUT
- STATUS_IOUT
- STATUS_TEMPERATURE
- STATUS_CML
- STATUS_FANS_1_2
- STATUS_FANS_3_4

Another status command code, MFR_STATUS, also needs to work with the SMBALERT_MASK command. However, SMBALERT_MASK can only write/read one byte mask at a time. Since MFR_STATUS contains 40 bits, it is split into 5 sub-commands to work with the SMBALERT_MASK command:

- MFR_STATUS_0: for MFR_STATUS bit 7 to 0
- MFR_STATUS_1: for MFR_STATUS bit 15 to 8
- MFR_STATUS_2: for MFR_STATUS bit 23 to 16
- MFR_STATUS_3: for MFR_STATUS bit 31 to 24
- MFR_STATUS_4: for MFR_STATUS bit 39 to 32

6.6 (20h) VOUT_MODE

This command, described in Sections 8.1 and 8.2 of the PMBus specification, indicates the data format used for all commands related to output voltage (all LINEAR16 commands). The command includes a 3-bit Mode field and a 5-bit Parameter field. In UCD90xxx, the Mode field is a read-only and is fixed to 000b(linear data format, described in Section 2.1). The Parameter field is the exponent value and can be modified.

NOTE: This exponent field must be updated before modifying any value that is affected by this setting (all LINEAR16 commands).

Table 5 shows the full-scale range and the resolution of different exponent values. For example, in order to monitor a 12-V signal with the finest possible resolution, the preferred exponent is –11.

Table 5. Exponent Influence on Voltage Range and Resolution

Exponent	Range (V)		Resolution (mV)
–7	0	255.99219	7.81250
–8	0	127.99609	3.90625
–9	0	63.99805	1.95313
–10	0	31.99902	0.97656
–11	0	15.99951	0.48828
–12	0	7.99976	0.24414
–13	0	3.99988	0.12207
–14	0	1.99994	0.06104
–15	0	0.99997	0.03052

The ADC full-scale range of UCD90xxx devices is 2.5 V (except UCD90240 which supports external reference). The monitored voltage signals must be scaled proportionally to fit into the ADC window. The nominal voltage value after scaling must be less than 2.5 V, so as to take into account overvoltage scenarios. Table 6 shows nominal voltage ranges suited for each exponent value and corresponding scale factors. Table 6 assumes the nominal voltages' setpoint is at 1.875 V after scaling, 75% of the 2.5-V ADC full-scale range. The scale factor is programmed by VOUT_SCALE_MONITOR command.

Table 6. Example Settings for Voltage Monitoring Ranges

Exponent	High		Low	
	Voltage	Scale	Voltage	Scale
–7	192	0.009766	96	0.019531
–8	96	0.019531	48	0.039063
–9	48	0.039063	24	0.078125
–10	24	0.078125	12	0.15625
–11	12	0.15625	6	0.3125
–12	6	0.3125	3	0.625
–13	3	0.625	1.5	1.25
–14	1.5	1.25	0.75	2.5
–15	0.75	2.5	0.375	5

6.7 (38h) IOUT_CAL_GAIN

This command, described in section 14.8 of the PMBus specification, is used to configure the gain of the current-sense circuit. The units for this command are milliohms (mV/A).

Note that some ambiguity exists in Rev 1.1 of the PMBus specification. One sentence says that the command uses the *conductance* of the sense resistor, but a later sentence says that the resistance must be used. In one place, the units are listed as ohms, but the default value is declared as 0 milliohms.

Rev 1.0 of the PMBus specification used resistance (not conductance) and milliohms. Rev 1.2 has cleared up this ambiguity and revert to the Rev 1.0 wording. For the UCD90xxx devices, the ambiguous language in Rev 1.1 is interpreted to have the same meaning as Rev 1.0 (that is, milliohms).

6.8 (3B-3Ch, 3E-3Fh) FAN_COMMAND_1 Through FAN_COMMAND_4

This command, described in section 14.12 of the PMBus specification, is used to adjust the operating speed of the fan. The PMBus specification describes two ways of setting the fan command (RPM or duty cycle), but the UCD90xxx only supports the duty cycle mode.

The meaning of this command can be modified by the speed type in the FAN_CONFIG command (see Section 10.24).

This command has two data bytes in the Linear11 data format. The units are percent duty cycle or percent operating speed, from 0 to 100% in integer form.

Note for versions with more than four fans: FAN_COMMAND_1 becomes an indexed command and along with FAN_CONFIG_INDEX is used to set the speed for all of the fans. FAN_COMMAND_2 through FAN_COMMAND_4 can still be used to directly set the speed for the corresponding fans.

6.9 (41h – 69h) xxx_FAULT_RESPONSE

The following commands are replaced by the FAULT_RESPONSES command (see Section 10.25).

Table 7. Replaced Fault Response Commands

Code	Command
41h	VOUT_OV_FAULT_RESPONSE
45h	VOUT_UV_FAULT_RESPONSE
47h	IOUT_OC_FAULT_RESPONSE
4Ch	IOUT_UC_FAULT_RESPONSE
50h	OT_FAULT_RESPONSE
63h	TON_MAX_FAULT_RESPONSE

6.10 (62h) TON_MAX_FAULT_LIMIT

This command, described in Section 16.3 of the PMBus specification, states that the "command sets an upper limit, in ms, on how long the unit can attempt to power up the output without reaching the *output undervoltage fault limit*". For the UCD90xxx, this command will instead "set an upper limit, in ms, on how long the unit can attempt to power up the output without reaching the *POWER_GOOD_ON voltage level*."

For devices other than the UCD90120 and UCD90124: When no voltage monitor pin is assigned to a rail, the sequencer cannot monitor the rail voltage and determine its power-good state. Therefore, after the rail is enabled, it will be given power-good state after a delay time defined by TON_MAX_FAULT_LIMIT.

6.11 (66h) TOFF_MAX_WARN_LIMIT

For devices other than the UCD90120 and UCD90124: When there is no voltage monitor pin assigned to a rail, this time is used to determine when a rail leaves the power-good state after it is disabled. In this case, setting TOFF_MAX_WARN_LIMIT to 0x7FFF (No Limit) will result in no delay between disabling the rail and leaving the power-good state.

6.12 (80h) STATUS_MFR_SPECIFIC

The UCD90xxx has replaced the STATUS_MFR_SPECIFIC command with MFR_STATUS (see Section 10.35) in order to support more than eight status bits.

6.13 (81h) STATUS_FAN_1_2 and (82h) STATUS_FAN_3_4

The FAN_n_FAULT bit is set to 1 when the measured fan speed is less than the value set by the "speed fault limit" in the FAN_CONFIG (0xE8) command for 5 consecutive seconds.

Table 8 and Table 9 outline what is supported in these commands.

Table 8. STATUS_FAN_1_2 Support

Bit	Name	Description	Supported
7	FAN_1_FAULT	Fan 1 Fault	Yes
6	FAN_2_FAULT	Fan 2 Fault	Yes
5	FAN_1_WARN	Fan 1 Warning	No
4	FAN_2_WARN	Fan 2 Warning	No
3	SPD_1	Fan 1 Speed Overridden	No
2	SPD_2	Fan 2 Speed Overridden	No
1	AIRFLOW_FAULT	Airflow Fault	No
0	AIRFLOW_WARN	Airflow Warning	No

Table 9. STATUS_FAN_3_4 Support

Bit	Name	Description	Supported
7	FAN_3_FAULT	Fan 3 Fault	Yes
6	FAN_4_FAULT	Fan 4 Fault	Yes
5	FAN_3_WARN	Fan 3 Warning	No
4	FAN_4_WARN	Fan 4 Warning	No
3	SPD_3	Fan 3 Speed Overridden	No
2	SPD_4	Fan 4 Speed Overridden	No
1	AIRFLOW_FAULT	Airflow Fault	No
0	AIRFLOW_WARN	Airflow Warning	No

Note for versions with more than four fans: When more than four fans are supported, the fan fault status are packed in the existing STATUS_FANS_1_2 (1-8) and STATUS_FANS_3_4 (9-16) commands as shown in Table 10 and Table 11 .

Table 10. STATUS_FAN_1_2 Support With More Than Four Fans

Bit	Name	Description
0	FAN_1_FAULT	Fan 1 Fault
1	FAN_2_FAULT	Fan 2 Fault
2	FAN_3_FAULT	Fan 3 Fault
3	FAN_4_FAULT	Fan 4 Fault
4	FAN_5_FAULT	Fan 5 Fault
5	FAN_6_FAULT	Fan 6 Fault
6	FAN_7_FAULT	Fan 7 Fault
7	FAN_8_FAULT	Fan 8 Fault

Table 11. STATUS_FAN_3_4 Support With More Than Four Fans

Bit	Name	Description
0	FAN_9_FAULT	Fan 9 Fault
1	FAN_10_FAULT	Fan 10 Fault
2	FAN_11_FAULT	Fan 11 Fault
3	FAN_12_FAULT	Fan 12 Fault
4	FAN_13_FAULT	Fan 13 Fault
5	FAN_14_FAULT	Fan 14 Fault
6	FAN_15_FAULT	Fan 15 Fault
7	FAN_16_FAULT	Fan 16 Fault

6.14 (8Dh) READ_TEMPERATURE_1

This read-only command returns the temperature from a sensor embedded inside the UCD90xxx controller.

6.15 (8Eh) READ_TEMPERATURE_2

This paged command returns the temperature from an external temperature sensor located in or near an output power module.

NOTE: If no temperature monitor pin is assigned to a rail, the internal temperature sensor is used for that rail. See the MONITOR_CONFIG command (Section 10.6).

Devices other than the UCD90120 and UCD90124: If the user writes this command, the written value will be used as the temperature until another value is written by the user, regardless whether or not a temperature monitor pin is assigned to the rail. When a temperature monitor pin is assigned, once READ_TEMPERATURE_2 is written, the temperature monitor pin will not be used again until the device is reset. Similarly, when no temperature monitor pin is assigned, once READ_TEMPERATURE_2 is written, the internal temperature sensor will not be used again until the device is reset.

6.16 (90-93h) FAN_SPEED_1 Through FAN_SPEED_4

The values returned from this command are only valid when the fan is enabled. The fan can be enabled with the FAN_CONFIG command (see Section 10.23).

Note for versions with more than four fans: FAN_SPEED_1 becomes an indexed command. It can be used with FAN_CONFIG_INDEX command to read the speed of all the fans. FAN_SPEED_2 through FAN_SPEED_4 can still be used to directly read corresponding fan speeds.

6.17 (ADh) IC_DEVICE_ID

This command is added in PMBUS1.2. It is used to read the part number of the device.

6.18 (AEh) IC_DEVICE_REV

This command is added in PMBUS1.2. It is used to read the revision of the device.

7 Input and Output Pin Configuration

Each of the input pins (Fan Tach, GPI, and so forth) and output pins (Enable, PWM, GPO, and so forth) are configured using one byte. Thee bits are defined as follows:

Bit	7	6	5	4	3	2	1	0
Purpose	**Pin ID** Table 12, Table 13: UCD90240 Pin ID Definitions Table 14: UCD9012x, UCD90160, and UCD90910 Pin ID Definitions Table 15: UCD9090 Pin ID Definitions					**Polarity** 0 = Active Low 1 = Active High	**Mode** 0 = Unused 1 = Input 2 = Actively Driven Output 3 = Open-Drain Output	

Bits 1:0 set the mode for the pin.

Bit 2 sets the pin polarity. A pin is asserted when its state is active level.

Bits 7:3 select the Pin ID of the desired I/O pin. Note that the Pin ID numbers are the same for all UCD90xxx devices except UCD90240. This is different from the hardware pin numbers which differ in different package types

This configuration byte is used in several of the following commands, such as FAN_CONFIG, SEQ_CONFIG, GPO_CONFIG, and GPI_CONFIG, and FAULT_PIN_CONFIG. The commands often dictate the Mode of the pin. For example, an Enable can only be an output. It cannot be configured as an input. But, for consistency, this configuration byte format previously described is always used.

Table 16 and Table 17 outline all of the usage options associated with each pin.

NOTE: Pin Usage Conflicts

It is possible to issue commands with conflicting pin selections. UCD90xxx firmware does not attempt to detect and prevent all possible invalid setting combinations. The Fusion Digital Power Designer GUI provides some additional validity checking, but it is the user's responsibility to eliminate conflicting GPIO configurations.

Example: If a command is used to configure a pin for a specific GPIO or sequencing purpose and then issued again with the same pin unassigned, the pin may not revert back to its default usage until after the controller has been reset or power cycled.

Table 12. UCD90240 PWM Margin Pin ID Definitions

Pin ID	Pin Name	157-Pin Pin Number	Purposes
0	PWM_00	J13	MARGIN
1	PWM_01	L5	MARGIN
2	PWM_02	D8	MARGIN
3	PWM_03	K6	MARGIN
4	PWM_04	D4	MARGIN
5	PWM_05	E4	MARGIN
6	PWM_06	F5	MARGIN
7	PWM_07	N5	MARGIN
8	PWM_08	N6	MARGIN
9	PWM_09	K5	MARGIN
10	PWM_10	M6	MARGIN
11	PWM_11	L6	MARGIN
12	PWM_12	D11	MARGIN
13	PWM_13	C12	MARGIN
14	PWM_14	A13	MARGIN
15	PWM_15	B13	MARGIN
16	PWM_16	D12	MARGIN

Table 12. UCD90240 PWM Margin Pin ID Definitions (continued)

Pin ID	Pin Name	157-Pin Pin Number	Purposes
17	PWM_17	C13	MARGIN
18	PWM_18	E12	MARGIN
19	PWM_19	E13	MARGIN
20	PWM_20	M13	MARGIN
21	PWM_21	L12	MARGIN
22	PWM_22	M5	MARGIN
23	PWM_23	J12	MARGIN

Table 13. UCD90240 GPO, GPI, and Enable Pin ID Definitions

Pin ID	Pin Name	157-Pin PinNum	Purposes		Pin ID	Pin Name	157-Pin PinNum	Purposes
24	GPIO_F0	M9	EN		56	GPIO_A0	L3	LGPO
25	GPIO_F1	N9	EN		57	GPIO_A1	M1	LGPO
26	GPIO_F2	L10	EN		58	GPIO_A2	M2	LGPO
27	GPIO_F3	K10	EN		59	GPIO_A3	M3	LGPO
28	GPIO_F4	L9	EN		60	GPIO_A4	L4	GPI/GPIO*
29	GPIO_F5	K9	EN		61	GPIO_A5	N1	GPI/GPIO*
30	GPIO_F6	N8	EN		62	GPIO_A6	M4	GPI/GPIO*
31	GPIO_F7	M8	EN		63	GPIO_A7	N2	GPI/GPIO*
32	GPIO_G0	L8	EN		64	GPIO_B6	F4	GPI/GPIO*
33	GPIO_G1	K8	EN		65	GPIO_B7	F3	GPI/GPIO*
34	GPIO_G2	N7	EN		66	GPIO_N2	G3	GPI/GPIO*
35	GPIO_G3	M7	EN		67	GPIO_N3	D10	GPI/GPIO*
36	GPIO_G4	K7	EN		68	GPIO_N4	L11	GPI/GPIO*
37	GPIO_G5	L7	EN		69	GPIO_N5	N12	GPI/GPIO*
38	GPIO_G6	N4	EN		70	GPIO_N6	N11	GPI/GPIO*
39	GPIO_G7	N3	EN		71	GPIO_N7	M11	GPI/GPIO*
40	GPIO_H0	K3	EN		72	GPIO_M0	F13	GPI/GPIO*
41	GPIO_H1	K4	EN		73	GPIO_M1	F12	GPI/GPIO*
42	GPIO_H2	J4	EN		74	GPIO_M2	G11	GPI/GPIO*
43	GPIO_H3	J2	EN		75	GPIO_M3	H10	GPI/GPIO*
44	GPIO_H4	J3	EN		76	GPIO_M4	H13	GPI/GPIO*
45	GPIO_H5	H4	EN		77	GPIO_M5	H12	GPI/GPIO*
46	GPIO_H6	H3	EN		78	GPIO_M6	H11	GPI/GPIO*
47	GPIO_H7	G4	EN		79	GPIO_M7	L13	GPI/GPIO*
48	GPIO_J0	C9	LGPO		80	GPIO_K4	B11	GPI/GPIO*
49	GPIO_J1	B9	LGPO		81	GPIO_K5	B12	GPI/GPIO*
50	GPIO_J2	A9	LGPO		82	GPIO_K6	C11	GPI/GPIO*
51	GPIO_J3	C8	LGPO		83	GPIO_K7	A12	GPI/GPIO*
52	GPIO_J4	D5	LGPO					
53	GPIO_J5	C5	LGPO					
54	GPIO_J6	C6	LGPO		*: These pins can also be used for command controlled GPO(GPIO_CONFIG command).			
55	GPIO_J7	C4	LGPO					

Table 14. UCD9012x, UCD90160, and UCD90910 Pin ID Definitions

Pin ID	Pin Name	Pin Number
0	FPWM1_GPIO5	17
1	FPWM2_GPIO6	18
2	FPWM3_GPIO7	19
3	FPWM4_GPIO8	20
4	FPWM5_GPIO9	21
5	FPWM6_GPIO10	22
6	FPWM7_GPIO11	23
7	FPWM8_GPIO12	24
8	GPI1_PWM1	31
9	GPI2_PWM2	32
10	GPI3_PWM3	42
11	GPI4_PWM4	41
12	GPIO14	29
13	GPIO15	30
14	TDO_GPIO20	37
15	TCK_GPIO19	36
16	TMS_GPIO22	39
17	TDI_GPIO21	38
18	GPIO1	11
19	GPIO2	12
20	GPIO3	13
21	GPIO4	14
22	GPIO13	25
23	GPIO16	33
24	GPIO17	34
25	GPIO18	35

Table 15. UCD9090 Pin ID Definitions

Pin ID	Pin Name	Pin Number
0	FPWM1_GPIO5	10
1	FPWM2_GPIO6	11
2	FPWM3_GPIO7	12
3	FPWM4_GPIO8	13
4	FPWM5_GPIO9	14
5	FPWM6_GPIO10	15
6	FPWM7_GPIO11	16
7	FPWM8_GPIO12	17
8	GPI1_PWM1	22
9	GPI2_PWM2	23
10	GPIO14	21
11	TDO_GPIO19	28
12	TCK_GPIO18	27
13	TMS_GPIO21	30
14	TDI_GPIO20	29
15	GPIO1	4
16	GPIO2	5
17	GPIO3	6

Table 15. UCD9090 Pin ID Definitions (continued)

Pin ID	Pin Name	Pin Number
18	GPIO4	7
19	GPIO13	18
20	GPIO15	24
21	GPIO16	25
22	GPIO17	26

Table 16. UCD9012x, UCD90160, and UCD90910 Pin Usage

Pin Name	Pin Number	Rail Enable	GPI	GPO	Fan Tach[1]	Fan PWM[1]	Fan Enable[1]	PWM Out	Margining PWM	Margining Enable
FPWM1_GPIO5	17	√	√	√	√	√	√	√	√	√
FPWM2_GPIO6	18	√	√	√	√	√	√	√	√	√
FPWM3_GPIO7	19	√	√	√	√	√	√	√	√	√
FPWM4_GPIO8	20	√	√	√	√	√	√	√	√	√
FPWM5_GPIO9	21	√	√	√	√	√	√	√	√	√
FPWM6_GPIO10	22	√	√	√	√	√	√	√	√	√
FPWM7_GPIO11	23	√	√	√	√	√	√	√	√	√
FPWM8_GPIO12	24	√	√	√	√	√	√	√	√	√
GPI1_PWM1	31		√		√	√		√	√	
GPI2_PWM2	32		√		√	√		√	√	
GPI3_PWM3	42		√		√	√		√	√	
GPI4_PWM4	41		√		√	√		√	√	
GPIO14	29	√	√	√	√		√			√
GPIO15	30	√	√	√	√		√			√
TDO_GPIO20	37	√	√	√	√		√			√
TCK_GPIO19	36	√	√	√	√		√			√
TMS_GPIO22	39	√	√	√	√		√			√
TDI_GPIO21	38	√	√	√	√		√			√
GPIO1	11	√	√[2]	√	√		√			√
GPIO2	12	√	√[2]	√	√		√			√
GPIO3	13	√	√[2]	√	√		√			√
GPIO4	14	√	√[2]	√	√		√			√
GPIO13	25	√	√[2]	√	√		√			√
GPIO16	33	√	√[2]	√	√		√			√
GPIO17	34	√	√[2]	√	√		√			√
GPIO18	35	√	√[2]	√	√		√			√

(1) The Fan Tach, Fan PWM, and Fan Enable modes are not supported in the UCD90120.

(2) These are Low Latency GPI pins. When using a GPI pin as an input to the logic for a GPO (see the Section 10.40 command), these GPI pins offer a faster response time than others.

Table 17. UCD9090 Pin Usage

Pin Name	Pin Number	Rail Enable	GPI	GPO	PWM Out	Margining PWM	Margining Enable
FPWM1_GPIO5	11	√	√	√	√	√	√
FPWM2_GPIO6	12	√	√	√	√	√	√
FPWM3_GPIO7	13	√	√	√	√	√	√
FPWM4_GPIO8	14	√	√	√	√	√	√
FPWM5_GPIO9	15	√	√	√	√	√	√
FPWM6_GPIO10	16	√	√	√	√	√	√
FPWM5_GPIO11	17	√	√	√	√	√	√
FPWM6_GPIO12	18	√	√	√	√	√	√
GPI1_PWM1	23		√		√	√	
GPI2_PWM2	24		√		√	√	
GPIO14	22	√	√	√			√
TDO_GPIO19	29	√	√	√			√
TCK_GPIO18	28	√	√	√			√
TMS_GPIO21	31	√	√	√			√
TDI_GPIO20	30	√	√	√			√
GPIO1	5	√	√(1)	√			√
GPIO2	6	√	√(1)	√			√
GPIO3	7	√	√(1)	√			√
GPIO4	8	√	√(1)	√			√
GPIO13	19	√	√(1)	√			√
GPIO15	25	√	√(1)	√			√
GPIO16	26	√	√(1)	√			√
GPIO17	27	√	√(1)	√			√

(1) These are Low Latency GPI pins. When using a GPI pin as an input to the logic for a GPO (see the Section 10.40 command), these GPI pins offer a faster response time than others.

8 PWM Configuration

PWM pins can be used to control fan speed (see FAN_CONFIG), margin a rail (see MARGIN_CONFIG), or as a general-purpose PWM (see PWM_CONFIG).

Table 18, Table 19, Table 20, and Table 21 outline the range of frequencies that can be configured for the various PWMs.

NOTE: When only one of the FPWM pins in an FPWM pair (for example, FPWM1 and FPWM2) is configured as a PWM, the other, unconfigured FPWM in the pair also outputs a PWM signal. If the unconfigured FPWM is not going to be used, it is recommended that the pin be configured as a GPO that is driven low (see the GPIO_CONFIG command, Section 10.43).

The two FPWM pins in an FPWM pair must have the same frequency. If both pins are configured as PWM, PWM_CONFIG command must be written for both FPWM pins if the frequency is changed.

When both FPWM pins in an FPWM pair are used for margining, and after the device is out of reset, the even FPWM pin may output some pulse for no more than 30 µs. This time varies depending on the configured duty cycle and frequency. These pulses may cause overshoot on the margining rail if the rail is regulated before the device is out of reset. Use the even FPWM pin to margin the rails that are directly controlled by the device.

Table 18. PWM-Supported Frequencies (UCD90240)

PWM Type	Supported Frequencies
PWM	1 kHz to 1 MHz

Table 19. PWM Supported Frequencies (all except UCD90240)

PWM Type	Supported Frequencies
FPWM	15.259 kHz to 125 MHz
PWM	1 Hz to 7.8125 MHz

Table 20. PWM Usage Notes (Devices Other Than the UCD9090)

PWM Name	Usage Note
FPWM1	Shares the same frequency as FPWM2
FPWM2	Shares the same frequency as FPWM1
FPWM3	Shares the same frequency as FPWM4
FPWM4	Shares the same frequency as FPWM3
FPWM5	Shares the same frequency as FPWM6
FPWM6	Shares the same frequency as FPWM5
FPWM7	Shares the same frequency as FPWM8
FPWM8	Shares the same frequency as FPWM7
PWM1(1)	Frequency is fixed at 10 kHz
PWM2(1)	Frequency is fixed at 1 kHz
PWM3	none
PWM4	none

(1) Devices other than the UCD90120 and UCD90124: when either PWM1 or PWM2 is configured as a PWM output and the duty cycle is set to 0%, small glitches occur on that signal. These glitches occur at the period boundary associated with the fixed frequency on those pins

Table 21. PWM Usage Notes (UCD9090)

PWM Name	Usage Note
FPWM1	Shares the same frequency as FPWM2
FPWM2	Shares the same frequency as FPWM1
FPWM3	Shares the same frequency as FPWM4
FPWM4	Shares the same frequency as FPWM3
FPWM5	Shares the same frequency as FPWM6
FPWM6	Shares the same frequency as FPWM5
FPWM7	Shares the same frequency as FPWM8
FPWM8	Shares the same frequency as FPWM7
PWM1	none
PWM2	none

9 Implementation Details for User Data Commands

This section is for UCD90240 only.

9.1 (B5h) BLACK_BOX_FAULT_INFO (USER_DATA_05)

The block read-only command returns detailed information of the first fault.

1. Time stamp in milliseconds and days
2. Whether or not the fault is page specific
3. The page or GPI that triggered the fault(when applicable)
4. Fault type
5. Status of all GPOs when the fault occurred
6. Status of all GPIs when the fault occurred

Clearing the Log: Writing a block with all 0x00 bytes clear the black box log entries. Nonzero values in any data byte returns a NACK due to Invalid Data.

Table 22. BLACK_BOX_FAULT_INFO Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = B5
1	0		BYTE_COUNT = 21
2	1	0	**Bit** **Description** 0 paged or non-paged fault 7:1 fault_page_num
3	2	1	Days(low byte)(1)
4	3	2	Days(high byte)(1)
5	4	3	**Bit** **Description** 0: first fault log valid(1)/not valid(0)(2) 7:1 Fault Type see Table 85
6	5	4	Fault value (low byte) see Table 85
7	6	5	Fault value (middle byte) see Table 85
8	7	6	Fault value (high byte) see Table 85
9	8	7	Milliseconds (low byte)(1)
10	9	8	Milliseconds (middle low byte)(1)
11	10	9	Milliseconds (middle high byte)(1)
12	11	10	Milliseconds (high byte)(1)
13	12	11	**Bit** **Description** 0 Not Valid Log(0)/Valid Log(1)(3) 7:1 Reserved bits
14	13	12	GPO status bit mask **Bit** **Description** 7:0 GPO[7-0]
15	14	13	**Bit** **Description** 3:0 GPO[11-8] status 7:4 Reserved

(1) The time stamp is offset from 2000-01-01 00:00:00.00. Adding that time base into the logged time stamp can get the actual time.
(2) When this bit is set, the first 10 byte payload data in the black box log (BLACK_BOX_FAULT_INFO) is valid, which describes basic information of the first fault. Additional information may or may not be valid depending on the Valid log bit (see Note 3).
(3) When this bit set, the whole black box log is valid. Application can call BLACK_BOX_FAULT_RAILS_WARNING and BLACK_BOX_FAULT_RAILS_VALUE command to obtain the full black box log information.

Table 22. BLACK_BOX_FAULT_INFO Command Format (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
16	15	14	GPI status bit mask (low byte). **Bit Description** 7:0 GPI[7-0]
17	16	15	GPI status bit mask (middle byte) **Bit Description** 7:0 GPI[15-8]
18	17	16	GPI status bit mask (high byte) **Bit Description** 7:0 GPI[23-16]
19	18	17	GPI status (Reserved for future)
20	19	18	Reserved
21	20	19	Reserved
22	21	20	Reserved

9.2 (B6h) BLACK_BOX_FAULT_RAILS_WARNING(USER_DATA_06)

The block read-only command returns warning status of all rails.

Table 23. BLACK_BOX_FAULT_WARNING Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = B6
1	0		BYTE_COUNT = 24
2	1	0	Rail 1 warning status **Bit Description** 7 Overvoltage warning 6 Undervoltage warning 5 Overcurrent Warning 4-3 Reserved 2 Power-down TOFF_MAX warning 1 Overtemperature warning 0 Reserved
3	2	1	Rail 2 warning status same as Rail1
…	…	…	Rail N warning status same as Rail1
25	24	23	Rail 24 warning status same as Rail1

9.3 (B7h) BLACK_BOX_LOG_RAILS_VALUE(USER_DATA_07)

The block read-only paged command returns warning status and monitored values for a given rail.

Table 24. BLACK_BOX_FAULT_WARNING Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = B7
1	0		BYTE_COUNT = 7
2	1	0	Warning status (see Table 23)
3	2	1	Monitored voltage value [low byte]
4	3	2	Monitored voltage value [high byte]
5	4	3	Monitored current value [low byte]
6	5	4	Monitored current value [high byte]
7	6	5	Monitored temperature value [low byte]
8	7	6	Monitored temperature value [high byte]

Table 25. Rail N Value

Description	Value Units	Description
Voltage Rail	Voltage	LINEAR16
Current Rail	Current	LINEAR11
Temperature Rail	Temperature	LINEAR11

9.4 (B9h) RAIL_STATE (USER_DATA_09)

The Read Block Paged Command returns the current state of the pages. This command is only available for UCD9090A and UCD90160A.

Table 26. RAIL_STATE Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = B9
1	0		BYTE_COUNT = 1
2	1	0	Rail State(see Table 20)

Table 27. Rail State

Rail State	Value	Description
IDLE	1	On condition is not met, or rail is shut down due to fault, or rail is waiting for the resequence
SEQ_ON	2	Wait the dependency to be met to assert ENABLE signal
START_DELAY	3	TON_DELAY to assert ENABLE signal
RAMP_UP	4	Enable is asserted and rail is on the way to reach power good
REGULATION	5	Once the monitoring voltage is over POWER_GOOD when enable signal is asserted, rails stay at this state even if the voltage is below POWER_GOOD late as long as there is no fault action taken.
SEQ_OFF	6	Wait the dependency to be met to de-assert ENABLE signal
STOP_DELAY	7	TOFF_DELAY to de-assert ENABLE signal
RAMP_DOWN	8	Enable signal is de-asserted and rail is ramping down. This state is only available if TOFF_MAX_WARN_LIMIT is not set to unlimited; or If the turn off is triggered by a fault action, rail must not be under fault retry to show RAMP DOWN state. Otherwise, IDLE state is present.

10 Implementation Details for Manufacturer-Specific Commands

10.1 (D0h) FAULT_PIN_CONFIG (MFR_SPECIFIC_00) (UCD90240 Only)

This Read/Write block command configures Fault Pin function for synchronized cascading operation. Fault Pins of different UCD90240 devices can be connected to the same Fault Bus. The Fault Bus is pulled up to 3.3 V through a resistor. When one Fault Pin pulls the bus low, other Fault Pins on the bus will detect the same fault event. As a result, several cascaded UCD90240 devices will respond to the fault event synchronously. The following events can impact the fault pins: RESEQUENCE_ERROR, SEQ_ON_TIMEOUT, SEQ_OFF_TIMEOUT, OT_FAULT, IOUT_UC_FAULT, IOUT_OC_FAULT, VOUT_UV_FAULT, VOUT_OV_FAULT, and TON_MAX_FAULT.

Fault pin configuration includes three commands: this command (D0h), (F9h) GPI_CONFIG (MFR_SPECIFIC_41) and (F4h) GPI_FAULT_RESPONSES (MFR_SPECIFIC_36). This command (D0h) configures Fault Pins as fault-influenced outputs. The state of a Fault Pin is determined by any fault of the selected rails. The (F9h) GPI_CONFIG (MFR_SPECIFIC_41) command configures Fault Pins as fault inputs, in which the Fault Enable Flags should be set (see Section 10.41.2). The (F4h) GPI_FAULT_RESPONSES (MFR_SPECIFIC_36) command configures fault response. This way, when there is a fault coming from the fault bus, the fault pin behaves as a GPI and triggers GPI fault response; where there is a fault raised from within the device, the fault pin pulls low the fault bus notifying other fault pins on the same bus. When using TI Fusion GUI to configure the device, the Fusion GUI will automatically issue the previous three commands to configure the fault pins.

Table 28. FAULT_PIN_CONFIG Command Format (UCD90240 Only)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = D0
1	0		BYTE_COUNT = 29
2	1	0	Fault Pin 0 Configuration
3	2	1	Fault Pin 1 Configuration
4	3	2	Fault Pin 2 Configuration
5	4	3	Fault Pin 3 Configuration
6	5	4	Page Mask for Fault Pin 0 (Byte 0 – LSB)
7	6	5	Page Mask for Fault Pin 0 (Byte 1)
8	7	6	Page Mask for Fault Pin 0 (Byte 2)
9	8	7	Reserved (must be set to 0)
10	9	8	Reserved (must be set to 0)
11	10	9	Reserved (must be set to 0)
12	11	10	Page Mask for Fault Pin 1 (Byte 0 – LSB)
13	12	11	Page Mask for Fault Pin 1 (Byte 1)
14	13	12	Page Mask for Fault Pin 1 (Byte 2)
15	14	13	Reserved (must be set to 0)
16	15	14	Reserved (must be set to 0)
17	16	15	Reserved (must be set to 0)
18	17	16	Page Mask for Fault Pin 2 (Byte 0 – LSB)
19	18	17	Page Mask for Fault Pin 2 (Byte 1)
20	19	18	Page Mask for Fault Pin 2 (Byte 2)
21	20	19	Reserved (must be set to 0)
22	21	20	Reserved (must be set to 0)
23	22	21	Reserved (must be set to 0)
24	23	22	Page Mask for Fault Pin 3 (Byte 0 – LSB)
25	24	23	Page Mask for Fault Pin 3 (Byte 1)
26	25	24	Page Mask for Fault Pin 3 (Byte 2)
27	26	25	Reserved (must be set to 0)
28	27	26	Reserved (must be set to 0)
29	28	27	Reserved (must be set to 0)
30	29	28	Other Mask

10.1.1 Fault Pin Configuration

This byte configures which pin is used for fault pin and its polarity. For details, see Section 7. **Only open-drain mode and active low** configuration is allowed for this command, other modes cause this command to be rejected (received a NACK). Only pin id from 60 to 83 can be configured as fault pin.

If less than 4 fault pins are used, lower-number fault pins must be used first. For example, if only one fault pin is used, it must be Fault Pin 0; if only two fault pins are used, they must be Fault Pin 0 and 1; if only three fault pins are used, they must be Fault Pin 0, 1, and 2

10.1.2 Page Mask

The Page Mask consists of three configuration bytes. The bits are defined as follows:

Bit	23	22	21	20	19	18	17	16
Purpose	PAGE23	PAGE22	PAGE21	PAGE20	PAGE19	PAGE18	PAGE17	PAGE16
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Purpose	PAGE15	PAGE14	PAGE13	PAGE12	PAGE11	PAGE10	PAGE9	PAGE8
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Purpose	PAGE7	PAGE6	PAGE5	PAGE4	PAGE3	PAGE2	PAGE1	PAGE0

If a bit is set, any fault of the corresponding page (rail) will assert the fault pin. If a bit is cleared, the faults of the corresponding page (rail) has no effect on the fault pin output.

10.1.3 Other Mask

This mask determines the connections between fault pins and system watchdog fault (see SYSTEM_WATCHDOG_CONFIG command in Section 10.4) and re-sequence error. If a bit is set, the corresponding connection is enabled, meaning the fault/error will assert the fault pin.

Bit	7	6	5	4	3	2	1	0
Purpose	Re-Sequence Error	Re-Sequence Error	Re-Sequence Error	Re-Sequence Error	System WatchDog	System WatchDog	System WatchDog	System WatchDog
	Fault Pin3	Fault Pin2	Fault Pin1	Fault Pin0	Fault Pin 3	Fault Pin 2	Fault Pin 1	Fault Pin 0

10.2 (D1h) VOUT_CAL_MONITOR (MFR_SPECIFIC_01)

This Read/Write Word command is used to apply a fixed offset voltage to the output voltage measured by the device and reported by the READ_VOUT command. It is typically used by the PMBus device manufacturer to calibrate a device in the factory.

The VOUT_CAL_MONITOR has two data bytes formatted as a two's-complement binary integer. The effect on this command depends on the settings of the VOUT_MODE command.

10.3 (D2h) SYSTEM_RESET_CONFIG (MFR_SPECIFIC_02)

This Read/Write Block command configures the system reset function. The system reset function allows the device to provide an external reset signal to the system. This signal can be based on time, the power-good state of selected rails, the state of selected GPI pins, or a combination of these things. This ensures that key devices (for example, a CPU) are held in reset until other dependent devices (for example, peripherals) are fully powered. A reset pulse can also be generated as a result of a System Watchdog Timeout.

Table 29. SYSTEM_RESET_CONFIG Command Format Format (UCD90120 and UCD90124)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = D2
1	0		BYTE_COUNT = 4
2	1	0	Page Flags (high byte)
3	2	1	Page Flags (low byte)
4	3	2	**Bit** **Description** 7 Reserved 6 De-Assert When Power-Good 5 Assert When NOT Power-Good (not available with the UCD90120and UCD90124) 4 Assert When Watchdog Timeout 3:0 Delay Time
5	4	3	Reset Pin Configuration

Table 30. SYSTEM_RESET_CONFIG Command Format (UCD90910)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = D2
1	0		BYTE_COUNT = 6
2	1	0	Page Flags (high byte)
3	2	1	Page Flags (low byte)
4	3	2	GPI Flags
5	4	3	Delay Time
6	5	4	**Bit(s)** **Description** 7:3 Reserved 2 De-Assert When Power-Good 1 Assert When NOT Power-Good 0 Assert when Watchdog Timeout
7	6	5	Reset Pin Configuration

Table 31. SYSTEM_RESET_CONFIG Command Format (UCD90240)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = D2
1	0		BYTE_COUNT = 12
2	1	0	Page Flags – Byte 0 (LSB)
3	2	1	Page Flags – Byte 1
4	3	2	Page Flags – Byte 2
5	4	3	GPI Flags – Byte 0 (LSB)
6	5	4	GPI Flags – Byte 1
7	6	5	GPI Flags – Byte 2
8	7	6	Delay Time
9	8	7	Pulse Time

Table 31. SYSTEM_RESET_CONFIG Command Format (UCD90240) (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
10	9	8	**Bit(s) Description** 7:3 GPI Number 2 De-Assert When Power-Good 1 Assert When NOT Power-Good 0 Assert when Watchdog Timeout
11	10	9	GPI Tracking **Bit(s) Description** 7 Enable 6:5 Reserved 4 Watchdog Timeout Assertion Uses GPI Tracking Release Delay 3:0 GPI Tracking Release Delay (100 µs)
12	11	10	GPI Tracking Release Delay (1 ms)
13	12	11	Reset Pin Configuration

Table 32. SYSTEM_RESET_CONFIG Command Format (Devices Other Than the UCD90120, UCD90124, UCD90910, or UCD90240)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = D2
1	0		BYTE_COUNT = 9
2	1	0	Page Flags (high byte)
3	2	1	Page Flags (low byte)
4	3	2	GPI Flags
5	4	3	Delay Time
6	5	4	Pulse Time
7	6	5	**Bit(s) Description** 7:5 Reserved 4 Watchdog Timeout Assertion Uses GPI Tracking Release Delay 3 Reserved 2 De-Assert when Power-Good 1 Assert when NOT Power-Good 0 Assert when Watchdog Timeout
8	7	6	GPI Tracking **Bit(s) Description** 7 Enable 6:4 GPI Number 3:0 GPI Tracking Release Delay (100 µs)
9	8	7	GPI Tracking Release Delay (1 ms)
10	9	8	Reset Pin Configuration

10.3.1 GPI Flags

NOTE: This function is not available with the UCD90120 and UCD90124.

When “De-assert When Power-Good” is selected, the reset pin is de-asserted after the GPI pins identified by these bits reach the asserted state and then the Delay Time passes. (see the *GPI_CONFIG*)

When “Assert When NOT Power-Good” is selected, the reset pin is immediately asserted whenever the any of the GPI pins identified by these bits leaves the asserted state.

Bit	7	6	5	4	3	2	1	0
Purpose	GPI Z	GPI Y	GPI X	GPI W	GPI V	GPI U	GPI T	GPI S

Note: This table assumes that the device supports 8 GPIs (0 to 7). For a given device, this may not be the case. The interpretation of this information should be adjusted for the correct number of GPIs.

10.3.2 Page Flags

When the "De-assert When Power-Good" bit is set, the reset pin is de-asserted after the pages identified by these bits reach the power-good state and then the Delay Time passes.

For devices other than the UCD90120 and UCD90124: when the "Assert When NOT Power-Good" bit is selected, the reset pin is immediately asserted whenever the any of the pages identified by these bits leaves the power-good state.

Bit	7	6	5	4	3	2	1	0
Purpose	PAGE15	PAGE14	PAGE13	PAGE12	PAGE11	PAGE10	PAGE9	PAGE8

Bit	7	6	5	4	3	2	1	0
Purpose	PAGE7	PAGE6	PAGE5	PAGE4	PAGE3	PAGE2	PAGE1	PAGE0

Note: This table assumes that the device supports 16 rails (0 to 15). For a given device, this may not be the case. The interpretation of this information should be adjusted for the correct number of rails.

10.3.3 De-Assert When Power-Good

When this bit is set, the reset pin is de-asserted whenever the pages identified in the Page Flags reach power-good, the GPI pins identified by the GPI Flags are asserted, and then the time identified by the Delay Time expires.

The default state of the System Reset pin is Assert. When the System Reset function is configured in-circuit via PMBus commands during normal operation, the System Reset pin will briefly assert by default, even if conditions for de-assert are present. This is because the firmware requires a finite time to examine the de-assert conditions.

10.3.4 Assert When NOT Power-Good

Note: This function is not available with the UCD90120 and UCD90124.

When this bit is set, the reset pin is immediately asserted whenever any of the pages identified in the Page Flags leaves the power-good state or any of the GPI pins identified by the GPI Flags are de-asserted. Whenever the reset pin is asserted because of the “Assert when NOT Power-Good” function, the device attempts to de-asserted the reset pin based on the Delay Time or a combination of the power-good state of selected rails, the asserted state of selected GPIs, and the Delay Time. The Delay Time must be nonzero when this is the only enabled feature of the system reset function.

10.3.5 Assert When Watchdog Timeout

When this bit is set, a system watchdog timeout causes the reset pin to be asserted for the time identified by the Delay Time.

For devices other than the UCD90120 and UCD90124: If the “Watchdog Timeout Assertion Uses GPI Tracking Release Delay” bit is set, the GPI Tracking Release Delay is used instead of the Delay Time.

10.3.6 Delay Time

These bits define how long the reset pin is asserted.

Table 33. Delay Time Encoding (UCD90120 and UCD90124)

Encoding	Delay Time (seconds)
0000	0.001
0001	0.002
0010	0.004
0011	0.008
0100	0.016
0101	0.032
0110	0.064
0111	0.128
1000	0.256
1001	0.512
1010	1.024
1011	2.048
1100	4.096
1101	8.192
1110	16.384
1111	32.768

For devices other than the UCD90120 and UCD90124, this byte is formatted according the 8-bit time encoding defined in Section 2.5.

10.3.7 Pulse Time

When this byte is nonzero, the pulse feature is enabled and this byte defines how long the reset pin is de-asserted after the Delay Time has passed. This byte is formatted according the 8-bit time encoding defined in Section 2.5.

10.3.8 GPI Tracking

This function allows the system reset pin to be more precisely influenced by a specific GPI pin. (The GPI pin may be a reset signal from another device or a push button.) Whenever the GPI de-asserts, the system reset will immediately assert. When the GPI asserts, the system reset will be held asserted for the GPI Tracking Release Delay time. After this delay time, the system reset will be de-asserted. The system reset pin tracks the inverse of the GPI to allow the GPI to be used with the “De-Assert When Power-Good” function.

Table 34. GPI Tracking Configuration

Configuration Parameter	Description
Enable	This bit enables the GPI Tracking function.
GPI Number	These bits identify which one of the GPI pins will be tracked (see the GPI_CONFIG).
GPI Tracking Release Delay (100 µs)	These bits are multiplied by 100 µs and used as the higher precision portion of the GPI Tracking Delay.
GPI Tracking Release Delay (1 ms)	This byte is formatted according the 8-bit time encoding defined in Section 2.5.

The total GPI Tracking Release Delay time is the sum of the 100-µs resolution delay time and the 1-ms resolution delay time.

10.3.9 Reset Pin Configuration

This byte configures the reset pin (see Section 7).

10.4 (D3h) SYSTEM_WATCHDOG_CONFIG (MFR_SPECIFIC_03)

This Read/Write Block command configures the system watchdog function. When the watchdog function is enabled, a timeout counter runs continuously. The counter is reset when the watchdog input (WDI) pin is toggled or when the SYSTEM_WATCHDOG_RESET command is received. The counter time period is configured by the Reset Period byte. When the counter expires, the watchdog output (WDO) pin will be asserted. The output pin stays asserted until the watchdog input pin is toggled or until the SYSTEM_WATCHDOG_RESET command is received.

NOTE: The WDI and WDO are required with the UCD90120 and the UCD90124. With other devices, each of these pins is optional.

For devices other than UCD90240, the state of the watchdog input pin is only checked approximately every one millisecond. Therefore, a WDI pin state shorter than 2 ms may not be detected by the device. The minimum time-between-toggles on the watchdog input pin must be no less than two milliseconds.

Table 35. SYSTEM_WATCHDOG_CONFIG Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = D3
1	0		BYTE_COUNT = 4
2	1	0	**Bit Description** 7 Enable 6 Watch System Reset Pin 5 MaximimFan Speed With Timeout 4 Disable Until System Reset Release 3:0 Start Time
3	2	1	**UCD90120 and UCD90124:** **Bit Description** 7:5 Reserved 4:0 Input Pin (WDI) **All other devices:** Input Pin (WDI) Configuration
4	3	2	Reset Period
5	4	3	Output Pin (WDO) Configuration

10.4.1 Enable

This bit enables the system watchdog function.

10.4.2 Watch Reset Pin

When this bit is set, the System Reset pin (see SYSTEM_RESET_CONFIG, Section 10.3) influences the system watchdog timeout behavior. When the system reset pin is asserted, a watchdog timeout no longer occurs until the reset is de-asserted. Once it is de-asserted, the system watchdog function waits the Start Time before monitoring the Input Pin again.

10.4.3 MaximumFan Speed With Timeout

If this bit is set, all fans are set to the maximum speed when a watchdog timeout occurs.

Note: This only applies to UCD90124, UCD90124A, and UCD90910 devices.

10.4.4 Disable Until System Reset Release

When this bit is set, the System Watchdog Reset function will be temporarily disabled until the System Reset pin is de-asserted. This temporarily disabled state only applies when the device comes out of reset or when the System Watchdog Reset command is written.

NOTE: This bit is not available in UCD90120 and UCD90124.

10.4.5 Start Time

These bits identify the time to delay before monitoring the input pin.

Encoding	Start Time (Seconds)
0000	0
0001	0.1
0010	0.2
0011	0.4
0100	0.8
0101	1.6
0110	3.2
0111	6.4
1000	12.8
1001	25.6
1010	51.2
1011	102.4
1100	204.8
1101	409.6
1110	819.2
1111	1638.4

10.4.6 Input Pin (WDI) Configuration

This byte identifies the Input Pin, see Table 13, Table 14, and Table 15. The format of this byte is defined in Section 7.

All other devices: This byte configures the input pin (see Section 7).

10.4.7 Reset Period

The system watchdog's timeout counter must be reset within the period of time defined by this byte, else the output pin is asserted. Either of these actions resets the counter:

1. Toggle the watchdog Input Pin (WDI).
2. Write to the SYSTEM_WATCHDOG_RESET command.

UCD90120 and UCD90124: This byte defines the period from 0 to 2.55 seconds with a 10-millisecond resolution.

UCD90240: This byte is formatted according to Table 36. Bits 6 and 7 are the index for the multiplier field and Bits 0 to 5 are the mantissa (0x00 to 0x3F). The two are multiplied together to derive the time. A mantissa of 0 will result in a time of 0 regardless of the multiplier value.

Table 36. Reset Period Configuration for UCD90240

Multiplier Index	Multiplier (ms)	Resulting Range
b'00	1	0 to 63 ms
b'01	16	16 to 1008 ms
b'10	256	256 ms to 16.128 s
b'11	4096	4096 ms to b5200

All other devices: This byte is formatted according the 8-bit time encoding defined in Section 2.5.

Note: The system watchdog will not function as expected when the reset period is set to 0.

10.4.8 Output Pin (WDO) Configuration

This byte configures the output pin (see Section 7). This pin is asserted if the system watchdog's timeout counter does not receive reset signal or command within the time period defined by the Reset Period byte.

UCD90120 and UCD90124: Only Modes two and three (output modes) are valid (see Section 7). Any other mode results in command returning a NACK when it is written.

10.5 (D4h) SYSTEM_WATCHDOG_RESET (MFR_SPECIFIC_04)

This write-only, Send Byte command resets the system watchdog's timeout counter. This is the equivalent to toggling the system watchdog Input Pin (WDI).

10.6 (D5h) MONITOR_CONFIG (MFR_SPECIFIC_05)

The monitor pins can be configured individually for one of the various types of monitoring listed in Table 37 and Table 38. The command format is shown in Table 39. The Monitor Type and Page byte format is shown in Table 40.

The MONITOR_CONFIG write command configures all monitor pins in one command. The byte position in this command determines which monitor pin is being configured. The size of the write command is variable. The maximum size is determined by the number of monitor pins supported by a given device (see Table 41). The UCD90xxx NACKs the command if the size exceeds this number.

The MONITOR_CONFIG read command always returns information on all of the monitors in a given package. The number of monitors for each device is shown in Table 41.

Table 37. Monitor Types (Except UCD90240)

Monitor Type	Encoding
Not Assigned	0
Voltage	1
Temperature	2
Current	3
Voltage With Hardware Comparator	4
Invalid	5–7

Table 38. Monitor Types (UCD90240)

Monitor Type	Encoding
Not Assigned	0
Voltage	1
Temperature	2
Current	3
Voltage With Hardware Comparator	4
Input Voltage	5

Table 38. Monitor Types (UCD90240) (continued)

Monitor Type	Encoding
Voltage With AVS	6
Input Voltage With AVS	7

The Voltage With Hardware Comparator monitor type is the same as the Voltage monitor type, except that the response time to an over/undervoltage fault is faster with the hardware comparator. The hardware comparator option is only available with up to six monitored voltages. A few limitations are associated with using the hardware comparators:

- When a fault is detected by the hardware comparator, the only response is to shut down immediately – no glitch filtering, no retries. (Re-sequence may be selected.)
- When either the "Margin Low (Ignore Fault)" or the "Margin High (Ignore Fault)" option in the OPERATION command is selected, the over/undervoltage fault detection is disabled.
- This feature is not available for UCD90240.

Input Voltage monitor type is the same as Voltage monitor type, except that it is used to monitor input voltage instead of output voltage. This type is only available in UCD90240. When a rail is configured as Input Voltage monitor type, the POWER_GOOD_OFF and VOUT_UV_FAULT_LIMIT threshold should be set to the same value, otherwise the function may not work correctly. When the monitored input voltage is below POWER_GOOD_OFF(VOUT_UV_FAULT_LIMIT), a graceful shutdown process will begin: the Vin UV fault will be recorded in NV memory with a time stamp; and the subsequent UV and UC faults and warnings from all downstream rails will be ignored. If the downstream rails are set by the Fault Slave Mask in the SEQ_CONFIG command (see Section 10.38). It is recommended to use a high number rail as Input Voltage monitor. During the graceful shutdown period, other faults from all downstream rails are still logged as normal. When the monitored input voltage rises above POWER_GOOD_ON, the graceful shutdown is cancelled.

Voltage with AVS monitor type is the same as voltage monitor type, except that it supports setting the warning and fault limits by a fixed percentage of the nominal voltages. This type is only available on UCD90240.

Due to the fact that the power supply and UCD90240 may not change Vout setpoint simultaneously or with the same slew rate, UCD90240 will take the following steps to avoid false-triggering warn/fault. If the new VOUT setpoint is higher than the current VOUT setpoint, the OV warn/fault thresholds will be immediately set to their respective new levels; other thresholds will increase by 20-mV step size in every 500 µs until the new levels are reached. If the new VOUT setpoint is lower than the current VOUT setpoint, the UV warn/fault and Power Good On/Off thresholds will be immediately set to their respective new levels; other thresholds will decrease by 20-mV step size in every 500 µs until the new levels are reached. The PMBus host should update VOUT setpoint in sequencer prior that in power stage controller to avoid false-trigger.

Input Voltage with AVS monitor type is the combination of the Input Voltage and Voltage with AVS monitor type. This type is only available in UCD90240.

NOTE: The Hardware Comparator function is not enabled until the rail is turned on and reaches the power-good state. If hardware comparator is configured while the rail is already in the power-good state, it will not take effect until the rails is powered down and powered up again.

NOTE: When a MON pin is Voltage With Hardware Comparator monitor type, do not use the “continue to operate” voltage fault response in either of VOUT_OV_FAULT_RESPONSE or VOUT_UV_FAULT_RESPONSE (see the Operation bit in Table 41). The device may not function properly in such a configuration.

Table 39. MONITOR_CONFIG Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = D5
1	0		BYTE_COUNT = N
2	1	0	Monitor 1 Type and Page
3	2	1	Monitor 2 Type and Page
4	3	2	Monitor 3 Type and Page
↓	↓	↓	↓
N+1	N	N	Monitor N Type and Page

Table 40. Monitor Type and Page Byte

Bits	7:5	4:0
Definition	Monitor Type (see Table 37 and Table 38)	Monitor Page Number UCD90240: 0-23 UCD9012x: 0-11 UCD90910: 0-11 UCD9160x: 0-15 UCD9090: 0-9

The status of the monitor pin can be read with the appropriate read command (READ_VOUT, READ_TEMPERATURE_2, READ_IOUT). The state of these monitor pins are also used to capture and report faults and warnings.

The number of monitor pins varies based on the device. Table 41 shows what is available for each device. This means that the UCD9012x has 13 monitors available. Any attempt to use a monitor number that is not available on a given device (denoted by "*Error*" in the table) results in a NACK to the MONITOR_CONFIG write command.

Table 41. Monitor Pin Definitions

Monitor ID	Pin Numbers			
	UCD9012x and UCD90910	UCD90160	UCD9090	UCD90240
1	1	1	1	E2
2	2	2	2	E1
3	3	3	38	F2
4	4	4	39	F1
5	5	5	40	B3
6	6	6	41	A3
7	59	55	42	B4
8	62	56	45	A4
9	63	57	46	B5
10	50	58	48	A5
11	52	59	37	B6
12	54	62	*Error*	A6
13	56	63	*Error*	C1
14	*Error*	50	*Error*	C2
15	*Error*	52	*Error*	B1
16	*Error*	54	*Error*	B2
17-	*Error*	*Error*	*Error*	G2
18	*Error*	*Error*	*Error*	G1

Table 41. Monitor Pin Definitions (continued)

Monitor ID	Pin Numbers			
	UCD9012x and UCD90910	UCD90160	UCD9090	UCD90240
19	*Error*	*Error*	*Error*	H1
20	*Error*	*Error*	*Error*	H2
21	*Error*	*Error*	*Error*	B7
22	*Error*	*Error*	*Error*	A7
23	*Error*	*Error*	*Error*	B8
24	*Error*	*Error*	*Error*	A8

The monitors shaded in grey (Example: monitor 12 for the UCD9012x) have a minor limitation on the lower range of monitoring – they can not detect voltage below 0.2 volt. Anything below that is reported as 0.2 volts.

10.7 (D6h) NUM_PAGES (MFR_SPECIFIC_06)

This read-only, byte command returns the number of active pages. This value is determined by the MONITOR_CONFIG and SEQ_CONFIG commands (see Section 10.6 and Section 10.38). It is the higher page number derived from these two evaluations:

- The highest number page that has an enable pin assigned to it. (SEQ_CONFIG)
- The highest number page that has a monitor pin assigned to it. (MONITOR_CONFIG)

10.8 (D7h) RUN_TIME_CLOCK (MFR_SPECIFIC_07)

This command returns the run-time clock value. It is given in milliseconds and days. Both are 32-bit numbers. The run-time clock may also be written. This allows the clock to be periodically corrected by the host. It also allows the clock to be initialized to the actual, absolute time in years (for example, March 23, 2010). The user must translate the absolute time to days and milliseconds.

NOTE: The *run-time* includes only normal operation time. Neither *boot time* or *device initialization time* is included in run-time. Only the UCD90124A, UCD9090A and UCD90160A offer the ability to preserve the real-time clock when brownout mode is enabled. All other UCD devices (except UCD90240) in this family reset the real-time clock to zero (0) even when brownout mode is enabled.

The three usage scenarios for the run-time clock are:

1. Time from restart (reset or power-on): the run-time clock starts from zero (0) each time the device is powered on.
2. Local time: an external processor sets the run-time clock to real-world time each time the device is restarted.
3. Absolute run-time, or alive time: the run-time clock is preserved across power-cycles, so you can keep up with the total time that the device has been in operation. In order to do this, the run-time clock must be saved when a power-down condition is detected. This means that the brownout mode feature must be enabled in this scenario (see brownout enable mode in MISC_CONFIG, this feature is not available for UCD90240).

For UCD90240, after each device reset, the latest time stamp of all fault logs and peak logs is used to resume the run-time clock. The run-time clock value is used to time-stamp any faults that are logged (see Section 10.28).

Table 42. RUN_TIME_CLOCK Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = D7
1	0		BYTE_COUNT = 8
2	1	0	Milliseconds (high byte)
3	2	1	Milliseconds
4	3	2	Milliseconds
5	4	3	Milliseconds (low byte)
6	5	4	Days (high byte)
7	6	5	Days
8	7	6	Days
9	8	7	Days (low byte)

10.9 (D8h) RUN_TIME_CLOCK_TRIM (MFR_SPECIFIC_08)

This command has two data bytes formatted in the Linear11 Data format. The value represents clock speed adjustment in percentage. The default value is 0.0%. Typical values are likely to be in the range from –2% to +2%. The command allows values from –100% to +99.9%. If the value returned from the RUN_TIME_CLOCK command (see Section 10.8) is too slow, a negative percentage value will correct it. If the run-time clock is too fast, a positive percentage value will correct it. This command is not supported by UCD90240.

10.10 (D9h) ROM_MODE (MFR_SPECIFIC_09)

This Send Byte command sends the system into ROM mode. Issue this command before attempting to download new firmware to the device. After this command is received, the device takes approximately 50 milliseconds to enter ROM mode and become responsive to subsequent commands. For UCD90240, this command does nothing.

10.10.1 ROM, PFlash, and Integrity

After a reset or power-up, the UCD90xxx device starts executing a boot loader algorithm stored in ROM. This boot loader supports a small set of specialty commands (not listed in this document) to allow device to test and update the firmware in Program Flash. After performing a few simple wakeup diagnostics, the boot ROM scans the Program Flash to validate its integrity. If the integrity is good, the processor reconfigures itself to disable the ROM and execute from Program Flash.

When a ROM_MODE or SOFT_RESET (see Section 10.12) command is issued, the processor will be reset. For a SOFT_RESET command, the Program Flash Integrity test will be performed, and if successful, the Program Flash firmware will start to execute automatically.

The ROM_MODE command, on the other hand, will erase the Program Flash Integrity Word (PFlash Checksum) before resetting the processor. Once the Integrity Word is erased, the Program Flash Integrity test will not pass, and thus the device will stay in ROM mode. In this case, Fusion Digital Power tools must be used to reload the Program Flash firmware or repair the PFlash Checksum. Until then, the existing flash firmware may only be executed by issuing the EXECUTE_FLASH command (see Section 10.32).

10.11 (DAh) USER_RAM_00 (MFR_SPECIFIC_10)

This Read/Write Byte command allows the user to read/write a byte value into a RAM location of the device. This RAM value is reset to a known value (0) when the device is reset. By monitoring this value, the user is able to tell whether the device has been reset during operation.

Note that this parameter is not stored to nonvolatile Default Store memory when the STORE_DEFAULT_ALL command is issued.

10.12 (DBh) SOFT_RESET (MFR_SPECIFIC_11)

This Write-Only Send Byte command restarts the controller firmware. Any active voltage outputs are turned off before the firmware restarts.

This is the same as the ROM_MODE command except that it does not ease the Program Flash Integrity Word. See Section 10.6 for details about ROM and the Program Flash Integrity Word.

10.13 (DCh) RESET_COUNT (MFR_SPECIFIC_12)

This Read/Write Byte command allows the user to track how many times the device has been reset. In a device that has not been configured, this value is zero and the number of resets is not tracked . To enable this feature, the value must be changed to a non-zero value and the device must be reset. After that, this value will be incremented each time the device is restarted (reset or power-on) and completes the start-up sequence.

If the brownout mode feature is not enabled (see brownout enable mode in MISC_CONFIG Section 10.44) and this feature is enabled, the reset count will be updated in data flash each time the device is restarted. If the brownout mode feature is enabled, the reset count is written to data flash before power-down. This lowers the number of times that the flash is written.

NOTE: **UCD90120A, UCD90124A, UCD9090, and UCD90160:** If the reset count exceeds the maximum value (65535), it will be set to zero which disables this function.

UCD90120, UCD90124, and UCD90910: This is a Read/Write byte command. If the reset count exceeds the maximum value (255), it will be set to zero and began counting again from there. This roll over can occur 255 times. When the count rolls over the 256th time, the count will remain zero and this function will be disabled.

10.14 (DDh) PIN_SELECTED_RAIL_STATES (MFR_SPECIFIC_13)

This Read Byte Block command allows use to configure up to 3 GPI pins to control the state of all the rails (up to 8 system states). This function can be used to put the system into a low power mode, for example. In each system state, the user will define which rails are on and which rails are off. If a new state is presented on the GPI, and a rail is required to change state, it will do so according to its startup or shutdown dependencies – all changes are done with full sequencing functionality.

NOTE: The Pin Selected Rail States function is implemented by modifying OPERATION command. Therefore, in order to use this function to control rail states, the related rails must be configured to use OPERATION command in ON_OFF CONFIG.

Whenever the device is reset, these pins will be sampled and used to update the system state, if the function is enabled.

Table 43. Changes to the OPERATION Command

New State	Soft Off Enable	OPERATION Command
On	n/a	0x80
Off	0	0x00
Off	1	0x40

The first 3 pins configured with the GPI_CONFIG command (see Section 10.41) can be used to select 1 of 8 system states.

Table 44. GPI Selection of System States

GPI 2 State	GPI 1 State	GPI 0 State	System State
NOT Asserted	NOT Asserted	NOT Asserted	0
NOT Asserted	NOT Asserted	Asserted	1
NOT Asserted	Asserted	NOT Asserted	2
NOT Asserted	Asserted	Asserted	3
Asserted	NOT Asserted	NOT Asserted	4
Asserted	NOT Asserted	Asserted	5
Asserted	Asserted	NOT Asserted	6
Asserted	Asserted	Asserted	7

NOTE: When selecting a new System State, changes to the status of the GPI pins must not take longer than 1 microsecond.

Table 45. PIN_SELECTED_RAIL_STATES Command Format (UCD90240)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = DD
1	0		BYTE_COUNT = 26
2	1	0	System State Enables
3	2	1	Soft Off Enables
4	3	2	System State 0 (Byte 0 – LSB)
5	4	3	System State 0 (Byte 1)
6	5	4	System State 0 (Byte 2)
7	6	5	System State 1 (Byte 0 – LSB)
8	7	6	System State 1 (Byte 1)
9	8	7	System State 1 (Byte 2)
10	9	8	System State 2 (Byte 0 – LSB)
11	10	9	System State 2 (Byte 1)
12	11	10	System State 2 (Byte 2)
13	12	11	System State 3 (Byte 0 – LSB)
14	13	12	System State 3 (Byte 1)
15	14	13	System State 3 (Byte 2)
16	15	14	System State 4 (Byte 0 – LSB)
17	16	15	System State 4 (Byte 1)
18	17	16	System State 4 (Byte 2)
19	18	17	System State 5 (Byte 0 – LSB)
20	19	18	System State 5 (Byte 1)
21	20	19	System State 5 (Byte 2)
22	21	20	System State 6 (Byte 0 – LSB)
23	22	21	System State 6 (Byte 1)
24	23	22	System State 6 (Byte 2)
25	24	23	System State 7 (Byte 0 – LSB)
26	25	24	System State 7 (Byte 1)
27	26	25	System State 7 (Byte 2)

Table 46. PIN_SELECTED_RAIL_STATES Command Format (Devices Other Than UCD90240)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = DD
1	0		BYTE_COUNT = 18
2	1	0	System State Enables
3	2	1	Soft Off Enables
4	3	2	System State 0 (high byte)
5	4	3	System State 0 (low byte)
6	5	4	System State 1 (high byte)
7	6	5	System State 1 (low byte)
8	7	6	System State 2 (high byte)
9	8	7	System State 2 (low byte)
10	9	8	System State 3 (high byte)
11	10	9	System State 3 (low byte)
12	11	10	System State 4 (high byte)
13	12	11	System State 4 (low byte)
14	13	12	System State 5 (high byte)
15	14	13	System State 5 (low byte)
16	15	14	System State 6 (high byte)
17	16	15	System State 6 (low byte)
18	17	16	System State 7 (high byte)
19	18	17	System State 7 (low byte)

10.14.1 System State Enables

Each bit in the System State Enables byte is used to enable or disable one of the 8 System States.

Bit	7	6	5	4	3	2	1	0
Purpose	System State 7 Enable	System State 6 Enable	System State 5 Enable	System State 4 Enable	System State 3 Enable	System State 2 Enable	System State 1 Enable	System State 0 Enable

10.14.2 Soft Off Enables

Each bit in the Soft Off Enables byte determines how to turn off (1-soft off or 0-immediate) any rails commanded to turn off by the associated System State.

Bit	7	6	5	4	3	2	1	0
Purpose	System State 7 Soft Off Enable	System State 6 Soft Off Enable	System State 5 Soft Off Enable	System State 4 Soft Off Enable	System State 3 Soft Off Enable	System State 2 Soft Off Enable	System State 1 Soft Off Enable	System State 0 Soft Off Enable

10.14.3 System State

The bits in the System State bytes determine if a rail should change states or not (1-on or 0-off).

Bit	15	14	13	12	11	10	9	8
Purpose	PAGE15 ON/OFF	PAGE14 ON/OFF	PAGE13 ON/OFF	PAGE12 ON/OFF	PAGE11 ON/OFF	PAGE10 ON/OFF	PAGE9 ON/OFF	PAGE8 ON/OFF
Bit	7	6	5	4	3	2	1	0
Purpose	PAGE7 ON/OFF	PAGE6 ON/OFF	PAGE5 ON/OFF	PAGE4 ON/OFF	PAGE3 ON/OFF	PAGE2 ON/OFF	PAGE1 ON/OFF	PAGE0 ON/OFF

NOTE: This table assumes that the device supports 16 rails (0 to 15). For a given device, this may not be the case. The interpretation of this information should be adjusted for the correct number of rails.

10.15 (DEh) RESEQUENCE (MFR_SPECIFIC_14)

This Write Word command is used to command specific rails to resequence. If a rail is commanded to resequence, it will first perform a soft off. After all of the rails that have been commanded to resequence are turned off (the voltage has fallen below POWER_GOOD_OFF), there will be a delay before the rails are commanded to turn back on. The delay is defined by the “Time between Resequences” byte in the MISC_CONFIG command (Section 10.44). After the delay, the rails will turn on according to any dependencies and/or TON_DELAY.

The bits in the two bytes that make up this command determine if a rail should resequence or not (1-yes or 0-no).

Bit	15	14	13	12	11	10	9	8
Purpose	PAGE15	PAGE14	PAGE13	PAGE12	PAGE11	PAGE10	PAGE9	PAGE8
Bit	7	6	5	4	3	2	1	0
Purpose	PAGE7	PAGE6	PAGE5	PAGE4	PAGE3	PAGE2	PAGE1	PAGE0

Note: This table assumes that the device supports 16 rails (0 to 15). For a given device, this may not be the case. The interpretation of this information should be adjusted for the correct number of rails.

Note: UCD90240 does not support this command.

10.16 (DFh) CONSTANTS (MFR_SPECIFIC_15)

This Read Byte Block command provides fixed information about the device.

Table 47. CONSTANTS Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = DF
1	0		BYTE_COUNT = 8
2	1	0	Maximum Number of Digital Comparators
3	2	1	Maximum Number of General-Purpose Outputs (GPOs)
4	3	2	Maximum Number of General-Purpose Inputs (GPIs)
5	4	3	Maximum Number of Pages
6	5	4	Maximum Number of Fans
7	6	5	Maximum Number of Monitors
8	7	6	Maximum Number of Entries in the Logged Fault Detail (see LOGGED_FAULT_DETAIL)
9	8	7	Maximum Number of PWM outputs

Table 48. CONSTANTS for Each Device

Constant	90120	90120A	90124	90124A	9090	90160	90910	90240
Digital Comparators	6	6	6	6	6	6	6	0
GPOs	12	12	12	12	10	16	10	12
GPIs	8	8	8	8	8	8	8	24
Pages	12	12	12	12	10	16	10	24
Fans	0	0	4	4	0	0	10	0
Monitors	13	13	13	13	11	16	13	24
Logged Fault Detail Entries	16	16	10	12	30	18	12	100
PWM outputs	12	12	12	12	10	12	12	24

10.17 (E0h) PWM_SELECT (MFR_SPECIFIC_16)

This Read/Write Byte command determines which PWM that the PWM_CONFIG command applies to. The value given here must be a valid Pin ID.

Table 49. Valid PWM Pin IDs

Device	Valid Pin IDs	Details
UCD9012, UCD90160x, and UCD90910	0-11	See Table 14
UCD9090	0-9	See Table 15
UCD90240	0-23	See Table 12

10.18 (E1h) PWM_CONFIG (MFR_SPECIFIC_17)

This Read/Write Byte command configures the PWM identified by the PWM_SELECT command. The duty cycle is in LINEAR11 format and valid values are between 0 and 100 (%). Frequency is an unformatted, 32-bit value. See Section 8 for more information about configuring the PWM frequency. The Phase is in LINEAR11 format and valid values are less than 360 (degrees) and greater than or equal to 0. Attempts to write invalid values to this command will result in a NACK. To unconfigure a PWM, set the frequency to zero, issue a STORE_DEFAULTS_ALL command, and reset the device.

Table 50. PWM_CONFIG Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = E1
1	0		BYTE_COUNT = 8
2	1	0	Duty Cycle (High Byte)
3	2	1	Duty Cycle (Low Byte)
4	3	2	Frequency (High Byte)
5	4	3	Frequency
6	5	4	Frequency
7	6	5	Frequency (Low Byte)
8	7	6	Phase (High Byte)(1)
9	8	7	Phase (Low Byte)(1)

(1) The Phase field only applies to the FPWM pins. The phase field must be set to zero for the non-FPWM pins.

NOTE: **Other than UCD90240:** For the best accuracy when phase shifting, the frequencies used should be the same or a harmonic of each other. Due to how the PWM signals are derived from a 250MHz clock, not all harmonic values can actually be synchronized. There is a simple test to check if they can be. Using division with truncation (no rounding), 250MHz divided by frequency A must be divisible by 250MHz divided by frequency B, where frequency A is greater than frequency B.

UCD90240 does not support Phase configuration.

10.19 (E2h) PARM_INFO (MFR_SPECIFIC_18)

This Read/Write Block command is used to configure the parameters used by the PARM_VALUE command.

The PARM_INFO command updates four variables that are needed to issue a generic read/write of RAM or hardware registers, and so forth. The four variables are parm_index, parm_offset, parm_count, and parm_size.

Their descriptions follow:

Parm_index – Index for base address
- 0 = RAM
- 1 = Hardware Peripherals
- 2 = Constants in Data Flash (Read Only, unless unlocked)
- 3 = Constants in Program Flash (Read Only)
- 4 = Data Flash Control Registers
- 5 = EEPROM (Read only, with Parm_size = 4 only)

Parm_offset – offset from the base address selected by parm_base.

Parm_count – number of elements to read or write

Parm_size – the size of each element in bytes. (Valid values are 1, 2, or 4).

PARM_INFO and PARM_VALUE are combined to provide a method for reading or writing to any RAM address or hardware register. A map file specific to the firmware release may be required to determine the offset for a particular RAM variable, because variables may be in different locations for each release.

Table 51. PARM_INFO Command Format (other than UCD90240)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = E2
1	0		BYTE_COUNT = 5
2	1	0	Index
3	2	1	Offset low byte
4	3	2	Offset high byte
5	4	3	Count
6	5	4	Size

Table 52. PARM_INFO Command Format (UCD90240 only)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = E2
1	0		BYTE_COUNT = 6
2	1	0	Index

Table 52. PARM_INFO Command Format (UCD90240 only) (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
3	2	1	Offset (low byte)
4	3	2	Offset (middle byte)
5	4	3	Offset (high byte)
6	5	4	Count
7	6	5	Size

10.20 (E3h) PARM_VALUE (MFR_SPECIFIC_19)

This Read/Write Block command is used to read and write to RAM addresses or hardware peripheral registers. This command assumes that the PARM_INFO command has be previously run to set up the parm_base, parm_offset, parm_count, and parm_size variables as needed.

10.21 (E4h) TEMPERATURE_CAL_GAIN (MFR_SPECIFIC_20)

This Read/Write Word command sets the gain calibration for the external sensors used by the READ_TEMPERATURE_2 command. Each external temperature sensor (typically one per power output rail) has its own calibration setting.

This command has two data bytes formatted in the Linear11 Data format. The units are Celsius degrees per volt.

10.22 (E5h) TEMPERATURE_CAL_OFFSET (MFR_SPECIFIC_21)

This Read/Write Word command sets the offset calibration for the external sensors used by the READ_TEMPERATURE_2 command. Each external temperature sensor (typically one per power output rail) has its own calibration setting.

This command has two data bytes formatted in the Linear11 Data format. The units are degrees Celsius.

10.23 (E7h) FAN_CONFIG_INDEX (MFR_SPECIFIC_23)

The value here determines to which fan that the FAN_CONFIG_N command applies.

Table 53. Relationship Between FAN_CONFIG_INDEX and the Actual Fan Number

FAN_CONFIG_INDEX	Fan
0	1
1	2
2	3
3	4

Note for versions with more than four fans: When more than four fans are supported, the FAN_CONFIG_INDEX also applies to these commands:

- FAN_COMMAND_1
- READ_FAN_SPEED_1

10.24 (E8h) FAN_CONFIG (MFR_SPECIFIC_24)

The command is used for advanced configuration of the fan specified by the FAN_CONFIG_INDEX command. Some basic configuration of the fan is always required (for example, identification of the tach and/or fan control pins).

Table 54. FAN_CONFIG Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = E8
1	0		BYTE_COUNT = 21
2	1	0	**Bit** **Description** 7:5 Speed change 4:0 Control pin
3	2	1	**Bit** **Description** 7 System shutdown enable 6:5 Fan Failure Count 4:0 Tach pin
4	3	2	**Bit** **Description** 7 PWM enable(1) 6 Invert PWM 5 Enable pin polarity 4 Tach enable 3:0 Temperature Sensor
5	4	3	**Bit** **Description** 7 Fan on 6 Auto-calibration in progress 5 Speed type 4 Auto-adjust enable 3 Auto-calibrate enable 2:1 Tach pulses per revolution 0 Fan is installed
6	5	4	Temperature level 1/Temperature off
7	6	5	Temperature level 2/Temperature on
8	7	6	Temperature level 3
9	8	7	Temperature level 4
10	9	8	Temperature level 5
11	10	9	Speed 1 - below temperature level 1

(1) If the PWM Enable bit is set, the associated PWM_CONFIG command must be written before the FAN_CONFIG command is written.

Table 54. FAN_CONFIG Command Format (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
12	11	10	Speed 2 - between temperature level 1 and 2
13	12	11	Speed 3 - between temperature level 2 and 3
14	13	12	Speed 4 - between temperature level 3 and 4
15	14	13	Speed 5 - between temperature level 4 and 5
16	15	14	Speed 6 - above temperature level 5
17	16	15	Fault increase speed
18	17	16	Speed fault limit (high byte)
19	18	17	Speed fault limit (low byte)
20	19	18	Duty cycle on
21	20	19	Duty cycle off
22	21	20	Duty cycle max

Table 55. FAN_CONFIG Configuration Parameters

Parameter Name	Description
Speed change	When the fan gets a new speed setting (manually or automatically adjusted), this is the percentage change in speed per second.
	b'000 – 0.125% b'001 – 0.25% b'010 – 0.5% b'011 – 1% (default) b'100 – 2% b'101 – 4% b'110 – 8% b'111 – Apply new speed immediately **Note:** The UCD90910 changes speed twice as fast as the values given here. For example, when this "speed change" value is set to b'010, the fan speed changes 1% per second.
Control pin	This value identifies the control pin to use with this fan. The value must be a "Pin ID" from Table 14 or Table 15. If the fan is to be controlled with a PWM signal ("PWM enable" bit set to 1), then only values corresponding to PWM pins are valid. The frequency for the PWM is configured with the PWM_CONFIG command (see Section 8).
System shutdown enable	The system shuts down (all rails are turned off) when this fan has failed, and the number of additional fans indicated by "Fan Failure Count" also has failed. TOFF_DELAY is applied when turning off each rail.
Fan Failure Count	The number of other fan failures (0-3) that causes the system to shut down if the "System shutdown enable" is set.
Tach pin	This value identifies the Tach pin to use with this fan. The value is a "Pin ID" from Table 14 or Table 15.
PWM enable	Setting this bit to one configures the control pin to the fan to use a variable duty cycle PWM signal. When set to zero, the control pin to the fan is a simple enable/disable signal. 0 – simple enable/disable 1 – variable PWM signal
Invert PWM	Setting this bit to one causes the duty cycle on the PWM to be inverted. So, a duty cycle of 100 becomes 0, 0 becomes 100, 40 becomes 60, and so on.
Enable pin polarity	When the control pin to the fan (identified by the "Control pin" parameter) is simply a enable/disable (not a PWM signal, "PWM enable" is set to 0), this bit determines the polarity of the control signal to the fan. 0 – Active Low 1 – Active High
Tach enable	Set to one if the fan has a tach output, and the "Tach pin" parameter has been configured. Else, set this to zero.
Temperature Sensor	If the auto-adjust function is enabled, this parameter identifies the page for the temperature sensor that is to be used with this fan.
Fan on	The status of the fan: 0 – off 1 – on (Read Only)
Auto-calibration in progress	This bit is set to one while the auto-calibration function is being performed. It is cleared once that function is complete. (Read Only)

Table 55. FAN_CONFIG Configuration Parameters (continued)

<table>
<tr><th>Parameter Name</th><th>Description</th></tr>
<tr><td>Speed type</td><td>Determines how the “Speed” parameter is used:
0 – The “Speed” parameter determines the percent duty cycle for the PWM signal to the fan.
1 – The “Speed” parameter sets the percent operating speed to the fan. At 1%, the fan runs at its slowest speed (“Duty cycle off”). At 100%, the fan runs at its fastest speed (“Duty cycle max”).</td></tr>
<tr><td>Auto-adjust enable</td><td>When this bit is set, the fan speed automatically is adjusted as the temperature changes. This function is only available when the “PWM enable” parameter is set to one and a “Temperature Sensor” is associated with this fan.</td></tr>
<tr><td>Auto-calibrate enable</td><td>When this bit is first set to one, the firmware varies the duty cycle to the fan to determine the fan's actual operating range (“Duty cycle on”, “Duty cycle off”, and “Duty cycle max”).
This process may take a couple of minutes. The “Duty cycle on” parameter can be set at the duty cycle to start from to help speed this up.
This function is only available when the “PWM enable” parameter is set to one and a “Temperature Sensor” is associated with this fan.</td></tr>
<tr><td>Tach pulses per revolution</td><td>The number of tach pulses that the fan generates per revolution.
00b = 1 pulse per revolution
01b = 2 pulses per revolution
10b = 3 pulses per revolution
11b = 4 pulses per revolution</td></tr>
<tr><td>Fan is installed</td><td>Set to one if a fan is installed in this position.</td></tr>
<tr><td>Temperature Levels 1–5</td><td>When the “Auto-adjust enable” bit is set, these temperatures (signed integer, –128°C to 127°C) determine the speed of the fan. This table shows how the speed is selected based on the current temperature (see the Temperature Sensor bit field).
<table>
<tr><th>Temperature</th><th>Speed</th></tr>
<tr><td>below temperature level 1</td><td>1</td></tr>
<tr><td>between temperature level 1 and 2</td><td>2</td></tr>
<tr><td>between temperature level 2 and 3</td><td>3</td></tr>
<tr><td>between temperature level 3 and 4</td><td>4</td></tr>
<tr><td>between temperature level 4 and 5</td><td>5</td></tr>
<tr><td>above temperature level 5</td><td>6</td></tr>
</table>
Note: The temperature and speed values must be listed in increasing order.
Temperature Level 1 and Temperature Level 2 act as “Temperature Off” and “Temperature On” when a simple enable/disable signal is used to control the fan instead of a PWM signal.</td></tr>
<tr><td>Speed 1-6</td><td>When the “Auto-adjust enable” bit is set, the current temperature is used with these values (0-100%) to set the fan speed. (see the “Speed type” parameter.)</td></tr>
<tr><td>Fault increase speed</td><td>When this fan fails, the other fans’ speeds (1-6) are incremented by this amount (0-100%). Speeds currently set to zero are not be modified. A ceiling of 100% is placed on the result of the speed increase. This function is only done when the "Auto-adjust enable” bit is set.
This function is only meaningful when the “Auto-adjust enable” bit is set.
UCD90124: When the value here is nonzero and the fan fails, the "Fan is installed" bit is set to zero, and the only way to get the fan to running again is to restart the UCD90xxx.
Other devices with fan support: When the value here is nonzero and the fan fails, the "Fault increase speed" bit is set to 0 and the other fan speeds are increased. This prevents this function from occurring a second time if the fan comes back on and then fails again.</td></tr>
<tr><td>Speed fault limit</td><td>This Read/Write Word command specifies the speed (RPM in Linear11 format) at which the fan speed control reports a fault. If the fan speed is below this limit for 5 consecutive seconds, the controller asserts the PMBus ALERT signal and sets the fault bits in the STATUS_FANS_1_2 or STATUS_FANS_3_4 and STATUS_WORD registers.
No faults are logged when the speed fault limit is set to zero.
Note: When a “speed fault” is first detected and you are operating in auto-adjust mode, the fan speed is set to the “Duty cycle on” level in an attempt to restart the fan. This keeps a fault from being logged when the fan is starting from the off position. During the time when the duty cycle is stepping up from that state, the fan is likely off long enough so that a fault appears to have occurred. This allows the fan to turn on at “Duty cycle on” speed and not cause a fault. This behavior may also correct stalls that may occur between the “Duty cycle on” and “Duty cycle off” levels.</td></tr>
</table>

Table 55. FAN_CONFIG Configuration Parameters (continued)

Parameter Name	Description
Duty cycle on	This value is set to the percent duty cycle where the fan turns on. (unsigned integer, 0-100%) When the “Auto-calibrate enable” bit is set, firmware calculates this value. A value close to and just below the duty cycle where the fan starts may be passed in to help speed up the Auto-calibrate process. If the “Auto-calibrate enable” bit is not set, this parameter can be passed in.
Duty cycle off	Given the fan is running, this is the percent duty cycle where the fan turns off. This is used as the lowest duty cycle that is ever applied to the fan (unsigned integer, 0-100%) When the “Auto-calibrate enable” bit is set, firmware calculates this value. If the “Auto-calibrate enable” bit is not set, this parameter can be passed in.
Duty cycle max	This is the percent duty cycle where the fan is at its maximum RPM. (unsigned integer, 0-100%) When the “Auto-calibrate enable” bit is set, firmware calculates this value. If the “Auto-calibrate enable” bit is not set, this parameter can be passed in.

10.24.1 Auto-Calibration Function

This function determines the actual operating range of the fan. The following outlines how that is done.

1. If the fan is running, wait for it to stop. If the fan does not stop after 6 seconds, assume that it never stops when powered, and begin the auto-calibration function.
2. Start the duty cycle at the "Duty cycle on" set by the user. (This must be set to some value that is known to be below the duty cycle where the fan turns on. If the user is uncertain about that value, use a value of 0.)
3. Increment the duty cycle by 1% every two seconds until the fan turns on
4. Record the "Duty cycle on".
5. Set the duty cycle to 100%.
6. Bring the duty cycle down by 5% every two seconds until there is a ≈1% difference in speed than what was seen at 100%.
7. Increment the duty cycle by 1% every two seconds until the fan speed stops increasing two sample times in a row.
8. Record the "Duty cycle max".
9. Set the duty cycle to "Duty cycle on".
10. Decrement the duty cycle by 1% every four seconds until the fan turns off.
11. Add 2% to the lowest duty cycle before the fan turned off, and record it as the "Duty cycle off".

NOTE: If the fan never comes on during this process, the Fan Fault bit in the STATUS_FAN_#_# command is set and the PMBus ALERT signal is asserted.

10.24.2 Control Pin Selection

Table 56 shows how to determine what type of control pin (PWM, simple enable/disable) is being used. Table 57 points out the types of fan control that are supported.

Table 56. Control Pin Selection

PWM Enable Bit	Auto-Adjust Enable Bit	Control Pin Type
0	0	None
0	1	Simple enable/disable
1	0	PWM
1	1	PWM

Table 57. Types of Fan Control

Type of Fan Control	PWM Enable Bit	Auto-Adjust Enable Bit
No fan control	0	0
Simple enable, auto adjust mode	0	1
Simple enable, manual fan control	Not Supported	
PWM, manual fan control	1	0
PWM, auto adjust mode	1	1

10.25 (E9h) FAULT_RESPONSES (MFR_SPECIFIC_25)

This paged, read/write block command sets the response to each fault condition. This command is used instead of the following standard PMBus commands:

- VOUT_OV_FAULT_RESPONSE
- VOUT_UV_FAULT_RESPONSE
- IOUT_OC_FAULT_RESPONSE
- IOUT_UC_FAULT_RESPONSE
- OT_FAULT_RESPONSE
- TON_MAX_FAULT_RESPONSE

As with the original PMBus fault response commands, whenever a fault occurs:

- The corresponding fault bit is the status register is set.
- The PMBus ALERT pin is asserted.
- The fault bit, once set, is cleared only in accordance to Section 10.2.3 in the PMBus specification and not when the fault condition is removed or corrected.

The command format is shown in Table 58 and Table 59.

Table 58. FAULT_RESPONSES Command Format (Devices Other Than UCD90160)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = E9
1	0		BYTE_COUNT = 9
2	1	0	VOUT_OV Fault Response
3	2	1	VOUT_UV Fault Response
4	3	2	IOUT_OC Fault Response
5	4	3	IOUT_UC Fault Response
6	5	4	OT Fault Response
7	6	5	TON_MAX Fault Response
8	7	6	Time between retries
9	8	7	Maximum glitch time for voltage faults
10	9	8	Maximum glitch time for non-voltage faults

Table 59. FAULT_RESPONSES Command Format (UCD90160)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = E9
1	0		BYTE_COUNT = 6
2	1	0	VOUT_OV Fault Response
3	2	1	VOUT_UV Fault Response
4	3	2	TON_MAX Fault Response

Table 59. FAULT_RESPONSES Command Format (UCD90160) (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
5	4	3	Time between retries
6	5	4	Maximum glitch time for voltage faults
7	6	5	Maximum glitch time for non-voltage faults

10.25.1 Fault Response Bytes

The Fault Response bytes (the first eight bytes) are formatted as shown in Table 60.

NOTE: The Glitch Filter option is not valid for the “TON_MAX Fault Response”. Attempting to set that bit to one returns a NACK due to Invalid Data.

For devices other than the UCD90120 and UCD90124: The device will not wait for sequence off dependencies when it turns off a rail enable to perform a retry. Once retries are exhausted, the device will wait for sequence off dependencies before turning off the rail enable.

Table 60. Fault Response Byte Format

Bits	Description	Value	Meaning
7	Operation	n/a	When this bit is set to one, the device shuts down (disables the output) and responds according to the retry setting in bits [3:0]. The function associated with the following Glitch Filter bit, may delay or prevent the shutdown. When set to zero, the PMBus device continues operation without interruption.
6	Glitch Filter	n/a	When this bit is set to one, the device continues operation for a delay time specified by the “Maximum glitch time for voltage faults” or the “Maximum glitch time for non-voltage faults” byte. If the fault condition is removed during the delay time, the timer will reset and the fault will be ignored. If the fault condition is present for longer than the delay time, the device will respond to the fault as programmed in the Retry Setting (bits[3:0]).
5	Soft Stop	n/a	If this bit is set to 1, the rail will come to a soft stop (using TOFF_DELAY). If it is set to 0, the rail shuts down immediately.
4	Re-sequence	n/a	When this bit is set to 1 and the retries have been exhausted, the rail and its Fault Slaves are shutdown in a manner based on the Soft Stop bit. All of those rails are resequenced after a delay time defined by the “Time between Resequences” byte in the MISC_CONFIG command (see Section 10.44)
3:0	Retry Setting	0000	A 0 value for the Retry Setting means that the device does not attempt to restart the rail. The rail remains off until a turn-off and then turn-on command (by OPERATION command or CONTROL pin or Pin-Selected State) are received.
		0001–1110	The device attempts to restart the rail for the number of times set by these bits. The minimum number is 1 and the maximum number is 14. If the rail fails to restart successfully within the allowed number of retries, the device disables the rail and remains off unless Resequence bit is set. The rail can be also turned back on according to the conditions described in Section 10.7 of PMBus specification. The time between the start of each restart attempt is set by the ”Time between retries” byte. **Note:** This retry count is reset whenever the rail stays in regulation for a TON_MAX_FAULT_LIMIT amount of time without having a glitch. (If TON_MAX_FAULT_LIMIT is set to 0, 4 seconds are used for the time.) Glitches on faults where the Operation bit is set to zero are ignored.
		1111	The device attempts to restart the rail continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the rail to shut down.

10.25.2 Re-Sequence

The option to re-sequence is offered as a response to each type of fault. The re-sequence operation is not performed until the retries are exhausted for a given fault. During the re-sequence operation:

- The faulty rail and its Fault Shutdown Slaves (FSS) rails are immediately disabled (Stop Immediately)

or disabled according to the configured shutdown sequence (Stop With Delay)

- After the faulted rail and its FSS rails' Enable pins are de-asserted and all of these rails have turned off (the voltage has fallen below POWER_GOOD_OFF), the UCD90xxx waits for a programmable delay time before starting the resequence. The delay time is configured by the "Time between Resequences" byte in the MISC_CONFIG command, (see Section 10.44). While waiting for the rails to turn off, if any rail voltage does not fall below 12.5% of nominal output voltage within a time period defined by TOFF_MAX_WARN_LIMIT, a TOFF_MAX_WARN warning will occur. User can configure whether to abort the resequence when the TOFF_MAX_)WARN warning occurs. For more information, see the MISC_CONFIG command (Section 10.44). For UCD9090A and UCD90160A, it is configurable to ignore the POWR_GOOD_OFF and TOFF_WARNING status of the rail when resequencing, (see Section 10.44). This is mainly for those rails whose EN signals are not controlled by UCD.
- After the resequence delay time, the faulty rail and its FSS rails are sequenced on according to the start-up sequence configuration. The resequence attempt can repeat 1-4 times or unlimited times to bring the faulty rail and its FSS rails to regulation. The maximum resequence times is configured in the Section 10.44. If a resequence operation is successful – that is, all of the rails that were resequenced maintain in normal operation (power-good and no retries) for 1 second – the resequence counter will be reset. (If a resequenced rail is not configured to turn on during the resequence , the device does not wait for that rail to come on before declaring the resequence operation is successful.) If the rails are resequenced the maximum number times and they fail to reach normal operation, a device reset is required to reset the resequence counter. Rails can be commanded off and then on in an attempt to get them back to normal operation.

This resequence operation is straight-forward if there is only one set of faulty rail and FSS rails. If two or more sets of rails require resequence at the same time, the device behavior is always conservative. For example, if a set of rails is already on its second resequence, and the device is configured to resequence three times, and another set of rails enters the resequence state, the second set of rails are only resequenced once so that the total resequence time is 3. Another example – if one set of rails is awaiting all of its rails to shutdown so that it can resequence, and another set of rails enters the resequence state, the device now waits for all rails from both sets to shutdown before resequencing.

NOTE: UCD9090A/UCD90160A - if any rails at the resequence state are caused by GPI fault response, the whole resequence is suspended until the GPI fault is physically clear.

10.25.3 Time Between Retries

When configured to retry, this value determines the amount of time that the device waits before it tries to re-enable a rail after it was shutdown due to a fault.

For the UCD90120 and UCD90124, the value in this byte is multiplied by 5 ms to get the “Time between retries”.

For devices other than the UCD90120 and UCD90124, this byte is formatted according to Section 2.5. For UCD90240, the minimum value is 1 ms.

For UCD90240, this value is also configured by (F4h) GPI_FAULT_RESPONSES in Section 10.36.2. The *Time Between Retries* value defined in the two commands should be identical, otherwise, whichever latter value is written to the device will take effect.

10.25.4 Maximum Glitch Time for Voltage Faults

The value in this byte is multiplied by 400 µs to get the “Maximum glitch time for voltage faults”. This applies to the following faults: VOUT_OV, VOUT_UV.

10.25.5 Maximum Glitch Time for Non-Voltage Faults

The value in this byte is multiplied by 100 ms to get the “Maximum glitch time for non-voltage faults”. This applies to the following faults: IOUT_OC, IOUT_UC, OT.

10.26 (EAh) LOGGED_FAULTS (MFR_SPECIFIC_26)

This read/write block command reports a history of all faults that have ever been reported and logged into nonvolatile memory.

Clearing the Log: Writing a block whose data bytes are all 0x00 resets all logged entries to 0. This also clears the LOGGED_FAULT_DETAIL entries (see Section 10.28). Nonzero values in any data byte returns a NACK due to Invalid Data. Clearing the log does not clear the non-volatile memory if brownout function is enabled. For the applications where brownout feature is required, the user must disable the brownout function before issuing a command to clear the log, and re-enable the brownout function after the log is cleared.

10.26.1 Command Format

This command returns a binary array in the order shown in Table 61 to Table 67. Note that the command sends information of all pages, even when some pages are not active. Log entries of inactive pages are reported as 0x00.

Table 61. LOGGED_FAULTS Command Format (UCD90120 and UCD90124)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = EA
1	0		BYTE_COUNT = 13
2	1	0	Non-Paged Faults
3	2	1	Page 0 Faults
4	3	2	Page 1 Faults
5	4	3	Page 2 Faults
. . .	. . .	. . .	. . .
14	13	12	Page 11 Faults

Note that the log includes pages 0 through 11, even when fewer than 12 pages are active.

Table 62. LOGGED_FAULTS Command Format (UCD9090 and UCD9090A)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = EA
1	0		BYTE_COUNT = 12
2	1	0	Non-Paged Faults
3	2	1	GPI Faults
4	3	2	Page 0 Faults
5	4	3	Page 1 Faults
. . .	. . .	. . .	. . .
13	12	11	Page 9 Faults

Table 63. LOGGED_FAULTS Command Format (UCD90160 and UCD90160A)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = EA
1	0		BYTE_COUNT = 18
2	1	0	Non-Paged Faults
3	2	1	GPI Faults
4	3	2	Page 0 Faults
5	4	3	Page 1 Faults

Table 63. LOGGED_FAULTS Command Format (UCD90160 and UCD90160A) (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
. . .	. . .	. . .	. . .
19	18	17	Page 15 Faults

Table 64. LOGGED_FAULTS Command Format (UCD90910)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = EA
1	0		BYTE_COUNT = 14
2	1	0	Non-Paged Faults
3	2	1	GPI Faults
4	3	2	Fan Faults (high byte)
5	4	3	Fan Faults (low byte)
6	5	4	Page 0 Faults
7	6	5	Page 1 Faults
. . .	. . .	. . .	. . .
15	14	13	Page 9 Faults

Table 65. LOGGED_FAULTS Command Format (UCD90120A)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = EA
1	0		BYTE_COUNT = 14
2	1	0	Non-Paged Faults
3	2	1	GPI Faults
4	3	2	Page 0 Faults
5	4	3	Page 1 Faults
. . .	. . .	. . .	. . .
15	14	13	Page 11 Faults

Table 66. LOGGED_FAULTS Command Format (UCD90124A)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = EA
1	0		BYTE_COUNT = 15
2	1	0	Non-Paged Faults
3	2	1	GPI Faults
4	3	2	Fan Faults
5	4	3	Page 0 Faults
6	5	4	Page 1 Faults
. . .	. . .	. . .	. . .
16	15	14	Page 11 Faults

Table 67. LOGGED_FAULTS Command Format (UCD90240)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = EA
1	0		BYTE_COUNT = 28
2	1	0	Non-Paged Faults
3	2	1	GPI Faults (Byte 0 - LSB)
4	3	2	GPI Faults (Byte 1)
5	4	3	GPI Faults (Byte 2)
6	5	4	Page 0 Faults
7	6	5	Page 1 Faults
. . .	. . .	. . .	. . .
29	28	27	Page 23 Faults

10.26.2 Non-Paged Faults

The bit definitions for common faults are shown in Table 68, Table 69, and Table 70.

By examining this single bit (bit 0 of the Non-Paged Faults byte), a host can determine if any page-dependent, GPI, or fan faults have occurred. A value of 0 in this bit indicates that all of the page-dependent, GPI, and fan fault log entries are 0 and need not be read. A value of 1 in this bit indicates that one or more of the page-dependent, GPI, or fan faults has occurred. In that case, the host must examine all of the log entries to determine which ones have log information.

Table 68. Non-Paged Fault Log Bit Definitions (UCD90120)

Bit	Description	Can Generate a LOGGED_FAULT_DETAIL Entry?
0	LOG_NOT_EMPTY	No
1	Reserved	No
2	Re-Sequence Error	No
3	Watchdog Timeout	Yes
4	Reserved	No
5	Reserved	No
6	Reserved	No
7	Reserved	No

Table 69. Non-Paged Fault Log Bit Definitions (UCD90124)

Bit	Description	Can Generate a LOGGED_FAULT_DETAIL Entry?
0	LOG_NOT_EMPTY	No
1	Reserved	No
2	Re-Sequence Error	No
3	Watchdog Timeout	Yes
4	Fan 1 Fault	Yes
5	Fan 2 Fault	Yes
6	Fan 3 Fault	Yes
7	Fan 4 Fault	Yes

Table 70. Non-Paged Fault Log Bit Definitions (Devices Other Than the UCD90120 or UCD90124)

Bit	Description	Can Generate a LOGGED_FAULT_DETAIL Entry?
0	LOG_NOT_EMPTY	No
1	System Watchdog Timeout	Yes
2	Resequence Error	No
3	Watchdog Timeout	Yes
4	Reserved	No
5	Reserved	No
6	Reserved	No
7	Reserved	No

10.26.3 GPI Faults

The bit definitions for GPI faults are shown in Table 71 and Table 72. These bits are set whenever the associated GPI is de-asserted.

Table 71. GPI Fault Log Bit Definitions (other than UCD90240)

Bit	Description	Can Generate a LOGGED_FAULT_DETAIL Entry?
0	GPI1	Yes
1	GPI2	Yes
2	GPI3	Yes
3	GPI4	Yes
4	GPI5	Yes
5	GPI6	Yes
6	GPI7	Yes
7	GPI8	Yes

Table 72. GPI Fault Log Bit Definitions (UCD90240)

Bit	Description	Can Generate a LOGGED_FAULT_DETAIL Entry?
		Byte 0 (LSB)
0	GPI_0	Yes
1	GPI_1	Yes
2	GPI_2	Yes
3	GPI_3	Yes
4	GPI_4	Yes
5	GPI_5	Yes
6	GPI_6	Yes
7	GPI_7	Yes
		Byte 1
0	GPI_8	Yes
1	GPI_9	Yes
2	GPI_10	Yes
3	GPI_11	Yes
4	GPI_12	Yes
5	GPI_13	Yes
6	GPI_14	Yes

Table 72. GPI Fault Log Bit Definitions (UCD90240) (continued)

Bit	Description	Can Generate a LOGGED_FAULT_DETAIL Entry?
7	GPI_15	Yes
		Byte 2
0	GPI_16	Yes
1	GPI_17	Yes
2	GPI_18	Yes
3	GPI_19	Yes
4	GPI_20	Yes
5	GPI_21	Yes
6	GPI_22	Yes
7	GPI_23	Yes

10.26.4 Fan Faults

The bit definitions for Fan faults are shown in Table 73 and Table 74.

Table 73. Fan Fault Log Bit Definitions (low byte)

Bit	Description	Can Generate a LOGGED_FAULT_DETAIL Entry?
0	FAN 1	Yes
1	FAN 2	Yes
2	FAN 3	Yes
3	FAN 4	Yes
4	FAN 5	Yes
5	FAN 6	Yes
6	FAN 7	Yes
7	FAN 8	Yes

Table 74. Fan Fault Log Bit Definitions (high byte)

Bit	Description	Can Generate a LOGGED_FAULT_DETAIL Entry?
0	FAN 9	Yes
1	FAN 10	Yes
2	Reserved	No
3	Reserved	No
4	Reserved	No
5	Reserved	No
6	Reserved	No
7	Reserved	No

10.26.5 Page-Dependent Faults

The bit definitions for page-dependent faults are shown in Table 75, Table 76, and Table 77.

Table 75. Page-Dependent Fault Log Bit Definitions (UCD90120 and UCD90124)

Bit	Description	Can Generate a LOGGED_FAULT_DETAIL Entry?
0	VOUT_OV Fault	Yes

Table 75. Page-Dependent Fault Log Bit Definitions (UCD90120 and UCD90124) (continued)

Bit	Description	Can Generate a LOGGED_FAULT_DETAIL Entry?
1	VOUT_UV Fault	Yes
2	TON_MAX Fault	Yes
3	IOUT_OC Fault	Yes
4	IOUT_UC Fault	Yes
5	TEMPERATURE_OT Fault	Yes
6	SEQ_TIMEOUT Fault	Yes
7	Slaved Fault	No

Table 76. Page-Dependent Fault Log Bit Definitions (Devices Other Than the UCD90120, UCD90124, and UCD90160)

Bit	Description	Can Generate a LOGGED_FAULT_DETAIL Entry?
0	VOUT_OV Fault	Yes
1	VOUT_UV Fault	Yes
2	TON_MAX Fault	Yes
3	IOUT_OC Fault	Yes
4	IOUT_UC Fault	Yes
5	TEMPERATURE_OT Fault	Yes
6	Sequence On Timeout	Yes
7	Sequence Off Timeout	Yes

Table 77. Page-Dependent Fault Log Bit Definitions (UCD90160)

Bit	Description	Can Generate a LOGGED_FAULT_DETAIL Entry?
0	VOUT_OV Fault	Yes
1	VOUT_UV Fault	Yes
2	TON_MAX Fault	Yes
3	Reserved	No
4	Reserved	No
5	Reserved	No
6	Sequence On Timeout	Yes
7	Sequence Off Timeout	Yes

10.27 (EBh) LOGGED_FAULT_DETAIL_INDEX (MFR_SPECIFIC_27)

The read form of this command reports the total number of LOGGED_FAULT_DETAIL entries and the current value of the index into those entries (see Section 10.28). The Fault index byte can be written.

Table 78. LOGGED_FAULT_DETAIL_INDEX Command Format

Byte Number	Description
1	Fault Index(R/W)
2	Total Number of LOGGED_FAULT_DETAIL entries (Read Only))

10.28 (ECh) LOGGED_FAULT_DETAIL (MFR_SPECIFIC_28)

This read-only command returns detail information about a given fault:

1. The time that it happened in milliseconds (0 to 86400000) and days (0 to 1048575)
2. Whether or not the fault is page specific
3. The page that the fault occurred on (when applicable)
4. The type of fault (see Section 10.26)

Table 79. LOGGED_FAULT_DETAIL Command Format

Byte Number (Read)	Payload Index	Description
		CMD = EC
0		BYTE_COUNT = 10
1	0	Milliseconds (high byte)
2	1	Milliseconds
3	2	Milliseconds
4	3	Milliseconds (low byte)
5	4	Fault ID + Days (high byte)
6	5	Fault ID + Days
7	6	Fault ID + Days
8	7	Fault ID + Days (low byte)
9	8	Fault Value (low byte)
10	9	Fault Value (high byte)

Table 80. LOGGED_FAULT_DETAIL Command Format (UCD90240 Only)

Byte Number (Read)	Payload Index	Description
		CMD = EC
0		BYTE_COUNT = 11
1	0	Page number + Milliseconds (high byte)(1)
2	1	Milliseconds
3	2	Milliseconds
4	3	Milliseconds (low byte)
5	4	Fault ID + Days (high byte)
6	5	Fault ID + Days
7	6	Fault ID + Days
8	7	Fault ID + Days (low byte)
9	8	Fault Value (low byte)
10	9	Fault Value (middle byte)
11	10	Fault Value (high byte)(2)

(1) Page number is at bits 31:27 and Milliseconds is at bit 26:0.
(2) This byte is valid only if the current fault type is either Sequence On Timeout or Sequence Off Timeout.

New LOGGED_FAULT_DETAIL entries for a given fault are logged once and then not logged again until one of the following events occurs:

1. Firmware is restarted.
2. The rail stays in regulation for the amount of time determined by TON_MAX_FAULT_LIMIT. If TON_MAX_FAULT_LIMIT is set to 0, 4 seconds are used for the time. (This applies to paged faults only)
3. The rail is turned off and then turned back on. (This applies to paged faults only.)
4. The CLEAR_FAULTS command is written.
5. The LOGGED_FAULTS command is written.

- CLEAR_FAULTS command applies to all faults on UCD90120, UCD90124, and UCD90910 products only. LOGGED_FAULT command: for UCD90120, UCD90124, and UCD90910, this applies to all faults. For UCD 90120A, UCD90124A, UCD9090, and UCD90160, this applies to GPI faults only.
  For UCD90240, the GPI fault is logged each time when the GPI state is changed to de-asserted.

The maximum number of entries per device is show in Table 81. Once the maximum entries have been logged, no more detail is logged until the fault log is cleared (see Section 10.26). Unless, the “Enable Log FIFO” bit in the MISC_CONFIG command is set (see Table 120).

Table 81. Number of Log Entries in Each Device Type

Device	Entries
UCD90120	16
UCD90120A	16
UCD90124	10
UCD90124A	12
UCD9090	30
UCD90910	12
UCD90160	18
UCD90240	100

The Days field is a 32-bit value where the top bits are used to encode other information as shown in Table 82 or Table 83.

Table 82. Fault Identification

Bits(s)	Description
31	Page Specific (1 – yes, 0 – no)
30–27	Fault Type
26–23	Page Number
22-0	Days

Table 83. Fault Identification + Days (UCD90240)

Bits(s)	Description
31	Page Specific (1 – yes, 0 – no)
30–27	Fault Type
26–11	Days[(1)]
10-0	Reserved

(1) The days is offset from 2000-01-01 00:00:00.00. It is responsible of application to add the that time base when retrieving the time stamp.

Information on the Fault Value (units and formatting) is shown in Table 84 and Table 85.

Table 84. Fault Value (UCD90120 and UCD90124 Devices)

Fault Type Number	Paged?	Description	Fault Value Units	Data Format
0	NO	Reserved		
1	No	Reserved		
2	No	Resequence Error	Not Valid	n/a
3	No	Watchdog Timeout	Not Valid	n/a
4	No	Fan 1 Fault	RPM	LINEAR11
5	No	Fan 2 Fault	RPM	LINEAR11
6	No	Fan 3 Fault	RPM	LINEAR11

Table 84. Fault Value (UCD90120 and UCD90124 Devices) (continued)

Fault Type Number	Paged?	Description	Fault Value Units	Data Format
7	No	Fan 4 Fault	RPM	LINEAR11
0	Yes	VOUT_OV Fault	Voltage	LINEAR16
1	Yes	VOUT_UV Fault	Voltage	LINEAR16
2	Yes	TON_MAX Fault	Voltage	LINEAR16
3	Yes	IOUT_OC Fault	Current	LINEAR11
4	Yes	IOUT_UC Fault	Current	LINEAR11
5	Yes	TEMPERATURE_OT Fault	Temperature	LINEAR11
6	Yes	SEQ_TIMEOUT Fault	Not Valid	n/a
7	Yes	Reserved		

Table 85. Fault Value (Devices Other Than UCD90120 and UCD90124)

Fault Type Number	Paged?	Description	Fault Value Units	Data Format
0	No	Reserved		
1	No	System Watchdog Timeout	Not Valid	n/a
2	No	Resequence Error	Not Valid	n/a
3	No	Watchdog Timeout	Not Valid	n/a
4	No	Reserved		LINEAR11
5	No	Reserved		LINEAR11
6	No	Reserved		LINEAR11
7	No	Reserved		LINEAR11
8	No	Fan Fault(1)	RPM	LINEAR11
9	No	GPI Fault(1)	Not Valid	n/a
0	Yes	VOUT_OV Fault	Voltage	LINEAR16
1	Yes	VOUT_UV Fault	Voltage	LINEAR16
2	Yes	TON_MAX Fault	Voltage	LINEAR16
3	Yes	IOUT_OC Fault	Current	LINEAR11
4	Yes	IOUT_UC Fault	Current	LINEAR11
5	Yes	TEMPERATURE_OT Fault	Temperature	LINEAR11
6	Yes	Sequence On Timeout	N/A	Bit Mask(2)(3)
7	Yes	Sequence Off Timeout	N/A	Bit Mask(2)(3)

(1) The Page Number is used to encode which Fan or GPI that the fault information applies to.

(2) Any bit set to 1 corresponds to a page dependency that is not met. The GPI dependencies that are not met are OR'ed into the top 8 bits. So, for example, if page dependencies 2 and 5 are not met and GPI W (bit 4) dependency is not met, the fault value is 0x1024.

(3) This is for UCD90240 only. Any bit set to 1 corresponds to a page dependency that is not met. The GPI dependencies that are not met are OR'ed into the all 24 bits. So, for example, if page dependencies 2 and 5 are not met and GPI W (bit 4) dependency is not met, the fault value is 0x000034.

10.29 (EDh) LOGGED_PAGE_PEAKS (MFR_SPECIFIC_29)

This Read/Write Block command returns the maximum temperatures, voltages, and currents seen during operation for a given page. Provisions exist to reset this nonvolatile logged information.

This command returns a binary array in the order shown in Table 86. Each temperature is one unsigned byte that contains the temperature in degrees C. Each voltage is two bytes in LINEAR16 format. Each current is two bytes in LINEAR11 format.

The temperature is from the external temperature sensor associated with this page and is the same one reported by the READ_TEMPERATURE_2 command.

Table 86. LOGGED_PAGE_PEAKS Command Format

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = ED
1	0		BYTE_COUNT = 5 (1)
2	1	0	Temperature (1) (2)
3	2	1	Voltage (low byte)
4	3	2	Voltage (high byte)
5	4	3	Current (low byte) (1) (3)
6	5	4	Current (high byte) (1) (3)

(1) the byte count varies up on the device monitoring feature, see (2) and (3) the following.
(2) This byte is only available if device support temperature monitoring.
(3) These two bytes are only available if device support current monitoring.

Clearing the Log: Writing a block whose data bytes are all 0x00 resets all logged entries to 0. Nonzero values in any data byte return a NACK due to Invalid Data. The peaks can be cleared for all pages by setting the PAGE command to 0xFF.

Flash Memory Management: To reduce unnecessary stress on the Flash memory, the peak values are stored in volatile RAM memory and only written to Flash memory under certain conditions:

a. If at least one temperature, voltage, or current value exceeds its previously logged maximum value a 30-second timer is started. At the end of this timer interval, the values are copied from RAM to Flash memory. During a transient event, the peak value may reach several new maximums in rapid succession; the 30-second timer combines them together for a single write operation.

b. If a new fault is recorded in the fault log (see Section 10.26), both the peak log and the fault log are written to Flash.

10.30 (EEh) LOGGED_COMMON_PEAKS (MFR_SPECIFIC_30)

This Read/Write Byte command returns the maximum internal temperature in degrees Celsius. Provisions exist to reset this nonvolatile logged information. The internal temperature sensor reading is the same one reported by the READ_TEMPERATURE_1 command.

Clearing the Log: Writing a value of 0x00 resets the log. Nonzero values return a NACK due to Invalid Data.

10.31 (EFh) LOG_FAULT_DETAIL_ENABLES (MFR_SPECIFIC_31)

This Read/Write Block command selects what fault detail (see Section 10.28) is logging by rail and by fault type. The command, the bytes in the command, and the bits in those bytes are formatted the same as the LOGGED_FAULTS command, see Section 10.26.1. For this LOGGED_FAULT_DETAIL_ENABLES command, the bits select if a fault is logged (1) or not (0).

Table 87. LOGGED_FAULT_DETAIL_ENABLES Command Format (UCD90240)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = EF
1	0		BYTE_COUNT = 28
2	1	0	Non-paged Enable Flags
3	2	1	GPI Enable Flags - Byte 0 (LSB)
4	3	2	GPI Enable Flags - Byte 1
5	4	3	GPI Enable Flags - Byte 2
6	5	4	Page Enable Flags – Page 0
7	6	5	Page Enable Flags – Page 1
8	7	6	Page Enable Flags – Page 2
9	8	7	Page Enable Flags – Page 3
10	9	8	Page Enable Flags – Page 4
11	10	9	Page Enable Flags – Page 5
12	11	10	Page Enable Flags – Page 6
13	12	11	Page Enable Flags – Page 7
14	13	12	Page Enable Flags – Page 8
15	14	13	Page Enable Flags – Page 9
16	15	14	Page Enable Flags – Page 10
17	16	15	Page Enable Flags – Page 11
18	17	16	Page Enable Flags – Page 12
19	18	17	Page Enable Flags – Page 13
20	19	18	Page Enable Flags – Page 14
21	20	19	Page Enable Flags – Page 15
22	21	20	Page Enable Flags – Page 16
23	22	21	Page Enable Flags – Page 17
24	23	22	Page Enable Flags – Page 18
25	24	23	Page Enable Flags – Page 19
26	25	24	Page Enable Flags – Page 20
27	26	25	Page Enable Flags – Page 21
28	27	26	Page Enable Flags – Page 22
29	28	27	Page Enable Flags – Page 23
30	29	28	Reserved Fan Enable Flags - Byte 0 (LSB)
31	30	29	Reserved Fan Enable Flags - Byte 1

10.32 (F0h) EXECUTE_FLASH (MFR_SPECIFIC_32)

If the device is in ROM mode, this command starts the device executing in FLASH mode. If the device is already in FLASH mode, the command has no effect. This command is not supported by UCD90240.

10.33 (F1h) SECURITY (MFR_SPECIFIC_33)

This Read/Write Block command allows certain commands to be write-protected. The data for this command is a 6-byte binary string containing the password. The password is stored in nonvolatile memory, and is used to secure the unit against unauthorized modification of its settings.

While security is turned on, certain commands (defined by the SECURITY_BIT_MASK (F4) command) are write-protected and may not be modified. Attempts to write to a protected command while security is on will result in a NACK. There is an exception for protected “Send Byte” commands. They will not return a NACK, but they will be ignored.

If the SECURITY_BIT_MASK is not supported, these are the only commands that can be written when security is enabled:

CLEAR_FAULTS
FAN_COMMAND_1
FAN_COMMAND_2
FAN_COMMAND_3
FAN_COMMAND_4
FAN_CONFIG_INDEX
GPIO_SELECT
GPO_CONFIG_INDEX
LOGGED_FAULT_DETAIL_INDEX
OPERATION
PAGE
PARM_INFO
PWM_SELECT
READ_TEMPERATURE_2
RESEQUENCE
RUN_TIME_CLOCK
SECURITY
STORE_DEFAULT_ALL
SYSTEM_WATCHDOG_RESET
USER_RAM_00

10.33.1 Enabling Security

When security has not yet been enabled or has been disabled, writing this command sets the new password and enables the security. The password can be any value other than [0xFF FF FF FF FF FF]. After security is enabled, a STORE_DEFAULT_ALL command must be issued to store the security setting into data flash. Otherwise the security setting will be lost after device reset.

10.33.2 Disabling Security

Whenever security is enabled, it can be temporarily disabled by issuing this command with the correct password. The security can be permanently disabled by first disabling security, then setting the password to [0xFF FF FF FF FF FF], and then issuing a STORE_DEFAULT_ALL command.

If the sent password does not match the stored password, the write command is NACKed. Additional attempts to write this command will be NACKed until the device is reset. This prevents an attacker from merely sending the command repeatedly with all possible passwords.

10.33.3 Reading this Command

For security reasons, reading this value does not return the actual password. The response code depends on the present security setting.

Read Response Code	Meaning
0x00 00 00 00 00 00	Security is turned off.
0x00 00 00 00 00 01	Security is turned on.
0x00 00 00 00 00 02	This command is locked due to incorrect password entry.

A PMBus host does not need to validate the entire 6-byte response code. Only the last byte is significant to determining the security status: 0x00 (security off), 0x01 (security on), 0x02 (Invalid password).

10.34 F2h) SECURITY_BIT_MASK (MFR_SPECIFIC_34)

This Read/Write Block command controls which PMBus commands are password-protected to prevent unauthorized modification.

The data for this command is a 32-byte binary string. Each bit in the string corresponds to one of the 256 possible PMBus command codes.

When a bit is set to 1, the corresponding PMBus command is write-protected if security is on.

When a bit is set to 0, the corresponding PMBus command is not write-protected even if security is on. For PMBus commands that do not support any write, the corresponding mask bit is ignored by firmware.

To password-protect a command, the byte and bit to be set in the security bit mask is determined from these formulas:

Byte = floor (Command_Code / 8)
Bit = 7 – (Command_Code – Byte × 8)

Byte	0								1								2		
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	…
Command Code	0	1	2	3	4	5	6	7	8	9	0A	0B	0C	0D	0E	0F	10	11	…

Byte		29		30								31							
Bit	…	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Command Code	…	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF

If security is turned on, the SECURITY command (F1h) must be issued to allow modifying the security bit mask. If security is turned off, the security bit mask can be modified anytime. The bit mask is stored directly into nonvolatile memory and does not require a STORE_DEFAULTS_ALL command.

10.35 (F3h) MFR_STATUS (MFR_SPECIFIC_35)

The Manufacturer Status bits are defined in Table 88. With the exception of the STORE_DEFAULT_ALL_DONE bit, whenever any of these bits are set, the PMBALERT# line is asserted.

NOTE: With the UCD90120 and UCD90124 devices, this command is 2 bytes long (bits 0-15). With the UCD90240, this command is 5 bytes long. With all other devices, it is 4 bytes long.

Table 88. Manufacturer Specific Status (UCD90120 and UCD90124)

Bit(s)	Name	Description
15-11	Reserved	
10	STORE_DEFAULT_ALL_ERROR	An error occurred during STORE_DEFAULT_ALL
9	STORE_DEFAULT_ALL_DONE	The STORE_DEFAULT_ALL operation has completed
8	WATCHDOG_TIMEOUT	A UCD90xxx internal watchdog timeout reset has occurred.
7	INVALID_LOGS	The fault and peak logs where corrupted and are no longer valid. They are zeroed out. This relates to these commands: LOGGED_FAULTS LOGGED_FAULT_DETAIL LOGGED_PAGE_PEAKS LOGGED_COMMON_PEAKS
6	LOGGED_FAULT_DETAIL_FULL	The LOGGED_FAULT_DETAIL buffer is full [See Section 10.28]
5	CONFIG_INVALID	Invalid SEQ_CONFIG, GPI_CONFIG, or GPO_CONFIG
4	RESEQUENCE_ERROR	An error occurred during the re-sequencing operation. This occurs when one of the rails that are part of the re-sequence operation does not turn off before its TOFF_MAX_WARN_LIMIT.
3	PKGID_MISMATCH	Hardware Package ID does not match firmware
2	HARDCODED_PARMS	PMBus hard-coded configuration values have been loaded into RAM. The data flash image on the device is empty or corrupt. This state is referred to as a NOBOARD configuration. This default configuration only minimally configures the device (for example, no rails are defined). Executing a STORE_DEFAULT_ALL command updates the data flash on the device. After a STORE_DEFAULT_ALL and reset, this HARDCODED_PARMS status bit is cleared. It also can be cleared with the CLEAR_FAULTS command.
1	SEQ_TIMEOUT	Sequencing timeout waiting for external event (paged) [See Section 10.1]
0	SLAVED_FAULT	The rail was shut down because it is dependent on another rail that had a fault [see Section 10.38.9].

Table 89. Manufacturer Specific Status (UCD90240)

Byte Number (write)	Byte Number (Read)	Payload Index	Bit in Each Payload Byte	Name	Descriptions
0					CMD = F3
1	0				BYTE_COUNT = 5
2	1	0	0	GPI17 Fault	Set whenever the GPI is de-asserted.
2	1	0	1	GPI18 Fault	See GPI17, bit 0 byte 0
2	1	0	2	GPI19 Fault	See GPI17, bit 0 byte 0
2	1	0	3	GPI20 Fault	See GPI17, bit 0 byte 0
2	1	0	4	GPI21 Fault	See GPI17, bit 0 byte 0
2	1	0	5	GPI22 Fault	See GPI17, bit 0 byte 0
2	1	0	6	GPI23 Fault	See GPI17, bit 0 byte 0
2	1	0	7	GPI24 Fault	See GPI17, bit 0 byte 0
3	2	1	0	GPI8 Fault	See GPI17, bit 0 byte 0
3	2	1	1	GPI9 Fault	See GPI17, bit 0 byte 0
3	2	1	2	GPI11 Fault	See GPI17, bit 0 byte 0
3	2	1	3	GPI12 Fault	See GPI17, bit 0 byte 0
3	2	1	4	GPI13 Fault	See GPI17, bit 0 byte 0
3	2	1	5	GPI14 Fault	See GPI17, bit 0 byte 0
3	2	1	6	GPI15 Fault	See GPI17, bit 0 byte 0
3	2	1	7	GPI16 Fault	See GPI17, bit 0 byte 0
4	3	2	0	GPI1 Fault	See GPI17, bit 0 byte 0
4	3	2	1	GPI2 Fault	See GPI17, bit 0 byte 0
4	3	2	2	GPI3 Fault	See GPI17, bit 0 byte 0
4	3	2	3	GPI4Fault	See GPI17, bit 0 byte 0
4	3	2	4	GPI5 Fault	See GPI17, bit 0 byte 0

Table 89. Manufacturer Specific Status (UCD90240) (continued)

Byte Number (write)	Byte Number (Read)	Payload Index	Bit in Each Payload Byte	Name	Descriptions
4	3	2	5	GPI6 Fault	See GPI17, bit 0 byte 0
4	4	2	6	GPI7 Fault	See GPI17, bit 0 byte 0
4	4	2	7	GPI8 Fault	See GPI17, bit 0 byte 0
5	4	3	0	WATCHDOG_TIMEOUT	A UCD90xxx internal watchdog timeout reset has occurred
5	4	3	1	STORE_DEFAULT_ALL_DONE	The STORE_DEFAULT_ALL operation has completed
5	4	3	2	STORE_DEFAULT_ALL_ERROR	An error occurred during STORE_DEFAULT_ALL
5	4	3	3	SYSTEM_WATCHDOG_TIMEOUT	A system watchdog timeout reset has occurred (see Section 10.4)
5	4	3	4	NEW_ LOGGED_FAULT_DETAIL	This bit is set whenever a new fault detail entry is logged. It is cleared whenever the LOGGED_FAULT_DETAIL command is read.
5	4	3	5:7	Reserved	
6	5	4	0	SLAVED_FAULT	The rail was shutdown because it is dependent on another rail that had a fault (paged) [See Section 10.38.9]
6	5	4	1	SEQ_ON_TIMEOUT	Sequence on timeout (paged) [See Section 10.38.4]
6	5	4	2	SEQ_OFF_TIMEOUT	Sequence off timeout (paged) [See Section 10.38.4]
6	5	4	3	HARDCODED_PARMS	PMBus hard-coded configuration values have been loaded into RAM. The data flash image on the device is empty or corrupt. This state is referred to as a NOBOARD configuration. This default configuration only minimally configures the
					device (for example, no rails are defined). Executing a STORE_DEFAULT_ALL command updates the data flash on the device. After a STORE_DEFAULT_ALL and reset, this HARDCODED_PARMS status bit is cleared. It also can be cleared with the CLEAR_FAULTS command.
6	5	4	4	PKGID_MISMATCH	Hardware Package ID does not match firmware
6	5	4	5	RESEQUENCE_ERROR	An error occurred during the re-sequencing operation. This occurs when one of the rails that are part of the resequence operation does not turn off before its TOFF_MAX_WARN_LIMIT.
6	5	4	6	LOGGED_FAULT_DETAIL_FULL	The LOGGED_FAULT_DETAIL buffer is full [See Section 10.26]
6	5	4	7	INVALID_LOGS	The fault and peak logs where corrupted and are no longer valid. They are zeroed out. This relates to these commands: LOGGED_FAULTS LOGGED_FAULT_DETAIL LOGGED_PAGE_PEAKS LOGGED_COMMON_PEAKS

Table 90. Manufacturer-Specific Status (Devices Other Than the UCD90120, UCD90124, and UCD90240)

Bit(s)	Name	Description
31-24	Reserved	
23	GPI8 Fault	Set whenever the GPI is de-asserted.
22	GPI7 Fault	See GPI8, bit 23
21	GPI6 Fault	See GPI8, bit 23
20	GPI5 Fault	See GPI8, bit 23
19	GPI4 Fault	See GPI8, bit 23
18	GPI3 Fault	See GPI8, bit 23
17	GPI2 Fault	See GPI8, bit 23
16	GPI1 Fault	See GPI8, bit 23
15-13	Reserved	
12	NEW_ LOGGED_FAULT_DETAIL	This bit is set whenever a new fault detail entry is logged. It is cleared whenever the LOGGED_FAULT_DETAIL command is read.
11	SYSTEM_WATCHDOG_ TIMEOUT	A system watchdog timeout reset has occurred (see Section 10.4)
10	STORE_DEFAULT_ALL_ ERROR	An error occurred during STORE_DEFAULT_ALL
9	STORE_DEFAULT_ALL_ DONE	The STORE_DEFAULT_ALL operation has completed
8	WATCHDOG_TIMEOUT	A UCD90xxx internal watchdog timeout reset has occurred
7	INVALID_LOGS	The fault and peak logs where corrupted and are no longer valid. They are zeroed out. This relates to these commands: LOGGED_FAULTS LOGGED_FAULT_DETAIL LOGGED_PAGE_PEAKS LOGGED_COMMON_PEAKS
6	LOGGED_FAULT_DETAIL_ FULL	The LOGGED_FAULT_DETAIL buffer is full [See Section 10.28]
5	RESEQUENCE_ERROR	An error occurred during the resequencing operation. This occurs when one of the rails that are part of the resequence operation does not turn off before its TOFF_MAX_WARN_LIMIT.
4	PKGID_MISMATCH	Hardware Package ID does not match firmware
3	HARDCODED_PARMS	PMBus hard-coded configuration values have been loaded into RAM. The data flash image on the device is empty or corrupt. This state is referred to as a NOBOARD configuration. This default configuration only minimally configures the
		device (for example, no rails are defined). Executing a STORE_DEFAULT_ALL command updates the data flash on the device. After a STORE_DEFAULT_ALL and reset, this HARDCODED_PARMS status bit is cleared. It also can be cleared with the CLEAR_FAULTS command.
2	SEQ_OFF_TIMEOUT	Sequence off timeout (paged) [See Section 10.38]
1	SEQ_ON_TIMEOUT	Sequence on timeout (paged)[See Section 10.38]
0	SLAVED_FAULT	The rail was shutdown because it is dependent on another rail that had a fault (paged) Section 10.38.9

10.36 (F4h) GPI_FAULT_RESPONSES (MFR_SPECIFIC_36)

This paged Read/Write Block command configures the rail response to GPI faults. The fault flag must be set for the corresponding GPI via GPI_CONFIG(F9h) command, or this command is ignored. GPI is treated as fault only if it is transited from assertion to de-assertion. See Section 10.41.2 for more details.

Devices other than UCD90240: this command is not supported.

Table 91. GPI_FAULT_RESPONSES Command Format (UCD90240 only)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = F4
1	0		BYTE_COUNT = 27
2	1	0	GPI Fault Responses – GPI 0
3	2	1	GPI Fault Responses – GPI 1

Table 91. GPI_FAULT_RESPONSES Command Format (UCD90240 only) (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
4	3	2	GPI Fault Responses – GPI 2
5	4	3	GPI Fault Responses – GPI 3
6	5	4	GPI Fault Responses – GPI 4
7	6	5	GPI Fault Responses – GPI 5
8	7	6	GPI Fault Responses – GPI 6
9	8	7	GPI Fault Responses – GPI 7
10	9	8	GPI Fault Responses – GPI 8
11	10	9	GPI Fault Responses – GPI 9
12	11	10	GPI Fault Responses – GPI 10
13	12	11	GPI Fault Responses – GPI 11
14	13	12	GPI Fault Responses – GPI 12
15	14	13	GPI Fault Responses – GPI 13
16	15	14	GPI Fault Responses – GPI 14
17	16	15	GPI Fault Responses – GPI 15
18	17	16	GPI Fault Responses – GPI 16
19	18	17	GPI Fault Responses – GPI 17
20	19	18	GPI Fault Responses – GPI 18
21	20	19	GPI Fault Responses – GPI 19
22	21	20	GPI Fault Responses – GPI 20
23	22	21	GPI Fault Responses – GPI 21
24	23	22	GPI Fault Responses – GPI 22
25	24	23	GPI Fault Responses – GPI 23
26	25	24	Time between retries
27	26	25	Maximum glitch time for GPI(high byte)
28	27	26	Maximum glitch time for GPI(low byte)

10.36.1 Fault Responses Byte

Refer to Section 10.25.1 for the byte definition of Fault Responses Byte, retry action is not supported by GPI fault response.

10.36.2 Time Between Retries

When configured to do so, this value determines the delay time before the device tries to re-enable a rail after it was shutdown due to a fault. The byte is formatted according to Section 2.5. This value has to be 1 ms or bigger.

This value is also configured by (E9h) FAULT_RESPONSES in Section 10.25.3. The *Time Between Retries* value defined in the two commands should be identical, otherwise, whichever latter value is written to the device will take effect.

10.36.3 Maximum Glitch Time for GPI

The value in this byte is multiplied by 300 µs to get the Maximum glitch of GPI input.

10.37 (F5h) MARGIN_CONFIG (MFR_SPECIFIC_37)

This paged Read/Write Byte command configures if a given rail can be margined, and if so, how.

Table 92. MARGIN_CONFIG Command Format (UCD90120 and UCD90124)

Bit(s)	Name	Description
7	Margin Enable[1]	Margining can be done on the associated rail.
6	Calibration Enable	When this bit is set to 1, firmware fine-tunes the normal (nonmargining) duty cycle. The first time that the rail is enabled for normal operation, the duty cycle is adjusted so that the monitored voltage is as close to VOUT_COMMAND as possible. This calibration will be redone after a reset or power cycle.
5	Ignore Faults	When margining is enabled with a pin, this bit determines if faults (overvoltage and undervoltage) are ignored or not.
4	Reserved	
3:0	PWM Pin	Selects the PWM pin. This value is a PWM-capable pin ID from Table 14. The frequency for the PWM is configured with the PWM_CONFIG command.

(1) If the Margin Enable bit is set, the associated PWM_CONFIG command must be written before the MARGIN_CONFIG command is written.

Table 93. MARGIN_CONFIG Command Format (UCD90240)

Bit(s)	Name	Description
		Byte 0
7:5	Reserved	Reserved
4:0	PWM Pin	Selects the PWM pin. This value is a PWM-capable pin ID from Table 12. The frequency for the PWM is configured with the PWM_CONFIG command.
		Byte 1
7:6	Mode[1]	b'00: DISABLE - Margining is disabled b'01: ENABLE_HIGH_IMPEDANCE - When not margining, the PWM pin is put in a high-impedance state b'10: ENABLE_ACTIVE_TRIM - When not margining, the PWM duty cycle is continuously adjusted to keep the voltage at VOUT_COMMAND b'11: ENABLE_FIXED_DUTY_CYCLE - When not margining, the PWM duty cycle is set to a fixed duty cycle
5	Ignore Faults	When margining is enabled with a pin, this bit determines if faults (over-voltage and under-voltage) are ignored or not.
4	Duty Cycle	This bit determines the relationship between the duty cycle and the output voltage. The output voltage increases when the duty cycle: 1 – increases 0 – decreases
3:0	Reserved	Reserved

(1) If the Mode is not DISABLE, the associated PWM_CONFIG command must be written before the MARGIN_CONFIG command is written.

Table 94. MARGIN_CONFIG Command Format (Devices Other Than the UCD90120, UCD90124, and UCD90240)

Bit(s)	Name	Description
7:6	Mode[1]	b'00: DISABLE - Margining is disabled
		b'01: ENABLE_HIGH_IMPEDANCE - When not margining, the PWM pin is put in a high-impedance state
		b'10: ENABLE_ACTIVE_TRIM - When not margining, the PWM duty cycle is continuously adjusted to keep the voltage at VOUT_COMMAND
		b'11: ENABLE_FIXED_DUTY_CYCLE - When not margining, the PWM duty cycle is set to a fixed duty cycle
5	Ignore Faults	When margining is enabled with a pin, this bit determines if faults (over-voltage and under-voltage) are ignored or not.

(1) If the Mode is not DISABLE, the associated PWM_CONFIG command must be written before the MARGIN_CONFIG command is written.

Table 94. MARGIN_CONFIG Command Format (Devices Other Than the UCD90120, UCD90124, and UCD90240) (continued)

Bit(s)	Name	Description
4	Duty Cycle	This bit determines the relationship between the duty cycle and the output voltage. The output voltage increases when the duty cycle: 1 – increases 0 – decreases **Note:** The UCD90910 does not support this configuration bit.
3:0	PWM Pin	Selects the PWM pin. This value is a PWM-capable pin ID from Table 14 or Table 15. The frequency for the PWM is configured with the PWM_CONFIG command.

10.38 (F6h) SEQ_CONFIG (MFR_SPECIFIC_38)

This Read/Write Block command configures the sequencing dependencies and enable pin for a given rail.

Features include:

1. Sequencing – Configures interdependency between how voltage rails are enabled/disabled
2. Fault Slaves – Configure slave pages which also shut down when a fault occurs
3. Enable Pin – Identifies the enable pin, and its operating characteristics.

NOTE: All configurations done with the GPI_CONFIG command must be done before writing this command.

When this command is written, the enable pin for the rail will be de-asserted. Then the state of the rail is re-evaluated. If it is determined that the rail should be on, the enable pin is then asserted.

Table 95. SEQ_CONFIG Command Format (UCD90240)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = F6
1	0		BYTE_COUNT = 19
2	1	0	Enable Pin Configuration
3	2	1	GPI Sequence On Dependency Mask (Byte 0 - LSB)
4	3	2	GPI Sequence On Dependency Mask (Byte 1)
5	4	3	GPI Sequence On Dependency Mask (Byte 2)
6	5	4	GPI Sequence Off Dependency Mask (Byte 0 - LSB)
7	6	5	GPI Sequence Off Dependency Mask (Byte 1)
8	7	6	GPI Sequence Off Dependency Mask (Byte 2)
9	8	7	Sequencing Timeout Configuration
10	9	8	Sequencing On Timeout
11	10	9	Sequencing Off Timeout
12	11	10	Page Sequence On Dependency Mask (Byte 0 - LSB)
13	12	11	Page Sequence On Dependency Mask (Byte 1)
14	13	12	Page Sequence On Dependency Mask (Byte 2)
15	14	13	Page Sequence Off Dependency Mask (Byte 0 - LSB)
16	15	14	Page Sequence Off Dependency Mask (Byte 1)
17	16	15	Page Sequence Off Dependency Mask (Byte 2)
18	17	16	Fault Slaves Mask (Byte 0 - LSB)
19	18	17	Fault Slaves Mask (Byte 1)
20	19	18	Fault Slaves Mask (Byte 2)

Table 96. SEQ_CONFIG Command Format (UCD90160A and UCD9090A Only)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = F6
1	0		BYTE_COUNT = 16
2	1	0	Enable Pin Configuration
3	2	1	GPI Sequence On Dependency Mask
4	3	2	GPI Sequence Off Dependency Mask
5	4	3	Sequencing Timeout Configuration
6	5	4	Sequencing On Timeout (high byte)
7	6	5	Sequencing On Timeout (low byte)
8	7	6	Sequencing Off Timeout (high byte)
9	8	7	Sequencing Off Timeout (low byte)
10	9	8	Page Sequence On Dependency Mask (high byte)
11	10	9	Page Sequence On Dependency Mask (low byte)
12	11	10	Page Sequence Off Dependency Mask (high byte)
13	12	11	Page Sequence Off Dependency Mask (low byte)
14	13	12	Fault Slaves Mask (high byte)
15	14	13	Fault Slaves Mask (low byte)
16	15	14	GPO Sequence On Dependency Mask
17	16	15	GPO Sequence Off Dependency Mask

Table 97. SEQ_CONFIG Command Format (UCD90120 and UCD90124)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = F6
1	0		BYTE_COUNT = 6
2	1	0	GPI Sequence On Dependency Mask
3	2	1	Page Sequence On Dependency Mask (high byte)
4	3	2	Page Sequence On Dependency Mask (low byte)
5	4	3	Fault Slaves Mask (high byte)
6	5	4	Fault Slaves Mask (low byte)
7	6	5	Enable Pin Configuration

Table 98. SEQ_CONFIG Command Format (Devices Other Than the UCD90240, UCD90120, UCD90124, UCD90160A, and UCD9090A)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = F6
1	0		BYTE_COUNT = 12
2	1	0	Enable Pin Configuration
3	2	1	GPI Sequence On Dependency Mask
4	3	2	GPI Sequence Off Dependency Mask
5	4	3	Sequencing Timeout Configuration
6	5	4	Sequencing On Timeout
7	6	5	Sequencing Off Timeout
8	7	6	Page Sequence On Dependency Mask (high byte)

Table 98. SEQ_CONFIG Command Format (Devices Other Than the UCD90240, UCD90120, UCD90124, UCD90160A, and UCD9090A) (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
9	8	7	Page Sequence On Dependency Mask (low byte)
10	9	8	Page Sequence Off Dependency Mask (high byte)
11	10	9	Page Sequence Off Dependency Mask (low byte)
12	11	10	Fault Slaves Mask (high byte)
13	12	11	Fault Slaves Mask (low byte)

The turn on condition for each page can depend on the state of several other pages and/or input pins. The same pages and pins also may be used to control multiple pages. The GPI and Page dependencies (Sequence On Dependencies) define a set of conditions which allow a page to turn on when met. Note that the logical AND of all conditions must be met before a page can be turned on. Once the page is on, these dependencies have no further effect on the operating status of the page. Specifically, they do not cause a page to turn off.

Sequence On Dependencies work in parallel with the PMBus defined mechanisms used to enable an output. That is, both the Sequence On Dependencies and the PMBus mechanism must be satisfied. For example, if the page responds to an OPERATION command and the OPERATION command specifies OFF, the page remains off even if all of the sequencing Sequence On Dependencies are met. Further, the order in which they are met is irrelevant; if the OPERATION command is issued first, the page will wait for the sequencing requirements to be met before it can be turned on; or if the sequencing requirements are met first, the page will wait for the OPERATION command before it can be turned on.

In the ON_OFF_CONFIG command, a “None” setting is still subject to the specified Sequence On Dependencies.

Turn on delay (TON_DELAY) is applied after the page has been commanded on and all Sequence On Dependencies are met.

For devices other that the UCD90120 and UCD90124: Unless the rail is instructed to turn off immediately, the previous descriptions also apply to the Sequence Off Dependencies – they must be met before the rail is turned off, the turn off delay (TOFF_DELAY) is applied after the dependencies are met, and so forth.

After a fault, the PMBus specification requires that an OFF/ON sequence should occur before the rail is allowed to restart. Note that the toggle of sequencing pin (such as CONTROL pin and Pin-Selected State GPI) is interpreted to meet this requirement. For example, consider a page that responds to the CONTROL pin and was shut down due to a fault. A toggle low then high on the CONTROL pin is sufficient to restart the page.

NOTE: Some tables in the following subsections assume that the device supports 16 rails (0 to 15). For a given device, this may not be the case. The interpretation of this information should be adjusted for the correct number of rails.

10.38.1 Enable Pin Configuration

See Section 7 for byte format and details.

Enable pins are configured just like output pins. They are active once conditions dictate that a page must be enabled and inactive until then. The conditions are defined by the ***GPI Dependency Mask*** and the ***Page Dependency Mask*** in this command and the value given by the TON_DELAY command.

NOTE: The “input” mode is invalid for enable pins. Attempting to set the mode bits to 1 returns a NACK due to Invalid Data.

10.38.2 GPI Sequence On Dependency Mask

Each page has its own GPI Sequence On Dependency Mask, whose bits are defined as follows:

Bit	7	6	5	4	3	2	1	0
Purpose	GPI Z	GPI Y	GPI X	GPI W	GPI V	GPI U	GPI T	GPI S

The enable pin for the page is not asserted until all of the input pins selected by the GPI bits are asserted. Once the enable pin is asserted, the state of these GPI pins has no effect on the state of the enable pin.

For devices other than UCD90240, each page can depend on the state of up to eight input pins. For UCD90240, each page can depend on the state of up to 24 input pins. The same pins can be used to control multiple pages. (see **Section 10.41 on page 127**).

10.38.3 GPI Sequence Off Dependency Mask

Each page has its own GPI Sequence Off Dependency Mask, whose bits are defined as follows:

Bit	7	6	5	4	3	2	1	0
Purpose	GPI Z	GPI Y	GPI X	GPI W	GPI V	GPI U	GPI T	GPI S

The enable pin for the page is not de-asserted until all of the input pins selected by the GPI bits are de-asserted. Once the enable pin is de-asserted, the state of these GPI pins has no effect on the state of the enable pin.

For devices other than UCD90240, each page can depend on the state of up to eight input pins. For UCD90240, each page can depend on the state of up to 24 input pins. The same pins can be used to control multiple pages. (see Section 10.41).

10.38.4 Sequencing Timeout Configuration

The configuration bits in Table 99 defines how the device will respond to sequence timeouts. Whenever a sequencing timeout occurs, the associated MRF Status and fault log information will be updated.

Table 99. Sequencing Timeout Configuration Byte

Bit(s)	Name	Description
7:4	Reserved	
3:2	Sequence-Off Timeout Action	This bits determine what action will be taken after a sequence-off timeout occurs: b'00 – The device continues to wait indefinitely for the sequence-off dependencies to be met. b'01 – The device stops waiting for the sequence-off dependencies to be met and continues the process of disabling the rail. b'10 – (same as b'00 action) b'11 – (same as b'00 action)
1:0	Sequence-On Timeout Action	This bits determine what action will be taken after a sequence-on timeout occurs: b'00 – The device continues to waits indefinitely for the sequence-on dependencies to be met. b'01 – The device stops waiting for the sequence-on dependencies to be met and continues the process of enabling the rail. b'10 – The device resequences this rail and all fault shutdown slaves associated with this rail. This operation will happen according to the "Time between Resequences" byte and the "Maximum Resequences" field in the MISC_CONFIG command (see Section 10.44). b'11 – (same as b'00 action)

10.38.5 Sequencing On Timeout

This timeout value is used to check that rail sequences on within a certain period of time. In other words, this timeout is used to detect if one of the rail's sequence-on dependencies is never met. When this occurs, a status bit will be set.

The timeout periods start to count when a rail receives a turn-on command as defined in ON_OFF_CONFIG. A timeout value of 0 disables the timeout monitoring function. This byte is formatted according to Section 2.5. For UCD90160A and UCD9090A, these two bytes are formatted according to Section 2.6.

10.38.6 Sequencing Off Timeout

This timeout value is used to check that rail sequences off within a certain period of time. In other words, this timeout is used to detect if one of the rail's sequence-off dependencies is never met. When this occurs, a status bit will be set. For UCD90160A and UCD9090A, these two bytes are formatted according to Section 2.6.

10.38.7 Page Sequence On Dependency Mask

Each page has its own Page Sequence On Dependency Mask, whose bits are defined as follows (assuming there are a total of 16 rails):

Bit	15	14	13	12	11	10	9	8
Purpose	PAGE15	PAGE14	PAGE13	PAGE12	PAGE11	PAGE10	PAGE9	PAGE8
Bit	7	6	5	4	3	2	1	0
Purpose	PAGE7	PAGE6	PAGE5	PAGE4	PAGE3	PAGE2	PAGE1	PAGE0

The enable pin for the page is not asserted until all of the rails selected by these bits have reached their power-good state.

Each page can depend on the state of several other pages. The same pages can be used to control other pages as well.

10.38.8 Page Sequence Off Dependency Mask

Each page has its own Page Sequence Off Dependency Mask, whose bits are defined as follows (assuming there are a total of 16 rails):

Bit	15	14	13	12	11	10	9	8
Purpose	PAGE15	PAGE14	PAGE13	PAGE12	PAGE11	PAGE10	PAGE9	PAGE8
Bit	7	6	5	4	3	2	1	0
Purpose	PAGE7	PAGE6	PAGE5	PAGE4	PAGE3	PAGE2	PAGE1	PAGE0

The enable pin for the page is not de-asserted until all of the rails selected by these bits have left their power-good state.

Each page can depend on the state of several other pages. The same pages can be used to control other pages as well.

10.38.9 Fault Slaves Mask

Each page has its own Fault Slaves Mask, whose bits are defined as follows (assuming there are a total of 16 rails):

Bit	15	14	13	12	11	10	9	8
Purpose	PAGE15 fault slave	PAGE14 fault slave	PAGE13 fault slave	PAGE12 fault slave	PAGE11 fault slave	PAGE10 fault slave	PAGE9 fault slave	PAGE8 fault slave
Bit	7	6	5	4	3	2	1	0
Purpose	PAGE7 fault slave	PAGE6 fault slave	PAGE5 fault slave	PAGE4 fault slave	PAGE3 fault slave	PAGE2 fault slave	PAGE1 fault slave	PAGE0 fault slave

Each page can have multiple fault slave pages. When a fault occurs on the master page, if its response is to shut down, all slave pages are also shut down. If retries are specified for the master page, the slave page(s) remain running until all retries are exhausted. For the UCD90120 and UCD90124 devices, the slave pages are shut down in the same way as the master page is (immediately or soft stop, see Section 10.25.1). For devices other than the UCD90120 and UCD90124, the slave pages are shut down using sequence off dependencies and TOFF_DELAY. The slave pages do not perform any retries during the fault slave shutdown.

After being shut down, slave rails are latched off as if they had experienced the fault. To re-enable their outputs, an off command must be received before another on command is accepted. A status bit is set in their MFR_STATUS word indicating the reason they are latched off.

The fault slaves Mask is also part of graceful shutdown function, which is defined in MONITOR_CONFIG command. During the graceful shutdown period, the UV faults from those rails defined by the Mask are not logged and responsed.

10.38.10 GPO Sequence On Dependency Mask

Each page has its own GPO Sequence On Dependency Mask, whose bits are defined in the following table:

Bit	7	6	5	4	3	2	1	0
Purpose	GPO8	GPO7	GPO6	GPO5	GPO4	GPO3	GPO2	GPO1

It is logical state selected by the GPO not the actual pin output of the GPO used as dependency. Only the logical state of the first 8 GPO can be used as Sequence On Dependency Mask.

The enable pin for the page is not de-asserted until all of the logical states selected by the GPO bits are FALSE. Once the enable pin is de-asserted, the logical state of these GPO has no effect on the state of the enable pin.

Each page can depend on the state of up to eight GPO logical states. The same states can be used to control multiple pages (see Section 10.40).

10.38.11 GPO Sequence Off Dependency Mask

Each page has its own GPO Sequence Off Dependency Mask, whose bits are defined in the following table:

Bit	7	6	5	4	3	2	1	0
Purpose	GPIZ	GPIY	GPIX	GPIW	GPIV	GPI3	GPI2	GPI1

It is logical state selected by the GPO not the actual pin output of the GPO used as dependency. Only the logical state of the first 8 GPO can be used as Sequence On Dependency Mask.

Each page can depend on the state of up to eight GPO logical states. The same states can be used to control multiple pages (see Section 10.40).

10.39 (F7h) GPO_CONFIG_INDEX (MFR_SPECIFIC_39)

This R/W Byte command selects the index of the GPO that will be used for subsequent GPO_CONFIG commands.

For UCD90240, this command also selects the index for the GPO AND-Path. The AND-Path Index is transmitted in the upper 3 bits and the GPO index is transmitted in the lower 5 bits.

For all previous models, there is no need for a separate AND-Path index so the upper 3 bits should be set to 000.

Bit	7	6	5	4	3	2	1	0
Purpose	AND-Path Index			GPO Index				

Table 100. Relationship Between GPO_CONFIG_INDEX and the Actual GPO Number (UCD90120 Example)

GPO_CONFIG_INDEX	GPO
0	1
1	2
. . .	. . .
11	12

10.40 (F8h) GPO_CONFIG (MFR_SPECIFIC_40)

This Read/Write Block command configures the functionality of a given output pin. This paged command allows pins to be configured as status/GPI-influenced outputs. The state of the output pin is determined by a selection of GPIs and statuses of rails, fans, other GPOs (with or without assignment of an actual pin), and other function blocks such as watchdog. The input states are processed through some combinational logic with optional inversion steps. Upon device power up, the GPO status has an initial evaluation according to its configuration. Thereafter, the evaluation will be triggered when any of the associated status changes.

NOTE: All configurations done with the MONITOR_CONFIG, GPI_CONFIG, and SEQ_CONFIG commands must be done before writing this command.

Figure 8 and Figure 9 provide an overview of how the state of the GPO is determined.

NOTE: This document refers to the AND paths starting with “AND Path 0”. Fusion refers to the AND paths starting with and index of 1 instead of 0.

The information in Figure 8 implies that the device supports 12 rails (0 to 11). For the UCD90910, this is not the case. It only supports 10 rails and the interpretation of this information should be adjusted for the correct number of rails.

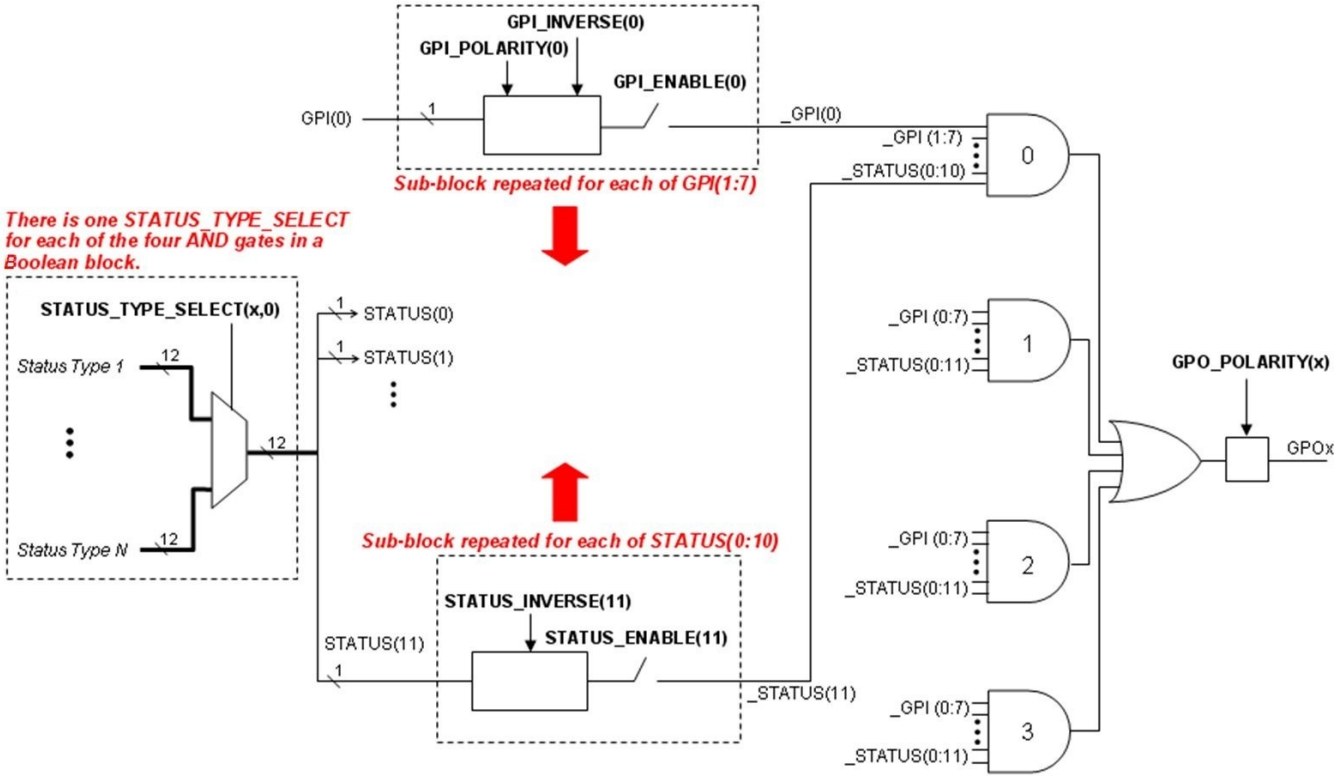


Figure 8. Factors Determining the State of a GPO (UCD90120, UCD90124, and UCD90910)

NOTE: The information in Figure 9 implies that the device supports 12 rails (0 to 11). For a given device, this may not be the case. The interpretation of this information should be adjusted for the correct number of rails.

The effect of State Machine Mode is not represented in Figure 9. When that mode is enabled, only one AND patch is active at a time.

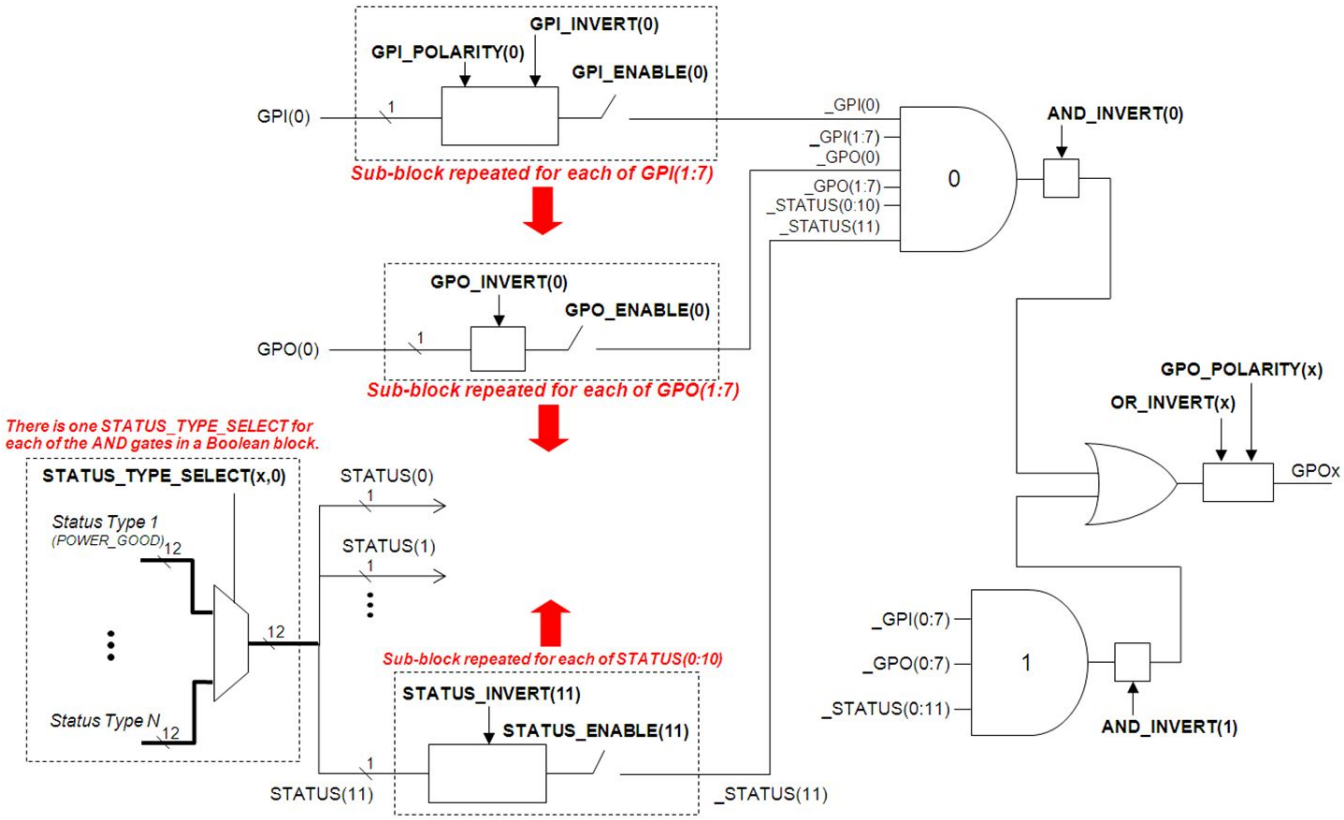


Figure 9. Factors Determining the State of a GPO (Devices Other Than UCD90120, UCD90124, and UCD90910)

NOTE: For the sake of code efficiency, all configured/active GPOs must be packed in the lower GPO indexes. This means, if there is only one configured GPO, it must be associated with GPO index 0. If there are two, they must be associated GPO indexes 0 and 1.

Table 101. GPO_CONFIG Command Format (UCD90120, UCD90124, and UCD90910)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = F8
1	0		BYTE_COUNT = 29
2	1	0	Output Pin Configuration
			AND Path 0
3	2	1	Status Mask 0 (high byte)
4	3	2	Status Mask 0 (low byte)
5	4	3	Status Inversion Mask 0 (high byte)
6	5	4	Status Inversion Mask 0 (low byte)
7	6	5	GPI Mask 0
8	7	6	GPI Inversion Mask 0
9	8	7	Status Type Select 0
			AND Path 1
10	9	8	Status Mask 1 (high byte)

Table 101. GPO_CONFIG Command Format (UCD90120, UCD90124, and UCD90910) (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
11	10	9	Status Mask 1 (low byte)
12	11	10	Status Inversion Mask 1 (high byte)
13	12	11	Status Inversion Mask 1 (low byte)
14	13	12	GPI Mask 1
15	14	13	GPI Inversion Mask1
16	15	14	Status Type Select 1
			AND Path 2
17	16	15	Status Mask 2 (high byte)
18	17	16	Status Mask 2 (low byte)
19	18	17	Status Inversion Mask 2 (high byte)
20	19	18	Status Inversion Mask 2 (low byte)
21	20	19	GPI Mask 2
22	21	20	GPI Inversion Mask 2
23	22	21	Status Type Select 2
			AND Path 3
24	23	22	Status Mask 3 (high byte)
25	24	23	Status Mask 3 (low byte)
26	25	24	Status Inversion Mask 3 (high byte)
27	26	25	Status Inversion Mask 3 (low byte)
28	27	26	GPI Mask 3
29	28	27	GPI Inversion Mask 3
30	29	28	Status Type Select 3

Table 102. GPO_CONFIG Command Format (Devices Other Than UCD90120, UCD90124, UCD90910, and UCD90240)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = F8
1	0		BYTE_COUNT = 21
2	1	0	Output Pin Configuration
3	2	1	**Bit** **Description** 7 Assert Delay Enable 6 De-assert Delay Enable 5 Invert OR Output 4 Ignore Inputs During Delay 3:0 High Resolution Delay Count
4	3	2	Millisecond Delay
5	4	3	AND Path 0 Configuration **Bit** **Description** 7 Invert AND Output 6 State Machine Mode Enable 5:0 Status Type

Table 102. GPO_CONFIG Command Format (Devices Other Than UCD90120, UCD90124, UCD90910, and UCD90240) (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
6	5	4	AND Path 1 Configuration **Bit Description** 7 Invert AND Output 6 reserved 5:0 Status Type
			AND Path 0
7	6	5	Status Mask 0 (high byte)
8	7	6	Status Mask 0 (low byte)
9	8	7	GPI Mask 0
10	9	8	GPO Mask 0
11	10	9	Status Inversion Mask 0 (high byte)
12	11	10	Status Inversion Mask 0 (low byte)
13	12	11	GPI Inversion Mask 0
14	13	12	GPO Inversion Mask 0
			AND Path 1
15	14	13	Status Mask 1 (high byte)
16	15	14	Status Mask 1 (low byte)
17	16	15	GPI Mask 1
18	17	16	GPO Mask 1
19	18	17	Status Inversion Mask 1 (high byte)
20	19	18	Status Inversion Mask 1 (low byte)
21	20	19	GPI Inversion Mask1
22	21	20	GPO Inversion Mask1

Table 103. GPO_CONFIG Command Format (UCD90240)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = F8
1	0		BYTE_COUNT = 24
2	1	0	Output Pin Configuration
3	2	1	**Bit Description** 7 Assert Delay Enable 6 De-assert Delay Enable 5 Invert OR Output 4 Ignore Inputs During Delay 3:0 High Resolution Delay Count
4	3	2	Millisecond Delay
5	4	3	AND Path x Configuration **Bit Description** 7 Invert AND Output 6 State Machine Mode Enable (Only in AND Path 0) 5:0 Status Type
			AND Path x
6	5	4	Status Mask (Byte 0 - LSB)

Table 103. GPO_CONFIG Command Format (UCD90240) (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
7	6	5	Status Mask (Byte 1)
8	7	6	Status Mask (Byte 2)
9	8	7	Status Inversion Mask (Byte 0 - LSB)
10	9	8	Status Inversion Mask (Byte 1)
11	10	9	Status Inversion Mask (Byte 2)
12	11	10	GPI Mask (Byte 0 – LSB)
13	12	11	GPI Mask (Byte 1)
14	13	12	GPI Mask (Byte 2)
15	14	13	GPI Inversion Mask (Byte 0 – LSB)
16	15	14	GPI Inversion Mask (Byte 1)
17	16	15	GPI Inversion Mask (Byte 2)
18	17	16	GPO Mask (Byte 0 – LSB)
19	18	17	GPO Mask (Byte 1)
20	19	18	Reserved
21	20	19	Reserved
22	21	20	GPO Inversion Mask (Byte 0 – LSB)
23	22	21	GPO Inversion Mask (Byte 1)
24	23	22	Reserved
25	24	23	Reserved

10.40.1 Output Pin Configuration

This byte configures which pin is used for this GPO, its polarity, and if it is actively driven or not. For details, see Section 8. A mode of “Input” causes this command to be rejected (receive a NACK).

NOTE: For the UCD90240, this value must be equal to the Pin ID from Table 13, minus an offset of 40.

For devices other than UCD90240, a GPO does not require to have a physical pin assigned to it.

10.40.2 Assert Delay Enable

When this bit is set there will be a delay (High Resolution and/or Millisecond) before the GPO is asserted.

10.40.3 De-Assert Delay Enable

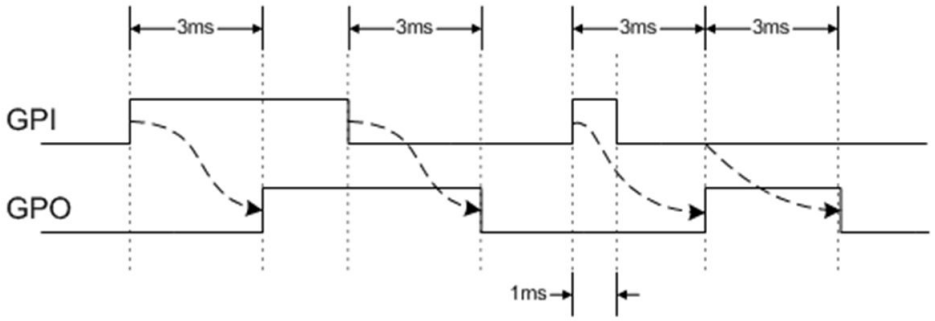
When this bit is set there will be a delay (High Resolution and/or Millisecond) before the GPO is de-asserted.

10.40.4 Invert OR Output

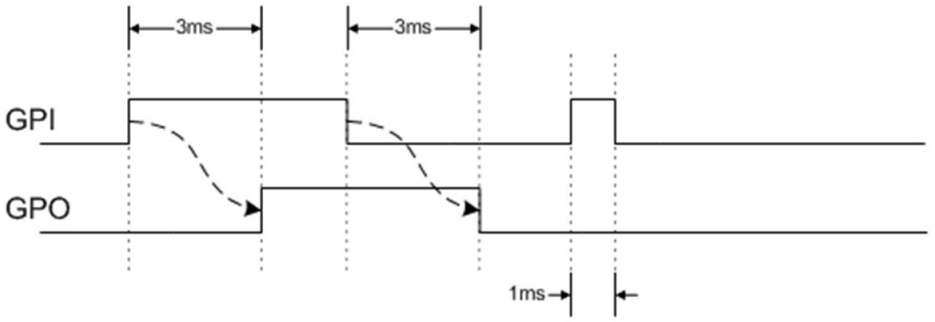
When this bit is set, the result of the OR operation is inverted. As an example, this function can be used to change the OR operation into an AND operation, (a OR b) = (a’ AND b’)’.

10.40.5 Ignore Inputs During Delay

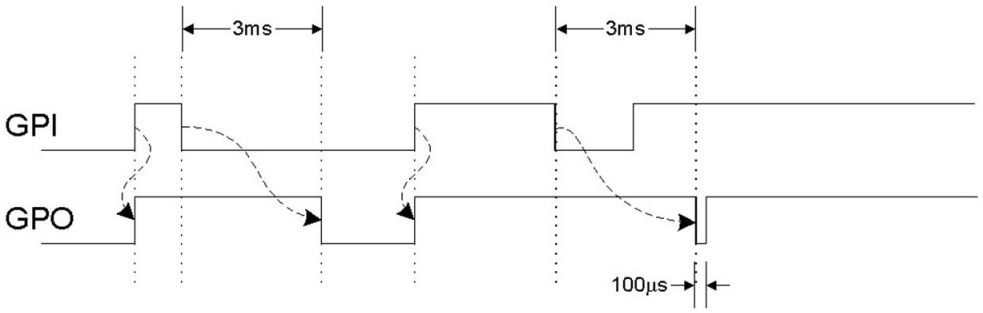
When this bit is set, changes to the inputs affecting the state of the GPO will be ignored while the update to the GPO is delayed. In other words, the GPO will change state upon the expiration of the delay time regardless the subsequent input state changes during the delay time. For example, if a GPO was simply following the state of a GPI with a 3 millisecond delay on assertion and deassertion, a timing diagram follows.



If this bit is not set, the GPO state will be re-evaluated upon the expiration of the delay time. If the input state returned to the original state at the re-evaluation point, the GPO state will not change. An example timing diagram follows.



When this bit is set, and there is a 3-ms delay on deassertion, but no delay on assertion, an example timing diagram follows. Note that the second deassert-to-assert pulse is only the sampling period of the GPI pins, which happens to be 100 µs.



10.40.6 Invert AND Output

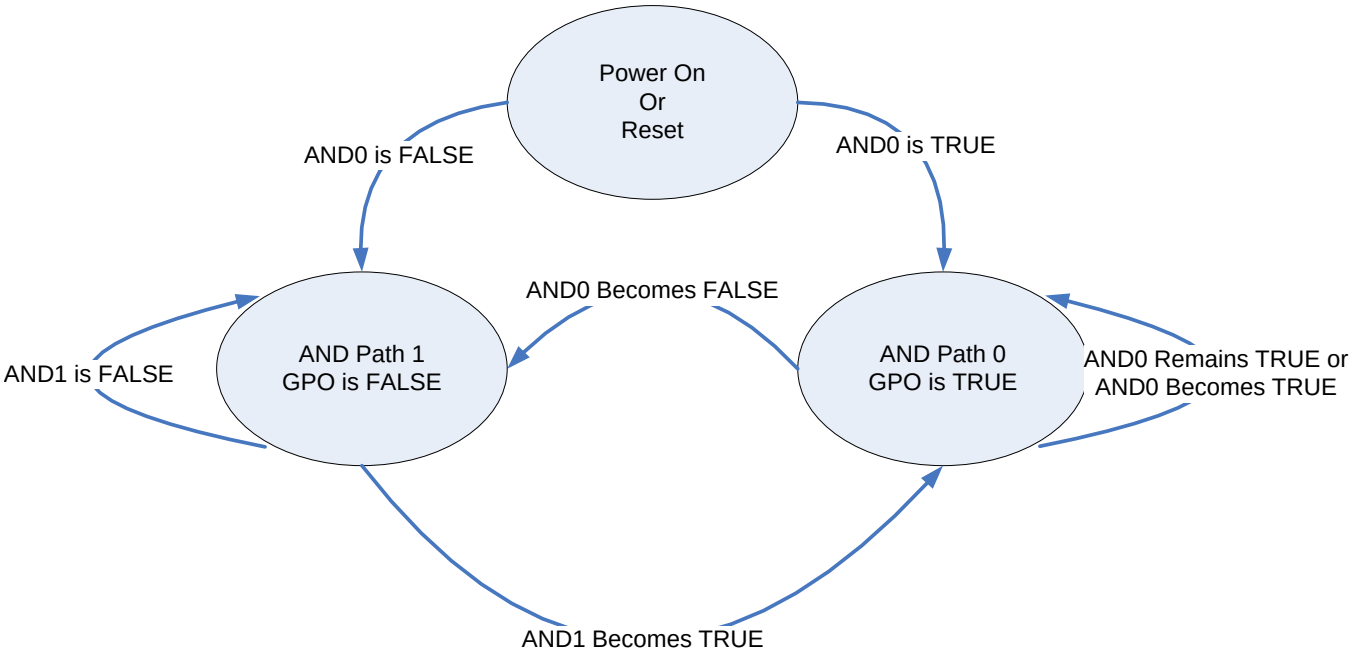
When this bit is set, the associated AND path result is inverted before it is fed into the OR gate. As an example, this function can be used to change the AND operation into an OR operation, (a' AND b')' = (a OR b).

10.40.7 State Machine Mode Enable

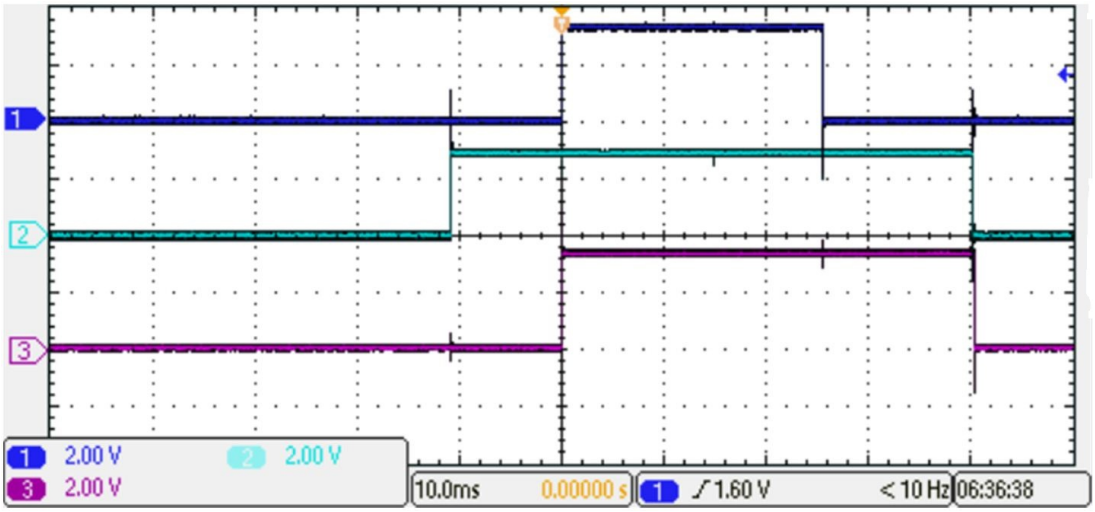
When this bit is set, only one of the AND path will be used at a given time. When the GPO logic result is currently TRUE, AND path 0 will be used until the result becomes FALSE. When the GPO logic result is currently FALSE, AND path 1 will be used until the result becomes TRUE. This provides a very simple state machine and allows for more complex logical combinations.

NOTE: The device initially evaluates AND path 0. If it is TRUE, it continues to evaluate AND path 0. If it is FALSE, it begins evaluating AND path 1 in the next evaluation cycle. Evaluation of a GPO is only triggered when its input states change; therefore, the state machine cannot be configured as a self-sustaining oscillator.

For UCD90240, this bit in AND path 0 determines the state machine mode. The same bit in AND path 1 is ignored.



For example, to configure a GPO in such a way that it is asserted when two GPI pins are both asserted and stay asserted until both GPIs are deasserted, we need to apply an AND operation when the GPO is deasserted and apply an OR operation when the GPO is asserted. This is shown in the following scope image, where waveform 1 is a GPI, waveform 2 is a GPI, and waveform 3 is a GPO.



This behavior is configured by setting the “State Machine Mode Enable”, configuring AND path 0 as (GPI1’ AND GPI2’)’, and configuring AND path 1 as (GPI1 AND GPI2).

10.40.8 High Resolution Delay Count

This value is multiplied by 100 µs to define the high resolution delay.

10.40.9 Millisecond Delay

This value is used to delay the update of a GPO. This byte is formatted according the 8-bit time encoding defined in Section 2.5.

10.40.10 Status Mask

The Status Mask selects which page(s) are to be used in a given AND path.

Bit	15	14	13	12	11	10	9	8
Purpose	PAGE15	PAGE14	PAGE13	PAGE12	PAGE11	PAGE10	PAGE9	PAGE8

Bit	7	6	5	4	3	2	1	0
Purpose	PAGE7	PAGE6	PAGE5	PAGE4	PAGE3	PAGE2	PAGE1	PAGE0

If a bit is set to 1, the corresponding page status is used in the AND path. If a bit is set to 0, the corresponding page status is not used by the AND path.

NOTE: This table assumes that the device supports 16 rails (0 to 15). For a given device, this may not be the case. The interpretation of this information should be adjusted for the correct number of rails.

10.40.11 Status Inversion Mask

The status of each page may be inverted before being used in a given AND path. If a bit is set to 1, the corresponding page status is inverted. Setting the bit to 0 has no effect.

Bit	15	14	13	12	11	10	9	8
Purpose	PAGE15	PAGE14	PAGE13	PAGE12	PAGE11	PAGE10	PAGE9	PAGE8

Bit	7	6	5	4	3	2	1	0
Purpose	PAGE7	PAGE6	PAGE5	PAGE4	PAGE3	PAGE2	PAGE1	PAGE0

NOTE: This table assumes that the device supports 16 rails (0 to 15). For a given device, this may not be the case. The interpretation of this information should be adjusted for the correct number of rails.

10.40.12 GPI Mask

This mask determines which GPIs are used for the given AND path. If a bit is set to 1, the corresponding GPI state is used by the AND path. If a bit is set to 0, the corresponding GPI state is not used by the AND path. See the GPI_CONFIG command.

Bit	7	6	5	4	3	2	1	0
Purpose	GPI Z	GPI Y	GPI X	GPI W	GPI V	GPI U	GPI T	GPI S

10.40.13 GPI Inversion Mask

This mask determines if the GPI state is inverted before being used for the given AND path. Setting the bit to 1 will invert the corresponding GPI state. Setting the bit to 0 has no effect.

Bit	7	6	5	4	3	2	1	0
Purpose	GPI Z	GPI Y	GPI X	GPI W	GPI V	GPI U	GPI T	GPI S

10.40.14 GPO Mask

This mask determines which of the first 8 GPOs are used for a given AND path. If a bit is set to 1, the corresponding GPO state will be used by the AND path. If a bit is set to 0, the corresponding GPO state will not be used by the AND path.

NOTE: When a GPO is used as an input to an AND path, the pin polarity setting of the GPO does not affect the evaluation result.

All of the 12 GPOs in UCD90240 can be used as AND path inputs.

Bit	7	6	5	4	3	2	1	0
Purpose	GPO 7	GPO 6	GPO 5	GPO 4	GPO 3	GPO 2	GPO 1	GPO 0

10.40.15 GPO Inversion Mask

This mask determines if the GPO state is inverted before being used for the given AND path. If a bit is set to 1, the corresponding GPO state is inverted. Setting the bit to 0 has no effect.

Bit	7	6	5	4	3	2	1	0
Purpose	GPO 7	GPO 6	GPO 5	GPO 4	GPO 3	GPO 2	GPO 1	GPO 0

10.40.16 Status Type Select

These bits select the status type to be applied to the Status Mask. Each AND path can select a different status type.

The _LATCH version of these status flags is latched and can only be cleared by a command (CLEAR_FAULTS) or a GPI (see Section 10.41.4). The non-_LATCH version is the actual current state of the condition.

NOTE:

1. Only the lowest four bits in the Status Mask and Status Inversion Mask are valid when the FAN_FAULT or the FAN_FAULT_LATCH Status Types are selected. Also, only the lowest bit is used for the SYSTEM_WATCHDOG_TIMEOUT and SYSTEM_WATCHDOG_TIMEOUT_LATCH statuses.
2. The FAN_FAULT or the FAN_FAULT_LATCH Status Types are only valid for the devices with fan support (UCD90124, UCD90124A, and UCD90910).
3. The MARGIN_EN and MRG_LOW_nHIGH statuses are updated based on GPI pins (see GPI_CONFIG, see Section 10.41) and/or the OPERATION command. Whenever the OPERATION command disables margining, the MRG_LOW_nHIGH status will be set to true.
4. After the following status types are set, they cannot be cleared until the rail is turned off and then back on: TON_MAX_FAULT, TOFF_MAX_WARN, SEQ_ON_TIMEOUT, SEQ_OFF_TIMEOUT. Note that a resequence operation will clear these status types, because it will turn the rail off and then turn the rail on.
5. When the _LATCH version of a status flag is cleared, it will stay FALSE even if the status is still TRUE. After that, it will only become TRUE again after the status goes to the FALSE state and back to the TRUE state.
6. The POWER_GOOD status used by GPO evaluation is based on actual voltage measurement of rails. For a rail that does not have a voltage monitor pin, its POWER GOOD status is used by sequencing purpose only, and is not used by GPO evaluation. For GPO evaluation, such a rail does NOT have POWER GOOD status

Table 104. Status Types

Encoding	Status Type
0	POWER_GOOD
1	MARGIN_EN
2	MRG_LOW_nHIGH
3	VOUT_OV_FAULT
4	VOUT_OV_WARN
5	VOUT_UV_WARN
6	VOUT_UV_FAULT
7	TON_MAX_FAULT
8	TOFF_MAX_WARN
9	IOUT_OC_FAULT
10	IOUT_OC_WARN
11	IOUT_UC_FAULT
12	TEMP_OT_FAULT
13	TEMP_OT_WARN
14	SEQ_TIMEOUT
15	VOUT_OV_FAULT_LATCH
16	VOUT_OV_WARN_LATCH
17	VOUT_UV_WARN_LATCH
18	VOUT_UV_FAULT_LATCH
19	TON_MAX_FAULT_LATCH
20	TOFF_MAX_WARN_LATCH
21	IOUT_OC_FAULT_LATCH
22	IOUT_OC_WARN_LATCH
23	IOUT_UC_FAULT_LATCH
24	TEMP_OT_FAULT_LATCH
25	TEMP_OT_WARN_LATCH
26	SEQ_TIMEOUT_LATCH

Table 105. Status Types (UCD90124)

Encoding	Status Type
0	POWER_GOOD
1	MARGIN_EN
2	MRG_LOW_nHIGH
3	VOUT_OV_FAULT
4	VOUT_OV_WARN
5	VOUT_UV_WARN
6	VOUT_UV_FAULT
7	TON_MAX_FAULT
8	TOFF_MAX_WARN
9	IOUT_OC_FAULT
10	IOUT_OC_WARN
11	IOUT_UC_FAULT
12	TEMP_OT_FAULT
13	TEMP_OT_WARN
14	SEQ_TIMEOUT
15	FAN_FAULT
16	VOUT_OV_FAULT_LATCH
17	VOUT_OV_WARN_LATCH
18	VOUT_UV_WARN_LATCH
19	VOUT_UV_FAULT_LATCH
20	TON_MAX_FAULT_LATCH
21	TOFF_MAX_WARN_LATCH
22	IOUT_OC_FAULT_LATCH
23	IOUT_OC_WARN_LATCH
24	IOUT_UC_FAULT_LATCH
25	TEMP_OT_FAULT_LATCH
26	TEMP_OT_WARN_LATCH
27	SEQ_TIMEOUT_LATCH
28	FAN_FAULT_LATCH

Table 106. Status Types (UCD90124A and UCD90910)

Encoding	Status Type
0	POWER_GOOD
1	MARGIN_EN
2	MRG_LOW_nHIGH
3	VOUT_OV_FAULT
4	VOUT_OV_WARN
5	VOUT_UV_WARN
6	VOUT_UV_FAULT
7	TON_MAX_FAULT
8	TOFF_MAX_WARN
9	IOUT_OC_FAULT
10	IOUT_OC_WARN
11	IOUT_UC_FAULT
12	TEMP_OT_FAULT
13	TEMP_OT_WARN
14	SEQ_ON_TIMEOUT

Table 106. Status Types (UCD90124A and UCD90910) (continued)

Encoding	Status Type
15	SEQ_OFF_TIMEOUT
16	FAN_FAULT
17	SYSTEM_WATCHDOG_TIMEOUT
18	VOUT_OV_FAULT_LATCH
19	VOUT_OV_WARN_LATCH
20	VOUT_UV_WARN_LATCH
21	VOUT_UV_FAULT_LATCH
22	TON_MAX_FAULT_LATCH
23	TOFF_MAX_WARN_LATCH
24	IOUT_OC_FAULT_LATCH
25	IOUT_OC_WARN_LATCH
26	IOUT_UC_FAULT_LATCH
27	TEMP_OT_FAULT_LATCH
28	TEMP_OT_WARN_LATCH
29	SEQ_ON_TIMEOUT_LATCH
30	SEQ_OFF_TIMEOUT_LATCH
31	FAN_FAULT_LATCH
32	SYSTEM_WATCHDOG_TIMEOUT_LATCH

Table 107. Status Types (UCD90120A and UCD9090)

Encoding	Status Type
0	POWER_GOOD
1	MARGIN_EN
2	MRG_LOW_nHIGH
3	VOUT_OV_FAULT
4	VOUT_OV_WARN
5	VOUT_UV_WARN
6	VOUT_UV_FAULT
7	TON_MAX_FAULT
8	TOFF_MAX_WARN
9	IOUT_OC_FAULT
10	IOUT_OC_WARN
11	IOUT_UC_FAULT
12	TEMP_OT_FAULT
13	TEMP_OT_WARN
14	SEQ_ON_TIMEOUT
15	SEQ_OFF_TIMEOUT
16	SYSTEM_WATCHDOG_TIMEOUT
17	VOUT_OV_FAULT_LATCH
18	VOUT_OV_WARN_LATCH
19	VOUT_UV_WARN_LATCH
20	VOUT_UV_FAULT_LATCH
21	TON_MAX_FAULT_LATCH
22	TOFF_MAX_WARN_LATCH
23	IOUT_OC_FAULT_LATCH
24	IOUT_OC_WARN_LATCH

Table 107. Status Types (UCD90120A and UCD9090) (continued)

Encoding	Status Type
25	IOUT_UC_FAULT_LATCH
26	TEMP_OT_FAULT_LATCH
27	TEMP_OT_WARN_LATCH
28	SEQ_ON_TIMEOUT_LATCH
29	SEQ_OFF_TIMEOUT_LATCH
30	SYSTEM_WATCHDOG_TIMEOUT_LATCH

Table 108. Status Types (UCD90160)

Encoding	Status Type
0	POWER_GOOD
1	MARGIN_EN
2	MRG_LOW_nHIGH
3	VOUT_OV_FAULT
4	VOUT_OV_WARN
5	VOUT_UV_WARN
6	VOUT_UV_FAULT
7	TON_MAX_FAULT
8	TOFF_MAX_WARN
9	SEQ_ON_TIMEOUT
10	SEQ_OFF_TIMEOUT
11	SYSTEM_WATCHDOG_TIMEOUT
12	VOUT_OV_FAULT_LATCH
13	VOUT_OV_WARN_LATCH
14	VOUT_UV_WARN_LATCH
15	VOUT_UV_FAULT_LATCH
16	TON_MAX_FAULT_LATCH
17	TOFF_MAX_WARN_LATCH
18	SEQ_ON_TIMEOUT_LATCH
19	SEQ_OFF_TIMEOUT_LATCH
20	SYSTEM_WATCHDOG_TIMEOUT_LATCH

10.40.17 GPO Configuration Examples

Example 1: GPO = POWER_GOOD(0) *AND* POWER_GOOD(2) *AND* POWER_GOOD(5) *AND* POWER_GOOD(7) *AND* POWER_GOOD(8)

Status Mask 0 = 0x01A3
Status Inversion Mask 0 = 0x0000
GPI Mask 0 = 0x00
Status Type Select 0 = 0

Status Mask 1 = 0x0000
GPI Mask 1 = 0x00

Status Mask 2 = 0x0000
GPI Mask 2 = 0x00

Status Mask 3 = 0x0000

GPI Mask 3 = 0x00

Example 2: GPO = (*NOT* POWER_GOOD[0]) *OR* (*NOT* POWER_GOOD[2]) *OR* (*NOT* POWER_GOOD[5]) *OR* (*NOT* POWER_GOOD[7])

Status Mask 0 = 0x0001
Status Inversion Mask 0 = 0x0001
GPI Mask 0 = 0x00
Status Type Select 0 = 0

Status Mask 1 = 0x0004
Status Inversion Mask 1 = 0x0004
GPI Mask 1 = 0x00
Status Type Select 1 = 0

Status Mask 2 = 0x0020
Status Inversion Mask 2 = 0x0020
GPI Mask 2 = 0x00
Status Type Select 2 = 0

Status Mask 3 = 0x0080
Status Inversion Mask 3 = 0x0080
GPI Mask 3 = 0x00
Status Type Select 3 = 0

Example 3: GPO = ((*NOT* POWER_GOOD[0]) *AND* (*NOT* GPI[3])) *OR* ((*NOT* POWER_GOOD[1]) *AND* (*NOT* GPI[3])) *OR* (VOUT_OV_WARN[2] *AND* (*NOT* GPI[3]))

Status Mask 0 = 0x0001
Status Inversion Mask 0 = 0x0001
GPI Mask 0 = 0x04
GPI Inversion Mask 0 = 0x04
Status Type Select 0 = 0

Status Mask 1 = 0x0002
Status Inversion Mask 1 = 0x0002
GPI Mask 1 = 0x04
GPI Inversion Mask 1 = 0x04
Status Type Select 1 = 0

Status Mask 2 = 0x0004
Status Inversion Mask 2 = 0x0004
GPI Mask 2 = 0x04
GPI Inversion Mask 2 = 0x04
Status Type Select 2 = 3

Status Mask 3 = 0x0000
GPI Mask 3 = 0x00

Example 4: GPO = (GPI[0] *AND* GPI[2]) *OR* (GPI[0] *AND* (*NOT* GPI[4]) *AND* (*NOT* GPI[7]) *OR* GPI[3] *OR* GPI[7]

Status Mask 0 = 0x0000
GPI Mask 0 = 0x05
GPI Inversion Mask 0 = 0x00

Status Mask 1 = 0x0000
GPI Mask 1 = 0x91

GPI Inversion Mask 1 = 0x90

Status Mask 2 = 0x0000
GPI Mask 2 = 0x04
GPI Inversion Mask 2 = 0x00

Status Mask 3 = 0x0000
GPI Mask 3 = 0x80
GPI Inversion Mask 3 = 0x00

Example 5: GPO = VOUT_OV_WARN[1] *AND* IOUT_OC_WARN[1]

Cannot implement this directly. Apply the relationship (a AND b) = (a' OR b')' = >
GPO = *NOT* ((*NOT* VOUT_OV_WARN[1]) *OR* (*NOT* IOUT_OC_WARN[1]))

Status Mask 0 = 0x0002
Status Inversion Mask 0 = 0x0002
GPI Mask 0 = 0x00
Status Type Select 0 = 4

Status Mask 1 = 0x0002
Status Inversion Mask 1 = 0x0002
GPI Mask 1 = 0x00
Status Type Select 1 = 16

Status Mask 2 = 0x0000
GPI Mask 2 = 0x00

Status Mask 3 = 0x0000
GPI Mask 3 = 0x00

Note UCD90120, UCD90124, and UCD90910): The first NOT, the one that applies to the entire equation, is actually handled by configuring the GPO's polarity backwards.

10.41 (F9h) GPI_CONFIG (MFR_SPECIFIC_41)

This Read/Write Block command configures the functionality for the input pins (GPI). For devices other than UCD90240, up to 8 pins (S through Z) may be configured as GPI.

Table 109. GPI_CONFIG Command Format UCD90120, UCD90124, and UCD90910)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = F9
1	0		BYTE_COUNT = 13
2	1	0	Input Pin S Configuration
3	2	1	Input Pin T Configuration
4	3	2	Input Pin U Configuration
5	4	3	Input Pin V Configuration
6	5	4	Input Pin W Configuration
7	6	5	Input Pin X Configuration
8	7	6	Input Pin Y Configuration
9	8	7	Input Pin Z Configuration
10	9	8	Sequence Timeout Pin Selection
11	10	9	Latched Statuses Clear Pin Selection
12	11	10	"Margin Enable" (MRG_EN) Pin Selection
13	12	11	"Margin Low/Not-High" (MRG_LOW_nHIGH) Pin Selection

Table 109. GPI_CONFIG Command Format UCD90120, UCD90124, and UCD90910) (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
14	13	12	Fans Installed Pin Selection

Table 110. GPI_CONFIG Command Format (UCD90910)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = F9
1	0		BYTE_COUNT = 12
2	1	0	Input Pin S Configuration
3	2	1	Input Pin T Configuration
4	3	2	Input Pin U Configuration
5	4	3	Input Pin V Configuration
6	5	4	Input Pin W Configuration
7	6	5	Input Pin X Configuration
8	7	6	Input Pin Y Configuration
9	8	7	Input Pin Z Configuration
10	9	8	Latched Statuses Clear Pin Selection
11	10	9	“Margin Enable” (MRG_EN) Pin Selection
12	11	10	"Margin Low/Not-High” (MRG_LOW_nHIGH) Pin Selection
13	12	11	Fans Installed Pin Selection

Table 111. GPI_CONFIG Command Format (Devices UCD9090A and UCD90160A Only)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = F9
1	0		BYTE_COUNT = 31
2	1	0	Input Pin S Configuration
3	2	1	Input Pin T Configuration
4	3	2	Input Pin U Configuration
5	4	3	Input Pin V Configuration
6	5	4	Input Pin W Configuration
7	6	5	Input Pin X Configuration
8	7	6	Input Pin Y Configuration
9	8	7	Input Pin Z Configuration
10	9	8	Fault Enable Flags
11	10	9	Latched Statuses Clear Pin Selection
12	11	10	“Margin Enable” (MRG_EN) Pin Selection
13	12	11	“Margin Low/Not-High” (MRG_LOW_nHIGH) Pin Selection
14	13	12	Fans Installed Pin Selection
15	14	13	GPI Fault response Pin Selection
16	15	14	Fault Responses Byte
17	16	15	PAGE Mask for GPI fault(High Byte)
18	17	16	PAGE Mask for GPI fault(Low Byte)
19	18	17	Maximum Glitch time for GPI(high byte)
20	19	18	Maximum Glitch time for GPI(low byte)

Table 111. GPI_CONFIG Command Format (Devices UCD9090A and UCD90160A Only) (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
21	20	19	Fault Pin Function Pin Selection
22	21	20	Fault Responses Byte for Fault Pin
23	22	21	PAGE Mask for Fault pin response(High Byte)
24	23	22	PAGE Mask for Fault pin response(Low Byte)
25	24	23	Maximum Glitch time for Fault pin(high byte)
26	25	24	Maximum Glitch time for Fault pin (low byte)
27	26	25	Page Mask for Fault pin output(High Byte)
28	27	26	Page Mask for Fault pin output(Low Byte)
29	28	27	Debug Mode Pin Selection
30	29	28	Cold Boot Mode Pin Selection
31	30	29	Cold Boot Timeout
32	31	30	Normal Boot Start Delay

Table 112. GPI_CONFIG Command Format (Devices Other Than UCD90120, UCD90124, UCD90910, and UCD90240)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = F9
1	0		BYTE_COUNT = 13
2	1	0	Input Pin S Configuration
3	2	1	Input Pin T Configuration
4	3	2	Input Pin U Configuration
5	4	3	Input Pin V Configuration
6	5	4	Input Pin W Configuration
7	6	5	Input Pin X Configuration
8	7	6	Input Pin Y Configuration
9	8	7	Input Pin Z Configuration
10	9	8	Fault Enable Flags
11	10	9	Latched Statuses Clear Pin Selection
12	11	10	“Margin Enable” (MRG_EN) Pin Selection
13	12	11	"Margin Low/Not-High” (MRG_LOW_nHIGH) Pin Selection
14	13	12	Fans Installed Pin Selection

Table 113. GPI_CONFIG Command Format (UC90240)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = F9
1	0		BYTE_COUNT = 31
2	1	0	GPI_0 Pin Configuration
3	2	1	GPI_1 Pin Configuration
4	3	2	GPI_2 Pin Configuration
5	4	3	GPI_3 Pin Configuration
6	5	4	GPI_4 Pin Configuration
7	6	5	GPI_5 Pin Configuration

Table 113. GPI_CONFIG Command Format (UC90240) (continued)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
8	7	6	GPI_6 Pin Configuration
9	8	7	GPI_7 Pin Configuration
10	9	8	GPI_8 Pin Configuration
11	10	9	GPI_9 Pin Configuration
12	11	10	GPI_10 Pin Configuration
13	12	11	GPI_11 Pin Configuration
14	13	12	GPI_12 Pin Configuration
15	14	13	GPI_13 Pin Configuration
16	15	14	GPI_14 Pin Configuration
17	16	15	GPI_15 Pin Configuration
18	17	16	GPI_16 Pin Configuration
19	18	17	GPI_17 Pin Configuration
20	19	18	GPI_18 Pin Configuration
21	20	19	GPI_19 Pin Configuration
22	21	20	GPI_20 Pin Configuration
23	22	21	GPI_21 Pin Configuration
24	23	22	GPI_22 Pin Configuration
25	24	23	GPI_23 Pin Configuration
26	25	24	Fault Enable Flags – Byte 0 (LSB)
27	26	25	Fault Enable Flags – Byte 1
28	27	26	Fault Enable Flags – Byte 2
29	28	27	Latched Statuses Clear Pin Selection
30	29	28	“Margin Enable” (MRG_EN) Pin Selection
31	30	29	“Margin Low/Not-High” (MRG_LOW_nHIGH) Pin Selection
32	31	30	Fans Installed Pin Selection

10.41.1 Input Pin S-Z Configuration

These bytes configure which pin is used for each GPI and its polarity. For details, see Section 7. A mode other than “Unused” or “Input” causes this command to be rejected (receive a NACK).

NOTE:

1. The input pin configurations, if used, must start in the Input Pin S Configuration byte and continue in consecutive order with no gaps. That is, no Unused-Mode Pin Configurations can be placed between any Input-Mode Pin Configurations.
2. When using a GPI as an input to the logic of a GPO (see the GPO_CONFIG command), be aware that there are two types of GPIs: Low Latency GPIs and regular GPIs. For Low Latency GPIs, the worst-case GPI-to-GPO delay time is 200 µs. For regular GPIs, the worst-case GPI-to-GPO delay time is 1 ms. For devices other than UCD90240, Low Latency GPI pins are the last 8 pins listed in the Pin ID tables (see Table 14 and Table 15). The order of these 8 Pin IDs is aligned with the order of the 8 GPIs. Only when the GPI and the assigned Pin ID have the same order, the GPI has the fast response feature. For example, Pin ID 21 from Table 14 is the 4th pin among the last 8 pins; it must be assigned to GPI V, the 4th GPI, to have the fast response feature. For UCD90240, all GPIs are Low Latency GPIs and do not have the previously stated pin alignment requirement.

10.41.2 Fault Enable Flags

When a bit is set, the de-assertion of the corresponding GPI is treated as a fault. This fault will be noted in the MFR_STATUS command (see Section 10.35) and will be logged if configured to do so (see LOGGED_FAULT_DETAIL_ENABLES). When a GPI fault occurs, the PMBALERT# pin is asserted.

UCD90240: GPI_FAULT_RESPONSE(0xF4) works only if the corresponding GPI bit is set here.

Table 114. Fault Enable Bits (UCD90240)

Byte 0 Bit	7	6	5	4	3	2	1	0
Purpose	GPI 7	GPI 6	GPI 5	GPI 4	GPI 3	GPI 2	GPI 1	GPI 0
Byte 1 Bit	7	6	5	4	3	2	1	0
Purpose	GPI 15	GPI 14	GPI 13	GPI 12	GPI 11	GPI 10	GPI 9	GPI 8
Byte 2 Bit	7	6	5	4	3	2	1	0
Purpose	GPI 23	GPI 22	GPI 21	GPI 20	GPI 19	GPI 18	GPI 17	GPI 16

Table 115. Fault Enable Bits (other than UCD90240)

Bit	7	6	5	4	3	2	1	0
Purpose	GPI Z	GPI Y	GPI X	GPI W	GPI V	GPI U	GPI T	GPI S

10.41.3 Sequence Timeout Pin Selection (UCD90120 and UCD90124 Only)

The SEQ_TIMEOUT command (D0h) defines a window during which an external event is expected to occur. That event is defined by the Input Pin selected by this byte (see Table 116). The pin is ignored if the value of this byte is zero or the SEQ_TIMEOUT window is set to 0.

Table 116. GPI Selection (UCD90120 and UCD90124 Only)

Value	Description
0	Unused
1	Input Pin S Configuration
2	Input Pin T Configuration
3	Input Pin U Configuration
4	Input Pin V Configuration
5	Input Pin W Configuration
6	Input Pin X Configuration
7	Input Pin Y Configuration
8	Input Pin Z Configuration
9-255	Invalid

10.41.4 Latched Statuses Clear Pin Selection

The latched status types (_LATCH) in the GPO_CONFIG command can be cleared by a pin. That Input Pin is selected by this byte (see Table 116). The pin is ignored if the value of this byte is 0.

NOTE: With the UCD90120 and UCD90124 devices, this pin is level-sensitive. With all other devices, this pin is edge-sensitive.

10.41.5 MRG_EN Pin Selection

Margining can be enabled with the Input Pin selected by this byte (see Table 116). The pin is ignored if the value of this byte is 0.

When this pin is asserted, all rails with margining enabled (see MARGIN_CONFIG, Section 10.37) are put in a margined state (low or high).

NOTE: If a pin is selected in this byte, another pin must be selected in the MRG_LOW_nHIGH byte as well.

10.41.6 MRG_LOW_nHIGH Pin Selection

The margining level (low or high) can be selected with the Input Pin selected by this byte (see Table 116). The pin is ignored if the value of this byte is 0.

When this pin is asserted, and the MRG_EN pin is asserted, all rails with margining enabled (see Table 116) will be pit in the margin-low state.

When this pin is not asserted and the MRG_EN pin is asserted, all rails with margining enabled will be put in the margin-high state.

10.41.7 Fans Installed Pin Selection

Whether or not fans are installed can be determined with the Input Pin selected by this byte (see Table 94). The pin is ignored if the value of this byte is 0.

When a valid pin is selected with this byte, all configuration and control of fans are ignored if this pin is not asserted (see FAN_CONFIG).

NOTE: When valid, this pin is only looked at during start-up. The fans are configured and enabled then, or not based on this pin.

10.41.8 GPI Fault Response Pin Selection

GPI fault response can be enabled with the Input Pin identified by this byte (see Table 94) if the corresponding fault enable bit is also set (see Section 10.40.2). The pin is ignored if the value of this byte is 0.

When this pin is changed from asserted to de-asserted, the corresponding fault response is performed.

10.41.9 Fault Response Byte

See Section 10.25.1 for the byte definition of Fault response byte. For the retry response, the time between retry is defined in Section 10.25.3.

10.41.10 Page Mask for GPI fault

The page mask is made up of two bytes whose bits are defined as follows:

Bit	15	14	13	12	11	10	9	8
Purpose	PAGE15	PAGE14	PAGE13	PAGE12	PAGE11	PAGE10	PAGE9	PAGE8
Bit	7	6	5	4	3	2	1	0
Purpose	PAGE7	PAGE6	PAGE5	PAGE4	PAGE3	PAGE2	PAGE1	PAGE0

Each bit selects which page(s) respond to GPI fault. Setting the bit associated with a given page to 1 enables fault response for that page. If the bit associated with a page is set to 0, the page does not respond the GPI fault.

10.41.11 Maximum Glitch Time For GPI

The value in these bytes is multiplied by 500 µs to get the Maximum glitch of GPI input if the GPI is used for fault response

10.41.12 Fault Pin Function Pin Selection

The Fault Pin can be enabled with the input pin identified by this bytes if the corresponding fault enable bit is also set (see Section 10.40.2). The pin is ignored if the value of the byte is 0. When the fault pin is on, the pin is active as a input to monitor the external event, if there is any internal rail faults, the device pulls the pin low to notify the other devices. When the fault is gone, the device releases the pin and continues the monitoring function on the assigned pin.

10.41.13 Fault Response Byte for Fault Pin

See Section 10.25.1 for the byte definition of Fault response byte. For the retry response, the time between retry is defined in Section 10.25.3.

10.41.14 PAGE Mask for Fault Pin Response

This page mask has the exact same function, format as Page Mask for GPI defined in Section 10.40.10.

10.41.15 Maximum Glitch Time for Fault Pin

This glitch time has the exact same function and format as Maximum Glitch for GPI defined in Section 10.40.11.

10.41.16 Page Mask for Fault Pin Output

The page mask is made up of two bytes whose bits are defined as follows:

Bit	15	14	13	12	11	10	9	8
Purpose	PAGE15	PAGE14	PAGE13	PAGE12	PAGE11	PAGE10	PAGE9	PAGE8
Bit	7	6	5	4	3	2	1	0
Purpose	PAGE7	PAGE6	PAGE5	PAGE4	PAGE3	PAGE2	PAGE1	PAGE0

Each bit selects which page(s) pulls the fault pin low when it has fault. Setting the bit associated with a given page to 1 enables fault pin output for that page. If the bit associated with a page is set to 0, the page does not pull the fault pin low when it has fault.

The following faults impact fault pin output:

RESEQUENCE_ ERROR	SEQ_ON_TIMEOUT	SEQ_OFF_TIMEOUT	OT_FAULT*	IOUT_OC_FAULT*
IOUT_UC_FAULT*	VOUT_UV_FAULT	VOUT_OV_FAULT	TON_MAX_FAULT	
* These are only available if the devices support temperature or current.				

10.41.17 GPI Debug Mode Pin Selection

GPI debug Function can be enabled with the input pin identified by this byte. The pin is ignored if the value of the byte is 0. Under Debug Mode, device shall not active PMBus alert pin for any faults/warnings, not response for any fault responses and not log any faults. This function is mainly designed for debug purpose and it is not recommended in the final production.

The following faults and warnings are impacted by impacted by degub mode:

VOUT_OV_FAULT	TON_MAX	IOUT_UC*	SYSTEM_WATCHDOG_TIMEOUT
VOUT_OV_WARNING	TOFF_MAX Warning	OT_FAULT*	RESEQUENCE_ERROR
VOUT_UV_FAULT	IOUT_OC_FAULT*	OT_WARNING*	SLAVE_FAULT
VOUT_UV_WARNING	IOUT_OC_WARNING*	SEQ_ON_TIMEOUT	SEQ_OFF_TIMEOUT
All GPI de-asserted			
* These are only available if the devices support temperature or current.			

When the debug mode is on, the rail sequence on/off dependency conditions are ignored, as soon as the sequence on/off timeout is expired, the rails will be sequenced on or off accordingly regardless of the timeout action, if the sequence on/off timeout value is set to 0, the rails will be sequenced on or off immediately. The fault pin shall not pull the fault bus low when debug mode is on. Moreover LGPO affected by these events should be back to its original states when debug mode is on.

10.41.18 Cold Boot Mode Pin Selection

Cold boot mode is a feature used to heat-up the system by turning on some particular rails for certain amounts of time when the system is under an extreme code temperature. UCD device is communicated with the system via particular GPI (thermal state GPI) which is output from a thermal device. Cold boot-up mode is only entering once per UCD reset. There is no system watch dog Reset during the cold boot-up mode. For the rest functions, device behaves the same when under cold boot-up mode.

Cold Boot mode can be enabled with the pin identified by this byte. The pin is ignored if the value of the byte is 0. When this byte is set to non-zero, the assigned GPI is defined as thermal state GPI. During the UCD9090A boot-up, it reads the thermal state GPI to determine whether it should start cold boot-up or not. When the input of thermal state GPI is DE-ASSERTED, device enters cold boot mode otherwise device enters normal mode. Device logs a GPI fault if the thermal state GPI is at DE_ASSERTED state after device is out of reset if the GPI fault log enable bit is set. The following changes on the thermal state GPI shall not introduce any logging. Only one GPI can be assigned for this function and one it is assigned, it cannot be used for any other GPI functions.

The rails used in the cold boot-up mode are configurable. For those rails **with** Sequence On Dependency on the thermal state GPI, they (non-cold boot-up rails) are not powered-up during the cold boot-up since the dependency is not met. But non-cold boot-up rails will be power-on under normal mode since thermal state GPI is treated as ASSERTED when cold boot-up mode is over. For those rails **without** sequence on dependency on the thermal state GPI, they (cold boot-up rails) are power-on on both cold boot-up and normal mode. It is application's responsibility to set the proper ON_OFF_CONFIG for those cold boot-up rails. Cold boot-up rails are not power-on if their ON_OFF_CONFIG settings are not met under cold boot mode.

Once the Cold boot-up is over, device stops monitoring the thermal state GPI, which is treated as ASSERTED afterward. Device shutdowns all cold boot-up rails which have EN pin associated immediately. For those cold boot-up rail without EN pin associated, device does not shutdown them. When all cold boot-up rails with EN pin are below power good off threshold, device waits the programmable delay (see Section 10.41.20) to repower on all rails. The On-Off-Config conditions and turn on dependencies must be met for the rails to be on properly. The following logic applies to cold boot mode operation:

```
If system temperature is < threshold deg C (Thermal State GPI)
     If yes(DE_ASSERTED), then:
          Log GPI fault
          Start Cold Boot Timeout
          No System Watchdog output
          Ramp up the power supplies based on on_off_config
          Wait for thermal state GPI ASSERTED OR "Cod boot Timeout expire"
          Disable the thermostat input listening mode
          Force to shutdown down all cold boot rails with EN control immediately
          Wait for all cold boot rails with EN control below POWER_GOOD_OFF
          Start and wait Start Delay after cold boot
Disable the thermostat input listening mode
Treat Thermal State GPI ASSERTED
Ramp up power supplies based on on_off_config
```

10.41.19 Cold Boot Mode Timeout

Cold boot mode timeout is only valid if the cold boot mode pin selection is set to a valid number. This byte is used to tell how long the device shall stay at the cold boot-up before it stops listening the thermal state GPI and shutdown all rails. If this byte is set to 0, device stays at the cold boot-up mode until the thermal state GPI is ASSERTED. The range is from 0-255minutes with step 1minutes. Cold boot mode timeout should never be reset unless UCD is reset.

10.41.20 Normal Boot Start Delay

This byte is only valid if the cold boot mode pin selection is set to a valid number. NORMAL_BOOT_START_DELAY is used to tell how long the UCD9090A should wait to ramp up the powers after the cold boot up is over. The start delay does not start until all cold-boot rails with EN pins power down during the cold boot mode are at POWER_GOOD_OFF. If NORMAL_BOOT_START_DELAY is set to 0, UCD should turn on rails as fast as it can after all rails are at POWER_GOOD_OFF state. This byte is formatted according the 8-bit time encoding defined in Section 2.5.

10.42 (FAh) GPIO_SELECT (MFR_SPECIFIC_42)

This read/write byte command determines to which GPIO that the GPIO_CONFIG command applies. For the UCD90240, the value must be in the range from 0 to 23, and is equal to the Pin ID 60 to 83 from Table 13.

For all other models, the value passed must a valid Pin ID from 0 to 25.

See Table 14 or Table 15.

10.43 (FBh) GPIO_CONFIG (MFR_SPECIFIC_43)

This Read/Write Byte Command configures the GPIO identified by the GPIO_SELECT command. The Status bit is read-only and gives the current state of the pin. The Out_Enable bit determines if the pin is an output (1 – actively driven) or an input (0 – high impedance). The Out_Value bit determines the state of the pin when it is configured as an output. The Enable bit is a flag indicating whether this command should be processed. When the Enable bit is cleared, this command is ignored. If user wants to temporarily change to an output pin's state, this command should be written twice. In the first time, the Enable bit should be set to 1 such that the changes can be applied. In the second time, the Enable bit should be set to 0. This will not change the pin's state; and because the Enable bit is 0, STORE_DEFAULT_ALL command will ignore this command when storing configurations from RAM to flash. This way, the new temporary configuration will not overwrite the default configuration.

Bit	7	6	5	4	3	2	1	0
Purpose	Reserved	Reserved	Reserved	Reserved	Status	Out_Value	Out_Enable	Enable

This configuration is stored to nonvolatile memory with the STORE_DEFAULT_ALL command. If the pin is configured as an output, it can take a very short time after a reset or power-cycle for the pin to reach the configured state. (The approximate, typical boot time is 15 milliseconds. For the UCD90120, UCD90124, and UCD90910, this may on occasion take up to 200 milliseconds, if the log memory has to be erased.)

NOTE: Configuring a pin that is also being used by another function (enable, fan control, and so forth) may likely result in unexpected and unwanted behavior.

10.44 (FCh) MISC_CONFIG (MFR_SPECIFIC_44)

This Read/Write Block Command configures features not covered by other commands.

Table 117. MISC_CONFIG Command Format (other than UCD90240)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = FC
1	0		BYTE_COUNT = 2
2	1	0	Miscellaneous Configuration Byte
3	2	1	Time between Resequences

Table 118. MISC_CONFIG Command Format (UCD9090A and UCD90160A only)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = FC
1	0		BYTE_COUNT = 4
2	1	0	Miscellaneous Configuration Byte
3	2	1	Time between Resequences
4	3	2	Resequences_rail_mask(high byte)
5	4	3	Resequences_rail_mask(low byte)

Table 119. MISC_CONFIG Command Format (UCD90240 only)

Byte Number (Write)	Byte Number (Read)	Payload Index	Description
0			CMD = FC
1	0		BYTE_COUNT = 2
2	1	0	Miscellaneous Configuration Byte
3	2	1	Time between Re-Sequences
4	3	2	External Reference Voltage(low byte)
5	4	3	External Reference Voltage(high byte)

10.44.1 Miscellaneous Configuration Byte

The bit definitions for the Miscellaneous Configuration Byte are shown in Table 120.

Table 120. Miscellaneous Configuration Byte

Bit(s)	Name	Description
7	Resequence Continuously	When this bit is set, there is no limit to the number of times that the device will attempt to resequence. The “Max Resequences” value does not apply.
6	Resequence Abort	If a TOFF_MAX_WARN warning occurs during resequencing, stop the resequencing operation
5:4	Max Re-Sequences	The maximum number of times to attempt to re-sequence. b'00 – 1 time b'01 – 2 times b'10 – 3 times b'11 – 4 times See Section 10.25.2 for more information.
3	Reserved	
2	Enable Log FIFO	When this bit is set, all or part of the LOGGED_FAULT_DETAIL is treated as a FIFO, depending on the "FIFO Entire Log" bit.
1	FIFO Entire Log	When this bit and the "Enable Log FIFO" bit are set, the entire LOGGED_FAULT_DETAIL is treated as a FIFO. When this bit is cleared and the "Enable Log FIFO" bit is set, the last half of the LOGGED_FAULT_DETAIL is treated as a FIFO.
0	brownout enable mode	Enables the brownout mode function which allows information (faults, peaks, run-time clock , and so forth) to be saved to flash only when the device is powered down. When this is not enabled, firmware must periodically update this information in flash. See the data sheet for details regarding the external circuitry required to support this feature.

Table 121. Miscellaneous Configuration Byte(UCD90160A and UCD9090A)

Bit(s)	Name	Description
7	Re-sequence Continuously	When this bit is set, there is no limit to the number of times that the device will attempt to resequence. The “Max Resequences” value does not apply.
6	Re-sequence Abort	If a rail fails to turn off during re-sequencing, stop the re-sequencing operation
5:4	Max Re-Sequences	The maximum number of times to attempt to re-sequence. b'00 – 1 time b'01 – 2 times b'10 – 3 times b'11 – 4 times See Section 10.25.2 for more information.
3	Flash_Log_Disable	When this bit is set, log(Fault, Peak and RTC) is only stored into the volatile memory and the non-volatile memory is not updated. When this bit is clear, log is stored into both volatile and non-volatile memory. Reset is required after the bit is toggled.
2	Enable Log FIFO	When this bit is set, all or part of the LOGGED_FAULT_DETAIL is treated as a FIFO, depending on the "FIFO Entire Log" bit.
1	FIFO Entire Log	When this bit and the "Enable Log FIFO" bit are set, the entire LOGGED_FAULT_DETAIL is treated as a FIFO. When this bit is cleared and the "Enable Log FIFO" bit is set, the last half of the LOGGED_FAULT_DETAIL is treated as a FIFO.
0	brownout enable mode	Enables the brownout mode function which allows information (faults, peaks, run-time clock , and so forth) to be saved to flash only when the device is powered down. When this is not enabled, firmware must periodically update this information in flash. See the data sheet for details regarding the external circuitry required to support this feature.

Table 122. Miscellaneous Configuration Byte (UCD90240 Only)

Bit(s)	Name	Description
7	Resequence Continuously	When this bit is set, there is no limit to the number of times that the device will attempt to resequence. The “Max Resequences” value does not apply.
6	Resequence Abort	If a rail fails to turn off during resequencing, stop the resequencing operation

Table 122. Miscellaneous Configuration Byte (UCD90240 Only) (continued)

Bit(s)	Name	Description
5:4	Max Resequences	The maximum number of times to attempt to re-sequence. b'00 – 1 time b'01 – 2 times b'10 – 3 times b'11 – 4 times See Section 10.25.2 for more information.
3	Slave	When this bit is set, the device is a slave to take external sync clock. This bit is only valid if it is under multi-chip user case.
2	Enable Log FIFO	When this bit is set, all or part of the LOGGED_FAULT_DETAIL is treated as a FIFO, depending on the "FIFO Entire Log" bit.
1	External ADC Reference	When this bit is set, the external ADC reference(2.4 V–3.0 V) is used for ADC, see Section 10.44.3. A device reset is required after this bit is changed(1).
0	Reserved	

(1) It is application's responsibility to make sure external reference is in place before setting this bit. Otherwise ADC results is unpredictable.

10.44.2 Time Between Resequences

UCD90120 and UCD90124: The value in this byte is multiplied by 5 ms to get the "Time between resequences".

For devices other than the UCD90120 and UCD90124, this byte is formatted according to Section 2.5.

10.44.3 External Reference Voltage

This is supported by UCD90240 only. This field defines the external ADC reference voltage and it follows LINEAR format defined in Section 2.2. The reference voltage should be between 2.4 V and 3 V with 0.01-V resolution.

10.44.4 Resequence_rails_mask

The page mask is made up of two bytes whose bits are defined as follows:

Bit	15	14	13	12	11	10	9	8
Purpose	PAGE15	PAGE14	PAGE13	PAGE12	PAGE11	PAGE10	PAGE9	PAGE8

Bit	7	6	5	4	3	2	1	0
Purpose	PAGE7	PAGE6	PAGE5	PAGE4	PAGE3	PAGE2	PAGE1	PAGE0

NOTE: This table assumes that the device supports 16 rails (0 to 15). For a given device, this may not be the case. The interpretation of this information should be adjusted for the correct number of rails.This table assumes that the device supports 16 rails (0 to 15). For a given device, this may not be the case. The interpretation of this information should be adjusted for the correct number of rails.

Each bit selects which page(s) should be not checked its POWER_GOOD_OFF and TOFF_WARN status when performing re-sequence. When the corresponding page bit is set to 1, the re-sequence engine does not check its POWER_GOOD_OFF and TOFF_WARN status. When the corresponding page bit is set to 0, the resequence engine checks its POWER_GOOD_OFF and TOFF_WARN status.

10.45 (FDh) DEVICE_ID (MFR_SPECIFIC_45)

This Read-only Block Read command returns an ASCII string up to 32 characters in length. It is divided into three or four sections, separated by the vertical bar character ('|'). The format within each section may change in future releases; therefore, support tools must not rely on specific byte alignment. Instead they must identify the sections and sub-sections using the vertical bar and the periods that separate them.

1. The first section is the hardware device ID (for example, 'UCD90xxx ").
2. The second section contains the firmware version information.

   Its format is "A.BB.C.DDDD", where:

   A = Major Release Level (1 character)
   BB = Minor Release Level (2 characters)
   C = Sub-Release (1 character)
   DDDD = Build Number (4 characters)

   The major and minor release numbers are incremented immediately after each official firmware release.

   The sub-release field allows for branching off the main development path to build updates based on older versions.

   The build number is automatically updated every time firmware is compiled. The value does not reset to 0 when the release level is updated. Several prerelease versions of firmware can have the same major, minor, and sub-release numbers. These different prerelease versions may be distinguished by the build number.
3. The third section contains the firmware compilation date.
   The date is reported in YYMMDD format, similar to the MFR_DATE command.
4. The optional fourth section may contain device-specific information.

Example: A typical DEVICE_ID string is "UCD90120|2.04.0.0069|070509". In this example,

Hardware device	= UCD90120
Firmware Major Release	= 2
Firmware Minor Release	= 04
Firmware Sub-Release	= 0
Firmware Build Number	= 69
Firmware Build Date	= May 9, 2007

11 Range Checking and Limits

Table 123 shows the numerical limits for all the supported PMBus commands.

Table 123. Range and Limits for PMBus Commands

Code (hex)	Command	Minimum	Maximum	Hardcoded Default	Comments
0	PAGE	0	13 or 255	0	
1	OPERATION	See comments	See comments	0	The seven meaningful values for this parameter are 0x00, 0x40, 0x80, 0x94, 0x98, 0x98, 0xA4 and 0xA8.
2	ON_OFF_CONFIG	See comments	See comments	0	>0x20 invalid, all others accepted
3	CLEAR_FAULTS	n/a	n/a	n/a	Write Only
4	PHASE				Not Supported
05-0F	Reserved				
10	WRITE_PROTECT				Not Supported
11	STORE_DEFAULT_ALL	n/a	n/a	n/a	Write Only
12	RESTORE_DEFAULT_ALL	n/a	n/a	n/a	Write Only
13	STORE_DEFAULT_CODE				Not Supported
14	RESTORE_DEFAULT_CODE				Not Supported
15	STORE_USER_ALL				Not Supported
16	RESTORE_USER_ALL				Not Supported
17	STORE_USER_CODE				Not Supported
18	RESTORE_USER_CODE				Not Supported
19	CAPABILITY	n/a	n/a	0xB0	Read Only
1A	QUERY				Not Supported
1B-1F	Reserved				
20	VOUT_MODE	–16	15	0	Five-bit, two's complement exponent
21	VOUT_COMMAND	0	See comment	0	Depends on VOUT_MODE
22	VOUT_TRIM				Not Supported
23	VOUT_CAL_OFFSET				Not Supported
24	VOUT_MAX				Not Supported
25	VOUT_MARGIN_HIGH	0	See comment	0	Depends on VOUT_MODE
26	VOUT_MARGIN_LOW	0	See comment	0	Depends on VOUT_MODE
27	VOUT_TRANSITION_RATE				Not Supported
28	VOUT_DROOP				Not Supported
29	VOUT_SCALE_LOOP				Not Supported
2A	VOUT_SCALE_MONITOR	0	See comment	0	Depends on VOUT_MODE
2B-2F	Reserved				
30	COEFFICIENTS				Not Supported
31	POUT_MAX				Not Supported
32	MAX_DUTY				Not Supported
33	FREQUENCY_SWITCH				Not Supported
34	Reserved				
35	VIN_ON				Not Supported
36	VIN_OFF				Not Supported
37	INTERLEAVE				Not Supported
38	IOUT_CAL_GAIN	0.6113	20000	0	A number from 20000 to 40031 results in 20000 because of internal resolution.
39	IOUT_CAL_OFFSET	–511.5	511.5	0	
3A	FAN_CONFIG_1_2				Not Supported
3B	FAN_COMMAND_1	0	100	0	
3C	FAN_COMMAND_2	0	100	0	
3D	FAN_CONFIG_3_4				Not Supported
3E	FAN_COMMAND_3	0	100	0	
3F	FAN_COMMAND_4	0	100	0	

Table 123. Range and Limits for PMBus Commands (continued)

Code (hex)	Command	Minimum	Maximum	Hardcoded Default	Comments
40	VOUT_OV_FAULT_LIMIT	0	See comment	0	Depends on VOUT_MODE
41	VOUT_OV_FAULT_RESPONSE				See FAULT_RESPONSES command
42	VOUT_OV_WARN_LIMIT	0	See comment	0	Depends on VOUT_MODE
43	VOUT_UV_WARN_LIMIT	0	See comment	0	Depends on VOUT_MODE
44	VOUT_UV_FAULT_LIMIT	0	See comment	0	Depends on VOUT_MODE
45	VOUT_UV_FAULT_RESPONSE				See FAULT_RESPONSES command
46	IOUT_OC_FAULT_LIMIT	–511.5	511.5	0	
47	IOUT_OC_FAULT_RESPONSE				See FAULT_RESPONSES command
48	IOUT_OC_LV_FAULT_LIMIT				Not Supported
49	IOUT_OC_LV_FAULT_RESPONSE				Not Supported
4A	IOUT_OC_WARN_LIMIT	–511.5	511.5	0	
4B	IOUT_UC_FAULT_LIMIT	–511.5	511.5	0	
4C	IOUT_UC_FAULT_RESPONSE				See FAULT_RESPONSES command
4D	Reserved				
4E	Reserved				
4F	OT_FAULT_LIMIT	–255.75	255.75	0	
50	OT_FAULT_RESPONSE				See FAULT_RESPONSES command
51	OT_WARN_LIMIT	–255.75	255.75	0	
52	UT_WARN_LIMIT				Not Supported
53	UT_FAULT_LIMIT				Not Supported
54	UT_FAULT_RESPONSE				Not Supported
55	VIN_OV_FAULT_LIMIT				Not Supported
56	VIN_OV_FAULT_RESPONSE				Not Supported
57	VIN_OV_WARN_LIMIT				Not Supported
58	VIN_UV_WARN_LIMIT				Not Supported
59	VIN_UV_FAULT_LIMIT				Not Supported
5A	VIN_UV_FAULT_RESPONSE				Not Supported
5B	IIN_OC_FAULT_LIMIT				Not Supported
5C	IIN_OC_FAULT_RESPONSE				Not Supported
5D	IIN_OC_WARN_LIMIT				Not Supported
5E	POWER_GOOD_ON	0	See comment	0	Depends on VOUT_MODE
5F	POWER_GOOD_OFF	0	See comment	0	Depends on VOUT_MODE
60	TON_DELAY	0	3276	0	
61	TON_RISE				Not Supported
62	TON_MAX_FAULT_LIMIT	0	3276	0	
63	TON_MAX_FAULT_RESPONSE				See FAULT_RESPONSES command
64	TOFF_DELAY	0	3276	0	
65	TOFF_FALL				Not Supported
66	TOFF_MAX_WARN_LIMIT	0	3276 or 0x7FFF	0	0x7FFF is a special value meaning there is no limit. See section 16.7 of the PMBus Specification.
67	Reserved				
68	POUT_OP_FAULT_LIMIT				Not Supported
69	POUT_OP_FAULT_RESPONSE				Not Supported
6A	POUT_OP_WARN_LIMIT				Not Supported
6B	PIN_OP_WARN_LIMIT				Not Supported
6C-77	Reserved				
78	STATUS_BYTE				Read Only
79	STATUS_WORD				Read Only
7A	STATUS_VOUT				Read Only
7B	STATUS_IOUT				Read Only
7C	STATUS_INPUT				Not Supported

Table 123. Range and Limits for PMBus Commands (continued)

Code (hex)	Command	Minimum	Maximum	Hardcoded Default	Comments
7D	STATUS_TEMPERATURE				Read Only
7E	STATUS_CML				Read Only
7F	STATUS_OTHER				Not Supported
80	STATUS_MFR_SPECIFIC				Not Supported
81	STATUS_FANS_1_2				Read Only
82	STATUS_FANS_3_4				Read Only
83-87	Reserved				
88	READ_VIN				Not Supported
89	READ_IIN				Not Supported
8A	READ_VCAP				Not Supported
8B	READ_VOUT				Read Only
8C	READ_IOUT				Read Only
8D	READ_TEMPERATURE_1				Read Only
8E	READ_TEMPERATURE_2				Read Only
8F	READ_TEMPERATURE_3				Not Supported
90	READ_FAN_SPEED_1	0	32767	0	Read Only
91	READ_FAN_SPEED_2	0	32767	0	Read Only
92	READ_FAN_SPEED_3	0	32767	0	Read Only
93	READ_FAN_SPEED_4	0	32767	0	Read Only
94	READ_DUTY_CYCLE				Not Supported
95	READ_FREQUENCY				Not Supported
96	READ_POUT				Not Supported
97	READ_PIN				Not Supported
98	PMBUS_REVISION				Read Only
99	MFR_ID	n/a	n/a	See comment	The default is an empty string, all zeros
9A	MFR_MODEL	n/a	n/a	See comment	The default is an empty string, all zeros
9B	MFR_REVISION	n/a	n/a	See comment	The default is an empty string, all zeros
9C	MFR_LOCATION	n/a	n/a	See comment	The default is an empty string, all zeros
9D	MFR_DATE	n/a	n/a	See comment	The default is an empty string, all zeros
9E	MFR_SERIAL	n/a	n/a	See comment	The default is an empty string, all zeros
9F	Reserved				
A0	MFR_VIN_MIN				Not Supported
A1	MFR_VIN_MAX				Not Supported
A2	MFR_IIN_MAX				Not Supported
A3	MFR_PIN_MAX				Not Supported
A4	MFR_VOUT_MIN				Not Supported
A5	MFR_VOUT_MAX				Not Supported
A6	MFR_IOUT_MAX				Not Supported
A7	MFR_POUT_MAX				Not Supported
A8	MFR_TAMBIENT_MAX				Not Supported
A9	MFR_TAMBIENT_MIN				Not Supported
AA-AF	Reserved				
B0-BF	USER_DATA_00 -USER_DATA_15				Not Supported
C0-CF	Reserved				
D0	SEQ_TIMEOUT(MFR_SPECIFIC_00)	0	3276	0	
D1	VOUT_CAL_MONITOR (MFR_SPECIFIC_01)	See comment	See comment	0	Depends on VOUT_MODE (Note this parameter is treated as a SIGNED variable)

Table 123. Range and Limits for PMBus Commands (continued)

Code (hex)	Command	Minimum	Maximum	Hardcoded Default	Comments
D2	SYSTEM_RESET_CONFIG (MFR_SPECIFIC_02)	n/a	n/a	0	
D3	SYSTEM_WATCHDOG_CONFIG (MFR_SPECIFIC_03)	n/a	n/a	0	
D4	SYSTEM_WATCHDOG_RESET (MFR_SPECIFIC_04)	n/a	n/a	0	
D5	MONITOR_CONFIG (MFR_SPECIFIC_05)	n/a	n/a	0	
D6	NUM_PAGES (MFR_SPECIFIC_06)	0	Device dependent	0	Read Only
D7	RUN_TIME_CLOCK (MFR_SPECIFIC_07)	n/a	n/a	0	
D8	RUN_TIME_CLOCK_TRIM (MFR_SPECIFIC_08)	n/a	n/a	0	
D9	ROM_MODE (MFR_SPECIFIC_09)	n/a	n/a	n/a	Write Only
DA	USER_RAM_00 (MFR_SPECIFIC_10)	0	255	0	
DB	SOFT_RESET (MFR_SPECIFIC_11)	n/a	n/a	n/a	Write Only
DC	RESET_COUNT (MFR_SPECIFIC_12)	0	65535	0	
DD	PIN_SELECTED_RAIL_STATES (MFR_SPECIFIC_13)	n/a	n/a	0	
DE	RESEQUENCE (MFR_SPECIFIC_14)	0	0xFFFF	n/a	Write Only
DF	CONSTANTS (MFR_SPECIFIC_15)	n/a	n/a	n/a	Read Only
E0	PWM_SELECT (MFR_SPECIFIC_16)	0	12	0	
E1	PWM_CONFIG (MFR_SPECIFIC_17)	n/a	n/a	0	
E2	PARM_INFO (MFR_SPECIFIC_18)	n/a	n/a	0	Index is checked to verify that it points to a valid base address
E3	PARM_VALUE (MFR_SPECIFIC_19)	n/a	n/a	0	
E4	TEMPERATURE_CAL_GAIN (MFR_SPECIFIC_20)	–1638	1638	0	
E5	TEMPERATURE_CAL_OFFSET (MFR_SPECIFIC_21)	–255.75	255.75	0	
E6	(MFR_SPECIFIC_22)				
E7	FAN_CONFIG_INDEX (MFR_SPECIFIC_23)	0	3	0	
E8	FAN_CONFIG (MFR_SPECIFIC_24)	n/a	n/a	0	
E9	FAULT_RESPONSES (MFR_SPECIFIC_25)	n/a	n/a	0	
EA	LOGGED_FAULTS (MFR_SPECIFIC_26)	n/a	n/a	n/a	Only valid write is all zeroes.
EB	LOGGED_FAULT_DETAIL_INDEX (MFR_SPECIFIC_27)	0	Device dependent	0	
EC	LOGGED_FAULT_DETAIL (MFR_SPECIFIC_28)	n/a	n/a	0	Read Only
ED	LOGGED_PAGE_PEAKS (MFR_SPECIFIC_29)	n/a	n/a	0	Only valid write is all zeroes.
EE	LOGGED_COMMON_PEAKS (MFR_SPECIFIC_30)	n/a	n/a	0	Only valid write is all zeroes.
EF	LOGGED_FAULT_DETAIL_ENABLES (MFR_SPECIFIC_31)	n/a	n/a	See comment	All logging is enabled by default
F0	EXECUTE_FLASH (MFR_SPECIFIC_32)	n/a	n/a	0	Write Only
F1	SECURITY (MFR_SPECIFIC_33)	n/a	n/a	See comment	Default password is 0xFFFFFFFFFFFF - security is disabled
F2	SECURITY_BIT_MASK (MFR_SPECIFIC_34)	n/a	n/a	n/a	Default bit mask is to have no commands secured.
F3	MFR_STATUS (MFR_SPECIFIC_35)	n/a	n/a	0	
F4	GPI_FAULT_RESPONSES (MFR_SPECIFIC_36)	n/a	n/a	0	
F5	MARGIN_CONFIG (MFR_SPECIFIC_37)	n/a	n/a	0	
F6	SEQ_CONFIG (MFR_SPECIFIC_38)	n/a	n/a	0	

Table 123. Range and Limits for PMBus Commands (continued)

Code (hex)	Command	Minimum	Maximum	Hardcoded Default	Comments
F7	GPO_CONFIG_INDEX (MFR_SPECIFIC_39)	0	12	0	
F8	GPO_CONFIG (MFR_SPECIFIC_40)	n/a	n/a	0	
F9	GPI_CONFIG (MFR_SPECIFIC_41)	n/a	n/a	0	
FA	GPIO_SELECT (MFR_SPECIFIC_42)	0	n/a	0	
FB	GPIO_CONFIG (MFR_SPECIFIC_43)	n/a	n/a	0	
FC	MISC_CONFIG (MFR_SPECIFIC_44)	n/a	n/a	0	
FD	DEVICE_ID (MFR_SPECIFIC_45)	n/a	n/a	Device dependent	
FE	Mfr_Specific_Extended_Command				Not Supported
FF	PMBUS_Extended_Command				Not Supported

12 Glossary

ACK: Acknowledge – Indicates that the PMBus has received the message correctly.

ADC: Analog-to-digital converter – Converts analog voltages to digital counts that may be used for monitoring or control.

DAC: Digital-to-analog converter

DFlash: Data Flash memory – Nonvolatile memory used for storing PMBus settings. The values in DFlash are automatically copied to RAM during wake up.

FPWM: Fast pulse width modulation pin. These pins are capable of a higher frequency than the other PWM pins.

GPI: General-purpose input

GPIO: General-purpose input/output

GPO: General-purpose output

NACK: Non-acknowledge – An error has occurred in the PMBus message transfer.

PFlash: Program Flash memory – Nonvolatile memory used for the UCD90xxx main firmware.

PMBus: Power Management Bus – An open-standard protocol that defines a means of communicating with power conversion devices using an I^2C physical interface.

PWM: Pulse width modulation or pulse width modulator

RAM: Random access memory – Volatile memory used to hold PMBus settings and internal variables. PMBus settings are lost after a reset unless they are stored to Data Flash.

ROM: Read-only memory – Nonvolatile memory used for the UCD90xxx boot algorithms and some common data tables.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from F Revision (May 2018) to G Revision	Page
• Changed table 66.	70

Changes from E Revision (October 2016) to F Revision **Page**

- Added paragraph to NOTE in *PWM Configuration* section 36
- Added NOTE to *(D7h) RUN_TIME_CLOCK (MFR_SPECIFIC_07)* section. 53
- Added content to the *(EAh) LOGGED_FAULTS (MFR_SPECIFIC_26)* section 69
- Updated Table 62: *LOGGED_FAULTS Command Format (UCD9090 and UCD9090A)* 69
- Updated Table 63: *LOGGED_FAULTS Command Format (UCD90160 and UCD90160A)* 69
- Deleted reference to UDC90910 device in Table 97: *SEQ_CONFIG Command Format (UCD90120 and UCD90124)* .. 88
- Deleted reference to UDC90910 device in Table 98: *SEQ_CONFIG Command Format (Devices Other Than the UCD90240, UCD90120, UCD90124, UCD90160A, and UCD9090A)* 88
- Added reference to UCD90160A, and UCD9090A devices in Table 98: *SEQ_CONFIG Command Format (Devices Other Than the UCD90240, UCD90120, UCD90124, UCD90160A, and UCD9090A)* 88

Changes from D Revision (September, 2016) to E Revision **Page**

- Added grey shading to the *UCD9012x and UCD90910* column and the *UCD9090* column of *Monitor ID* row *11* of Table 41. 52
- Updated Table 61 69

Changes from C Revision (January, 2016) to D Revision **Page**

- Added UCD9090A to the *PMBus Status Supported by the UCD90120A, UCD9090* caption. 7
- Added UCD90160A to the *PMBus Status Supported by the UCD90160* caption. 10
- Added *16-Bit Time Encoding* section. 14
- Updated entire *PMBus Commands* table. 17
- Added *(B9h) RAIL_STATE (USER_DATA_09)* section. 41
- Added content to the end of the second bullet in the *Re-Sequence* section. 68
- Changed sub-bullet content in list item number 5. 76
- Added *SEQ_CONFIG Command Format (UCD90160A and UCD9090A Only)* table. 88
- Added two-byte formatting for the UCD90160A and UCD9090A to the end of the *Sequencing On Timeout* section. 91
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