EVM User's Guide: LMKDB1112EVM

LMKDB1112 Evaluation Module

Description

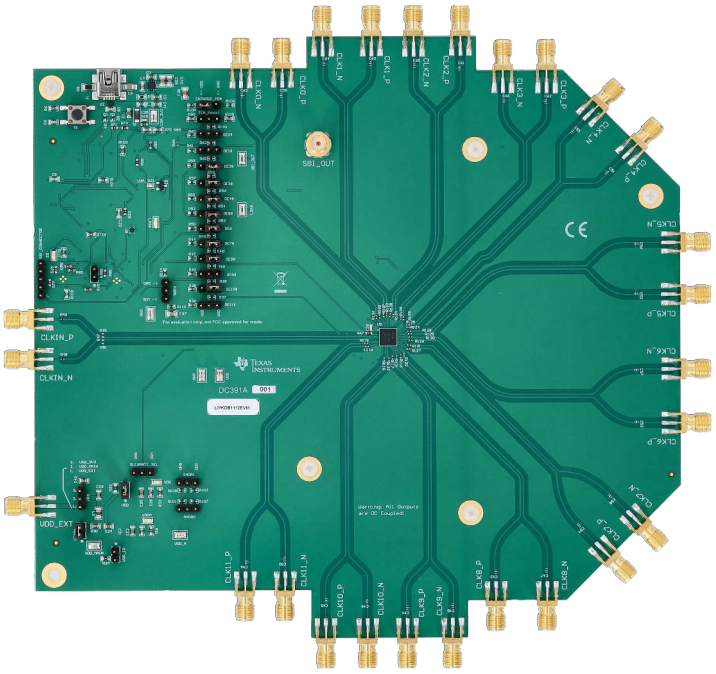
The LMKDB1112 Evaluation Module (EVM) is designed to provide a quick setup to evaluate the LMKDB1112 LP-HCSL buffer that supports PCIe Gen 1 to Gen 7 and is DB2000QL compliant. The printed circuit board (PCB) contains several jumpers and a USB connection to enable the LMKDB1112 with desired user programming and setup. The evaluation module provides flexibility for compliance testing, system prototyping, and performance evaluation of the LMKDB1112 device.

Features

- PCIe Gen 1 to Gen 7 and DB2000QL compliant buffer
- External and USB power supply options
- Programmablity through TICS Pro 2 Software GUI graphical user interface (GUI)
- Onboard input and output expander for output enable or disable through pin controls

Applications

- High performance computing
- Server motherboard
- NIC/SmartNIC
- Hardware accelerator



LMKDB1112 EVM Default Settings

1 Evaluation Module Overview

1.1 Introduction

The EVM can be configured through an on-board USB microcontroller (MCU) interface using a PC with TI's TICS Pro Software GUI. TICSPro can also be used to import and export register data for flexible programming of device. Input and outputs of LMKDB1112 can be interfaced with external system for evaluating compatibility and performance through a coaxial cable. On-board LDOs give users an option to use the USB as power supply to minimize the number of test equipment needed. Side Band Interface (SBI) header pins can be used to daisy chain or control the outputs of LMKDB1112 for fast switching.

1.2 Kit Contents

LMKDB1120EVM box contains:

- One LMKDB1112EVM board (DC391A).
- 3ft mini-USB cable (MPN 3021003-03).

1.3 Specification

Some key specifications for LMKDB1112 device and EVM are noted in Table 1-1.

Table 1-1. LMKDB1112 Key Parameters

Parameter	Value
Ambient temperature	-40ºC to 105ºC
Power supply	1.8V ± 10%, 3.3V ± 10%
Operating frequency	1MHz to 400MHz. (automatic output disable (AOD) disabled)
	25MHz to 400MHz. (automatic output disable (AOD) enabled)
Output format	LP-HCSL

1.4 Device Information

The LMKDB1112 is a high performance LP-HCSL buffer that supports PCIe Gen 1 to Gen 7 and is DB2000QL compliant. LMKDB1112 has extremely low additive jitter, fail safe inputs, flexible power-up sequence, individual output enable pins (OE#), loss of input signal detection (LOS), and 3-wire or 4-wire SBI and SMBus interface. The EVM has integrated LDOs for excellent power supply noise suppression with operating supply voltage of 3.3V.

2 EVM Quick Start

The default jumper configuration for the EVM to power the device from an onboard 3.3V LDO with USB supply option is shown in Table 2-1. Configure the EVM for initial bring up as specified in Table 2-1. The EVM can also be configured to external power supply by changing the position of jumper JP17 as described in Table 2-1.

Table 2-1. Default Jumper Configuration

Category	Reference Designator	Default Position	Description
Power	VDD_A	1-2	Connect USB or external supply to VDDA of device.
	VDD	1-2	Connect USB or external supply to output bank and digital supply of the chip (VDD).
	VDD_IO	1-2	Connect USB or external supply to IO pins on board (VDD_IO).
	JP3	1-2	Choose between USB power supply and external. Current configuration is for external supply. To change to USB power, change jumper position to 2-3.
Output Enable Control Pins	OE0#, OE#1, OE#2, OE#3, OE#4, OE#5, OE#6, OE#7, OE#8, OE#9, OE#10, OE11#	2-3	Pull down to GND to enable output (OE#0-11) with pin control option.
SMBus Address Control Pins	SADR0, SADR1	-	Refer to Table 3-6 or selecting SMBus address.
Digital Pins	TCA_Reset, CKPWRGD_PD#	1-2	TCA Reset and CLKPWRGD_PD# pulled high.
	SBEN	2-3	3-pin header. To enable SBI, change jumper position to 1-2 (connect to VDD).
	SBEN	-	SN74LVC125 buffer enable control pin (2-pin header). Default pull down to GND.

2.1 Hardware Setup

LMKDB1112 EVM Default Settings shows default jumper configuration for the EVM. Make sure to adjust the jumpers as shown for initial boot-up using USB power supply option.

To begin using the LMKDB1112EVM, follow the steps below.

1. Verify the EVM default jumper as described in Table 2-1 and LMKDB1112 EVM Default Settings.
2. Connect the USB cable to USB port at J1.
3. Connect 100MHz reference clock to CLKIN_P/N. Refer to Figure 3-1 for different input reference configurations.

A labeled image of the LMKDB1112EVM is shown in Figure 2-1.

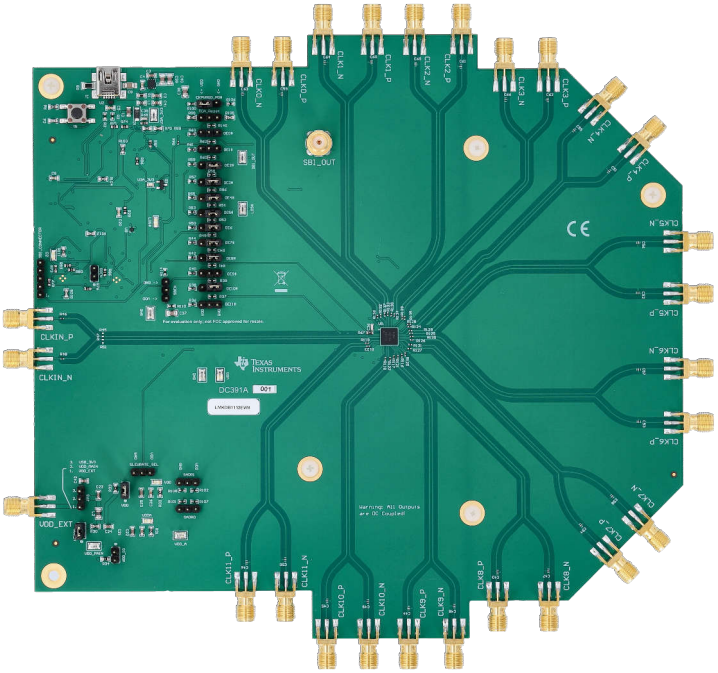


Figure 2-1. LMKDB1112EVM Labeled

2.2 Software Setup

2.2.1 TICS Pro GUI Setup

1. If not already installed, then install TICS Pro software from TI website: TICS Pro 2 Software GUI.
2. Start TICS Pro software.
3. Make sure the steps under Section 2.1 have been completed before performing this step. Select the LMKDB1112 profile from *Select Device* → *Clock Buffer* → *LMKDB1112*.
4. Confirm communication with the board as follows:
   a. Check to see that Connection mode is USB2ANY with green background (at bottom of TICS Pro 2 software)
   b. Click *Scan SMBus* in the top left hand corner of TICS Pro 2 Software. The device should be found at a specified address.
   c. Confirm following field the *Communication Setup* pop-up window:
      i. Make sure *USB2ANY* is selected as the interface.
      ii. In case of multiple USB2ANY, select desired interface. If a USB2ANY is currently in use in another TICS Pro, then the user must release that interface by changing the interface setting to *Demo Mode*.

2.2.2 Power Up Sequence

By default, the LMKDB1112 and the GUI are started with the default configuration. When using the on-board USB supply option, the following steps can be followed to avoid any improper power up sequence issues when plugging the USB cable to the EVM.

1. After all the steps above, toggle the *USB 3V3 Supply* pin *Low* → *High* for power reset.
2. Click on *Scan Bus* in the *Communication Setup* window to find and update device address.
3. Click on *Read All Regs* to update the register readback from the device.

2.3 EVM Measurements

Measurements can now be made on the clock outputs using an oscilloscope or a phase noise analyzer.

3 Hardware

3.1 Device Operation Modes

The LMKDB1112 can be configured to start up in one of two modes during power-on/reset (POR). SBEN enable pin determines the mode of operation during power supply ramp up. Below are both of the modes for the device:

1. **SMBus Mode Only** (EVM default): When SBEN pin is set to low during power up, SBI interface is disabled and output enable (OE) control is only accessible through the SMBus and OE control pins.
2. **SBI Mode and SMBus Mode**: When SBEN pin is set to high during power up, SBI interface is enabled and the outputs can be controlled through SBI interface, as well as SMBus and OE control pins. OE pin control is not possible for pins J4, A10, and K10 since these pins are being used for SBI communications.

3.2 EVM Configuration

The LMKDB1112EVM can be configured for multiple modes using on board MCU and can be powered via USB or external power supply. The following sections describes power, logic, clock input, and output interfaces on the EVM and how to configure the EVM accordingly.

Some of the key components and the reference designator are noted in Table 3-1.

Table 3-1. Key Components Reference Designator and Descriptions

Item No.	Reference Designators	Description
1	U1A	LMKDB1112
2A	VDD_EXT	External VDD option through a SMA Port.
2B	JP3	Jumper header to select between external or onboard 3.3V USB supply option.
3	CLKIN_P, CLKIN_N	SMA ports for clock input
4	CLK0_P, CLK0_N, ..., CLKx_P, CLKx_N, ..., CLK11_P, CLK11_N	SMA ports for clock outputs (CLKXX_P, CLKXX_N).
5	SADR0, SADR1	SADR0_tri and SADR1_tri jumper header option to select different address as defined in Table 3-6.
6	SBEN	3-pin SBEN pin header jumper to enable or disable SBI interface during power-up.
7	TCA_Reset	TCA_RESET pin header jumper for Input / Output (IO) Expander. TCA_RESET pin header jumper needs to be connected to pull-up for proper operation. Default configuration is set to pull-up.
8	CKPWRGD_PD#	CLKPWRGD_PD# pin header jumper to enable or disable the LMKDB1120.
11A	SBI_CONNECTOR	SBI Connector header jumper for daisy chain option.
11B	SBEN	2-pin SBI_PRIMARY header jumper option to disable the U3A, U3B, U3C, U3D buffer part on the EVM.
12	U9	USB power option LDO.
13	U8A, U8B, U8C, U8D	Hi-Z buffer part used on SBI lines for daisy chain configuration.
14	U6	MUX part to choose between MCU and IO expander option on OE#5, OE#6, and OE#10 pins.
15	U7	IO Expander used for all OE# pin controls.
16	U4	MSP430F5529IPN MCU.

3.2.1 Power Supply

The LMKDB1112 has VDDA and VDD supply pins that operate from 1.8V ± 10% and 3.3V ± 10%. The EVM has two different method of supplying power to the device as listed in Table 3-2.

For 3.3V supply option, the EVM has an on-board LDO which is selected by default to reduce the need for external power supply and operate the EVM using a USB cable with a PC.

To use 1.8V ± 10% supply on the EVM, J4 can be used to force external supply voltage.

Table 3-2. EVM Power Modes

EVM Power Mode	Designator	Position	Supply Voltage	Description
External	VDD_EXT	External Supply	1.8V ± 10%, 3.3V ± 10%	External supply option is selected.
	JP3	1-2		
USB (default)	VDD_EXT	Not Connected	3.3V ± 10%	USB 3.3V supply option is selected.
	JP3	2-3		

3.2.2 Logic Input and Outputs

The logic input and output pins on LMKDB1112 provides different options to select device functional modes, output enable and disable control, loss of signal (LOS) detection, and different device address selection. The following section describes the function of different input and output logic pins. Voltage levels for input pins can be set through TICSPro GUI or using on-board jumper as specified in Table 3-1.

Table 3-3. Device Start-Up Modes

SBEN_EN Input Level	Start-up Mode
Low (default)	SBI inactive
High	SBI active

Table 3-4. Output Enable Pin Control

OE0# to OE11# INPUT LEVEL	OUTPUT STATUS
Low (default)	Active
High	Inactive

Table 3-5. Loss of Signal Detection (LOS)

LOSb OUTPUT LEVEL (Status pin)	LOS STATUS
Low	Detected
High	Not detected

Table 3-6. SMBus Address Decode

Address Selection		Binary Value								Hex Value	
SADR1_tri	**SADR0_tri**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**Rd/Wrt**	Without **Rd/Wrt**	With **Rd/Wrt**
0	0	1	1	0	1	1	0	0	0	6C	D8
	M	1	1	0	1	1	0	1	0	6D	DA
	1	1	1	0	1	1	1	1	0	6F	DE
M	0	1	1	0	0	0	0	1	0	61	C2
	M	1	1	0	0	0	1	0	0	62	C4
	1	1	1	0	0	0	1	1	0	63	C6
1	0	1	1	0	0	1	0	1	0	65	CA
	M	1	1	0	0	1	1	0	0	66	CC
	1	1	1	0	0	1	1	1	0	67	CE

Note

SMBus address for the device is Bits[7:1]. Often Rd/Wrt bit is included in the hex value depending on the different vendors. *With **Rd/Wrt*** column shows hex value when Rd/Wrt value is considered 0, while *Without **Rd/Wrt*** is the SMBus address.

3.2.3 Clock Input

LMKDB1112 can support different input interfaces depending on the input swing and common mode voltage. There are four input interfaces type that can be configured on LMKDB1112 using external components and internal termination schemes as shown in Figure 3-1. If using signal generator, then make sure to populate *R47* with a *100Ω* resistor or use internal or external 50Ω termination to ground.

1. DC Coupled HCSL/LP HCSL Input.
2. DC Coupled LVDS Input.
3. External AC Coupled Input.
4. Internal 50Ω to ground terminations.

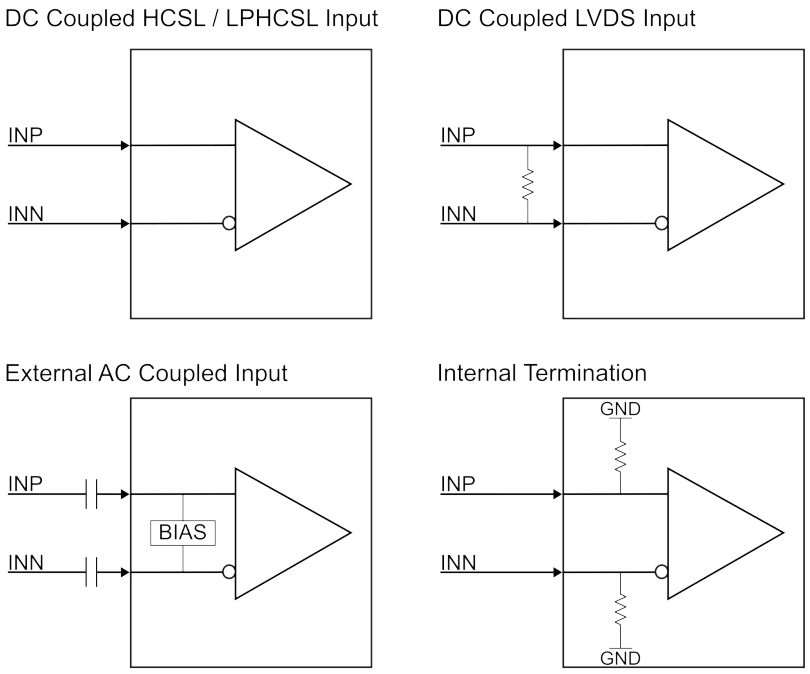


Figure 3-1. Input Interfaces

How to setup all different interfaces supported by LMKDB1112 is outlined in Table 3-7.

Table 3-7. Input Interfaces

Input Interface	Configuration
DC coupled HCSL or LP-HCSL	This is default EVM and device configuration. *R46* and *R48* values are ***0Ω*** and *Input Interface Type* on *Input* page is selected to *DC Coupled*.
DC coupled LVDS input	Populate *R47* with a ***100Ω*** resistor and set *Input Interface Type* on *Input* page to *DC Coupled*.
External AC coupled input	Replace *R46* and *R48* with ***0.1uF*** capacitor and set *Input Interface Type* on *Input* page to *AC Coupled*.
Internal termination	To enable internal 50Ω to ground terminations, set the *Input Termination* on *Input* page to *Enabled*.

3.2.4 Clock Outputs

LMKDB1112 has 12 differential clock outputs (CLK[11:0]_P/N).

All the outputs are DC coupled with a capacitive load of 2pF, and all outputs have SMA ports soldered on board.

WARNING

DC-coupled clocks must not be directly connect to RF equipment, which cannot accept DC voltages greater than 0V, such as spectrum analyzers and phase noise analyzers.

3.2.5 Status Outputs, LEDs, and Test Points

LMKDB1112EVM has a status output signal from LMKDB1112, LEDs and test points to monitor signal voltage and supply voltage on the board. All the status signals and test points on the board are summarized in Table 3-8.

Table 3-8. Status Output, LEDs and Test Points

Function or Test Signal	Status Pin / LED Designator	Description
LOSb	LOS#	Test point to monitor LOSb status.
	LOS#	LED status light for LOSb detection.
SBI OUT	SBI_OUT	SMA Port for SBI OUT pin.
	SBI_OUT	Additional test point for SBI OUT pin.
	SBI_CONNECTOR	Jumper header for SBI OUT, SBI_IN, SBI_DATA, and SHFT_LD# pins to connect all signals needed for daisy chain in one place.
VDDA	VDD_A	LED status light for VDDA supply pin.
	VDD_A	Test point for VDDA supply pins.
VDD	VDD	LED status light for VDD supply pins.
	VDD	Test point for VDD supply pins.
VDD_MAIN	VDD_MAIN	Test point to measure the VDD supply selected from USB option or external option through JP3.
GND	GND, GND	Test points for GND reference on the board.
USB LED	D2	USB LED status light to verify USB2ANY communication to board.
U2A_3V3	U2A_3V3	USB2ANY LDO supply status LED.
	U2A_3V3	Test point for USB2ANY LDO supply pin.

4 Software

4.1 TICS Pro 2 LMKDB1112 Software

LMKDB1112 TICS Pro 2GUI provides full functionality to interact with the device through SMBus, SBI, and OE pin option to interact with the device. TI recommends to use GUI interface while evaluating LMKDB1112EVM to fully utilize all the functionalities of the EVM. The GUI interface consists of *User Controls* and *Raw Register* page to write directly into each register bit or field values. The GUI interface also has *Input*, *Device Info*, and *Output* pages, which can be used to evaluate functions available on the device. The following sections describe the details of each page.

4.1.1 Input

Input page provides access to configure different input modes and read back live status for loss of signal (LOSb) as shown in Figure 4-1.

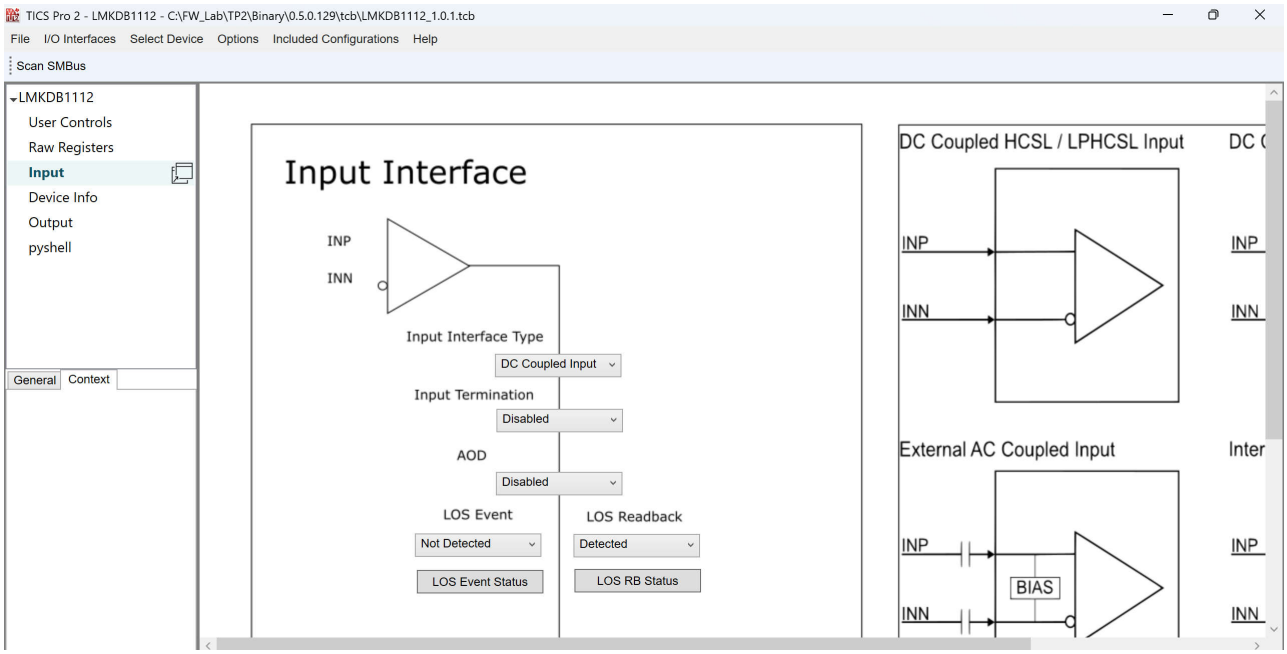


Figure 4-1. Input Interface

4.1.1.1 Input Interface Type

Input interface type can be configured as AC Coupled or DC coupled. AC coupled option provides internal bias to the clock inputs connected.

4.1.1.2 Input Termination

Internal 50Ω to ground terminations can be enabled or disabled using the *Input Termination* drop-down menu.

4.1.1.3 Automatic Output Disable (AOD)

Automatic output disable (AOD) can be enabled or disabled using this control. AOD is enabled by default on LMKDB1112. AOD disables the outputs when low when there is a loss of signal (LOS) detected on the input. When AOD is disabled, outputs follow the input clock in DC state.

4.1.1.4 LOS Event

LOS Event Status gives information when there is loss of signal (LOS) event. Make sure to clear the LOS event by writing 1 or selecting *Detected* from the *LOS Event* drop-down menu.

4.1.1.5 LOS Readback

LOS Readback provides live status of loss of signal detection.

4.1.2 Device Info and EVM Setup

The *Device Info* page contains three different sections and LMKDB1112EVM information.

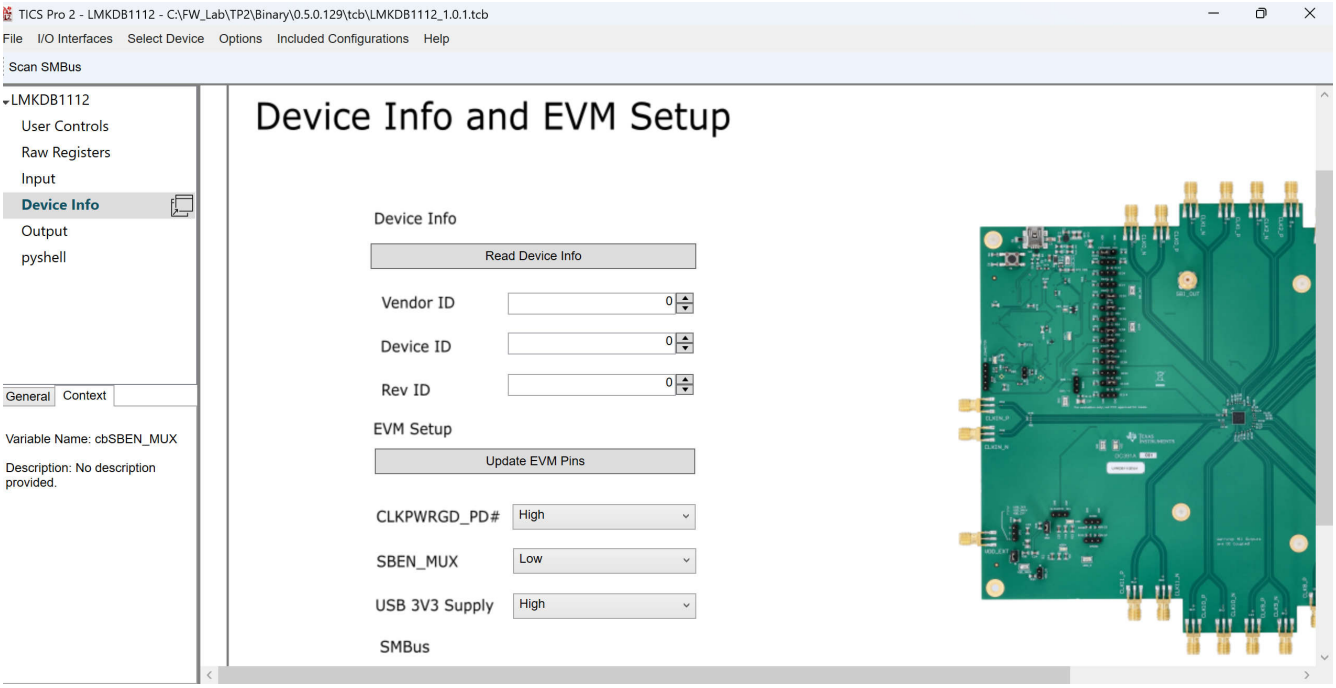


Figure 4-2. Device Info

4.1.2.1 Device Info

This section contains following information related to device which can be read back using *Read Device Info* button.

1. Vendor ID
2. Device ID
3. Rev ID

4.1.2.2 EVM Setup

EVM setup has key pins to configure device. Table 4-1 and Table 4-2 outline usage of each pin option.

Table 4-1. CLKPWRGD_PD#

Pin Level	Function
Low	LMKDB1112 power down mode.
High	LMKDB1112 normal operation mode (default).
Hi-Z	When Hi-Z is selected, on-board header jumper CKPWRGD_PD# can be used to force external voltages on the pin.

Table 4-2. SBEN_MUX

Pin Level	Function
Low	SBEN MUX (U6) configured to OE option for pin OE4#, OE7# and OE10# through IO expander (default).
High	SBEN MUX (U6) switches to USB2ANY MCU for SBI_IN, SBI_DATA, and SHFT_LD#. SBI becomes available after power reset in this setting on the device. Output page have *Enable SBI Control* button to configure all the setting automatically.
Hi-Z	When Hi-Z is selected, on-board header jumper can be used to force external voltages on the pin.

4.1.2.3 SMBus

Byte counter value determines the number of register readback during block read operation.

4.1.3 Output

The output page in TICS Pro 2has controls for clock outputs through SMBus, OE pins, and SBI.

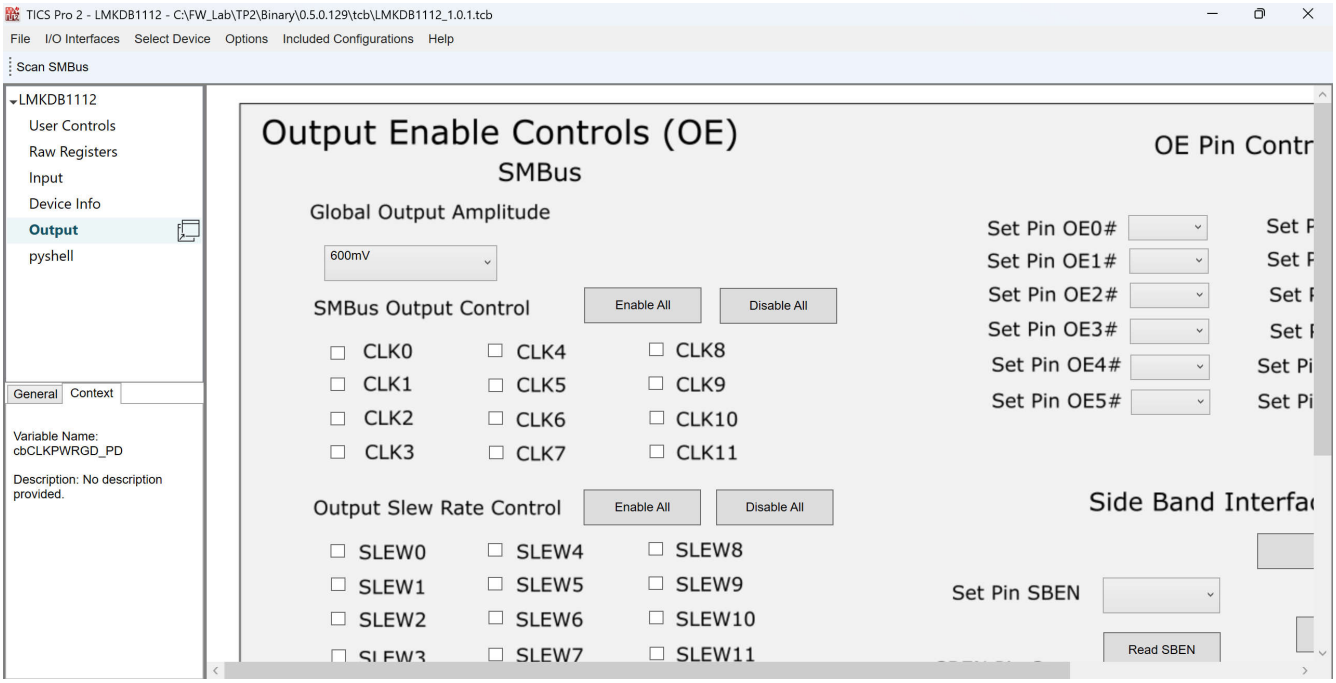


Figure 4-3. Output

4.1.3.1 SMBus

SMBus can be used to control the following parameters on the outputs:

1. Global Output Amplitude: To program output VOD (single-ended swing) from 600mV to 975mV with a step size of 25mV.
2. SMBus Output Control: To enable or disable CLK0 to CLK11 through register bits.
3. Output Slew Rate Control: To program slew rate values for a specifc output.
4. SBI Mask Register: To enable or disable SBI mask bits. When a mask bit is enabled, an output is controlled through SMBus and SBI control doesn't have any affect on the output. This is used when critical outputs needs to stay on.
5. OE# Pin Readback: To read status of OE# pins.

4.1.3.1.1 Programmable Output Slew Rate Control

The LMKDB1112 has 16 different slew rates options that can be assigned to the outputs. 0x0 is the fastest slew rate setting and 0xF is the slowest slew rate setting. To set the slew rate of each output, follow these steps:

1. There are four different registers, SLEWRATE_OPT#, that can store up to four different slew rates. Select your desired slew rates by assigning a value from 0x0 (fastest) to 0xF (slowest) to each SLEWRATE_OPT# register. The default values set to each SLEWRATE_OPT# register can be found in Table 4-3.
   a. For example, if you wanted the fastest, second fastest, and the slowest slew rate, assign 0x0, 0x1, and 0xF to registers SLEWRATE_OPT#. SLEWRATE_OPT1 = 0x0 (fastest), SLEWRATE_OPT2 = 0x1 (second fastest), and SLEWRATE_OPT3 = 0xF (slowest). SLEWRATE_OPT4 does not have to be assigned, but if you want more than one register set to a slew rate, then SLEWRATE_OPT4 can be assigned to any of the three previous settings. For this example, SLEWRATE_OPT4 = 0xF (slowest) as shown in Figure 4-4.

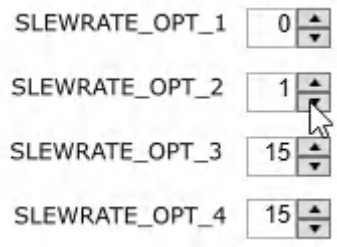


Figure 4-4. SLEWRATE_OPT# Assignment Example in TICS Pro 2

Table 4-3. Default SLEWRATE_OPT_# Values

Register Field Name	Default Value	Default Slew Rate
SLEWRATE_OPT_1	0x0	Fastest
SLEWRATE_OPT_2	0x6	Fast
SLEWRATE_OPT_3	0xA	Slow
SLEWRATE_OPT_4	0xF	Slowest

2. Set a slew rate for each output by using the drop-down menus under the *Output Slew Rate Control* Section. The default SLEWRATE_OPT# register assignment for all outputs is SLEWRATE_OPT2, which has a default slew rate of 0x6.
   a. Following the example from step 1a, if you wanted CLK0, CLK1, CLK2, and CLK3 to have the fastest slew rate, CLK4 and CLK7 to have the slowest slew rate, and CLK 5 and CLK6 to have the second fastest slew rate, set the drop-down menus of CLK0, CLK1, CLK2, and CLK3 to OPT_1, CLK4 and CLK7 to OPT_3 or OPT_4, and CLK5 and CLK6 to OPT_2 as shown in Figure 4-5. Repeat this step to set the slew rate of the other 12 outputs.

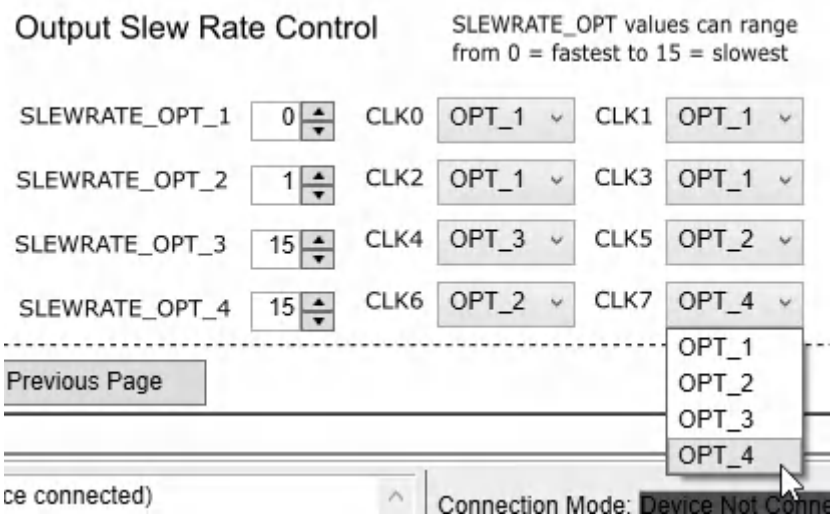


Figure 4-5. Setting Output Slew Rate Example in TICS Pro 2

4.1.3.2 OE Pin Control

LMKDB1112EVM has on-board IO expander to provide output enable and disable controls for OE# pins. Low and high voltage levels can be set on all the pins using GUI without needing on-board headers. If on-board headers are used, then set all the OE# pins to Hi-Z using the *All Hi-Z* button under the OE Pin Control on output page.

4.1.3.3 Side Band Interface (SBI)

Side band interface can be evaluated using controls available on the output page. There are two methods that can be used to enable SBI on the LMKDB1112.

1. Automated: When using on-board USB power supply option on the EVM, clicking once on the *Enable SBI Control* button configures the LMKDB1112 into SBI mode.
2. Manual: This method requires to set the *Set Pin SBEN* to *High* followed with a power cycle on the board. This is needed when using external supply option or when not using the *Enable SBI Control* button. SBI is enabled on LMKDB1112 after the restart.

After using any of the method above, press *Read SBEN* to verify status of SBI mode on the device. Use check boxes for CLK0 to CLK11 to enable (checked) or disable (unchecked) the desired outputs. Once selected, click on *SBI Latch Enable* to load data into shift register.

5 Implementation Results

5.1 Typical Phase Noise Characteristic

The typical phase noise performance for 156.25MHz reference clock input using a SMA100B is shown in Figure 5-1.

LMKDB1112EVM was configured in cascaded mode to get these measurements:

1. SMA100B → LMKDB1112EVM input. Then, LMKDB1112EVM to secondary LMKDB1112 EVM. This was done to get good slew rate at the input. Other methods like a clipping circuit can be used to get a desired slew rate and square wave form from the SMA100B.
2. Outputs phase noise is measured through a Balun to convert the differential waveform from the LMKDB1112 into a single-ended waveform for a phase noise analyzer.

   As shown below in Figure 5-1, reference input jitter is 36.7 fs. The measured jitter on the output of LMKDB1112 is 43.7 fs is shown in Figure 5-2. Calculated typical additive jitter is about 24 fs for the LMKDB1112.

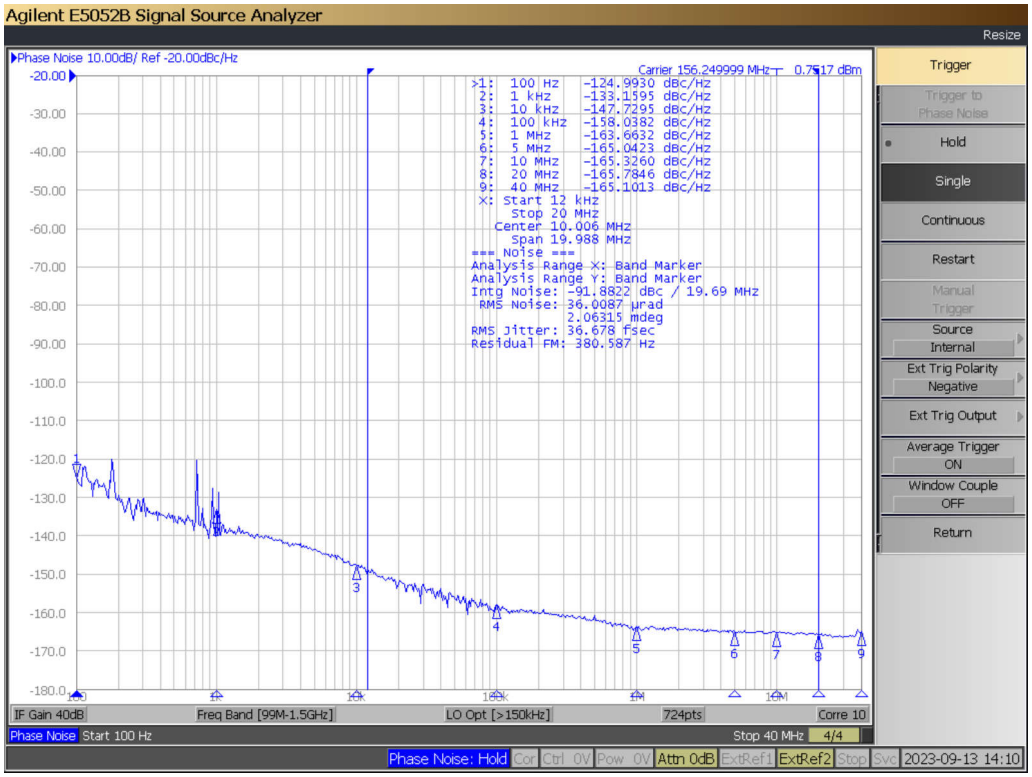


Figure 5-1. Reference Clock Input Phase Noise

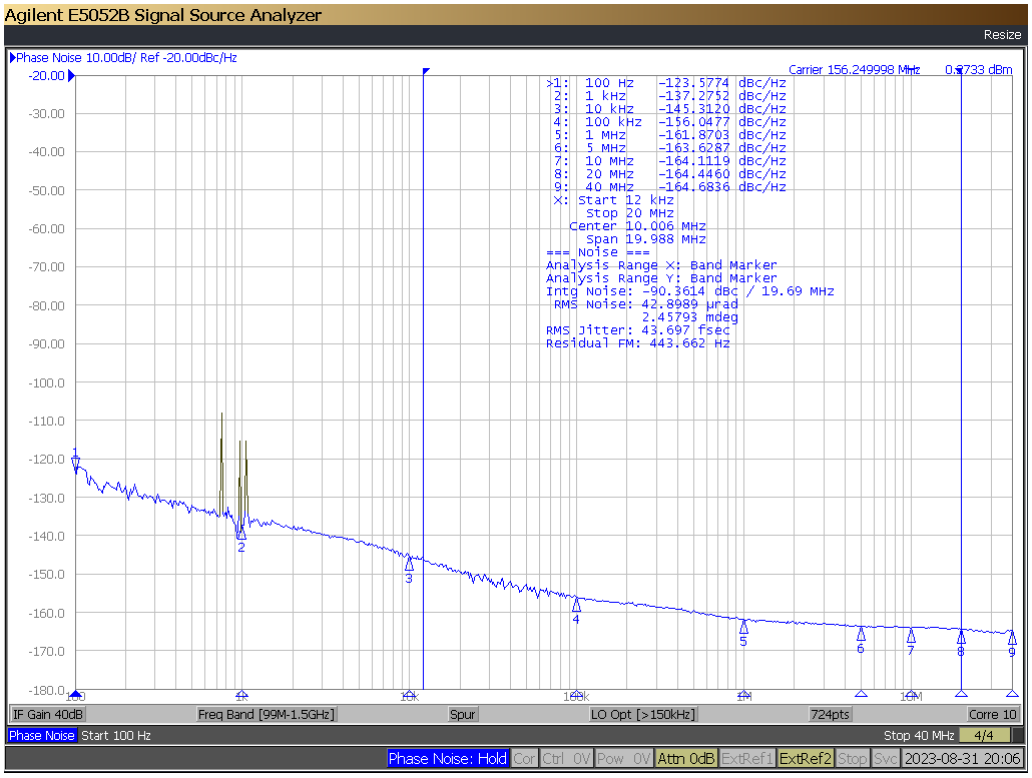


Figure 5-2. LMKDB1112 Output Clock Phase Noise

6 Hardware Design Files

6.1 Schematics

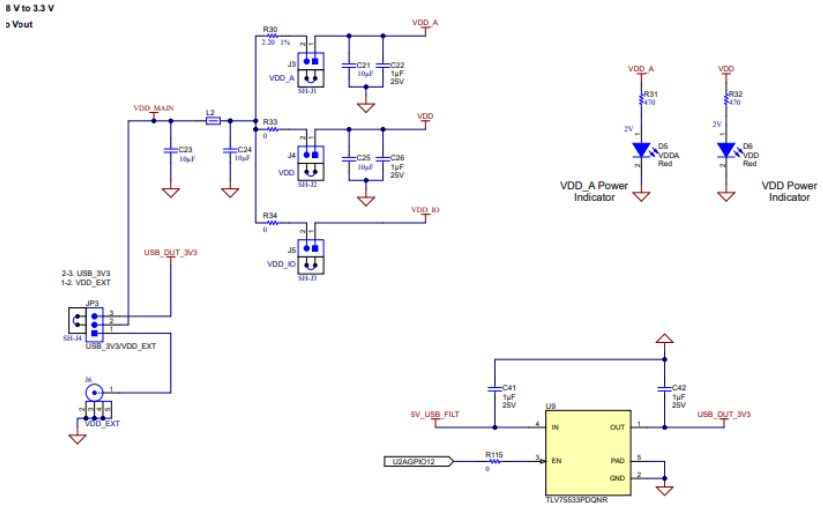


Figure 6-1. Power Supply (External and USB option)

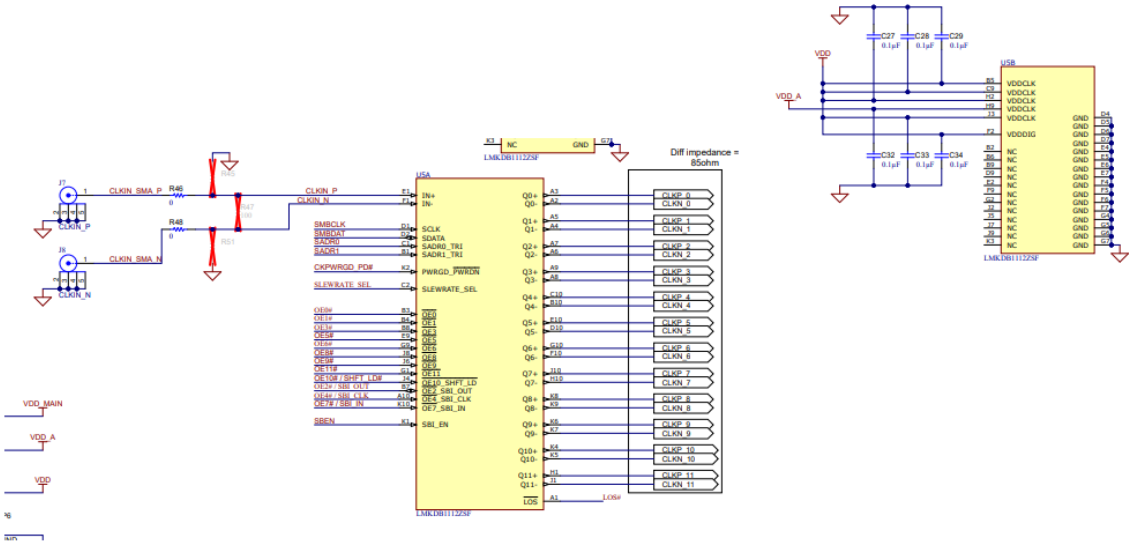


Figure 6-2. LMKDB1112 Device and CLKIN_P/N Reference

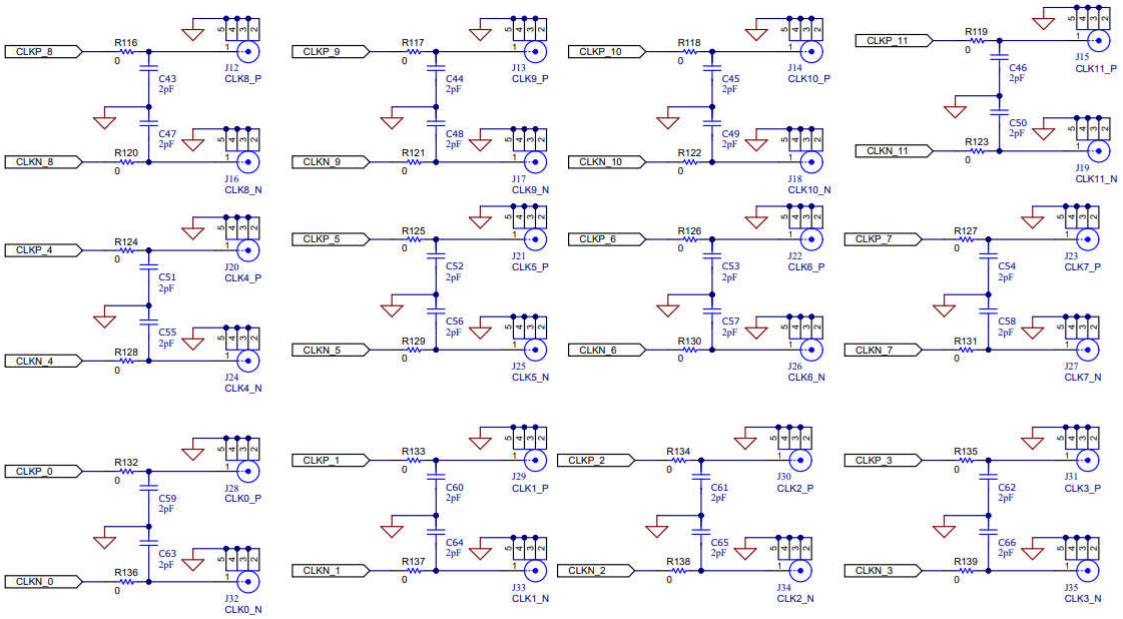


Figure 6-3. Clock Outputs CLK0 to CLK11

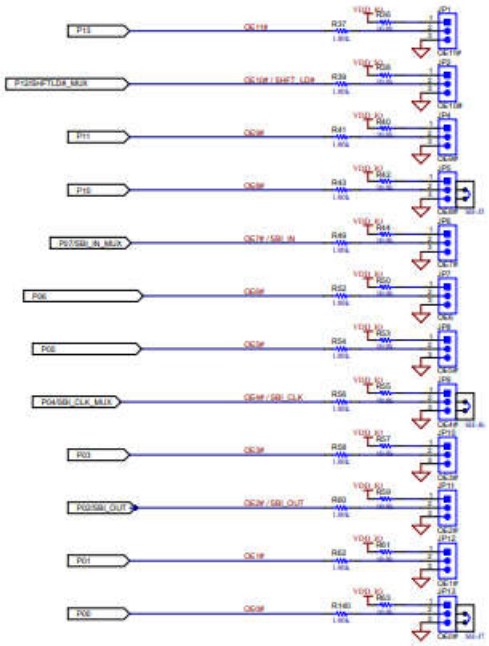


Figure 6-4. Output Enable Pins (OE#)

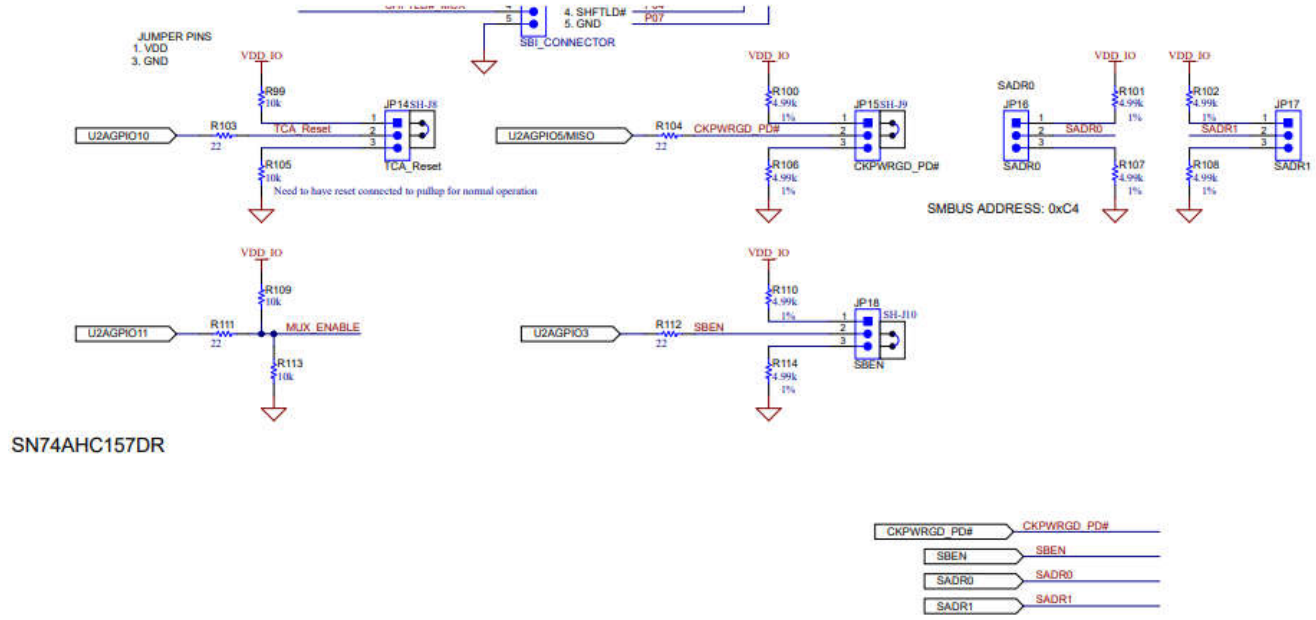


Figure 6-5. Logic I/O Jumpers

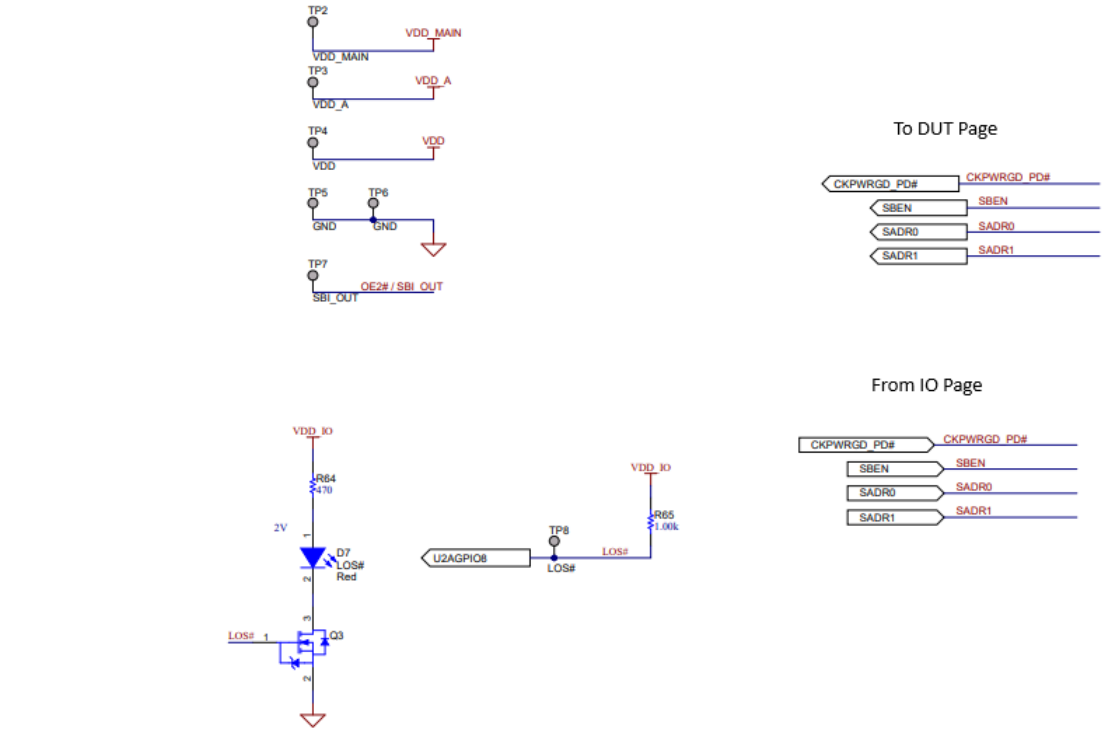


Figure 6-6. Status LEDs and Test Points

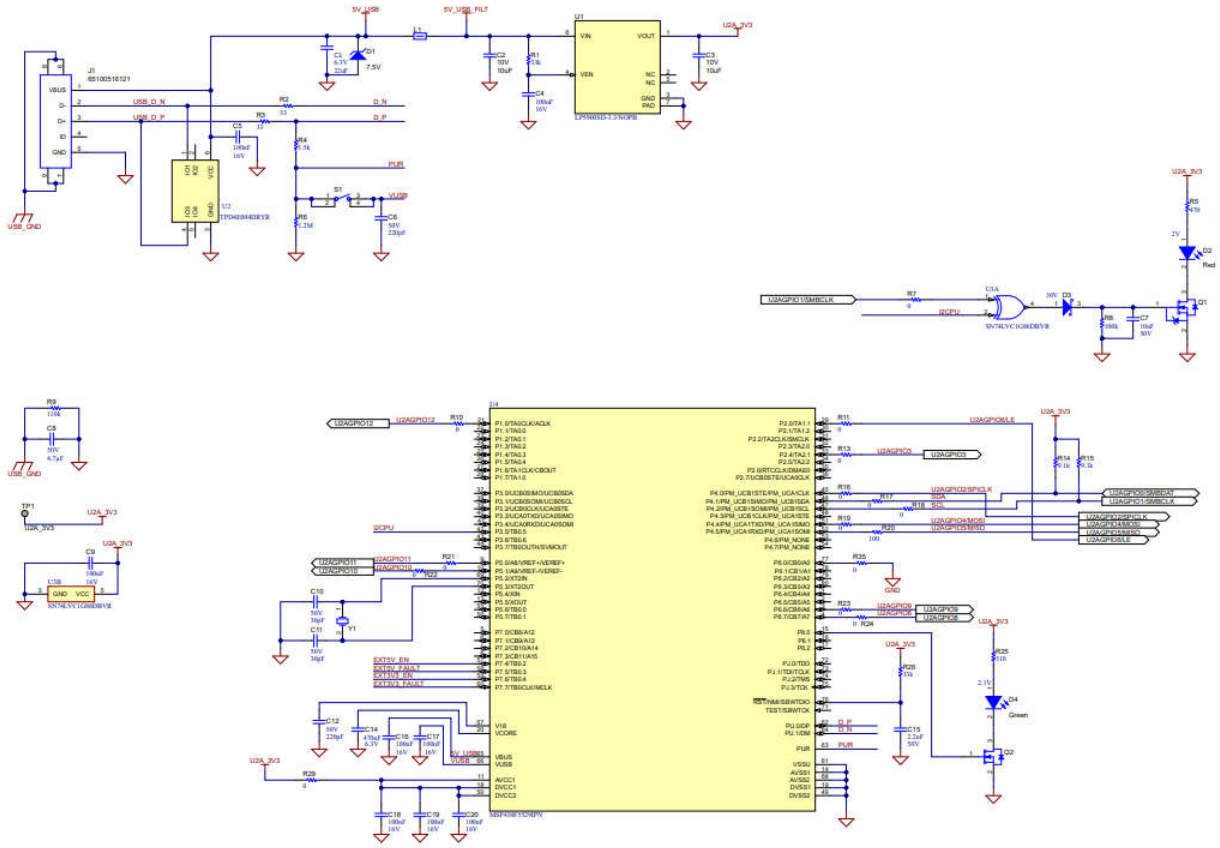


Figure 6-7. USB Schematic

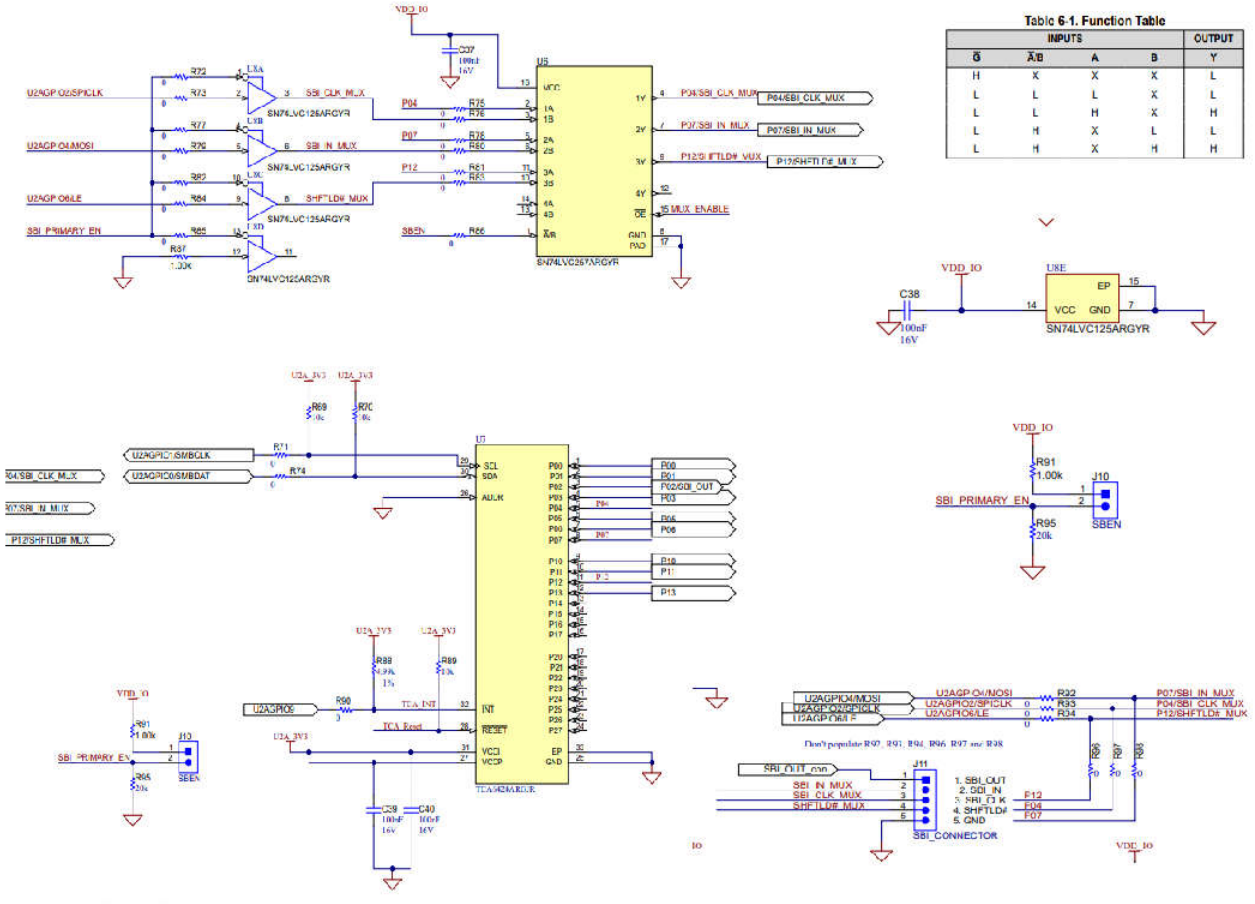


Figure 6-8. I/O Expander, MUX and Buffer used for SBI and OE pin Control

6.2 PCB Layouts

Layer Stackup :

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.80mil	3.5	
1	Top Layer	Copper	2.80mil		
	Dielectric 1	FR-4 High Tg	6.00mil	4.2	
2	GND 1	Copper	1.40mil		
	Dielectric 2	FR-4 High Tg	10.00mil	4.2	
3	Signal 1	Copper	1.40mil		
	Dielectric 3	FR-4 High Tg	17.20mil	4.2	
4	PWR	Copper	1.40mil		
	Dielectric 4	FR-4 High Tg	10.00mil	4.2	
5	GND 2	Copper	1.40mil		
	Dielectric 5	FR-4 High Tg	6.00mil	4.2	
6	Bottom Layer	Copper	2.80mil		
	Bottom Solder	Solder Resist	0.80mil	3.5	
	Bottom Overlay				

Figure 6-9. Layer Stackup

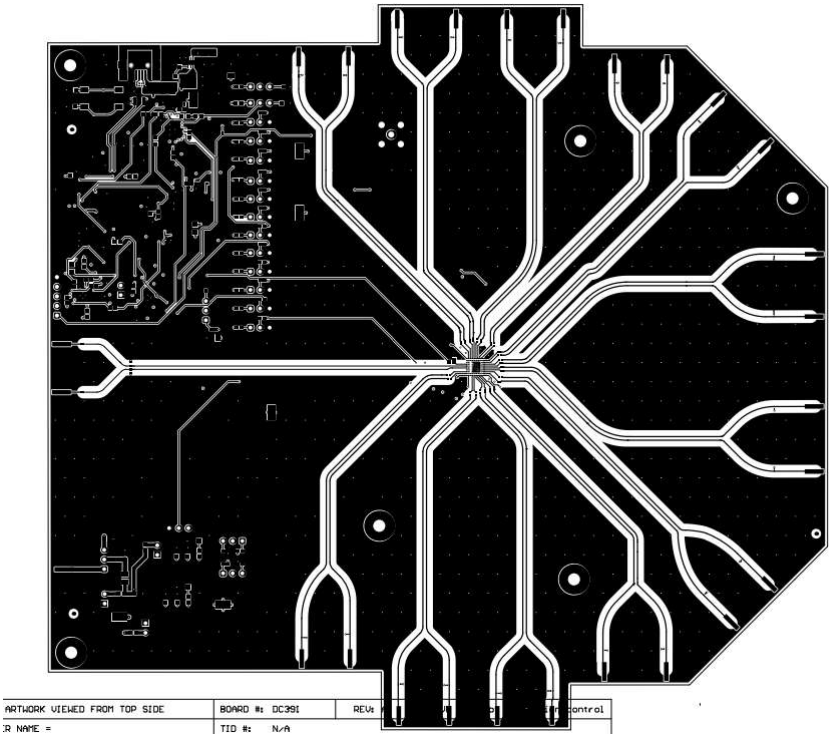


Figure 6-10. Top Layer (CLKIN / CLKOUT Signals)

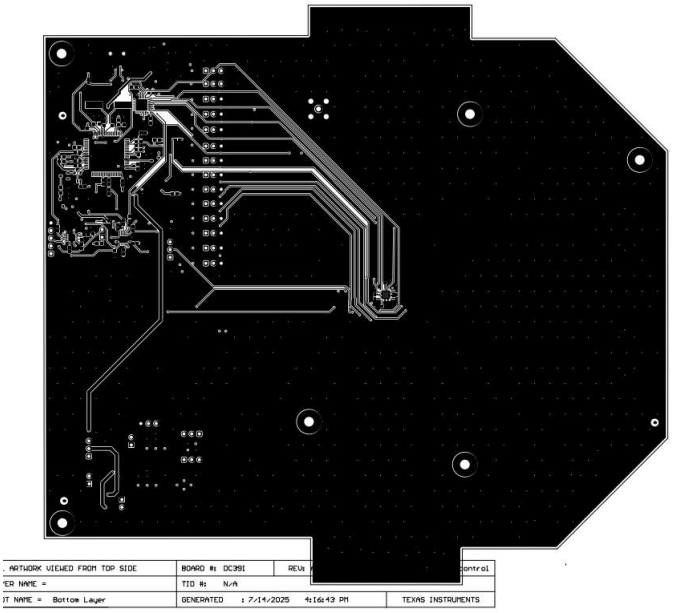


Figure 6-11. Bottom Layer

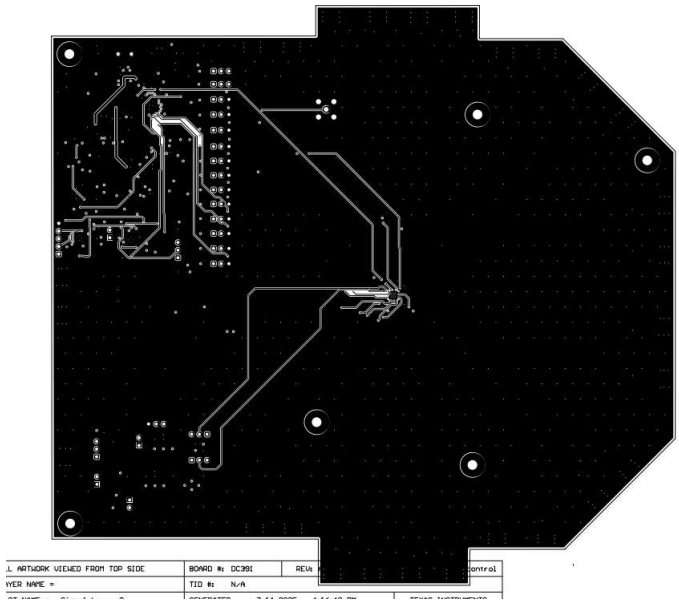


Figure 6-12. Signal 1 Layer

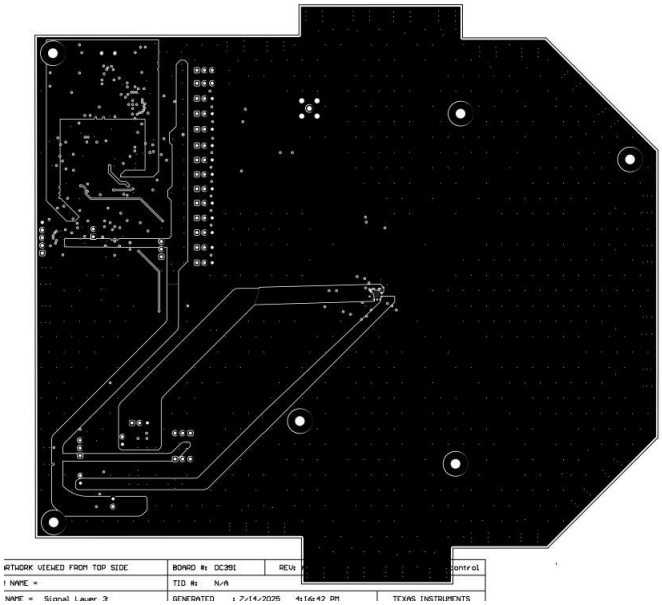


Figure 6-13. PWR Layer

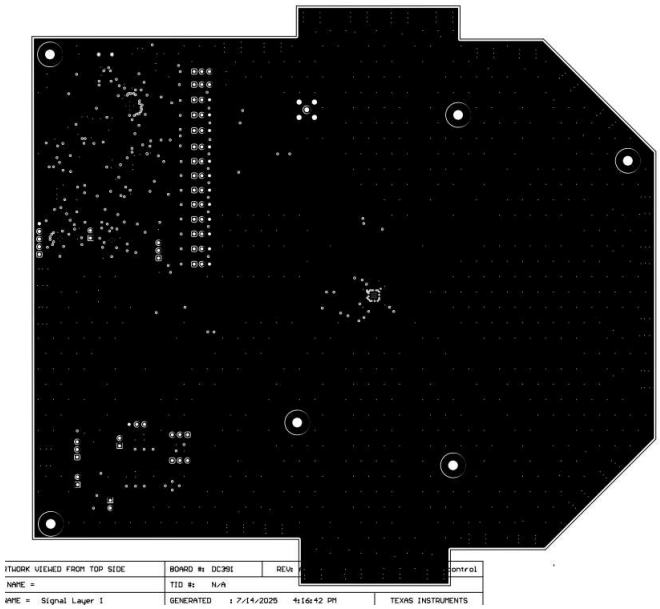


Figure 6-14. GND 1 Layer

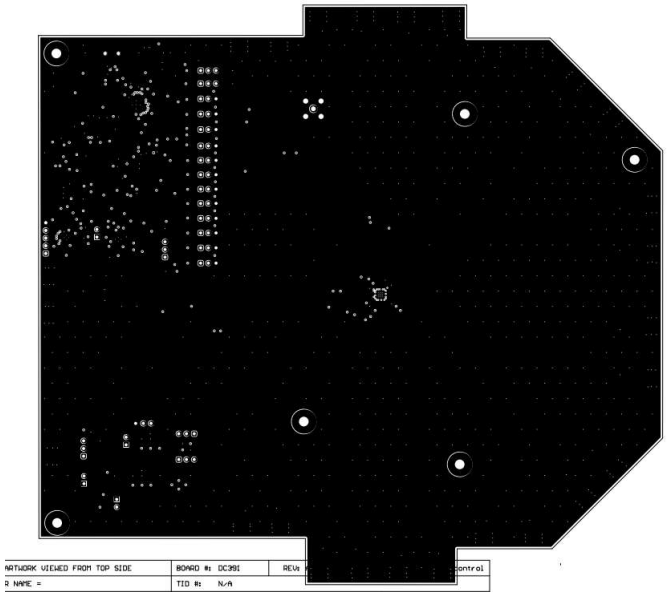


Figure 6-15. GND 2 Layer

6.3 Bill of Materials (BOM)

Table 6-1. Bill of Materials (BOM)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C1	1	22µF	Multilayer Ceramic Capacitor 22uF 6.3V X6S 20% SMD 0805 T/R	0805	JMK212BC6226MG-T	Taiyo Yuden
C2, C3	2	10uF	CAP, CERM, 10 uF, 10 V, +/- 20%, X6S, 0603	0603	GRM188C81A106MA73D	MuRata
C4, C5, C9, C16, C17, C18, C19, C20	8	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 5%, X7R, 0603	0603	C0603C104J4RACTU	Kemet
C6, C12	2	220pF	CAP, CERM, 220 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H221JA01D	MuRata
C7	1	0.01uF	CAP, CERM, 0.01 uF, 50 V, +/- 5%, X7R, 0603	0603	C0603C103J5RACTU	Kemet
C8	1	4.7uF	CAP, CERM, 4.7 µF, 50 V,+/- 10%, X7R, 1206	1206	C3216X7R1H475K160AE	TDK
C10, C11	2	30pF	CAP, CERM, 30 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H300JA01D	MuRata
C14	1	0.47uF	CAP, CERM, 0.47 µF, 6.3 V,+/- 10%, X7R, 0603	0603	0603B474K6R3CT	Walsin
C15	1	2200pF	CAP, CERM, 2200 pF, 50 V, +/- 10%, X7R, 0603	0603	C0603C222K5RACTU	Kemet
C21, C23, C24, C25	4	10uF	CAP, CERM, 10 µF, 16 V,+/- 20%, X6S, 0603	0603	GRM188C81C106MA73D	MuRata
C22, C26, C41, C42	4	1uF	CAP, CERM, 1 µF, 25 V,+/- 20%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E1X7R1E105M080AC	TDK
C27, C28, C29, C32, C33, C34	6	0.1uF	CAP, CERM, 0.1 µF, 16 V,+/- 10%, X7R, 0402	0402	EMK105B7104KV-F	Taiyo Yuden
C35, C36	2	33pF	CAP, CERM, 33 pF, 100 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C2A330JA01D	MuRata
C37, C38, C39, C40	4	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0805	0805	C0805C104K4RACTU	Kemet

Table 6-1. Bill of Materials (BOM) (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66	24	2pF	Ceramic Capacitor 2pF ±0.1pF 25V C0G 0201 (0603 Metric)	0201	GJM0335C1E2R0BB01D	Murata
D1	1	7.5V	Diode, Zener, 7.5 V, 500 mW, SOD-123	SOD-123	MMSZ4693T1G	ON Semiconductor
D2, D5, D6, D7	4	Red	LED, Red, SMD	Red 0805 LED	LTST-C170KRKT	Lite-On
D3	1	30V	Diode, Schottky, 30 V, 0.2 A, SOT-23	SOT-23	BAT54-7-F	Diodes Inc.
D4	1	Green	LED, Green, SMD	1.6x0.8x0.8mm	LTST-C190GKT	Lite-On
FID1, FID2, FID3, FID4, FID5, FID6	6		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H2, H3, H4, H9, H10	6		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8, H11, H12	6		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1	1		Connector, Receptacle, USB Mini B 2.0, SMT	Connector, Receptacle, USB Mini B 2.0, 5 Position, SMT	65100516121	Wurth Elektronik
J3, J4, J5, J10	4		Header, 100mil, 2x1, Gold, TH	Header, 2x1, 100mil	5-146261-1	TE Connectivity
J6, J7, J8, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32, J33, J34, J35	27		CONN SMA JACK STR EDGE MNT	CONN_JACK	CON-SMA-EDGE-S	RF Solutions Ltd.
J9	1		Connector, SMA, TH	SMA	142-0701-231	Cinch Connectivity

Table 6-1. Bill of Materials (BOM) (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
J11	1		Header, 2.54mm, 5x1, Gold, TH	Header, 2.54mm, 5x1, TH	61300511121	Wurth Elektronik
JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP8, JP9, JP10, JP11, JP12, JP13, JP14, JP15, JP16, JP17, JP18, JP19	19		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
L1	1	60 ohm	Ferrite Bead, 60 ohm @ 100 MHz, 3.5 A, 0603	0603	MPZ1608S600ATAH0	TDK
L2	1	330 ohm	Ferrite Bead, 330 ohm @ 100 MHz, 2 A, 0805	0805	742792037	Wurth Elektronik
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
Q1, Q3	2	25V	MOSFET, N-CH, 25 V, 0.22 A, SOT-23	SOT-23	FDV301N	Fairchild Semiconductor
Q2	1	50V	MOSFET, N-CH, 50 V, 0.22 A, SOT-23	SOT-23	BSS138	Fairchild Semiconductor
R1, R26	2	33k	RES, 33 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060333K0JNEA	Vishay-Dale
R2, R3	2	33	RES, 33, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040233R0JNED	Vishay-Dale
R4	1	1.5k	RES, 1.5 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K50JNED	Vishay-Dale
R5, R31, R32, R64	4	470	RES, 470, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603470RJNEA	Vishay-Dale
R6	1	1.2Meg	RES, 1.2 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031M20JNEA	Vishay-Dale

Table 6-1. Bill of Materials (BOM) (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R7, R10, R11, R13, R16, R17, R18, R19, R21, R22, R23, R24, R29, R67, R68, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R90, R92, R93, R94, R96, R97, R98	38	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R8	1	100k	RES, 100 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100KJNEA	Vishay-Dale
R9	1	110k	RES, 110 k, 1%, 0.25 W, 1206	1206	RC1206FR-07110KL	Yageo America
R14, R15	2	9.1k	RES, 9.1 k, 5%, 0.1 W, 0603	0603	RC0603JR-079K1L	Yageo
R20	1	100	RES, 100, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100RJNEA	Vishay-Dale
R25	1	510	RES, 510, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603510RJNEA	Vishay-Dale
R30	1	2.2	RES, 2.20, 1%, 0.1 W, 0603	0603	ERJ-3RQF2R2V	Panasonic
R33, R34	2	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEY0R00V	Panasonic
R35	1	0	RES, 0, 5%, 0.03 W, 01005	01005	RC0402J000CS	Samsung
R36, R38, R40, R42, R44, R50, R53, R55, R57, R59, R61, R63	12	10.0k	RES, 10.0 k, 0.5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040210K0DHEDP	Vishay-Dale
R37, R39, R41, R43, R49, R52, R54, R56, R58, R60, R62, R140	12	1.00k	RES, 1.00 k, 1%, 0.063 W, 0402	0402	MCR01MZPF1001	Rohm

Table 6-1. Bill of Materials (BOM) (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R46, R48, R66, R115, R116, R117, R118, R119, R120, R121, R122, R123, R124, R125, R126, R127, R128, R129, R130, R131, R132, R133, R134, R135, R136, R137, R138, R139	28	0	RES, 0, 5%, .05 W, AEC-Q200 Grade 0, 0201	0201	ERJ-1GN0R00C	Panasonic
R65	1	1.00k	RES, 1.00 k, 1%, 0.1 W, 0402	0402	ERJ-2RKF1001X	Panasonic
R69, R70, R89, R95, R99, R105, R109, R113	8	10k	RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310K0JNEA	Vishay-Dale
R87, R91	2	1.00k	RES, 1.00 k, 0.5%, 0.1 W, 0603	0603	RT0603DRE071KL	Yageo America
R88, R100, R101, R102, R106, R107, R108, R110, R114	9	4.99k	RES, 4.99 k, 1%, 0.063 W, 0402	0402	RC0402FR-074K99L	Yageo America
R103, R104, R111, R112	4	22	RES, 22, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060322R0JNEA	Vishay-Dale
S1	1		Switch, Tactile, SPST-NO, 0.05A, 12V, SMT	SW, SPST 6x6 mm	FSM4JSMA	TE Connectivity
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11	11	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	8		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone
U1	1		150-mA Ultra-Low Noise LDO for RF and Analog Circuits Requires No Bypass Capacitor, NGF0006A (WSON-6)	NGF0006A	LP5900SD-3.3/NOPB	Texas Instruments

Table 6-1. Bill of Materials (BOM) (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
U2	1		4-Channel ESD Protection Array for High-Speed Data Interfaces, DRY0006A (USON-6)	DRY0006A	TPD4E004DRYR	Texas Instruments
U3	1		Single 2-Input Exclusive-OR Gate, DBV0005A (SOT-23-5)	DBV0005A	SN74LVC1G86DBVR	Texas Instruments
U4	1		25 MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 degC, 80-pin QFP (PN), Green (RoHS & no Sb/Br)	PN0080A	MSP430F5529IPN	Texas Instruments
U5	1		LMKDB1112ZSF	LGA80	LMKDB1112ZSF	Texas Instruments
U6	1		Quadruple 2-Line To 1-Line Data Selector/Multiplexer With 3-State Outputs, RGY0016A (VQFN-16)	RGY0016A	SN74LVC257ARGYR	Texas Instruments
U7	1		Low-Voltage 24-Bit I2C and SMBus I/O Expander, 24 Outputs, 1.65 to 5.5 V, -40 to 85 degC, 32-pin UQFN (RGJ), Green (RoHS & no Sb/Br)	RGJ0032A	TCA6424ARGJR	Texas Instruments
U8	1		Quadruple Bus Buffer Gate With 3-State Outputs, RGY0014A, LARGE T&R	RGY0014A	SN74LVC125ARGYR	Texas Instruments
U9	1		500-mA, Low IQ, Small Size, Low Dropout Regulator, DQN0004A (X2SON-4)	DQN0004A	TLV75533PDQNR	Texas Instruments
Y1	1		Crystal, 24.000 MHz, 20pF, SMD	Crystal, 11.4x4.3x3.8mm	ECS-240-20-5PX-TR	ECS Inc.
R45, R51	0	49.9	RES, 49.9, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	RMCF0402FT49R9	Stackpole Electronics Inc
R47	0	100	RES, 100, 1%, 0.1 W, 0402	0402	ERJ-2RKF1000X	Panasonic

7 Compliance Information

7.1 Compliance and Certifications

Refer to *LMKDB1112EVM EU Declaration of Conformity (DoC)*.

8 References

For additional information on LMKDB1112, refer to *LMKDB1120/1108/1104/1102/1204/1202 PCIe Gen 1 to Gen 6 Ultra Low Jitter 1:20, 1:8, 1:4, 1:2, 2:4, 2:2 LP-HCSL Clock Buffer and Clock MUX*

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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