Application Note

Clocking Selection Guide for FPD-Link III and FPD-Link IV SerDes

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ABSTRACT

This document summarizes the REFCLK requirements for FPD-Link SerDes devices and the test methodology for measuring AC parameters of the clock signal. The document also describes the measurement setup for both frequency-domain and time-domain jitter measurements. Lastly, there is a selection guide for the corresponding TI clocking device for every FPD-Link device in the FPD-Link III and FPD-Link IV product families that requires an external REFCLK.

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Trademarks

1 Introduction

FPD-Link devices require an external clock signal for certain configurations and system applications. The jitter performance of the reference clock is typically stringent since this can contribute noise to the serializer's PLL input and can impact the horizontal eye margin of the data link. To optimize link quality, make sure the reference clock meets jitter requirements based on the system needs. This document summarizes time-domain and frequency-domain jitter requirements for all FPD-Link devices that require an external clock reference and provide a selection guide of TI's automotive grade clocking designs. TI's BAW technology is used in the CDC6C-Q1 low-power LVCMOS oscillator, as well as the LMK3H0102-Q1 and LMK1C0105-Q1 clock generators.

Note that throughout this document, *REFCLK* can be used as a term for *external oscillator*. These terms are sometimes used interchangeably across different FPD-Link device data sheets.

2 FPD-Link REFCLK Requirements and Jitter Definitions

FPD-Link REFCLK jitter requirements are generally specified in either the time-domain or frequency-domain. Frequency-domain jitter measurements are taken with a phase noise analyzer (PNA), such as the Keysight E5052. To calculate RMS phase jitter, the measured phase noise curve is integrated over a defined frequency band (usually 12kHz to 20MHz) and normalized based on the carrier frequency.

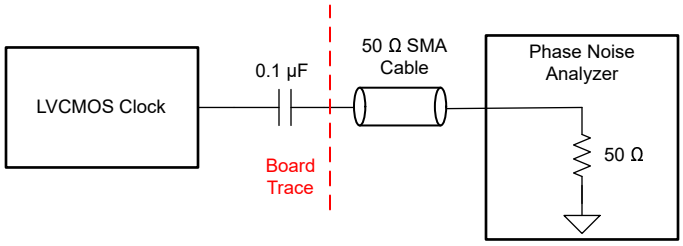

Figure 2-1. Frequency-Domain Jitter Measurement Setup With PNA

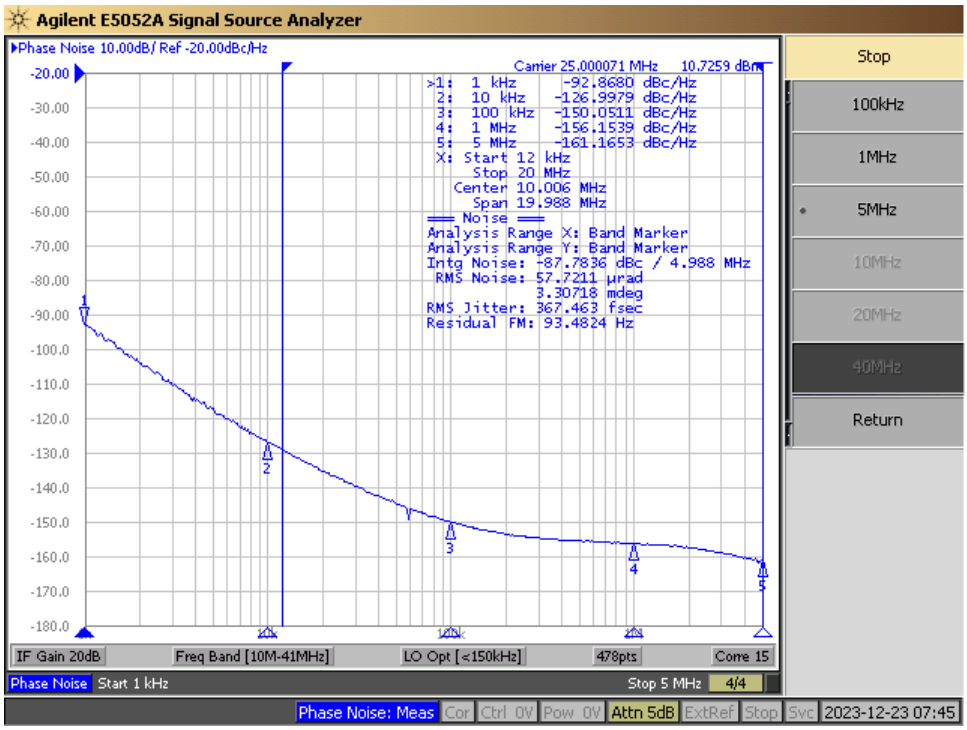

Figure 2-2. Phase Noise Measurement Example

Time-domain jitter measurements are taken with a jitter analysis software suite on a high-speed oscilloscope. TI commonly uses the DPOJET jitter and eye analysis tool provided on Tektronix oscilloscopes for such measurements. In this case, TI recommends measuring the total jitter (TJ) at a given bit error rate (BER) with

the clock recovery settings designed to match the input PLL characteristic of the serializer device. The following sections provide more details on how to configure the jitter analysis tool.

To open DPOJET, launch *One Touch Jitter* or *Serial Data/Jitter Wizard* from the utilities menu. Launching the tool can automatically set the acquisition settings and vertical and horizontal scaling based on the active input signal. A new window is also opened with various configuration options and measurement results. To configure FPD-Link REFCLK time-domain jitter measurements, enter the *Select* tab and add a measurement for *TJ@BER* with a BER setting of 10^{-10}. The clock recovery filters can be set in the *Configure* tab and needs to be set based on the FPD-Link device as described in Section 2.1.

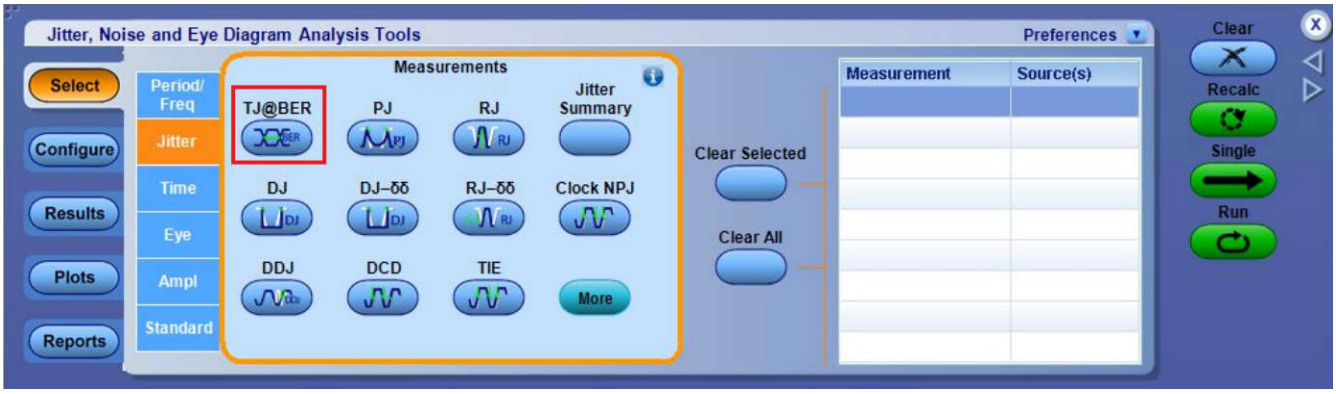

Figure 2-3. DPOJET Jitter Measurement Configuration

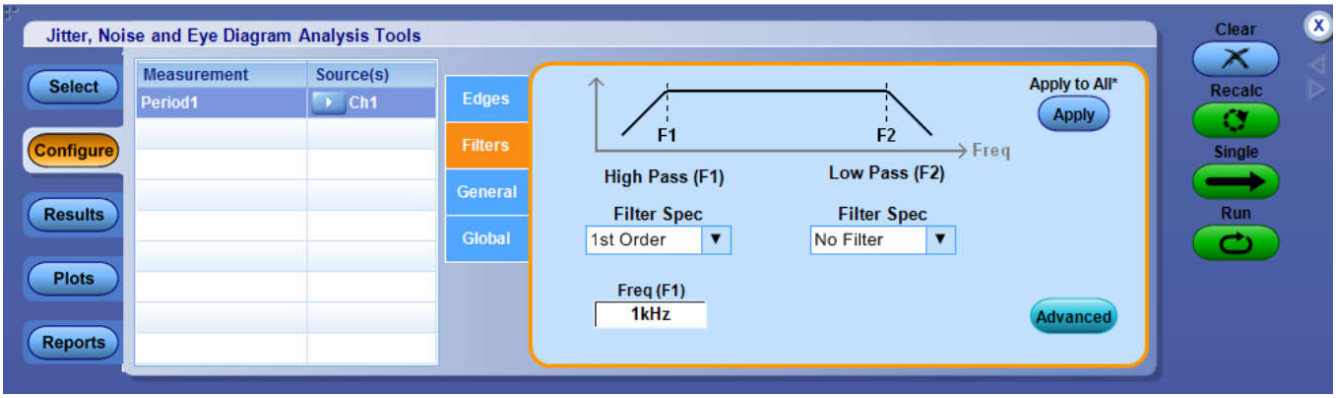

Figure 2-4. DPOJET Clock Recovery Filter Configuration

2.1 FPD-Link III REFCLK Requirements

FPD-Link III devices require different REFCLK frequencies based on the imager or camera pixel clock (PCLK) frequency used in the system. Similarly, the time-domain jitter specification depends on the PCLK frequency, UI, and various link configuration settings. The summary below lists the time-domain and frequency-domain jitter limits and UI definitions for all FPD-Link III devices which require an external REFCLK. All devices can support a standard 1.8V LVCMOS clock input with ±50ppm frequency accuracy. For time-domain jitter measurements, a custom second order PLL model needs to be configured in the jitter analysis software tool. The following loop bandwidth, low pass filter, and BER settings are used for time-domain jitter analysis for all FPD-Link III devices:

$$\text{LPF} = \frac{f_{OSC}}{20} \quad (1)$$

$$\text{CDR PLL LBW} = \frac{f_{OSC}}{15} \quad (2)$$

$$\text{BER} = 10^{-10} \quad (3)$$

DS90UB933-Q1 and DS90UB633A-Q1 UI Definition and Time-Domain Jitter Limit

$$10-\text{bit Mode: UI} = \frac{1}{\frac{f_{PCLK}}{2} \times 28} \quad (4)$$

$$12-\text{bit Mode: UI} = \frac{1}{f_{PCLK} \times \frac{2}{3} \times 28} \quad (5)$$

$$\text{Jitter limit} = 0.45 \times \text{UI} \quad (6)$$

DS90UB913A-Q1 and DS90UB913Q-Q1 UI Definition and Time-Domain Jitter Limit

$$10-\text{bit Mode: UI} = \frac{1}{\frac{f_{PCLK}}{2} \times 28} \quad (7)$$

$$12-\text{bit HF Mode: UI} = \frac{1}{f_{PCLK} \times \frac{2}{3} \times 28} \quad (8)$$

$$12-\text{bit LF Mode: UI} = \frac{1}{f_{PCLK} \times 28} \quad (9)$$

$$\text{Jitter limit} = 0.1 \times \text{UI} \quad (10)$$

DS90UB935-Q1 DS90UB953-Q1, DS90UB953A-Q1, and DS90UB635-Q1 UI Definition and Time-Domain Jitter Limit

$$\text{UI} = \frac{1}{f_{OSC}} \quad (11)$$

$$\text{Jitter limit} = 0.05 \times \text{UI} \quad (12)$$

DS90UB954-Q1, DS90UB936-Q1, DS90UB958-Q1, and DS90UB638-Q1 Frequency-Domain Jitter Limit

Phase noise integration range: 200kHz - 10MHz

Jitter limit = 50ps peak-peak

DS90UB960-Q1, DS90UB962-Q1, and DS90UB662-Q1 Frequency-Domain Jitter Limit

Phase noise integration range: 200kHz - 10MHz

Jitter limit = 50ps peak-peak

DS90Ux941AS-Q1 UI Definition and Time-Domain Jitter Limit

$$\text{Single}-\text{link Mode: UI} = \frac{1}{f_{PCLK} \times 35} \quad (13)$$

$$\text{Dual}-\text{link Mode: UI} = \frac{1}{\frac{f_{PCLK}}{2} \times 35} \quad (14)$$

$$\text{Jitter limit} = 0.028 \times \text{UI} \quad (15)$$

2.2 FPD-Link IV REFCLK Requirements

All FPD-Link IV devices share the same 1.5ps RMS (12kHz - 20MHz integration range) maximum frequency-domain jitter limit. The REFCLK input is generally 25MHz for camera (ADAS) SerDes and 27MHz for display (IVI) SerDes.

3 FPD-Link Clocking Selection Guide

Table 3-1 and Table 3-2 summarize typical configurations and REFCLK jitter requirements for all FPD-Link III and FPD-Link IV devices that require an external oscillator. CDC6C-Q1, LMK3H0102-Q1, and LMK3C0105-Q1 jitter measurements are provided for typical REFCLK frequencies and jitter test conditions. LMK3H0102-Q1 and LMK3C0105-Q1 measurements include worst-case crosstalk with common frequency combinations (ex: 25MHz, 27MHz, and 100MHz) to represent more realistic system use cases. Time-domain measurements only include typical values. RMS phase jitter measurements in Table 3-2 also include maximum specifications across PVT based on device characterization.

If only one output frequency is needed, the CDC6C-Q1 oscillator is generally recommended. This is offered in the industry smallest package size and has minimal power consumption. If multiple output frequencies are required, a clock generator such as LMK3H0102-Q1 or LMK3C0105-Q1 can often be the simplest system design.

Table 3-1. FPD-Link III Typical REFCLK Configuration and Jitter Measurements with TI Clocking Devices

FPD-Link device	TI Clocking Designs	Typical Configuration	Typical REFCLK Jitter Requirement	LMK3H0102/ LMK3C0105 Jitter Measurement	CDC6C Jitter Measurement
DS90UB933-Q1 DS90UB633A-Q1	CDC6CE025000XXXXX-Q1 LMK3H0102-Q1 LMK3C-Q1	REFCLK = 25MHz, PCLK = 50MHz, 12 bit mode	643ps	8.4ps	8.5ps
DS90UB913A-Q1 DS90UB913Q-Q1	CDC6CE048000XXXXX-Q1 LMK3H0102-Q1 LMK3C-Q1	REFCLK = 48MHz, PCLK = 72MHz, 12-bit LF mode	50ps	5.51ps	6.7ps
DS90UB935-Q1 DS90UB953-Q1 DS90UB953A-Q1 DS90UB635-Q1	CDC6CE050000XXXXX-Q1 LMK3H0102-Q1 LMK3C-Q1	REFCLK = 50MHz, PCLK = 50MHz	1000ps	4.20ps	6.8ps
DS90UB954-Q1 DS90UB936-Q1 DS90UB958-Q1 DS90UB638-Q1	CDC6CE025000XXXXX-Q1 LMK3H0102-Q1 LMK3C-Q1	REFCLK = 25MHz, PCLK = 25MHz	50ps p-p (200kHz-10MHz Integration Band)	4.498ps p-p	3.3ps p-p
DS90UB960-Q1 DS90UB962-Q1 DS90UB662-Q1	CDC6CE025000XXXXX-Q1 LMK3H0102-Q1 LMK3C-Q1	REFCLK = 25MHz, PCLK = 25MHz	50ps peak-peak (200kHz-10MHz integration band)	4.498ps p-p	3.3ps p-p
DS90Ux941AS-Q1	CDC6CE025000XXXXX-Q1 LMK3H0102-Q1 LMK3C-Q1	REFCLK = 25MHz, PCLK = 25MHz, Dual-link mode	32ps	8.4ps	8.5ps

Table 3-2. FPD-Link IV Typical REFCLK Configuration and Jitter Measurements with TI Clocking Devices

FPD-Link Device	TI Clocking Designs	REFCLK Frequency	REFCLK Phase Jitter Requirement (12kHz - 20MHz)	LMK3H0102/ LMK3C0105 Jitter Measurement	CDC6C Jitter Measurement
DS90UB964-Q1	CDC6CE025000XXXXX-Q1 LMK3H0102-Q1 LMK3C-Q1	25MHz	1.5ps RMS	310fs RMS (typical)	750fs RMS (typical) 1ps RMS (max)
DS90UB971-Q1	CDC6CE025000XXXXX-Q1 LMK3H0102-Q1 LMK3C-Q1	25MHz	1.5ps RMS	310fs RMS (typical)	750fs RMS (typical) 1ps RMS (max)
DS90UB9702-Q1 DS90UB9722-Q1 DS90UB9724-Q1	CDC6CE025000XXXXX-Q1 LMK3H0102-Q1 LMK3C-Q1	25MHz	1.5ps RMS	310fs RMS (typical)	750fs RMS (typical) 1ps RMS (max)
DS90Ux981-Q1	CDC6CE027000XXXXX-Q1 LMK3H0102-Q1 LMK3C-Q1	27MHz	1.5ps RMS	340fs RMS (typical)	550 fs RMS (typical)
DS90Ux983-Q1 DS90Ux943A-Q1	CDC6CE027000XXXXX-Q1 LMK3H0102-Q1 LMK3C-Q1	27MHz	1.5ps RMS	340fs RMS (typical)	550 fs RMS (typical)
DS90Ux984-Q1 DS90Ux944A-Q1	CDC6CE027000XXXXX-Q1 LMK3H0102-Q1 LMK3C-Q1	27MHz	1.5ps RMS	340fs RMS (typical)	550 fs RMS (typical)
DS90Ux988-Q1 DS90Ux688-Q1	CDC6CE027000XXXXX-Q1 LMK3H0102-Q1 LMK3C-Q1	27MHz	1.5ps RMS	340fs RMS (typical)	550 fs RMS (typical)

4 EMI Considerations

For automotive qualification, many systems using FPD-Link devices must comply with CISPR-25 radiated emission specifications. Although the FPD-Link SerDes link generally dominates the overall radiated emissions, the REFCLK signal can also impact system EMI performance. The CDC6C-Q1 oscillator has different slew rate options to slow down rise/fall times and reduce the impact of higher order harmonics in the emission spectrum. Similarly, the LMK3H0102-Q1 and LMK3C0105-Q1 clock generators can operate with spread spectrum clocking (SSC) enabled to reduce the radiated power emissions seen at the REFCLK frequency and the harmonics.

TI clocking devices can pass up to CISPR-25 Class 5 radiated EMI emissions performance. Testing was completed in TI's pre-compliant EMI chamber set up for CISPR-25 with antennas operating up to 1GHz. EMI compliance reports are available for the CDC6C-Q1 and *LMK3C0105 CISPR-25 EMI Report* device families that contain more detail about EMI performance and the testing setup.

			CISPR-25 Radiation Limits (ALSE method) [dBµV/m]						1.8V							
			Class 5			Class 4			Class for CISPR-25				Significant Spurs [dBµV/m]			
Service/Band	Frequency (MHz)	Antenna	Peak	Quasi-Peak	Average	Peak	Quasi-Peak	Average	LMK3C0105 Variant 1	LMK3C0105 Variant 2	LMK3C0105 Variant 3	Competitor XO Variant 4	LMK3C0105 Variant 1	LMK3C0105 Variant 2	LMK3C0105 Variant 3	Competitor XO Variant 4
Analogue broadcast services																
LW	0.15 to 0.3	Monopole	46	33	26	56	43	36	Class 5	Class 5	Class 5	Class 5				
MW	0.53 to 1.8	Monopole	40	27	20	48	35	28	Class 5	Class 5	Class 5	Class 5				
SW	5.9 to 6.2	Monopole	40	27	20	46	33	26	Class 5	Class 5	Class 5	Class 5				
FM	76 to 108	Bi-conical	38	25	18	44	31	24	Class 5	Class 5	Class 5	Class 5				
TV Band I	41 to 88	Bi-conical	28	–	18	34	–	24	Class 5	Class 5	Class 5	Class 5				
TV Band III	174 to 230	Bi-con/LPA	20	–	10	26	–	16	Class 5	Class 5	Class 5	Class 5				
TV Band IV	470 to 944	Log-Periodic	41	–	31	47	–	37	Class 5	Class 5	Class 5	Class 5				
Digital broadcast services																
DAB III	171 to 245	Bi-con/LPA	30	-	20	36	-	26	Class 5	Class 5	Class 5	Class 5				
TV Band III	174 to 230	Bi-con/LPA	30	-	20	36	-	26	Class 5	Class 5	Class 5	Class 5				
DTTV	470 to 770	Log-Periodic	46	-	36	52	-	42	Class 5	Class 5	Class 5	Class 5				
DAB L Band	447 to 1,494	LPA/Horn	54	-	44	60	-	50	Class 5	Class 5	Class 5	Class 5				
SDARS	320 to 2,345	LPA/Horn	58	-	48	64	-	54	Class 5	Class 5	Class 5	Class 5				
Mobile services																
CB	26 to 28	Monopole	40	27	20	46	33	26	Class 5	Class 5	Class 5	Class 5				
VHF	30 to 54	Bi-conical	40	27	20	46	33	26	Class 5	Class 5	Class 5	Class 5				
VHF	68 to 87	Bi-conical	35	22	15	41	28	21	Class 5	Class 5	Class 5	Class 5				
VHF	142 to 175	Bi-conical	35	22	15	41	28	21	Class 5	Class 5	Class 5	Class 5				
Analogue UHF	380 to 512	Log-Periodic	38	25	18	44	31	24	Class 5	Class 5	Class 5	Class 5				
RKE & TPMS 1	300 to 330	Log-Periodic	32	–	18	38	–	24	Class 5	Class 5	Class 5	Class 5				
RKE & TPMS 2	420 to 450	Log-Periodic	32	–	18	38	–	24	Class 5	Class 5	Class 5	Class 5				
Analogue UHF	820 to 960	Log-Periodic	44	31	24	50	37	30	Class 5	Class 5	Class 5	Class 5				
GPS L5	1,156.45 to 1,196.45	Horn	-	-	20	-	-	26	Class 5	Class 5	Class 5	Class 5			**1075 MHz:** AVG = 12	
BDS, B1I	1,553.098 to 1,569.098	Horn	-	-	5.5	-	-	11.5	Class 5	Class 5	Class 5	Class 5				
GPS L1	1,567.42 to 1,583.42	Horn	–	–	10	–	–	16	Class 5	Class 5	Class 5	Class 4-5				**1575 MHz:** AVG = 10
GLONASS L1	1,590.781 to 1,616.594	Horn	–	–	10	–	–	16	Class 5	Class 5	Class 5	Class 5				
Wi-Fi / Bluetooth	2,402 to 2,494	Horn	52	-	32	58	-	38	Class 5	Class 5	Class 5	Class 5			**2470 MHz:** AVG = 22.5	
Wi-Fi	5,150 to 5,350	Horn	59	-	39	65	-	45	Class 5	Class 5	Class 5	Class 5				
Wi-Fi	5,470 to 5,725	Horn	59	-	39	65	-	45	Class 5	Class 5	Class 5	Class 5				
V2X (Wi-Fi)	5,850 to 5,925	Horn	84	-	64	90	-	70	Class 5	Class 5	Class 5	Class 5				

Figure 4-1. CISPR-25 Performance Summary With TI Clocking Devices

5 Summary

Based on the information provided in this application note, this is possible to determine FPD-Link REFCLK jitter requirements for any device configuration. CDC6C-Q1, LMK3H0102-Q1, and LMK3C0105-Q1 can meet FPD-Link III and FPD-Link IV REFCLK jitter requirements with healthy margin for all typical use cases.

6 References

- Texas Instruments, *LMK3C0105 CISPR-25 EMI Report*, application note.
- Texas Instruments, *CDC6Cx-Q1 Low Power LVCMOS Output BAW Oscillator*, data sheet
- Texas Instruments, *LMK3H0102-Q1 Reference-Less 2-Differential or 5-Single-Ended Output PCIe Gen 1-6 Compliant Programmable BAW Clock Generator*, data sheet
- Texas Instruments, *LMK3C0105 Reference-less 5-LVCMOS-Output Programmable BAW Clock Generator*, data sheet
- Tektronix, *DPOJET Jitter, Noise and Eye Diagram Analysis Solution Printable Application Help*

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