User's Guide

LMK05318B Programmer's Guide

ABSTRACT

This programming guide lists the device registers of the LMK05318B.

Trademarks

1 Device Registers

Table 1-1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 1-1 should be considered as reserved locations and the register contents should not be modified.

Table 1-1. DEVICE Registers

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0	R0	VNDRID_15:8							
0x1	R1	VNDRID							
0x2	R2	PRODID							
0x3	R3	REVID							
0x4	R4	PRTID_31:24							
0x5	R5	PRTID_23:16							
0x6	R6	PRTID_15:8							
0x7	R7	PRTID							
0x8	R8	RESERVED	HW_SW_CTRL_MODE	RESERVED			OP_MODE		
0xA	R10	I2C_ADDR_GPIO1_SW					RESERVED		
0xB	R11	EEREV							
0xC	R12	RESET_SW	SYNC_SW	RESERVED	SYNC_AUTO_APLL	SYNC_MUTE	RESERVED	PLLSTRTMODE	RESERVED
0xD	R13	RESERVED			LOS_FDET_XO	LOL_PLL2	LOL_PLL1	RESERVED	LOS_XO
0xE	R14	LOPL_DPLL	LOFL_DPLL	HIST	HLDOVR	REFSWITCH	LOR_MISSCLK	LOR_FREQ	LOR_AMP
0xF	R15	RESERVED			LOS_FDET_XO_MASK	LOL_PLL2_MASK	LOL_PLL1_MASK	RESERVED	LOS_XO_MASK
0x10	R16	LOPL_DPLL_MASK	LOFL_DPLL_MASK	HIST_MASK	HLDOVR_MASK	REFSWITCH_MASK	LOR_MISSCLK_MASK	LOR_FREQ_MASK	LOR_AMP_MASK
0x11	R17	RESERVED			LOS_FDET_XO_POL	LOL_PLL2_POL	LOL_PLL1_POL	RESERVED	LOS_XO_POL
0x12	R18	LOPL_DPLL_POL	LOFL_DPLL_POL	HIST_POL	HLDOVR_POL	REFSWITCH_POL	LOR_MISSCLK_POL	LOR_FREQ_POL	LOR_AMP_POL
0x13	R19	RESERVED			LOS_FDET_XO_INTR	LOL_PLL2_INTR	LOL_PLL1_INTR	RESERVED	LOS_XO_INTR
0x14	R20	LOPL_DPLL_INTR	LOFL_DPLL_INTR	HIST_INTR	HLDOVR_INTR	REFSWITCH_INTR	LOR_MISSCLK_INTR	LOR_FREQ_INTR	LOR_AMP_INTR
0x15	R21	RESERVED						INT_AND_OR	INT_EN
0x16	R22	RESERVED						STAT1_POL	STAT0_POL
0x17	R23	CH3_MUTE_LVL		CH2_MUTE_LVL		CH1_MUTE_LVL		CH0_MUTE_LVL	
0x18	R24	CH7_MUTE_LVL		CH6_MUTE_LVL		CH5_MUTE_LVL		CH4_MUTE_LVL	

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x19	R25	CH7_MUTE	CH6_MUTE	CH5_MUTE	CH4_MUTE	CH3_MUTE	CH2_MUTE	CH1_MUTE	CH0_MUTE
0x1D	R29	RESERVED			MUTE_APLL2_LOCK	RESERVED	MUTE_DPLL_PHLOCK	MUTE_DPLL_FRLOCK	MUTE_APLL1_LOCK
0x24	R36	RESERVED						GPIO_STAT1_OUT	GPIO_STAT0_OUT
0x27	R39	RESERVED						GPIO2_OUT	APLL1_DEN_MODE
0x28	R40	RESERVED				SECREF_DC_MODE	PRIREF_DC_MODE	RESERVED	APLL2_DEN_MODE
0x2A	R42	RESERVED			OSCIN_DBLR_EN	XO_FDET_BYP	RESERVED		
0x2B	R43	RESERVED	XO_TYPE				RESERVED		XO_DRV_APLL2_EN
0x2C	R44	RESERVED			OSCIN_RDIV				
0x2D	R45	RESERVED				SECREF_CMOS_SLEW	PRIREF_CMOS_SLEW	SECREF_BUF_MODE	PRIREF_BUF_MODE
0x2E	R46	SECREF_TYPE				PRIREF_TYPE			
0x2F	R47	PLL2_RCLK_SEL	RESERVED						
0x30	R48	RESERVED	STAT0_SEL						
0x31	R49	RESERVED	STAT1_SEL						
0x32	R50	GPIO_FDEV_EN	RESERVED	CH7_PD	CH6_PD	CH5_PD	CH4_PD	CH2_3_PD	CH0_1_PD
0x33	R51	CH0_1_MUX		OUT0_SEL		OUT0_MODE1		OUT0_MODE2	
0x34	R52	RESERVED		OUT1_SEL		OUT1_MODE1		OUT1_MODE2	
0x35	R53	OUT0_1_DIV							
0x36	R54	CH2_3_MUX		OUT2_SEL		OUT2_MODE1		OUT2_MODE2	
0x37	R55	RESERVED		OUT3_SEL		OUT3_MODE1		OUT3_MODE2	
0x38	R56	OUT2_3_DIV							
0x39	R57	CH4_MUX		OUT4_SEL		OUT4_MODE1		OUT4_MODE2	
0x3A	R58	OUT4_DIV							
0x3B	R59	CH5_MUX		OUT5_SEL		OUT5_MODE1		OUT5_MODE2	
0x3C	R60	OUT5_DIV							
0x3D	R61	CH6_MUX		OUT6_SEL		OUT6_MODE1		OUT6_MODE2	
0x3E	R62	OUT6_DIV							
0x3F	R63	CH7_MUX		OUT7_SEL		OUT7_MODE1		OUT7_MODE2	
0x40	R64	OUT7_STG2_DIV_23:16							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x41	R65	OUT7_STG2_DIV_15:8							
0x42	R66	OUT7_STG2_DIV							
0x43	R67	OUT7_DIV							
0x44	R68	RESERVED				PLL1_CP_BAW			
0x46	R70	RESERVED					PLL2_P2_SYNC_EN	PLL2_P1_SYNC_EN	PLL1_P1_SYNC_EN
0x47	R71	RESERVED		CH7_SYNC_EN	CH6_SYNC_EN	CH5_SYNC_EN	CH4_SYNC_EN	CH2_3_SYNC_EN	CH0_1_SYNC_EN
0x48	R72	RESERVED		CH7_ACT	CH6_ACT	CH5_ACT	CH4_ACT	CH2_3_ACT	CH0_1_ACT
0x49	R73	RESERVED						REF_BYPASS_EN	REF_BYPASS_SEL
0x4A	R74	RESERVED							PLL1_PDN
0x4B	R75	RESERVED					PLL1_VM_BYP	PLL1_CP	
0x4C	R76	RESERVED					PLL1_P1		
0x4D	R77	RESERVED				PLL1_DISABLE_3RD4TH			
0x4F	R79	RESERVED			BAW_LOCKDET_EN	RESERVED			
0x50	R80	BAW_LOCK	BAW_LOCK_PPM_MAX_14:8						
0x51	R81	BAW_LOCK_PPM_MAX							
0x52	R82	RESERVED		BAW_LOCK_CNTSTRT_29:24					
0x53	R83	BAW_LOCK_CNTSTRT_23:16							
0x54	R84	BAW_LOCK_CNTSTRT_15:8							
0x55	R85	BAW_LOCK_CNTSTRT							
0x56	R86	RESERVED		BAW_LOCK_VCO_CNTSTRT_29:24					
0x57	R87	BAW_LOCK_VCO_CNTSTRT_23:16							
0x58	R88	BAW_LOCK_VCO_CNTSTRT_15:8							
0x59	R89	BAW_LOCK_VCO_CNTSTRT							
0x5A	R90	RESERVED	BAW_UNLK_PPM_MAX_14:8						
0x5B	R91	BAW_UNLK_PPM_MAX							
0x5C	R92	RESERVED		BAW_UNLK_CNTSTRT_29:24					
0x5D	R93	BAW_UNLK_CNTSTRT_23:16							
0x5E	R94	BAW_UNLK_CNTSTRT_15:8							
0x5F	R95	BAW_UNLK_CNTSTRT							
0x60	R96	RESERVED		BAW_UNLK_VCO_CNTSTRT_29:24					
0x61	R97	BAW_UNLK_VCO_CNTSTRT_23:16							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x62	R98	BAW_UNLK_VCO_CNTSTRT_15:8							
0x63	R99	BAW_UNLK_VCO_CNTSTRT							
0x64	R100	PLL2_RDIV_SEC					PLL2_RDIV_PRE		PLL2_PDN
0x65	R101	RESERVED						PLL2_CP	
0x66	R102	RESERVED	PLL2_P2			RESERVED	PLL2_P1		
0x67	R103	RESERVED				PLL2_DISABLE_3RD4TH			
0x68	R104	RESERVED		PLL2_RBLEED_CP					
0x69	R105	RESERVED				PLL2_CLSDWAIT		RESERVED	
0x6A	R106	RESERVED				PLL1_NDLYDIV_11:8			
0x6B	R107	PLL1_NDLYDIV							
0x6C	R108	RESERVED				PLL1_NDIV_11:8			
0x6D	R109	PLL1_NDIV							
0x6E	R110	PLL1_NUM_39:32							
0x6F	R111	PLL1_NUM_31:24							
0x70	R112	PLL1_NUM_23:16							
0x71	R113	PLL1_NUM_15:8							
0x72	R114	PLL1_NUM							
0x73	R115	RESERVED			PLL1_DTHRMODE		PLL1_ORDER		
0x74	R116	RESERVED						PLL1_FDEV_EN	PLL1_MODE
0x75	R117	RESERVED		PLL1_FDEV_37:32					
0x76	R118	PLL1_FDEV_31:24							
0x77	R119	PLL1_FDEV_23:16							
0x78	R120	PLL1_FDEV_15:8							
0x79	R121	PLL1_FDEV							
0x7B	R123	PLL1_NUM_STAT_39:32							
0x7C	R124	PLL1_NUM_STAT_31:24							
0x7D	R125	PLL1_NUM_STAT_23:16							
0x7E	R126	PLL1_NUM_STAT_15:8							
0x7F	R127	PLL1_NUM_STAT							
0x81	R129	RESERVED		PLL1_LF_R2					
0x82	R130	RESERVED					PLL1_LF_C1		
0x83	R131	RESERVED		PLL1_LF_R3					
0x84	R132	RESERVED		PLL1_LF_R4					
0x85	R133	RESERVED	PLL1_LF_C4			RESERVED	PLL1_LF_C3		

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x86	R134	RESERVED							PLL2_NDIV_8:8
0x87	R135	PLL2_NDIV							
0x88	R136	PLL2_NUM_23:16							
0x89	R137	PLL2_NUM_15:8							
0x8A	R138	PLL2_NUM							
0x8B	R139	RESERVED			PLL2_DTHRMODE		PLL2_ORDER		
0x8C	R140	RESERVED		PLL2_LF_R2					
0x8D	R141	RESERVED					PLL2_LF_C1		
0x8E	R142	RESERVED		PLL2_LF_R3					
0x8F	R143	RESERVED		PLL2_LF_R4					
0x90	R144	RESERVED	PLL2_LF_C4			RESERVED	PLL2_LF_C3		
0x91	R145	RESERVED					XO_TIMER		
0x9B	R155	NVMSCRC							
0x9C	R156	NVMCNT							
0x9D	R157	RESERVED	REGCOMMIT	NVMCRCERR	RESERVED	NVMCOMMIT	NVMBUSY	RESERVED	
0x9E	R158	NVMLCRC							
0x9F	R159	RESERVED			MEMADR_12:8				
0xA0	R160	MEMADR							
0xA1	R161	NVMDAT							
0xA2	R162	RAMDAT							
0xA4	R164	NVMUNLK							
0xA7	R167	RESERVED						DPLL_REFSEL_STAT	
0xA8	R168	RESERVED					DPLL_PHASE_LOCK	DPLL_LOCK	RESERVED
0xB4	R180	RESERVED		DPLL_TUNING_FREE_RUN_37:32					
0xB5	R181	DPLL_TUNING_FREE_RUN_31:24							
0xB6	R182	DPLL_TUNING_FREE_RUN_23:16							
0xB7	R183	DPLL_TUNING_FREE_RUN_15:8							
0xB8	R184	DPLL_TUNING_FREE_RUN							
0xB9	R185	DPLL_REF_HIST_INTMD				RESERVED			DPLL_REF_HIST_EN
0xBA	R186	RESERVED			DPLL_REF_HISTCNT				
0xBB	R187	RESERVED	DPLL_REF_HISTDLY_30:24						
0xBC	R188	DPLL_REF_HISTDLY_23:16							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xBD	R189	DPLL_REF_HISTDLY_15:8							
0xBE	R190	DPLL_REF_HISTDLY							
0xBF	R191	RESERVED						REF_DPLL_DBLR_EN	REF_DPLL_EN
0xC0	R192	DETECT_MODE_SECREF		DETECT_MODE_PRIREF		SECREF_LVL_SEL		PRIREF_LVL_SEL	
0xC1	R193	RESERVED		PRIREF_EARLY_DET_EN	PRIREF_PH_VALID_EN	PRIREF_VALTMR_EN	PRIREF_PPM_EN	PRIREF_MISSCLK_EN	PRIREF_AMPDET_EN
0xC2	R194	RESERVED		SECREF_EARLY_DET_EN	SECREF_PH_VALID_EN	SECREF_VALTMR_EN	SECREF_PPM_EN	SECREF_MISSCLK_EN	SECREF_AMPDET_EN
0xC3	R195	RESERVED		PRIREF_MISSCLK_DIV_21:16					
0xC4	R196	PRIREF_MISSCLK_DIV_15:8							
0xC5	R197	PRIREF_MISSCLK_DIV							
0xC6	R198	RESERVED		SECREF_MISSCLK_DIV_21:16					
0xC7	R199	SECREF_MISSCLK_DIV_15:8							
0xC8	R200	SECREF_MISSCLK_DIV							
0xC9	R201	RESERVED						SECREF_WINDOW_DET_DBLR_EN	PRIREF_WINDOW_DET_DBLR_EN
0xCA	R202	RESERVED		PRIREF_EARLY_CLK_DIV_21:16					
0xCB	R203	PRIREF_EARLY_CLK_DIV_15:8							
0xCC	R204	PRIREF_EARLY_CLK_DIV							
0xCD	R205	RESERVED		SECREF_EARLY_CLK_DIV_21:16					
0xCE	R206	SECREF_EARLY_CLK_DIV_15:8							
0xCF	R207	SECREF_EARLY_CLK_DIV							
0xD0	R208	RESERVED	PRIREF_PPM_MIN_14:8						
0xD1	R209	PRIREF_PPM_MIN							
0xD2	R210	RESERVED	PRIREF_PPM_MAX_14:8						
0xD3	R211	PRIREF_PPM_MAX							
0xD4	R212	RESERVED	SECREF_PPM_MIN_14:8						
0xD5	R213	SECREF_PPM_MIN							
0xD6	R214	RESERVED	SECREF_PPM_MAX_14:8						
0xD7	R215	SECREF_PPM_MAX							
0xD8	R216	RESERVED				SECREF_PPMDIV		PRIREF_PPMDIV	
0xD9	R217	RESERVED				PRIREF_CNTSTRT_27:24			
0xDA	R218	PRIREF_CNTSTRT_23:16							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xDB	R219	PRIREF_CNTSTRT_15:8							
0xDC	R220	PRIREF_CNTSTRT							
0xDD	R221	RESERVED				PRIREF_HOLD_CNTSTRT_27:24			
0xDE	R222	PRIREF_HOLD_CNTSTRT_23:16							
0xDF	R223	PRIREF_HOLD_CNTSTRT_15:8							
0xE0	R224	PRIREF_HOLD_CNTSTRT							
0xE1	R225	RESERVED				SECREF_CNTSTRT_27:24			
0xE2	R226	SECREF_CNTSTRT_23:16							
0xE3	R227	SECREF_CNTSTRT_15:8							
0xE4	R228	SECREF_CNTSTRT							
0xE5	R229	RESERVED				SECREF_HOLD_CNTSTRT_27:24			
0xE6	R230	SECREF_HOLD_CNTSTRT_23:16							
0xE7	R231	SECREF_HOLD_CNTSTRT_15:8							
0xE8	R232	SECREF_HOLD_CNTSTRT							
0xE9	R233	RESERVED			PRIREFVLDTMR				
0xEA	R234	RESERVED			SECREFVLDTMR				
0xEB	R235	RESERVED	PRIREF_PH_VALID_CNT_30:24						
0xEC	R236	PRIREF_PH_VALID_CNT_23:16							
0xED	R237	PRIREF_PH_VALID_CNT_15:8							
0xEE	R238	PRIREF_PH_VALID_CNT							
0xEF	R239	RESERVED	SECREF_PH_VALID_CNT_30:24						
0xF0	R240	SECREF_PH_VALID_CNT_23:16							
0xF1	R241	SECREF_PH_VALID_CNT_15:8							
0xF2	R242	SECREF_PH_VALID_CNT							
0xF3	R243	RESERVED		PRIREF_PH_VALID_THR					
0xF4	R244	RESERVED		SECREF_PH_VALID_THR					
0xF9	R249	RESERVED		DPLL_SECREF_AUTO_PRTY		RESERVED		DPLL_PRIREF_AUTO_PRTY	
0xFB	R251	RESERVED		DPLL_REF_MAN_SEL	DPLL_REF_MAN_REG_SEL	RESERVED		DPLL_SWITCH_MODE	
0xFC	R252	DPLL_REF_SYNC_OUT7_EN	DPLL_REF_SYNC_OUT7_NDIV_RST_DIS	DPLL_SWITCHOVER_ALWAYS	DPLL_FASTLOCK_ALWAYS	DPLL_LOCKDET_PPM_EN	DPLL_HLDOVR_MODE	RESERVED	DPLL_LOOP_EN
0x100	R256	DPLL_PRIREF_RDIV_15:8							
0x101	R257	DPLL_PRIREF_RDIV							
0x102	R258	DPLL_SECREF_RDIV_15:8							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x103	R259	DPLL_SECREF_RDIV							
0x11E	R286	RESERVED						DPLL_REF_TMR_FL1_9:8	
0x11F	R287	DPLL_REF_TMR_FL1							
0x120	R288	RESERVED						DPLL_REF_TMR_FL2_9:8	
0x121	R289	DPLL_REF_TMR_FL2							
0x122	R290	RESERVED						DPLL_REF_TMR_LCK_9:8	
0x123	R291	DPLL_REF_TMR_LCK							
0x12D	R301	RESERVED		DPLL_PL_LOCK_THRESH					
0x12E	R302	RESERVED		DPLL_PL_UNLK_THRESH					
0x130	R304	RESERVED				DPLL_REF_FB_PRE_DIV			
0x131	R305	RESERVED		DPLL_REF_FB_DIV_29:24					
0x132	R306	DPLL_REF_FB_DIV_23:16							
0x133	R307	DPLL_REF_FB_DIV_15:8							
0x134	R308	DPLL_REF_FB_DIV							
0x135	R309	DPLL_REF_NUM_39:32							
0x136	R310	DPLL_REF_NUM_31:24							
0x137	R311	DPLL_REF_NUM_23:16							
0x138	R312	DPLL_REF_NUM_15:8							
0x139	R313	DPLL_REF_NUM							
0x13A	R314	DPLL_REF_DEN_39:32							
0x13B	R315	DPLL_REF_DEN_31:24							
0x13C	R316	DPLL_REF_DEN_23:16							
0x13D	R317	DPLL_REF_DEN_15:8							
0x13E	R318	DPLL_REF_DEN							
0x140	R320	RESERVED	DPLL_REF_LOCKDET_PPM_MAX_14:8						
0x141	R321	DPLL_REF_LOCKDET_PPM_MAX							
0x142	R322	RESERVED		DPLL_REF_LOCKDET_CNTSTRT_29:24					
0x143	R323	DPLL_REF_LOCKDET_CNTSTRT_23:16							
0x144	R324	DPLL_REF_LOCKDET_CNTSTRT_15:8							
0x145	R325	DPLL_REF_LOCKDET_CNTSTRT							
0x146	R326	RESERVED		DPLL_REF_LOCKDET_VCO_CNTSTRT_29:24					
0x147	R327	DPLL_REF_LOCKDET_VCO_CNTSTRT_23:16							
0x148	R328	DPLL_REF_LOCKDET_VCO_CNTSTRT_15:8							
0x149	R329	DPLL_REF_LOCKDET_VCO_CNTSTRT							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x14A	R330	RESERVED	DPLL_REF_UNLOCKDET_PPM_MAX_14:8						
0x14B	R331	DPLL_REF_UNLOCKDET_PPM_MAX							
0x14C	R332	RESERVED		DPLL_REF_UNLOCKDET_CNTSTRT_29_24					
0x14D	R333	PLL2_DEN_23:16							
0x14E	R334	PLL2_DEN_15:8							
0x14F	R335	PLL2_DEN							
0x150	R336	RESERVED		DPLL_REF_UNLOCKDET_VCO_CNTSTRT_29_24					
0x151	R337	DPLL_REF_UNLOCKDET_VCO_CNTSTRT_23_16							
0x152	R338	DPLL_REF_UNLOCKDET_VCO_CNTSTRT_15_8							
0x153	R339	PLL1_24b_NUM_MSB							
0x154	R340	RESERVED			DPLL_REF_SYNC_PH_OFFSET_44:40				
0x155	R341	DPLL_REF_SYNC_PH_OFFSET_39:32							
0x156	R342	DPLL_REF_SYNC_PH_OFFSET_31:24							
0x157	R343	DPLL_REF_SYNC_PH_OFFSET_23:16							
0x158	R344	DPLL_REF_SYNC_PH_OFFSET_15:8							
0x159	R345	DPLL_REF_SYNC_PH_OFFSET							
0x15A	R346	RESERVED							DPLL_FDEV_EN
0x15B	R347	RESERVED		DPLL_FDEV_37:32					
0x15C	R348	DPLL_FDEV_31:24							
0x15D	R349	DPLL_FDEV_23:16							
0x15E	R350	DPLL_FDEV_15:8							
0x15F	R351	DPLL_FDEV							
0x165	R357	RESERVED		PLL1_VM_INSIDE	RESERVED				
0x16F	R367	RESERVED		PLL2_VM_INSIDE	RESERVED				
0x19B	R411	RESERVED				SECREF_VALSTAT	PRIREF_VALSTAT	RESERVED	

Complex bit access types are encoded to fit into small table cells. Table 1-2 shows the codes that are used for access types in this section.

Table 1-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read

Table 1-2. Device Access Type Codes (continued)

Access Type	Code	Description
Write Type		
W	W	Write
WSC	W	Write
Reset or Default Value		
-n		Value after reset or the default value

1.1 R0 (Offset = 0x0)

Return to the Summary Table.

Table 1-3. R0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VNDRID_15:8	R	0x10	Bits 15:8 of VNDRID

1.2 R1 (Offset = 0x1)

Return to the Summary Table.

Table 1-4. R1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VNDRID	R	0xB	Vendor Identification Number Unique 16-bit number assigned to chip vendors.

1.3 R2 (Offset = 0x2)

Return to the Summary Table.

Table 1-5. R2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRODID	R	0x35	Product Identification Number Unique 8-bit number used to identify each different LMK05318B device.

1.4 R3 (Offset = 0x3)

Return to the Summary Table.

Table 1-6. R3 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REVID	R	0x2A	Device Revision Number Used to identify the mask-set revision.

1.5 R4 (Offset = 0x4)

Return to the Summary Table.

Table 1-7. R4 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRTID_31:24	R	0x4	Bits 31:24 of PRTID

1.6 R5 (Offset = 0x5)

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Table 1-8. R5 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRTID_23:16	R	0xE	Bits 23:16 of PRTID

1.7 R6 (Offset = 0x6)

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Table 1-9. R6 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRTID_15:8	R	0x17	Bits 15:8 of PRTID

1.8 R7 (Offset = 0x7)

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Table 1-10. R7 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRTID	R	0x0	Part Identification Number 32-bit number used to serialize individual LMK05318 devices. Factory programmed. Cannot be modified by the user.

1.9 R8 (Offset = 0x8)

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Table 1-11. R8 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	HW_SW_CTRL_MODE	R	0x0	HW_SW_CTRL Pin Configuration Reflects the values sampled on the HW_SW_CTRL pin during device power-on reset (POR). 0x0 = Soft Pin Mode 0x1 = Hard Pin Mode
5:3	RESERVED	R	0x0	Reserved
2:0	OP_MODE	R	0x2	Operating Mode The OP_MODE fields reflects the device operating mode as determined by the input levels on the HW_SW_CTRL, STATUS0, and STATUS1 pins respectively during POR. 0x0 = Reserved 0x1 = Reserved 0x2 = EEPROM + I2C, Soft pin mode [HW_SW_CTRL=0, STATUS0=X, STATUS1=X] 0x3 = ROM + I2C, Hard pin mode [HW_SW_CTRL=1, STATUS0=X, STATUS1=X] 0x4 = EEPROM + SPI, Soft pin mode [HW_SW_CTRL=F, STATUS0=F, STATUS1=F]

1.10 R10 (Offset = 0xA)

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Table 1-12. R10 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	I2C_ADDR_GPIO1_SW	R	0x19	7-bit I2C Target Address The five MSBs (base address bits) are programmable in EEPROM, which is 11001b for generic factory devices. The two LSBs are determined by control input pin levels. When the HW_SW_CTRL pin is 1, the two LSBs are fixed to 00b. When the HW_SW_CTRL pin is 0, the 2 LSBs are determined the GPIO1 input state (3-level) during POR. 0x0 = 0x00 + GPIO1 0x1 = 0x04 + GPIO1 0x2 = 0x08 + GPIO1 0x3 = 0x0C + GPIO1 0x4 = 0x10 + GPIO1 0x5 = 0x14 + GPIO1 0x6 = 0x18 + GPIO1 0x7 = 0x1C + GPIO1 0x8 = 0x20 + GPIO1 0x9 = 0x24 + GPIO1 0xA = 0x28 + GPIO1 0xB = 0x2C + GPIO1 0xC = 0x30 + GPIO1 0xD = 0x34 + GPIO1 0xE = 0x38 + GPIO1 0xF = 0x3C + GPIO1 0x10 = 0x40 + GPIO1 0x11 = 0x44 + GPIO1 0x12 = 0x48 + GPIO1 0x13 = 0x4C + GPIO1 0x14 = 0x50 + GPIO1 0x15 = 0x54 + GPIO1 0x16 = 0x58 + GPIO1 0x17 = 0x5C + GPIO1 0x18 = 0x60 + GPIO1 0x19 = 0x64 + GPIO1 0x1A = 0x68 + GPIO1 0x1B = 0x6C + GPIO1 0x1C = 0x70 + GPIO1 0x1D = 0x74 + GPIO1 0x1E = 0x78 + GPIO1 0x1F = 0x7C + GPIO1
2:0	RESERVED	R	0x0	Reserved

1.11 R11 (Offset = 0xB)

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Table 1-13. R11 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	EEREV	R	0x0	EEPROM Image Revision ID The ID value is automatically retrieved from EEPROM at boot-up and reflected in the EEREV register. The register can only be modified through the SRAM and EEPROM programming using the Direct Writes Method, refer to the datasheet for more details.

1.12 R12 (Offset = 0xC)

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Table 1-14. R12 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET_SW	R/W	0x0	Software reset, also known as the APLL recalibration bit Writing a 1 will cause the device to re-initiate the PLL Initialization Sequence, which can cause a momentary interruption on the output clocks, refer to the datasheet for more details. The user register configuration remains unchanged after issuing a software reset. The bit is not self-clearing and must be toggled (0 --> 1 --> 0) to issue the software reset. It is recommended to trigger a software reset after modifying the APLL registers post boot-up. The reset is not necessary after modifying the output channel divider and output format registers.
6	SYNC_SW	R/W	0x0	Output Synchronization (SYNC) Assert bit
5	RESERVED	R	0x0	Reserved
4	SYNC_AUTO_APLL	R/W	0x1	Enable Automatic Output SYNC after PLL lock
3	SYNC_MUTE	R/W	0x1	Determines if the output drivers are muted during a SYNC event 0x0 = Do not mute any outputs during SYNC 0x1 = Mute all outputs during SYNC
2	RESERVED	R	0x0	Reserved
1	PLLSTRTMODE	R/W	0x1	PLL Startup Mode . When using cascade mode, PLL1 is fixed to a center value while PLL2 locks. Then PLL1 performs final lock. Recommended Setting is 0x1. 0x0 = Independent 0x1 = Cascade: PLL2 then PLL1.
0	RESERVED	R	0x0	Reserved

1.13 R13 (Offset = 0xD)

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Table 1-15. R13 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	LOS_FDET_XO	R	0x0	Loss of source freq detection XO
3	LOL_PLL2	R	0x1	Loss of Lock APLL2

Table 1-15. R13 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	LOL_PLL1	R	0x0	Loss of Lock APLL1
1	RESERVED	R	0x0	Reserved
0	LOS_XO	R	0x0	Loss of source XO

1.14 R14 (Offset = 0xE)

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Table 1-16. R14 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL	R	0x0	Loss of phase lock DPLL
6	LOFL_DPLL	R	0x0	Loss of frequency lock DPLL
5	HIST	R	0x0	Tuning word history update DPLL
4	HLDOVR	R	0x0	Holdover event DPLL
3	REFSWITCH	R	0x0	Reference switchover DPLL
2	LOR_MISSCLK	R	0x0	Loss of active reference missing clock DPLL
1	LOR_FREQ	R	0x0	Loss of active reference frequency DPLL
0	LOR_AMP	R	0x0	Loss of active reference amplitude DPLL

1.15 R15 (Offset = 0xF)

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Table 1-17. R15 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	LOS_FDET_XO_MASK	R/W	0x0	Mask Loss of Source Freq Det XO
3	LOL_PLL2_MASK	R/W	0x0	Mask Loss of Lock APLL2
2	LOL_PLL1_MASK	R/W	0x0	Mask Loss of Lock APLL1
1	RESERVED	R	0x0	Reserved
0	LOS_XO_MASK	R/W	0x0	Mask Loss of source XO

1.16 R16 (Offset = 0x10)

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Table 1-18. R16 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL_MASK	R/W	0x0	Mask Loss of Phase Lock DPLL
6	LOFL_DPLL_MASK	R/W	0x0	Mask Loss of Freq Lock DPLL
5	HIST_MASK	R/W	0x0	Mask Tuning word history update DPLL
4	HLDOVR_MASK	R/W	0x0	Mask Holdover event DPLL
3	REFSWITCH_MASK	R/W	0x0	Mask Reference switchover DPLL
2	LOR_MISSCLK_MASK	R/W	0x0	Loss of active reference missing clk DPLL
1	LOR_FREQ_MASK	R/W	0x0	Loss of active reference freq DPLL
0	LOR_AMP_MASK	R/W	0x0	Mask Loss of active reference amplitude DPLL

1.17 R17 (Offset = 0x11)

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Table 1-19. R17 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	LOS_FDET_XO_POL	R/W	0x1	LOS_FDET_XO Flag Polarity
3	LOL_PLL2_POL	R/W	0x1	LOL_PLL2 Flag Polarity
2	LOL_PLL1_POL	R/W	0x1	LOL_PLL1 Flag Polarity
1	RESERVED	R	0x0	Reserved
0	LOS_XO_POL	R/W	0x1	LOS_XO Flag Polarity

1.18 R18 (Offset = 0x12)

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Table 1-20. R18 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL_POL	R/W	0x1	LOPL_DPLL Flag Polarity
6	LOFL_DPLL_POL	R/W	0x1	LOFL_DPLL Flag Polarity
5	HIST_POL	R/W	0x1	HIST Flag Polarity
4	HLDOVR_POL	R/W	0x1	HLDOVR Flag Polarity
3	REFSWITCH_POL	R/W	0x1	REFSWITCH Flag Polarity
2	LOR_MISSCLK_POL	R/W	0x1	LOR_MISSCLK Flag Polarity
1	LOR_FREQ_POL	R/W	0x1	LOR_FREQ Flag Polarity

Table 1-20. R18 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LOR_AMP_POL	R/W	0x1	LOR_AMP Flag Polarity

1.19 R19 (Offset = 0x13)

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Table 1-21. R19 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	LOS_FDET_XO_INTR	R	0x0	LOL_FDET_XO Interrupt Bit is set when an edge of the correct polarity is detected on the LOL_FDET_XO interrupt source. The bit is cleared by writing a 0.
3	LOL_PLL2_INTR	R	0x1	LOL_PLL2 Interrupt Bit is set when an edge of the correct polarity is detected on the LOL_PLL2 interrupt source. The bit is cleared by writing a 0.
2	LOL_PLL1_INTR	R	0x0	LOL_PLL1 Interrupt Bit is set when an edge of the correct polarity is detected on the LOL_PLL1 interrupt source. The bit is cleared by writing a 0.
1	RESERVED	R	0x0	Reserved
0	LOS_XO_INTR	R	0x0	LOS_XO Interrupt Bit is set when an edge of the correct polarity is detected on the LOS_XO interrupt source. The bit is cleared by writing a 0.

1.20 R20 (Offset = 0x14)

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Table 1-22. R20 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL_INTR	R	0x0	LOPL_DPLL Interrupt Bt is set when an edge of the correct polarity is detected on the LOPL_DPLL interrupt source. The bit is cleared by writing a 0.
6	LOFL_DPLL_INTR	R	0x0	LOFL_DPLL Interrupt Bit is set when an edge of the correct polarity is detected on the LOFL_DPLL interrupt source. The bit is cleared by writing a 0.
5	HIST_INTR	R	0x1	HIST Interrupt Bit is set when an edge of the correct polarity is detected on the HIST interrupt source. The bit is cleared by writing a 0.

Table 1-22. R20 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	HLDOVR_INTR	R	0x0	HLDOVR Interrupt Bit is set when an edge of the correct polarity is detected on the HLDOVR interrupt source. The bit is cleared by writing a 0.
3	REFSWITCH_INTR	R	0x0	REFSWITCH Interrupt Bit is set when an edge of the correct polarity is detected on the REFSWITCH interrupt source. The bit is cleared by writing a 0.
2	LOR_MISSCLK_INTR	R	0x0	LOR_MISSCLK Interrupt Bit is set when an edge of the correct polarity is detected on the LOR_MISSCLK interrupt source. The bit is cleared by writing a 0.
1	LOR_FREQ_INTR	R	0x0	LOR_FREQ Interrupt Bit is set when an edge of the correct polarity is detected on the LOR_FREQ interrupt source. The bit is cleared by writing a 0.
0	LOR_AMP_INTR	R	0x0	LOR_AMP Interrupt Bit is set when an edge of the correct polarity is detected on the LOR_AMP interrupt source. The bit is cleared by writing a 0.

1.21 R21 (Offset = 0x15)

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Table 1-23. R21 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	INT_AND_OR	R/W	0x0	Interrupt Logical AND or OR Combination 0x0 = OR 0x1 = AND
0	INT_EN	R/W	0x1	Interrupt Enable

1.22 R22 (Offset = 0x16)

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Table 1-24. R22 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	STAT1_POL	R/W	0x0	STATUS1 Output Polarity. The STAT1_POL bit defines the polarity of information presented on the STATUS1 output. 0x0 = Active high 0x1 = Active low

Table 1-24. R22 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	STAT0_POL	R/W	0x0	STATUS0 Output Polarity. The STAT0_POL bit defines the polarity of information presented on the STATUS0 output. 0x0 = Active high 0x1 = Active low

1.23 R23 (Offset = 0x17)

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Table 1-25. R23 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CH3_MUTE_LVL	R/W	0x1	Output 3 Mute Level See CH0_MUTE_LVL for description and bit settings. 0x0 = Normal operation, Normal operation 0x1 = Powerdown, output goes to Vcm0, Out1 Normal Operation, Out0 Force Input Low 0x2 = Force output High, Out1 Force Input Low, Out0 Normal Operation 0x3 = Force output Low, Out1 Force Input Low, Out0 Force Input Low
5:4	CH2_MUTE_LVL	R/W	0x1	Output 2 Mute Level See CH0_MUTE_LVL for description and bit settings. 0x0 = Normal operation, Normal operation 0x1 = Powerdown, output goes to Vcm0, Out1 Normal Operation, Out0 Force Input Low 0x2 = Force output High, Out1 Force Input Low, Out0 Normal Operation 0x3 = Force output Low, Out1 Force Input Low, Out0 Force Input Low
3:2	CH1_MUTE_LVL	R/W	0x1	Output 1 Mute Level See CH0_MUTE_LVL for description and bit settings. 0x0 = Normal operation, Normal operation 0x1 = Powerdown, output goes to Vcm0, Out1 Normal Operation, Out0 Force Input Low 0x2 = Force output High, Out1 Force Input Low, Out0 Normal Operation 0x3 = Force output Low, Out1 Force Input Low, Out0 Force Input Low
1:0	CH0_MUTE_LVL	R/W	0x1	Output 0 Mute Level Determines the configuration of the Output Driver during mute. 0x0 = Normal operation, Normal operation 0x1 = Powerdown, output goes to Vcm0, Out1 Normal Operation, Out0 Force Input Low 0x2 = Force output High, Out1 Force Input Low, Out0 Normal Operation 0x3 = Force output Low, Out1 Force Input Low, Out0 Force Input Low

1.24 R24 (Offset = 0x18)

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Table 1-26. R24 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CH7_MUTE_LVL	R/W	0x1	Output 7 Mute Level See CH0_MUTE_LVL for description and bit settings. 0x0 = Normal operation, Normal operation 0x1 = Powerdown, output goes to Vcm0, Out1 Normal Operation, Out0 Force Input Low 0x2 = Force output High, Out1 Force Input Low, Out0 Normal Operation 0x3 = Force output Low, Out1 Force Input Low, Out0 Force Input Low
5:4	CH6_MUTE_LVL	R/W	0x1	Output 6 Mute Level See CH0_MUTE_LVL for description and bit settings. 0x0 = Normal operation, Normal operation 0x1 = Powerdown, output goes to Vcm0, Out1 Normal Operation, Out0 Force Input Low 0x2 = Force output High, Out1 Force Input Low, Out0 Normal Operation 0x3 = Force output Low, Out1 Force Input Low, Out0 Force Input Low
3:2	CH5_MUTE_LVL	R/W	0x1	Output 5 Mute Level See CH0_MUTE_LVL for description and bit settings. 0x0 = Normal operation, Normal operation 0x1 = Powerdown, output goes to Vcm0, Out1 Normal Operation, Out0 Force Input Low 0x2 = Force output High, Out1 Force Input Low, Out0 Normal Operation 0x3 = Force output Low, Out1 Force Input Low, Out0 Force Input Low
1:0	CH4_MUTE_LVL	R/W	0x1	Output 4 Mute Level See CH0_MUTE_LVL for description and bit settings. 0x0 = Normal operation, Normal operation 0x1 = Powerdown, output goes to Vcm0, Out1 Normal Operation, Out0 Force Input Low 0x2 = Force output High, Out1 Force Input Low, Out0 Normal Operation 0x3 = Force output Low, Out1 Force Input Low, Out0 Force Input Low

1.25 R25 (Offset = 0x19)

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Table 1-27. R25 Field Descriptions

Bit	Field	Type	Reset	Description
7	CH7_MUTE	R/W	0x0	Output 7 Mute Control
6	CH6_MUTE	R/W	0x0	Output 6 Mute Control
5	CH5_MUTE	R/W	0x0	Output 5 Mute Control
4	CH4_MUTE	R/W	0x0	Output 4 Mute Control
3	CH3_MUTE	R/W	0x0	Output 3 Mute Control
2	CH2_MUTE	R/W	0x0	Output 2 Mute Control
1	CH1_MUTE	R/W	0x0	Output 1 Mute Control
0	CH0_MUTE	R/W	0x0	Output 0 Mute Control

1.26 R29 (Offset = 0x1D)

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Table 1-28. R29 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	MUTE_APLL2_LOCK	R/W	0x1	APLL2 mute enabled during PLL lock
3	RESERVED	R	0x0	Reserved
2	MUTE_DPLL_PHLOCK	R/W	0x0	DPLL mute enabled during phase lock
1	MUTE_DPLL_FRLOCK	R/W	0x1	DPLL mute enabled during DPLL frequency lock
0	MUTE_APLL1_LOCK	R/W	0x1	APLL1 mute enabled during PLL lock

1.27 R36 (Offset = 0x24)

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Table 1-29. R36 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	GPIO_STAT1_OUT	R/W	0x1	STAT1 Driver Type Output 0x0 = NMOS Open Drain 0x1 = CMOS
0	GPIO_STAT0_OUT	R/W	0x1	STAT0 Driver Type Output 0x0 = NMOS Open Drain 0x1 = CMOS

1.28 R39 (Offset = 0x27)

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Table 1-30. R39 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R	0x0	Reserved
1	GPIO2_OUT	R/W	0x1	GPIO2 Driver Type GPIO2 0x0 = NMOS open drain (external pull-up) 0x1 = CMOS

Table 1-30. R39 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	APLL1_DEN_MODE	R/W	0x0	APLL1 denominator mode. 0: Fixed 40-bit APLL1 denominator (chosen if DPLL is enabled) 1: Programmable 24-bit numerator and 24-bit denominator for APLL1 (chosen only in free-running mode where DPLL is powered down)

1.29 R40 (Offset = 0x28)

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Table 1-31. R40 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	SECREF_DC_MODE	R/W	0x0	SECREF DC coupled input buffer mode. 0: AC coupled SECREF 1: DC coupled SECREF
2	PRIREF_DC_MODE	R/W	0x0	PRIREF DC coupled input buffer mode. 0: AC coupled PRIREF 1: DC coupled PRIREF
1	RESERVED	R	0x0	Reserved
0	APLL2_DEN_MODE	R/W	0x1	APLL2 denominator mode. 0: Fixed 24-bit APLL2 denominator 1: Programmable 24-bit APLL2 denominator

1.30 R42 (Offset = 0x2A)

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Table 1-32. R42 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	OSCIN_DBLR_EN	R/W	0x0	Enable OSCIn doubler
3	XO_FDET_BYP	R/W	0x0	XO Frequency Detector Bypass If bypassed, the XO detector status is ignored and the XO input is considered valid by the PLL control state machines
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

1.31 R43 (Offset = 0x2B)

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Table 1-33. R43 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:3	XO_TYPE	R/W	0x8	Set to 1 to enable XO buffer path to APLL2 when the XO input is the APLL reference (R47[7]=1). Set to 0 to disable XO buffer path to APLL2 when the VCO1 cascaded output is the APLL2 reference (R47[7]=0). 0x1 = DIFF (no term.) 0x3 = DIFF (100 Ohm) 0x5 = DIFF (50 Ohm) 0x8 = SE (no term.) 0xC = SE (50 Ohm)
2:1	RESERVED	R	0x0	Reserved
0	XO_DRV_APLL2_EN	R/W	0x0	Select oscillator output to APLL2 reference path

1.32 R44 (Offset = 0x2C)

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Table 1-34. R44 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OSCIN_RDIV	R/W	0x0	Oscillator Input Divider

1.33 R45 (Offset = 0x2D)

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Table 1-35. R45 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	SECREF_CMOS_SLEW	R/W	0x0	SECREF input buffer slew rate 0x0 = Amplitude Detector Mode 0x1 = CMOS Slew Rate Detector Mode
2	PRIREF_CMOS_SLEW	R/W	0x0	PRIREF input buffer slew rate 0x0 = Amplitude Detector Mode 0x1 = CMOS Slew Rate Detector Mode

Table 1-35. R45 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SECREF_BUF_MODE	R/W	0x1	SECREF buffer mode 0: set input hysteresis to 50mV for AC coupled SECREF, or enable hysteresis for DC coupled SECREF 1: set input hysteresis to 200mV for AC coupled SECREF, or disable hysteresis for DC coupled SECREF
0	PRIREF_BUF_MODE	R/W	0x1	PRIREF buffer mode 0: set input hysteresis to 50mV for AC coupled PRIREF, or enable hysteresis for DC coupled PRIREF 1: set input hysteresis to 200mV for AC coupled PRIREF, or disable hysteresis for DC coupled PRIREF

1.34 R46 (Offset = 0x2E)

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Table 1-36. R46 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	SECREF_TYPE	R/W	0x0	SECREF Input Type See PRIREF_TYPE for input type bit settings. 0x1 = DIFF (no term.) 0x3 = DIFF (100 Ohm) 0x5 = DIFF (50 Ohm) 0x8 = SE (no term.) 0xC = SE (50 Ohm)
3:0	PRIREF_TYPE	R/W	0x0	PRIREF Input Type 0x1 = DIFF (no term.) 0x3 = DIFF (100 Ohm) 0x5 = DIFF (50 Ohm) 0x8 = SE (no term.) 0xC = SE (50 Ohm)

1.35 R47 (Offset = 0x2F)

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Table 1-37. R47 Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL2_RCLK_SEL	R/W	0x0	PLL2 Reference clock selection 0x0 = VCO1 - Cascaded Mode (Default) 0x1 = XO
6:4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved

Table 1-37. R47 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	R	0x0	Reserved

1.36 R48 (Offset = 0x30)

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Table 1-38. R48 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-38. R48 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	STAT0_SEL	R/W	0x50	STATUS0 Indicator Signal Select The output pin state of 1 indicates the status condition is true. 0x0 = XO Input Loss of Signal (LOS) 0x1 = Low 0x2 = Reserved 0x3 = PLL1 Digital Lock Detect (DLD) 0x4 = PLL1 VCO Calibration Active 0x5 = PLL1 N Divider, div-by-2 0x6 = PLL2 Digital Lock Detect (DLD) 0x7 = PLL2 VCO Calibration Active 0x8 = PLL2 N Divider, div-by-2 0x9 = EEPROM Active 0xA = Interrupt (INTR) 0xB = Reserved 0xC = DPLL Phase Lock Detected (LOPL* Inverted Signal of DPLL_LOPL status bit) 0xD = PRIREF Monitor Divider Output, div-by-2 0xE = SECREF Monitor Divider Output, div-by-2 0xF = PLL2 R Divider, div-by-2 0x10 = Reserved 0x11 = PRIREF Amplitude Monitor Fault 0x12 = SECREF Amplitude Monitor Fault 0x13 = Reserved 0x14 = Reserved 0x15 = PRIREF Frequency Monitor Fault 0x16 = SECREF Frequency Monitor Fault 0x17 = Reserved 0x18 = Reserved 0x19 = PRIREF Missing or Early Pulse Monitor Fault 0x1A = SECREF Missing or Early Pulse Monitor Fault 0x1B = Reserved 0x1C = Reserved 0x1D = PRIREF Validation Timer Active 0x1E = SECREF Validation Timer Active 0x1F = Reserved 0x20 = Reserved 0x21 = Reserved 0x22 = Reserved 0x23 = Reserved 0x24 = Reserved 0x25 = PRIREF Phase Validation Monitor Fault 0x26 = SECREF Phase Validation Monitor Fault 0x27 = Reserved 0x28 = Reserved 0x29 = PLL1 Lock Detected (LOL*) 0x2A = PLL2 Lock Detected (LOL*) 0x2B = Reserved 0x2C = Reserved 0x2D = Reserved 0x2E = Reserved

Table 1-38. R48 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = Reserved 0x30 = Reserved 0x31 = Reserved 0x32 = Reserved 0x33 = Reserved 0x34 = Reserved 0x35 = Reserved 0x36 = Reserved 0x37 = Reserved 0x38 = Reserved 0x39 = Reserved 0x3A = Reserved 0x3B = Reserved 0x3C = Reserved 0x3D = Reserved 0x3E = Reserved 0x3F = Reserved 0x40 = DPLL R Divider, div-by-2 0x41 = DPLL FB Divider, div-by-2 0x42 = Reserved 0x43 = Reserved 0x44 = Reserved 0x45 = Reserved 0x46 = DPLL PRIREF Selected 0x47 = DPLL SECREF Selected 0x48 = Reserved 0x49 = Reserved 0x4A = DPLL Holdover Active 0x4B = DPLL Reference Switchover Event 0x4C = Reserved 0x4D = DPLL Tuning History Update 0x4E = DPLL Fast Lock Active 0x4F = Reserved 0x50 = DPLL Loss of Lock (LOFL)

1.37 R49 (Offset = 0x31)

Return to the Summary Table.

Table 1-39. R49 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-39. R49 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	STAT1_SEL	R/W	0x4A	STATUS1 Indicator Signal Select See STAT0_SEL for status signal and bit settings. 0x0 = XO Input Loss of Signal (LOS) 0x1 = Low 0x2 = Reserved 0x3 = PLL1 Digital Lock Detect (DLD) 0x4 = PLL1 VCO Calibration Active 0x5 = PLL1 N Divider, div-by-2 0x6 = PLL2 Digital Lock Detect (DLD) 0x7 = PLL2 VCO Calibration Active 0x8 = PLL2 N Divider, div-by-2 0x9 = EEPROM Active 0xA = Interrupt (INTR) 0xB = Reserved 0xC = DPLL Phase Lock Detected (LOPL*Inverted Signal of DPLL_LOPL status bit) 0xD = PRIREF Monitor Divider Output, div-by-2 0xE = SECREF Monitor Divider Output, div-by-2 0xF = PLL2 R Divider, div-by-2 0x10 = Reserved 0x11 = PRIREF Amplitude Monitor Fault 0x12 = SECREF Amplitude Monitor Fault 0x13 = Reserved 0x14 = Reserved 0x15 = PRIREF Frequency Monitor Fault 0x16 = SECREF Frequency Monitor Fault 0x17 = Reserved 0x18 = Reserved 0x19 = PRIREF Missing or Early Pulse Monitor Fault 0x1A = SECREF Missing or Early Pulse Monitor Fault 0x1B = Reserved 0x1C = Reserved 0x1D = PRIREF Validation Timer Active 0x1E = SECREF Validation Timer Active 0x1F = Reserved 0x20 = Reserved 0x21 = Reserved 0x22 = Reserved 0x23 = Reserved 0x24 = Reserved 0x25 = PRIREF Phase Validation Monitor Fault 0x26 = SECREF Phase Validation Monitor Fault 0x27 = Reserved 0x28 = Reserved 0x29 = PLL1 Lock Detected (LOL*) 0x2A = PLL2 Lock Detected (LOL*) 0x2B = Reserved 0x2C = Reserved 0x2D = Reserved 0x2E = Reserved

Table 1-39. R49 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = Reserved 0x30 = Reserved 0x31 = Reserved 0x32 = Reserved 0x33 = Reserved 0x34 = Reserved 0x35 = Reserved 0x36 = Reserved 0x37 = Reserved 0x38 = Reserved 0x39 = Reserved 0x3A = Reserved 0x3B = Reserved 0x3C = Reserved 0x3D = Reserved 0x3E = Reserved 0x3F = Reserved 0x40 = DPLL R Divider, div-by-2 0x41 = DPLL FB Divider, div-by-2 0x42 = Reserved 0x43 = Reserved 0x44 = Reserved 0x45 = Reserved 0x46 = DPLL PRIREF Selected 0x47 = DPLL SECREF Selected 0x48 = Reserved 0x49 = Reserved 0x4A = DPLL Holdover Active 0x4B = DPLL Reference Switchover Event 0x4C = Reserved 0x4D = DPLL Tuning History Update 0x4E = DPLL Fast Lock Active 0x4F = Reserved 0x50 = DPLL Loss of Lock (LOFL)

1.38 R50 (Offset = 0x32)

Return to the Summary Table.

Table 1-40. R50 Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_FDEV_EN	R/W	0x0	Enable DCO Frequency When enabled, a rising edge on these pins will update the DCO frequency accordingly.
6	RESERVED	R	0x0	Reserved

Table 1-40. R50 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CH7_PD	R/W	0x0	Channel 7 Powerdown When CH7_PD is 1 the regulator that supplies the divider and drivers for OUT7 will be disabled.
4	CH6_PD	R/W	0x0	Channel 6 Powerdown When CH6_PD is 1 the regulator that supplies the divider and drivers for OUT6 will be disabled.
3	CH5_PD	R/W	0x0	Channel 5 Powerdown When CH5_PD is 1 the regulator that supplies the divider and drivers for OUT5 will be disabled.
2	CH4_PD	R/W	0x0	Channel 4 Powerdown When CH4_PD is 1 the regulator that supplies the divider and drivers for OUT4 will be disabled.
1	CH2_3_PD	R/W	0x0	Channel 2 and 3 Powerdown When CH2_3_PD is 1 the regulator that supplies the divider and drivers for OUT2 and OUT3 will be disabled.
0	CH0_1_PD	R/W	0x0	Channel 0 and 1 Powerdown When CH0_1_PD is 1 the regulator that supplies the divider and drivers for OUT0 and OUT1 will be disabled.

1.39 R51 (Offset = 0x33)

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Table 1-41. R51 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CH0_1_MUX	R/W	0x0	Channel 0 and 1 Output Mux Selects frequency source for OUT0 and OUT1. 0x0 = APLL1 P1 0x1 = APLL1 P1 Inverted 0x2 = APLL2 P1 0x3 = APLL2 P2
5:4	OUT0_SEL	R/W	0x1	0x0 = Disabled 0x1 = AC-LVPECL/LVDS 0x2 = HCSL 0x3 = Disabled
3:2	OUT0_MODE1	R/W	0x2	0x0 = 4mA 0x1 = 6mA 0x2 = 8mA 0x3 = 8mA for AC-LVPECL/LVDS, 16mA for HCSL

Table 1-41. R51 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	OUT0_MODE2	R/W	0x0	0x0 = Tristate 0x1 = 50Ω 0x2 = 100Ω 0x3 = 200Ω

1.40 R52 (Offset = 0x34)

Return to the Summary Table.

Table 1-42. R52 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	OUT1_SEL	R/W	0x1	0x0 = Disabled 0x1 = AC-LVPECL/LVDS 0x2 = HCSL 0x3 = Disabled
3:2	OUT1_MODE1	R/W	0x2	0x0 = 4mA 0x1 = 6mA 0x2 = 8mA 0x3 = 8mA for AC-LVPECL/LVDS, 16mA for HCSL
1:0	OUT1_MODE2	R/W	0x0	0x0 = Tristate 0x1 = 50Ω 0x2 = 100Ω 0x3 = 200Ω

1.41 R53 (Offset = 0x35)

Return to the Summary Table.

Table 1-43. R53 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT0_1_DIV	R/W	0xF	Channel 0 and Channel 1 Output Divider This is an 8-bit divider. The valid values for OUT0_1_DIV range from 1 to 255. 0x0 = Disabled 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7 0x7 = 8 0x8 = 9 0x9 = 10 0xA = 11 0xB = 12 0xC = 13 0xD = 14 0xE = 15 0xF = 16 0x10 = 17 0x11 = 18 0x12 = 19 0x13 = 20 0x14 = 21 0x15 = 22 0x16 = 23 0x17 = 24 0x18 = 25 0x19 = 26 0x1A = 27 0x1B = 28 0x1C = 29 0x1D = 30 0x1E = 31 0x1F = 32 0x20 = 33 0x21 = 34 0x22 = 35 0x23 = 36 0x24 = 37 0x25 = 38 0x26 = 39 0x27 = 40 0x28 = 41 0x29 = 42 0x2A = 43 0x2B = 44 0x2C = 45 0x2D = 46 0x2E = 47

Table 1-43. R53 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 48 0x30 = 49 0x31 = 50 0x32 = 51 0x33 = 52 0x34 = 53 0x35 = 54 0x36 = 55 0x37 = 56 0x38 = 57 0x39 = 58 0x3A = 59 0x3B = 60 0x3C = 61 0x3D = 62 0x3E = 63 0x3F = 64 0x40 = 65 0x41 = 66 0x42 = 67 0x43 = 68 0x44 = 69 0x45 = 70 0x46 = 71 0x47 = 72 0x48 = 73 0x49 = 74 0x4A = 75 0x4B = 76 0x4C = 77 0x4D = 78 0x4E = 79 0x4F = 80 0x50 = 81 0x51 = 82 0x52 = 83 0x53 = 84 0x54 = 85 0x55 = 86 0x56 = 87 0x57 = 88 0x58 = 89 0x59 = 90 0x5A = 91 0x5B = 92 0x5C = 93 0x5D = 94 0x5E = 95 0x5F = 96

Table 1-43. R53 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x60 = 97 0x61 = 98 0x62 = 99 0x63 = 100 0x64 = 101 0x65 = 102 0x66 = 103 0x67 = 104 0x68 = 105 0x69 = 106 0x6A = 107 0x6B = 108 0x6C = 109 0x6D = 110 0x6E = 111 0x6F = 112 0x70 = 113 0x71 = 114 0x72 = 115 0x73 = 116 0x74 = 117 0x75 = 118 0x76 = 119 0x77 = 120 0x78 = 121 0x79 = 122 0x7A = 123 0x7B = 124 0x7C = 125 0x7D = 126 0x7E = 127 0x7F = 128 0x80 = 129 0x81 = 130 0x82 = 131 0x83 = 132 0x84 = 133 0x85 = 134 0x86 = 135 0x87 = 136 0x88 = 137 0x89 = 138 0x8A = 139 0x8B = 140 0x8C = 141 0x8D = 142 0x8E = 143 0x8F = 144 0x90 = 145

Table 1-43. R53 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x91 = 146 0x92 = 147 0x93 = 148 0x94 = 149 0x95 = 150 0x96 = 151 0x97 = 152 0x98 = 153 0x99 = 154 0x9A = 155 0x9B = 156 0x9C = 157 0x9D = 158 0x9E = 159 0x9F = 160 0xA0 = 161 0xA1 = 162 0xA2 = 163 0xA3 = 164 0xA4 = 165 0xA5 = 166 0xA6 = 167 0xA7 = 168 0xA8 = 169 0xA9 = 170 0xAA = 171 0xAB = 172 0xAC = 173 0xAD = 174 0xAE = 175 0xAF = 176 0xB0 = 177 0xB1 = 178 0xB2 = 179 0xB3 = 180 0xB4 = 181 0xB5 = 182 0xB6 = 183 0xB7 = 184 0xB8 = 185 0xB9 = 186 0xBA = 187 0xBB = 188 0xBC = 189 0xBD = 190 0xBE = 191 0xBF = 192 0xC0 = 193 0xC1 = 194

Table 1-43. R53 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xC2 = 195 0xC3 = 196 0xC4 = 197 0xC5 = 198 0xC6 = 199 0xC7 = 200 0xC8 = 201 0xC9 = 202 0xCA = 203 0xCB = 204 0xCC = 205 0xCD = 206 0xCE = 207 0xCF = 208 0xD0 = 209 0xD1 = 210 0xD2 = 211 0xD3 = 212 0xD4 = 213 0xD5 = 214 0xD6 = 215 0xD7 = 216 0xD8 = 217 0xD9 = 218 0xDA = 219 0xDB = 220 0xDC = 221 0xDD = 222 0xDE = 223 0xDF = 224 0xE0 = 225 0xE1 = 226 0xE2 = 227 0xE3 = 228 0xE4 = 229 0xE5 = 230 0xE6 = 231 0xE7 = 232 0xE8 = 233 0xE9 = 234 0xEA = 235 0xEB = 236 0xEC = 237 0xED = 238 0xEE = 239 0xEF = 240 0xF0 = 241 0xF1 = 242 0xF2 = 243

Table 1-43. R53 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xF3 = 244 0xF4 = 245 0xF5 = 246 0xF6 = 247 0xF7 = 248 0xF8 = 249 0xF9 = 250 0xFA = 251 0xFB = 252 0xFC = 253 0xFD = 254 0xFE = 255 0xFF = 256

1.42 R54 (Offset = 0x36)

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Table 1-44. R54 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CH2_3_MUX	R/W	0x0	Channel 2 and 3 Output Mux Selects frequency source for OUT2 and OUT3. See CH0_1_MUX for bit settings. 0x0 = APLL1 P1 0x1 = APLL1 P1 Inverted 0x2 = APLL2 P1 0x3 = APLL2 P2
5:4	OUT2_SEL	R/W	0x1	0x0 = Disabled 0x1 = AC-LVPECL/LVDS 0x2 = HCSL 0x3 = Disabled
3:2	OUT2_MODE1	R/W	0x2	0x0 = 4mA 0x1 = 6mA 0x2 = 8mA 0x3 = 8mA for AC-LVPECL/LVDS, 16mA for HCSL
1:0	OUT2_MODE2	R/W	0x0	0x0 = Tristate 0x1 = 50Ω 0x2 = 100Ω 0x3 = 200Ω

1.43 R55 (Offset = 0x37)

Return to the Summary Table.

Table 1-45. R55 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	OUT3_SEL	R/W	0x1	0x0 = Disabled 0x1 = AC-LVPECL/LVDS 0x2 = HCSL 0x3 = Disabled
3:2	OUT3_MODE1	R/W	0x2	0x0 = 4mA 0x1 = 6mA 0x2 = 8mA 0x3 = 8mA for AC-LVPECL/LVDS, 16mA for HCSL
1:0	OUT3_MODE2	R/W	0x0	0x0 = Tristate 0x1 = 50Ω 0x2 = 100Ω 0x3 = 200Ω

1.44 R56 (Offset = 0x38)

Return to the Summary Table.

Table 1-46. R56 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT2_3_DIV	R/W	0xF	Channel 2 and Channel 3 Output Divider See OUT0_1_DIV for description and bit settings. 0x0 = Disabled 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7 0x7 = 8 0x8 = 9 0x9 = 10 0xA = 11 0xB = 12 0xC = 13 0xD = 14 0xE = 15 0xF = 16 0x10 = 17 0x11 = 18 0x12 = 19 0x13 = 20 0x14 = 21 0x15 = 22 0x16 = 23 0x17 = 24 0x18 = 25 0x19 = 26 0x1A = 27 0x1B = 28 0x1C = 29 0x1D = 30 0x1E = 31 0x1F = 32 0x20 = 33 0x21 = 34 0x22 = 35 0x23 = 36 0x24 = 37 0x25 = 38 0x26 = 39 0x27 = 40 0x28 = 41 0x29 = 42 0x2A = 43 0x2B = 44 0x2C = 45 0x2D = 46 0x2E = 47

Table 1-46. R56 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 48 0x30 = 49 0x31 = 50 0x32 = 51 0x33 = 52 0x34 = 53 0x35 = 54 0x36 = 55 0x37 = 56 0x38 = 57 0x39 = 58 0x3A = 59 0x3B = 60 0x3C = 61 0x3D = 62 0x3E = 63 0x3F = 64 0x40 = 65 0x41 = 66 0x42 = 67 0x43 = 68 0x44 = 69 0x45 = 70 0x46 = 71 0x47 = 72 0x48 = 73 0x49 = 74 0x4A = 75 0x4B = 76 0x4C = 77 0x4D = 78 0x4E = 79 0x4F = 80 0x50 = 81 0x51 = 82 0x52 = 83 0x53 = 84 0x54 = 85 0x55 = 86 0x56 = 87 0x57 = 88 0x58 = 89 0x59 = 90 0x5A = 91 0x5B = 92 0x5C = 93 0x5D = 94 0x5E = 95 0x5F = 96

Table 1-46. R56 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x60 = 97 0x61 = 98 0x62 = 99 0x63 = 100 0x64 = 101 0x65 = 102 0x66 = 103 0x67 = 104 0x68 = 105 0x69 = 106 0x6A = 107 0x6B = 108 0x6C = 109 0x6D = 110 0x6E = 111 0x6F = 112 0x70 = 113 0x71 = 114 0x72 = 115 0x73 = 116 0x74 = 117 0x75 = 118 0x76 = 119 0x77 = 120 0x78 = 121 0x79 = 122 0x7A = 123 0x7B = 124 0x7C = 125 0x7D = 126 0x7E = 127 0x7F = 128 0x80 = 129 0x81 = 130 0x82 = 131 0x83 = 132 0x84 = 133 0x85 = 134 0x86 = 135 0x87 = 136 0x88 = 137 0x89 = 138 0x8A = 139 0x8B = 140 0x8C = 141 0x8D = 142 0x8E = 143 0x8F = 144 0x90 = 145

Table 1-46. R56 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x91 = 146 0x92 = 147 0x93 = 148 0x94 = 149 0x95 = 150 0x96 = 151 0x97 = 152 0x98 = 153 0x99 = 154 0x9A = 155 0x9B = 156 0x9C = 157 0x9D = 158 0x9E = 159 0x9F = 160 0xA0 = 161 0xA1 = 162 0xA2 = 163 0xA3 = 164 0xA4 = 165 0xA5 = 166 0xA6 = 167 0xA7 = 168 0xA8 = 169 0xA9 = 170 0xAA = 171 0xAB = 172 0xAC = 173 0xAD = 174 0xAE = 175 0xAF = 176 0xB0 = 177 0xB1 = 178 0xB2 = 179 0xB3 = 180 0xB4 = 181 0xB5 = 182 0xB6 = 183 0xB7 = 184 0xB8 = 185 0xB9 = 186 0xBA = 187 0xBB = 188 0xBC = 189 0xBD = 190 0xBE = 191 0xBF = 192 0xC0 = 193 0xC1 = 194

Table 1-46. R56 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xC2 = 195 0xC3 = 196 0xC4 = 197 0xC5 = 198 0xC6 = 199 0xC7 = 200 0xC8 = 201 0xC9 = 202 0xCA = 203 0xCB = 204 0xCC = 205 0xCD = 206 0xCE = 207 0xCF = 208 0xD0 = 209 0xD1 = 210 0xD2 = 211 0xD3 = 212 0xD4 = 213 0xD5 = 214 0xD6 = 215 0xD7 = 216 0xD8 = 217 0xD9 = 218 0xDA = 219 0xDB = 220 0xDC = 221 0xDD = 222 0xDE = 223 0xDF = 224 0xE0 = 225 0xE1 = 226 0xE2 = 227 0xE3 = 228 0xE4 = 229 0xE5 = 230 0xE6 = 231 0xE7 = 232 0xE8 = 233 0xE9 = 234 0xEA = 235 0xEB = 236 0xEC = 237 0xED = 238 0xEE = 239 0xEF = 240 0xF0 = 241 0xF1 = 242 0xF2 = 243

Table 1-46. R56 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xF3 = 244 0xF4 = 245 0xF5 = 246 0xF6 = 247 0xF7 = 248 0xF8 = 249 0xF9 = 250 0xFA = 251 0xFB = 252 0xFC = 253 0xFD = 254 0xFE = 255 0xFF = 256

1.45 R57 (Offset = 0x39)

Return to the Summary Table.

Table 1-47. R57 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CH4_MUX	R/W	0x0	Channel 4 Output Mux Selects frequency source for OUT4. See CH0_1_MUX for bit settings. 0x0 = APLL1 P1 0x1 = APLL1 P1 Inverted 0x2 = APLL2 P1 0x3 = APLL2 P2
5:4	OUT4_SEL	R/W	0x1	0x0 = Disabled 0x1 = AC-LVPECL/LVDS 0x2 = HCSL 0x3 = LVCMOS
3:2	OUT4_MODE1	R/W	0x2	0x0 = 4mA, Powerdown, tristate 0x1 = 6mA, Powerdown, low 0x2 = 8mA, Powerup, negative polarity 0x3 = 8mA for AC-LVPECL/LVDS, 16mA for HCSL, Powerup, positive polarity
1:0	OUT4_MODE2	R/W	0x0	0x0 = Tristate, Powerdown, tristate 0x1 = 50Ω, Powerdown, low 0x2 = 100Ω, Powerup, negative polarity 0x3 = 200Ω, Powerup, positive polarity

1.46 R58 (Offset = 0x3A)

Return to the Summary Table.

Table 1-48. R58 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT4_DIV	R/W	0xF	Channel 4 Output Divider See OUT0_1_DIV for description and bit settings. 0x0 = Disabled 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7 0x7 = 8 0x8 = 9 0x9 = 10 0xA = 11 0xB = 12 0xC = 13 0xD = 14 0xE = 15 0xF = 16 0x10 = 17 0x11 = 18 0x12 = 19 0x13 = 20 0x14 = 21 0x15 = 22 0x16 = 23 0x17 = 24 0x18 = 25 0x19 = 26 0x1A = 27 0x1B = 28 0x1C = 29 0x1D = 30 0x1E = 31 0x1F = 32 0x20 = 33 0x21 = 34 0x22 = 35 0x23 = 36 0x24 = 37 0x25 = 38 0x26 = 39 0x27 = 40 0x28 = 41 0x29 = 42 0x2A = 43 0x2B = 44 0x2C = 45 0x2D = 46 0x2E = 47

Table 1-48. R58 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 48 0x30 = 49 0x31 = 50 0x32 = 51 0x33 = 52 0x34 = 53 0x35 = 54 0x36 = 55 0x37 = 56 0x38 = 57 0x39 = 58 0x3A = 59 0x3B = 60 0x3C = 61 0x3D = 62 0x3E = 63 0x3F = 64 0x40 = 65 0x41 = 66 0x42 = 67 0x43 = 68 0x44 = 69 0x45 = 70 0x46 = 71 0x47 = 72 0x48 = 73 0x49 = 74 0x4A = 75 0x4B = 76 0x4C = 77 0x4D = 78 0x4E = 79 0x4F = 80 0x50 = 81 0x51 = 82 0x52 = 83 0x53 = 84 0x54 = 85 0x55 = 86 0x56 = 87 0x57 = 88 0x58 = 89 0x59 = 90 0x5A = 91 0x5B = 92 0x5C = 93 0x5D = 94 0x5E = 95 0x5F = 96

Table 1-48. R58 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x60 = 97 0x61 = 98 0x62 = 99 0x63 = 100 0x64 = 101 0x65 = 102 0x66 = 103 0x67 = 104 0x68 = 105 0x69 = 106 0x6A = 107 0x6B = 108 0x6C = 109 0x6D = 110 0x6E = 111 0x6F = 112 0x70 = 113 0x71 = 114 0x72 = 115 0x73 = 116 0x74 = 117 0x75 = 118 0x76 = 119 0x77 = 120 0x78 = 121 0x79 = 122 0x7A = 123 0x7B = 124 0x7C = 125 0x7D = 126 0x7E = 127 0x7F = 128 0x80 = 129 0x81 = 130 0x82 = 131 0x83 = 132 0x84 = 133 0x85 = 134 0x86 = 135 0x87 = 136 0x88 = 137 0x89 = 138 0x8A = 139 0x8B = 140 0x8C = 141 0x8D = 142 0x8E = 143 0x8F = 144 0x90 = 145

Table 1-48. R58 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x91 = 146 0x92 = 147 0x93 = 148 0x94 = 149 0x95 = 150 0x96 = 151 0x97 = 152 0x98 = 153 0x99 = 154 0x9A = 155 0x9B = 156 0x9C = 157 0x9D = 158 0x9E = 159 0x9F = 160 0xA0 = 161 0xA1 = 162 0xA2 = 163 0xA3 = 164 0xA4 = 165 0xA5 = 166 0xA6 = 167 0xA7 = 168 0xA8 = 169 0xA9 = 170 0xAA = 171 0xAB = 172 0xAC = 173 0xAD = 174 0xAE = 175 0xAF = 176 0xB0 = 177 0xB1 = 178 0xB2 = 179 0xB3 = 180 0xB4 = 181 0xB5 = 182 0xB6 = 183 0xB7 = 184 0xB8 = 185 0xB9 = 186 0xBA = 187 0xBB = 188 0xBC = 189 0xBD = 190 0xBE = 191 0xBF = 192 0xC0 = 193 0xC1 = 194

Table 1-48. R58 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xC2 = 195 0xC3 = 196 0xC4 = 197 0xC5 = 198 0xC6 = 199 0xC7 = 200 0xC8 = 201 0xC9 = 202 0xCA = 203 0xCB = 204 0xCC = 205 0xCD = 206 0xCE = 207 0xCF = 208 0xD0 = 209 0xD1 = 210 0xD2 = 211 0xD3 = 212 0xD4 = 213 0xD5 = 214 0xD6 = 215 0xD7 = 216 0xD8 = 217 0xD9 = 218 0xDA = 219 0xDB = 220 0xDC = 221 0xDD = 222 0xDE = 223 0xDF = 224 0xE0 = 225 0xE1 = 226 0xE2 = 227 0xE3 = 228 0xE4 = 229 0xE5 = 230 0xE6 = 231 0xE7 = 232 0xE8 = 233 0xE9 = 234 0xEA = 235 0xEB = 236 0xEC = 237 0xED = 238 0xEE = 239 0xEF = 240 0xF0 = 241 0xF1 = 242 0xF2 = 243

Table 1-48. R58 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xF3 = 244 0xF4 = 245 0xF5 = 246 0xF6 = 247 0xF7 = 248 0xF8 = 249 0xF9 = 250 0xFA = 251 0xFB = 252 0xFC = 253 0xFD = 254 0xFE = 255 0xFF = 256

1.47 R59 (Offset = 0x3B)

Return to the Summary Table.

Table 1-49. R59 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CH5_MUX	R/W	0x0	Channel 5 Output Mux Selects frequency source for OUT5. See CH0_1_MUX for bit settings. 0x0 = APLL1 P1 0x1 = APLL1 P1 Inverted 0x2 = APLL2 P1 0x3 = APLL2 P2
5:4	OUT5_SEL	R/W	0x1	0x0 = Disabled 0x1 = AC-LVPECL/LVDS 0x2 = HCSL 0x3 = LVCMOS
3:2	OUT5_MODE1	R/W	0x2	0x0 = 4mA, Powerdown, tristate 0x1 = 6mA, Powerdown, low 0x2 = 8mA, Powerup, negative polarity 0x3 = 8mA for AC-LVPECL/LVDS, 16mA for HCSL, Powerup, positive polarity
1:0	OUT5_MODE2	R/W	0x0	0x0 = Tristate, Powerdown, tristate 0x1 = 50Ω, Powerdown, low 0x2 = 100Ω, Powerup, negative polarity 0x3 = 200Ω, Powerup, positive polarity

1.48 R60 (Offset = 0x3C)

Return to the Summary Table.

Table 1-50. R60 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT5_DIV	R/W	0xF	Channel 5 Output Divider See OUT0_1_DIV for description and bit settings. 0x0 = Disabled 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7 0x7 = 8 0x8 = 9 0x9 = 10 0xA = 11 0xB = 12 0xC = 13 0xD = 14 0xE = 15 0xF = 16 0x10 = 17 0x11 = 18 0x12 = 19 0x13 = 20 0x14 = 21 0x15 = 22 0x16 = 23 0x17 = 24 0x18 = 25 0x19 = 26 0x1A = 27 0x1B = 28 0x1C = 29 0x1D = 30 0x1E = 31 0x1F = 32 0x20 = 33 0x21 = 34 0x22 = 35 0x23 = 36 0x24 = 37 0x25 = 38 0x26 = 39 0x27 = 40 0x28 = 41 0x29 = 42 0x2A = 43 0x2B = 44 0x2C = 45 0x2D = 46 0x2E = 47

Table 1-50. R60 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 48 0x30 = 49 0x31 = 50 0x32 = 51 0x33 = 52 0x34 = 53 0x35 = 54 0x36 = 55 0x37 = 56 0x38 = 57 0x39 = 58 0x3A = 59 0x3B = 60 0x3C = 61 0x3D = 62 0x3E = 63 0x3F = 64 0x40 = 65 0x41 = 66 0x42 = 67 0x43 = 68 0x44 = 69 0x45 = 70 0x46 = 71 0x47 = 72 0x48 = 73 0x49 = 74 0x4A = 75 0x4B = 76 0x4C = 77 0x4D = 78 0x4E = 79 0x4F = 80 0x50 = 81 0x51 = 82 0x52 = 83 0x53 = 84 0x54 = 85 0x55 = 86 0x56 = 87 0x57 = 88 0x58 = 89 0x59 = 90 0x5A = 91 0x5B = 92 0x5C = 93 0x5D = 94 0x5E = 95 0x5F = 96

Table 1-50. R60 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x60 = 97 0x61 = 98 0x62 = 99 0x63 = 100 0x64 = 101 0x65 = 102 0x66 = 103 0x67 = 104 0x68 = 105 0x69 = 106 0x6A = 107 0x6B = 108 0x6C = 109 0x6D = 110 0x6E = 111 0x6F = 112 0x70 = 113 0x71 = 114 0x72 = 115 0x73 = 116 0x74 = 117 0x75 = 118 0x76 = 119 0x77 = 120 0x78 = 121 0x79 = 122 0x7A = 123 0x7B = 124 0x7C = 125 0x7D = 126 0x7E = 127 0x7F = 128 0x80 = 129 0x81 = 130 0x82 = 131 0x83 = 132 0x84 = 133 0x85 = 134 0x86 = 135 0x87 = 136 0x88 = 137 0x89 = 138 0x8A = 139 0x8B = 140 0x8C = 141 0x8D = 142 0x8E = 143 0x8F = 144 0x90 = 145

Table 1-50. R60 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x91 = 146 0x92 = 147 0x93 = 148 0x94 = 149 0x95 = 150 0x96 = 151 0x97 = 152 0x98 = 153 0x99 = 154 0x9A = 155 0x9B = 156 0x9C = 157 0x9D = 158 0x9E = 159 0x9F = 160 0xA0 = 161 0xA1 = 162 0xA2 = 163 0xA3 = 164 0xA4 = 165 0xA5 = 166 0xA6 = 167 0xA7 = 168 0xA8 = 169 0xA9 = 170 0xAA = 171 0xAB = 172 0xAC = 173 0xAD = 174 0xAE = 175 0xAF = 176 0xB0 = 177 0xB1 = 178 0xB2 = 179 0xB3 = 180 0xB4 = 181 0xB5 = 182 0xB6 = 183 0xB7 = 184 0xB8 = 185 0xB9 = 186 0xBA = 187 0xBB = 188 0xBC = 189 0xBD = 190 0xBE = 191 0xBF = 192 0xC0 = 193 0xC1 = 194

Table 1-50. R60 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xC2 = 195 0xC3 = 196 0xC4 = 197 0xC5 = 198 0xC6 = 199 0xC7 = 200 0xC8 = 201 0xC9 = 202 0xCA = 203 0xCB = 204 0xCC = 205 0xCD = 206 0xCE = 207 0xCF = 208 0xD0 = 209 0xD1 = 210 0xD2 = 211 0xD3 = 212 0xD4 = 213 0xD5 = 214 0xD6 = 215 0xD7 = 216 0xD8 = 217 0xD9 = 218 0xDA = 219 0xDB = 220 0xDC = 221 0xDD = 222 0xDE = 223 0xDF = 224 0xE0 = 225 0xE1 = 226 0xE2 = 227 0xE3 = 228 0xE4 = 229 0xE5 = 230 0xE6 = 231 0xE7 = 232 0xE8 = 233 0xE9 = 234 0xEA = 235 0xEB = 236 0xEC = 237 0xED = 238 0xEE = 239 0xEF = 240 0xF0 = 241 0xF1 = 242 0xF2 = 243

Table 1-50. R60 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xF3 = 244 0xF4 = 245 0xF5 = 246 0xF6 = 247 0xF7 = 248 0xF8 = 249 0xF9 = 250 0xFA = 251 0xFB = 252 0xFC = 253 0xFD = 254 0xFE = 255 0xFF = 256

1.49 R61 (Offset = 0x3D)

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Table 1-51. R61 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CH6_MUX	R/W	0x0	Channel 6 Output Mux Selects frequency source for OUT6. See CH0_1_MUX for bit settings. 0x0 = APLL1 P1 0x1 = APLL1 P1 Inverted 0x2 = APLL2 P1 0x3 = APLL2 P2
5:4	OUT6_SEL	R/W	0x1	0x0 = Disabled 0x1 = AC-LVPECL/LVDS 0x2 = HCSL 0x3 = LVCMOS
3:2	OUT6_MODE1	R/W	0x2	0x0 = 4mA, Powerdown, tristate 0x1 = 6mA, Powerdown, low 0x2 = 8mA, Powerup, negative polarity 0x3 = 8mA for AC-LVPECL/LVDS, 16mA for HCSL, Powerup, positive polarity
1:0	OUT6_MODE2	R/W	0x0	0x0 = Tristate, Powerdown, tristate 0x1 = 50Ω, Powerdown, low 0x2 = 100Ω, Powerup, negative polarity 0x3 = 200Ω, Powerup, positive polarity

1.50 R62 (Offset = 0x3E)

Return to the Summary Table.

Table 1-52. R62 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT6_DIV	R/W	0x63	Channel 6 Output Divider See OUT0_1_DIV for description and bit settings. 0x0 = Disabled 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7 0x7 = 8 0x8 = 9 0x9 = 10 0xA = 11 0xB = 12 0xC = 13 0xD = 14 0xE = 15 0xF = 16 0x10 = 17 0x11 = 18 0x12 = 19 0x13 = 20 0x14 = 21 0x15 = 22 0x16 = 23 0x17 = 24 0x18 = 25 0x19 = 26 0x1A = 27 0x1B = 28 0x1C = 29 0x1D = 30 0x1E = 31 0x1F = 32 0x20 = 33 0x21 = 34 0x22 = 35 0x23 = 36 0x24 = 37 0x25 = 38 0x26 = 39 0x27 = 40 0x28 = 41 0x29 = 42 0x2A = 43 0x2B = 44 0x2C = 45 0x2D = 46 0x2E = 47

Table 1-52. R62 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 48 0x30 = 49 0x31 = 50 0x32 = 51 0x33 = 52 0x34 = 53 0x35 = 54 0x36 = 55 0x37 = 56 0x38 = 57 0x39 = 58 0x3A = 59 0x3B = 60 0x3C = 61 0x3D = 62 0x3E = 63 0x3F = 64 0x40 = 65 0x41 = 66 0x42 = 67 0x43 = 68 0x44 = 69 0x45 = 70 0x46 = 71 0x47 = 72 0x48 = 73 0x49 = 74 0x4A = 75 0x4B = 76 0x4C = 77 0x4D = 78 0x4E = 79 0x4F = 80 0x50 = 81 0x51 = 82 0x52 = 83 0x53 = 84 0x54 = 85 0x55 = 86 0x56 = 87 0x57 = 88 0x58 = 89 0x59 = 90 0x5A = 91 0x5B = 92 0x5C = 93 0x5D = 94 0x5E = 95 0x5F = 96

Table 1-52. R62 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x60 = 97 0x61 = 98 0x62 = 99 0x63 = 100 0x64 = 101 0x65 = 102 0x66 = 103 0x67 = 104 0x68 = 105 0x69 = 106 0x6A = 107 0x6B = 108 0x6C = 109 0x6D = 110 0x6E = 111 0x6F = 112 0x70 = 113 0x71 = 114 0x72 = 115 0x73 = 116 0x74 = 117 0x75 = 118 0x76 = 119 0x77 = 120 0x78 = 121 0x79 = 122 0x7A = 123 0x7B = 124 0x7C = 125 0x7D = 126 0x7E = 127 0x7F = 128 0x80 = 129 0x81 = 130 0x82 = 131 0x83 = 132 0x84 = 133 0x85 = 134 0x86 = 135 0x87 = 136 0x88 = 137 0x89 = 138 0x8A = 139 0x8B = 140 0x8C = 141 0x8D = 142 0x8E = 143 0x8F = 144 0x90 = 145

Table 1-52. R62 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x91 = 146 0x92 = 147 0x93 = 148 0x94 = 149 0x95 = 150 0x96 = 151 0x97 = 152 0x98 = 153 0x99 = 154 0x9A = 155 0x9B = 156 0x9C = 157 0x9D = 158 0x9E = 159 0x9F = 160 0xA0 = 161 0xA1 = 162 0xA2 = 163 0xA3 = 164 0xA4 = 165 0xA5 = 166 0xA6 = 167 0xA7 = 168 0xA8 = 169 0xA9 = 170 0xAA = 171 0xAB = 172 0xAC = 173 0xAD = 174 0xAE = 175 0xAF = 176 0xB0 = 177 0xB1 = 178 0xB2 = 179 0xB3 = 180 0xB4 = 181 0xB5 = 182 0xB6 = 183 0xB7 = 184 0xB8 = 185 0xB9 = 186 0xBA = 187 0xBB = 188 0xBC = 189 0xBD = 190 0xBE = 191 0xBF = 192 0xC0 = 193 0xC1 = 194

Table 1-52. R62 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xC2 = 195 0xC3 = 196 0xC4 = 197 0xC5 = 198 0xC6 = 199 0xC7 = 200 0xC8 = 201 0xC9 = 202 0xCA = 203 0xCB = 204 0xCC = 205 0xCD = 206 0xCE = 207 0xCF = 208 0xD0 = 209 0xD1 = 210 0xD2 = 211 0xD3 = 212 0xD4 = 213 0xD5 = 214 0xD6 = 215 0xD7 = 216 0xD8 = 217 0xD9 = 218 0xDA = 219 0xDB = 220 0xDC = 221 0xDD = 222 0xDE = 223 0xDF = 224 0xE0 = 225 0xE1 = 226 0xE2 = 227 0xE3 = 228 0xE4 = 229 0xE5 = 230 0xE6 = 231 0xE7 = 232 0xE8 = 233 0xE9 = 234 0xEA = 235 0xEB = 236 0xEC = 237 0xED = 238 0xEE = 239 0xEF = 240 0xF0 = 241 0xF1 = 242 0xF2 = 243

Table 1-52. R62 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xF3 = 244 0xF4 = 245 0xF5 = 246 0xF6 = 247 0xF7 = 248 0xF8 = 249 0xF9 = 250 0xFA = 251 0xFB = 252 0xFC = 253 0xFD = 254 0xFE = 255 0xFF = 256

1.51 R63 (Offset = 0x3F)

Return to the Summary Table.

Table 1-53. R63 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CH7_MUX	R/W	0x0	Channel 7 Output Mux Selects frequency source for OUT7. See CH0_1_MUX for bit settings. 0x0 = APLL1 P1 0x1 = APLL1 P1 Inverted 0x2 = APLL2 P1 0x3 = APLL2 P2
5:4	OUT7_SEL	R/W	0x1	0x0 = Disabled 0x1 = AC-LVPECL/LVDS 0x2 = HCSL 0x3 = LVCMOS
3:2	OUT7_MODE1	R/W	0x2	0x0 = 4mA, Powerdown, tristate 0x1 = 6mA, Powerdown, low 0x2 = 8mA, Powerup, negative polarity 0x3 = 8mA for AC-LVPECL/LVDS, 16mA for HCSL, Powerup, positive polarity
1:0	OUT7_MODE2	R/W	0x0	0x0 = Tristate, Powerdown, tristate 0x1 = 50Ω, Powerdown, low 0x2 = 100Ω, Powerup, negative polarity 0x3 = 200Ω, Powerup, positive polarity

1.52 R64 (Offset = 0x40)

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Table 1-54. R64 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT7_STG2_DIV_23:16	R/W	0x0	Bits 23:16 of OUT7_STG2_DIV

1.53 R65 (Offset = 0x41)

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Table 1-55. R65 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT7_STG2_DIV_15:8	R/W	0x0	Bits 15:8 of OUT7_STG2_DIV

1.54 R66 (Offset = 0x42)

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Table 1-56. R66 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT7_STG2_DIV	R/W	0x0	Channel 7 Stage Two Output Divider OD2 = OUT7_STG2_DIV + 1 If OD2 > 1, then ODout7 must be ≥ 6. Total output 7 divide value = OD2 * ODout7.

1.55 R67 (Offset = 0x43)

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Table 1-57. R67 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT7_DIV	R/W	0x18	Channel 7 Output Divider This is an 8-bit divider. The valid values for OUT7_DIV range from 1 to 255. ODOUT7 = OUT7_DIV + 1. If OD2 > 1, then total output 7 divide value = OD2 * ODout7 where OD2 is OUT7 secondary output divider value. Note: 0x00 is disabled. 0x0 = Disabled 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7 0x7 = 8 0x8 = 9 0x9 = 10 0xA = 11 0xB = 12 0xC = 13 0xD = 14 0xE = 15 0xF = 16 0x10 = 17 0x11 = 18 0x12 = 19 0x13 = 20 0x14 = 21 0x15 = 22 0x16 = 23 0x17 = 24 0x18 = 25 0x19 = 26 0x1A = 27 0x1B = 28 0x1C = 29 0x1D = 30 0x1E = 31 0x1F = 32 0x20 = 33 0x21 = 34 0x22 = 35 0x23 = 36 0x24 = 37 0x25 = 38 0x26 = 39 0x27 = 40 0x28 = 41 0x29 = 42 0x2A = 43 0x2B = 44

Table 1-57. R67 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2C = 45 0x2D = 46 0x2E = 47 0x2F = 48 0x30 = 49 0x31 = 50 0x32 = 51 0x33 = 52 0x34 = 53 0x35 = 54 0x36 = 55 0x37 = 56 0x38 = 57 0x39 = 58 0x3A = 59 0x3B = 60 0x3C = 61 0x3D = 62 0x3E = 63 0x3F = 64 0x40 = 65 0x41 = 66 0x42 = 67 0x43 = 68 0x44 = 69 0x45 = 70 0x46 = 71 0x47 = 72 0x48 = 73 0x49 = 74 0x4A = 75 0x4B = 76 0x4C = 77 0x4D = 78 0x4E = 79 0x4F = 80 0x50 = 81 0x51 = 82 0x52 = 83 0x53 = 84 0x54 = 85 0x55 = 86 0x56 = 87 0x57 = 88 0x58 = 89 0x59 = 90 0x5A = 91 0x5B = 92 0x5C = 93

Table 1-57. R67 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x5D = 94 0x5E = 95 0x5F = 96 0x60 = 97 0x61 = 98 0x62 = 99 0x63 = 100 0x64 = 101 0x65 = 102 0x66 = 103 0x67 = 104 0x68 = 105 0x69 = 106 0x6A = 107 0x6B = 108 0x6C = 109 0x6D = 110 0x6E = 111 0x6F = 112 0x70 = 113 0x71 = 114 0x72 = 115 0x73 = 116 0x74 = 117 0x75 = 118 0x76 = 119 0x77 = 120 0x78 = 121 0x79 = 122 0x7A = 123 0x7B = 124 0x7C = 125 0x7D = 126 0x7E = 127 0x7F = 128 0x80 = 129 0x81 = 130 0x82 = 131 0x83 = 132 0x84 = 133 0x85 = 134 0x86 = 135 0x87 = 136 0x88 = 137 0x89 = 138 0x8A = 139 0x8B = 140 0x8C = 141 0x8D = 142

Table 1-57. R67 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x8E = 143 0x8F = 144 0x90 = 145 0x91 = 146 0x92 = 147 0x93 = 148 0x94 = 149 0x95 = 150 0x96 = 151 0x97 = 152 0x98 = 153 0x99 = 154 0x9A = 155 0x9B = 156 0x9C = 157 0x9D = 158 0x9E = 159 0x9F = 160 0xA0 = 161 0xA1 = 162 0xA2 = 163 0xA3 = 164 0xA4 = 165 0xA5 = 166 0xA6 = 167 0xA7 = 168 0xA8 = 169 0xA9 = 170 0xAA = 171 0xAB = 172 0xAC = 173 0xAD = 174 0xAE = 175 0xAF = 176 0xB0 = 177 0xB1 = 178 0xB2 = 179 0xB3 = 180 0xB4 = 181 0xB5 = 182 0xB6 = 183 0xB7 = 184 0xB8 = 185 0xB9 = 186 0xBA = 187 0xBB = 188 0xBC = 189 0xBD = 190 0xBE = 191

Table 1-57. R67 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xBF = 192 0xC0 = 193 0xC1 = 194 0xC2 = 195 0xC3 = 196 0xC4 = 197 0xC5 = 198 0xC6 = 199 0xC7 = 200 0xC8 = 201 0xC9 = 202 0xCA = 203 0xCB = 204 0xCC = 205 0xCD = 206 0xCE = 207 0xCF = 208 0xD0 = 209 0xD1 = 210 0xD2 = 211 0xD3 = 212 0xD4 = 213 0xD5 = 214 0xD6 = 215 0xD7 = 216 0xD8 = 217 0xD9 = 218 0xDA = 219 0xDB = 220 0xDC = 221 0xDD = 222 0xDE = 223 0xDF = 224 0xE0 = 225 0xE1 = 226 0xE2 = 227 0xE3 = 228 0xE4 = 229 0xE5 = 230 0xE6 = 231 0xE7 = 232 0xE8 = 233 0xE9 = 234 0xEA = 235 0xEB = 236 0xEC = 237 0xED = 238 0xEE = 239 0xEF = 240

Table 1-57. R67 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xF0 = 241 0xF1 = 242 0xF2 = 243 0xF3 = 244 0xF4 = 245 0xF5 = 246 0xF6 = 247 0xF7 = 248 0xF8 = 249 0xF9 = 250 0xFA = 251 0xFB = 252 0xFC = 253 0xFD = 254 0xFE = 255 0xFF = 256

1.56 R68 (Offset = 0x44)

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Table 1-58. R68 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PLL1_CP_BAW	R/W	0x8	APLL1 Charge Pump Current Gain PLL1_CP_BAW ranges from 0 to 15. Gain = PLL1_CP_BAW x 100 µA. 0x0 = 0 uA 0x1 = 100 uA 0x2 = 200 uA 0x3 = 300 uA 0x4 = 400 uA 0x5 = 500 uA 0x6 = 600 uA 0x7 = 700 uA 0x8 = 800 uA 0x9 = 900 uA 0xA = 1000 uA 0xB = 1100 uA 0xC = 1200 uA 0xD = 1300 uA 0xE = 1400 uA 0xF = 1500 uA

1.57 R70 (Offset = 0x46)

Return to the Summary Table.

Table 1-59. R70 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2	PLL2_P2_SYNC_EN	R/W	0x0	Enable PLL2 P2 divider channel synchronizatrion
1	PLL2_P1_SYNC_EN	R/W	0x0	Enable PLL2 P1 divider channel synchronizatrion
0	PLL1_P1_SYNC_EN	R/W	0x0	Enable PLL1 P1 divider channel synchronizatrion

1.58 R71 (Offset = 0x47)

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Table 1-60. R71 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	CH7_SYNC_EN	R/W	0x0	Enable Channel 7 output synchronization
4	CH6_SYNC_EN	R/W	0x0	Enable Channel 6 output synchronization
3	CH5_SYNC_EN	R/W	0x0	Enable Channel 5 output synchronization
2	CH4_SYNC_EN	R/W	0x0	Enable Channel 4 output synchronization
1	CH2_3_SYNC_EN	R/W	0x0	Enable Channels 2 and 3 output synchronization
0	CH0_1_SYNC_EN	R/W	0x0	Enable Channels 0 and 1 output synchronization

1.59 R72 (Offset = 0x48)

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Table 1-61. R72 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	CH7_ACT	R	0x1	Channel 7 Output Active flag Reads 1 when output channel is powered-up and active.
4	CH6_ACT	R	0x1	Channel 6 Output Active flag Reads 1 when output channel is powered-up and active.
3	CH5_ACT	R	0x0	Channel 45 Output Active flag Reads 1 when output channel is powered-up and active.
2	CH4_ACT	R	0x0	Channel 23 Output Active flag Reads 1 when output channel is powered-up and active.

Table 1-61. R72 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CH2_3_ACT	R	0x1	Channel 1 Output Active flag Reads 1 when output channel is powered-up and active.
0	CH0_1_ACT	R	0x1	Channel 0 Output Active flag Reads 1 when output channel is powered-up and active.

1.60 R73 (Offset = 0x49)

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Table 1-62. R73 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	REF_BYPASS_EN	R/W	0x0	Reference Bypass Selection Enable When ref_bypass_en=1, the reference selected by ref_bypass_sel will be routed to the channel outputs instead of VCO1. 0x0 = VCO1 0x1 = Reference
0	REF_BYPASS_SEL	R/W	0x0	Reference Bypass Selection Register When ref_bypass_en=1, ref_bypass_sel will select which reference input to drive channel outputs. 0x0 = Primary Reference 0x1 = Secondary Reference

1.61 R74 (Offset = 0x4A)

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Table 1-63. R74 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL1_PDN	R/W	0x0	PLL1 Power down The PLL1_PDN bit determines whether PLL1 is automatically enabled and calibrated after a hardware reset. 0x0 = PLL1 Enabled 0x1 = PLL1 Disabled

1.62 R75 (Offset = 0x4B)

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Table 1-64. R75 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2	PLL1_VM_BYP	R/W	0x0	PLL1 Vtune Monitor Bypass
1:0	PLL1_CP	R/W	0x0	PLL1 Charge Pump Gain 0x0 = 1.6 mA 0x1 = 3.2 mA 0x2 = 4.8 mA 0x3 = 6.4 mA

1.63 R76 (Offset = 0x4C)

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Table 1-65. R76 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:0	PLL1_P1	R/W	0x0	PLL1 Post-Divider1 Note: A RESET is required after changing Divider values. 0x0 = Invalid 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7 0x7 = Invalid

1.64 R77 (Offset = 0x4D)

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Table 1-66. R77 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PLL1_DISABLE_3RD4TH	R/W	0xF	PLL1 Loop Filter Settings

1.65 R79 (Offset = 0x4F)

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Table 1-67. R79 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	BAW_LOCKDET_EN	R/W	0x1	BAW Lock Detect Enable
3:0	RESERVED	R	0x0	Reserved

1.66 R80 (Offset = 0x50)

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Table 1-68. R80 Field Descriptions

Bit	Field	Type	Reset	Description
7	BAW_LOCK	R	0x1	BAW Lock Detect Status 0x0 = Unlocked 0x1 = Locked
6:0	BAW_LOCK_PPM_MAX_14:8	R/W	0x0	BAW VCO Lock Detection

1.67 R81 (Offset = 0x51)

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Table 1-69. R81 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_LOCK_PPM_MAX	R/W	0xA	BAW VCO Lock Detection

1.68 R82 (Offset = 0x52)

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Table 1-70. R82 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	BAW_LOCK_CNTSTRT_29:24	R/W	0x0	BAW VCO Lock Detection

1.69 R83 (Offset = 0x53)

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Table 1-71. R83 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_LOCK_CNTSTRT_23:16	R/W	0xE	BAW VCO Lock Detection

1.70 R84 (Offset = 0x54)

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Table 1-72. R84 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_LOCK_CNTSTRT_15:8	R/W	0x10	BAW VCO Lock Detection

1.71 R85 (Offset = 0x55)

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Table 1-73. R85 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_LOCK_CNTSTRT	R/W	0x5D	BAW VCO Lock Detection

1.72 R86 (Offset = 0x56)

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Table 1-74. R86 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	BAW_LOCK_VCO_CNTSTRT_29:24	R/W	0x0	BAW VCO Lock Detection

1.73 R87 (Offset = 0x57)

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Table 1-75. R87 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_LOCK_VCO_CNTSTRT_23:16	R/W	0x1E	BAW VCO Lock Detection

1.74 R88 (Offset = 0x58)

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Table 1-76. R88 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_LOCK_VCO_CNTSTRT_15:8	R/W	0x84	BAW VCO Lock Detection

1.75 R89 (Offset = 0x59)

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Table 1-77. R89 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_LOCK_VCO_CNTSTRT	R/W	0x82	BAW VCO Lock Detection

1.76 R90 (Offset = 0x5A)

Return to the Summary Table.

Table 1-78. R90 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	BAW_UNLK_PPM_MAX_14:8	R/W	0x0	BAW VCO Unlock Detection

1.77 R91 (Offset = 0x5B)

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Table 1-79. R91 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_UNLK_PPM_MAX	R/W	0x14	BAW VCO Unlock Detection

1.78 R92 (Offset = 0x5C)

Return to the Summary Table.

Table 1-80. R92 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-80. R92 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	BAW_UNLK_CNTSTRT_29:24	R/W	0x0	BAW VCO Unlock Detection

1.79 R93 (Offset = 0x5D)

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Table 1-81. R93 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_UNLK_CNTSTRT_23:16	R/W	0xE	BAW VCO Unlock Detection

1.80 R94 (Offset = 0x5E)

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Table 1-82. R94 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_UNLK_CNTSTRT_15:8	R/W	0x10	BAW VCO Unlock Detection

1.81 R95 (Offset = 0x5F)

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Table 1-83. R95 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_UNLK_CNTSTRT	R/W	0x5D	BAW VCO Unlock Detection

1.82 R96 (Offset = 0x60)

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Table 1-84. R96 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	BAW_UNLK_VCO_CNTSTRT_29:24	R/W	0x0	BAW VCO Unlock Detection

1.83 R97 (Offset = 0x61)

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Table 1-85. R97 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_UNLK_VCO_CNTSTRT_23:16	R/W	0x1E	BAW VCO Unlock Detection

1.84 R98 (Offset = 0x62)

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Table 1-86. R98 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_UNLK_VCO_CNTSTRT_15:8	R/W	0x84	BAW VCO Unlock Detection

1.85 R99 (Offset = 0x63)

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Table 1-87. R99 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_UNLK_VCO_CNTSTRT	R/W	0x82	BAW VCO Unlock Detection

1.86 R100 (Offset = 0x64)

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Table 1-88. R100 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	PLL2_RDIV_SEC	R/W	0x5	APLL2 secondary reference divider in cascaded APLL2 mode Divider value ranges from 1-32. Divider value = PLL2_RDIV_SEC + 1. 0x0 = 1 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7 0x7 = 8 0x8 = 9 0x9 = 10 0xA = 11 0xB = 12 0xC = 13 0xD = 14 0xE = 15 0xF = 16 0x10 = 17 0x11 = 18 0x12 = 19 0x13 = 20 0x14 = 21 0x15 = 22 0x16 = 23 0x17 = 24 0x18 = 25 0x19 = 26 0x1A = 27 0x1B = 28 0x1C = 29 0x1D = 30 0x1E = 31 0x1F = 32
2:1	PLL2_RDIV_PRE	R/W	0x0	APLL2 primary reference divider in cascaded APLL2 mode
0	PLL2_PDN	R/W	0x1	PLL2 Power down The PLL2_PDN bit determines whether PLL2 is automatically enabled and calibrated after a hardware reset. 0x0 = PLL2 Enabled 0x1 = PLL2 Disabled

1.87 R101 (Offset = 0x65)

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Table 1-89. R101 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1:0	PLL2_CP	R/W	0x1	PLL2 Charge Pump Gain 0x0 = 1.6 mA 0x1 = 3.2 mA 0x2 = 4.8 mA 0x3 = 6.4 mA

1.88 R102 (Offset = 0x66)

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Table 1-90. R102 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	PLL2_P2	R/W	0x2	PLL2 Post-Divider2 Note: A RESET is required after changing Divider values. See PLL2_P1 for bit settings. 0x0 = Invalid 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7 0x7 = Invalid
3	RESERVED	R	0x0	Reserved
2:0	PLL2_P1	R/W	0x2	PLL2 Post-Divider1 Note: A RESET is required after changing Divider values. 0x0 = Invalid 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7 0x7 = Invalid

1.89 R103 (Offset = 0x67)

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Table 1-91. R103 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PLL2_DISABLE_3RD4TH	R/W	0xF	PLL2 Loop Filter Settings 0x0 = Loop filter input from CP net not shorted to GND [when 0 shorted -- normally 1, test function engineering only] 0x1 = Loop filter output to VCO Vtune net is not shorted to GND 0x2 = 3rd order pole enabled (if 0 cap disabled, r still in place) 0x3 = 4th order pole enabled (if 0 cap disabled, r still in place)

1.90 R104 (Offset = 0x68)

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Table 1-92. R104 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-92. R104 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL2_RBLEED_CP	R/W	0x1F	PLL2 Bleed resistor selection (Ω) 0x0 = Open (no resistance) 0x1 = 23713.2 0x2 = 11875.2 0x3 = 7915.62 0x4 = 5843.79 0x5 = 4753.58 0x6 = 3963.08 0x7 = 3393.52 0x8 = 2970.14 0x9 = 2638.54 0xA = 2375.04 0xB = 2158.91 0xC = 1980.99 0xD = 1827.03 0xE = 1696.76 0xF = 1584.26 0x10 = 1486.55 0x11 = 1397.73 0x12 = 1320.66 0x13 = 1249.6 0x14 = 1187.43 0x15 = 1131.17 0x16 = 1077.88 0x17 = 1033.47 0x18 = 991.03 0x19 = 950.53 0x1A = 913.52 0x1B = 879.47 0x1C = 848.38 0x1D = 818.77 0x1E = 792.13 0x1F = 766.96

1.91 R105 (Offset = 0x69)

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Table 1-93. R105 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved

Table 1-93. R105 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	PLL2_CLSDWAIT	R/W	0x1	Closed Loop Wait Period VCO calibration time per step (up to 7 steps). 0x0 = 300 us, 3600 0x1 = 3 ms, 36000 0x2 = 30 ms, 360000 0x3 = 300 ms, 3600000
1:0	RESERVED	R	0x0	Reserved

1.92 R106 (Offset = 0x6A)

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Table 1-94. R106 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PLL1_NDLYDIV_11:8	R/W	0x0	Bits 11:8 of PLL1_NDLYDIV

1.93 R107 (Offset = 0x6B)

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Table 1-95. R107 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NDLYDIV	R/W	0x64	PLL1 N Delay Divider

1.94 R108 (Offset = 0x6C)

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Table 1-96. R108 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PLL1_NDIV_11:8	R/W	0x0	Bits 11:8 of PLL1_NDIV

1.95 R109 (Offset = 0x6D)

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Table 1-97. R109 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NDIV	R/W	0x34	PLL1 N Divider

1.96 R110 (Offset = 0x6E)

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Table 1-98. R110 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_39:32	R/W	0x14	1. If APLL1 has 40-bit fixed denominator, then this register is APLL1 numerator [39:32]. 2. If APLL1 has 24-bit programmable denominator, then this register is APLL1 numerator [15:8].

1.97 R111 (Offset = 0x6F)

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Table 1-99. R111 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_31:24	R/W	0x0	1. If APLL1 has 40-bit fixed denominator, then this register is APLL1 numerator [31:24]. 2. If APLL1 has 24-bit programmable denominator, then this register is APLL1 numerator [7:0].

1.98 R112 (Offset = 0x70)

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Table 1-100. R112 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_23:16	R/W	0x8	1. If APLL1 has 40-bit fixed denominator, then this register is APLL1 numerator [23:16]. 2. If APLL1 has 24-bit programmable denominator, then this register is APLL1 denominator [23:16].

1.99 R113 (Offset = 0x71)

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Table 1-101. R113 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_15:8	R/W	0xBC	1. If APLL1 has 40-bit fixed denominator, then this register is APLL1 numerator [15:8]. 2. If APLL1 has 24-bit programmable denominator, then this register is APLL1 denominator [15:8].

1.100 R114 (Offset = 0x72)

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Table 1-102. R114 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM	R/W	0xBD	1. If APLL1 has 40-bit fixed denominator, then this register is APLL1 numerator [7:0]. 2. If APLL1 has 24-bit programmable denominator, then this register is APLL1 denominator [7:0].

1.101 R115 (Offset = 0x73)

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Table 1-103. R115 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:3	PLL1_DTHRMODE	R/W	0x0	APLL1 SDM Dither Mode 0x0 = Weak Dither 0x1 = Medium Dither 0x2 = Strong Dither 0x3 = Dither Disabled
2:0	PLL1_ORDER	R/W	0x3	APLL1 SDM Order 0x0 = Integer Mode Divider 0x1 = 1st order 0x2 = 2nd order 0x3 = 3rd order 0x4 = 4th order

1.102 R116 (Offset = 0x74)

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Table 1-104. R116 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved

Table 1-104. R116 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESERVED	R	0x0	Reserved
1	PLL1_FDEV_EN	R/W	0x0	PLL1 Freq Incr/Decr enable via pin or reg control
0	PLL1_MODE	R/W	0x1	PLL1 operational mode 0x0 = Free-run mode (APLL only) 0x1 = DPLL mode

1.103 R117 (Offset = 0x75)

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Table 1-105. R117 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	PLL1_FDEV_37:32	R/W	0x0	Bits 37:32 of PLL1_FDEV

1.104 R118 (Offset = 0x76)

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Table 1-106. R118 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_FDEV_31:24	R/W	0x0	Bits 31:24 of PLL1_FDEV

1.105 R119 (Offset = 0x77)

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Table 1-107. R119 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_FDEV_23:16	R/W	0x0	Bits 23:16 of PLL1_FDEV

1.106 R120 (Offset = 0x78)

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Table 1-108. R120 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_FDEV_15:8	R/W	0x0	Bits 15:8 of PLL1_FDEV

1.107 R121 (Offset = 0x79)

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Table 1-109. R121 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_FDEV	R/W	0x0	PLL1 Freq Incr/Decr Numerator

1.108 R123 (Offset = 0x7B)

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Table 1-110. R123 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_STAT_39:32	R	0x28	Bits 39:32 of PLL1_NUM_STAT

1.109 R124 (Offset = 0x7C)

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Table 1-111. R124 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_STAT_31:24	R	0x0	Bits 31:24 of PLL1_NUM_STAT

1.110 R125 (Offset = 0x7D)

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Table 1-112. R125 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_STAT_23:16	R	0x11	Bits 23:16 of PLL1_NUM_STAT

1.111 R126 (Offset = 0x7E)

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Table 1-113. R126 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_STAT_15:8	R	0x79	Bits 15:8 of PLL1_NUM_STAT

1.112 R127 (Offset = 0x7F)

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Table 1-114. R127 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_STAT	R	0x7A	APLL1 Numerator Status Byte

1.113 R129 (Offset = 0x81)

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Table 1-115. R129 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-115. R129 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL1_LF_R2	R/W	0x1	PLL1 Loop Filter R2 (Ω) 0x0 = 0 0x1 = 414 0x2 = 880 0x3 = 1294 0x4 = 1625 0x5 = 2039 0x6 = 2505 0x7 = 2919 0x8 = 3250 0x9 = 3664 0xA = 4130 0xB = 4544 0xC = 4875 0xD = 5289 0xE = 5755 0xF = 6169 0x10 = 6400 0x11 = 6814 0x12 = 7280 0x13 = 7694 0x14 = 8025 0x15 = 8439 0x16 = 8905 0x17 = 9319 0x18 = 9650 0x19 = 10064 0x1A = 10530 0x1B = 10944 0x1C = 11275 0x1D = 11689 0x1E = 12155 0x1F = 12569 0x20 = 12800 0x21 = 13214 0x22 = 13680 0x23 = 14094 0x24 = 14425 0x25 = 14839 0x26 = 15305 0x27 = 15719 0x28 = 16050 0x29 = 16464 0x2A = 16930 0x2B = 17344 0x2C = 17675 0x2D = 18089 0x2E = 18555 0x2F = 18969

Table 1-115. R129 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x30 = 19200 0x31 = 19614 0x32 = 20080 0x33 = 20494 0x34 = 20825 0x35 = 21239 0x36 = 21705 0x37 = 22119 0x38 = 22450 0x39 = 22864 0x3A = 23330 0x3B = 23744 0x3C = 24075 0x3D = 24489 0x3E = 24955 0x3F = 25369

1.114 R130 (Offset = 0x82)

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Table 1-116. R130 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:0	PLL1_LF_C1	R/W	0x0	PLL1 Loop Filter C1. Not Used, fixed 100pF 0x0 = 100 pF 0x1 = Reserved 1 0x2 = Reserved 2 0x3 = Reserved 3 0x4 = Reserved 4 0x5 = Reserved 5 0x6 = Reserved 6 0x7 = Reserved 7

1.115 R131 (Offset = 0x83)

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Table 1-117. R131 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-117. R131 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL1_LF_R3	R/W	0x1	PLL1 Loop Filter R3 (Ω) 0x0 = 0 0x1 = 200 0x2 = 580 0x3 = 148.7 0x4 = 700 0x5 = 155.6 0x6 = 317.2 0x7 = 122.7 0x8 = 800 0x9 = 1000 0xA = 1380 0xB = 948.7 0xC = 1500 0xD = 955.6 0xE = 1117.2 0xF = 922.7 0x10 = 1600 0x11 = 1800 0x12 = 2180 0x13 = 1748.7 0x14 = 2300 0x15 = 1755.6 0x16 = 1917.2 0x17 = 1722.7 0x18 = 2400 0x19 = 2600 0x1A = 2980 0x1B = 2548.7 0x1C = 3100 0x1D = 2555.6 0x1E = 2717.2 0x1F = 2522.7 0x20 = 3200 0x21 = 3400 0x22 = 3780 0x23 = 3348.7 0x24 = 3900 0x25 = 3355.6 0x26 = 3517.2 0x27 = 3322.7 0x28 = 4000 0x29 = 4200 0x2A = 4580 0x2B = 4148.7 0x2C = 4700 0x2D = 4155.6 0x2E = 4317.2 0x2F = 4122.7

Table 1-117. R131 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x30 = 4800 0x31 = 5000 0x32 = 5380 0x33 = 4948.7 0x34 = 5500 0x35 = 4955.6 0x36 = 5117.2 0x37 = 4922.7 0x38 = 5600 0x39 = 5800 0x3A = 6180 0x3B = 5748.7 0x3C = 6300 0x3D = 5755.6 0x3E = 5917.2 0x3F = 5722.7

1.116 R132 (Offset = 0x84)

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Table 1-118. R132 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-118. R132 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL1_LF_R4	R/W	0x1	PLL1 Loop Filter R4 See PLL1_LF_R3 for bit settings. 0x0 = 0 0x1 = 200 0x2 = 580 0x3 = 148.7 0x4 = 700 0x5 = 155.6 0x6 = 317.2 0x7 = 122.7 0x8 = 800 0x9 = 1000 0xA = 1380 0xB = 948.7 0xC = 1500 0xD = 955.6 0xE = 1117.2 0xF = 922.7 0x10 = 1600 0x11 = 1800 0x12 = 2180 0x13 = 1748.7 0x14 = 2300 0x15 = 1755.6 0x16 = 1917.2 0x17 = 1722.7 0x18 = 2400 0x19 = 2600 0x1A = 2980 0x1B = 2548.7 0x1C = 3100 0x1D = 2555.6 0x1E = 2717.2 0x1F = 2522.7 0x20 = 3200 0x21 = 3400 0x22 = 3780 0x23 = 3348.7 0x24 = 3900 0x25 = 3355.6 0x26 = 3517.2 0x27 = 3322.7 0x28 = 4000 0x29 = 4200 0x2A = 4580 0x2B = 4148.7 0x2C = 4700 0x2D = 4155.6 0x2E = 4317.2

Table 1-118. R132 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 4122.7 0x30 = 4800 0x31 = 5000 0x32 = 5380 0x33 = 4948.7 0x34 = 5500 0x35 = 4955.6 0x36 = 5117.2 0x37 = 4922.7 0x38 = 5600 0x39 = 5800 0x3A = 6180 0x3B = 5748.7 0x3C = 6300 0x3D = 5755.6 0x3E = 5917.2 0x3F = 5722.7

1.117 R133 (Offset = 0x85)

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Table 1-119. R133 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	PLL1_LF_C4	R/W	0x7	PLL1 Loop Filter C4 See PLL1_LF_C3 for bit settings. 0x0 = 0 0x1 = 40 0x2 = 20 0x3 = 60 0x4 = 10 0x5 = 50 0x6 = 30 0x7 = 70
3	RESERVED	R	0x0	Reserved

Table 1-119. R133 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	PLL1_LF_C3	R/W	0x7	PLL1 Loop Filter C3 0x0 = 0 0x1 = 40 0x2 = 20 0x3 = 60 0x4 = 10 0x5 = 50 0x6 = 30 0x7 = 70

1.118 R134 (Offset = 0x86)

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Table 1-120. R134 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL2_NDIV_8:8	R/W	0x0	Bit 8 of PLL2_NDIV

1.119 R135 (Offset = 0x87)

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Table 1-121. R135 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NDIV	R/W	0x2B	Bits 7:0 of PLL2 N Divider

1.120 R136 (Offset = 0x88)

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Table 1-122. R136 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_23:16	R/W	0x0	Bits 23:16 of PLL2_NUM

1.121 R137 (Offset = 0x89)

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Table 1-123. R137 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_15:8	R/W	0x28	Bits 15:8 of PLL2_NUM

1.122 R138 (Offset = 0x8A)

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Table 1-124. R138 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM	R/W	0xE5	PLL2 Fractional Divider Numerator

1.123 R139 (Offset = 0x8B)

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Table 1-125. R139 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:3	PLL2_DTHRMODE	R/W	0x0	SDM Dither Mode 0x0 = Weak Dither 0x1 = Medium Dither 0x2 = Strong Dither 0x3 = Dither Disabled
2:0	PLL2_ORDER	R/W	0x3	APLL2 SDM Order 0x0 = Integer Mode Divider 0x1 = 1st order 0x2 = 2nd order 0x3 = 3rd order 0x4 = 4th order

1.124 R140 (Offset = 0x8C)

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Table 1-126. R140 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-126. R140 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL2_LF_R2	R/W	0x2	PLL2 Loop Filter R2 See PLL1_LF_R2 for bit settings. 0x0 = 0 0x1 = 200 0x2 = 300 0x3 = 120 0x4 = 580 0x5 = 148.7 0x6 = 197.7 0x7 = 99.4 0x8 = 1067 0x9 = 168.4 0xA = 234.2 0xB = 107.9 0xC = 375.7 0xD = 130.5 0xE = 166.8 0xF = 91 0x10 = 800 0x11 = 1000 0x12 = 1100 0x13 = 920 0x14 = 1380 0x15 = 948.7 0x16 = 997.7 0x17 = 899.4 0x18 = 1867 0x19 = 968.4 0x1A = 1034.2 0x1B = 907.9 0x1C = 1175.7 0x1D = 930.5 0x1E = 966.8 0x1F = 891 0x20 = 1600 0x21 = 1800 0x22 = 1900 0x23 = 1720 0x24 = 2180 0x25 = 1748.7 0x26 = 1797.7 0x27 = 1699.4 0x28 = 2667 0x29 = 1768.4 0x2A = 1834.2 0x2B = 1707.9 0x2C = 1975.7 0x2D = 1730.5 0x2E = 1766.8

Table 1-126. R140 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 1691 0x30 = 2400 0x31 = 2600 0x32 = 2700 0x33 = 2520 0x34 = 2980 0x35 = 2548.7 0x36 = 2597.7 0x37 = 2499.4 0x38 = 3467 0x39 = 2568.4 0x3A = 2634.2 0x3B = 2507.9 0x3C = 2775.7 0x3D = 2530.5 0x3E = 2566.8 0x3F = 2491

1.125 R141 (Offset = 0x8D)

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Table 1-127. R141 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:0	PLL2_LF_C1	R/W	0x0	PLL2 Loop Filter C1. Not Used, fixed 100pF 0x0 = 100 pF 0x1 = 100 pF 0x2 = 100 pF 0x3 = 100 pF 0x4 = 100 pF 0x5 = 100 pF 0x6 = 100 pF 0x7 = 100 pF

1.126 R142 (Offset = 0x8E)

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Table 1-128. R142 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-128. R142 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL2_LF_R3	R/W	0x1	PLL2 Loop Filter R3 See PLL1_LF_R3 for bit settings. 0x0 = 0 0x1 = 200 0x2 = 580 0x3 = 148.7 0x4 = 700 0x5 = 155.6 0x6 = 317.2 0x7 = 122.7 0x8 = 800 0x9 = 1000 0xA = 1380 0xB = 948.7 0xC = 1500 0xD = 955.6 0xE = 1117.2 0xF = 922.7 0x10 = 1600 0x11 = 1800 0x12 = 2180 0x13 = 1748.7 0x14 = 2300 0x15 = 1755.6 0x16 = 1917.2 0x17 = 1722.7 0x18 = 2400 0x19 = 2600 0x1A = 2980 0x1B = 2548.7 0x1C = 3100 0x1D = 2555.6 0x1E = 2717.2 0x1F = 2522.7 0x20 = 3200 0x21 = 3400 0x22 = 3780 0x23 = 3348.7 0x24 = 3900 0x25 = 3355.6 0x26 = 3517.2 0x27 = 3322.7 0x28 = 4000 0x29 = 4200 0x2A = 4580 0x2B = 4148.7 0x2C = 4700 0x2D = 4155.6 0x2E = 4317.2

Table 1-128. R142 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 4122.7 0x30 = 4800 0x31 = 5000 0x32 = 5380 0x33 = 4948.7 0x34 = 5500 0x35 = 4955.6 0x36 = 5117.2 0x37 = 4922.7 0x38 = 5600 0x39 = 5800 0x3A = 6180 0x3B = 5748.7 0x3C = 6300 0x3D = 5755.6 0x3E = 5917.2 0x3F = 5722.7

1.127 R143 (Offset = 0x8F)

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Table 1-129. R143 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-129. R143 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL2_LF_R4	R/W	0x1	PLL2 Loop Filter R4 See PLL1_LF_R3 for bit settings. 0x0 = 0 0x1 = 200 0x2 = 580 0x3 = 148.7 0x4 = 700 0x5 = 155.6 0x6 = 317.2 0x7 = 122.7 0x8 = 800 0x9 = 1000 0xA = 1380 0xB = 948.7 0xC = 1500 0xD = 955.6 0xE = 1117.2 0xF = 922.7 0x10 = 1600 0x11 = 1800 0x12 = 2180 0x13 = 1748.7 0x14 = 2300 0x15 = 1755.6 0x16 = 1917.2 0x17 = 1722.7 0x18 = 2400 0x19 = 2600 0x1A = 2980 0x1B = 2548.7 0x1C = 3100 0x1D = 2555.6 0x1E = 2717.2 0x1F = 2522.7 0x20 = 3200 0x21 = 3400 0x22 = 3780 0x23 = 3348.7 0x24 = 3900 0x25 = 3355.6 0x26 = 3517.2 0x27 = 3322.7 0x28 = 4000 0x29 = 4200 0x2A = 4580 0x2B = 4148.7 0x2C = 4700 0x2D = 4155.6 0x2E = 4317.2

Table 1-129. R143 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 4122.7 0x30 = 4800 0x31 = 5000 0x32 = 5380 0x33 = 4948.7 0x34 = 5500 0x35 = 4955.6 0x36 = 5117.2 0x37 = 4922.7 0x38 = 5600 0x39 = 5800 0x3A = 6180 0x3B = 5748.7 0x3C = 6300 0x3D = 5755.6 0x3E = 5917.2 0x3F = 5722.7

1.128 R144 (Offset = 0x90)

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Table 1-130. R144 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	PLL2_LF_C4	R/W	0x7	PLL2 Loop Filter C4 See PLL2_LF_C3 for bit settings. 0x0 = 0 0x1 = 40 0x2 = 20 0x3 = 60 0x4 = 10 0x5 = 50 0x6 = 30 0x7 = 70
3	RESERVED	R	0x0	Reserved

Table 1-130. R144 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	PLL2_LF_C3	R/W	0x7	PLL2 Loop Filter C3 0x0 = 0 0x1 = 40 0x2 = 20 0x3 = 60 0x4 = 10 0x5 = 50 0x6 = 30 0x7 = 70

1.129 R145 (Offset = 0x91)

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Table 1-131. R145 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:3	RESERVED	R	0x0	Reserved
2:0	XO_TIMER	R/W	0x1	XO Input Wait Timer Sets the startup time for the oscillator input. 0x0 = 1.6 ms 0x1 = 3.3 ms 0x2 = 6.6 ms 0x3 = 13.1 ms 0x4 = 26.2 ms 0x5 = 52.4 ms 0x6 = 104.9 ms 0x7 = Reserved - 7

1.130 R155 (Offset = 0x9B)

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Table 1-132. R155 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMSCRC	R	0x32	NVM Stored CRC

1.131 R156 (Offset = 0x9C)

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Table 1-133. R156 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMCNT	R	0x1	NVM Program Count The NVMCNT increments automatically after every EEPROM Erase/Program Cycle (after a subsequent power-cycle or hard reset). The NVMCNT value is retrieved automatically after reset or after a NVM Commit operation.

1.132 R157 (Offset = 0x9D)

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Table 1-134. R157 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	REGCOMMIT	R/WSC	0x0	REG Commit to NVM SRAM Array The REGCOMMIT bit is used to initiate a transfer from the on-chip registers back to the corresponding location in the NVM SRAM Array. The REGCOMMIT bit is automatically cleared to 0 when the transfer is complete.
5	NVMCRCERR	R	0x0	NVM CRC Error Indication This bit will read 1 when a CRC Error has been detected reading back from on-chip EEPROM during device initialization, where the NVMLCRC value does not match NVMSCRC. This bit can only be cleared by successful EEPROM programming and power-on/reset cycle, such that the NVMLCRC value matches NVMSCRC.
4	RESERVED	R	0x0	Reserved
3	NVMCOMMIT	R/WSC	0x0	NVM Commit to Registers The NVMCOMMIT bit is used to initiate a transfer of the on-chip EEPROM contents to internal registers. The transfer happens automatically after reset or when NVMCOMMIT is set to 1. The NVMCOMMIT bit is automatically cleared to 0. The registers cannot be read while a NVM Commit operation is taking place.
2	NVMBUSY	R	0x0	NVM Program Busy Indication This bit will read 1 when an EEPROM Erase/Program cycle is active, during which the EEPROM cannot be accessed.
1:0	RESERVED	R	0x0	Reserved

1.133 R158 (Offset = 0x9E)

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Table 1-135. R158 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMLCRC	R	0x0	NVM Live CRC T his field holds the Live CRC computed from the EEPROM data during device initialization. During initialization, the internal EEPROM controller does a CRC check to compare the Live CRC value with the Stored CRC value written to EEPROM (NVMSCRC byte) in the last NVM program cycle. If the Live and Stored CRC values match (no CRC error), the EEPROM data is valid and the device controller allows normal start-up operation to continue; otherwise, if Live and Stored CRC do not match (CRC error detected), the EEPROM data is considered invalid and the controller halts start-up operation after register load (e.g. PLL lock sequence, etc.). The CRC error status can be read from the NVMCRCERR bit.

1.134 R159 (Offset = 0x9F)

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Table 1-136. R159 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	MEMADR_12:8	R/W	0x0	Bits 12:8 of MEMADR

1.135 R160 (Offset = 0xA0)

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Table 1-137. R160 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	MEMADR	R/W	0xFC	Memory Address The MEMADR value determines the starting address for access to the on-chip memories. NVMDAT register = NVM EEPROM Data Array (Read only) RAMDAT register = NVM SRAM Data Array (Read/Write) ROMDAT register = ROM Data Array (Read only)

1.136 R161 (Offset = 0xA1)

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Table 1-138. R161 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMDAT	R	0x32	EEPROM Read Data

1.137 R162 (Offset = 0xA2)

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Table 1-139. R162 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RAMDAT	R/W	0x0	RAM Read/Write Data

1.138 R164 (Offset = 0xA4)

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Table 1-140. R164 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMUNLK	R/W	0x0	NVM Program Unlock To perform an EEPROM erase and program operation, this register must be written with a value of 0xEA (unlock code) immediately before setting the NVM_ERASE_PROG bits to 0x3 on the next register write.

1.139 R167 (Offset = 0xA7)

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Table 1-141. R167 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL_REFSEL_STAT	R	0x1	0x0 = Holdover 0x1 = PRIREF 0x2 = SECREF 0x3 = Reserved

1.140 R168 (Offset = 0xA8)

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Table 1-142. R168 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	DPLL_PHASE_LOCK	R	0x0	Reads the DPLL phase lock
1	DPLL_LOCK	R	0x0	Reads the DPLL lock control

Table 1-142. R168 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RESERVED	R	0x0	Reserved

1.141 R180 (Offset = 0xB4)

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Table 1-143. R180 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_TUNING_FREE_RUN_37:32	R/W	0x0	Bits 37:32 of DPLL_TUNING_FREE_RUN

1.142 R181 (Offset = 0xB5)

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Table 1-144. R181 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_TUNING_FREE_RUN_31:24	R/W	0x0	Bits 31:24 of DPLL_TUNING_FREE_RUN

1.143 R182 (Offset = 0xB6)

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Table 1-145. R182 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_TUNING_FREE_RUN_23:16	R/W	0x0	Bits 23:16 of DPLL_TUNING_FREE_RUN

1.144 R183 (Offset = 0xB7)

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Table 1-146. R183 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_TUNING_FREE_RUN_15:8	R/W	0x0	Bits 15:8 of DPLL_TUNING_FREE_RUN

1.145 R184 (Offset = 0xB8)

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Table 1-147. R184 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_TUNING_FREE_RUN	R/W	0x0	DPLL Free-run tuning word

1.146 R185 (Offset = 0xB9)

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Table 1-148. R185 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	DPLL_REF_HIST_INTMD	R/W	0x0	Controls intermediate updates to DPLL REF tuning history Updates only occur during first averaging period Tavg after reset. Programming restriction: DPLL_REF_HIST_INTMD ≤ DPLL_REF_HISTCNT. 0x0 = No intermediate update 0x1 = 1 intermediate update at Tavg/2 0x2 = 2 intermediate update at Tavg/4 and Tavg/2 0x3 = 3 intermediate updates at Tavg/8, Tavg/4 and Tavg/2 0xF = 15 intermediate updates at Tavg/32768, Tavg/16384, ... Tavg/4 and Tavg/2. 0x0 = No intermediate update 0x1 = 1 intermediate update at Tavg/2 0x2 = 2 intermediate update at Tavg/4, Tavg/2 0x3 = 3 intermediate updates at Tavg/8, Tavg/4, Tavg/2 0x4 = intermediate updates at Tavg/2^K, K=0 to 4 0x5 = intermediate updates at Tavg/2^K, K=0 to 5 0x6 = intermediate updates at Tavg/2^K, K=0 to 6 0x7 = intermediate updates at Tavg/2^K, K=0 to 7 0x8 = intermediate updates at Tavg/2^K, K=0 to 8 0x9 = intermediate updates at Tavg/2^K, K=0 to 9 0xA = intermediate updates at Tavg/2^K, K=0 to 10 0xB = intermediate updates at Tavg/2^K, K=0 to 11 0xC = intermediate updates at Tavg/2^K, K=0 to 12 0xD = intermediate updates at Tavg/2^K, K=0 to 13 0xE = intermediate updates at Tavg/2^K, K=0 to 14 0xF = intermediate updates at Tavg/2^K, K=0 to 15
3	RESERVED	R	0x0	Reserved
2:1	RESERVED	R	0x0	Reserved
0	DPLL_REF_HIST_EN	R/W	0x1	Enables DPLL REF tuning history monitor

1.147 R186 (Offset = 0xBA)

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Table 1-149. R186 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL_REF_HISTCNT	R/W	0x8	DPLL REF Tuning History Timer Valid range is 0 to 30.

1.148 R187 (Offset = 0xBB)

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Table 1-150. R187 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	DPLL_REF_HISTDLY_30:24	R/W	0x0	Bits 30:24 of DPLL_REF_HISTDLY

1.149 R188 (Offset = 0xBC)

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Table 1-151. R188 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_HISTDLY_23:16	R/W	0x0	Bits 23:16 of DPLL_REF_HISTDLY

1.150 R189 (Offset = 0xBD)

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Table 1-152. R189 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_HISTDLY_15:8	R/W	0x0	Bits 15:8 of DPLL_REF_HISTDLY

1.151 R190 (Offset = 0xBE)

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Table 1-153. R190 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_HISTDLY	R/W	0x2C	DPLL REF Tuning History delay

1.152 R191 (Offset = 0xBF)

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Table 1-154. R191 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	REF_DPLL_DBLR_EN	R/W	0x0	Doubler for VCO1 /8 clock signal frequency for PRIREF/SECREF reference input frequency window detector. (/4 if enabled)
0	REF_DPLL_EN	R/W	0x0	Enables ref path to DPLL TDC

1.153 R192 (Offset = 0xC0)

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Table 1-155. R192 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	DETECT_MODE_SECREF	R/W	0x1	SECREF Input Energy Detector Mode Control Determines the method for Energy Detection on the SECREF Input. See DETECT_MODE_PRIREF for bit settings. 0x0 = Rising Slew Rate Detector 0x1 = Rising and Falling Slew Rate Detector 0x2 = Falling Slew Rate Detector 0x3 = VIH and VIL Level Detector
5:4	DETECT_MODE_PRIREF	R/W	0x1	PRIREF Input Energy Detector Mode Control Determines the method for Energy Detection on the PRIREF Input. 0x0 = Rising Slew Rate Detector 0x1 = Rising and Falling Slew Rate Detector 0x2 = Falling Slew Rate Detector 0x3 = VIH and VIL Level Detector
3:2	SECREF_LVL_SEL	R/W	0x0	SECREF Input Amplitude Detector See PRIREF_LVL_SEL for description and bit settings. 0x0 = Vid = 200 mV Diff or 400 mVpp Single-Ended 0x1 = Vid = 250 mV Diff or 500 mVpp Single-Ended 0x2 = Vid = 300 mV Diff or 600 mVpp Single-Ended 0x3 = Reserved
1:0	PRIREF_LVL_SEL	R/W	0x0	PRIREF Input Amplitude Detector Specifies the minimum differential input peak-to-peak swing to be qualified. 0x0 = Vid = 200 mV Diff or 400 mVpp Single-Ended 0x1 = Vid = 250 mV Diff or 500 mVpp Single-Ended 0x2 = Vid = 300 mV Diff or 600 mVpp Single-Ended 0x3 = Reserved

1.154 R193 (Offset = 0xC1)

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Table 1-156. R193 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	PRIREF_EARLY_DET_EN	R/W	0x1	PRIREF Early Clock Detect Enable
4	PRIREF_PH_VALID_EN	R/W	0x0	PRIREF Phase Valid Detect Enable
3	PRIREF_VALTMR_EN	R/W	0x1	PRIREF Validation Timer Enable
2	PRIREF_PPM_EN	R/W	0x1	PRIREF Frequency ppm Detect Enable
1	PRIREF_MISSCLK_EN	R/W	0x1	PRIREF Missing Clock Detect Enable
0	PRIREF_AMPDET_EN	R/W	0x1	PRIREF Amplitude Detect Enable

1.155 R194 (Offset = 0xC2)

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Table 1-157. R194 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	SECREF_EARLY_DET_EN	R/W	0x1	SECREF Early Clock Detect Enable
4	SECREF_PH_VALID_EN	R/W	0x0	SECREF Phase Valid Detect Enable
3	SECREF_VALTMR_EN	R/W	0x1	SECREF Validation Timer Enable
2	SECREF_PPM_EN	R/W	0x1	SECREF Frequency ppm Detect Enable
1	SECREF_MISSCLK_EN	R/W	0x1	SECREF Missing Clock Detect Enable
0	SECREF_AMPDET_EN	R/W	0x1	SECREF Amplitude Detect Enable

1.156 R195 (Offset = 0xC3)

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Table 1-158. R195 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	PRIREF_MISSCLK_DIV_21:16	R/W	0x0	PRIREF Missing Clock Detection

1.157 R196 (Offset = 0xC4)

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Table 1-159. R196 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_MISSCLK_DIV_15:8	R/W	0x0	PRIREF Missing Clock Detection

1.158 R197 (Offset = 0xC5)

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Table 1-160. R197 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_MISSCLK_DIV	R/W	0x1D	PRIREF Missing Clock Detection

1.159 R198 (Offset = 0xC6)

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Table 1-161. R198 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	SECREF_MISSCLK_DIV_21:16	R/W	0x0	SECREF Missing Clock Detection

1.160 R199 (Offset = 0xC7)

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Table 1-162. R199 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_MISSCLK_DIV_15:8	R/W	0x0	SECREF Missing Clock Detection

1.161 R200 (Offset = 0xC8)

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Table 1-163. R200 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_MISSCLK_DIV	R/W	0x1D	SECREF Missing Clock Detection

1.162 R201 (Offset = 0xC9)

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Table 1-164. R201 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	SECREF_WINDOW_DET_DBLR_EN	R/W	0x0	SECREF Window Detection
0	PRIREF_WINDOW_DET_DBLR_EN	R/W	0x0	PRIREF Window Detection

1.163 R202 (Offset = 0xCA)

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Table 1-165. R202 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	PRIREF_EARLY_CLK_DIV_21:16	R/W	0x0	PRIREF Early Clock Detection

1.164 R203 (Offset = 0xCB)

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Table 1-166. R203 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_EARLY_CLK_DIV_15:8	R/W	0x0	PRIREF Early Clock Detection

1.165 R204 (Offset = 0xCC)

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Table 1-167. R204 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_EARLY_CLK_DIV	R/W	0x15	PRIREF Early Clock Detection

1.166 R205 (Offset = 0xCD)

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Table 1-168. R205 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	SECREF_EARLY_CLK_DIV_21:16	R/W	0x0	SECREF Early Clock Detection

1.167 R206 (Offset = 0xCE)

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Table 1-169. R206 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_EARLY_CLK_DIV_15:8	R/W	0x0	SECREF Early Clock Detection

1.168 R207 (Offset = 0xCF)

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Table 1-170. R207 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_EARLY_CLK_DIV	R/W	0x15	SECREF Early Clock Detection

1.169 R208 (Offset = 0xD0)

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Table 1-171. R208 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	PRIREF_PPM_MIN_14:8	R/W	0x0	PRIREF Frequency Detection

1.170 R209 (Offset = 0xD1)

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Table 1-172. R209 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_PPM_MIN	R/W	0x14	PRIREF Frequency Detection

1.171 R210 (Offset = 0xD2)

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Table 1-173. R210 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	PRIREF_PPM_MAX_14:8	R/W	0x0	PRIREF Frequency Detection

1.172 R211 (Offset = 0xD3)

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Table 1-174. R211 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_PPM_MAX	R/W	0x16	PRIREF Frequency Detection

1.173 R212 (Offset = 0xD4)

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Table 1-175. R212 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	SECREF_PPM_MIN_14:8	R/W	0x0	SECREF Frequency Detection

1.174 R213 (Offset = 0xD5)

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Table 1-176. R213 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_PPM_MIN	R/W	0x14	SECREF Frequency Detection

1.175 R214 (Offset = 0xD6)

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Table 1-177. R214 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	SECREF_PPM_MAX_14:8	R/W	0x0	SECREF Frequency Detection

1.176 R215 (Offset = 0xD7)

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Table 1-178. R215 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_PPM_MAX	R/W	0x16	SECREF Frequency Detection

1.177 R216 (Offset = 0xD8)

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Table 1-179. R216 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:2	SECREF_PPMDIV	R/W	0x3	SECREF Frequency Detection 0x0 = 1 0x1 = 4 0x2 = Reserved 0x3 = 16
1:0	PRIREF_PPMDIV	R/W	0x3	PRIREF Frequency Detection 0x0 = 1 0x1 = 4 0x2 = Reserved 0x3 = 16

1.178 R217 (Offset = 0xD9)

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Table 1-180. R217 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PRIREF_CNTSTRT_27:24	R/W	0x0	PRIREF Frequency Detection

1.179 R218 (Offset = 0xDA)

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Table 1-181. R218 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_CNTSTRT_23:16	R/W	0x0	PRIREF Frequency Detection

1.180 R219 (Offset = 0xDB)

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Table 1-182. R219 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_CNTSTRT_15:8	R/W	0x19	PRIREF Frequency Detection

1.181 R220 (Offset = 0xDC)

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Table 1-183. R220 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_CNTSTRT	R/W	0x6E	PRIREF Frequency Detection

1.182 R221 (Offset = 0xDD)

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Table 1-184. R221 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PRIREF_HOLD_CNTSTRT_27:24	R/W	0x0	PRIREF Frequency Detection

1.183 R222 (Offset = 0xDE)

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Table 1-185. R222 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_HOLD_CNTSTRT_23:16	R/W	0x3	PRIREF Frequency Detection

1.184 R223 (Offset = 0xDF)

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Table 1-186. R223 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_HOLD_CNTSTRT_15:8	R/W	0xD	PRIREF Frequency Detection

1.185 R224 (Offset = 0xE0)

Return to the Summary Table.

Table 1-187. R224 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_HOLD_CNTSTRT	R/W	0x47	PRIREF Frequency Detection

1.186 R225 (Offset = 0xE1)

Return to the Summary Table.

Table 1-188. R225 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SECREF_CNTSTRT_27:24	R/W	0x0	SECREF Frequency Detection

1.187 R226 (Offset = 0xE2)

Return to the Summary Table.

Table 1-189. R226 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_CNTSTRT_23:16	R/W	0x0	SECREF Frequency Detection

1.188 R227 (Offset = 0xE3)

Return to the Summary Table.

Table 1-190. R227 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_CNTSTRT_15:8	R/W	0x19	SECREF Frequency Detection

1.189 R228 (Offset = 0xE4)

Return to the Summary Table.

Table 1-191. R228 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_CNTSTRT	R/W	0x6E	SECREF Frequency Detection

1.190 R229 (Offset = 0xE5)

Return to the Summary Table.

Table 1-192. R229 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SECREF_HOLD_CNTSTRT_27:24	R/W	0x0	SECREF Frequency Detection

1.191 R230 (Offset = 0xE6)

Return to the Summary Table.

Table 1-193. R230 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_HOLD_CNTSTRT_23:16	R/W	0x3	SECREF Frequency Detection

1.192 R231 (Offset = 0xE7)

Return to the Summary Table.

Table 1-194. R231 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_HOLD_CNTSTRT_15:8	R/W	0xD	SECREF Frequency Detection

1.193 R232 (Offset = 0xE8)

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Table 1-195. R232 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_HOLD_CNTSTRT	R/W	0x47	SECREF Frequency Detection

1.194 R233 (Offset = 0xE9)

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Table 1-196. R233 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PRIREFVLDTMR	R/W	0xA	PRIREF Validation Timer Timer = 0.1 ms x $2^{PRIREFVLDTMR}$ 0x0 = 0.1 ms 0x1 = 0.2 ms 0x2 = 0.4 ms 0x3 = 0.8 ms 0x4 = 1.6 ms 0x5 = 3.2 ms 0x6 = 6.4 ms 0x7 = 12.8 ms 0x8 = 25.6 ms 0x9 = 51.2 ms 0xA = 102.4 ms 0xB = 204.8 ms 0xC = 409.6 ms 0xD = 819.2 ms 0xE = 1.6384 s 0xF = 3.2768 s 0x10 = 6.5536 s 0x11 = 13.1072 s 0x12 = 26.2144 s 0x13 = 52.4288 s 0x14 = 104.8576 s 0x15 = 209.7152 s 0x16 = 419.4304 s 0x17 = 838.8608 s 0x18 = 1677.7216 s 0x19 = 3355.4432 s 0x1A = 6710.8864 s 0x1B = 13421.7728 s 0x1C = 26843.5456 s 0x1D = 53687.0912 s 0x1E = 107374.1824 s 0x1F = 214748.3648 s

1.195 R234 (Offset = 0xEA)

Return to the Summary Table.

Table 1-197. R234 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	SECREFVLDTMR	R/W	0xA	SECREF Validation Timer Timer = 0.1 ms x $2^{SECREFVLDTMR}$ 0x0 = 0.1 ms 0x1 = 0.2 ms 0x2 = 0.4 ms 0x3 = 0.8 ms 0x4 = 1.6 ms 0x5 = 3.2 ms 0x6 = 6.4 ms 0x7 = 12.8 ms 0x8 = 25.6 ms 0x9 = 51.2 ms 0xA = 102.4 ms 0xB = 204.8 ms 0xC = 409.6 ms 0xD = 819.2 ms 0xE = 1.6384 s 0xF = 3.2768 s 0x10 = 6.5536 s 0x11 = 13.1072 s 0x12 = 26.2144 s 0x13 = 52.4288 s 0x14 = 104.8576 s 0x15 = 209.7152 s 0x16 = 419.4304 s 0x17 = 838.8608 s 0x18 = 1677.7216 s 0x19 = 3355.4432 s 0x1A = 6710.8864 s 0x1B = 13421.7728 s 0x1C = 26843.5456 s 0x1D = 53687.0912 s 0x1E = 107374.1824 s 0x1F = 214748.3648 s

1.196 R235 (Offset = 0xEB)

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Table 1-198. R235 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	PRIREF_PH_VALID_CNT_30:24	R/W	0x0	PRIREF Phase-valid Detection

1.197 R236 (Offset = 0xEC)

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Table 1-199. R236 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_PH_VALID_CNT_23:16	R/W	0xC3	PRIREF Phase-valid Detection

1.198 R237 (Offset = 0xED)

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Table 1-200. R237 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_PH_VALID_CNT_15:8	R/W	0x50	PRIREF Phase-valid Detection

1.199 R238 (Offset = 0xEE)

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Table 1-201. R238 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_PH_VALID_CNT	R/W	0x0	PRIREF Phase-valid Detection

1.200 R239 (Offset = 0xEF)

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Table 1-202. R239 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	SECREF_PH_VALID_CNT_30:24	R/W	0x0	SECREF Phase-valid Detection

1.201 R240 (Offset = 0xF0)

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Table 1-203. R240 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_PH_VALID_CNT_23:16	R/W	0xC3	SECREF Phase-valid Detection

1.202 R241 (Offset = 0xF1)

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Table 1-204. R241 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_PH_VALID_CNT_15:8	R/W	0x50	SECREF Phase-valid Detection

1.203 R242 (Offset = 0xF2)

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Table 1-205. R242 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_PH_VALID_CNT	R/W	0x0	SECREF Phase-valid Detection

1.204 R243 (Offset = 0xF3)

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Table 1-206. R243 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	PRIREF_PH_VALID_THR	R/W	0x0	PRIREF Phase Valid Threshold

1.205 R244 (Offset = 0xF4)

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Table 1-207. R244 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	SECREF_PH_VALID_THR	R/W	0x0	SECREF Phase Valid Threshold

1.206 R249 (Offset = 0xF9)

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Table 1-208. R249 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	DPLL_SECREF_AUTO_PRTY	R/W	0x2	Set priority for SECREF See DPLL_PRIREF_AUTO_PRTY for bit settings. 0x0 = Not available for selection 0x1 = First priority 0x2 = Second priority 0x3 = Reserved
3:2	RESERVED	R	0x0	Reserved
1:0	DPLL_PRIREF_AUTO_PRTY	R/W	0x1	Set priority for PRIREF 0x0 = Not available for selection 0x1 = First priority 0x2 = Second priority 0x3 = Reserved

1.207 R251 (Offset = 0xFB)

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Table 1-209. R251 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	DPLL_REF_MAN_SEL	R/W	0x0	Controls source of manual selection 0x0 = Manually select by register 0x1 = Manually select by REFSEL pin
4	DPLL_REF_MAN_REG_SEL	R/W	0x0	Controls software manual Ref selection 0x0 = Register select - PRIREF 0x1 = Register select - SECREF
3:2	RESERVED	R	0x0	Reserved
1:0	DPLL_SWITCH_MODE	R/W	0x2	Controls switchover mode 0x0 = Auto non-revertive 0x1 = Auto revertive 0x2 = Manual fallback 0x3 = Manual holdover

1.208 R252 (Offset = 0xFC)

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Table 1-210. R252 Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL_REF_SYNC_OUT7_EN	R/W	0x0	OUT7 SYNC to DPLL REF enable

Table 1-210. R252 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DPLL_REF_SYNC_OUT7_NDIV_RST_DIS	R/W	0x0	DPLL NDIV reset disable when OUT7_REF_SYNC mode is enabled
5	DPLL_SWITCHOVER_ALWAYS	R/W	0x1	DPLL Switchover Timer
4	DPLL_FASTLOCK_ALWAYS	R/W	0x0	Enable DPLL fast lock
3	DPLL_LOCKDET_PPM_EN	R/W	0x1	Reserved
2	DPLL_HLDOVR_MODE	R/W	0x1	DPLL Holdover mode when tuning word history unavailable 0x0 = Enter free-run mode 0x1 = Hold last control value prior to holdover
1	RESERVED	R	0x0	Reserved
0	DPLL_LOOP_EN	R/W	0x1	DPLL Enable

1.209 R256 (Offset = 0x100)

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Table 1-211. R256 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_PRIREF_RDIV_15:8	R/W	0x0	Bits 15:8 of DPLL_PRIREF_RDIV

1.210 R257 (Offset = 0x101)

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Table 1-212. R257 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_PRIREF_RDIV	R/W	0x1	DPLL PRIREF divider control

1.211 R258 (Offset = 0x102)

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Table 1-213. R258 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_SECREF_RDIV_15:8	R/W	0x0	Bits 15:8 of DPLL_SECREF_RDIV

1.212 R259 (Offset = 0x103)

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Table 1-214. R259 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_SECREF_RDIV	R/W	0x1	DPLL SECREF divider control

1.213 R286 (Offset = 0x11E)

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Table 1-215. R286 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL_REF_TMR_FL1_9:8	R/W	0x2	DPLL Loop Filter

1.214 R287 (Offset = 0x11F)

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Table 1-216. R287 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_TMR_FL1	R/W	0x30	DPLL Loop Filter

1.215 R288 (Offset = 0x120)

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Table 1-217. R288 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL_REF_TMR_FL2_9:8	R/W	0x0	DPLL Loop Filter

1.216 R289 (Offset = 0x121)

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Table 1-218. R289 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_TMR_FL2	R/W	0xEE	DPLL Loop Filter

1.217 R290 (Offset = 0x122)

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Table 1-219. R290 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL_REF_TMR_LCK_9:8	R/W	0x2	DPLL Phase Lock Detection

1.218 R291 (Offset = 0x123)

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Table 1-220. R291 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_TMR_LCK	R/W	0xCA	DPLL Phase Lock Detection

1.219 R301 (Offset = 0x12D)

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Table 1-221. R301 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_PL_LOCK_THRESH	R/W	0x1C	Phase lock declaration threshold

1.220 R302 (Offset = 0x12E)

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Table 1-222. R302 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_PL_UNLK_THRESH	R/W	0x20	Phase un-lock declaration threshold

1.221 R304 (Offset = 0x130)

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Table 1-223. R304 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	DPLL_REF_FB_PRE_DIV	R/W	0x1	DPLL REF Feedback Pre Divider value Divider value ranges from 2 to 17. Divider value = DPLL_REF_FB_PRE_DIV + 2. 0x0 = 2 0x1 = 3 0x2 = 4 0x3 = 5 0x4 = 6 0x5 = 7 0x6 = 8 0x7 = 9 0x8 = 10 0x9 = 11 0xA = 12 0xB = 13 0xC = 14 0xD = 15 0xE = 16 0xF = 17

1.222 R305 (Offset = 0x131)

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Table 1-224. R305 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_REF_FB_DIV_29:24	R/W	0x0	Bits 29:24 of DPLL_REF_FB_DIV

1.223 R306 (Offset = 0x132)

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Table 1-225. R306 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_FB_DIV_23:16	R/W	0x0	Bits 23:16 of DPLL_REF_FB_DIV

1.224 R307 (Offset = 0x133)

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Table 1-226. R307 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_FB_DIV_15:8	R/W	0x0	Bits 15:8 of DPLL_REF_FB_DIV

1.225 R308 (Offset = 0x134)

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Table 1-227. R308 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_FB_DIV	R/W	0x10	DPLL REF Feedback Divider value

1.226 R309 (Offset = 0x135)

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Table 1-228. R309 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_NUM_39:32	R/W	0xAA	Bits 39:32 of DPLL_REF_NUM

1.227 R310 (Offset = 0x136)

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Table 1-229. R310 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_NUM_31:24	R/W	0xAA	Bits 31:24 of DPLL_REF_NUM

1.228 R311 (Offset = 0x137)

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Table 1-230. R311 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_NUM_23:16	R/W	0xAA	Bits 23:16 of DPLL_REF_NUM

1.229 R312 (Offset = 0x138)

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Table 1-231. R312 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_NUM_15:8	R/W	0xAA	Bits 15:8 of DPLL_REF_NUM

1.230 R313 (Offset = 0x139)

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Table 1-232. R313 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_NUM	R/W	0xAA	DPLL REF FB Divider Numerator

1.231 R314 (Offset = 0x13A)

Return to the Summary Table.

Table 1-233. R314 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_DEN_39:32	R/W	0xFF	Bits 39:32 of DPLL_REF_DEN

1.232 R315 (Offset = 0x13B)

Return to the Summary Table.

Table 1-234. R315 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_DEN_31:24	R/W	0xFF	Bits 31:24 of DPLL_REF_DEN

1.233 R316 (Offset = 0x13C)

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Table 1-235. R316 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_DEN_23:16	R/W	0xFF	Bits 23:16 of DPLL_REF_DEN

1.234 R317 (Offset = 0x13D)

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Table 1-236. R317 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_DEN_15:8	R/W	0xFF	Bits 15:8 of DPLL_REF_DEN

1.235 R318 (Offset = 0x13E)

Return to the Summary Table.

Table 1-237. R318 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_DEN	R/W	0xFF	DPLL REF FB Divider denominator

1.236 R320 (Offset = 0x140)

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Table 1-238. R320 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	DPLL_REF_LOCKDET_PPM_MAX_14:8	R/W	0x0	DPLL DCO Lock Detection

1.237 R321 (Offset = 0x141)

Return to the Summary Table.

Table 1-239. R321 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_LOCKDET_PPM_MAX	R/W	0xA	DPLL DCO Lock Detection

1.238 R322 (Offset = 0x142)

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Table 1-240. R322 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-240. R322 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	DPLL_REF_LOCKDET_CNTSTRT_29:24	R/W	0x0	DPLL DCO Lock Detection

1.239 R323 (Offset = 0x143)

Return to the Summary Table.

Table 1-241. R323 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_LOCKDET_CNTSTRT_23:16	R/W	0x24	DPLL DCO Lock Detection

1.240 R324 (Offset = 0x144)

Return to the Summary Table.

Table 1-242. R324 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_LOCKDET_CNTSTRT_15:8	R/W	0x9F	DPLL DCO Lock Detection

1.241 R325 (Offset = 0x145)

Return to the Summary Table.

Table 1-243. R325 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_LOCKDET_CNTSTRT	R/W	0x0	DPLL DCO Lock Detection

1.242 R326 (Offset = 0x146)

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Table 1-244. R326 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_REF_LOCKDET_VCO_CNTSTRT_29:24	R/W	0x0	DPLL DCO Lock Detection

1.243 R327 (Offset = 0x147)

Return to the Summary Table.

Table 1-245. R327 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_LOCKDET_VCO_CNTSTRT_23:16	R/W	0x98	DPLL DCO Lock Detection

1.244 R328 (Offset = 0x148)

Return to the Summary Table.

Table 1-246. R328 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_LOCKDET_VCO_CNTSTRT_15:8	R/W	0x96	DPLL DCO Lock Detection

1.245 R329 (Offset = 0x149)

Return to the Summary Table.

Table 1-247. R329 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_LOCKDET_VCO_CNTSTRT	R/W	0x80	DPLL DCO Lock Detection

1.246 R330 (Offset = 0x14A)

Return to the Summary Table.

Table 1-248. R330 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	DPLL_REF_UNLOCKDET_PPM_MAX_14:8	R/W	0x0	DPLL DCO Unlock Detection

1.247 R331 (Offset = 0x14B)

Return to the Summary Table.

Table 1-249. R331 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_UNLOCKDET_PPM_MAX	R/W	0x64	DPLL DCO Unlock Detection

1.248 R332 (Offset = 0x14C)

Return to the Summary Table.

Table 1-250. R332 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_REF_UNLOCKDET_CNTSTRT_29_24	R/W	0x0	DPLL DCO Unlock Detection

1.249 R333 (Offset = 0x14D)

Return to the Summary Table.

Table 1-251. R333 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_DEN_23:16	R/W	0x0	APLL2 denominator [23:16]

1.250 R334 (Offset = 0x14E)

Return to the Summary Table.

Table 1-252. R334 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_DEN_15:8	R/W	0x3D	APLL2 denominator [15:8]

1.251 R335 (Offset = 0x14F)

Return to the Summary Table.

Table 1-253. R335 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_DEN	R/W	0x9	APLL2 denominator [7:0]

1.252 R336 (Offset = 0x150)

Return to the Summary Table.

Table 1-254. R336 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_REF_UNLOCKDET_VCO_CNTSTRT_29_24	R/W	0x0	DPLL DCO Unlock Detection

1.253 R337 (Offset = 0x151)

Return to the Summary Table.

Table 1-255. R337 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_UNLOCKDET_VCO_CNTSTRT_23_16	R/W	0x98	DPLL DCO Unlock Detection

1.254 R338 (Offset = 0x152)

Return to the Summary Table.

Table 1-256. R338 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_UNLOCKDET_VCO_CNTSTRT_15_8	R/W	0x96	DPLL DCO Unlock Detection

1.255 R339 (Offset = 0x153)

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Table 1-257. R339 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_24b_NUM_MSB	R/W	0x0	PLL1 24-bit programmable numerator

1.256 R340 (Offset = 0x154)

Return to the Summary Table.

Table 1-258. R340 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL_REF_SYNC_PH_OFFSET_44:40	R/W	0x0	Bits 44:40 of DPLL_REF_SYNC_PH_OFFSET

1.257 R341 (Offset = 0x155)

Return to the Summary Table.

Table 1-259. R341 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_SYNC_PH_OFFSET_39:32	R/W	0x0	Bits 39:32 of DPLL_REF_SYNC_PH_OFFSET

1.258 R342 (Offset = 0x156)

Return to the Summary Table.

Table 1-260. R342 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_SYNC_PH_OFFSET_31:24	R/W	0x0	Bits 31:24 of DPLL_REF_SYNC_PH_OFFSET

1.259 R343 (Offset = 0x157)

Return to the Summary Table.

Table 1-261. R343 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_SYNC_PH_OFFSET_23:16	R/W	0x0	Bits 23:16 of DPLL_REF_SYNC_PH_OFFSET

1.260 R344 (Offset = 0x158)

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Table 1-262. R344 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_SYNC_PH_OFFSET_15:8	R/W	0x0	Bits 15:8 of DPLL_REF_SYNC_PH_OFFSET

1.261 R345 (Offset = 0x159)

Return to the Summary Table.

Table 1-263. R345 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_SYNC_PH_OFFSET	R/W	0x0	DPLL REF Zero Delay Mode Phase Offset

1.262 R346 (Offset = 0x15A)

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Table 1-264. R346 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	DPLL_FDEV_EN	R/W	0x0	DPLL Freq Incr/Decr enable via pin or reg control

1.263 R347 (Offset = 0x15B)

Return to the Summary Table.

Table 1-265. R347 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_FDEV_37:32	R/W	0x0	Bits 37:32 of DPLL_FDEV

1.264 R348 (Offset = 0x15C)

Return to the Summary Table.

Table 1-266. R348 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_FDEV_31:24	R/W	0x0	Bits 31:24 of DPLL_FDEV

1.265 R349 (Offset = 0x15D)

Return to the Summary Table.

Table 1-267. R349 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_FDEV_23:16	R/W	0x0	Bits 23:16 of DPLL_FDEV

1.266 R350 (Offset = 0x15E)

Return to the Summary Table.

Table 1-268. R350 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_FDEV_15:8	R/W	0x0	Bits 15:8 of DPLL_FDEV

1.267 R351 (Offset = 0x15F)

Return to the Summary Table.

Table 1-269. R351 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_FDEV	R/W	0x0	DPLL Freq Incr/Decr Numerator Step Word This step word is computed based on the desired DCO frequecy step size in ppb (parts-per-billion).

1.268 R357 (Offset = 0x165)

Return to the Summary Table.

Table 1-270. R357 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	PLL1_VM_INSIDE	R	0x1	PLL1 VCO Status Denotes if the PLL1 charge pump voltage is within operational range.
4:0	RESERVED	R	0x0	Reserved

1.269 R367 (Offset = 0x16F)

Return to the Summary Table.

Table 1-271. R367 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	PLL2_VM_INSIDE	R	0x0	PLL2 VCO Status Denotes if the PLL2 charge pump voltage is within operational range.
4:0	RESERVED	R	0x0	Reserved

1.270 R411 (Offset = 0x19B)

Return to the Summary Table.

Table 1-272. R411 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	SECREF_VALSTAT	R	0x1	SECREF valid state
2	PRIREF_VALSTAT	R	0x1	PRIREF valid state
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from September 30, 2025 to November 30, 2025 (from Revision D (September 2025) to Revision E (November 2025)) **Page**

- Updated Device Registers section..... 2

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