Programmer's Guide

LMK5C33216 Programming Guide

ABSTRACT

Reset values in register tables are provided for EE_ROM_PAGE_SEL = 0 with GPIO0 = L and GPIO2 = L on start-up. EE_ROM_PAGE_SEL factory default is 0.

Trademarks

1 Device Registers

Table 1-1 lists the Device registers. All register offset addresses not listed in Table 1-1 should be considered as reserved locations and the register contents should not be modified.

Table 1-1. Device Registers

Offset	Acronym	Register Name	Section
0x0	R0	VNDRID_BY1	Go
0x1	R1	VNDRID_BY0	Go
0x2	R2	PRODID	Go
0x3	R3	REVID	Go
0x10	R16	NVMCNT	Go
0x12	R18	SLAVEADR	Go
0x13	R19	EEREV	Go
0x14	R20	EE_ROM_PAGE	Go
0x15	R21	DEV_CTL1	Go
0x16	R22	DEV_CTL2	Go
0x17	R23	SWRST	Go
0x18	R24	STRT_PRTY	Go
0x19	R25	SYNC_CTL	Go
0x1A	R26	SYSREF_REQ_CTL	Go
0x1B	R27	TOD_BY4	Go
0x1C	R28	TOD_BY3	Go
0x1D	R29	TOD_BY2	Go
0x1E	R30	TOD_BY1	Go
0x1F	R31	TOD_BY0	Go
0x20	R32	TOD_CTRL	Go
0x21	R33	INT_LIVE0	Go
0x22	R34	INT_LIVE1	Go
0x23	R35	INT_LIVE2	Go
0x24	R36	INT_LIVE3	Go
0x25	R37	INT_MASK0	Go
0x26	R38	INT_MASK1	Go
0x27	R39	INT_MASK2	Go
0x28	R40	INT_MASK3	Go
0x29	R41	INT_FLAG_POL0	Go
0x2A	R42	INT_FLAG_POL1	Go
0x2B	R43	INT_FLAG_POL2	Go
0x2C	R44	INT_FLAG_POL3	Go
0x2D	R45	INT_FLAG0	Go
0x2E	R46	INT_FLAG1	Go
0x2F	R47	INT_FLAG2	Go
0x30	R48	INT_FLAG3	Go
0x31	R49	INT_CTL	Go
0x32	R50	REFIN_STAT	Go
0x34	R52	REFIN_STAT3	Go
0x35	R53	OPCTRL_STAT	Go
0x36	R54	GPIO0_CONFIG	Go
0x37	R55	GPIO1_CONFIG	Go
0x38	R56	GPIO2_CONFIG	Go

Table 1-1. Device Registers (continued)

Offset	Acronym	Register Name	Section
0x39	R57	GPIO0_SEL	Go
0x3A	R58	GPIO1_SEL	Go
0x3B	R59	GPIO2_SEL	Go
0x3C	R60	GPIO_OUT_CTL	Go
0x3D	R61	DPLL_MUTE	Go
0x3E	R62	DPLL_MUTE	Go
0x3F	R63	XO_CLKCTL	Go
0x40	R64	XO_OUT_SEL	Go
0x43	R67	REF1_CTL	Go
0x44	R68	REF0_CTL	Go
0x45	R69	OUT0_1_CMV	Go
0x46	R70	OUT2_3_CMV	Go
0x47	R71	OUT4_7_CMV	Go
0x48	R72	OUT8_13_CMV	Go
0x49	R73	OUT8_13_CMV	Go
0x4A	R74	OUT14_15_CMV	Go
0x4B	R75	TDC3_ZDLY	Go
0x4C	R76	TDC2_ZDLY	Go
0x4D	R77	TDC1_ZDLY	Go
0x4E	R78	REF_OUT_SEL	Go
0x4F	R79	REF0_DETEN	Go
0x50	R80	REF1_DETEN	Go
0x53	R83	REF0_3_CLK_DIV	Go
0x54	R84	REF0_MISSCLK_DIV_BY2	Go
0x55	R85	REF0_MISSCLK_DIV_BY1	Go
0x56	R86	REF0_MISSCLK_DIV_BY0	Go
0x57	R87	REF1_MISSCLK_DIV_BY2	Go
0x58	R88	REF1_MISSCLK_DIV_BY1	Go
0x59	R89	REF1_MISSCLK_DIV_BY0	Go
0x60	R96	REF_MISSCLK_CTL	Go
0x61	R97	REF0_EARLY_CLK_DIV_BY2	Go
0x62	R98	REF0_EARLY_CLK_DIV_BY1	Go
0x63	R99	REF0_EARLY_CLK_DIV_BY0	Go
0x64	R100	REF1_EARLY_CLK_DIV_BY2	Go
0x65	R101	REF1_EARLY_CLK_DIV_BY1	Go
0x66	R102	REF1_EARLY_CLK_DIV_BY0	Go
0x6D	R109	REF0_PPM_MIN_BY1	Go
0x6E	R110	REF0_PPM_MIN_BY0	Go
0x6F	R111	REF0_PPM_MAX_BY1	Go
0x70	R112	REF0_PPM_MAX_BY0	Go
0x71	R113	REF1_PPM_MIN_BY1	Go
0x72	R114	REF1_PPM_MIN_BY0	Go
0x73	R115	REF1_PPM_MAX_BY1	Go
0x74	R116	REF1_PPM_MAX_BY0	Go
0x9D	R157	REF0_VLDTMR	Go
0x9E	R158	REF1_VLDTMR	Go
0xA1	R161	REF0_PH_VALID_THR_BY1	Go

Table 1-1. Device Registers (continued)

Offset	Acronym	Register Name	Section
0xA2	R162	REF0_PH_VALID_THR_BY0	Go
0xA3	R163	REF1_PH_VALID_THR_BY1	Go
0xA4	R164	REF1_PH_VALID_THR_BY0	Go
0xAA	R170	NVMSCRC	Go
0xAB	R171	NVMCTL	Go
0xAD	R173	MEMADR_BY1	Go
0xAE	R174	MEMADR_BY0	Go
0xB0	R176	RAMDAT	Go
0xB4	R180	NVMUNLK	Go
0xDE	R222	DFT_CTL	Go
0xDF	R223	DPLL1_REF1	Go
0xE1	R225	DPLL1_REF3	Go
0xE2	R226	DPLL1_REF4	Go
0xE3	R227	DPLL1_REFSEL_STAT	Go
0xE4	R228	DPLL1_FDET_LCK_BY1	Go
0xE5	R229	DPLL1_FDET_LCK_BY0	Go
0xE6	R230	DPLL1_FDET_UNLCK_BY1	Go
0xE7	R231	DPLL1_FDET_UNLCK_BY0	Go
0xE8	R232	DPLL1_FDET2_CNTSTRT_BY3	Go
0xE9	R233	DPLL1_FDET2_CNTSTRT_BY2	Go
0xEA	R234	DPLL1_FDET2_CNTSTRT_BY1	Go
0xEB	R235	DPLL1_FDET2_CNTSTRT_BY0	Go
0xEC	R236	DPLL1_FDET_CNTSTRT_BY3	Go
0xED	R237	DPLL1_FDET_CNTSTRT_BY2	Go
0xEE	R238	DPLL1_FDET_CNTSTRT_BY1	Go
0xEF	R239	DPLL1_FDET_CNTSTRT_BY0	Go
0xF0	R240	DPLL1_FDET_VCO_CNTSTRT_BY3	Go
0xF1	R241	DPLL1_FDET_VCO_CNTSTRT_BY2	Go
0xF2	R242	DPLL1_FDET_VCO_CNTSTRT_BY1	Go
0xF3	R243	DPLL1_FDET_VCO_CNTSTRT_BY0	Go
0xF4	R244	DPLL1_FDET_STATUS	Go
0xF7	R247	DPLL1_CTRL1	Go
0xF8	R248	DPLL1_SCLR_BY1	Go
0xFA	R250	DPLL1_PHOFF_BY5	Go
0xFB	R251	DPLL1_PHOFF_BY4	Go
0xFC	R252	DPLL1_PHOFF_BY3	Go
0xFD	R253	DPLL1_PHOFF_BY2	Go
0xFE	R254	DPLL1_PHOFF_BY1	Go
0xFF	R255	DPLL1_PHOFF_BY0	Go
0x100	R256	DPLL1_FREERUN_BY4	Go
0x101	R257	DPLL1_FREERUN_BY3	Go
0x102	R258	DPLL1_FREERUN_BY2	Go
0x103	R259	DPLL1_FREERUN_BY1	Go
0x104	R260	DPLL1_FREERUN_BY0	Go
0x122	R290	DPLL1_LCKTMR_BY1	Go
0x123	R291	DPLL1_LCKTMR_BY0	Go
0x126	R294	DPLL1_HOLDTMR_BY1	Go

Table 1-1. Device Registers (continued)

Offset	Acronym	Register Name	Section
0x127	R295	DPLL1_HOLDTMR_BY0	Go
0x128	R296	DPLL1_PHS1TMR_BY1	Go
0x129	R297	DPLL1_PHS1TMR_BY0	Go
0x12F	R303	DPLL1_PLLK	Go
0x130	R304	DPLL1_PLUNLK	Go
0x131	R305	DPLL1_PHS1LIM	Go
0x134	R308	DPLL1_HOLDLIM	Go
0x136	R310	DPLL1_DBG2	Go
0x137	R311	DPLL1_DBG3	Go
0x13A	R314	DPLL1_FBDIV_BY4	Go
0x13B	R315	DPLL1_FBDIV_BY3	Go
0x13C	R316	DPLL1_FBDIV_BY2	Go
0x13D	R317	DPLL1_FBDIV_BY1	Go
0x13E	R318	DPLL1_FBDIV_BY0	Go
0x13F	R319	DPLL1_FBNUM_BY4	Go
0x140	R320	DPLL1_FBNUM_BY3	Go
0x141	R321	DPLL1_FBNUM_BY2	Go
0x142	R322	DPLL1_FBNUM_BY1	Go
0x143	R323	DPLL1_FBNUM_BY0	Go
0x144	R324	DPLL1_FBDEN_BY4	Go
0x145	R325	DPLL1_FBDEN_BY3	Go
0x146	R326	DPLL1_FBDEN_BY2	Go
0x147	R327	DPLL1_FBDEN_BY1	Go
0x148	R328	DPLL1_FBDEN_BY0	Go
0x149	R329	DPLL1_FBDIV2_BY4	Go
0x14A	R330	DPLL1_FBDIV2_BY3	Go
0x14B	R331	DPLL1_FBDIV2_BY2	Go
0x14C	R332	DPLL1_FBDIV2_BY1	Go
0x14D	R333	DPLL1_FBDIV2_BY0	Go
0x14E	R334	DPLL1_FBNUM2_BY4	Go
0x14F	R335	DPLL1_FBNUM2_BY3	Go
0x150	R336	DPLL1_FBNUM2_BY2	Go
0x151	R337	DPLL1_FBNUM2_BY1	Go
0x152	R338	DPLL1_FBNUM2_BY0	Go
0x153	R339	DPLL1_FBDEN2_BY4	Go
0x154	R340	DPLL1_FBDEN2_BY3	Go
0x155	R341	DPLL1_FBDEN2_BY2	Go
0x156	R342	DPLL1_FBDEN2_BY1	Go
0x157	R343	DPLL1_FBDEN2_BY0	Go
0x158	R344	DPLL1_FBDIV_SEL	Go
0x159	R345	DPLL1_FBMASHCTL	Go
0x15A	R346	DPLL1_FBFDEV_BY4	Go
0x15B	R347	DPLL1_FBFDEV_BY3	Go
0x15C	R348	DPLL1_FBFDEV_BY2	Go
0x15D	R349	DPLL1_FBFDEV_BY1	Go
0x15E	R350	DPLL1_FBFDEV_BY0	Go
0x15F	R351	DPLL1_FBFDEVUPDATE	Go

Table 1-1. Device Registers (continued)

Offset	Acronym	Register Name	Section
0x160	R352	DPLL1_FBFDEVEN	Go
0x161	R353	DPLL1_FBNUM_STAT_BY4	Go
0x162	R354	DPLL1_FBNUM_STAT_BY3	Go
0x163	R355	DPLL1_FBNUM_STAT_BY2	Go
0x164	R356	DPLL1_FBNUM_STAT_BY1	Go
0x165	R357	DPLL1_FBNUM_STAT_BY0	Go
0x166	R358	DPLL1_REF_DBLR	Go
0x167	R359	DPLL1_REF0RDIV1	Go
0x168	R360	DPLL1_REF0RDIV2	Go
0x169	R361	DPLL1_REF1RDIV1	Go
0x16A	R362	DPLL1_REF1RDIV2	Go
0x171	R369	DPLL1_REF5RDIV1	Go
0x172	R370	DPLL1_REF5RDIV2	Go
0x175	R373	DPLL2_REF1	Go
0x177	R375	DPLL2_REF3	Go
0x178	R376	DPLL2_REF4	Go
0x179	R377	DPLL2_REFSEL_STAT	Go
0x17A	R378	DPLL2_FDET_LCK_BY1	Go
0x17B	R379	DPLL2_FDET_LCK_BY0	Go
0x17C	R380	DPLL2_FDET_UNLCK_BY1	Go
0x17D	R381	DPLL2_FDET_UNLCK_BY0	Go
0x17E	R382	DPLL2_FDET2_CNTSTRT_BY3	Go
0x17F	R383	DPLL2_FDET2_CNTSTRT_BY2	Go
0x180	R384	DPLL2_FDET2_CNTSTRT_BY1	Go
0x181	R385	DPLL2_FDET2_CNTSTRT_BY0	Go
0x182	R386	DPLL2_FDET_CNTSTRT_BY3	Go
0x183	R387	DPLL2_FDET_CNTSTRT_BY2	Go
0x184	R388	DPLL2_FDET_CNTSTRT_BY1	Go
0x185	R389	DPLL2_FDET_CNTSTRT_BY0	Go
0x186	R390	DPLL2_FDET_VCO_CNTSTRT_BY3	Go
0x187	R391	DPLL2_FDET_VCO_CNTSTRT_BY2	Go
0x188	R392	DPLL2_FDET_VCO_CNTSTRT_BY1	Go
0x189	R393	DPLL2_FDET_VCO_CNTSTRT_BY0	Go
0x18A	R394	DPLL2_FDET_STATUS	Go
0x18D	R397	DPLL2_CTRL1	Go
0x18E	R398	DPLL2_SCLR_BY1	Go
0x190	R400	DPLL2_PHOFF_BY5	Go
0x191	R401	DPLL2_PHOFF_BY4	Go
0x192	R402	DPLL2_PHOFF_BY3	Go
0x193	R403	DPLL2_PHOFF_BY2	Go
0x194	R404	DPLL2_PHOFF_BY1	Go
0x195	R405	DPLL2_PHOFF_BY0	Go
0x196	R406	DPLL2_FREERUN_BY4	Go
0x197	R407	DPLL2_FREERUN_BY3	Go
0x198	R408	DPLL2_FREERUN_BY2	Go
0x199	R409	DPLL2_FREERUN_BY1	Go
0x19A	R410	DPLL2_FREERUN_BY0	Go

Table 1-1. Device Registers (continued)

Offset	Acronym	Register Name	Section
0x1B8	R440	DPLL2_LCKTMR_BY1	Go
0x1B9	R441	DPLL2_LCKTMR_BY0	Go
0x1BC	R444	DPLL2_HOLDTMR_BY1	Go
0x1BD	R445	DPLL2_HOLDTMR_BY0	Go
0x1BE	R446	DPLL2_PHS1TMR_BY1	Go
0x1BF	R447	DPLL2_PHS1TMR_BY0	Go
0x1C5	R453	DPLL2_PLLK	Go
0x1C6	R454	DPLL2_PLUNLK	Go
0x1C7	R455	DPLL2_PHS1LIM	Go
0x1CA	R458	DPLL2_HOLDLIM	Go
0x1CC	R460	DPLL2_DBG2	Go
0x1CD	R461	DPLL2_DBG3	Go
0x1D0	R464	DPLL2_FBDIV_BY4	Go
0x1D1	R465	DPLL2_FBDIV_BY3	Go
0x1D2	R466	DPLL2_FBDIV_BY2	Go
0x1D3	R467	DPLL2_FBDIV_BY1	Go
0x1D4	R468	DPLL2_FBDIV_BY0	Go
0x1D5	R469	DPLL2_FBNUM_BY4	Go
0x1D6	R470	DPLL2_FBNUM_BY3	Go
0x1D7	R471	DPLL2_FBNUM_BY2	Go
0x1D8	R472	DPLL2_FBNUM_BY1	Go
0x1D9	R473	DPLL2_FBNUM_BY0	Go
0x1DA	R474	DPLL2_FBDEN_BY4	Go
0x1DB	R475	DPLL2_FBDEN_BY3	Go
0x1DC	R476	DPLL2_FBDEN_BY2	Go
0x1DD	R477	DPLL2_FBDEN_BY1	Go
0x1DE	R478	DPLL2_FBDEN_BY0	Go
0x1DF	R479	DPLL2_FBDIV2_BY4	Go
0x1E0	R480	DPLL2_FBDIV2_BY3	Go
0x1E1	R481	DPLL2_FBDIV2_BY2	Go
0x1E2	R482	DPLL2_FBDIV2_BY1	Go
0x1E3	R483	DPLL2_FBDIV2_BY0	Go
0x1E4	R484	DPLL2_FBNUM2_BY4	Go
0x1E5	R485	DPLL2_FBNUM2_BY3	Go
0x1E6	R486	DPLL2_FBNUM2_BY2	Go
0x1E7	R487	DPLL2_FBNUM2_BY1	Go
0x1E8	R488	DPLL2_FBNUM2_BY0	Go
0x1E9	R489	DPLL2_FBDEN2_BY4	Go
0x1EA	R490	DPLL2_FBDEN2_BY3	Go
0x1EB	R491	DPLL2_FBDEN2_BY2	Go
0x1EC	R492	DPLL2_FBDEN2_BY1	Go
0x1ED	R493	DPLL2_FBDEN2_BY0	Go
0x1EE	R494	DPLL2_FBDIV_SEL	Go
0x1EF	R495	DPLL2_FBMASHCTL	Go
0x1F0	R496	DPLL2_FBFDEV_BY4	Go
0x1F1	R497	DPLL2_FBFDEV_BY3	Go
0x1F2	R498	DPLL2_FBFDEV_BY2	Go

Table 1-1. Device Registers (continued)

Offset	Acronym	Register Name	Section
0x1F3	R499	DPLL2_FBFDEV_BY1	Go
0x1F4	R500	DPLL2_FBFDEV_BY0	Go
0x1F5	R501	DPLL2_FBFDEVUPDATE	Go
0x1F6	R502	DPLL2_FBFDEVEN	Go
0x1F7	R503	DPLL2_FBNUM_STAT_BY4	Go
0x1F8	R504	DPLL2_FBNUM_STAT_BY3	Go
0x1F9	R505	DPLL2_FBNUM_STAT_BY2	Go
0x1FA	R506	DPLL2_FBNUM_STAT_BY1	Go
0x1FB	R507	DPLL2_FBNUM_STAT_BY0	Go
0x1FC	R508	DPLL2_REF_DBLR	Go
0x1FD	R509	DPLL2_REF0RDIV1	Go
0x1FE	R510	DPLL2_REF0RDIV2	Go
0x1FF	R511	DPLL2_REF1RDIV1	Go
0x200	R512	DPLL2_REF1RDIV2	Go
0x205	R517	DPLL2_REF4RDIV1	Go
0x206	R518	DPLL2_REF4RDIV2	Go
0x207	R519	DPLL2_REF5RDIV1	Go
0x208	R520	DPLL2_REF5RDIV2	Go
0x20B	R523	DPLL3_REF1	Go
0x20D	R525	DPLL3_REF3	Go
0x20E	R526	DPLL3_REF4	Go
0x20F	R527	DPLL3_REFSEL_STAT	Go
0x210	R528	DPLL3_FDET_LCK_BY1	Go
0x211	R529	DPLL3_FDET_LCK_BY0	Go
0x212	R530	DPLL3_FDET_UNLCK_BY1	Go
0x213	R531	DPLL3_FDET_UNLCK_BY0	Go
0x214	R532	DPLL3_FDET2_CNTSTRT_BY3	Go
0x215	R533	DPLL3_FDET2_CNTSTRT_BY2	Go
0x216	R534	DPLL3_FDET2_CNTSTRT_BY1	Go
0x217	R535	DPLL3_FDET2_CNTSTRT_BY0	Go
0x218	R536	DPLL3_FDET_CNTSTRT_BY3	Go
0x219	R537	DPLL3_FDET_CNTSTRT_BY2	Go
0x21A	R538	DPLL3_FDET_CNTSTRT_BY1	Go
0x21B	R539	DPLL3_FDET_CNTSTRT_BY0	Go
0x21C	R540	DPLL3_FDET_VCO_CNTSTRT_BY3	Go
0x21D	R541	DPLL3_FDET_VCO_CNTSTRT_BY2	Go
0x21E	R542	DPLL3_FDET_VCO_CNTSTRT_BY1	Go
0x21F	R543	DPLL3_FDET_VCO_CNTSTRT_BY0	Go
0x220	R544	DPLL3_FDET_STATUS	Go
0x223	R547	DPLL3_CTRL1	Go
0x224	R548	DPLL3_SCLR_BY1	Go
0x226	R550	DPLL3_PHOFF_BY5	Go
0x227	R551	DPLL3_PHOFF_BY4	Go
0x228	R552	DPLL3_PHOFF_BY3	Go
0x229	R553	DPLL3_PHOFF_BY2	Go
0x22A	R554	DPLL3_PHOFF_BY1	Go
0x22B	R555	DPLL3_PHOFF_BY0	Go

Table 1-1. Device Registers (continued)

Offset	Acronym	Register Name	Section
0x22C	R556	DPLL3_FREERUN_BY4	Go
0x22D	R557	DPLL3_FREERUN_BY3	Go
0x22E	R558	DPLL3_FREERUN_BY2	Go
0x22F	R559	DPLL3_FREERUN_BY1	Go
0x230	R560	DPLL3_FREERUN_BY0	Go
0x24E	R590	DPLL3_LCKTMR_BY1	Go
0x24F	R591	DPLL3_LCKTMR_BY0	Go
0x252	R594	DPLL3_HOLDTMR_BY1	Go
0x253	R595	DPLL3_HOLDTMR_BY0	Go
0x254	R596	DPLL3_PHS1TMR_BY1	Go
0x255	R597	DPLL3_PHS1TMR_BY0	Go
0x25B	R603	DPLL3_PLLK	Go
0x25C	R604	DPLL3_PLUNLK	Go
0x25D	R605	DPLL3_PHS1LIM	Go
0x262	R610	DPLL3_DBG2	Go
0x263	R611	DPLL3_DBG3	Go
0x266	R614	DPLL3_FBDIV_BY4	Go
0x267	R615	DPLL3_FBDIV_BY3	Go
0x268	R616	DPLL3_FBDIV_BY2	Go
0x269	R617	DPLL3_FBDIV_BY1	Go
0x26A	R618	DPLL3_FBDIV_BY0	Go
0x26B	R619	DPLL3_FBNUM_BY4	Go
0x26C	R620	DPLL3_FBNUM_BY3	Go
0x26D	R621	DPLL3_FBNUM_BY2	Go
0x26E	R622	DPLL3_FBNUM_BY1	Go
0x26F	R623	DPLL3_FBNUM_BY0	Go
0x270	R624	DPLL3_FBDEN_BY4	Go
0x271	R625	DPLL3_FBDEN_BY3	Go
0x272	R626	DPLL3_FBDEN_BY2	Go
0x273	R627	DPLL3_FBDEN_BY1	Go
0x274	R628	DPLL3_FBDEN_BY0	Go
0x275	R629	DPLL3_FBDIV2_BY4	Go
0x276	R630	DPLL3_FBDIV2_BY3	Go
0x277	R631	DPLL3_FBDIV2_BY2	Go
0x278	R632	DPLL3_FBDIV2_BY1	Go
0x279	R633	DPLL3_FBDIV2_BY0	Go
0x27A	R634	DPLL3_FBNUM2_BY4	Go
0x27B	R635	DPLL3_FBNUM2_BY3	Go
0x27C	R636	DPLL3_FBNUM2_BY2	Go
0x27D	R637	DPLL3_FBNUM2_BY1	Go
0x27E	R638	DPLL3_FBNUM2_BY0	Go
0x27F	R639	DPLL3_FBDEN2_BY4	Go
0x280	R640	DPLL3_FBDEN2_BY3	Go
0x281	R641	DPLL3_FBDEN2_BY2	Go
0x282	R642	DPLL3_FBDEN2_BY1	Go
0x283	R643	DPLL3_FBDEN2_BY0	Go
0x284	R644	DPLL3_FBDIV_SEL	Go

Table 1-1. Device Registers (continued)

Offset	Acronym	Register Name	Section
0x285	R645	DPLL3_FBMASHCTL	Go
0x286	R646	DPLL3_FBFDEV_BY4	Go
0x287	R647	DPLL3_FBFDEV_BY3	Go
0x288	R648	DPLL3_FBFDEV_BY2	Go
0x289	R649	DPLL3_FBFDEV_BY1	Go
0x28A	R650	DPLL3_FBFDEV_BY0	Go
0x28B	R651	DPLL3_FBFDEVUPDATE	Go
0x28C	R652	DPLL3_FBFDEVEN	Go
0x28D	R653	DPLL3_FBNUM_STAT_BY4	Go
0x28E	R654	DPLL3_FBNUM_STAT_BY3	Go
0x28F	R655	DPLL3_FBNUM_STAT_BY2	Go
0x290	R656	DPLL3_FBNUM_STAT_BY1	Go
0x291	R657	DPLL3_FBNUM_STAT_BY0	Go
0x292	R658	DPLL3_REF_DBLR	Go
0x293	R659	DPLL3_REF0RDIV1	Go
0x294	R660	DPLL3_REF0RDIV2	Go
0x295	R661	DPLL3_REF1RDIV1	Go
0x296	R662	DPLL3_REF1RDIV2	Go
0x297	R663	DPLL3_REF2RDIV1	Go
0x298	R664	DPLL3_REF2RDIV2	Go
0x29D	R669	DPLL3_REF5RDIV1	Go
0x29E	R670	DPLL3_REF5RDIV2	Go
0x2C3	R707	APLL1_CP_RPU	Go
0x2C4	R708	APLL1_CPG	Go
0x2C5	R709	APLL1_LPF_R2	Go
0x2C6	R710	APLL1_LPF_R3	Go
0x2C7	R711	APLL1_LPF_R4	Go
0x2C8	R712	APLL1_LPF_C3C4	Go
0x2C9	R713	APLL1_RDIV_BY1	Go
0x2CA	R714	APLL1_RDIV_BY0	Go
0x2CB	R715	APLL1_RDIV_CTL	Go
0x2CC	R716	APLL1_NDIV_BY1	Go
0x2CD	R717	APLL1_NDIV_BY0	Go
0x2CE	R718	APLL1_NUM_MSB	Go
0x2CF	R719	APLL1_NUM_BY4	Go
0x2D0	R720	APLL1_NUM_BY3	Go
0x2D1	R721	APLL1_NUM_BY2	Go
0x2D2	R722	APLL1_NUM_BY1	Go
0x2D3	R723	APLL1_NUM_BY0	Go
0x2D4	R724	APLL1_MASH_CTL	Go
0x2D5	R725	APLL1_NUM_STAT_BY4	Go
0x2D6	R726	APLL1_NUM_STAT_BY3	Go
0x2D7	R727	APLL1_NUM_STAT_BY2	Go
0x2D8	R728	APLL1_NUM_STAT_BY1	Go
0x2D9	R729	APLL1_NUM_STAT_BY0	Go
0x2DB	R731	APLL1_VCO_PRIDIV_CTL	Go
0x2DC	R732	APLL1_VCO_SECDIV_CTL	Go

Table 1-1. Device Registers (continued)

Offset	Acronym	Register Name	Section
0x2DD	R733	APLL1_VCO_BUF_CTL	Go
0x2E5	R741	APLL1_CALSTAT1	Go
0x305	R773	APLL2_CAL	Go
0x309	R777	APLL2_CP_PU	Go
0x30A	R778	APLL2_CPG	Go
0x30B	R779	APLL2_LPF_R2	Go
0x30C	R780	APLL2_LPF_R3	Go
0x30D	R781	APLL2_LPF_R4	Go
0x30E	R782	APLL2_LPF_C3C4	Go
0x30F	R783	APLL2_RDIV_BY1	Go
0x310	R784	APLL2_RDIV_BY0	Go
0x311	R785	APLL2_RDIV_CTL	Go
0x312	R786	APLL2_NDIV_BY1	Go
0x313	R787	APLL2_NDIV_BY0	Go
0x314	R788	APLL2_NUM_MSB	Go
0x315	R789	APLL2_NUM_BY4	Go
0x316	R790	APLL2_NUM_BY3	Go
0x317	R791	APLL2_NUM_BY2	Go
0x318	R792	APLL2_NUM_BY1	Go
0x319	R793	APLL2_NUM_BY0	Go
0x31A	R794	APLL2_MASH_CTL	Go
0x31B	R795	APLL2_NUM_STAT_BY4	Go
0x31C	R796	APLL2_NUM_STAT_BY3	Go
0x31D	R797	APLL2_NUM_STAT_BY2	Go
0x31E	R798	APLL2_NUM_STAT_BY1	Go
0x31F	R799	APLL2_NUM_STAT_BY0	Go
0x323	R803	APLL2_VCO_BUF_CTL	Go
0x324	R804	APLL2_VCO_DIV	Go
0x325	R805	APLL2_VCO_DRVR	Go
0x32D	R813	APLL2_CALSTAT1	Go
0x348	R840	APLL3_CPBLEED	Go
0x349	R841	APLL3_CPG	Go
0x34A	R842	APLL3_LPF_R2	Go
0x34B	R843	APLL3_LPF_R3	Go
0x34C	R844	APLL3_LPF_R4	Go
0x34D	R845	APLL3_LPF_C3C4	Go
0x34E	R846	APLL3_RDIV_BY1	Go
0x34F	R847	APLL3_RDIV_BY0	Go
0x350	R848	APLL3_RDIV_CTL	Go
0x351	R849	APLL3_NDIV_BY1	Go
0x352	R850	APLL3_NDIV_BY0	Go
0x353	R851	APLL3_NUM_MSB	Go
0x354	R852	APLL3_NUM_BY4	Go
0x355	R853	APLL3_NUM_BY3	Go
0x356	R854	APLL3_NUM_BY2	Go
0x357	R855	APLL3_NUM_BY1	Go
0x358	R856	APLL3_NUM_BY0	Go

Table 1-1. Device Registers (continued)

Offset	Acronym	Register Name	Section
0x359	R857	APLL3_MASH_CTL	Go
0x35A	R858	APLL3_NUM_STAT_BY4	Go
0x35B	R859	APLL3_NUM_STAT_BY3	Go
0x35C	R860	APLL3_NUM_STAT_BY2	Go
0x35D	R861	APLL3_NUM_STAT_BY1	Go
0x35E	R862	APLL3_NUM_STAT_BY0	Go
0x360	R864	APLL3_VCO_CTL	Go
0x361	R865	APLL3_VCO_CTL2	Go
0x362	R866	APLL3_VCO_BUF_CTL	Go
0x3C1	R961	OUT0_MODE	Go
0x3C2	R962	OUT0_CTL	Go
0x3C3	R963	OUT0_CTL	Go
0x3C4	R964	OUT1_MODE	Go
0x3C5	R965	OUT1_CTL	Go
0x3C6	R966	OUT1_CTL	Go
0x3C7	R967	OUT0_1_CMOS_CTL	Go
0x3C8	R968	CH0_1_ZDLY	Go
0x3C9	R969	CH0_1_CTL	Go
0x3CC	R972	CH0_1_MUX_CTL2	Go
0x3CD	R973	CH0_1_MUX_CTL2	Go
0x3CE	R974	CH0_1_CH0_STATIC_OFFSET_BY1	Go
0x3CF	R975	CH0_1_CH0_STATIC_OFFSET_BY0	Go
0x3D0	R976	CH0_1_CH1_STATIC_OFFSET_BY1	Go
0x3D1	R977	CH0_1_CH1_STATIC_OFFSET_BY0	Go
0x3D2	R978	CH0_1_CH0_DIV_BY1	Go
0x3D3	R979	CH0_1_CH0_DIV_BY0	Go
0x3D4	R980	CH0_1_CH1_DIV_BY1	Go
0x3D5	R981	CH0_1_CH1_DIV_BY0	Go
0x3D6	R982	CH0_1_SR_ANA_DELAY	Go
0x3D7	R983	CH0_1_SR_ANA_DELAY_CTL	Go
0x3D8	R984	CH0_1_SR_DDLY	Go
0x3D9	R985	CH0_1_SR_DIV_BY2	Go
0x3DA	R986	CH0_1_SR_DIV_BY1	Go
0x3DB	R987	CH0_1_SR_DIV_BY0	Go
0x3DC	R988	CH0_1_SR_STATIC_OFFSET_BY1	Go
0x3DD	R989	CH0_1_SR_STATIC_OFFSET_BY0	Go
0x3DE	R990	CH0_1_SR_CTL	Go
0x3DF	R991	CH0_1_DFT	Go
0x400	R1024	OUT2_MODE	Go
0x401	R1025	OUT2_CTL	Go
0x402	R1026	CH2_CTL	Go
0x403	R1027	CH2_CTL2	Go
0x404	R1028	CH2_STATIC_OFFSET_BY1	Go
0x405	R1029	CH2_STATIC_OFFSET_BY0	Go
0x406	R1030	CH2_DIV_BY1	Go
0x407	R1031	CH2_DIV_BY0	Go
0x420	R1056	OUT3_MODE	Go

Table 1-1. Device Registers (continued)

Offset	Acronym	Register Name	Section
0x421	R1057	OUT3_CTL	Go
0x422	R1058	CH3_CTL	Go
0x423	R1059	CH3_CTL2	Go
0x424	R1060	CH3_STATIC_OFFSET_BY1	Go
0x425	R1061	CH3_STATIC_OFFSET_BY0	Go
0x426	R1062	CH3_DIV_BY1	Go
0x427	R1063	CH3_DIV_BY0	Go
0x440	R1088	CH4_5_SR_ANA_DLY_TRIM	Go
0x441	R1089	OUT4_MODE	Go
0x442	R1090	OUT4_CTL	Go
0x443	R1091	OUT5_MODE	Go
0x444	R1092	OUT5_CTL	Go
0x445	R1093	CH4_5_CTL	Go
0x446	R1094	CH4_5_CTL2	Go
0x447	R1095	CH4_5_STATIC_OFFSET_BY1	Go
0x448	R1096	CH4_5_STATIC_OFFSET_BY0	Go
0x449	R1097	CH4_5_DIV_BY1	Go
0x44A	R1098	CH4_5_DIV_BY0	Go
0x44B	R1099	CH4_5_SR_ANA_DELAY	Go
0x44C	R1100	CH4_5_SR_ANA_DELAY_CTL	Go
0x44D	R1101	CH4_5_SR_DDLY	Go
0x44E	R1102	CH4_5_SR_DIV_BY2	Go
0x44F	R1103	CH4_5_SR_DIV_BY1	Go
0x450	R1104	CH4_5_SR_DIV_BY0	Go
0x451	R1105	CH4_5_SR_STATIC_OFFSET_BY1	Go
0x452	R1106	CH4_5_SR_STATIC_OFFSET_BY0	Go
0x453	R1107	CH4_5_SR_PULSE_CTL	Go
0x454	R1108	CH4_5_DFT	Go
0x461	R1121	OUT6_MODE	Go
0x462	R1122	OUT6_CTL	Go
0x463	R1123	OUT7_MODE	Go
0x464	R1124	OUT7_CTL	Go
0x465	R1125	CH6_7_CTL	Go
0x466	R1126	CH6_7_CTL2	Go
0x467	R1127	CH6_7_STATIC_OFFSET_BY1	Go
0x468	R1128	CH6_7_STATIC_OFFSET_BY0	Go
0x469	R1129	CH6_7_DIV_BY1	Go
0x46A	R1130	CH6_7_DIV_BY0	Go
0x46B	R1131	CH6_7_SR_ANA_DELAY	Go
0x46C	R1132	CH6_7_SR_ANA_DELAY_CTL	Go
0x46D	R1133	CH6_7_SR_DDLY	Go
0x46E	R1134	CH6_7_SR_DIV_BY2	Go
0x46F	R1135	CH6_7_SR_DIV_BY1	Go
0x470	R1136	CH6_7_SR_DIV_BY0	Go
0x471	R1137	CH6_7_SR_STATIC_OFFSET_BY1	Go
0x472	R1138	CH6_7_SR_STATIC_OFFSET_BY0	Go
0x473	R1139	CH6_7_SR_PULSE_CTL	Go

Table 1-1. Device Registers (continued)

Offset	Acronym	Register Name	Section
0x474	R1140	CH6_7_DFT	Go
0x481	R1153	OUT8_MODE	Go
0x482	R1154	OUT8_CTL	Go
0x483	R1155	OUT9_MODE	Go
0x484	R1156	OUT9_CTL	Go
0x485	R1157	CH8_9_CTL	Go
0x486	R1158	CH8_9_CTL2	Go
0x487	R1159	CH8_9_STATIC_OFFSET_BY1	Go
0x488	R1160	CH8_9_STATIC_OFFSET_BY0	Go
0x489	R1161	CH8_9_DIV_BY1	Go
0x48A	R1162	CH8_9_DIV_BY0	Go
0x48B	R1163	CH8_9_SR_ANA_DELAY	Go
0x48C	R1164	CH8_9_SR_ANA_DELAY_CTL	Go
0x48D	R1165	CH8_9_SR_DDLY	Go
0x48E	R1166	CH8_9_SR_DIV_BY2	Go
0x48F	R1167	CH8_9_SR_DIV_BY1	Go
0x490	R1168	CH8_9_SR_DIV_BY0	Go
0x491	R1169	CH8_9_SR_STATIC_OFFSET_BY1	Go
0x492	R1170	CH8_9_SR_STATIC_OFFSET_BY0	Go
0x493	R1171	CH8_9_SR_PULSE_CTL	Go
0x4A1	R1185	OUT10_MODE	Go
0x4A2	R1186	OUT10_CTL	Go
0x4A3	R1187	OUT11_MODE	Go
0x4A4	R1188	OUT11_CTL	Go
0x4A5	R1189	CH10_11_CTL	Go
0x4A6	R1190	CH10_11_CTL2	Go
0x4A7	R1191	CH10_11_STATIC_OFFSET_BY1	Go
0x4A8	R1192	CH10_11_STATIC_OFFSET_BY0	Go
0x4A9	R1193	CH10_11_DIV_BY1	Go
0x4AA	R1194	CH10_11_DIV_BY0	Go
0x4AB	R1195	CH10_11_SR_ANA_DELAY	Go
0x4AC	R1196	CH10_11_SR_ANA_DELAY_CTL	Go
0x4AD	R1197	CH10_11_SR_DDLY	Go
0x4AE	R1198	CH10_11_SR_DIV_BY2	Go
0x4AF	R1199	CH10_11_SR_DIV_BY1	Go
0x4B0	R1200	CH10_11_SR_DIV_BY0	Go
0x4B1	R1201	CH10_11_SR_STATIC_OFFSET_BY1	Go
0x4B2	R1202	CH10_11_SR_STATIC_OFFSET_BY0	Go
0x4B3	R1203	CH10_11_SR_PULSE_CTL	Go
0x4B4	R1204	CH10_11_DFT	Go
0x4C1	R1217	OUT12_MODE	Go
0x4C2	R1218	OUT12_CTL	Go
0x4C3	R1219	OUT13_MODE	Go
0x4C4	R1220	OUT12_CTL	Go
0x4C5	R1221	CH12_13_CTL	Go
0x4C6	R1222	CH12_13_CTL2	Go
0x4C7	R1223	CH12_13_STATIC_OFFSET_BY1	Go

Table 1-1. Device Registers (continued)

Offset	Acronym	Register Name	Section
0x4C8	R1224	CH12_13_STATIC_OFFSET_BY0	Go
0x4C9	R1225	CH12_13_DIV_BY1	Go
0x4CA	R1226	CH12_13_DIV_BY0	Go
0x4CB	R1227	CH12_13_SR_ANA_DELAY	Go
0x4CC	R1228	CH12_13_SR_ANA_DELAY_CTL	Go
0x4CD	R1229	CH12_13_SR_DDLY	Go
0x4CE	R1230	CH12_13_SR_DIV_BY2	Go
0x4CF	R1231	CH12_13_SR_DIV_BY1	Go
0x4D0	R1232	CH12_13_SR_DIV_BY0	Go
0x4D1	R1233	CH12_13_SR_STATIC_OFFSET_BY1	Go
0x4D2	R1234	CH12_13_SR_STATIC_OFFSET_BY0	Go
0x4D3	R1235	CH12_13_SR_PULSE_CTL	Go
0x4D4	R1236	CH12_13_DFT	Go
0x4E0	R1248	OUT14_MODE	Go
0x4E1	R1249	OUT14_CTL	Go
0x4E2	R1250	CH14_CTL	Go
0x4E3	R1251	CH14_CTL2	Go
0x4E4	R1252	CH14_STATIC_OFFSET_BY1	Go
0x4E5	R1253	CH14_STATIC_OFFSET_BY0	Go
0x4E6	R1254	CH14_DIV_BY1	Go
0x4E7	R1255	CH14_DIV_BY0	Go
0x500	R1280	OUT15_MODE	Go
0x501	R1281	OUT15_CTL	Go
0x502	R1282	CH15_CTL	Go
0x503	R1283	CH15_CTL2	Go
0x504	R1284	CH15_STATIC_OFFSET_BY1	Go
0x505	R1285	CH15_STATIC_OFFSET_BY0	Go
0x506	R1286	CH15_DIV_BY1	Go
0x507	R1287	CH15_DIV_BY0	Go

Complex bit access types are encoded to fit into small table cells. Table 1-2 shows the codes that are used for access types in this section.

Table 1-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
WSC	W	Write
Reset or Default Value		
- *n*		Value after reset or the default value

1.1 R0 Register (Offset = 0x0) [Reset = 0x10]

R0 is shown in Table 1-3.

Return to the Summary Table.

Table 1-3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VNDRID_15:8	R	0x10	See Register 1

1.2 R1 Register (Offset = 0x1) [Reset = 0xB]

R1 is shown in Table 1-4.

Return to the Summary Table.

Table 1-4. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VNDRID	R	0xB	Vendor Identification Number. The Vendor Identification Number is a unique 16-bit identification number assigned to I2C/SMBus vendors. ROM=N, EEPROM=N

1.3 R2 Register (Offset = 0x2) [Reset = 0x40]

R2 is shown in Table 1-5.

Return to the Summary Table.

Table 1-5. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRODID	R	0x40	Product ID ROM=N, EEPROM=N

1.4 R3 Register (Offset = 0x3) [Reset = 0x5]

R3 is shown in Table 1-6.

Return to the Summary Table.

Table 1-6. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REVID	R	0x5	Revision ID. LMK5C33216 = 0x05 ROM=N, EEPROM=N

1.5 R16 Register (Offset = 0x10) [Reset = 0x0]

R16 is shown in Table 1-7.

Return to the Summary Table.

Table 1-7. R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMCNT	R	0x0	NVM Program Count. The NVMCNT increments automatically after every EEPROM Erase/Program Cycle. The NVMCNT value is retreived automatically after reset, after a NVM Commit operation, or after a Erase/Program cycle. The NVMCNT register will increment until it reaches it's maximum value of 255 after which no further increments will take place. ROM=N, EEPROM=Y

1.6 R18 Register (Offset = 0x12) [Reset = 0x0]

R18 is shown in Table 1-8.

Return to the Summary Table.

Table 1-8. R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	SLAVEADR_MSB	R	0x0	I2C/SMBus Slave Address. This field holds the 5 MSB bits of the Slave Address used to identify this device during I2C/SMBus transactions. The two least significant bits of the Slave Address are defined by CSC/ADD/TOD pin upon power-up. This is user writeable to EEPROM only through SRAM register at address 12. ROM=N, EEPROM=Y

1.7 R19 Register (Offset = 0x13) [Reset = 0x0]

R19 is shown in Table 1-9.

Return to the Summary Table.

Table 1-9. R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	EEREV	R/W	0x0	EEPROM Image Revision ID. EEPROM Image Revision is automatically retrieved from EEPROM and stored in the EEREV register after areset or after a NVM commit operation. This is user writeable to EEPROM only through SRAM register address 13. ROM=N, EEPROM=Y

1.8 R20 Register (Offset = 0x14) [Reset = 0x0]

R20 is shown in Table 1-10.

Return to the Summary Table.

Table 1-10. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ROM_PLUS_EE	R/W	0x0	When set, the thin EEPROM settings are loaded. This is user writeable to EEPROM only through SRAM register address 14. ROM=N, EEPROM=Y
6:3	EE_ROM_PAGE_SEL	R/W	0x0	EE_ROM_PAGE_SEL value is added to the GPIO pin value for selecting the start-up ROM. ROM=N, EEPROM=Y
2:0	RESERVED	R	0x0	Reserved

1.9 R21 Register (Offset = 0x15) [Reset = 0x80]

R21 is shown in Table 1-11.

Return to the Summary Table.

Table 1-11. R21 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPI_3WIRE_DIS	R/W	0x1	Disable SPI 3 wire readback. ROM=Y, EEPROM=N 0x0 = 3-wire SPI readback enabled 0x1 = 3-wire SPI readback disabled
6	SYNC_SW	R/W	0x0	Software SYNC Assertion. Writing a '1' to this bit is equivalent to asserting the SYNC pin. SYNC_EN must also be set to 1. ROM=Y, EEPROM=Y
5:0	RESERVED	R	0x0	Reserved

1.10 R22 Register (Offset = 0x16) [Reset = 0x3D]

R22 is shown in Table 1-12.

Return to the Summary Table.

Table 1-12. R22 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	DPLL3_EN	R/W	0x1	Enable DPLL3. ROM=Y, EEPROM=N
4	APLL3_EN	R/W	0x1	Enable APLL3. ROM=Y, EEPROM=Y
3	DPLL2_EN	R/W	0x1	Enable DPLL2. ROM=Y, EEPROM=N
2	APLL2_EN	R/W	0x1	Enable APLL2. ROM=Y, EEPROM=Y
1	DPLL1_EN	R/W	0x0	Enable DPLL1. ROM=Y, EEPROM=N
0	APLL1_EN	R/W	0x1	Enable APLL1. ROM=Y, EEPROM=Y

1.11 R23 Register (Offset = 0x17) [Reset = 0x0]

R23 is shown in Table 1-13.

Return to the Summary Table.

Table 1-13. R23 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	SWRST	R/W	0x0	Software Reset ALL functions (active low). Writing a '0' will cause the device to return to its power-up state apart from the I2C registers and the configuration controller. The configuration controller is excluded to prevent an re-transfer of EEPROM data to on-chip registers. Not a self clearing field. ROM=N, EEPROM=N
5:0	RESERVED	R	0x0	Reserved

1.12 R24 Register (Offset = 0x18) [Reset = 0x1]

R24 is shown in Table 1-14.

Return to the Summary Table.

Table 1-14. R24 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	APLL3_STRT_PRTY	R/W	0x0	APLL3 Startup Priority. 0 is highest priority. APLLs with the same priority will start simultaneously. ROM=Y, EEPROM=Y
3:2	APLL2_STRT_PRTY	R/W	0x0	APLL2 Startup Priority. 0 is highest priority. APLLs with the same priority will start simultaneously. ROM=Y, EEPROM=Y
1:0	APLL1_STRT_PRTY	R/W	0x1	APLL1 Startup Priority. 0 is highest priority. APLLs with the same priority will start simultaneously. ROM=Y, EEPROM=Y

1.13 R25 Register (Offset = 0x19) [Reset = 0x0]

R25 is shown in Table 1-15.

Return to the Summary Table.

Table 1-15. R25 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:1	RESERVED	R	0x0	Reserved
0	SYNC_EN	R/W	0x0	Allows SYNC from SYNC_SW and GPIO pin. For GPIO sync, must be set together with SYNC input for GPIOx_MODE. ROM=Y, EEPROM=Y

1.14 R26 Register (Offset = 0x1A) [Reset = 0x0]

R26 is shown in Table 1-16.

Return to the Summary Table.

Table 1-16. R26 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:1	RESERVED	R	0x0	Reserved
0	SYSREF_REQ_SW	R/WSC	0x0	Software SYSREF request trigger ROM=N, EEPROM=N

1.15 R27 Register (Offset = 0x1B) [Reset = 0x0]

R27 is shown in Table 1-17.

Return to the Summary Table.

Table 1-17. R27 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TOD_CNTR_39:32	R	0x0	Time of Day Readback ROM=N, EEPROM=N

1.16 R28 Register (Offset = 0x1C) [Reset = 0x0]

R28 is shown in Table 1-18.

Return to the Summary Table.

Table 1-18. R28 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TOD_CNTR_31:24	R	0x0	Time of Day Readback ROM=N, EEPROM=N

1.17 R29 Register (Offset = 0x1D) [Reset = 0x0]

R29 is shown in Table 1-19.

Return to the Summary Table.

Table 1-19. R29 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TOD_CNTR_23:16	R	0x0	Time of Day Readback ROM=N, EEPROM=N

1.18 R30 Register (Offset = 0x1E) [Reset = 0x0]

R30 is shown in Table 1-20.

Return to the Summary Table.

Table 1-20. R30 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TOD_CNTR_15:8	R	0x0	Time of Day Readback ROM=N, EEPROM=N

1.19 R31 Register (Offset = 0x1F) [Reset = 0x0]

R31 is shown in Table 1-21.

Return to the Summary Table.

Table 1-21. R31 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TOD_CNTR	R	0x0	Time of Day Readback ROM=N, EEPROM=N

1.20 R32 Register (Offset = 0x20) [Reset = 0x0]

R32 is shown in Table 1-22.

Return to the Summary Table.

Table 1-22. R32 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	TOD_CNTR_TRIG_SEL	R/W	0x0	Time of Day trigger select. If using GPIO, must also set GPIOx_MODE to provide ToD trigger. ROM=Y, EEPROM=N 0x0 = SPI 0x1 = GPIO
0	TOD_CNTR_EN	R/W	0x0	Time of Day counter enable. When transitioning from 0 --> 1, the ToD counter will start from 0. ROM=Y, EEPROM=N

1.21 R33 Register (Offset = 0x21) [Reset = 0x0]

R33 is shown in Table 1-23.

Return to the Summary Table.

Table 1-23. R33 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	LOL_PLL1	R	0x0	Loss of Lock - APLL1 ROM=N, EEPROM=N

Table 1-23. R33 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	LOL_PLL2	R	0x0	Loss of Lock - APLL2 ROM=N, EEPROM=N
1	RESERVED	R	0x0	Reserved
0	LOS_FDET_XO	R	0x0	Loss of Source Freq Detection - XO ROM=N, EEPROM=N

1.22 R34 Register (Offset = 0x22) [Reset = 0x0]

R34 is shown in Table 1-24.

Return to the Summary Table.

Table 1-24. R34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL1	R	0x0	Loss of Phase Lock - DPLL1 ROM=N, EEPROM=N
6	LOFL_DPLL1	R	0x0	Loss of Frequency Lock - DPLL1 ROM=N, EEPROM=N
5	HIST1	R	0x0	Tuning word history update - DPLL1 ROM=N, EEPROM=N
4	HLDOVR1	R	0x0	Holdover event - DPLL1 ROM=N, EEPROM=N
3	REFSWITCH1	R	0x0	Reference Switchover - DPLL1 ROM=N, EEPROM=N
2	LOR_MISSCLK1	R	0x0	Loss of Active Reference - Missing Clock - DPLL1 ROM=N, EEPROM=N
1	LOR_FREQ1	R	0x0	Loss of Active Reference - Frequency - DPLL1 ROM=N, EEPROM=N
0	LOR_PH1	R	0x0	Loss of Active Reference - Phase - DPLL1 ROM=N, EEPROM=N

1.23 R35 Register (Offset = 0x23) [Reset = 0x0]

R35 is shown in Table 1-25.

Return to the Summary Table.

Table 1-25. R35 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL2	R	0x0	Loss of Phase Lock - DPLL2 ROM=N, EEPROM=N
6	LOFL_DPLL2	R	0x0	Loss of Frequency Lock - DPLL2 ROM=N, EEPROM=N
5	HIST2	R	0x0	Tuning word history update - DPLL2 ROM=N, EEPROM=N
4	HLDOVR2	R	0x0	Holdover event - DPLL2 ROM=N, EEPROM=N
3	REFSWITCH2	R	0x0	Reference Switchover - DPLL2 ROM=N, EEPROM=N
2	LOR_MISSCLK2	R	0x0	Loss of Active Reference - Missinig Clock - DPLL2 ROM=N, EEPROM=N
1	LOR_FREQ2	R	0x0	Loss of Active Reference - Frequency - DPLL2 ROM=N, EEPROM=N
0	LOR_PH2	R	0x0	Loss of Active Reference - Phase - DPLL2 ROM=N, EEPROM=N

1.24 R36 Register (Offset = 0x24) [Reset = 0x0]

R36 is shown in Table 1-26.

Return to the Summary Table.

Table 1-26. R36 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL3	R	0x0	Loss of Phase Lock - DPLL3 ROM=N, EEPROM=N
6	LOFL_DPLL3	R	0x0	Loss of Frequency Lock - DPLL3 ROM=N, EEPROM=N
5	HIST3	R	0x0	Tuning word history update - DPLL3 ROM=N, EEPROM=N
4	HLDOVR3	R	0x0	Holdover event - DPLL3 ROM=N, EEPROM=N
3	REFSWITCH3	R	0x0	Reference Switchover - DPLL3 ROM=N, EEPROM=N
2	LOR_MISSCLK3	R	0x0	Loss of Active Reference - Missinig Clock - DPLL3 ROM=N, EEPROM=N
1	LOR_FREQ3	R	0x0	Loss of Active Reference - Frequency - DPLL3 ROM=N, EEPROM=N
0	LOR_PH3	R	0x0	Loss of Active Reference - Phase - DPLL3 ROM=N, EEPROM=N

1.25 R37 Register (Offset = 0x25) [Reset = 0x0]

R37 is shown in Table 1-27.

Return to the Summary Table.

Table 1-27. R37 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	LOL_PLL1_MASK	R/W	0x0	Masks Loss of Lock - APLL1. When LOL_PLL1_MASK is 1 then the LOL_PLL1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
2	LOL_PLL2_MASK	R/W	0x0	Masks Loss of Lock - APLL2. When LOL_PLL2_MASK is 1 then the LOL_PLL2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
1	RESERVED	R	0x0	Reserved
0	LOS_FDET_XO_MASK	R/W	0x0	Masks Loss of Source Freq Detection - XO. When LOS_FDET_XO_MASK is 1 then the LOS_FDET_XO interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

1.26 R38 Register (Offset = 0x26) [Reset = 0xFF]

R38 is shown in Table 1-28.

Return to the Summary Table.

Table 1-28. R38 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL1_MASK	R/W	0x1	Masks Loss of Phase Lock - DPLL1. When LOPL_DPLL1_MASK is 1 then the LOPL_DPLL1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

Table 1-28. R38 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	LOFL_DPLL1_MASK	R/W	0x1	Masks Loss of Freq Lock - DPLL1. When LOFL_DPLL1_MASK is 1 then the LOFL_DPLL1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
5	HIST1_MASK	R/W	0x1	Masks Tuning word history update - DPLL1. When HIST1_MASK is 1 then the HIST1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
4	HLDOVR1_MASK	R/W	0x1	Masks Holdover event - DPLL1. When HLDOVR1_MASK is 1 then the HLDOVR1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
3	REFSWITCH1_MASK	R/W	0x1	Masks Reference Switchover - DPLL1. When REFSWITCH1_MASK is 1 then the REFSWITCH1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
2	LOR_MISSCLK1_MASK	R/W	0x1	Masks Loss of Active Reference - Missinig Clock - DPLL1. When LOR_MISSCLK1_MASK is 1 then the LOR_MISSCLK1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
1	LOR_FREQ1_MASK	R/W	0x1	Masks Loss of Active Reference - Frequency - DPLL1. When LOR_FREQ1_MASK is 1 then the LOR_FREQ1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
0	LOR_PH1_MASK	R/W	0x1	Masks Loss of Active Reference - Phase - DPLL1. When LOR_PH1_MASK is 1 then the LOR_PH1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

1.27 R39 Register (Offset = 0x27) [Reset = 0x20]

R39 is shown in Table 1-29.

Return to the Summary Table.

Table 1-29. R39 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL2_MASK	R/W	0x0	Masks Loss of Phase Lock - DPLL2. When LOPL_DPLL2_MASK is 1 then the LOPL_DPLL2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
6	LOFL_DPLL2_MASK	R/W	0x0	Masks Loss of Freq Lock - DPLL2. When LOFL_DPLL2_MASK is 1 then the LOFL_DPLL2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
5	HIST2_MASK	R/W	0x1	Masks Tuning word history update - DPLL2. When HIST2_MASK is 1 then the HIST2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
4	HLDOVR2_MASK	R/W	0x0	Masks Holdover event - DPLL2. When HLDOVR2_MASK is 1 then the HLDOVR2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
3	REFSWITCH2_MASK	R/W	0x0	Masks Reference Switchover - DPLL2. When REFSWITCH2_MASK is 1 then the REFSWITCH2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

Table 1-29. R39 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	LOR_MISSCLK2_MASK	R/W	0x0	Masks Loss of Active Reference - Missing Clock - DPLL2. When LOR_MISSCLK2_MASK is 1 then the LOR_MISSCLK2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
1	LOR_FREQ2_MASK	R/W	0x0	Masks Loss of Active Reference - Frequency - DPLL2. When LOR_FREQ2_MASK is 1 then the LOR_FREQ2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
0	LOR_PH2_MASK	R/W	0x0	Masks Loss of Active Reference - Phase - DPLL2. When LOR_PH2_MASK is 1 then the LOR_PH2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

1.28 R40 Register (Offset = 0x28) [Reset = 0x20]

R40 is shown in Table 1-30.

Return to the Summary Table.

Table 1-30. R40 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL3_MASK	R/W	0x0	Masks Loss of Phase Lock - DPLL3. When LOPL_DPLL3_MASK is 1 then the LOPL_DPLL3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
6	LOFL_DPLL3_MASK	R/W	0x0	Masks Loss of Freq Lock - DPLL3. When LOFL_DPLL3_MASK is 1 then the LOFL_DPLL3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
5	HIST3_MASK	R/W	0x1	Masks Tuning word history update - DPLL3. When HIST3_MASK is 1 then the HIST3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
4	HLDOVR3_MASK	R/W	0x0	Masks Holdover event - DPLL3. When HLDOVR3_MASK is 1 then the HLDOVR3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
3	REFSWITCH3_MASK	R/W	0x0	Masks Reference Switchover - DPLL3. When REFSWITCH3_MASK is 1 then the REFSWITCH3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
2	LOR_MISSCLK3_MASK	R/W	0x0	Masks Loss of Active Reference - Missinig Clock - DPLL3. When LOR_MISSCLK3_MASK is 1 then the LOR_MISSCLK3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
1	LOR_FREQ3_MASK	R/W	0x0	Masks Loss of Active Reference - Frequency - DPLL3. When LOR_FREQ3_MASK is 1 then the LOR_FREQ3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
0	LOR_PH3_MASK	R/W	0x0	Masks Loss of Active Reference - Phase - DPLL3. When LOR_PH3_MASK is 1 then the LOR_PH3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

1.29 R41 Register (Offset = 0x29) [Reset = 0x0]

R41 is shown in Table 1-31.

Return to the Summary Table.

Table 1-31. R41 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	LOL_PLL1_POL	R/W	0x0	LOL_PLL1 Flag Polarity. When LOL_PLL1_POL is 1 then a high on LOL_PLL1 will set the LOL_PLL1_INTR bit in register R45. When LOL_PLL1_POL is 0 then a low on LOL_PLL1 will set the LOL_PLL1_INTR bit. ROM=Y, EEPROM=N
2	LOL_PLL2_POL	R/W	0x0	LOL_PLL2 Flag Polarity. When LOL_PLL2_POL is 1 then a high on LOL_PLL2 will set the LOL_PLL2_INTR bit in register R45. When LOL_PLL2_POL is 0 then a low on LOL_PLL2 will set the LOL_PLL2_INTR bit. ROM=Y, EEPROM=N
1	RESERVED	R	0x0	Reserved
0	LOS_FDET_XO_POL	R/W	0x0	LOS_FDET_XO Flag Polarity. When LOS_FDET_XO_POL is 1 then a high on LOS_FDET_XO will set the LOS_FDET_XO_INTR bit in register R45. When LOS_FDET_XO_POL is 0 then a low on LOS_FDET_XO will set the LOS_FDET_XO_INTR bit. ROM=Y, EEPROM=N

1.30 R42 Register (Offset = 0x2A) [Reset = 0x0]

R42 is shown in Table 1-32.

Return to the Summary Table.

Table 1-32. R42 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL1_POL	R/W	0x0	LOPL_DPLL1 Flag Polarity. When LOPL_DPLL1_POL is 1 then a high on LOPL_DPLL1 will set the LOPL_DPLL1_INTR bit in register R46. When LOPL_DPLL1_POL is 0 then a low on LOPL_DPLL1 will set the LOPL_DPLL1_INTR bit. ROM=Y, EEPROM=N
6	LOFL_DPLL1_POL	R/W	0x0	LOFL_DPLL1 Flag Polarity. When LOFL_DPLL1_POL is 1 then a high on LOFL_DPLL1 will set the LOFL_DPLL1_INTR bit in register R46. When LOFL_DPLL1_POL is 0 then a low on LOFL_DPLL1 will set the LOFL_DPLL1_INTR bit. ROM=Y, EEPROM=N
5	HIST1_POL	R/W	0x0	HIST1 Flag Polarity. When HIST1_POL is 1 then a high on HIST1 will set the HIST1_INTR bit in register R46. When HIST1_POL is 0 then a low on HIST1 will set the HIST1_INTR bit. ROM=Y, EEPROM=N
4	HLDOVR1_POL	R/W	0x0	HLDOVR1 Flag Polarity. When HLDOVR1_POL is 1 then a high on HLDOVR1 will set the HLDOVR1_INTR bit in register R46. When HLDOVR1_POL is 0 then a low on HLDOVR1 will set the HLDOVR1_INTR bit. ROM=Y, EEPROM=N
3	REFSWITCH1_POL	R/W	0x0	REFSWITCH1 Flag Polarity. When REFSWITCH1_POL is 1 then a high on REFSWITCH1 will set the REFSWITCH1_INTR bit in register R46. When REFSWITCH1_POL is 0 then a low on REFSWITCH1 will set the REFSWITCH1_INTR bit. ROM=Y, EEPROM=N
2	LOR_MISSCLK1_POL	R/W	0x0	LOR_MISSCLK1 Flag Polarity. When LOR_MISSCLK1_POL is 1 then a high on LOR_MISSCLK1 will set the LOR_MISSCLK1_INTR in R40. When LOR_MISSCLK1_POL is 0 then a low on LOR_MISSCLK1 will set the LOR_MISSCLK1_INTR bit. ROM=Y, EEPROM=N

Table 1-32. R42 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	LOR_FREQ1_POL	R/W	0x0	LOR_FREQ1 Flag Polarity. When LOR_FREQ1_POL is 1 then a high on LOR_FREQ1 will set the LOR_FREQ1_INTR in register R46. When LOR_FREQ1_POL is 0 then a low on LOR_FREQ1 will set the LOR_FREQ1_INTR bit. ROM=Y, EEPROM=N
0	LOR_PH1_POL	R/W	0x0	LOR_PH1 Flag Polarity. When LOR_PH1_POL is 1 then a high on LOR_PH1 will set the LOR_PH1_INTR bit in register R46. When LOR_PH1_POL is 0 then a low on LOR_PH1 will set the LOR_PH1_INTR bit. ROM=Y, EEPROM=N

1.31 R43 Register (Offset = 0x2B) [Reset = 0x0]

R43 is shown in Table 1-33.

Return to the Summary Table.

Table 1-33. R43 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL2_POL	R/W	0x0	LOPL_DPLL2 Flag Polarity. When LOPL_DPLL2_POL is 1 then a high on LOPL_DPLL2 will set the LOPL_DPLL2_INTR in register R47. When LOPL_DPLL2_POL is 0 then a low on LOPL_DPLL2 will set the LOPL_DPLL2_INTR bit. ROM=Y, EEPROM=N
6	LOFL_DPLL2_POL	R/W	0x0	LOFL_DPLL2 Flag Polarity. When LOFL_DPLL2_POL is 1 then a high on LOFL_DPLL2 will set the LOFL_DPLL2_INTR bit in register R47. When LOFL_DPLL2_POL is 0 then a low on LOFL_DPLL2 will set the LOFL_DPLL2_INTR bit. ROM=Y, EEPROM=N
5	HIST2_POL	R/W	0x0	HIST2 Flag Polarity. When HIST2_POL is 1 then a high on HIST2 will set the HIST2_INTR bit in register R47. When HIST2_POL is 0 then a low on HIST2 will set the HIST2_INTR bit. ROM=Y, EEPROM=N
4	HLDOVR2_POL	R/W	0x0	HLDOVR2 Flag Polarity. When HLDOVR2_POL is 1 then a high on HLDOVR2 will set the HLDOVR2_INTR bit in register R47. When HLDOVR2_POL is 0 then a low on HLDOVR2 will set the HLDOVR2_INTR bit. ROM=Y, EEPROM=N
3	REFSWITCH2_POL	R/W	0x0	REFSWITCH2 Flag Polarity. When REFSWITCH2_POL is 1 then a high on REFSWITCH2 will set the REFSWITCH2_INTR in R41. When REFSWITCH2_POL is 0 then a low on REFSWITCH2 will set the REFSWITCH2_INTR bit. ROM=Y, EEPROM=N
2	LOR_MISSCLK2_POL	R/W	0x0	LOR_MISSCLK2 Flag Polarity. When LOR_MISSCLK2_POL is 1 then a high on LOR_MISSCLK2 will set the LOR_MISSCLK2_INTR bit in register R47. When LOR_MISSCLK2_POL is 0 then a low on LOR_MISSCLK2 will set the LOR_MISSCLK2_INTR bit. ROM=Y, EEPROM=N
1	LOR_FREQ2_POL	R/W	0x0	LOR_FREQ2 Flag Polarity. When LOR_FREQ2_POL is 1 then a high on LOR_FREQ2 will set the LOR_FREQ2_INTR bit in register R47. When LOR_FREQ2_POL is 0 then a low on LOR_FREQ2 will set the LOR_FREQ2_INTR bit. ROM=Y, EEPROM=N
0	LOR_PH2_POL	R/W	0x0	LOR_FREQ2 Flag Polarity. When LOR_FREQ2_POL is 1 then a high on LOR_FREQ2 will set the LOR_FREQ2_INTR in R41. When LOR_FREQ2_POL is 0 then a low on LOR_FREQ2 will set the LOR_FREQ2_INTR bit. ROM=Y, EEPROM=N

1.32 R44 Register (Offset = 0x2C) [Reset = 0x0]

R44 is shown in Table 1-34.

Return to the Summary Table.

Table 1-34. R44 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL3_POL	R/W	0x0	LOPL_DPLL3 Flag Polarity. When LOPL_DPLL3_POL is 1 then a high on LOPL_DPLL3 will set the LOPL_DPLL3_INTR bit in register R48. When LOPL_DPLL3_POL is 0 then a low on LOPL_DPLL3 will set the LOPL_DPLL3_INTR bit. ROM=Y, EEPROM=N
6	LOFL_DPLL3_POL	R/W	0x0	LOFL_DPLL3 Flag Polarity. When LOFL_DPLL3_POL is 1 then a high on LOFL_DPLL3 will set the LOFL_DPLL3_INTR bit in register R48. When LOFL_DPLL3_POL is 0 then a low on LOFL_DPLL3 will set the LOFL_DPLL3_INTR bit. ROM=Y, EEPROM=N
5	HIST3_POL	R/W	0x0	HIST3 Flag Polarity. When HIST3_POL is 1 then a high on HIST3 will set the HIST3_INTR bit in register R48. When HIST3_POL is 0 then a low on HIST3 will set the HIST3_INTR bit. ROM=Y, EEPROM=N
4	HLDOVR3_POL	R/W	0x0	HLDOVR3 Flag Polarity. When HLDOVR3_POL is 1 then a high on HLDOVR3 will set the HLDOVR3_INTR bit in register R48. When HLDOVR3_POL is 0 then a low on HLDOVR3 will set the HLDOVR3_INTR bit. ROM=Y, EEPROM=N
3	REFSWITCH3_POL	R/W	0x0	REFSWITCH3 Flag Polarity. When REFSWITCH3_POL is 1 then a high on REFSWITCH3 will set the REFSWITCH3_INTR bit in register R48. When REFSWITCH3_POL is 0 then a low on REFSWITCH3 will set the REFSWITCH3_INTR bit. ROM=Y, EEPROM=N
2	LOR_MISSCLK3_POL	R/W	0x0	LOR_MISSCLK3 Flag Polarity. When LOR_MISSCLK3_POL is 1 then a high on LOR_MISSCLK3 will set the LOR_MISSCLK3_INTR bit in register R48. When LOR_MISSCLK3_POL is 0 then a low on LOR_MISSCLK3 will set the LOR_MISSCLK3_INTR bit. ROM=Y, EEPROM=N
1	LOR_FREQ3_POL	R/W	0x0	LOR_FREQ3 Flag Polarity. When LOR_FREQ3_POL is 1 then a high on LOR_FREQ3 will set the LOR_FREQ3_INTR in R42. When LOR_FREQ3_POL is 0 then a low on LOR_FREQ3 will set the LOR_FREQ3_INTR bit. ROM=Y, EEPROM=N
0	LOR_PH3_POL	R/W	0x0	LOR_PH3 Flag Polarity. When LOR_PH3_POL is 1 then a high on LOR_PH3 will set the LOR_PH3_INTR bit in register R48. When LOR_PH3_POL is 0 then a low on LOR_PH3 will set the LOR_PH3_INTR bit. ROM=Y, EEPROM=N

1.33 R45 Register (Offset = 0x2D) [Reset = 0x0]

R45 is shown in Table 1-35.

Return to the Summary Table.

Table 1-35. R45 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	LOL_PLL1_INTR	R	0x0	LOL_PLL1 Interrupt. The LOL_PLL1_INTR bit is set when a level of the correct polarity is detected on the LOL_PLL1 interrupt source. The LOL_PLL1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N

Table 1-35. R45 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	LOL_PLL2_INTR	R	0x0	LOL_PLL2 Interrupt. The LOL_PLL2_INTR bit is set when a level of the correct polarity is detected on the LOL_PLL2 interrupt source. The LOL_PLL2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
1	RESERVED	R	0x0	Reserved
0	LOS_FDET_XO_INTR	R	0x0	LOL_FDET_XO Interrupt. The LOL_FDET_XO_INTR bit is set when a level of the correct polarity is detected on the LOL_FDET_XO interrupt source. The LOL_FDET_XO_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N

1.34 R46 Register (Offset = 0x2E) [Reset = 0x0]

R46 is shown in Table 1-36.

Return to the Summary Table.

Table 1-36. R46 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL1_INTR	R	0x0	LOPL_DPLL1 Interrupt. The LOPL_DPLL1_INTR bit is set when a level of the correct polarity is detected on the LOPL_DPLL1 interrupt source. The LOPL_DPLL1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
6	LOFL_DPLL1_INTR	R	0x0	LOFL_DPLL1 Interrupt. The LOFL_DPLL1_INTR bit is set when a level of the correct polarity is detected on the LOFL_DPLL1 interrupt source. The LOFL_DPLL1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
5	HIST1_INTR	R	0x0	HIST1 Interrupt. The HIST1_INTR bit is set when a level of the correct polarity is detected on the HIST1 interrupt source. The HIST1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
4	HLDOVR1_INTR	R	0x0	HLDOVR1 Interrupt. The HLDOVR1_INTR bit is set when a level of the correct polarity is detected on the HLDOVR1 interrupt source. The HLDOVR1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
3	REFSWITCH1_INTR	R	0x0	REFSWITCH1 Interrupt. The REFSWITCH1_INTR bit is set when a level of the correct polarity is detected on the REFSWITCH1 interrupt source. The REFSWITCH1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
2	LOR_MISSCLK1_INTR	R	0x0	LOR_MISSCLK1 Interrupt. The LOR_MISSCLK1_INTR bit is set when a level of the correct polarity is detected on the LOR_MISSCLK1 interrupt source. The LOR_MISSCLK1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
1	LOR_FREQ1_INTR	R	0x0	LOR_FREQ1 Interrupt. The LOR_FREQ1_INTR bit is set when a level of the correct polarity is detected on the LOR_FREQ1 interrupt source. The LOR_FREQ1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
0	LOR_PH1_INTR	R	0x0	LOR_PH1 Interrupt. The LOR_PH1_INTR bit is set when a level of the correct polarity is detected on the LOR_PH1 interrupt source. The LOR_PH1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N

1.35 R47 Register (Offset = 0x2F) [Reset = 0x0]

R47 is shown in Table 1-37.

Return to the Summary Table.

Table 1-37. R47 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL2_INTR	R	0x0	LOPL_DPLL2 Interrupt. The LOPL_DPLL2_INTR bit is set when a level of the correct polarity is detected on the LOPL_DPLL2 interrupt source. The LOPL_DPLL2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
6	LOFL_DPLL2_INTR	R	0x0	LOFL_DPLL2 Interrupt. The LOFL_DPLL2_INTR bit is set when a level of the correct polarity is detected on the LOFL_DPLL2 interrupt source. The LOFL_DPLL2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
5	HIST2_INTR	R	0x0	HIST2 Interrupt. The HIST2_INTR bit is set when a level of the correct polarity is detected on the HIST2 interrupt source. The HIST2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
4	HLDOVR2_INTR	R	0x0	HLDOVR2 Interrupt. The HLDOVR2_INTR bit is set when a level of the correct polarity is detected on the HLDOVR2 interrupt source. The HLDOVR2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
3	REFSWITCH2_INTR	R	0x0	REFSWITCH2 Interrupt. The REFSWITCH2_INTR bit is set when a level of the correct polarity is detected on the REFSWITCH2 interrupt source. The REFSWITCH2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
2	LOR_MISSCLK2_INTR	R	0x0	LOR_MISSCLK2 Interrupt. The LOR_MISSCLK2_INTR bit is set when a level of the correct polarity is detected on the LOR_MISSCLK2 interrupt source. The LOR_MISSCLK2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
1	LOR_FREQ2_INTR	R	0x0	LOR_FREQ2 Interrupt. The LOR_FREQ2_INTR bit is set when a level of the correct polarity is detected on the LOR_FREQ2 interrupt source. The LOR_FREQ2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
0	LOR_PH2_INTR	R	0x0	LOR_PH2 Interrupt. The LOR_PH2_INTR bit is set when a level of the correct polarity is detected on the LOR_PH2 interrupt source. The LOR_PH2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N

1.36 R48 Register (Offset = 0x30) [Reset = 0x0]

R48 is shown in Table 1-38.

Return to the Summary Table.

Table 1-38. R48 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL3_INTR	R	0x0	LOPL_DPLL3 Interrupt. The LOPL_DPLL3_INTR bit is set when a level of the correct polarity is detected on the LOPL_DPLL3 interrupt source. The LOPL_DPLL3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
6	LOFL_DPLL3_INTR	R	0x0	LOFL_DPLL3 Interrupt. The LOFL_DPLL3_INTR bit is set when a level of the correct polarity is detected on the LOFL_DPLL3 interrupt source. The LOFL_DPLL3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
5	HIST3_INTR	R	0x0	HIST3 Interrupt. The HIST3_INTR bit is set when a level of the correct polarity is detected on the HIST3 interrupt source. The HIST3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N

Table 1-38. R48 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	HLDOVR3_INTR	R	0x0	HLDOVR3 Interrupt. The HLDOVR3_INTR bit is set when a level of the correct polarity is detected on the HLDOVR3 interrupt source. The HLDOVR3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
3	REFSWITCH3_INTR	R	0x0	REFSWITCH3 Interrupt. The REFSWITCH3_INTR bit is set when a level of the correct polarity is detected on the REFSWITCH3 interrupt source. The REFSWITCH3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
2	LOR_MISSCLK3_INTR	R	0x0	LOR_MISSCLK3 Interrupt. The LOR_MISSCLK3_INTR bit is set when a level of the correct polarity is detected on the LOR_MISSCLK3 interrupt source. The LOR_MISSCLK3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
1	LOR_FREQ3_INTR	R	0x0	LOR_FREQ3 Interrupt. The LOR_FREQ3_INTR bit is set when a level of the correct polarity is detected on the LOR_FREQ3 interrupt source. The LOR_FREQ3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
0	LOR_PH3_INTR	R	0x0	LOR_PH3 Interrupt. The LOR_PH3_INTR bit is set when a level of the correct polarity is detected on the LOR_PH3 interrupt source. The LOR_PH3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N

1.37 R49 Register (Offset = 0x31) [Reset = 0x2]

R49 is shown in Table 1-39.

Return to the Summary Table.

Table 1-39. R49 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	INT_EN	R/W	0x1	Interrupt Enable. If INT_EN is 1 then the interrupt circuit is enabled. If INT_EN is 0 the interrupt circuit is disabled. When INT_EN is 0, interrupts cannot be signalled on the GPIOx pins, and the flag registers (*_INTR) will not be updated; however, the live status registers will still reflect the current state of the internal interrupt source signals. To provide an interrupt on a pin, a GPIOx pin must also be configured as interrupt output. Interrupts may be enabled without providing a GPIOx output to allow sticky bits to be set. ROM=Y, EEPROM=N
0	INT_CLR	R/WSC	0x0	Clears all interrupt flag (*_INTR) registers ROM=N, EEPROM=N

1.38 R50 Register (Offset = 0x32) [Reset = 0x0]

R50 is shown in Table 1-40.

Return to the Summary Table.

Table 1-40. R50 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:2	RESERVED	R	0x0	Reserved
1	REF1_VALID_STATUS	R	0x0	Status of Reference Input Validation for IN1 ROM=N, EEPROM=N

Table 1-40. R50 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	REF0_VALID_STATUS	R	0x0	Status of Reference Input Validation for IN0 ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.39 R52 Register (Offset = 0x34) [Reset = 0x0]

R52 is shown in Table 1-41.

Return to the Summary Table.

Table 1-41. R52 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF1_PH_STATUS	R	0x0	Status of Reference 1 Phase Validation ROM=N, EEPROM=N
4	REF1_MISSCLK_STATUS	R	0x0	Status of Reference 1 Missing Clock Validation ROM=N, EEPROM=N
3	REF1_FDET_STATUS	R	0x0	Status of Reference 1 Frequency Validation ROM=N, EEPROM=N
2	REF0_PH_STATUS	R	0x0	Status of Reference 0 Phase Validation ROM=N, EEPROM=N
1	REF0_MISSCLK_STATUS	R	0x0	Status of Reference 0 Missing Clock Validation ROM=N, EEPROM=N
0	REF0_FDET_STATUS	R	0x0	Status of Reference 0 Frequency Validation ROM=N, EEPROM=N

1.40 R53 Register (Offset = 0x35) [Reset = 0x0]

R53 is shown in Table 1-42.

Return to the Summary Table.

Table 1-42. R53 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	TOD_CNTR_HELD	R	0x0	TOD Holded. A GPIO or SPI event has latched a holdover value. Will clear to 0 after TOD CNTR LSB is read. ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.41 R54 Register (Offset = 0x36) [Reset = 0x0]

R54 is shown in Table 1-43.

Return to the Summary Table.

Table 1-43. R54 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	GPIO0_IN_FLT_EN	R/W	0x0	Enable GPIO0 Input Pin Deglitch Filter ROM=Y, EEPROM=N

Table 1-43. R54 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	GPIO0_MODE	R/W	0x0	Select GPIO0 Pin Operating Mode. ROM=Y, EEPROM=N 0x0 = STATUS or INT, Acts as status or interrupt outputs (See section on STATUS/INTERRUPT) 0x1 = INSEL01_DPLL1, Selects input 0 or input 1 for DPLL1 0x2 = INSEL01_DPLL2, Selects input 0 or input 1 for DPLL2 0x3 = INSEL01_DPLL3, Selects input 0 or input 1 for DPLL3 0x4 = Reserved 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved 0x8 = Reserved 0x9 = Reserved 0xA = Reserved 0xB = Reserved 0xC = Reserved 0xD = Reserved 0xE = Reserved 0xF = Reserved 0x10 = Reserved 0x11 = Reserved 0x12 = Reserved 0x13 = Reserved 0x14 = Reserved 0x15 = Reserved 0x16 = Reserved 0x17 = Reserved 0x18 = Reserved 0x19 = Reserved 0x1A = Reserved 0x1B = Reserved 0x1C = Reserved 0x1D = Reserved 0x1E = Reserved 0x1F = SYNC, Synchronizes selected outputs on a low-to-high pulse. "1" is normal state for outputs. "0" sets outputs in SYNC. 0x20 = SYSREF_REQ, Can request SYSREF pulses on appropriate output channels via low-to-high pulse. 0x21 = FDEV_TRIG_DPLL1, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL1 0x22 = FDEV_TRIG_DPLL2, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL2 0x23 = FDEV_TRIG_DPLL3, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL3 0x24 = FDEV_DIR_DPLL1, FDEV_DIR_DPLL1 will determine the direction of the FDEV trigger. 0 = Positive and 1 = Negative 0x25 = FDEV_DIR_DPLL2, FDEV_DIR_DPLL2 will determine the direction of the FDEV trigger. 0 = Positive and 1 = Negative 0x26 = FDEV_DIR_DPLL3, FDEV_DIR_DPLL3 will determine the direction of the FDEV trigger. 0 = Positive and 1 = Negative 0x27 = TOD_TRIG_SEL

1.42 R55 Register (Offset = 0x37) [Reset = 0x27]

R55 is shown in Table 1-44.

Return to the Summary Table.

Table 1-44. R55 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	GPIO1_IN_FLT_EN	R/W	0x0	Enable GPIO1 Input Pin Deglitch Filter ROM=Y, EEPROM=N

Table 1-44. R55 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	GPIO1_MODE	R/W	0x27	Select GPIO1 Pin Operating Mode. ROM=Y, EEPROM=N 0x0 = STATUS or INT, Acts as status or interrupt outputs (See section on STATUS/INTERRUPT) 0x1 = INSEL01_DPLL1, Selects input 0 or input 1 for DPLL1 0x2 = INSEL01_DPLL2, Selects input 0 or input 1 for DPLL2 0x3 = INSEL01_DPLL3, Selects input 0 or input 1 for DPLL3 0x4 = Reserved 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved 0x8 = Reserved 0x9 = Reserved 0xA = Reserved 0xB = Reserved 0xC = Reserved 0xD = Reserved 0xE = Reserved 0xF = Reserved 0x10 = Reserved 0x11 = Reserved 0x12 = Reserved 0x13 = Reserved 0x14 = Reserved 0x15 = Reserved 0x16 = Reserved 0x17 = Reserved 0x18 = Reserved 0x19 = Reserved 0x1A = Reserved 0x1B = Reserved 0x1C = Reserved 0x1D = Reserved 0x1E = Reserved 0x1F = SYNC, Synchronizes selected outputs on a low-to-high pulse. "1" is normal state for outputs. "0" sets outputs in SYNC. 0x20 = SYSREF_REQ, Can request SYSREF pulses on appropriate output channels via low-to-high pulse. 0x21 = FDEV_TRIG_DPLL1, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL1 0x22 = FDEV_TRIG_DPLL2, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL2 0x23 = FDEV_TRIG_DPLL3, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL3 0x24 = FDEV_DIR_DPLL1, FDEV_DIR_DPLL1 will determine the direction of the FDEV trigger. 0 = Positive and 1 = Negative 0x25 = FDEV_DIR_DPLL2, FDEV_DIR_DPLL2 will determine the direction of the FDEV trigger. 0 = Positive and 1 = Negative 0x26 = FDEV_DIR_DPLL3, FDEV_DIR_DPLL3 will determine the direction of the FDEV trigger. 0 = Positive and 1 = Negative 0x27 = TOD_TRIG_SEL

1.43 R56 Register (Offset = 0x38) [Reset = 0x0]

R56 is shown in Table 1-45.

Return to the Summary Table.

Table 1-45. R56 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	GPIO2_IN_FLT_EN	R/W	0x0	Enable GPIO2 Input Pin Deglitch Filter ROM=Y, EEPROM=N

Table 1-45. R56 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	GPIO2_MODE	R/W	0x0	Select GPIO2 Pin Operating Mode. ROM=Y, EEPROM=N 0x0 = STATUS or INT, Acts as status or interrupt outputs (See section on STATUS/INTERRUPT) 0x1 = INSEL01_DPLL1, Selects input 0 or input 1 for DPLL1 0x2 = INSEL01_DPLL2, Selects input 0 or input 1 for DPLL2 0x3 = INSEL01_DPLL3, Selects input 0 or input 1 for DPLL3 0x4 = Reserved 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved 0x8 = Reserved 0x9 = Reserved 0xA = Reserved 0xB = Reserved 0xC = Reserved 0xD = Reserved 0xE = Reserved 0xF = Reserved 0x10 = Reserved 0x11 = Reserved 0x12 = Reserved 0x13 = Reserved 0x14 = Reserved 0x15 = Reserved 0x16 = Reserved 0x17 = Reserved 0x18 = Reserved 0x19 = Reserved 0x1A = Reserved 0x1B = Reserved 0x1C = Reserved 0x1D = Reserved 0x1E = Reserved 0x1F = SYNC, Synchronizes selected outputs on a low-to-high pulse. "1" is normal state for outputs. "0" sets outputs in SYNC. 0x20 = SYSREF_REQ, Can request SYSREF pulses on appropriate output channels via low-to-high pulse. 0x21 = FDEV_TRIG_DPLL1, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL1 0x22 = FDEV_TRIG_DPLL2, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL2 0x23 = FDEV_TRIG_DPLL3, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL3 0x24 = FDEV_DIR_DPLL1, FDEV_DIR_DPLL1 will determine the direction of the FDEV trigger. 0 = Positive and 1 = Negative 0x25 = FDEV_DIR_DPLL2, FDEV_DIR_DPLL2 will determine the direction of the FDEV trigger. 0 = Positive and 1 = Negative 0x26 = FDEV_DIR_DPLL3, FDEV_DIR_DPLL3 will determine the direction of the FDEV trigger. 0 = Positive and 1 = Negative 0x27 = TOD_TRIG_SEL

1.44 R57 Register (Offset = 0x39) [Reset = 0xF]

R57 is shown in Table 1-46.

Return to the Summary Table.

Table 1-46. R57 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-46. R57 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	GPIO0_SEL	R/W	0xF	GPIO0 Status Signal Select. ROM=Y, EEPROM=N 0x0 = XO Loss of Signal (LOS) 0x1 = PLL1 Loss of Lock (LOL) 0x2 = PLL2 Loss of Lock (LOL) 0x3 = PLL3 Loss of Lock (LOL) 0x4 = DPLL1 Loss of Phase Lock (LOPL) 0x5 = DPLL1 Loss of Frequency Lock (LOFL) 0x6 = PLL1 LOL | DPLL1 LOPL | DPLL1 LOFL 0x7 = DPLL2 Loss of Phase Lock (LOPL) 0x8 = DPLL2 Loss of Frequency Lock (LOFL) 0x9 = PLL2 LOL | DPLL2 LOPL | DPLL2 LOFL 0xA = DPLL3 Loss of Phase Lock (LOPL) 0xB = DPLL3 Loss of Frequency Lock (LOFL) 0xC = PLL3 LOL | DPLL3 LOPL | DPLL3 LOFL 0xD = DPLL1 | DPLL2 | DPLL3 LOL 0xE = Interrupt (INTR). Derived from INT_FLAG register bits. 0xF = SPI Readback Data (SDO) 0x10 = Reserved 0x11 = Reserved 0x12 = Reserved 0x13 = Reserved 0x14 = Reserved 0x15 = DPLL1 REF0 Selected 0x16 = DPLL1 REF1 Selected 0x17 = Reserved 0x18 = Reserved 0x19 = Reserved 0x1A = DPLL1 Holdover Active 0x1B = DPLL2 REF0 Selected 0x1C = DPLL2 REF1 Selected 0x1D = Reserved 0x1E = Reserved 0x1F = Reserved 0x20 = DPLL2 Holdover Active 0x21 = DPLL3 REF0 Selected 0x22 = DPLL3 REF1 Selected 0x23 = Reserved 0x24 = Reserved 0x25 = Reserved 0x26 = DPLL3 Holdover Active 0x27 = REF0 Frequency Monitor 0x28 = REF1 Frequency Monitor 0x29 = Reserved 0x2A = Reserved 0x2B = Reserved 0x2C = REF0 Missing Clock Monitor 0x2D = REF1 Missing Clock Monitor 0x2E = Reserved 0x2F = Reserved 0x30 = Reserved 0x31 = Reserved 0x32 = Reserved 0x33 = Reserved 0x34 = Reserved 0x35 = Reserved 0x36 = Reserved 0x37 = Reserved 0x38 = Reserved 0x39 = Reserved 0x3A = Reserved 0x3B = REF0 Phase Validation Monitor 0x3C = REF1 Phase Validation Monitor

1.45 R58 Register (Offset = 0x3A) [Reset = 0x0]

R58 is shown in Table 1-47.

Return to the Summary Table.

Table 1-47. R58 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-47. R58 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	GPIO1_SEL	R/W	0x0	GPIO1 Status Signal Select. ROM=Y, EEPROM=N 0x0 = XO Loss of Signal (LOS) 0x1 = PLL1 Loss of Lock (LOL) 0x2 = PLL2 Loss of Lock (LOL) 0x3 = PLL3 Loss of Lock (LOL) 0x4 = DPLL1 Loss of Phase Lock (LOPL) 0x5 = DPLL1 Loss of Frequency Lock (LOFL) 0x6 = PLL1 LOL | DPLL1 LOPL | DPLL1 LOFL 0x7 = DPLL2 Loss of Phase Lock (LOPL) 0x8 = DPLL2 Loss of Frequency Lock (LOFL) 0x9 = PLL2 LOL | DPLL2 LOPL | DPLL2 LOFL 0xA = DPLL3 Loss of Phase Lock (LOPL) 0xB = DPLL3 Loss of Frequency Lock (LOFL) 0xC = PLL3 LOL | DPLL3 LOPL | DPLL3 LOFL 0xD = DPLL1 | DPLL2 | DPLL3 LOL 0xE = Interrupt (INTR). Derived from INT_FLAG register bits. 0xF = SPI Readback Data (SDO) 0x10 = Reserved 0x11 = Reserved 0x12 = Reserved 0x13 = Reserved 0x14 = Reserved 0x15 = DPLL1 REF0 Selected 0x16 = DPLL1 REF1 Selected 0x17 = Reserved 0x18 = Reserved 0x19 = Reserved 0x1A = DPLL1 Holdover Active 0x1B = DPLL2 REF0 Selected 0x1C = DPLL2 REF1 Selected 0x1D = Reserved 0x1E = Reserved 0x1F = Reserved 0x20 = DPLL2 Holdover Active 0x21 = DPLL3 REF0 Selected 0x22 = DPLL3 REF1 Selected 0x23 = Reserved 0x24 = Reserved 0x25 = Reserved 0x26 = DPLL3 Holdover Active 0x27 = REF0 Frequency Monitor 0x28 = REF1 Frequency Monitor 0x29 = Reserved 0x2A = Reserved 0x2B = Reserved 0x2C = REF0 Missing Clock Monitor 0x2D = REF1 Missing Clock Monitor 0x2E = Reserved 0x2F = Reserved 0x30 = Reserved 0x31 = Reserved 0x32 = Reserved 0x33 = Reserved 0x34 = Reserved 0x35 = Reserved 0x36 = Reserved 0x37 = Reserved 0x38 = Reserved 0x39 = Reserved 0x3A = Reserved 0x3B = REF0 Phase Validation Monitor 0x3C = REF1 Phase Validation Monitor

1.46 R59 Register (Offset = 0x3B) [Reset = 0xE]

R59 is shown in Table 1-48.

Return to the Summary Table.

Table 1-48. R59 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-48. R59 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	GPIO2_SEL	R/W	0xE	GPIO2 Status Signal Select. ROM=Y, EEPROM=N 0x0 = XO Loss of Signal (LOS) 0x1 = PLL1 Loss of Lock (LOL) 0x2 = PLL2 Loss of Lock (LOL) 0x3 = PLL3 Loss of Lock (LOL) 0x4 = DPLL1 Loss of Phase Lock (LOPL) 0x5 = DPLL1 Loss of Frequency Lock (LOFL) 0x6 = PLL1 LOL | DPLL1 LOPL | DPLL1 LOFL 0x7 = DPLL2 Loss of Phase Lock (LOPL) 0x8 = DPLL2 Loss of Frequency Lock (LOFL) 0x9 = PLL2 LOL | DPLL2 LOPL | DPLL2 LOFL 0xA = DPLL3 Loss of Phase Lock (LOPL) 0xB = DPLL3 Loss of Frequency Lock (LOFL) 0xC = PLL3 LOL | DPLL3 LOPL | DPLL3 LOFL 0xD = DPLL1 | DPLL2 | DPLL3 LOL 0xE = Interrupt (INTR). Derived from INT_FLAG register bits. 0xF = SPI Readback Data (SDO) 0x10 = Reserved 0x11 = Reserved 0x12 = Reserved 0x13 = Reserved 0x14 = Reserved 0x15 = DPLL1 REF0 Selected 0x16 = DPLL1 REF1 Selected 0x17 = Reserved 0x18 = Reserved 0x19 = Reserved 0x1A = DPLL1 Holdover Active 0x1B = DPLL2 REF0 Selected 0x1C = DPLL2 REF1 Selected 0x1D = Reserved 0x1E = Reserved 0x1F = Reserved 0x20 = DPLL2 Holdover Active 0x21 = DPLL3 REF0 Selected 0x22 = DPLL3 REF1 Selected 0x23 = Reserved 0x24 = Reserved 0x25 = Reserved 0x26 = DPLL3 Holdover Active 0x27 = REF0 Frequency Monitor 0x28 = REF1 Frequency Monitor 0x29 = Reserved 0x2A = Reserved 0x2B = Reserved 0x2C = REF0 Missing Clock Monitor 0x2D = REF1 Missing Clock Monitor 0x2E = Reserved 0x2F = Reserved 0x30 = Reserved 0x31 = Reserved 0x32 = Reserved 0x33 = Reserved 0x34 = Reserved 0x35 = Reserved 0x36 = Reserved 0x37 = Reserved 0x38 = Reserved 0x39 = Reserved 0x3A = Reserved 0x3B = REF0 Phase Validation Monitor 0x3C = REF1 Phase Validation Monitor

1.47 R60 Register (Offset = 0x3C) [Reset = 0x0]

R60 is shown in Table 1-49.

Return to the Summary Table.

Table 1-49. R60 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	GPIO0_OPEND	R/W	0x0	GPIO0 Open Drain Enable ROM=Y, EEPROM=N 0x0 = CMOS 0x1 = NMOS open drain (external pull-up)
4	GPIO1_OPEND	R/W	0x0	GPIO1 Open Drain Enable ROM=Y, EEPROM=N 0x0 = CMOS 0x1 = NMOS open drain (external pull-up)
3	GPIO2_OPEND	R/W	0x0	GPIO2 Open Drain Enable ROM=Y, EEPROM=N 0x0 = CMOS 0x1 = NMOS open drain (external pull-up)
2	GPIO0_POL	R/W	0x0	GPIO0 Status Output Polarity. The GPIO0_STAT_POL bit defines the polarity of information presented on the GPIO0 output. If GPIO0_STAT_POL is set to 1, then GPIO0 is active high. If GPIO0_STAT_POL is 0, then GPIO0 is active low. ROM=Y, EEPROM=N 0x0 = Active High 0x1 = Active Low
1	GPIO1_POL	R/W	0x0	GPIO1 Status Output Polarity. The GPIO1_STAT_POL bit defines the polarity of information presented on the GPIO1 output. If GPIO1_STAT_POL is set to 1, then GPIO1 is active high. If GPIO1_STAT_POL is 0, then GPIO1 is active low. ROM=Y, EEPROM=N 0x0 = Active High 0x1 = Active Low
0	GPIO2_POL	R/W	0x0	GPIO2 Status Output Polarity. The GPIO2_STAT_POL bit defines the polarity of information presented on the GPIO2 output. If GPIO2_STAT_POL is set to 1, then GPIO2 is active high. If GPIO2_STAT_POL is 0, then GPIO2 is active low. ROM=Y, EEPROM=N 0x0 = Active High 0x1 = Active Low

1.48 R61 Register (Offset = 0x3D) [Reset = 0x1]

R61 is shown in Table 1-50.

Return to the Summary Table.

Table 1-50. R61 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:2	GPIO_SYSREF_SEL	R/W	0x0	Select SYSREF output for GPIO output. When GPIOx_SEL choses SYSREF, this is the SYSREF source which is output on the GPIO. Select SYSREF after static digital delay but before the analog and digital delay. ROM=Y, EEPROM=N 0x0 = OUT_0_1 0x1 = OUT_4_5 0x2 = OUT_6_7 0x3 = OUT_8_9 0x4 = OUT_10_11 0x5 = OUT_12_13 0x6 = NA 0x7 = NA

Table 1-50. R61 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	MUTE_DPLL3_PHLOCK	R/W	0x0	DPLL3 mute enabled during phase lock ROM=Y, EEPROM=Y
0	MUTE_DPLL3_LOCK	R/W	0x1	DPLL3 mute enabled during dpll lock ROM=Y, EEPROM=Y

1.49 R62 Register (Offset = 0x3E) [Reset = 0x0]

R62 is shown in Table 1-51.

Return to the Summary Table.

Table 1-51. R62 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	MUTE_DPLL2_PHLOCK	R/W	0x0	DPLL2 mute enabled during phase lock ROM=Y, EEPROM=Y
4	MUTE_DPLL2_LOCK	R/W	0x0	DPLL2 mute enabled during dpll lock ROM=Y, EEPROM=Y
3	MUTE_APLL2_LOCK	R/W	0x0	APLL2 mute enabled during PLL lock ROM=Y, EEPROM=Y
2	MUTE_DPLL1_PHLOCK	R/W	0x0	DPLL1 mute enabled during phase lock ROM=Y, EEPROM=Y
1	MUTE_DPLL1_LOCK	R/W	0x0	DPLL1 mute enabled during dpll lock ROM=Y, EEPROM=Y
0	MUTE_APLL1_LOCK	R/W	0x0	APLL1 mute enabled during PLL lock ROM=Y, EEPROM=Y

1.50 R63 Register (Offset = 0x3F) [Reset = 0x0]

R63 is shown in Table 1-52.

Return to the Summary Table.

Table 1-52. R63 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	XO_FDET_BYP	R/W	0x0	Freq Detector Bypass. When XO_FDET_BYP is set to 1, the output of the XO/TCXO freq detector is ignored. ROM=Y, EEPROM=N
3:0	XO_ITYPE	R/W	0x0	To be updated. XO interface type control. ROM=Y, EEPROM=Y 0x0 = DC-DIFF (ext. term) 0x1 = AC-DIFF (ext. term) 0x3 = LVDS/HSDS (AC-DIFF, int. 100 Ω) 0x4 = HCSL (DC-DIFF, int. 50 Ω to GND) 0x5 = LVPECL (AC-DIFF, int. 50 Ω to GND) 0x8 = CMOS 0xC = S-E (int. 50 Ω)

1.51 R64 Register (Offset = 0x40) [Reset = 0xD]

R64 is shown in Table 1-53.

Return to the Summary Table.

Table 1-53. R64 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	XO_OUT_BUF_EN	R/W	0xD	Bit position enables XO Output Buffer path to: [0] The XO Freq Detector [1] APLL1 REF [2] APLL2 REF [3] APLL3 REF, and [4] OUT0_1 ROM=Y, EEPROM=Y

1.52 R67 Register (Offset = 0x43) [Reset = 0x0]

R67 is shown in Table 1-54.

Return to the Summary Table.

Table 1-54. R67 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF1_HYST_TOGGLE	R/W	0x0	Increases hysteresis for AC coupled clocks. For use with low frequency reference input clocks below TBD MHz which are AC coupled. ROM=Y, EEPROM=N
4	REF1_DC_COUPLED_EN	R/W	0x0	DC couple input. Eliminates need for hysteresis for low frequency input clocks. ROM=Y, EEPROM=N
3:0	REF1_ITYPE	R/W	0x0	To be updated. REF1 interface type control. ROM=Y, EEPROM=N 0x0 = DC-DIFF (ext. term) 0x1 = AC-DIFF (ext. term) 0x2 = DC-DIFF (int. 100 Ω term) 0x3 = LVDS/HSDS (AC-DIFF, int. 100 Ω) 0x4 = HCSL (DC-DIFF, int. 50 Ω to GND) 0x5 = LVPECL (AC-DIFF, int. 50 Ω to GND) 0x8 = CMOS 0xC = S-E (int. 50 Ω)

1.53 R68 Register (Offset = 0x44) [Reset = 0x0]

R68 is shown in Table 1-55.

Return to the Summary Table.

Table 1-55. R68 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF0_HYST_TOGGLE	R/W	0x0	Increases hysteresis for AC coupled clocks. For use with low frequency reference input clocks below TBD MHz which are AC coupled. ROM=Y, EEPROM=N
4	REF0_DC_COUPLED_EN	R/W	0x0	DC couple input. Eliminates need for hysteresis for low frequency input clocks. ROM=Y, EEPROM=N

Table 1-55. R68 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	REF0_ITYPE	R/W	0x0	To be updated. REF0 interface type control. ROM=Y, EEPROM=N 0x0 = DC-DIFF (ext. term) 0x1 = AC-DIFF (ext. term) 0x2 = DC-DIFF (int. 100 Ω term) 0x3 = LVDS/HSDS (AC-DIFF, int. 100 Ω) 0x4 = HCSL (DC-DIFF, int. 50 Ω to GND) 0x5 = LVPECL (AC-DIFF, int. 50 Ω to GND) 0x8 = CMOS 0xC = S-E (int. 50 Ω)

1.54 R69 Register (Offset = 0x45) [Reset = 0x88]

R69 is shown in Table 1-56.

Return to the Summary Table.

Table 1-56. R69 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CH_0_VCM	R/W	0x8	Sets the common-mode DC voltage for OUT0. Excluding CMOS output mode. ROM=Y, EEPROM=N
3:0	CH_1_VCM	R/W	0x8	Sets the common-mode DC voltage for OUT1. Excluding CMOS output mode. ROM=Y, EEPROM=N

1.55 R70 Register (Offset = 0x46) [Reset = 0x88]

R70 is shown in Table 1-57.

Return to the Summary Table.

Table 1-57. R70 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CH_2_VCM	R/W	0x8	Sets the common-mode DC voltage for OUT2. ROM=Y, EEPROM=N
3:0	CH_3_VCM	R/W	0x8	Sets the common-mode DC voltage for OUT3. ROM=Y, EEPROM=N

1.56 R71 Register (Offset = 0x47) [Reset = 0x88]

R71 is shown in Table 1-58.

Return to the Summary Table.

Table 1-58. R71 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CH_4_6_VCM	R/W	0x8	Sets the common-mode DC voltage for OUT4 and OUT5 (Excluding CML output mode). ROM=Y, EEPROM=N
3:0	CH_7_8_VCM	R/W	0x8	Sets the common-mode DC voltage for OUT6 and OUT7. (Excluding CML output mode). ROM=Y, EEPROM=N

1.57 R72 Register (Offset = 0x48) [Reset = 0x88]

R72 is shown in Table 1-59.

Return to the Summary Table.

Table 1-59. R72 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CH_8_9_VCM	R/W	0x8	Sets the common-mode DC voltage for OUT8 and OUT9. ROM=Y, EEPROM=N
3:0	CH_10_11_VCM	R/W	0x8	Sets the common-mode DC voltage for OUT10 and OUT11. ROM=Y, EEPROM=N

1.58 R73 Register (Offset = 0x49) [Reset = 0x8]

R73 is shown in Table 1-60.

Return to the Summary Table.

Table 1-60. R73 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	CH_12_13_VCM	R/W	0x8	Sets the common-mode DC voltage for OUT12 and OUT13. ROM=Y, EEPROM=N

1.59 R74 Register (Offset = 0x4A) [Reset = 0x88]

R74 is shown in Table 1-61.

Return to the Summary Table.

Table 1-61. R74 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CH_14_VCM	R/W	0x8	Sets the common-mode DC voltage for OUT14. ROM=Y, EEPROM=N
3:0	CH_15_VCM	R/W	0x8	Sets the common-mode DC voltage for OUT15. ROM=Y, EEPROM=N

1.60 R75 Register (Offset = 0x4B) [Reset = 0x1A]

R75 is shown in Table 1-62.

Return to the Summary Table.

Table 1-62. R75 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	TDC3_ZDM_BYPASS_FB_DIV	R/W	0x0	Selects TDC3 feedback input source ROM=Y, EEPROM=N 0x0 = Feedback Divider 0x1 = Bypass FB DIV
5	TDC3_ZDM_FB_PRE_BYP	R/W	0x0	Inserts TDC3 feedback divider in series with selected channel divider ROM=Y, EEPROM=N 0x0 = Select FB Prescaler 0x1 = Bypass FB Prescaler
4:3	TDC3_IN_SEL	R/W	0x3	Selects TDC3 zero delay input ROM=Y, EEPROM=N 0x0 = NA 0x1 = OUT_10_11_ZD_FB 0x2 = OUT_0_1_ZD_FB 0x3 = VCO3_HS_CLK

Table 1-62. R75 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	TDC3_IN_DRV_SEL	R/W	0x2	Enables zero delay input mux output ROM=Y, EEPROM=N 0x0 = NA 0x1 = NA(Bypass) 0x2 = Normal Feedback Divider Path 0x3 = NA 0x4 = NA(Bypass Pre) 0x5 = Bypass Feedback Divider 0x6 = Bypass Feedback Divider Prescaler 0x7 = NA

1.61 R76 Register (Offset = 0x4C) [Reset = 0x1A]

R76 is shown in Table 1-63.

Return to the Summary Table.

Table 1-63. R76 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	TDC2_ZDM_BYPASS_FB_DIV	R/W	0x0	Selects TDC feedback input. 0=FB_DIV, 1=ZD bypass FBDIV ROM=Y, EEPROM=N 0x0 = Feedback Divider 0x1 = Bypass FB DIV
5	TDC2_ZDM_FB_PRE_BYP	R/W	0x0	Inserts TDC feedback divider in series with selected channel divider ROM=Y, EEPROM=N 0x0 = Select FB Prescaler 0x1 = Bypass FB Prescaler
4:3	TDC2_IN_SEL	R/W	0x3	Selects zero delay input ROM=Y, EEPROM=N 0x0 = NA 0x1 = OUT_4_5_ZD_FB 0x2 = OUT_0_1_ZD_FB 0x3 = VCO2_HS_CLK
2:0	TDC2_IN_DRV_SEL	R/W	0x2	Enables zero delay input mux output ROM=Y, EEPROM=N 0x0 = NA 0x1 = NA(Bypass) 0x2 = Normal Feedback Divider Path 0x3 = NA 0x4 = NA(Bypass Pre) 0x5 = Bypass Feedback Divider 0x6 = Bypass Feedback Divider Prescaler 0x7 = NA

1.62 R77 Register (Offset = 0x4D) [Reset = 0x1A]

R77 is shown in Table 1-64.

Return to the Summary Table.

Table 1-64. R77 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	TDC1_ZDM_BYPASS_FB_DIV	R/W	0x0	Selects TDC feedback input. 0=FB_DIV, 1=ZD bypass FBDIV ROM=Y, EEPROM=N 0x0 = Feedback Divider 0x1 = Bypass FB DIV

Table 1-64. R77 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TDC1_ZDM_FB_PRE_BYP	R/W	0x0	Inserts TDC feedback divider in series with selected channel divider ROM=Y, EEPROM=N 0x0 = Select FB Prescaler 0x1 = Bypass FB Prescaler
4:3	TDC1_IN_SEL	R/W	0x3	Selects zero delay input ROM=Y, EEPROM=N 0x0 = NA 0x1 = OUT_0_1_ZD_FB 0x2 = OUT_0_1_ZD_FB 0x3 = VCO1_HS_CLK
2:0	TDC1_IN_DRV_SEL	R/W	0x2	Enables zero delay input mux output ROM=Y, EEPROM=N 0x0 = NA 0x1 = NA(Bypass) 0x2 = Normal Feedback Divider Path 0x3 = NA 0x4 = NA(Bypass Pre) 0x5 = Bypass Feedback Divider 0x6 = Bypass Feedback Divider Prescaler 0x7 = NA

1.63 R78 Register (Offset = 0x4E) [Reset = 0x0]

R78 is shown in Table 1-65.

Return to the Summary Table.

Table 1-65. R78 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF_OUT01_EN	R/W	0x0	Ref to OUT0_1 Enable. Enables the path for a reference clock (selected by REF_2OUT01_SEL) to be an input clock for OUT0_1. ROM=Y, EEPROM=N
4:0	REF_OUT01_SEL	R/W	0x0	Ref to OUT0_1 Select. Selects one reference clock which will be fed to the input of OUT0_1 (if path enabled by REF_2OUT01_EN). ROM=Y, EEPROM=N 0x0 = OFF 0x1 = REF0 0x2 = REF1 0x4 = Reserved 0x8 = Reserved

1.64 R79 Register (Offset = 0x4F) [Reset = 0xA]

R79 is shown in Table 1-66.

Return to the Summary Table.

Table 1-66. R79 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF0_EARLY_DET_EN	R/W	0x0	REF0 Early Clock Detect Enable ROM=Y, EEPROM=N
4	REF0_PH_VALID_EN	R/W	0x0	REF0 Phase Validation Enable ROM=Y, EEPROM=N
3	REF0_VALTMR_EN	R/W	0x1	REF0 Validation Timer Enable ROM=Y, EEPROM=N
2	REF0_PPM_EN	R/W	0x0	REF0 Freq ppm Enable ROM=Y, EEPROM=N

Table 1-66. R79 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	REF0_MISSCLK_EN	R/W	0x1	REF0 Missing Clock Detect Enable ROM=Y, EEPROM=N
0	REF0_AMPDET_EN	R/W	0x0	REF0 Amplitude Detect Enable ROM=Y, EEPROM=N

1.65 R80 Register (Offset = 0x50) [Reset = 0xE]

R80 is shown in Table 1-67.

Return to the Summary Table.

Table 1-67. R80 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF1_EARLY_DET_EN	R/W	0x0	REF1 Early Clock Detect Enable ROM=Y, EEPROM=N
4	REF1_PH_VALID_EN	R/W	0x0	REF1 Phase Validation Enable ROM=Y, EEPROM=N
3	REF1_VALTMR_EN	R/W	0x1	REF1 Validation Timer Enable ROM=Y, EEPROM=N
2	REF1_PPM_EN	R/W	0x1	REF1 Freq ppm Enable ROM=Y, EEPROM=N
1	REF1_MISSCLK_EN	R/W	0x1	REF1 Missing Clock Detect Enable ROM=Y, EEPROM=N
0	REF1_AMPDET_EN	R/W	0x0	REF1 Amplitude Detect Enable ROM=Y, EEPROM=N

1.66 R83 Register (Offset = 0x53) [Reset = 0x8]

R83 is shown in Table 1-68.

Return to the Summary Table.

Table 1-68. R83 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:2	REF1_DET_CLK_DIV	R/W	0x2	REF1 Clock Detector Divider. Bit 0 controls the divide value (0=Div4, 1=Div16). Bit 1, if set, causes the divider to be bypassed. ROM=Y, EEPROM=N 0x0 = Div By 4 0x1 = Div By 16 0x2 = Bypass 0x3 = Bypass (Reserved)
1:0	REF0_DET_CLK_DIV	R/W	0x0	REF0 Clock Detector Divider. Bit 0 controls the divide value (0=Div4, 1=Div16). Bit 1, if set, causes the divider to be bypassed. ROM=Y, EEPROM=N 0x0 = Div By 4 0x1 = Div By 16 0x2 = Bypass 0x3 = Bypass (Reserved)

1.67 R84 Register (Offset = 0x54) [Reset = 0x0]

R84 is shown in Table 1-69.

Return to the Summary Table.

Table 1-69. R84 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF0_MISSCLK_DIV_21:16	R/W	0x0	See Register 86

1.68 R85 Register (Offset = 0x55) [Reset = 0x0]

R85 is shown in Table 1-70.

Return to the Summary Table.

Table 1-70. R85 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_MISSCLK_DIV_15:8	R/W	0x0	See Register 86

1.69 R86 Register (Offset = 0x56) [Reset = 0x14]

R86 is shown in Table 1-71.

Return to the Summary Table.

Table 1-71. R86 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_MISSCLK_DIV	R/W	0x14	REF0 Missing Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO3/2 to REF0 or VCO2/5 to REF0 (determined by REF0_MISSCLK_VCOSEL selection) with some offset added for upper bound. ROM=Y, EEPROM=N

1.70 R87 Register (Offset = 0x57) [Reset = 0x0]

R87 is shown in Table 1-72.

Return to the Summary Table.

Table 1-72. R87 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF1_MISSCLK_DIV_21:16	R/W	0x0	See Register 89

1.71 R88 Register (Offset = 0x58) [Reset = 0x0]

R88 is shown in Table 1-73.

Return to the Summary Table.

Table 1-73. R88 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_MISSCLK_DIV_15:8	R/W	0x0	See Register 89

1.72 R89 Register (Offset = 0x59) [Reset = 0xFA]

R89 is shown in Table 1-74.

Return to the Summary Table.

Table 1-74. R89 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_MISSCLK_DIV	R/W	0xFA	REF1 Missing Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO3/2 to REF1 or VCO2/5 to REF1 (determined by REF0_MISSCLK_VCOSEL selection) with some offset added for upper bound. ROM=Y, EEPROM=N

1.73 R96 Register (Offset = 0x60) [Reset = 0x0]

R96 is shown in Table 1-75.

Return to the Summary Table.

Table 1-75. R96 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:1	RESERVED	R	0x0	Reserved
0	REF0_MISSCLK_VCOSEL	R/W	0x0	Missing/Early Clock Detector VCO selection for all references. Also selects TOD clock source. ROM=Y, EEPROM=N 0x0 = VCO3 0x1 = VCO2

1.74 R97 Register (Offset = 0x61) [Reset = 0x0]

R97 is shown in Table 1-76.

Return to the Summary Table.

Table 1-76. R97 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF0_EARLY_CLK_DIV_21:16	R/W	0x0	See Register 99

1.75 R98 Register (Offset = 0x62) [Reset = 0x0]

R98 is shown in Table 1-77.

Return to the Summary Table.

Table 1-77. R98 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_EARLY_CLK_DIV_15:8	R/W	0x0	See Register 99

1.76 R99 Register (Offset = 0x63) [Reset = 0x3]

R99 is shown in Table 1-78.

Return to the Summary Table.

Table 1-78. R99 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_EARLY_CLK_DIV	R/W	0x3	REF0 Early Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO3/2 to REF0 or VCO2/5 to REF0 (determined by REF0_MISSCLK_VCOSEL selection) with some offset subtracted for lower bound. ROM=Y, EEPROM=N

1.77 R100 Register (Offset = 0x64) [Reset = 0x0]

R100 is shown in Table 1-79.

Return to the Summary Table.

Table 1-79. R100 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF1_EARLY_CLK_DIV_21:16	R/W	0x0	See Register 102

1.78 R101 Register (Offset = 0x65) [Reset = 0x0]

R101 is shown in Table 1-80.

Return to the Summary Table.

Table 1-80. R101 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_EARLY_CLK_DIV_15:8	R/W	0x0	See Register 102

1.79 R102 Register (Offset = 0x66) [Reset = 0x76]

R102 is shown in Table 1-81.

Return to the Summary Table.

Table 1-81. R102 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_EARLY_CLK_DIV	R/W	0x76	REF1 Early Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO3/2 to REF1 or VCO2/5 to REF1 (determined by REF0_MISSCLK_VCOSEL selection) with some offset subtracted for lower bound. ROM=Y, EEPROM=N

1.80 R109 Register (Offset = 0x6D) [Reset = 0x0]

R109 is shown in Table 1-82.

Return to the Summary Table.

Table 1-82. R109 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF0_PPM_MIN_14:8	R/W	0x0	See Register 110

1.81 R110 Register (Offset = 0x6E) [Reset = 0x1E]

R110 is shown in Table 1-83.

Return to the Summary Table.

Table 1-83. R110 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_PPM_MIN	R/W	0x1E	REF0 Frequency PPM Lower Limit ROM=Y, EEPROM=N

1.82 R111 Register (Offset = 0x6F) [Reset = 0x0]

R111 is shown in Table 1-84.

Return to the Summary Table.

Table 1-84. R111 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF0_PPM_MAX_14:8	R/W	0x0	See Register 112

1.83 R112 Register (Offset = 0x70) [Reset = 0x2D]

R112 is shown in Table 1-85.

Return to the Summary Table.

Table 1-85. R112 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_PPM_MAX	R/W	0x2D	REF0 Frequency PPM Upper Limit ROM=Y, EEPROM=N

1.84 R113 Register (Offset = 0x71) [Reset = 0x0]

R113 is shown in Table 1-86.

Return to the Summary Table.

Table 1-86. R113 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF1_PPM_MIN_14:8	R/W	0x0	See Register 114

1.85 R114 Register (Offset = 0x72) [Reset = 0x14]

R114 is shown in Table 1-87.

Return to the Summary Table.

Table 1-87. R114 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_PPM_MIN	R/W	0x14	REF1 Frequency PPM Lower Limit ROM=Y, EEPROM=N

1.86 R115 Register (Offset = 0x73) [Reset = 0x0]

R115 is shown in Table 1-88.

Return to the Summary Table.

Table 1-88. R115 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF1_PPM_MAX_14:8	R/W	0x0	See Register 116

1.87 R116 Register (Offset = 0x74) [Reset = 0x1E]

R116 is shown in Table 1-89.

Return to the Summary Table.

Table 1-89. R116 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_PPM_MAX	R/W	0x1E	REF1 Frequency PPM Upper Limit ROM=Y, EEPROM=N

1.88 R157 Register (Offset = 0x9D) [Reset = 0xE]

R157 is shown in Table 1-90.

Return to the Summary Table.

Table 1-90. R157 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	REF0VLDTMR	R/W	0xE	REF0 Validation Timer. All selected validations must be valid for selected amount of time before the IN0/REF0 is considered valid. ROM=Y, EEPROM=N 0x0 = 0.1 ms 0x1 = 0.2 ms 0x2 = 0.4 ms 0x3 = 0.8 ms 0x4 = 1.6 ms 0x5 = 3.2 ms 0x6 = 6.4 ms 0x7 = 12.8 ms 0x8 = 25.6 ms 0x9 = 51.2 ms 0xA = 102.4 ms 0xB = 204.8 ms 0xC = 409.6 ms 0xD = 819.2 ms 0xE = 1.6 s 0xF = 3.3 s 0x10 = 6.6 s 0x11 = 13.1 s 0x12 = 26.2 s 0x13 = 52.4 s 0x14 = 1.7 min 0x15 = 3.5 min 0x16 = 7.0 min 0x17 = 14.0 min 0x18 = 28.0 min 0x19 = 55.9 min 0x1A = 1.9 hr 0x1B = 3.7 hr 0x1C = 7.5 hr 0x1D = 14.9 hr 0x1E = 29.8 hr 0x1F = 59.7 hr

1.89 R158 Register (Offset = 0x9E) [Reset = 0xE]

R158 is shown in Table 1-91.

Return to the Summary Table.

Table 1-91. R158 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	REF1VLDTMR	R/W	0xE	REF1 Validation Timer. All selected validations must be valid for selected amount of time before the IN1/REF1 is considered valid. ROM=Y, EEPROM=N 0x0 = 0.1 ms 0x1 = 0.2 ms 0x2 = 0.4 ms 0x3 = 0.8 ms 0x4 = 1.6 ms 0x5 = 3.2 ms 0x6 = 6.4 ms 0x7 = 12.8 ms 0x8 = 25.6 ms 0x9 = 51.2 ms 0xA = 102.4 ms 0xB = 204.8 ms 0xC = 409.6 ms 0xD = 819.2 ms 0xE = 1.6 s 0xF = 3.3 s 0x10 = 6.6 s 0x11 = 13.1 s 0x12 = 26.2 s 0x13 = 52.4 s 0x14 = 1.7 min 0x15 = 3.5 min 0x16 = 7.0 min 0x17 = 14.0 min 0x18 = 28.0 min 0x19 = 55.9 min 0x1A = 1.9 hr 0x1B = 3.7 hr 0x1C = 7.5 hr 0x1D = 14.9 hr 0x1E = 29.8 hr 0x1F = 59.7 hr

1.90 R161 Register (Offset = 0xA1) [Reset = 0x0]

R161 is shown in Table 1-92.

Return to the Summary Table.

Table 1-92. R161 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF0_PH_VALID_THR_13:8	R/W	0x0	REF0 Phase Validation Threshold ROM=Y, EEPROM=N

1.91 R162 Register (Offset = 0xA2) [Reset = 0x0]

R162 is shown in Table 1-93.

Return to the Summary Table.

Table 1-93. R162 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_PH_VALID_THR	R/W	0x0	REF0 Phase Validation Threshold ROM=Y, EEPROM=N

1.92 R163 Register (Offset = 0xA3) [Reset = 0x0]

R163 is shown in Table 1-94.

Return to the Summary Table.

Table 1-94. R163 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF1_PH_VALID_THR_13:8	R/W	0x0	REF1 Phase Validation Threshold ROM=Y, EEPROM=N

1.93 R164 Register (Offset = 0xA4) [Reset = 0x0]

R164 is shown in Table 1-95.

Return to the Summary Table.

Table 1-95. R164 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_PH_VALID_THR	R/W	0x0	REF1 Phase Validation Threshold ROM=Y, EEPROM=N

1.94 R170 Register (Offset = 0xAA) [Reset = 0x0]

R170 is shown in Table 1-96.

Return to the Summary Table.

Table 1-96. R170 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMSCRC	R	0x0	NVM Stored CRC ROM=N, EEPROM=N

1.95 R171 Register (Offset = 0xAB) [Reset = 0x0]

R171 is shown in Table 1-97.

Return to the Summary Table.

Table 1-97. R171 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	REGCOMMIT	R/WSC	0x0	Copy fields which also exist in SRAM to SRAM memory. The REGCOMMIT bit is automatically cleared to 0 when the transfer is complete. Next an EEPROM programming operation may be performed to update NVM EEPROM. When programming to alter an NVM profile, it is suggested to toggle PD# to assure default conditions, change the desired fields, then assert the REGCOMMIT bit. ROM=N, EEPROM=N

Table 1-97. R171 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	NVMCRCERR	R	0x0	NVM CRC Error Indication. The NVMCRCERR bit is set to 1 if a CRC Error has been detected when reading back from on-chip EEPROM during device configuration. ROM=N, EEPROM=N
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	NVMBUSY	R	0x0	NVM Program Busy Indication. The NVMBUSY bit is 1 during an on-chip EEPROM Erase/Program cycle. While NVMBUSY is 1 the on-chip EEPROM cannot be accessed. Toggling PD# or removing power while NVMBUSY is asserted will corrupt the EEPROM. ROM=N, EEPROM=N
1	NVMERASE	R/WSC	0x0	NVM Erase Start. The NVMERASE bit is used to begin an on-chip EEPROM Erase cycle. The Erase cycle is only initiated if the immediately preceding I2C/SMBus transaction was a write to the NVMUNLK register withthe appropriate code. The NVMERASE bit is automatically cleared to 0.
0	NVMPROG	R/WSC	0x0	NVM Program Start. The NVMPROG bit is used to begin an on-chip EEPROM Program cycle. The Program cycle is only initiated if the immediately preceding I2C/SMBus transaction was a write to the NVMUNLK register withthe appropriate code. The NVMPROG bit is automatically cleared to 0.

1.96 R173 Register (Offset = 0xAD) [Reset = 0x0]

R173 is shown in Table 1-98.

Return to the Summary Table.

Table 1-98. R173 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	MEMADR_12:8	R/W	0x0	See Register 174 0x0 = MEMADR[8:0], NVMDAT 0x1 = MEMADR[8:0], RAMDAT 0x2 = MEMADR[12:0], ROMDAT

1.97 R174 Register (Offset = 0xAE) [Reset = 0x0]

R174 is shown in Table 1-99.

Return to the Summary Table.

Table 1-99. R174 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	MEMADR	R/W	0x0	Memory Address. The MEMADR value determines the starting address for access to the on-chip memories. This same MEMADR value is used for EEPROM and SRAM access which share the same memory map and also ROM access. The NVMDAT field is used to read and write from EEPROM. The RAMDAT field is used to read and write from SRAM. The ROMDAT field is used to read and write from ROM. ROM=N, EEPROM=N

1.98 R176 Register (Offset = 0xB0) [Reset = 0x40]

R176 is shown in Table 1-100.

Return to the Summary Table.

Table 1-100. R176 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RAMDAT	R/W	0x40	RAM Read/Write Data. The first time an I2C/SMBus read or write transaction accesses the RAMDAT register address, either because it was explicitly targeted or because the address was auto-incremented, a readtransaction will return the RAM data located at the address specified by the MEMADR register and a writetransaction will cause the current I2C/SMBus data to be written to the address specified by the MEMADR register.Any additional accesses which are part of the same transaction will cause the RAM address to be incremented anda read or write access will take place to the next SRAM address. The I2C/SMBus address will no longerbe auto-incremented, i.e the I2C/SMBus address will be locked to the RAMDAT register after the first access.Access to the RAMDAT register will terminate at the end of the current I2C/SMBus transaction. ROM=N, EEPROM=N

1.99 R180 Register (Offset = 0xB4) [Reset = 0x0]

R180 is shown in Table 1-101.

Return to the Summary Table.

Table 1-101. R180 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMUNLK	R/W	0x0	NVM Prog Unlock. The NVMUNLK register must be written immediately prior to setting the NVMERASE and NVMPROG bit, otherwise the Erase/Program cycle will not be triggered. NVMUNLK must be written with a value of 0xEA. ROM=N, EEPROM=N

1.100 R222 Register (Offset = 0xDE) [Reset = 0x0]

R222 is shown in Table 1-102.

Return to the Summary Table.

Table 1-102. R222 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	STATUS_MUX_DIV2_EN	R/W	0x0	Enable all DivideBy2 clocks for Status MUX debug signals ROM=N, EEPROM=N
5:0	RESERVED	R	0x0	Reserved

1.101 R223 Register (Offset = 0xDF) [Reset = 0x0]

R223 is shown in Table 1-103.

Return to the Summary Table.

Table 1-103. R223 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-103. R223 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:3	DPLL1_REF0_AUTO_PRTY	R/W	0x0	REF0 Priority for Automatic Switchover. Sets the priority for REF0 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL1_REF1_AUTO_PRTY	R/W	0x0	REF1 Priority for Automatic Switchover. Sets the priority for REF1 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.102 R225 Register (Offset = 0xE1) [Reset = 0x0]

R225 is shown in Table 1-104.

Return to the Summary Table.

Table 1-104. R225 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL1_REF4_AUTO_PRTY	R/W	0x0	REF4 Priority for Automatic Switchover. Sets the priority for REF4 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL1_REF5_AUTO_PRTY	R/W	0x0	REF5 Priority for Automatic Switchover. Sets the priority for REF5 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.103 R226 Register (Offset = 0xE2) [Reset = 0x1]

R226 is shown in Table 1-105.

Return to the Summary Table.

Table 1-105. R226 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL1_MAN_REFSEL	R/W	0x0	DPLL1 Manual Reference Selection Mode. Determines how the manually selected reference is chosen. If this is set to a '1', the manually selected reference is taken from a GPIO input pin. If it is set to a '0', the manually selected reference is taken from ROM=Y, EEPROM=N 0x0 = REF0 0x1 = REF1 0x2 = Reserved 0x3 = Reserved 0x4 = PLL2 0x5 = PLL3
2	DPLL1_MAN_SWITCH_PIN_MODE	R/W	0x0	DPLL1 Manual Reference Selection Mode. Determines how the manually selected reference is chosen. If this is set to a '1', the manually selected reference is taken from a GPIO input pin. If it is set to a '0', the manually selected reference is taken from a register. ROM=Y, EEPROM=N 0x0 = Register 0x1 = Pin
1:0	DPLL1_SWITCH_MODE	R/W	0x1	DPLL1 Reference Switchover Mode. Selects between Automatic Non-revertive, Automatic Revertive, Manual Selection with Automatic Fallback, and Manual Selection with Automatic Holdover. ROM=Y, EEPROM=N 0x0 = Auto Non-revertive 0x1 = Auto Revertive 0x2 = Manual w/ Fallback 0x3 = Manual w/ Holdover

1.104 R227 Register (Offset = 0xE3) [Reset = 0x0]

R227 is shown in Table 1-106.

Return to the Summary Table.

Table 1-106. R227 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_REFSEL_STAT	R	0x0	Reports the DPLL1 selected reference ROM=N, EEPROM=N 0x0 = Holdover 0x1 = REF0 0x2 = REF1 0x4 = Reserved 0x8 = Reserved 0x10 = APLL2 0x20 = APLL3

1.105 R228 Register (Offset = 0xE4) [Reset = 0x0]

R228 is shown in Table 1-107.

Return to the Summary Table.

Table 1-107. R228 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL1_LOCKDET_PPM_EN	R/W	0x0	DPLL frequency lock detect enable ROM=Y, EEPROM=N

Table 1-107. R228 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	DPLL1_LOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 229

1.106 R229 Register (Offset = 0xE5) [Reset = 0x5A]

R229 is shown in Table 1-108.

Return to the Summary Table.

Table 1-108. R229 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_PPM_MAX	R/W	0x5A	DPLL frequency lock detect in-lock threshhold ROM=Y, EEPROM=N

1.107 R230 Register (Offset = 0xE6) [Reset = 0x0]

R230 is shown in Table 1-109.

Return to the Summary Table.

Table 1-109. R230 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	DPLL1_UNLOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 231

1.108 R231 Register (Offset = 0xE7) [Reset = 0x78]

R231 is shown in Table 1-110.

Return to the Summary Table.

Table 1-110. R231 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_UNLOCKDET_PPM_MAX	R/W	0x78	DPLL frequency lock detect out-of-lock threshhold ROM=Y, EEPROM=N

1.109 R232 Register (Offset = 0xE8) [Reset = 0x0]

R232 is shown in Table 1-111.

Return to the Summary Table.

Table 1-111. R232 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_LOCKDET2_PPM_CNTSTRT_29:24	R/W	0x0	See Register 235

1.110 R233 Register (Offset = 0xE9) [Reset = 0x1]

R233 is shown in Table 1-112.

Return to the Summary Table.

Table 1-112. R233 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET2_PPM_CNTSTRT_23:16	R/W	0x1	See Register 235

1.111 R234 Register (Offset = 0xEA) [Reset = 0x86]

R234 is shown in Table 1-113.

Return to the Summary Table.

Table 1-113. R234 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET2_PPM_CNTSTRT_15:8	R/W	0x86	See Register 235

1.112 R235 Register (Offset = 0xEB) [Reset = 0xA0]

R235 is shown in Table 1-114.

Return to the Summary Table.

Table 1-114. R235 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET2_PPM_CNTSTRT	R/W	0xA0	DPLL frequency lock detect reference count value used with DPLL1 feedback configuration 2 ROM=Y, EEPROM=N

1.113 R236 Register (Offset = 0xEC) [Reset = 0x0]

R236 is shown in Table 1-115.

Return to the Summary Table.

Table 1-115. R236 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_LOCKDET_PPM_CNTSTRT_29:24	R/W	0x0	See Register 239

1.114 R237 Register (Offset = 0xED) [Reset = 0x1]

R237 is shown in Table 1-116.

Return to the Summary Table.

Table 1-116. R237 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_PPM_CNTSTRT_23:16	R/W	0x1	See Register 239

1.115 R238 Register (Offset = 0xEE) [Reset = 0x77]

R238 is shown in Table 1-117.

Return to the Summary Table.

Table 1-117. R238 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_PPM_CNTSTRT_15:8	R/W	0x77	See Register 239

1.116 R239 Register (Offset = 0xEF) [Reset = 0x0]

R239 is shown in Table 1-118.

Return to the Summary Table.

Table 1-118. R239 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_PPM_CNTSTRT	R/W	0x0	DPLL frequency lock detect reference count value used with DPLL1 feedback configuration 1 ROM=Y, EEPROM=N

1.117 R240 Register (Offset = 0xF0) [Reset = 0x0]

R240 is shown in Table 1-119.

Return to the Summary Table.

Table 1-119. R240 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_LOCKDET_VCO_PPM_CNTSTRT_29:24	R/W	0x0	See Register 243

1.118 R241 Register (Offset = 0xF1) [Reset = 0xF]

R241 is shown in Table 1-120.

Return to the Summary Table.

Table 1-120. R241 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_VCO_PPM_CNTSTRT_23:16	R/W	0xF	See Register 243

1.119 R242 Register (Offset = 0xF2) [Reset = 0x42]

R242 is shown in Table 1-121.

Return to the Summary Table.

Table 1-121. R242 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_VCO_PPM_CNTSTRT_15:8	R/W	0x42	See Register 243

1.120 R243 Register (Offset = 0xF3) [Reset = 0x40]

R243 is shown in Table 1-122.

Return to the Summary Table.

Table 1-122. R243 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_VCO_PPM_CNTSTRT	R/W	0x40	DPLL frequency lock detect VCO count value ROM=Y, EEPROM=N

1.121 R244 Register (Offset = 0xF4) [Reset = 0x0]

R244 is shown in Table 1-123.

Return to the Summary Table.

Table 1-123. R244 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:1	RESERVED	R	0x0	Reserved
0	DPLL1_STATUS_PPM_LOCK	R	0x0	Readback lock indicator from DPLL PPM Checker ROM=N, EEPROM=N

1.122 R247 Register (Offset = 0xF7) [Reset = 0x4]

R247 is shown in Table 1-124.

Return to the Summary Table.

Table 1-124. R247 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL1_LOOP_EN	R/W	0x0	Enable DPLL1 loop filter and R-Div mash engine ROM=Y, EEPROM=N
6	DPLL1_PHASE_CANCEL_EN	R/W	0x0	Enable Phase Cancellation ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4	DPLL1_PHS1_EN	R/W	0x0	Enable Phase Slew control type 1 ROM=Y, EEPROM=N
3	DPLL1_ZDM_EN	R/W	0x0	Enable Zero Delay ROM=Y, EEPROM=N
2	DPLL1_HIST_EN	R/W	0x1	Enable History word to be used during holdover ROM=Y, EEPROM=N
1:0	RESERVED	R	0x0	Reserved

1.123 R248 Register (Offset = 0xF8) [Reset = 0x4]

R248 is shown in Table 1-125.

Return to the Summary Table.

Table 1-125. R248 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL1_HOLD_SLEW_LIM_EN	R/W	0x0	Enable slew limiter when entering holdover. Allows slew rate control between current DPLL value before entering holdover and history value. ROM=Y, EEPROM=N
6	RESERVED	R	0x0	Reserved
5:3	RESERVED	R	0x0	Reserved
2	DPLL1_CLK_DIV_SRC_SEL	R/W	0x1	DPLL1 cannot be used without DPLL2 or DPLL3 operating. DPLL1 clock select 0x0 = DPLL3 0x1 = DPLL2

Table 1-125. R248 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	RESERVED	R	0x0	Reserved

1.124 R250 Register (Offset = 0xFA) [Reset = 0x0]

R250 is shown in Table 1-126.

Return to the Summary Table.

Table 1-126. R250 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL1_PH_OFFSET_44:40	R/W	0x0	See Register 255

1.125 R251 Register (Offset = 0xFB) [Reset = 0x0]

R251 is shown in Table 1-127.

Return to the Summary Table.

Table 1-127. R251 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_PH_OFFSET_39:32	R/W	0x0	See Register 255

1.126 R252 Register (Offset = 0xFC) [Reset = 0x0]

R252 is shown in Table 1-128.

Return to the Summary Table.

Table 1-128. R252 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_PH_OFFSET_31:24	R/W	0x0	See Register 255

1.127 R253 Register (Offset = 0xFD) [Reset = 0x0]

R253 is shown in Table 1-129.

Return to the Summary Table.

Table 1-129. R253 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_PH_OFFSET_23:16	R/W	0x0	See Register 255

1.128 R254 Register (Offset = 0xFE) [Reset = 0x0]

R254 is shown in Table 1-130.

Return to the Summary Table.

Table 1-130. R254 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_PH_OFFSET_15:8	R/W	0x0	See Register 255

1.129 R255 Register (Offset = 0xFF) [Reset = 0x0]

R255 is shown in Table 1-131.

Return to the Summary Table.

Table 1-131. R255 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_PH_OFFSET	R/W	0x0	Phase offset to control input to output phase in ZDM. ROM=Y, EEPROM=N

1.130 R256 Register (Offset = 0x100) [Reset = 0x0]

R256 is shown in Table 1-132.

Return to the Summary Table.

Table 1-132. R256 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FREE_RUN_39:32	R/W	0x0	See Register 260

1.131 R257 Register (Offset = 0x101) [Reset = 0x0]

R257 is shown in Table 1-133.

Return to the Summary Table.

Table 1-133. R257 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FREE_RUN_31:24	R/W	0x0	See Register 260

1.132 R258 Register (Offset = 0x102) [Reset = 0x0]

R258 is shown in Table 1-134.

Return to the Summary Table.

Table 1-134. R258 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FREE_RUN_23:16	R/W	0x0	See Register 260

1.133 R259 Register (Offset = 0x103) [Reset = 0x0]

R259 is shown in Table 1-135.

Return to the Summary Table.

Table 1-135. R259 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FREE_RUN_15:8	R/W	0x0	See Register 260

1.134 R260 Register (Offset = 0x104) [Reset = 0x0]

R260 is shown in Table 1-136.

Return to the Summary Table.

Table 1-136. R260 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FREE_RUN	R/W	0x0	DPLL1 starting word. Also non-history holdover word. ROM=Y, EEPROM=N

1.135 R290 Register (Offset = 0x122) [Reset = 0x1]

R290 is shown in Table 1-137.

Return to the Summary Table.

Table 1-137. R290 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL1_LCK_TIMER_9:8	R/W	0x1	See Register 291

1.136 R291 Register (Offset = 0x123) [Reset = 0x88]

R291 is shown in Table 1-138.

Return to the Summary Table.

Table 1-138. R291 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LCK_TIMER	R/W	0x88	Minimum amount of time until DPLL1_LOPL will be deasserted after starting to lock. Timer begins once device is within valid phase lock window. ROM=Y, EEPROM=N

1.137 R294 Register (Offset = 0x126) [Reset = 0x1]

R294 is shown in Table 1-139.

Return to the Summary Table.

Table 1-139. R294 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R	0x0	Reserved
1:0	DPLL1_HOLD_TIMER_9:8	R/W	0x1	See Register 295

1.138 R295 Register (Offset = 0x127) [Reset = 0x42]

R295 is shown in Table 1-140.

Return to the Summary Table.

Table 1-140. R295 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_HOLD_TIMER	R/W	0x42	Rate of change to DPLL or APLL numerator during phase slew control. See DPLLx_HOLD_SLEW_STEP. ROM=Y, EEPROM=N

1.139 R296 Register (Offset = 0x128) [Reset = 0x1]

R296 is shown in Table 1-141.

Return to the Summary Table.

Table 1-141. R296 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL1_PHS1_TIMER_9:8	R/W	0x1	See Register 297

1.140 R297 Register (Offset = 0x129) [Reset = 0x40]

R297 is shown in Table 1-142.

Return to the Summary Table.

Table 1-142. R297 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_PHS1_TIMER	R/W	0x40	Phase slew control update timer. ROM=Y, EEPROM=N

1.141 R303 Register (Offset = 0x12F) [Reset = 0x26]

R303 is shown in Table 1-143.

Return to the Summary Table.

Table 1-143. R303 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_PL_THRESH	R/W	0x26	Phase lock in-lock threshold ROM=Y, EEPROM=N

1.142 R304 Register (Offset = 0x130) [Reset = 0x27]

R304 is shown in Table 1-144.

Return to the Summary Table.

Table 1-144. R304 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_PL_UNLK_THRESH	R/W	0x27	Phase lock out-of-lock threshold ROM=Y, EEPROM=N

1.143 R305 Register (Offset = 0x131) [Reset = 0x7]

R305 is shown in Table 1-145.

Return to the Summary Table.

Table 1-145. R305 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_PHS1_THRESH	R/W	0x7	Phase slew type 1 threshold ROM=Y, EEPROM=N

1.144 R308 Register (Offset = 0x134) [Reset = 0x0]

R308 is shown in Table 1-146.

Return to the Summary Table.

Table 1-146. R308 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_HOLD_SLEW_STEP	R/W	0x0	When DPLL exits holdover, rate of phase change relates to DPLLx_HOLD_SLEW_STEP over DPLLx_HOLD_TIMER. DPLLx_HOLD_SLEW_STEP is applied to DPLL numerator when exiting holdover or APLL numerator when using APLL relative DCO. ROM=Y, EEPROM=N

1.145 R310 Register (Offset = 0x136) [Reset = 0x0]

R310 is shown in Table 1-147.

Return to the Summary Table.

Table 1-147. R310 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	DPLL1_STATUS_PL	R	0x0	Readback the phase lock status ROM=N, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.146 R311 Register (Offset = 0x137) [Reset = 0x0]

R311 is shown in Table 1-148.

Return to the Summary Table.

Table 1-148. R311 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	DPLL1_DCO_SLEW_ACTIVE	R	0x0	Readback DCO slew status ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.147 R314 Register (Offset = 0x13A) [Reset = 0x0]

R314 is shown in Table 1-149.

Return to the Summary Table.

Table 1-149. R314 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved

Table 1-149. R314 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DPLL1_FB_DIV_32:32	R/W	0x0	See Register 318

1.148 R315 Register (Offset = 0x13B) [Reset = 0x0]

R315 is shown in Table 1-150.

Return to the Summary Table.

Table 1-150. R315 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DIV_31:24	R/W	0x0	See Register 318

1.149 R316 Register (Offset = 0x13C) [Reset = 0x0]

R316 is shown in Table 1-151.

Return to the Summary Table.

Table 1-151. R316 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DIV_23:16	R/W	0x0	See Register 318

1.150 R317 Register (Offset = 0x13D) [Reset = 0x1]

R317 is shown in Table 1-152.

Return to the Summary Table.

Table 1-152. R317 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DIV_15:8	R/W	0x1	See Register 318

1.151 R318 Register (Offset = 0x13E) [Reset = 0xF4]

R318 is shown in Table 1-153.

Return to the Summary Table.

Table 1-153. R318 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DIV	R/W	0xF4	DPLL Feedback Divider N Value used with DPLL1 feedback configuration 1 ROM=Y, EEPROM=N

1.152 R319 Register (Offset = 0x13F) [Reset = 0x0]

R319 is shown in Table 1-154.

Return to the Summary Table.

Table 1-154. R319 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_39:32	R/W	0x0	See Register 323

1.153 R320 Register (Offset = 0x140) [Reset = 0x0]

R320 is shown in Table 1-155.

Return to the Summary Table.

Table 1-155. R320 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_31:24	R/W	0x0	See Register 323

1.154 R321 Register (Offset = 0x141) [Reset = 0x0]

R321 is shown in Table 1-156.

Return to the Summary Table.

Table 1-156. R321 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_23:16	R/W	0x0	See Register 323

1.155 R322 Register (Offset = 0x142) [Reset = 0x0]

R322 is shown in Table 1-157.

Return to the Summary Table.

Table 1-157. R322 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_15:8	R/W	0x0	See Register 323

1.156 R323 Register (Offset = 0x143) [Reset = 0x0]

R323 is shown in Table 1-158.

Return to the Summary Table.

Table 1-158. R323 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM	R/W	0x0	DPLL Feedback Divider Numerator Value used with DPLL1 feedback configuration 1 ROM=Y, EEPROM=N

1.157 R324 Register (Offset = 0x144) [Reset = 0x0]

R324 is shown in Table 1-159.

Return to the Summary Table.

Table 1-159. R324 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DEN_39:32	R/W	0x0	See Register 328

1.158 R325 Register (Offset = 0x145) [Reset = 0x0]

R325 is shown in Table 1-160.

Return to the Summary Table.

Table 1-160. R325 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DEN_31:24	R/W	0x0	See Register 328

1.159 R326 Register (Offset = 0x146) [Reset = 0x0]

R326 is shown in Table 1-161.

Return to the Summary Table.

Table 1-161. R326 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DEN_23:16	R/W	0x0	See Register 328

1.160 R327 Register (Offset = 0x147) [Reset = 0x0]

R327 is shown in Table 1-162.

Return to the Summary Table.

Table 1-162. R327 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DEN_15:8	R/W	0x0	See Register 328

1.161 R328 Register (Offset = 0x148) [Reset = 0x0]

R328 is shown in Table 1-163.

Return to the Summary Table.

Table 1-163. R328 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DEN	R/W	0x0	DPLL Feedback Divider Denominator Value used with DPLL1 feedback configuration 1 ROM=Y, EEPROM=N

1.162 R329 Register (Offset = 0x149) [Reset = 0x0]

R329 is shown in Table 1-164.

Return to the Summary Table.

Table 1-164. R329 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL1_FB2_DIV_32:32	R/W	0x0	See Register 333

1.163 R330 Register (Offset = 0x14A) [Reset = 0x0]

R330 is shown in Table 1-165.

Return to the Summary Table.

Table 1-165. R330 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DIV_31:24	R/W	0x0	See Register 333

1.164 R331 Register (Offset = 0x14B) [Reset = 0x0]

R331 is shown in Table 1-166.

Return to the Summary Table.

Table 1-166. R331 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DIV_23:16	R/W	0x0	See Register 333

1.165 R332 Register (Offset = 0x14C) [Reset = 0x1]

R332 is shown in Table 1-167.

Return to the Summary Table.

Table 1-167. R332 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DIV_15:8	R/W	0x1	See Register 333

1.166 R333 Register (Offset = 0x14D) [Reset = 0xD8]

R333 is shown in Table 1-168.

Return to the Summary Table.

Table 1-168. R333 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DIV	R/W	0xD8	DPLL Feedback Divider N Value used with DPLL1 feedback configuration 2 ROM=Y, EEPROM=N

1.167 R334 Register (Offset = 0x14E) [Reset = 0x93]

R334 is shown in Table 1-169.

Return to the Summary Table.

Table 1-169. R334 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_NUM_39:32	R/W	0x93	See Register 338

1.168 R335 Register (Offset = 0x14F) [Reset = 0x3D]

R335 is shown in Table 1-170.

Return to the Summary Table.

Table 1-170. R335 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_NUM_31:24	R/W	0x3D	See Register 338

1.169 R336 Register (Offset = 0x150) [Reset = 0x39]

R336 is shown in Table 1-171.

Return to the Summary Table.

Table 1-171. R336 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_NUM_23:16	R/W	0x39	See Register 338

1.170 R337 Register (Offset = 0x151) [Reset = 0xEF]

R337 is shown in Table 1-172.

Return to the Summary Table.

Table 1-172. R337 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_NUM_15:8	R/W	0xEF	See Register 338

1.171 R338 Register (Offset = 0x152) [Reset = 0xF0]

R338 is shown in Table 1-173.

Return to the Summary Table.

Table 1-173. R338 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_NUM	R/W	0xF0	DPLL Feedback Divider Numerator Value used with DPLL1 feedback configuration 2 ROM=Y, EEPROM=N

1.172 R339 Register (Offset = 0x153) [Reset = 0xFF]

R339 is shown in Table 1-174.

Return to the Summary Table.

Table 1-174. R339 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DEN_39:32	R/W	0xFF	See Register 343

1.173 R340 Register (Offset = 0x154) [Reset = 0xFF]

R340 is shown in Table 1-175.

Return to the Summary Table.

Table 1-175. R340 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DEN_31:24	R/W	0xFF	See Register 343

1.174 R341 Register (Offset = 0x155) [Reset = 0x4E]

R341 is shown in Table 1-176.

Return to the Summary Table.

Table 1-176. R341 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DEN_23:16	R/W	0x4E	See Register 343

1.175 R342 Register (Offset = 0x156) [Reset = 0x93]

R342 is shown in Table 1-177.

Return to the Summary Table.

Table 1-177. R342 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DEN_15:8	R/W	0x93	See Register 343

1.176 R343 Register (Offset = 0x157) [Reset = 0x0]

R343 is shown in Table 1-178.

Return to the Summary Table.

Table 1-178. R343 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DEN	R/W	0x0	DPLL Feedback Divider Denominator Value used with DPLL1 feedback configuration 2 ROM=Y, EEPROM=N

1.177 R344 Register (Offset = 0x158) [Reset = 0x1]

R344 is shown in Table 1-179.

Return to the Summary Table.

Table 1-179. R344 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	DPLL1_REF5_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF3. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
4:2	RESERVED	R	0x0	Reserved
1	DPLL1_REF1_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF1. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
0	DPLL1_REF0_FB_SEL	R/W	0x1	DPLL Feedback N, NUM, DEN select for REF0. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2

1.178 R345 Register (Offset = 0x159) [Reset = 0x2]

R345 is shown in Table 1-180.

Return to the Summary Table.

Table 1-180. R345 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:3	RESERVED	R	0x0	Reserved

Table 1-180. R345 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	DPLL1_FB_MASH_ORDER	R/W	0x2	DPLL Feedback Divider MASH Order. ROM=Y, EEPROM=N

1.179 R346 Register (Offset = 0x15A) [Reset = 0x0]

R346 is shown in Table 1-181.

Return to the Summary Table.

Table 1-181. R346 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_FB_FDEV_37:32	R/W	0x0	See Register 350

1.180 R347 Register (Offset = 0x15B) [Reset = 0x0]

R347 is shown in Table 1-182.

Return to the Summary Table.

Table 1-182. R347 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_FDEV_31:24	R/W	0x0	See Register 350

1.181 R348 Register (Offset = 0x15C) [Reset = 0x0]

R348 is shown in Table 1-183.

Return to the Summary Table.

Table 1-183. R348 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_FDEV_23:16	R/W	0x0	See Register 350

1.182 R349 Register (Offset = 0x15D) [Reset = 0xD6]

R349 is shown in Table 1-184.

Return to the Summary Table.

Table 1-184. R349 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_FDEV_15:8	R/W	0xD6	See Register 350

1.183 R350 Register (Offset = 0x15E) [Reset = 0xC0]

R350 is shown in Table 1-185.

Return to the Summary Table.

Table 1-185. R350 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_FDEV	R/W	0xC0	DPLL Feedback Divider DCO Frequency Deviation Value ROM=Y, EEPROM=N

1.184 R351 Register (Offset = 0x15F) [Reset = 0x0]

R351 is shown in Table 1-186.

Return to the Summary Table.

Table 1-186. R351 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL1_FB_FDEV_UPDATE	R/W	0x0	Increment/Decrement DPLL Feedback Numerator value with DPLL_FB_FDEV value ROM=Y, EEPROM=N

1.185 R352 Register (Offset = 0x160) [Reset = 0x0]

R352 is shown in Table 1-187.

Return to the Summary Table.

Table 1-187. R352 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL1_FB_FDEV_EN	R/W	0x0	Enable DPLL DCO mode ROM=Y, EEPROM=N

1.186 R353 Register (Offset = 0x161) [Reset = 0x0]

R353 is shown in Table 1-188.

Return to the Summary Table.

Table 1-188. R353 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_STAT_39:32	R	0x0	See Register 357

1.187 R354 Register (Offset = 0x162) [Reset = 0x0]

R354 is shown in Table 1-189.

Return to the Summary Table.

Table 1-189. R354 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_STAT_31:24	R	0x0	See Register 357

1.188 R355 Register (Offset = 0x163) [Reset = 0x0]

R355 is shown in Table 1-190.

Return to the Summary Table.

Table 1-190. R355 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_STAT_23:16	R	0x0	See Register 357

1.189 R356 Register (Offset = 0x164) [Reset = 0x0]

R356 is shown in Table 1-191.

Return to the Summary Table.

Table 1-191. R356 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_STAT_15:8	R	0x0	See Register 357

1.190 R357 Register (Offset = 0x165) [Reset = 0x0]

R357 is shown in Table 1-192.

Return to the Summary Table.

Table 1-192. R357 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_STAT	R	0x0	Readback DPLL Feedback Divider Numerator value as a result of DCO mode ROM=N, EEPROM=N

1.191 R358 Register (Offset = 0x166) [Reset = 0x0]

R358 is shown in Table 1-193.

Return to the Summary Table.

Table 1-193. R358 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	DPLL1_REF0_DBLR_EN	R/W	0x0	DPLL Reference 0 Doubler Enable ROM=Y, EEPROM=N
2	DPLL1_REF1_DBLR_EN	R/W	0x0	DPLL Reference 1 Doubler Enable ROM=Y, EEPROM=N
1:0	RESERVED	R	0x0	Reserved

1.192 R359 Register (Offset = 0x167) [Reset = 0x0]

R359 is shown in Table 1-194.

Return to the Summary Table.

Table 1-194. R359 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF0_RDIV_15:8	R/W	0x0	See Register 360

1.193 R360 Register (Offset = 0x168) [Reset = 0xF]

R360 is shown in Table 1-195.

Return to the Summary Table.

Table 1-195. R360 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF0_RDIV	R/W	0xF	DPLL REF0 R-divider value ROM=Y, EEPROM=N

1.194 R361 Register (Offset = 0x169) [Reset = 0x0]

R361 is shown in Table 1-196.

Return to the Summary Table.

Table 1-196. R361 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF1_RDIV_15:8	R/W	0x0	See Register 362

1.195 R362 Register (Offset = 0x16A) [Reset = 0x1]

R362 is shown in Table 1-197.

Return to the Summary Table.

Table 1-197. R362 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF1_RDIV	R/W	0x1	DPLL REF1 R-divider value ROM=Y, EEPROM=N

1.196 R369 Register (Offset = 0x171) [Reset = 0x0]

R369 is shown in Table 1-198.

Return to the Summary Table.

Table 1-198. R369 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF5_RDIV_15:8	R/W	0x0	DPLL REF5 R-divider value ROM=Y, EEPROM=N

1.197 R370 Register (Offset = 0x172) [Reset = 0x0]

R370 is shown in Table 1-199.

Return to the Summary Table.

Table 1-199. R370 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF5_RDIV	R/W	0x0	DPLL REF5 R-divider value ROM=Y, EEPROM=N

1.198 R373 Register (Offset = 0x175) [Reset = 0x1]

R373 is shown in Table 1-200.

Return to the Summary Table.

Table 1-200. R373 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-200. R373 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:3	DPLL2_REF0_AUTO_PRTY	R/W	0x0	REF0 Priority for Automatic Switchover. Sets the priority for REF0 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL2_REF1_AUTO_PRTY	R/W	0x1	REF1 Priority for Automatic Switchover. Sets the priority for REF1 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.199 R375 Register (Offset = 0x177) [Reset = 0x0]

R375 is shown in Table 1-201.

Return to the Summary Table.

Table 1-201. R375 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL2_REF4_AUTO_PRTY	R/W	0x0	REF4 Priority for Automatic Switchover. Sets the priority for REF4 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL2_REF5_AUTO_PRTY	R/W	0x0	REF5 Priority for Automatic Switchover. Sets the priority for REF5 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.200 R376 Register (Offset = 0x178) [Reset = 0x1]

R376 is shown in Table 1-202.

Return to the Summary Table.

Table 1-202. R376 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL2_MAN_REFSEL	R/W	0x0	DPLL2 Manual Reference Selection ROM=Y, EEPROM=N 0x0 = REF0 0x1 = REF1 0x2 = Reserved 0x3 = Reserved 0x4 = PLL1 0x5 = PLL3
2	DPLL2_MAN_SWITCH_PIN_MODE	R/W	0x0	DPLL2 Manual Reference Selection Mode. Determines how the manually selected reference is chosen. If this is set to a '1', the manually selected reference is taken from a GPIO input pin. If it is set to a '0', the manually selected reference is taken from a register. ROM=Y, EEPROM=N 0x0 = Register 0x1 = Pin
1:0	DPLL2_SWITCH_MODE	R/W	0x1	DPLL2 Reference Switchover Mode. Selects between Automatic Non-revertive, Automatic Revertive, Manual Selection with Automatic Fallback, and Manual Selection with Automatic Holdover. ROM=Y, EEPROM=N 0x0 = Auto non-revertive 0x1 = Auto revertive 0x2 = Manual fallback 0x3 = Manual Holdover

1.201 R377 Register (Offset = 0x179) [Reset = 0x0]

R377 is shown in Table 1-203.

Return to the Summary Table.

Table 1-203. R377 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_REFSEL_STAT	R	0x0	Reads the DPLL2 selected reference ROM=N, EEPROM=N 0x0 = Holdover 0x1 = REF0 0x2 = REF1 0x4 = Reserved 0x8 = Reserved 0x10 = APLL1 0x20 = APLL3

1.202 R378 Register (Offset = 0x17A) [Reset = 0x80]

R378 is shown in Table 1-204.

Return to the Summary Table.

Table 1-204. R378 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL2_LOCKDET_PPM_EN	R/W	0x1	DPLL frequency lock detect enable ROM=Y, EEPROM=N
6:0	DPLL2_LOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 379

1.203 R379 Register (Offset = 0x17B) [Reset = 0x5A]

R379 is shown in Table 1-205.

Return to the Summary Table.

Table 1-205. R379 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_PPM_MAX	R/W	0x5A	DPLL frequency lock detect in-lock threshhold ROM=Y, EEPROM=N

1.204 R380 Register (Offset = 0x17C) [Reset = 0x0]

R380 is shown in Table 1-206.

Return to the Summary Table.

Table 1-206. R380 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	DPLL2_UNLOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 381

1.205 R381 Register (Offset = 0x17D) [Reset = 0x78]

R381 is shown in Table 1-207.

Return to the Summary Table.

Table 1-207. R381 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_UNLOCKDET_PPM_MAX	R/W	0x78	DPLL frequency lock detect out-of-lock threshhold ROM=Y, EEPROM=N

1.206 R382 Register (Offset = 0x17E) [Reset = 0x0]

R382 is shown in Table 1-208.

Return to the Summary Table.

Table 1-208. R382 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_LOCKDET2_PPM_CNTSTRT_29:24	R/W	0x0	See Register 385

1.207 R383 Register (Offset = 0x17F) [Reset = 0x1]

R383 is shown in Table 1-209.

Return to the Summary Table.

Table 1-209. R383 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET2_PPM_CNTSTRT_23:16	R/W	0x1	See Register 385

1.208 R384 Register (Offset = 0x180) [Reset = 0xB2]

R384 is shown in Table 1-210.

Return to the Summary Table.

Table 1-210. R384 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET2_PPM_CNTSTRT_15:8	R/W	0xB2	See Register 385

1.209 R385 Register (Offset = 0x181) [Reset = 0x8]

R385 is shown in Table 1-211.

Return to the Summary Table.

Table 1-211. R385 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET2_PPM_CNTSTRT	R/W	0x8	DPLL frequency lock detect reference count value used with DPLL2 feedback configuration 2 ROM=Y, EEPROM=N

1.210 R386 Register (Offset = 0x182) [Reset = 0x0]

R386 is shown in Table 1-212.

Return to the Summary Table.

Table 1-212. R386 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_LOCKDET_PPM_CNTSTRT_29:24	R/W	0x0	See Register 389

1.211 R387 Register (Offset = 0x183) [Reset = 0x1]

R387 is shown in Table 1-213.

Return to the Summary Table.

Table 1-213. R387 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_PPM_CNTSTRT_23:16	R/W	0x1	See Register 389

1.212 R388 Register (Offset = 0x184) [Reset = 0xA0]

R388 is shown in Table 1-214.

Return to the Summary Table.

Table 1-214. R388 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_PPM_CNTSTRT_15:8	R/W	0xA0	See Register 389

1.213 R389 Register (Offset = 0x185) [Reset = 0xAB]

R389 is shown in Table 1-215.

Return to the Summary Table.

Table 1-215. R389 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_PPM_CNTSTRT	R/W	0xAB	DPLL frequency lock detect reference count value used with DPLL2 feedback configuration 1 ROM=Y, EEPROM=N

1.214 R390 Register (Offset = 0x186) [Reset = 0x0]

R390 is shown in Table 1-216.

Return to the Summary Table.

Table 1-216. R390 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_LOCKDET_VCO_PPM_CNTSTRT_29:24	R/W	0x0	See Register 393

1.215 R391 Register (Offset = 0x187) [Reset = 0xF]

R391 is shown in Table 1-217.

Return to the Summary Table.

Table 1-217. R391 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_VCO_PPM_CNTSTRT_23:16	R/W	0xF	See Register 393

1.216 R392 Register (Offset = 0x188) [Reset = 0x42]

R392 is shown in Table 1-218.

Return to the Summary Table.

Table 1-218. R392 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_VCO_PPM_CNTSTRT_15:8	R/W	0x42	See Register 393

1.217 R393 Register (Offset = 0x189) [Reset = 0x43]

R393 is shown in Table 1-219.

Return to the Summary Table.

Table 1-219. R393 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_VCO_PPM_CNTSTRT	R/W	0x43	DPLL frequency lock detect VCO count value ROM=Y, EEPROM=N

1.218 R394 Register (Offset = 0x18A) [Reset = 0x0]

R394 is shown in Table 1-220.

Return to the Summary Table.

Table 1-220. R394 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:1	RESERVED	R	0x0	Reserved
0	DPLL2_STATUS_PPM_LOCK	R	0x0	Readback lock indicator from DPLL PPM Checker ROM=N, EEPROM=N

1.219 R397 Register (Offset = 0x18D) [Reset = 0xC4]

R397 is shown in Table 1-221.

Return to the Summary Table.

Table 1-221. R397 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL2_LOOP_EN	R/W	0x1	Enable DPLL2 loop filter and R-Div mash engine ROM=Y, EEPROM=N
6	DPLL2_PHASE_CANCEL_EN	R/W	0x1	Enable Phase Cancellation ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4	DPLL2_PHS1_EN	R/W	0x0	Enable Phase Slew control type 1 ROM=Y, EEPROM=N
3	DPLL2_ZDM_EN	R/W	0x0	Enable Zero Delay ROM=Y, EEPROM=N
2	DPLL2_HIST_EN	R/W	0x1	Enable History word to be used during holdover ROM=Y, EEPROM=N
1:0	RESERVED	R	0x0	Reserved

1.220 R398 Register (Offset = 0x18E) [Reset = 0x0]

R398 is shown in Table 1-222.

Return to the Summary Table.

Table 1-222. R398 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL2_HOLD_SLEW_LIM_EN	R/W	0x0	Enable slew limiter when entering holdover ROM=Y, EEPROM=N
6:0	RESERVED	R	0x0	Reserved

1.221 R400 Register (Offset = 0x190) [Reset = 0x0]

R400 is shown in Table 1-223.

Return to the Summary Table.

Table 1-223. R400 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL2_PH_OFFSET_44:40	R/W	0x0	See Register 405

1.222 R401 Register (Offset = 0x191) [Reset = 0x0]

R401 is shown in Table 1-224.

Return to the Summary Table.

Table 1-224. R401 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PH_OFFSET_39:32	R/W	0x0	See Register 405

1.223 R402 Register (Offset = 0x192) [Reset = 0x0]

R402 is shown in Table 1-225.

Return to the Summary Table.

Table 1-225. R402 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PH_OFFSET_31:24	R/W	0x0	See Register 405

1.224 R403 Register (Offset = 0x193) [Reset = 0x0]

R403 is shown in Table 1-226.

Return to the Summary Table.

Table 1-226. R403 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PH_OFFSET_23:16	R/W	0x0	See Register 405

1.225 R404 Register (Offset = 0x194) [Reset = 0x0]

R404 is shown in Table 1-227.

Return to the Summary Table.

Table 1-227. R404 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PH_OFFSET_15:8	R/W	0x0	See Register 405

1.226 R405 Register (Offset = 0x195) [Reset = 0x0]

R405 is shown in Table 1-228.

Return to the Summary Table.

Table 1-228. R405 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PH_OFFSET	R/W	0x0	Phase offset to control input to output phase in ZDM. ROM=Y, EEPROM=N

1.227 R406 Register (Offset = 0x196) [Reset = 0x0]

R406 is shown in Table 1-229.

Return to the Summary Table.

Table 1-229. R406 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FREE_RUN_39:32	R/W	0x0	See Register 410

1.228 R407 Register (Offset = 0x197) [Reset = 0x0]

R407 is shown in Table 1-230.

Return to the Summary Table.

Table 1-230. R407 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FREE_RUN_31:24	R/W	0x0	See Register 410

1.229 R408 Register (Offset = 0x198) [Reset = 0x0]

R408 is shown in Table 1-231.

Return to the Summary Table.

Table 1-231. R408 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FREE_RUN_23:16	R/W	0x0	See Register 410

1.230 R409 Register (Offset = 0x199) [Reset = 0x0]

R409 is shown in Table 1-232.

Return to the Summary Table.

Table 1-232. R409 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FREE_RUN_15:8	R/W	0x0	See Register 410

1.231 R410 Register (Offset = 0x19A) [Reset = 0x0]

R410 is shown in Table 1-233.

Return to the Summary Table.

Table 1-233. R410 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FREE_RUN	R/W	0x0	DPLL2 starting word. Also non-history holdover word. ROM=Y, EEPROM=N

1.232 R440 Register (Offset = 0x1B8) [Reset = 0x2]

R440 is shown in Table 1-234.

Return to the Summary Table.

Table 1-234. R440 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL2_LCK_TIMER_9:8	R/W	0x2	See Register 441

1.233 R441 Register (Offset = 0x1B9) [Reset = 0xB]

R441 is shown in Table 1-235.

Return to the Summary Table.

Table 1-235. R441 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LCK_TIMER	R/W	0xB	Minimum amount of time until DPLL2_LOPL will be deasserted after starting to lock. Timer begins once device is within valid phase lock window. ROM=Y, EEPROM=N

1.234 R444 Register (Offset = 0x1BC) [Reset = 0x1]

R444 is shown in Table 1-236.

Return to the Summary Table.

Table 1-236. R444 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R	0x0	Reserved
1:0	DPLL2_HOLD_TIMER_9:8	R/W	0x1	See Register 445

1.235 R445 Register (Offset = 0x1BD) [Reset = 0x42]

R445 is shown in Table 1-237.

Return to the Summary Table.

Table 1-237. R445 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_HOLD_TIMER	R/W	0x42	Rate of change to DPLL or APLL numerator during phase slew control. See DPLLx_HOLD_SLEW_STEP. ROM=Y, EEPROM=N

1.236 R446 Register (Offset = 0x1BE) [Reset = 0x1]

R446 is shown in Table 1-238.

Return to the Summary Table.

Table 1-238. R446 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL2_PHS1_TIMER_9:8	R/W	0x1	See Register 447

1.237 R447 Register (Offset = 0x1BF) [Reset = 0x40]

R447 is shown in Table 1-239.

Return to the Summary Table.

Table 1-239. R447 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PHS1_TIMER	R/W	0x40	Phase slew control update timer. ROM=Y, EEPROM=N

1.238 R453 Register (Offset = 0x1C5) [Reset = 0x29]

R453 is shown in Table 1-240.

Return to the Summary Table.

Table 1-240. R453 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_PL_THRESH	R/W	0x29	Phase lock in-lock threshold ROM=Y, EEPROM=N

1.239 R454 Register (Offset = 0x1C6) [Reset = 0x2A]

R454 is shown in Table 1-241.

Return to the Summary Table.

Table 1-241. R454 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_PL_UNLK_THRESH	R/W	0x2A	Phase lock out-of-lock threshold ROM=Y, EEPROM=N

1.240 R455 Register (Offset = 0x1C7) [Reset = 0x7]

R455 is shown in Table 1-242.

Return to the Summary Table.

Table 1-242. R455 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_PHS1_THRESH	R/W	0x7	Phase slew type 1 threshold ROM=Y, EEPROM=N

1.241 R458 Register (Offset = 0x1CA) [Reset = 0x0]

R458 is shown in Table 1-243.

Return to the Summary Table.

Table 1-243. R458 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_HOLD_SLEW_STEP	R/W	0x0	When DPLL exits holdover, rate of phase change relates to DPLLx_HOLD_SLEW_STEP over DPLLx_HOLD_TIMER. DPLLx_HOLD_SLEW_STEP is applied to DPLL numerator when exiting holdover or APLL numerator when using APLL relative DCO. ROM=Y, EEPROM=N

1.242 R460 Register (Offset = 0x1CC) [Reset = 0x0]

R460 is shown in Table 1-244.

Return to the Summary Table.

Table 1-244. R460 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	DPLL2_STATUS_PL	R	0x0	Readback the phase lock status ROM=N, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.243 R461 Register (Offset = 0x1CD) [Reset = 0x0]

R461 is shown in Table 1-245.

Return to the Summary Table.

Table 1-245. R461 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	DPLL2_DCO_SLEW_ACTIVE	R	0x0	Readback DCO slew status ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.244 R464 Register (Offset = 0x1D0) [Reset = 0x0]

R464 is shown in Table 1-246.

Return to the Summary Table.

Table 1-246. R464 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL2_FB_DIV_32:32	R/W	0x0	See Register 468

1.245 R465 Register (Offset = 0x1D1) [Reset = 0x0]

R465 is shown in Table 1-247.

Return to the Summary Table.

Table 1-247. R465 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DIV_31:24	R/W	0x0	See Register 468

1.246 R466 Register (Offset = 0x1D2) [Reset = 0x0]

R466 is shown in Table 1-248.

Return to the Summary Table.

Table 1-248. R466 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DIV_23:16	R/W	0x0	See Register 468

1.247 R467 Register (Offset = 0x1D3) [Reset = 0x2]

R467 is shown in Table 1-249.

Return to the Summary Table.

Table 1-249. R467 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DIV_15:8	R/W	0x2	See Register 468

1.248 R468 Register (Offset = 0x1D4) [Reset = 0x32]

R468 is shown in Table 1-250.

Return to the Summary Table.

Table 1-250. R468 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DIV	R/W	0x32	DPLL Feedback Divider N Value used with DPLL2 feedback configuration 1 ROM=Y, EEPROM=N

1.249 R469 Register (Offset = 0x1D5) [Reset = 0x80]

R469 is shown in Table 1-251.

Return to the Summary Table.

Table 1-251. R469 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_39:32	R/W	0x80	See Register 473

1.250 R470 Register (Offset = 0x1D6) [Reset = 0x0]

R470 is shown in Table 1-252.

Return to the Summary Table.

Table 1-252. R470 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_31:24	R/W	0x0	See Register 473

1.251 R471 Register (Offset = 0x1D7) [Reset = 0x0]

R471 is shown in Table 1-253.

Return to the Summary Table.

Table 1-253. R471 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_23:16	R/W	0x0	See Register 473

1.252 R472 Register (Offset = 0x1D8) [Reset = 0x0]

R472 is shown in Table 1-254.

Return to the Summary Table.

Table 1-254. R472 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_15:8	R/W	0x0	See Register 473

1.253 R473 Register (Offset = 0x1D9) [Reset = 0x0]

R473 is shown in Table 1-255.

Return to the Summary Table.

Table 1-255. R473 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM	R/W	0x0	DPLL Feedback Divider Numerator Value used with DPLL2 feedback configuration 1 ROM=Y, EEPROM=N

1.254 R474 Register (Offset = 0x1DA) [Reset = 0x0]

R474 is shown in Table 1-256.

Return to the Summary Table.

Table 1-256. R474 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DEN_39:32	R/W	0x0	See Register 478

1.255 R475 Register (Offset = 0x1DB) [Reset = 0x0]

R475 is shown in Table 1-257.

Return to the Summary Table.

Table 1-257. R475 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DEN_31:24	R/W	0x0	See Register 478

1.256 R476 Register (Offset = 0x1DC) [Reset = 0x0]

R476 is shown in Table 1-258.

Return to the Summary Table.

Table 1-258. R476 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DEN_23:16	R/W	0x0	See Register 478

1.257 R477 Register (Offset = 0x1DD) [Reset = 0x0]

R477 is shown in Table 1-259.

Return to the Summary Table.

Table 1-259. R477 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DEN_15:8	R/W	0x0	See Register 478

1.258 R478 Register (Offset = 0x1DE) [Reset = 0x0]

R478 is shown in Table 1-260.

Return to the Summary Table.

Table 1-260. R478 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DEN	R/W	0x0	DPLL Feedback Divider Denominator Value used with DPLL2 feedback configuration 1 ROM=Y, EEPROM=N

1.259 R479 Register (Offset = 0x1DF) [Reset = 0x0]

R479 is shown in Table 1-261.

Return to the Summary Table.

Table 1-261. R479 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL2_FB2_DIV_32:32	R/W	0x0	See Register 483

1.260 R480 Register (Offset = 0x1E0) [Reset = 0x0]

R480 is shown in Table 1-262.

Return to the Summary Table.

Table 1-262. R480 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DIV_31:24	R/W	0x0	See Register 483

1.261 R481 Register (Offset = 0x1E1) [Reset = 0x0]

R481 is shown in Table 1-263.

Return to the Summary Table.

Table 1-263. R481 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DIV_23:16	R/W	0x0	See Register 483

1.262 R482 Register (Offset = 0x1E2) [Reset = 0x2]

R482 is shown in Table 1-264.

Return to the Summary Table.

Table 1-264. R482 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DIV_15:8	R/W	0x2	See Register 483

1.263 R483 Register (Offset = 0x1E3) [Reset = 0x1C]

R483 is shown in Table 1-265.

Return to the Summary Table.

Table 1-265. R483 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DIV	R/W	0x1C	DPLL Feedback Divider N Value used with DPLL2 feedback configuration 2. ROM=Y, EEPROM=N

1.264 R484 Register (Offset = 0x1E4) [Reset = 0x0]

R484 is shown in Table 1-266.

Return to the Summary Table.

Table 1-266. R484 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_NUM_39:32	R/W	0x0	See Register 488

1.265 R485 Register (Offset = 0x1E5) [Reset = 0x0]

R485 is shown in Table 1-267.

Return to the Summary Table.

Table 1-267. R485 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_NUM_31:24	R/W	0x0	See Register 488

1.266 R486 Register (Offset = 0x1E6) [Reset = 0x0]

R486 is shown in Table 1-268.

Return to the Summary Table.

Table 1-268. R486 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_NUM_23:16	R/W	0x0	See Register 488

1.267 R487 Register (Offset = 0x1E7) [Reset = 0x0]

R487 is shown in Table 1-269.

Return to the Summary Table.

Table 1-269. R487 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_NUM_15:8	R/W	0x0	See Register 488

1.268 R488 Register (Offset = 0x1E8) [Reset = 0x0]

R488 is shown in Table 1-270.

Return to the Summary Table.

Table 1-270. R488 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_NUM	R/W	0x0	DPLL Feedback Divider Numerator Value used with DPLL2 feedback configuration 2 ROM=Y, EEPROM=N

1.269 R489 Register (Offset = 0x1E9) [Reset = 0x0]

R489 is shown in Table 1-271.

Return to the Summary Table.

Table 1-271. R489 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DEN_39:32	R/W	0x0	See Register 493

1.270 R490 Register (Offset = 0x1EA) [Reset = 0x0]

R490 is shown in Table 1-272.

Return to the Summary Table.

Table 1-272. R490 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DEN_31:24	R/W	0x0	See Register 493

1.271 R491 Register (Offset = 0x1EB) [Reset = 0x0]

R491 is shown in Table 1-273.

Return to the Summary Table.

Table 1-273. R491 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DEN_23:16	R/W	0x0	See Register 493

1.272 R492 Register (Offset = 0x1EC) [Reset = 0x0]

R492 is shown in Table 1-274.

Return to the Summary Table.

Table 1-274. R492 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DEN_15:8	R/W	0x0	See Register 493

1.273 R493 Register (Offset = 0x1ED) [Reset = 0x0]

R493 is shown in Table 1-275.

Return to the Summary Table.

Table 1-275. R493 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DEN	R/W	0x0	DPLL Feedback Divider Denominator Value used with DPLL2 feedback configuration 2 ROM=Y, EEPROM=N

1.274 R494 Register (Offset = 0x1EE) [Reset = 0x1]

R494 is shown in Table 1-276.

Return to the Summary Table.

Table 1-276. R494 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	DPLL2_REF5_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF3. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
4:2	RESERVED	R	0x0	Reserved
1	DPLL2_REF1_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF1. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
0	DPLL2_REF0_FB_SEL	R/W	0x1	DPLL Feedback N, NUM, DEN select for REF0. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2

1.275 R495 Register (Offset = 0x1EF) [Reset = 0x2]

R495 is shown in Table 1-277.

Return to the Summary Table.

Table 1-277. R495 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:3	RESERVED	R	0x0	Reserved
2:0	DPLL2_FB_MASH_ORDER	R/W	0x2	DPLL Feedback Divider MASH Order. ROM=Y, EEPROM=N

1.276 R496 Register (Offset = 0x1F0) [Reset = 0x0]

R496 is shown in Table 1-278.

Return to the Summary Table.

Table 1-278. R496 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_FB_FDEV_37:32	R/W	0x0	See Register 500

1.277 R497 Register (Offset = 0x1F1) [Reset = 0x0]

R497 is shown in Table 1-279.

Return to the Summary Table.

Table 1-279. R497 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_FDEV_31:24	R/W	0x0	See Register 500

1.278 R498 Register (Offset = 0x1F2) [Reset = 0x0]

R498 is shown in Table 1-280.

Return to the Summary Table.

Table 1-280. R498 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_FDEV_23:16	R/W	0x0	See Register 500

1.279 R499 Register (Offset = 0x1F3) [Reset = 0xF1]

R499 is shown in Table 1-281.

Return to the Summary Table.

Table 1-281. R499 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_FDEV_15:8	R/W	0xF1	See Register 500

1.280 R500 Register (Offset = 0x1F4) [Reset = 0x98]

R500 is shown in Table 1-282.

Return to the Summary Table.

Table 1-282. R500 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_FDEV	R/W	0x98	DPLL Feedback Divider DCO Frequency Deviation Value ROM=Y, EEPROM=N

1.281 R501 Register (Offset = 0x1F5) [Reset = 0x0]

R501 is shown in Table 1-283.

Return to the Summary Table.

Table 1-283. R501 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL2_FB_FDEV_UPDATE	R/W	0x0	Increment/Decrement DPLL Feedback Numerator value with DPLL_FB_FDEV value ROM=Y, EEPROM=N

1.282 R502 Register (Offset = 0x1F6) [Reset = 0x1]

R502 is shown in Table 1-284.

Return to the Summary Table.

Table 1-284. R502 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL2_FB_FDEV_EN	R/W	0x1	Enable DPLL DCO mode ROM=Y, EEPROM=N

1.283 R503 Register (Offset = 0x1F7) [Reset = 0x0]

R503 is shown in Table 1-285.

Return to the Summary Table.

Table 1-285. R503 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_STAT_39:32	R	0x0	See Register 507

1.284 R504 Register (Offset = 0x1F8) [Reset = 0x0]

R504 is shown in Table 1-286.

Return to the Summary Table.

Table 1-286. R504 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_STAT_31:24	R	0x0	See Register 507

1.285 R505 Register (Offset = 0x1F9) [Reset = 0x0]

R505 is shown in Table 1-287.

Return to the Summary Table.

Table 1-287. R505 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_STAT_23:16	R	0x0	See Register 507

1.286 R506 Register (Offset = 0x1FA) [Reset = 0x0]

R506 is shown in Table 1-288.

Return to the Summary Table.

Table 1-288. R506 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_STAT_15:8	R	0x0	See Register 507

1.287 R507 Register (Offset = 0x1FB) [Reset = 0x0]

R507 is shown in Table 1-289.

Return to the Summary Table.

Table 1-289. R507 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_STAT	R	0x0	Readback DPLL Feedback Divider Numerator value as a result of DCO mode ROM=N, EEPROM=N

1.288 R508 Register (Offset = 0x1FC) [Reset = 0x0]

R508 is shown in Table 1-290.

Return to the Summary Table.

Table 1-290. R508 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	DPLL2_REF0_DBLR_EN	R/W	0x0	DPLL Reference 0 Doubler Enable ROM=Y, EEPROM=N
2	DPLL2_REF1_DBLR_EN	R/W	0x0	DPLL Reference 1 Doubler Enable ROM=Y, EEPROM=N
1:0	RESERVED	R	0x0	Reserved

1.289 R509 Register (Offset = 0x1FD) [Reset = 0x0]

R509 is shown in Table 1-291.

Return to the Summary Table.

Table 1-291. R509 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF0_RDIV_15:8	R/W	0x0	See Register 510

1.290 R510 Register (Offset = 0x1FE) [Reset = 0xF]

R510 is shown in Table 1-292.

Return to the Summary Table.

Table 1-292. R510 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF0_RDIV	R/W	0xF	DPLL Reference 0 R divider value ROM=Y, EEPROM=N

1.291 R511 Register (Offset = 0x1FF) [Reset = 0x0]

R511 is shown in Table 1-293.

Return to the Summary Table.

Table 1-293. R511 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF1_RDIV_15:8	R/W	0x0	See Register 512

1.292 R512 Register (Offset = 0x200) [Reset = 0x1]

R512 is shown in Table 1-294.

Return to the Summary Table.

Table 1-294. R512 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF1_RDIV	R/W	0x1	DPLL Reference 1 R divider value ROM=Y, EEPROM=N

1.293 R517 Register (Offset = 0x205) [Reset = 0x0]

R517 is shown in Table 1-295.

Return to the Summary Table.

Table 1-295. R517 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF4_RDIV_15:8	R/W	0x0	See Register 518

1.294 R518 Register (Offset = 0x206) [Reset = 0x3]

R518 is shown in Table 1-296.

Return to the Summary Table.

Table 1-296. R518 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF4_RDIV	R/W	0x3	DPLL REF4 R-divider value ROM=Y, EEPROM=N

1.295 R519 Register (Offset = 0x207) [Reset = 0x0]

R519 is shown in Table 1-297.

Return to the Summary Table.

Table 1-297. R519 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF5_RDIV_15:8	R/W	0x0	See Register 520

1.296 R520 Register (Offset = 0x208) [Reset = 0x0]

R520 is shown in Table 1-298.

Return to the Summary Table.

Table 1-298. R520 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF5_RDIV	R/W	0x0	DPLL Reference 3 R divider value ROM=Y, EEPROM=N

1.297 R523 Register (Offset = 0x20B) [Reset = 0x1]

R523 is shown in Table 1-299.

Return to the Summary Table.

Table 1-299. R523 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL3_REF0_AUTO_PRTY	R/W	0x0	REF0 Priority for Automatic Switchover. Sets the priority for REF0 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

Table 1-299. R523 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	DPLL3_REF1_AUTO_PRTY	R/W	0x1	REF1 Priority for Automatic Switchover. Sets the priority for REF1 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.298 R525 Register (Offset = 0x20D) [Reset = 0x0]

R525 is shown in Table 1-300.

Return to the Summary Table.

Table 1-300. R525 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL3_REF4_AUTO_PRTY	R/W	0x0	REF4 Priority for Automatic Switchover. Sets the priority for REF4 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL3_REF5_AUTO_PRTY	R/W	0x0	REF5 Priority for Automatic Switchover. Sets the priority for REF5 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.299 R526 Register (Offset = 0x20E) [Reset = 0x1]

R526 is shown in Table 1-301.

Return to the Summary Table.

Table 1-301. R526 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-301. R526 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:3	DPLL3_MAN_REFSEL	R/W	0x0	DPLL3 Manual Reference Selection Mode. Determines how the manually selected reference is chosen. If this is set to a '1', the manually selected reference is taken from a GPIO input pin. If it is set to a '0', the manually selected reference is taken from a register. ROM=Y, EEPROM=N 0x0 = REF0 0x1 = REF1 0x2 = Reserved 0x3 = Reserved 0x4 = PLL1 0x5 = PLL2
2	DPLL3_MAN_SWITCH_PIN_MODE	R/W	0x0	DPLL3 Manual Reference Selection Mode. Determines how the manually selected reference is chosen. If this is set to a '1', the manually selected reference is taken from a GPIO input pin. If it is set to a '0', the manually selected reference is taken from a register. ROM=Y, EEPROM=N 0x0 = Register 0x1 = Pin
1:0	DPLL3_SWITCH_MODE	R/W	0x1	DPLL3 Reference Switchover Mode. Selects between Automatic Non-revertive, Automatic Revertive, Manual Selection with Automatic Fallback, and Manual Selection with Automatic Holdover. ROM=Y, EEPROM=N 0x0 = Auto non-revertive 0x1 = Auto revertive 0x2 = Manual fallback 0x3 = Manual Holdover

1.300 R527 Register (Offset = 0x20F) [Reset = 0x0]

R527 is shown in Table 1-302.

Return to the Summary Table.

Table 1-302. R527 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_REFSEL_STAT	R	0x0	Reads the DPLL3 selected reference ROM=N, EEPROM=N 0x0 = Holdover 0x1 = REF0 0x2 = REF1 0x4 = Reserved 0x8 = Reserved 0x10 = APLL1 0x20 = APLL2

1.301 R528 Register (Offset = 0x210) [Reset = 0x80]

R528 is shown in Table 1-303.

Return to the Summary Table.

Table 1-303. R528 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL3_LOCKDET_PPM_EN	R/W	0x1	DPLL frequency lock detect enable ROM=Y, EEPROM=N
6:0	DPLL3_LOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 529

1.302 R529 Register (Offset = 0x211) [Reset = 0x5A]

R529 is shown in Table 1-304.

Return to the Summary Table.

Table 1-304. R529 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_PPM_MAX	R/W	0x5A	DPLL frequency lock detect in-lock threshold ROM=Y, EEPROM=N

1.303 R530 Register (Offset = 0x212) [Reset = 0x0]

R530 is shown in Table 1-305.

Return to the Summary Table.

Table 1-305. R530 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	DPLL3_UNLOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 531

1.304 R531 Register (Offset = 0x213) [Reset = 0x78]

R531 is shown in Table 1-306.

Return to the Summary Table.

Table 1-306. R531 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_UNLOCKDET_PPM_MAX	R/W	0x78	DPLL frequency lock detect out-of-lock threshold ROM=Y, EEPROM=N

1.305 R532 Register (Offset = 0x214) [Reset = 0x0]

R532 is shown in Table 1-307.

Return to the Summary Table.

Table 1-307. R532 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_LOCKDET2_PPM_CNTSTRT_29:24	R/W	0x0	See Register 535

1.306 R533 Register (Offset = 0x215) [Reset = 0x1]

R533 is shown in Table 1-308.

Return to the Summary Table.

Table 1-308. R533 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET2_PPM_CNTSTRT_23:16	R/W	0x1	See Register 535

1.307 R534 Register (Offset = 0x216) [Reset = 0x8D]

R534 is shown in Table 1-309.

Return to the Summary Table.

Table 1-309. R534 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET2_PPM_CNTSTRT_15:8	R/W	0x8D	See Register 535

1.308 R535 Register (Offset = 0x217) [Reset = 0x5E]

R535 is shown in Table 1-310.

Return to the Summary Table.

Table 1-310. R535 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET2_PPM_CNTSTRT	R/W	0x5E	DPLL frequency lock detect reference count value used with DPLL1 feedback configuration 2 ROM=Y, EEPROM=N

1.309 R536 Register (Offset = 0x218) [Reset = 0x0]

R536 is shown in Table 1-311.

Return to the Summary Table.

Table 1-311. R536 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_LOCKDET_PPM_CNTSTRT_29:24	R/W	0x0	See Register 539

1.310 R537 Register (Offset = 0x219) [Reset = 0x1]

R537 is shown in Table 1-312.

Return to the Summary Table.

Table 1-312. R537 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_PPM_CNTSTRT_23:16	R/W	0x1	See Register 539

1.311 R538 Register (Offset = 0x21A) [Reset = 0x7D]

R538 is shown in Table 1-313.

Return to the Summary Table.

Table 1-313. R538 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_PPM_CNTSTRT_15:8	R/W	0x7D	See Register 539

1.312 R539 Register (Offset = 0x21B) [Reset = 0x79]

R539 is shown in Table 1-314.

Return to the Summary Table.

Table 1-314. R539 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_PPM_CNTSTRT	R/W	0x79	DPLL frequency lock detect reference count value used with DPLL3 feedback configuration 1 ROM=Y, EEPROM=N

1.313 R540 Register (Offset = 0x21C) [Reset = 0x0]

R540 is shown in Table 1-315.

Return to the Summary Table.

Table 1-315. R540 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_LOCKDET_VCO_PPM_CNTSTRT_29:24	R/W	0x0	See Register 543

1.314 R541 Register (Offset = 0x21D) [Reset = 0xF]

R541 is shown in Table 1-316.

Return to the Summary Table.

Table 1-316. R541 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_VCO_PPM_CNTSTRT_23:16	R/W	0xF	See Register 543

1.315 R542 Register (Offset = 0x21E) [Reset = 0x42]

R542 is shown in Table 1-317.

Return to the Summary Table.

Table 1-317. R542 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_VCO_PPM_CNTSTRT_15:8	R/W	0x42	See Register 543

1.316 R543 Register (Offset = 0x21F) [Reset = 0x48]

R543 is shown in Table 1-318.

Return to the Summary Table.

Table 1-318. R543 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_VCO_PPM_CNTSTRT	R/W	0x48	DPLL frequency lock detect VCO count value ROM=Y, EEPROM=N

1.317 R544 Register (Offset = 0x220) [Reset = 0x0]

R544 is shown in Table 1-319.

Return to the Summary Table.

Table 1-319. R544 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:1	RESERVED	R	0x0	Reserved
0	DPLL3_STATUS_PPM_LOCK	R	0x0	Readback lock indicator from DPLL PPM Checker ROM=N, EEPROM=N

1.318 R547 Register (Offset = 0x223) [Reset = 0xC4]

R547 is shown in Table 1-320.

Return to the Summary Table.

Table 1-320. R547 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL3_LOOP_EN	R/W	0x1	Enable DPLL3 loop filter and R-Div mash engine ROM=Y, EEPROM=N
6	DPLL3_PHASE_CANCEL_EN	R/W	0x1	Enable Phase Cancellation ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4	DPLL3_PHS1_EN	R/W	0x0	Enable Phase Slew control type 1 ROM=Y, EEPROM=N
3	DPLL3_ZDM_EN	R/W	0x0	Enable Zero Delay mode ROM=Y, EEPROM=N
2	DPLL3_HIST_EN	R/W	0x1	Enable History word to be used during holdover ROM=Y, EEPROM=N
1:0	RESERVED	R	0x0	Reserved

1.319 R548 Register (Offset = 0x224) [Reset = 0x0]

R548 is shown in Table 1-321.

Return to the Summary Table.

Table 1-321. R548 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL3_HOLD_SLEW_LIM_EN	R/W	0x0	During holdover enable slew limiter ROM=Y, EEPROM=N
6:0	RESERVED	R	0x0	Reserved

1.320 R550 Register (Offset = 0x226) [Reset = 0x0]

R550 is shown in Table 1-322.

Return to the Summary Table.

Table 1-322. R550 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL3_PH_OFFSET_44:40	R/W	0x0	See Register 555

1.321 R551 Register (Offset = 0x227) [Reset = 0x0]

R551 is shown in Table 1-323.

Return to the Summary Table.

Table 1-323. R551 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_PH_OFFSET_39:32	R/W	0x0	See Register 555

1.322 R552 Register (Offset = 0x228) [Reset = 0x0]

R552 is shown in Table 1-324.

Return to the Summary Table.

Table 1-324. R552 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_PH_OFFSET_31:24	R/W	0x0	See Register 555

1.323 R553 Register (Offset = 0x229) [Reset = 0x0]

R553 is shown in Table 1-325.

Return to the Summary Table.

Table 1-325. R553 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_PH_OFFSET_23:16	R/W	0x0	See Register 555

1.324 R554 Register (Offset = 0x22A) [Reset = 0x0]

R554 is shown in Table 1-326.

Return to the Summary Table.

Table 1-326. R554 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_PH_OFFSET_15:8	R/W	0x0	See Register 555

1.325 R555 Register (Offset = 0x22B) [Reset = 0x0]

R555 is shown in Table 1-327.

Return to the Summary Table.

Table 1-327. R555 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_PH_OFFSET	R/W	0x0	Phase offset to control input to output phase in ZDM. ROM=Y, EEPROM=N

1.326 R556 Register (Offset = 0x22C) [Reset = 0x0]

R556 is shown in Table 1-328.

Return to the Summary Table.

Table 1-328. R556 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FREE_RUN_39:32	R/W	0x0	See Register 560

1.327 R557 Register (Offset = 0x22D) [Reset = 0x0]

R557 is shown in Table 1-329.

Return to the Summary Table.

Table 1-329. R557 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FREE_RUN_31:24	R/W	0x0	See Register 560

1.328 R558 Register (Offset = 0x22E) [Reset = 0x0]

R558 is shown in Table 1-330.

Return to the Summary Table.

Table 1-330. R558 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FREE_RUN_23:16	R/W	0x0	See Register 560

1.329 R559 Register (Offset = 0x22F) [Reset = 0x0]

R559 is shown in Table 1-331.

Return to the Summary Table.

Table 1-331. R559 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FREE_RUN_15:8	R/W	0x0	See Register 560

1.330 R560 Register (Offset = 0x230) [Reset = 0x0]

R560 is shown in Table 1-332.

Return to the Summary Table.

Table 1-332. R560 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FREE_RUN	R/W	0x0	DPLL starting word. Also non-history holdover word. ROM=Y, EEPROM=N

1.331 R590 Register (Offset = 0x24E) [Reset = 0x3]

R590 is shown in Table 1-333.

Return to the Summary Table.

Table 1-333. R590 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL3_LCK_TIMER_9:8	R/W	0x3	See Register 591

1.332 R591 Register (Offset = 0x24F) [Reset = 0xA]

R591 is shown in Table 1-334.

Return to the Summary Table.

Table 1-334. R591 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LCK_TIMER	R/W	0xA	Minimum amount of time until DPLL3_LOPL will be deasserted after starting to lock. Timer begins once device is within valid phase lock window. ROM=Y, EEPROM=N

1.333 R594 Register (Offset = 0x252) [Reset = 0x1]

R594 is shown in Table 1-335.

Return to the Summary Table.

Table 1-335. R594 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R	0x0	Reserved
1:0	DPLL3_HOLD_TIMER_9:8	R/W	0x1	See Register 595

1.334 R595 Register (Offset = 0x253) [Reset = 0x42]

R595 is shown in Table 1-336.

Return to the Summary Table.

Table 1-336. R595 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_HOLD_TIMER	R/W	0x42	Rate of change to DPLL or APLL numerator during phase slew control. See DPLLx_HOLD_SLEW_STEP. ROM=Y, EEPROM=N

1.335 R596 Register (Offset = 0x254) [Reset = 0x1]

R596 is shown in Table 1-337.

Return to the Summary Table.

Table 1-337. R596 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL3_PHS1_TIMER_9:8	R/W	0x1	See Register 597

1.336 R597 Register (Offset = 0x255) [Reset = 0x40]

R597 is shown in Table 1-338.

Return to the Summary Table.

Table 1-338. R597 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_PHS1_TIMER	R/W	0x40	Phase slew control update timer. ROM=Y, EEPROM=N

1.337 R603 Register (Offset = 0x25B) [Reset = 0x29]

R603 is shown in Table 1-339.

Return to the Summary Table.

Table 1-339. R603 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_PL_THRESH	R/W	0x29	Phase lock in-lock threshold ROM=Y, EEPROM=N

1.338 R604 Register (Offset = 0x25C) [Reset = 0x2A]

R604 is shown in Table 1-340.

Return to the Summary Table.

Table 1-340. R604 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_PL_UNLK_THRESH	R/W	0x2A	Phase lock out-of-lock threshold ROM=Y, EEPROM=N

1.339 R605 Register (Offset = 0x25D) [Reset = 0x7]

R605 is shown in Table 1-341.

Return to the Summary Table.

Table 1-341. R605 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_PHS1_THRESH	R/W	0x7	Phase slew type 1 threshold ROM=Y, EEPROM=N

1.340 R610 Register (Offset = 0x262) [Reset = 0x0]

R610 is shown in Table 1-342.

Return to the Summary Table.

Table 1-342. R610 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	DPLL3_STATUS_PL	R	0x0	Readback the phase lock status ROM=N, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.341 R611 Register (Offset = 0x263) [Reset = 0x0]

R611 is shown in Table 1-343.

Return to the Summary Table.

Table 1-343. R611 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	DPLL3_DCO_SLEW_ACTIVE	R	0x0	Readback DCO slew status ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.342 R614 Register (Offset = 0x266) [Reset = 0x0]

R614 is shown in Table 1-344.

Return to the Summary Table.

Table 1-344. R614 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL3_FB_DIV_32:32	R/W	0x0	See Register 618

1.343 R615 Register (Offset = 0x267) [Reset = 0x0]

R615 is shown in Table 1-345.

Return to the Summary Table.

Table 1-345. R615 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DIV_31:24	R/W	0x0	See Register 618

1.344 R616 Register (Offset = 0x268) [Reset = 0x0]

R616 is shown in Table 1-346.

Return to the Summary Table.

Table 1-346. R616 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DIV_23:16	R/W	0x0	See Register 618

1.345 R617 Register (Offset = 0x269) [Reset = 0x0]

R617 is shown in Table 1-347.

Return to the Summary Table.

Table 1-347. R617 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DIV_15:8	R/W	0x0	See Register 618

1.346 R618 Register (Offset = 0x26A) [Reset = 0xF5]

R618 is shown in Table 1-348.

Return to the Summary Table.

Table 1-348. R618 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DIV	R/W	0xF5	DPLL Feedback Divider N Value used with DPLL3 feedback configuration 1 ROM=Y, EEPROM=N

1.347 R619 Register (Offset = 0x26B) [Reset = 0xC2]

R619 is shown in Table 1-349.

Return to the Summary Table.

Table 1-349. R619 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_39:32	R/W	0xC2	See Register 623

1.348 R620 Register (Offset = 0x26C) [Reset = 0x8F]

R620 is shown in Table 1-350.

Return to the Summary Table.

Table 1-350. R620 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_31:24	R/W	0x8F	See Register 623

1.349 R621 Register (Offset = 0x26D) [Reset = 0x5C]

R621 is shown in Table 1-351.

Return to the Summary Table.

Table 1-351. R621 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_23:16	R/W	0x5C	See Register 623

1.350 R622 Register (Offset = 0x26E) [Reset = 0x28]

R622 is shown in Table 1-352.

Return to the Summary Table.

Table 1-352. R622 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_15:8	R/W	0x28	See Register 623

1.351 R623 Register (Offset = 0x26F) [Reset = 0xF5]

R623 is shown in Table 1-353.

Return to the Summary Table.

Table 1-353. R623 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM	R/W	0xF5	DPLL Feedback Divider Numerator Value used with DPLL3 feedback configuration 1 ROM=Y, EEPROM=N

1.352 R624 Register (Offset = 0x270) [Reset = 0xFF]

R624 is shown in Table 1-354.

Return to the Summary Table.

Table 1-354. R624 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DEN_39:32	R/W	0xFF	See Register 628

1.353 R625 Register (Offset = 0x271) [Reset = 0xFF]

R625 is shown in Table 1-355.

Return to the Summary Table.

Table 1-355. R625 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DEN_31:24	R/W	0xFF	See Register 628

1.354 R626 Register (Offset = 0x272) [Reset = 0xFF]

R626 is shown in Table 1-356.

Return to the Summary Table.

Table 1-356. R626 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DEN_23:16	R/W	0xFF	See Register 628

1.355 R627 Register (Offset = 0x273) [Reset = 0xFF]

R627 is shown in Table 1-357.

Return to the Summary Table.

Table 1-357. R627 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DEN_15:8	R/W	0xFF	See Register 628

1.356 R628 Register (Offset = 0x274) [Reset = 0xFF]

R628 is shown in Table 1-358.

Return to the Summary Table.

Table 1-358. R628 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DEN	R/W	0xFF	DPLL Feedback Divider Denominator Value used with DPLL3 feedback configuration 1 ROM=Y, EEPROM=N

1.357 R629 Register (Offset = 0x275) [Reset = 0x0]

R629 is shown in Table 1-359.

Return to the Summary Table.

Table 1-359. R629 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL3_FB2_DIV_32:32	R/W	0x0	See Register 633

1.358 R630 Register (Offset = 0x276) [Reset = 0x0]

R630 is shown in Table 1-360.

Return to the Summary Table.

Table 1-360. R630 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DIV_31:24	R/W	0x0	See Register 633

1.359 R631 Register (Offset = 0x277) [Reset = 0x0]

R631 is shown in Table 1-361.

Return to the Summary Table.

Table 1-361. R631 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DIV_23:16	R/W	0x0	See Register 633

1.360 R632 Register (Offset = 0x278) [Reset = 0x0]

R632 is shown in Table 1-362.

Return to the Summary Table.

Table 1-362. R632 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DIV_15:8	R/W	0x0	See Register 633

1.361 R633 Register (Offset = 0x279) [Reset = 0xEB]

R633 is shown in Table 1-363.

Return to the Summary Table.

Table 1-363. R633 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DIV	R/W	0xEB	DPLL Feedback Divider N Value used with DPLL3 feedback configuration 2 ROM=Y, EEPROM=N

1.362 R634 Register (Offset = 0x27A) [Reset = 0xED]

R634 is shown in Table 1-364.

Return to the Summary Table.

Table 1-364. R634 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_NUM_39:32	R/W	0xED	See Register 638

1.363 R635 Register (Offset = 0x27B) [Reset = 0xFA]

R635 is shown in Table 1-365.

Return to the Summary Table.

Table 1-365. R635 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_NUM_31:24	R/W	0xFA	See Register 638

1.364 R636 Register (Offset = 0x27C) [Reset = 0x43]

R636 is shown in Table 1-366.

Return to the Summary Table.

Table 1-366. R636 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_NUM_23:16	R/W	0x43	See Register 638

1.365 R637 Register (Offset = 0x27D) [Reset = 0xFD]

R637 is shown in Table 1-367.

Return to the Summary Table.

Table 1-367. R637 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_NUM_15:8	R/W	0xFD	See Register 638

1.366 R638 Register (Offset = 0x27E) [Reset = 0x5C]

R638 is shown in Table 1-368.

Return to the Summary Table.

Table 1-368. R638 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_NUM	R/W	0x5C	DPLL Feedback Divider Numerator Value used with DPLL3 feedback configuration 2 ROM=Y, EEPROM=N

1.367 R639 Register (Offset = 0x27F) [Reset = 0xFF]

R639 is shown in Table 1-369.

Return to the Summary Table.

Table 1-369. R639 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DEN_39:32	R/W	0xFF	See Register 643

1.368 R640 Register (Offset = 0x280) [Reset = 0xFF]

R640 is shown in Table 1-370.

Return to the Summary Table.

Table 1-370. R640 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DEN_31:24	R/W	0xFF	See Register 643

1.369 R641 Register (Offset = 0x281) [Reset = 0xFF]

R641 is shown in Table 1-371.

Return to the Summary Table.

Table 1-371. R641 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DEN_23:16	R/W	0xFF	See Register 643

1.370 R642 Register (Offset = 0x282) [Reset = 0xFE]

R642 is shown in Table 1-372.

Return to the Summary Table.

Table 1-372. R642 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DEN_15:8	R/W	0xFE	See Register 643

1.371 R643 Register (Offset = 0x283) [Reset = 0xEC]

R643 is shown in Table 1-373.

Return to the Summary Table.

Table 1-373. R643 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DEN	R/W	0xEC	DPLL Feedback Divider Denominator Value used with DPLL3 feedback configuration 2 ROM=Y, EEPROM=N

1.372 R644 Register (Offset = 0x284) [Reset = 0x1]

R644 is shown in Table 1-374.

Return to the Summary Table.

Table 1-374. R644 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	DPLL3_REF5_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF5. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2

Table 1-374. R644 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DPLL3_REF4_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF4. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
3:2	RESERVED	R	0x0	Reserved
1	DPLL3_REF1_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF1. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
0	DPLL3_REF0_FB_SEL	R/W	0x1	DPLL Feedback N, NUM, DEN select for REF0. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2

1.373 R645 Register (Offset = 0x285) [Reset = 0x2]

R645 is shown in Table 1-375.

Return to the Summary Table.

Table 1-375. R645 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:3	RESERVED	R	0x0	Reserved
2:0	DPLL3_FB_MASH_ORDER	R/W	0x2	DPLL Feedback Divider MASH Order. ROM=Y, EEPROM=N

1.374 R646 Register (Offset = 0x286) [Reset = 0x0]

R646 is shown in Table 1-376.

Return to the Summary Table.

Table 1-376. R646 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_FB_FDEV_37:32	R/W	0x0	See Register 650

1.375 R647 Register (Offset = 0x287) [Reset = 0x0]

R647 is shown in Table 1-377.

Return to the Summary Table.

Table 1-377. R647 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_FDEV_31:24	R/W	0x0	See Register 650

1.376 R648 Register (Offset = 0x288) [Reset = 0x0]

R648 is shown in Table 1-378.

Return to the Summary Table.

Table 1-378. R648 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_FDEV_23:16	R/W	0x0	See Register 650

1.377 R649 Register (Offset = 0x289) [Reset = 0x69]

R649 is shown in Table 1-379.

Return to the Summary Table.

Table 1-379. R649 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_FDEV_15:8	R/W	0x69	See Register 650

1.378 R650 Register (Offset = 0x28A) [Reset = 0x8E]

R650 is shown in Table 1-380.

Return to the Summary Table.

Table 1-380. R650 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_FDEV	R/W	0x8E	DPLL Feedback Divider DCO Frequency Deviation Value ROM=Y, EEPROM=N

1.379 R651 Register (Offset = 0x28B) [Reset = 0x0]

R651 is shown in Table 1-381.

Return to the Summary Table.

Table 1-381. R651 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL3_FB_FDEV_UPDATE	R/W	0x0	Increment/Decrement DPLL Feedback Numerator value with DPLL_FB_FDEV value ROM=Y, EEPROM=N

1.380 R652 Register (Offset = 0x28C) [Reset = 0x1]

R652 is shown in Table 1-382.

Return to the Summary Table.

Table 1-382. R652 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL3_FB_FDEV_EN	R/W	0x1	Enable DPLL DCO mode ROM=Y, EEPROM=N

1.381 R653 Register (Offset = 0x28D) [Reset = 0x0]

R653 is shown in Table 1-383.

Return to the Summary Table.

Table 1-383. R653 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_STAT_39:32	R	0x0	See Register 657

1.382 R654 Register (Offset = 0x28E) [Reset = 0x0]

R654 is shown in Table 1-384.

Return to the Summary Table.

Table 1-384. R654 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_STAT_31:24	R	0x0	See Register 657

1.383 R655 Register (Offset = 0x28F) [Reset = 0x0]

R655 is shown in Table 1-385.

Return to the Summary Table.

Table 1-385. R655 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_STAT_23:16	R	0x0	See Register 657

1.384 R656 Register (Offset = 0x290) [Reset = 0x0]

R656 is shown in Table 1-386.

Return to the Summary Table.

Table 1-386. R656 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_STAT_15:8	R	0x0	See Register 657

1.385 R657 Register (Offset = 0x291) [Reset = 0x0]

R657 is shown in Table 1-387.

Return to the Summary Table.

Table 1-387. R657 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_STAT	R	0x0	Readback DPLL Feedback Divider Numerator value as a result of DCO mode ROM=N, EEPROM=N

1.386 R658 Register (Offset = 0x292) [Reset = 0x0]

R658 is shown in Table 1-388.

Return to the Summary Table.

Table 1-388. R658 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	DPLL3_REF0_DBLR_EN	R/W	0x0	DPLL Reference 0 Doubler Enable ROM=Y, EEPROM=N
2	DPLL3_REF1_DBLR_EN	R/W	0x0	DPLL Reference 1 Doubler Enable ROM=Y, EEPROM=N
1:0	RESERVED	R	0x0	Reserved

1.387 R659 Register (Offset = 0x293) [Reset = 0x0]

R659 is shown in Table 1-389.

Return to the Summary Table.

Table 1-389. R659 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF0_RDIV_15:8	R/W	0x0	See Register 660

1.388 R660 Register (Offset = 0x294) [Reset = 0xF]

R660 is shown in Table 1-390.

Return to the Summary Table.

Table 1-390. R660 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF0_RDIV	R/W	0xF	DPLL Reference 0 R divider value ROM=Y, EEPROM=N

1.389 R661 Register (Offset = 0x295) [Reset = 0x0]

R661 is shown in Table 1-391.

Return to the Summary Table.

Table 1-391. R661 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF1_RDIV_15:8	R/W	0x0	See Register 662

1.390 R662 Register (Offset = 0x296) [Reset = 0x1]

R662 is shown in Table 1-392.

Return to the Summary Table.

Table 1-392. R662 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF1_RDIV	R/W	0x1	DPLL Reference 1 R divider value ROM=Y, EEPROM=N

1.391 R663 Register (Offset = 0x297) [Reset = 0x0]

R663 is shown in Table 1-393.

Return to the Summary Table.

Table 1-393. R663 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF2_RDIV_15:8	R/W	0x0	See Register 664

1.392 R664 Register (Offset = 0x298) [Reset = 0x3]

R664 is shown in Table 1-394.

Return to the Summary Table.

Table 1-394. R664 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF2_RDIV	R/W	0x3	DPLL Reference 2 R divider value ROM=Y, EEPROM=N

1.393 R669 Register (Offset = 0x29D) [Reset = 0x1]

R669 is shown in Table 1-395.

Return to the Summary Table.

Table 1-395. R669 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF5_RDIV_15:8	R/W	0x1	See Register 670

1.394 R670 Register (Offset = 0x29E) [Reset = 0x1]

R670 is shown in Table 1-396.

Return to the Summary Table.

Table 1-396. R670 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF5_RDIV	R/W	0x1	DPLL Reference 5 R divider value ROM=Y, EEPROM=N

1.395 R707 Register (Offset = 0x2C3) [Reset = 0x50]

R707 is shown in Table 1-397.

Return to the Summary Table.

Table 1-397. R707 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_CP_PU_R	R/W	0x50	PLL charge pump pull-up resistor selection ROM=Y, EEPROM=N 0x0 = Disabled 0x1 = 78 kΩ 0x2 = 39 kΩ 0x3 = 26 kΩ 0x4 = 20 kΩ 0x5 = 15.9 kΩ 0x6 = 13.2 kΩ 0x7 = 11.3 kΩ 0x8 = 9.8 kΩ 0x9 = 8.71 kΩ 0xA = 7.83 kΩ 0xB = 7.12 kΩ 0xC = 6.58 kΩ 0xD = 6.07 kΩ 0xE = 5.63 kΩ 0xF = 5.25 kΩ 0x10 = 4.9 kΩ 0x11 = 4.61 kΩ 0x12 = 4.35 kΩ 0x13 = 4.12 kΩ 0x14 = 3.94 kΩ 0x15 = 3.75 kΩ 0x16 = 3.57 kΩ 0x17 = 3.42 kΩ 0x18 = 3.27 kΩ 0x19 = 3.14 kΩ 0x1A = 3.01 kΩ 0x1B = 2.9 kΩ 0x1C = 2.81 kΩ 0x1D = 2.71 kΩ 0x1E = 2.62 kΩ 0x1F = 2.53 kΩ 0x20 = 2.4 kΩ 0x21 = 2.33 kΩ 0x22 = 2.26 kΩ 0x23 = 2.2 kΩ 0x24 = 2.14 kΩ 0x25 = 2.09 kΩ 0x26 = 2.03 kΩ 0x27 = 1.98 kΩ 0x28 = 1.93 kΩ 0x29 = 1.88 kΩ 0x2A = 1.84 kΩ 0x2B = 1.79 kΩ 0x2C = 1.76 kΩ 0x2D = 1.72 kΩ 0x2E = 1.68 kΩ 0x2F = 1.65 kΩ 0x30 = 1.61 kΩ 0x31 = 1.58 kΩ 0x32 = 1.55 kΩ 0x33 = 1.52 kΩ 0x34 = 1.49 kΩ 0x35 = 1.46 kΩ 0x36 = 1.44 kΩ 0x37 = 1.41 kΩ 0x38 = 1.38 kΩ 0x39 = 1.36 kΩ 0x3A = 1.34 kΩ 0x3B = 1.31 kΩ 0x3C = 1.29 kΩ 0x3D = 1.27 kΩ 0x3E = 1.25 kΩ 0x3F = 1.23 kΩ 0x40 = 1.2 kΩ 0x41 = 1.18 kΩ

Table 1-397. R707 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x42 = 1.16 kΩ 0x43 = 1.15 kΩ 0x44 = 1.13 kΩ 0x45 = 1.12 kΩ 0x46 = 1.1 kΩ 0x47 = 1.08 kΩ 0x48 = 1.07 kΩ 0x49 = 1.05 kΩ 0x4A = 1.04 kΩ 0x4B = 1.03 kΩ 0x4C = 1.01 kΩ 0x4D = 1 kΩ 0x4E = 0.989 kΩ 0x4F = 0.977 kΩ 0x50 = 0.964 kΩ 0x51 = 0.952 kΩ 0x52 = 0.941 kΩ 0x53 = 0.929 kΩ 0x54 = 0.92 kΩ 0x55 = 0.909 kΩ 0x56 = 0.898 kΩ 0x57 = 0.888 kΩ 0x58 = 0.878 kΩ 0x59 = 0.868 kΩ 0x5A = 0.858 kΩ 0x5B = 0.849 kΩ 0x5C = 0.841 kΩ 0x5D = 0.832 kΩ 0x5E = 0.823 kΩ 0x5F = 0.814 kΩ 0x60 = 0.8 kΩ 0x61 = 0.792 kΩ 0x62 = 0.784 kΩ 0x63 = 0.776 kΩ 0x64 = 0.769 kΩ 0x65 = 0.762 kΩ 0x66 = 0.754 kΩ 0x67 = 0.747 kΩ 0x68 = 0.74 kΩ 0x69 = 0.733 kΩ 0x6A = 0.726 kΩ 0x6B = 0.719 kΩ 0x6C = 0.713 kΩ 0x6D = 0.707 kΩ 0x6E = 0.7 kΩ 0x6F = 0.694 kΩ 0x70 = 0.688 kΩ 0x71 = 0.682 kΩ 0x72 = 0.676 kΩ 0x73 = 0.67 kΩ 0x74 = 0.665 kΩ 0x75 = 0.659 kΩ 0x76 = 0.654 kΩ 0x77 = 0.648 kΩ 0x78 = 0.643 kΩ 0x79 = 0.637 kΩ 0x7A = 0.632 kΩ 0x7B = 0.627 kΩ 0x7C = 0.623 kΩ 0x7D = 0.618 kΩ 0x7E = 0.613 kΩ 0x7F = 0.608 kΩ 0x80 = 0.6 kΩ 0x81 = 0.595 kΩ 0x82 = 0.591 kΩ 0x83 = 0.586 kΩ 0x84 = 0.583 kΩ 0x85 = 0.578 kΩ

Table 1-397. R707 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x86 = 0.574 kΩ 0x87 = 0.57 kΩ 0x88 = 0.565 kΩ 0x89 = 0.561 kΩ 0x8A = 0.557 kΩ 0x8B = 0.553 kΩ 0x8C = 0.55 kΩ 0x8D = 0.546 kΩ 0x8E = 0.542 kΩ 0x8F = 0.538 kΩ 0x90 = 0.535 kΩ 0x91 = 0.531 kΩ 0x92 = 0.527 kΩ 0x93 = 0.524 kΩ 0x94 = 0.521 kΩ 0x95 = 0.517 kΩ 0x96 = 0.514 kΩ 0x97 = 0.51 kΩ 0x98 = 0.507 kΩ 0x99 = 0.504 kΩ 0x9A = 0.5 kΩ 0x9B = 0.497 kΩ 0x9C = 0.494 kΩ 0x9D = 0.491 kΩ 0x9E = 0.488 kΩ 0x9F = 0.485 kΩ 0xA0 = 0.48 kΩ 0xA1 = 0.477 kΩ 0xA2 = 0.474 kΩ 0xA3 = 0.471 kΩ 0xA4 = 0.469 kΩ 0xA5 = 0.466 kΩ 0xA6 = 0.463 kΩ 0xA7 = 0.46 kΩ 0xA8 = 0.458 kΩ 0xA9 = 0.455 kΩ 0xAA = 0.452 kΩ 0xAB = 0.45 kΩ 0xAC = 0.447 kΩ 0xAD = 0.445 kΩ 0xAE = 0.442 kΩ 0xAF = 0.44 kΩ 0xB0 = 0.437 kΩ 0xB1 = 0.435 kΩ 0xB2 = 0.432 kΩ 0xB3 = 0.43 kΩ 0xB4 = 0.428 kΩ 0xB5 = 0.425 kΩ 0xB6 = 0.423 kΩ 0xB7 = 0.421 kΩ 0xB8 = 0.419 kΩ 0xB9 = 0.416 kΩ 0xBA = 0.414 kΩ 0xBB = 0.412 kΩ 0xBC = 0.41 kΩ 0xBD = 0.408 kΩ 0xBE = 0.406 kΩ 0xBF = 0.404 kΩ 0xC0 = 0.4 kΩ 0xC1 = 0.398 kΩ 0xC2 = 0.396 kΩ 0xC3 = 0.394 kΩ 0xC4 = 0.392 kΩ 0xC5 = 0.39 kΩ 0xC6 = 0.388 kΩ 0xC7 = 0.386 kΩ 0xC8 = 0.384 kΩ 0xC9 = 0.382 kΩ

Table 1-397. R707 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xCA = 0.381 kΩ 0xCB = 0.379 kΩ 0xCC = 0.377 kΩ 0xCD = 0.375 kΩ 0xCE = 0.373 kΩ 0xCF = 0.372 kΩ 0xD0 = 0.37 kΩ 0xD1 = 0.368 kΩ 0xD2 = 0.366 kΩ 0xD3 = 0.365 kΩ 0xD4 = 0.363 kΩ 0xD5 = 0.361 kΩ 0xD6 = 0.36 kΩ 0xD7 = 0.358 kΩ 0xD8 = 0.356 kΩ 0xD9 = 0.355 kΩ 0xDA = 0.353 kΩ 0xDB = 0.352 kΩ 0xDC = 0.35 kΩ 0xDD = 0.349 kΩ 0xDE = 0.347 kΩ 0xDF = 0.345 kΩ 0xE0 = 0.343 kΩ 0xE1 = 0.341 kΩ 0xE2 = 0.34 kΩ 0xE3 = 0.338 kΩ 0xE4 = 0.337 kΩ 0xE5 = 0.336 kΩ 0xE6 = 0.334 kΩ 0xE7 = 0.333 kΩ 0xE8 = 0.331 kΩ 0xE9 = 0.33 kΩ 0xEA = 0.328 kΩ 0xEB = 0.327 kΩ 0xEC = 0.326 kΩ 0xED = 0.325 kΩ 0xEE = 0.323 kΩ 0xEF = 0.322 kΩ 0xF0 = 0.32 kΩ 0xF1 = 0.319 kΩ 0xF2 = 0.318 kΩ 0xF3 = 0.317 kΩ 0xF4 = 0.315 kΩ 0xF5 = 0.314 kΩ 0xF6 = 0.313 kΩ 0xF7 = 0.312 kΩ 0xF8 = 0.31 kΩ 0xF9 = 0.309 kΩ 0xFA = 0.308 kΩ 0xFB = 0.307 kΩ 0xFC = 0.306 kΩ 0xFD = 0.304 kΩ 0xFE = 0.303 kΩ 0xFF = 0.302 kΩ

1.396 R708 Register (Offset = 0x2C4) [Reset = 0x3]

R708 is shown in Table 1-398.

Return to the Summary Table.

Table 1-398. R708 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved

Table 1-398. R708 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PLL1_CPG	R/W	0x3	PLL charge pump gain Pump up/down. ROM=Y, EEPROM=Y 0x0 = 1.6 mA 0x1 = 3.2 mA 0x2 = 4.8 mA 0x3 = 6.4 mA

1.397 R709 Register (Offset = 0x2C5) [Reset = 0x2]

R709 is shown in Table 1-399.

Return to the Summary Table.

Table 1-399. R709 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-399. R709 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL1_LF_R2	R/W	0x2	PLL Loop Filter R2 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.262 kΩ 0x2 = 0.357 kΩ 0x3 = 0.166 kΩ 0x4 = 0.642 kΩ 0x5 = 0.199 kΩ 0x6 = 0.244 kΩ 0x7 = 0.142 kΩ 0x8 = 1.14 kΩ 0x9 = 0.222 kΩ 0xA = 0.283 kΩ 0xB = 0.152 kΩ 0xC = 0.425 kΩ 0xD = 0.177 kΩ 0xE = 0.21 kΩ 0xF = 0.132 kΩ 0x10 = 0.847 kΩ 0x11 = 1.06 kΩ 0x12 = 1.16 kΩ 0x13 = 0.966 kΩ 0x14 = 1.44 kΩ 0x15 = 0.998 kΩ 0x16 = 1.04 kΩ 0x17 = 0.941 kΩ 0x18 = 1.94 kΩ 0x19 = 1.02 kΩ 0x1A = 1.08 kΩ 0x1B = 0.951 kΩ 0x1C = 1.22 kΩ 0x1D = 0.976 kΩ 0x1E = 1.01 kΩ 0x1F = 0.931 kΩ 0x20 = 1.66 kΩ 0x21 = 1.88 kΩ 0x22 = 1.97 kΩ 0x23 = 1.78 kΩ 0x24 = 2.26 kΩ 0x25 = 1.81 kΩ 0x26 = 1.86 kΩ 0x27 = 1.76 kΩ 0x28 = 2.75 kΩ 0x29 = 1.84 kΩ 0x2A = 1.9 kΩ 0x2B = 1.77 kΩ 0x2C = 2.04 kΩ 0x2D = 1.79 kΩ 0x2E = 1.82 kΩ 0x2F = 1.75 kΩ 0x30 = 2.46 kΩ 0x31 = 2.68 kΩ 0x32 = 2.77 kΩ 0x33 = 2.58 kΩ 0x34 = 3.06 kΩ 0x35 = 2.61 kΩ 0x36 = 2.66 kΩ 0x37 = 2.56 kΩ 0x38 = 3.55 kΩ 0x39 = 2.64 kΩ 0x3A = 2.7 kΩ 0x3B = 2.57 kΩ 0x3C = 2.84 kΩ 0x3D = 2.59 kΩ 0x3E = 2.62 kΩ 0x3F = 2.55 kΩ

1.398 R710 Register (Offset = 0x2C6) [Reset = 0x6]

R710 is shown in Table 1-400.

Return to the Summary Table.

Table 1-400. R710 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-400. R710 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL1_LF_R3	R/W	0x6	PLL Loop Filter R3 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.277 kΩ 0x2 = 0.657 kΩ 0x3 = 0.214 kΩ 0x4 = 0.754 kΩ 0x5 = 0.221 kΩ 0x6 = 0.375 kΩ 0x7 = 0.183 kΩ 0x8 = 0.863 kΩ 0x9 = 1.08 kΩ 0xA = 1.46 kΩ 0xB = 1.01 kΩ 0xC = 1.55 kΩ 0xD = 1.02 kΩ 0xE = 1.17 kΩ 0xF = 0.982 kΩ 0x10 = 1.68 kΩ 0x11 = 1.89 kΩ 0x12 = 2.27 kΩ 0x13 = 1.83 kΩ 0x14 = 2.37 kΩ 0x15 = 1.84 kΩ 0x16 = 1.99 kΩ 0x17 = 1.8 kΩ 0x18 = 2.48 kΩ 0x19 = 2.69 kΩ 0x1A = 3.07 kΩ 0x1B = 2.63 kΩ 0x1C = 3.17 kΩ 0x1D = 2.63 kΩ 0x1E = 2.79 kΩ 0x1F = 2.6 kΩ 0x20 = 3.31 kΩ 0x21 = 3.52 kΩ 0x22 = 3.9 kΩ 0x23 = 3.46 kΩ 0x24 = 4 kΩ 0x25 = 3.47 kΩ 0x26 = 3.62 kΩ 0x27 = 3.43 kΩ 0x28 = 4.11 kΩ 0x29 = 4.32 kΩ 0x2A = 4.7 kΩ 0x2B = 4.26 kΩ 0x2C = 4.8 kΩ 0x2D = 4.26 kΩ 0x2E = 4.42 kΩ 0x2F = 4.23 kΩ 0x30 = 4.92 kΩ 0x31 = 5.14 kΩ 0x32 = 5.52 kΩ 0x33 = 5.07 kΩ 0x34 = 5.61 kΩ 0x35 = 5.08 kΩ 0x36 = 5.23 kΩ 0x37 = 5.04 kΩ 0x38 = 5.72 kΩ 0x39 = 5.94 kΩ 0x3A = 6.32 kΩ 0x3B = 5.87 kΩ 0x3C = 6.41 kΩ 0x3D = 5.88 kΩ 0x3E = 6.03 kΩ 0x3F = 5.84 kΩ

1.399 R711 Register (Offset = 0x2C7) [Reset = 0x6]

R711 is shown in Table 1-401.

Return to the Summary Table.

Table 1-401. R711 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-401. R711 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL1_LF_R4	R/W	0x6	PLL Loop Filter R4 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.277 kΩ 0x2 = 0.657 kΩ 0x3 = 0.214 kΩ 0x4 = 0.754 kΩ 0x5 = 0.221 kΩ 0x6 = 0.375 kΩ 0x7 = 0.183 kΩ 0x8 = 0.863 kΩ 0x9 = 1.08 kΩ 0xA = 1.46 kΩ 0xB = 1.01 kΩ 0xC = 1.55 kΩ 0xD = 1.02 kΩ 0xE = 1.17 kΩ 0xF = 0.982 kΩ 0x10 = 1.68 kΩ 0x11 = 1.89 kΩ 0x12 = 2.27 kΩ 0x13 = 1.83 kΩ 0x14 = 2.37 kΩ 0x15 = 1.84 kΩ 0x16 = 1.99 kΩ 0x17 = 1.8 kΩ 0x18 = 2.48 kΩ 0x19 = 2.69 kΩ 0x1A = 3.07 kΩ 0x1B = 2.63 kΩ 0x1C = 3.17 kΩ 0x1D = 2.63 kΩ 0x1E = 2.79 kΩ 0x1F = 2.6 kΩ 0x20 = 3.31 kΩ 0x21 = 3.52 kΩ 0x22 = 3.9 kΩ 0x23 = 3.46 kΩ 0x24 = 4 kΩ 0x25 = 3.47 kΩ 0x26 = 3.62 kΩ 0x27 = 3.43 kΩ 0x28 = 4.11 kΩ 0x29 = 4.32 kΩ 0x2A = 4.7 kΩ 0x2B = 4.26 kΩ 0x2C = 4.8 kΩ 0x2D = 4.26 kΩ 0x2E = 4.42 kΩ 0x2F = 4.23 kΩ 0x30 = 4.92 kΩ 0x31 = 5.14 kΩ 0x32 = 5.52 kΩ 0x33 = 5.07 kΩ 0x34 = 5.61 kΩ 0x35 = 5.08 kΩ 0x36 = 5.23 kΩ 0x37 = 5.04 kΩ 0x38 = 5.72 kΩ 0x39 = 5.94 kΩ 0x3A = 6.32 kΩ 0x3B = 5.87 kΩ 0x3C = 6.41 kΩ 0x3D = 5.88 kΩ 0x3E = 6.03 kΩ 0x3F = 5.84 kΩ

1.400 R712 Register (Offset = 0x2C8) [Reset = 0xFF]

R712 is shown in Table 1-402.

Return to the Summary Table.

Table 1-402. R712 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	PLL1_DISABLE_3RD4TH	R/W	0x3	PLL Loop Filter Disconnects C3 and C4 ROM=Y, EEPROM=N 0x0 = C3/C4 Disconnected 0x1 = C3=Enabled, C4=Disconnected 0x2 = C3=Disconnected, C4=Enabled 0x3 = C3=Enabled, C4=Enabled
5:3	PLL1_LF_C3	R/W	0x7	PLL Loop Filter C3 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF
2:0	PLL1_LF_C4	R/W	0x7	PLL Loop Filter C4 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF

1.401 R713 Register (Offset = 0x2C9) [Reset = 0x0]

R713 is shown in Table 1-403.

Return to the Summary Table.

Table 1-403. R713 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL1_RDIV_8:8	R/W	0x0	See Register 714

1.402 R714 Register (Offset = 0x2CA) [Reset = 0xB]

R714 is shown in Table 1-404.

Return to the Summary Table.

Table 1-404. R714 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_RDIV	R/W	0xB	PLL R Divider ROM=Y, EEPROM=Y

1.403 R715 Register (Offset = 0x2CB) [Reset = 0x2]

R715 is shown in Table 1-405.

Return to the Summary Table.

Table 1-405. R715 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	PLL1_RDIV_XO_EN	R/W	0x0	APLL reference source is from XO. Must also enable XO to drive this APLL with XO_OUT_BUF_EN[1] = 1 ROM=Y, EEPROM=Y
3	PLL1_RDIV_XO_DBLR_EN	R/W	0x0	Enables XO Doubler ROM=Y, EEPROM=Y
2	PLL1_RDIV_BYPASS_EN	R/W	0x0	Bypass R Divider ROM=Y, EEPROM=Y
1:0	PLL1_RDIV_MUX_SEL	R/W	0x2	Select R Divider input. When enabling reference from feedback divider, the APLL PLLx_VCO_BUF_2REF_EN bit must also be set appropriately. ROM=Y, EEPROM=Y 0x0 = XO 0x1 = VCO2 feedback divider 0x2 = VCO3 feedback divider

1.404 R716 Register (Offset = 0x2CC) [Reset = 0x0]

R716 is shown in Table 1-406.

Return to the Summary Table.

Table 1-406. R716 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL1_NDIV_8:8	R/W	0x0	See Register 717

1.405 R717 Register (Offset = 0x2CD) [Reset = 0x34]

R717 is shown in Table 1-407.

Return to the Summary Table.

Table 1-407. R717 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NDIV	R/W	0x34	PLL N Divider ROM=Y, EEPROM=Y

1.406 R718 Register (Offset = 0x2CE) [Reset = 0x4C]

R718 is shown in Table 1-408.

Return to the Summary Table.

Table 1-408. R718 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_MSB	R/W	0x4C	PLL Numerator MSB's when DPLL is disabled and MASH is 24 bit programmable Denominator ROM=Y, EEPROM=Y

1.407 R719 Register (Offset = 0x2CF) [Reset = 0xE5]

R719 is shown in Table 1-409.

Return to the Summary Table.

Table 1-409. R719 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_39:32	R/W	0xE5	See Register 723

1.408 R720 Register (Offset = 0x2D0) [Reset = 0xAA]

R720 is shown in Table 1-410.

Return to the Summary Table.

Table 1-410. R720 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_31:24	R/W	0xAA	See Register 723

1.409 R721 Register (Offset = 0x2D1) [Reset = 0xAA]

R721 is shown in Table 1-411.

Return to the Summary Table.

Table 1-411. R721 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_23:16	R/W	0xAA	See Register 723

1.410 R722 Register (Offset = 0x2D2) [Reset = 0xAA]

R722 is shown in Table 1-412.

Return to the Summary Table.

Table 1-412. R722 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_15:8	R/W	0xAA	See Register 723

1.411 R723 Register (Offset = 0x2D3) [Reset = 0xAB]

R723 is shown in Table 1-413.

Return to the Summary Table.

Table 1-413. R723 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM	R/W	0xAB	PLL Numerator in DPLL Mode, PLL Denominator when DPLL mode is disabled ROM=Y, EEPROM=Y

1.412 R724 Register (Offset = 0x2D4) [Reset = 0x7]

R724 is shown in Table 1-414.

Return to the Summary Table.

Table 1-414. R724 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-414. R724 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	PLL1_DTHRMODE	R/W	0x0	PLL MASH Dither Mode ROM=Y, EEPROM=N 0x0 = Constant Dither MACC2 0x1 = Constant Dither MACC2 and MACC3 0x2 = LFSR Dither MACC2 0x3 = Dither Disabled
3:1	PLL1_ORDER	R/W	0x3	PLL MASH Order ROM=Y, EEPROM=N 0x0 = Integer Mode Divider 0x1 = 1st 0x2 = 2nd 0x3 = 3rd
0	PLL1_MODE	R/W	0x1	In APLL 24-bit num/den mode, APLL denominator is programmable. Recommended not for use with DPLL mode. In 24-bit mode, the denominator is stored in PLL1_NUM[23:0] The numerator is stored in (PLL1_NUM_MSB << 16) + PLL1_NUM[39:24]. In APLL 40-bit mode, APLL denominator is fixed. For use with DPLL. ROM=Y, EEPROM=Y 0x0 = APLL 24-bit num/den 0x1 = APLL 40-bit num (Req for DPLL)

1.413 R725 Register (Offset = 0x2D5) [Reset = 0x0]

R725 is shown in Table 1-415.

Return to the Summary Table.

Table 1-415. R725 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL1_NUM_STAT_39:32	R	0x0	See Register 729

1.414 R726 Register (Offset = 0x2D6) [Reset = 0x0]

R726 is shown in Table 1-416.

Return to the Summary Table.

Table 1-416. R726 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL1_NUM_STAT_31:24	R	0x0	See Register 729

1.415 R727 Register (Offset = 0x2D7) [Reset = 0x0]

R727 is shown in Table 1-417.

Return to the Summary Table.

Table 1-417. R727 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL1_NUM_STAT_23:16	R	0x0	See Register 729

1.416 R728 Register (Offset = 0x2D8) [Reset = 0x0]

R728 is shown in Table 1-418.

Return to the Summary Table.

Table 1-418. R728 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL1_NUM_STAT_15:8	R	0x0	See Register 729

1.417 R729 Register (Offset = 0x2D9) [Reset = 0x0]

R729 is shown in Table 1-419.

Return to the Summary Table.

Table 1-419. R729 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL1_NUM_STAT	R	0x0	Readback current MASH Numerator after FDEV and or DPLL correction ROM=N, EEPROM=N

1.418 R731 Register (Offset = 0x2DB) [Reset = 0xE4]

R731 is shown in Table 1-420.

Return to the Summary Table.

Table 1-420. R731 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL1_PRI_DIV_SYNC_EN	R/W	0x1	PLL1 Primary Divider Sync Enable. Enables synchronization of primary post-dividers and reference dividers at startup for PLL1. ROM=Y, EEPROM=N
6	PLL1_PRI_DIV_EN	R/W	0x1	Enables the primary VCO1 divider ROM=Y, EEPROM=Y
5:3	PLL1_PRI_DIV	R/W	0x4	Sets the primary VCO1 divider divide value from 2 to 7 ROM=Y, EEPROM=Y 0x0 = 2 (Reserved) 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7
2:0	PLL1_PRI_DIV_DRVR_EN	R/W	0x4	Enables primary VCO1 divider output driver to channel output banks: [Bit 0] -> OUT0_1 [Bit 1] -> OUT2_3 [Bit 2] -> OUT14_15 ROM=Y, EEPROM=Y

1.419 R732 Register (Offset = 0x2DC) [Reset = 0x88]

R732 is shown in Table 1-421.

Return to the Summary Table.

Table 1-421. R732 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL1_SEC_DIV_SYNC_EN	R/W	0x1	PLL1 Secondary Divider Sync Enable. Enables synchronization of secondary post-dividers and reference dividers at startup for PLL1. ROM=Y, EEPROM=N
6	PLL1_SEC_DIV_EN	R/W	0x0	Enables the secondary VCO1 divider ROM=Y, EEPROM=Y

Table 1-421. R732 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:3	PLL1_SEC_DIV	R/W	0x1	Sets the secondary VCO1 divider divide value from 2 to 7 ROM=Y, EEPROM=Y 0x0 = 2 (Reserved) 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7
2:0	PLL1_SEC_DIV_DRVR_EN	R/W	0x0	Enables the secondary VCO1 divider output driver to channel output banks: [Bit 0] -> OUT0_1 [Bit 1] -> OUT2_3 [Bit 2] -> Reserved ROM=Y, EEPROM=Y

1.420 R733 Register (Offset = 0x2DD) [Reset = 0x0]

R733 is shown in Table 1-422.

Return to the Summary Table.

Table 1-422. R733 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL1_VCO_BUF_EN	R/W	0x0	Enables the VCO1 Buffer which drives the DPLL feedback, reference window detector, DPLL reference for cascade mode, and test mode ROM=Y, EEPROM=N
6:5	PLL1_VCO_BUF_2REF_EN	R/W	0x0	Enables the VCO1 Div By 4 Buffer output driver to APLL2/3 reference input for cascade mode. [0] - > APLL2, [1] -> APLL3 ROM=Y, EEPROM=Y
4	PLL1_VCO_BUF_2DPLL_EN	R/W	0x0	Enables the VCO1 Buffer output driver to DPLL feedback divider ROM=Y, EEPROM=N
3	RESERVED	R	0x0	Reserved
2	PLL1_VCO_BUF_PPM_CHECK_EN	R/W	0x0	Enables the VCO1 Div By 48 Buffer output driver to DPLL/PPM frequency detector ROM=Y, EEPROM=N
1:0	PLL1_VCO_BUF_FB_TDC_EN	R/W	0x0	Enables VCO1 Div By 8 Buffer output driver to TDC2 and TDC3 for cascade mode [0] = TDC2 driver enable [1] = TDC3 driver enable ROM=Y, EEPROM=N

1.421 R741 Register (Offset = 0x2E5) [Reset = 0x0]

R741 is shown in Table 1-423.

Return to the Summary Table.

Table 1-423. R741 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	PLL1_VM_INSIDE	R	0x0	Denotes if the VCO tuning voltage is within operational range. ROM=N, EEPROM=N
4	PLL1_VM_HI	R	0x0	vco_hi status. Denotes if the charge pump voltage is too high and outside range ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.422 R773 Register (Offset = 0x305) [Reset = 0x6]

R773 is shown in Table 1-424.

Return to the Summary Table.

Table 1-424. R773 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	RESERVED	R	0x0	Reserved
3:2	PLL2_CLSDWAIT	R/W	0x1	Sets the calibration closed loop wait time to allow the vtune voltage to settle after switching to new capcode ROM=Y, EEPROM=N 0x0 = 300 us 0x1 = 3 ms 0x2 = 30 ms 0x3 = 300 ms
1:0	PLL2_OPENWAIT	R/W	0x2	Sets the initial delay for the VCO to settle before starting the frequency calibration ROM=Y, EEPROM=N 0x0 = 20 us 0x1 = 400 us 0x2 = 8 ms 0x3 = 200 ms

1.423 R777 Register (Offset = 0x309) [Reset = 0x4D]

R777 is shown in Table 1-425.

Return to the Summary Table.

Table 1-425. R777 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_CP_PU_R	R/W	0x4D	PLL charge pump pull-up resistor selection ROM=Y, EEPROM=N 0x0 = Disabled 0x1 = 78 kΩ 0x2 = 39 kΩ 0x3 = 26 kΩ 0x4 = 20 kΩ 0x5 = 15.9 kΩ 0x6 = 13.2 kΩ 0x7 = 11.3 kΩ 0x8 = 9.8 kΩ 0x9 = 8.71 kΩ 0xA = 7.83 kΩ 0xB = 7.12 kΩ 0xC = 6.58 kΩ 0xD = 6.07 kΩ 0xE = 5.63 kΩ 0xF = 5.25 kΩ 0x10 = 4.9 kΩ 0x11 = 4.61 kΩ 0x12 = 4.35 kΩ 0x13 = 4.12 kΩ 0x14 = 3.94 kΩ 0x15 = 3.75 kΩ 0x16 = 3.57 kΩ 0x17 = 3.42 kΩ 0x18 = 3.27 kΩ 0x19 = 3.14 kΩ 0x1A = 3.01 kΩ 0x1B = 2.9 kΩ 0x1C = 2.81 kΩ 0x1D = 2.71 kΩ 0x1E = 2.62 kΩ 0x1F = 2.53 kΩ 0x20 = 2.4 kΩ 0x21 = 2.33 kΩ 0x22 = 2.26 kΩ 0x23 = 2.2 kΩ 0x24 = 2.14 kΩ 0x25 = 2.09 kΩ 0x26 = 2.03 kΩ 0x27 = 1.98 kΩ 0x28 = 1.93 kΩ 0x29 = 1.88 kΩ 0x2A = 1.84 kΩ 0x2B = 1.79 kΩ 0x2C = 1.76 kΩ 0x2D = 1.72 kΩ 0x2E = 1.68 kΩ 0x2F = 1.65 kΩ 0x30 = 1.61 kΩ 0x31 = 1.58 kΩ 0x32 = 1.55 kΩ 0x33 = 1.52 kΩ 0x34 = 1.49 kΩ 0x35 = 1.46 kΩ 0x36 = 1.44 kΩ 0x37 = 1.41 kΩ 0x38 = 1.38 kΩ 0x39 = 1.36 kΩ 0x3A = 1.34 kΩ 0x3B = 1.31 kΩ 0x3C = 1.29 kΩ 0x3D = 1.27 kΩ 0x3E = 1.25 kΩ 0x3F = 1.23 kΩ 0x40 = 1.2 kΩ 0x41 = 1.18 kΩ

Table 1-425. R777 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x42 = 1.16 kΩ 0x43 = 1.15 kΩ 0x44 = 1.13 kΩ 0x45 = 1.12 kΩ 0x46 = 1.1 kΩ 0x47 = 1.08 kΩ 0x48 = 1.07 kΩ 0x49 = 1.05 kΩ 0x4A = 1.04 kΩ 0x4B = 1.03 kΩ 0x4C = 1.01 kΩ 0x4D = 1 kΩ 0x4E = 0.989 kΩ 0x4F = 0.977 kΩ 0x50 = 0.964 kΩ 0x51 = 0.952 kΩ 0x52 = 0.941 kΩ 0x53 = 0.929 kΩ 0x54 = 0.92 kΩ 0x55 = 0.909 kΩ 0x56 = 0.898 kΩ 0x57 = 0.888 kΩ 0x58 = 0.878 kΩ 0x59 = 0.868 kΩ 0x5A = 0.858 kΩ 0x5B = 0.849 kΩ 0x5C = 0.841 kΩ 0x5D = 0.832 kΩ 0x5E = 0.823 kΩ 0x5F = 0.814 kΩ 0x60 = 0.8 kΩ 0x61 = 0.792 kΩ 0x62 = 0.784 kΩ 0x63 = 0.776 kΩ 0x64 = 0.769 kΩ 0x65 = 0.762 kΩ 0x66 = 0.754 kΩ 0x67 = 0.747 kΩ 0x68 = 0.74 kΩ 0x69 = 0.733 kΩ 0x6A = 0.726 kΩ 0x6B = 0.719 kΩ 0x6C = 0.713 kΩ 0x6D = 0.707 kΩ 0x6E = 0.7 kΩ 0x6F = 0.694 kΩ 0x70 = 0.688 kΩ 0x71 = 0.682 kΩ 0x72 = 0.676 kΩ 0x73 = 0.67 kΩ 0x74 = 0.665 kΩ 0x75 = 0.659 kΩ 0x76 = 0.654 kΩ 0x77 = 0.648 kΩ 0x78 = 0.643 kΩ 0x79 = 0.637 kΩ 0x7A = 0.632 kΩ 0x7B = 0.627 kΩ 0x7C = 0.623 kΩ 0x7D = 0.618 kΩ 0x7E = 0.613 kΩ 0x7F = 0.608 kΩ 0x80 = 0.6 kΩ 0x81 = 0.595 kΩ 0x82 = 0.591 kΩ 0x83 = 0.586 kΩ 0x84 = 0.583 kΩ 0x85 = 0.578 kΩ

Table 1-425. R777 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x86 = 0.574 kΩ 0x87 = 0.57 kΩ 0x88 = 0.565 kΩ 0x89 = 0.561 kΩ 0x8A = 0.557 kΩ 0x8B = 0.553 kΩ 0x8C = 0.55 kΩ 0x8D = 0.546 kΩ 0x8E = 0.542 kΩ 0x8F = 0.538 kΩ 0x90 = 0.535 kΩ 0x91 = 0.531 kΩ 0x92 = 0.527 kΩ 0x93 = 0.524 kΩ 0x94 = 0.521 kΩ 0x95 = 0.517 kΩ 0x96 = 0.514 kΩ 0x97 = 0.51 kΩ 0x98 = 0.507 kΩ 0x99 = 0.504 kΩ 0x9A = 0.5 kΩ 0x9B = 0.497 kΩ 0x9C = 0.494 kΩ 0x9D = 0.491 kΩ 0x9E = 0.488 kΩ 0x9F = 0.485 kΩ 0xA0 = 0.48 kΩ 0xA1 = 0.477 kΩ 0xA2 = 0.474 kΩ 0xA3 = 0.471 kΩ 0xA4 = 0.469 kΩ 0xA5 = 0.466 kΩ 0xA6 = 0.463 kΩ 0xA7 = 0.46 kΩ 0xA8 = 0.458 kΩ 0xA9 = 0.455 kΩ 0xAA = 0.452 kΩ 0xAB = 0.45 kΩ 0xAC = 0.447 kΩ 0xAD = 0.445 kΩ 0xAE = 0.442 kΩ 0xAF = 0.44 kΩ 0xB0 = 0.437 kΩ 0xB1 = 0.435 kΩ 0xB2 = 0.432 kΩ 0xB3 = 0.43 kΩ 0xB4 = 0.428 kΩ 0xB5 = 0.425 kΩ 0xB6 = 0.423 kΩ 0xB7 = 0.421 kΩ 0xB8 = 0.419 kΩ 0xB9 = 0.416 kΩ 0xBA = 0.414 kΩ 0xBB = 0.412 kΩ 0xBC = 0.41 kΩ 0xBD = 0.408 kΩ 0xBE = 0.406 kΩ 0xBF = 0.404 kΩ 0xC0 = 0.4 kΩ 0xC1 = 0.398 kΩ 0xC2 = 0.396 kΩ 0xC3 = 0.394 kΩ 0xC4 = 0.392 kΩ 0xC5 = 0.39 kΩ 0xC6 = 0.388 kΩ 0xC7 = 0.386 kΩ 0xC8 = 0.384 kΩ 0xC9 = 0.382 kΩ

Table 1-425. R777 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xCA = 0.381 kΩ 0xCB = 0.379 kΩ 0xCC = 0.377 kΩ 0xCD = 0.375 kΩ 0xCE = 0.373 kΩ 0xCF = 0.372 kΩ 0xD0 = 0.37 kΩ 0xD1 = 0.368 kΩ 0xD2 = 0.366 kΩ 0xD3 = 0.365 kΩ 0xD4 = 0.363 kΩ 0xD5 = 0.361 kΩ 0xD6 = 0.36 kΩ 0xD7 = 0.358 kΩ 0xD8 = 0.356 kΩ 0xD9 = 0.355 kΩ 0xDA = 0.353 kΩ 0xDB = 0.352 kΩ 0xDC = 0.35 kΩ 0xDD = 0.349 kΩ 0xDE = 0.347 kΩ 0xDF = 0.345 kΩ 0xE0 = 0.343 kΩ 0xE1 = 0.341 kΩ 0xE2 = 0.34 kΩ 0xE3 = 0.338 kΩ 0xE4 = 0.337 kΩ 0xE5 = 0.336 kΩ 0xE6 = 0.334 kΩ 0xE7 = 0.333 kΩ 0xE8 = 0.331 kΩ 0xE9 = 0.33 kΩ 0xEA = 0.328 kΩ 0xEB = 0.327 kΩ 0xEC = 0.326 kΩ 0xED = 0.325 kΩ 0xEE = 0.323 kΩ 0xEF = 0.322 kΩ 0xF0 = 0.32 kΩ 0xF1 = 0.319 kΩ 0xF2 = 0.318 kΩ 0xF3 = 0.317 kΩ 0xF4 = 0.315 kΩ 0xF5 = 0.314 kΩ 0xF6 = 0.313 kΩ 0xF7 = 0.312 kΩ 0xF8 = 0.31 kΩ 0xF9 = 0.309 kΩ 0xFA = 0.308 kΩ 0xFB = 0.307 kΩ 0xFC = 0.306 kΩ 0xFD = 0.304 kΩ 0xFE = 0.303 kΩ 0xFF = 0.302 kΩ

1.424 R778 Register (Offset = 0x30A) [Reset = 0xB]

R778 is shown in Table 1-426.

Return to the Summary Table.

Table 1-426. R778 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved

Table 1-426. R778 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	PLL2_CPG	R/W	0xB	PLL charge pump gain ROM=Y, EEPROM=Y 0x0 = 0 mA 0x1 = 0.4 mA 0x2 = 0.8 mA 0x3 = 1.2 mA 0x4 = 1.6 mA 0x5 = 2.0 mA 0x6 = 2.4 mA 0x7 = 2.8 mA 0x8 = 3.0 mA 0x9 = 3.4 mA 0xA = 3.8 mA 0xB = 4.2 mA 0xC = 4.6 mA 0xD = 5.0 mA 0xE = 5.4 mA 0xF = 5.8 mA

1.425 R779 Register (Offset = 0x30B) [Reset = 0x7]

R779 is shown in Table 1-427.

Return to the Summary Table.

Table 1-427. R779 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_LF_R2	R/W	0x7	PLL Loop Filter R2 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.301 kΩ 0x2 = 0.551 kΩ 0x3 = 0.209 kΩ 0x4 = 1.05 kΩ 0x5 = 0.244 kΩ 0x6 = 0.375 kΩ 0x7 = 0.183 kΩ 0x8 = 2.05 kΩ 0x9 = 0.269 kΩ 0xA = 0.444 kΩ 0xB = 0.194 kΩ 0xC = 0.709 kΩ 0xD = 0.224 kΩ 0xE = 0.0446 kΩ 0xF = 0.0421 kΩ 0x10 = 0.932 kΩ 0x11 = 1.18 kΩ 0x12 = 1.43 kΩ 0x13 = 1.09 kΩ 0x14 = 1.93 kΩ 0x15 = 1.13 kΩ 0x16 = 1.26 kΩ 0x17 = 1.07 kΩ 0x18 = 2.93 kΩ 0x19 = 1.15 kΩ 0x1A = 1.33 kΩ 0x1B = 1.08 kΩ 0x1C = 1.59 kΩ 0x1D = 1.11 kΩ 0x1E = 0.929 kΩ 0x1F = 0.926 kΩ 0x20 = 1.83 kΩ 0x21 = 2.08 kΩ 0x22 = 2.33 kΩ 0x23 = 1.99 kΩ 0x24 = 2.83 kΩ 0x25 = 2.03 kΩ 0x26 = 2.16 kΩ 0x27 = 1.97 kΩ 0x28 = 3.83 kΩ 0x29 = 2.05 kΩ 0x2A = 2.23 kΩ 0x2B = 1.98 kΩ 0x2C = 2.49 kΩ 0x2D = 2.01 kΩ 0x2E = 1.83 kΩ 0x2F = 1.83 kΩ 0x30 = 2.72 kΩ 0x31 = 2.97 kΩ 0x32 = 3.22 kΩ 0x33 = 2.88 kΩ 0x34 = 3.72 kΩ 0x35 = 2.91 kΩ 0x36 = 3.04 kΩ 0x37 = 2.85 kΩ 0x38 = 4.72 kΩ 0x39 = 2.94 kΩ 0x3A = 3.11 kΩ 0x3B = 2.86 kΩ 0x3C = 3.38 kΩ 0x3D = 2.89 kΩ 0x3E = 2.71 kΩ 0x3F = 2.71 kΩ

1.426 R780 Register (Offset = 0x30C) [Reset = 0x6]

R780 is shown in Table 1-428.

Return to the Summary Table.

Table 1-428. R780 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-428. R780 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL2_LF_R3	R/W	0x6	PLL Loop Filter R3 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.277 kΩ 0x2 = 0.657 kΩ 0x3 = 0.214 kΩ 0x4 = 0.754 kΩ 0x5 = 0.221 kΩ 0x6 = 0.375 kΩ 0x7 = 0.183 kΩ 0x8 = 0.863 kΩ 0x9 = 1.08 kΩ 0xA = 1.46 kΩ 0xB = 1.01 kΩ 0xC = 1.55 kΩ 0xD = 1.02 kΩ 0xE = 1.17 kΩ 0xF = 0.982 kΩ 0x10 = 1.68 kΩ 0x11 = 1.89 kΩ 0x12 = 2.27 kΩ 0x13 = 1.83 kΩ 0x14 = 2.37 kΩ 0x15 = 1.84 kΩ 0x16 = 1.99 kΩ 0x17 = 1.8 kΩ 0x18 = 2.48 kΩ 0x19 = 2.69 kΩ 0x1A = 3.07 kΩ 0x1B = 2.63 kΩ 0x1C = 3.17 kΩ 0x1D = 2.63 kΩ 0x1E = 2.79 kΩ 0x1F = 2.6 kΩ 0x20 = 3.31 kΩ 0x21 = 3.52 kΩ 0x22 = 3.9 kΩ 0x23 = 3.46 kΩ 0x24 = 4 kΩ 0x25 = 3.47 kΩ 0x26 = 3.62 kΩ 0x27 = 3.43 kΩ 0x28 = 4.11 kΩ 0x29 = 4.32 kΩ 0x2A = 4.7 kΩ 0x2B = 4.26 kΩ 0x2C = 4.8 kΩ 0x2D = 4.26 kΩ 0x2E = 4.42 kΩ 0x2F = 4.23 kΩ 0x30 = 4.92 kΩ 0x31 = 5.14 kΩ 0x32 = 5.52 kΩ 0x33 = 5.07 kΩ 0x34 = 5.61 kΩ 0x35 = 5.08 kΩ 0x36 = 5.23 kΩ 0x37 = 5.04 kΩ 0x38 = 5.72 kΩ 0x39 = 5.94 kΩ 0x3A = 6.32 kΩ 0x3B = 5.87 kΩ 0x3C = 6.41 kΩ 0x3D = 5.88 kΩ 0x3E = 6.03 kΩ 0x3F = 5.84 kΩ

1.427 R781 Register (Offset = 0x30D) [Reset = 0x6]

R781 is shown in Table 1-429.

Return to the Summary Table.

Table 1-429. R781 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-429. R781 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL2_LF_R4	R/W	0x6	PLL Loop Filter R4 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.277 kΩ 0x2 = 0.657 kΩ 0x3 = 0.214 kΩ 0x4 = 0.754 kΩ 0x5 = 0.221 kΩ 0x6 = 0.375 kΩ 0x7 = 0.183 kΩ 0x8 = 0.863 kΩ 0x9 = 1.08 kΩ 0xA = 1.46 kΩ 0xB = 1.01 kΩ 0xC = 1.55 kΩ 0xD = 1.02 kΩ 0xE = 1.17 kΩ 0xF = 0.982 kΩ 0x10 = 1.68 kΩ 0x11 = 1.89 kΩ 0x12 = 2.27 kΩ 0x13 = 1.83 kΩ 0x14 = 2.37 kΩ 0x15 = 1.84 kΩ 0x16 = 1.99 kΩ 0x17 = 1.8 kΩ 0x18 = 2.48 kΩ 0x19 = 2.69 kΩ 0x1A = 3.07 kΩ 0x1B = 2.63 kΩ 0x1C = 3.17 kΩ 0x1D = 2.63 kΩ 0x1E = 2.79 kΩ 0x1F = 2.6 kΩ 0x20 = 3.31 kΩ 0x21 = 3.52 kΩ 0x22 = 3.9 kΩ 0x23 = 3.46 kΩ 0x24 = 4 kΩ 0x25 = 3.47 kΩ 0x26 = 3.62 kΩ 0x27 = 3.43 kΩ 0x28 = 4.11 kΩ 0x29 = 4.32 kΩ 0x2A = 4.7 kΩ 0x2B = 4.26 kΩ 0x2C = 4.8 kΩ 0x2D = 4.26 kΩ 0x2E = 4.42 kΩ 0x2F = 4.23 kΩ 0x30 = 4.92 kΩ 0x31 = 5.14 kΩ 0x32 = 5.52 kΩ 0x33 = 5.07 kΩ 0x34 = 5.61 kΩ 0x35 = 5.08 kΩ 0x36 = 5.23 kΩ 0x37 = 5.04 kΩ 0x38 = 5.72 kΩ 0x39 = 5.94 kΩ 0x3A = 6.32 kΩ 0x3B = 5.87 kΩ 0x3C = 6.41 kΩ 0x3D = 5.88 kΩ 0x3E = 6.03 kΩ 0x3F = 5.84 kΩ

1.428 R782 Register (Offset = 0x30E) [Reset = 0xFF]

R782 is shown in Table 1-430.

Return to the Summary Table.

Table 1-430. R782 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	PLL2_DISABLE_3RD4TH	R/W	0x3	PLL Loop Filter Disconnects C3 and C4 ROM=Y, EEPROM=N 0x0 = C3/C4 Disconnected 0x1 = C3=Enabled, C4=Disconnected 0x2 = C3=Disconnected, C4=Enabled 0x3 = C3=Enabled, C4=Enabled
5:3	PLL2_LF_C3	R/W	0x7	PLL Loop Filter C3 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF
2:0	PLL2_LF_C4	R/W	0x7	PLL Loop Filter C4 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF

1.429 R783 Register (Offset = 0x30F) [Reset = 0x0]

R783 is shown in Table 1-431.

Return to the Summary Table.

Table 1-431. R783 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL2_RDIV_8:8	R/W	0x0	See Register 784

1.430 R784 Register (Offset = 0x310) [Reset = 0x1]

R784 is shown in Table 1-432.

Return to the Summary Table.

Table 1-432. R784 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_RDIV	R/W	0x1	PLL R Divider ROM=Y, EEPROM=Y

1.431 R785 Register (Offset = 0x311) [Reset = 0x1C]

R785 is shown in Table 1-433.

Return to the Summary Table.

Table 1-433. R785 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	PLL2_RDIV_XO_EN	R/W	0x1	APLL reference source is from XO. Must also enable XO to drive this APLL with XO_OUT_BUF_EN[2] = 1 ROM=Y, EEPROM=Y
3	PLL2_RDIV_XO_DBLR_EN	R/W	0x1	Enables XO Doubler ROM=Y, EEPROM=Y
2	PLL2_RDIV_BYPASS_EN	R/W	0x1	Bypass R Divider ROM=Y, EEPROM=Y
1:0	PLL2_RDIV_MUX_SEL	R/W	0x0	Select R Divider input: 0=XO, 1=VCO1 feedback divider, 2=VCO3 feedback divider ROM=Y, EEPROM=Y 0x0 = XO 0x1 = VCO1 feedback divider 0x2 = VCO3 feedback divider

1.432 R786 Register (Offset = 0x312) [Reset = 0x0]

R786 is shown in Table 1-434.

Return to the Summary Table.

Table 1-434. R786 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL2_NDIV_8:8	R/W	0x0	See Register 787

1.433 R787 Register (Offset = 0x313) [Reset = 0x48]

R787 is shown in Table 1-435.

Return to the Summary Table.

Table 1-435. R787 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NDIV	R/W	0x48	PLL N Divider ROM=Y, EEPROM=Y

1.434 R788 Register (Offset = 0x314) [Reset = 0x29]

R788 is shown in Table 1-436.

Return to the Summary Table.

Table 1-436. R788 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_MSB	R/W	0x29	PLL Numerator MSB's when DPLL is disabled and MASH is 24 bit programmable Denominator ROM=Y, EEPROM=Y

1.435 R789 Register (Offset = 0x315) [Reset = 0x56]

R789 is shown in Table 1-437.

Return to the Summary Table.

Table 1-437. R789 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_39:32	R/W	0x56	See Register 793

1.436 R790 Register (Offset = 0x316) [Reset = 0x84]

R790 is shown in Table 1-438.

Return to the Summary Table.

Table 1-438. R790 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_31:24	R/W	0x84	See Register 793

1.437 R791 Register (Offset = 0x317) [Reset = 0xBD]

R791 is shown in Table 1-439.

Return to the Summary Table.

Table 1-439. R791 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_23:16	R/W	0xBD	See Register 793

1.438 R792 Register (Offset = 0x318) [Reset = 0xA1]

R792 is shown in Table 1-440.

Return to the Summary Table.

Table 1-440. R792 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_15:8	R/W	0xA1	See Register 793

1.439 R793 Register (Offset = 0x319) [Reset = 0x2F]

R793 is shown in Table 1-441.

Return to the Summary Table.

Table 1-441. R793 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM	R/W	0x2F	PLL Numerator in DPLL Mode, PLL Denominator when DPLL mode is disabled ROM=Y, EEPROM=Y

1.440 R794 Register (Offset = 0x31A) [Reset = 0x7]

R794 is shown in Table 1-442.

Return to the Summary Table.

Table 1-442. R794 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-442. R794 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	PLL2_DTHRMODE	R/W	0x0	PLL MASH Dither Mode ROM=Y, EEPROM=N 0x0 = Constant Dither MACC2 0x1 = Constant Dither MACC2 and MACC3 0x2 = LFSR Dither MACC2 0x3 = Dither Disabled
3:1	PLL2_ORDER	R/W	0x3	PLL MASH Order ROM=Y, EEPROM=N 0x0 = Integer Mode Divider 0x1 = 1st 0x2 = 2nd 0x3 = 3rd
0	PLL2_MODE	R/W	0x1	In APLL 24-bit num/den mode, APLL denominator is programmable. Not for use with DPLL mode. In 24-bit mode, the denominator is stored in PLL2_NUM[23:0] The numerator is stored in (PLL2_NUM_MSB << 16) + PLL2_NUM[39:24]. In APLL 40-bit mode, APLL denominator is fixed. For use with DPLL. ROM=Y, EEPROM=Y 0x0 = APLL 24-bit num/den 0x1 = APLL 40-bit num (Req for DPLL)

1.441 R795 Register (Offset = 0x31B) [Reset = 0x0]

R795 is shown in Table 1-443.

Return to the Summary Table.

Table 1-443. R795 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_STAT_39:32	R	0x0	See Register 799

1.442 R796 Register (Offset = 0x31C) [Reset = 0x0]

R796 is shown in Table 1-444.

Return to the Summary Table.

Table 1-444. R796 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_STAT_31:24	R	0x0	See Register 799

1.443 R797 Register (Offset = 0x31D) [Reset = 0x0]

R797 is shown in Table 1-445.

Return to the Summary Table.

Table 1-445. R797 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_STAT_23:16	R	0x0	See Register 799

1.444 R798 Register (Offset = 0x31E) [Reset = 0x0]

R798 is shown in Table 1-446.

Return to the Summary Table.

Table 1-446. R798 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_STAT_15:8	R	0x0	See Register 799

1.445 R799 Register (Offset = 0x31F) [Reset = 0x0]

R799 is shown in Table 1-447.

Return to the Summary Table.

Table 1-447. R799 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_STAT	R	0x0	Readback current MASH Numerator after FDEV and or DPLL correction ROM=N, EEPROM=N

1.446 R803 Register (Offset = 0x323) [Reset = 0x53]

R803 is shown in Table 1-448.

Return to the Summary Table.

Table 1-448. R803 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	PLL2_VCO_DIV_3_SEL	R/W	0x1	Selects VCO2 divide value for OUT4/OUT6 CML Output Drivers from: 0=VCO2 Div By 2, or 1=VCO2 Div By 3. ROM=Y, EEPROM=Y 0x0 = 2 0x1 = 3
5	PLL2_VCO_DIV_2_3_EN	R/W	0x0	Enables the VCO2 Div By 2 or 3 divide block used for driving CML outputs ROM=Y, EEPROM=Y
4	PLL2_VCO_BUF_EN	R/W	0x1	Enables the VCO2 Buffer which drives the DPLL feedback, reference window detector, DPLL reference for cascade mode, and test mode ROM=Y, EEPROM=N
3:2	PLL2_VCO_BUF_2REF_EN	R/W	0x0	Enables the VCO2 Div By 4 buffer output driver to [0] -> APLL1 and [1] -> APLL3 reference input for cascade mode. ROM=Y, EEPROM=Y
1	PLL2_VCO_BUF_2DPLL_EN	R/W	0x1	Enables the VCO2 Buffer output driver to DPLL2 feedback divider ROM=Y, EEPROM=N
0	PLL2_VCO_BUF_2WNDDET_EN	R/W	0x1	Enables the VCO2 Div By 5 Buffer output driver to reference window detectors input buffer and prepares predivided clock for DPLL2 loopfilter and PPM/Frequency detector. ROM=Y, EEPROM=N

1.447 R804 Register (Offset = 0x324) [Reset = 0x39]

R804 is shown in Table 1-449.

Return to the Summary Table.

Table 1-449. R804 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	PLL2_VCO_DIV_SYNC_EN	R/W	0x1	PLL2 Divider Sync Enable. Enables synchronization of post-dividers and reference dividers at startup for PLL2. ROM=Y, EEPROM=N

Table 1-449. R804 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	PLL2_VCO_DIV_EN	R/W	0x1	Enables the VCO2 Div By 2 to 13 divide block. ROM=Y, EEPROM=Y
3:0	PLL2_VCO_DIV	R/W	0x9	Sets the VCO2 divider divide value from 2 to 13 ROM=Y, EEPROM=Y 0x0 = 2 (Reserved) 0x1 = 2 (Reserved) 0x2 = 2 0x3 = 3 0x4 = 4 0x5 = 5 0x6 = 6 0x7 = 7 0x8 = 8 0x9 = 9 0xA = 10 0xB = 11 0xC = 12 0xD = 13

1.448 R805 Register (Offset = 0x325) [Reset = 0x6]

R805 is shown in Table 1-450.

Return to the Summary Table.

Table 1-450. R805 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	PLL2_VCO_BUF_FB_TDC_EN	R/W	0x0	Enables VCO2 Div By 10 Buffer output driver to TDC1 and TDC3 for cascade mode [0] = TDC1 driver enable [1] = TDC3 driver enable ROM=Y, EEPROM=N
4:0	PLL2_VCO_DIV_DRVR_EN	R/W	0x6	Enables VCO2 to Outputs output buffer outputs: [0] -> OUT0_1, [1] -> OUT2_3, [2] -> OUT4_5 and OUT6_7, [3] -> OUT8_9, OUT10_11, and OUT12_13, and [4] -> OUT14_15. ROM=Y, EEPROM=Y

1.449 R813 Register (Offset = 0x32D) [Reset = 0x0]

R813 is shown in Table 1-451.

Return to the Summary Table.

Table 1-451. R813 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	PLL2_VM_INSIDE	R	0x0	Denotes if the VCO tuning voltage is within operational range. ROM=N, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.450 R840 Register (Offset = 0x348) [Reset = 0x57]

R840 is shown in Table 1-452.

Return to the Summary Table.

Table 1-452. R840 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_CPBAW_BLEED	R/W	0x57	PLL charge pump pull-up resistor selection ROM=Y, EEPROM=N 0x0 = Disabled 0x1 = 78 kΩ 0x2 = 39 kΩ 0x3 = 26 kΩ 0x4 = 20 kΩ 0x5 = 15.9 kΩ 0x6 = 13.2 kΩ 0x7 = 11.3 kΩ 0x8 = 9.8 kΩ 0x9 = 8.71 kΩ 0xA = 7.83 kΩ 0xB = 7.12 kΩ 0xC = 6.58 kΩ 0xD = 6.07 kΩ 0xE = 5.63 kΩ 0xF = 5.25 kΩ 0x10 = 4.9 kΩ 0x11 = 4.61 kΩ 0x12 = 4.35 kΩ 0x13 = 4.12 kΩ 0x14 = 3.94 kΩ 0x15 = 3.75 kΩ 0x16 = 3.57 kΩ 0x17 = 3.42 kΩ 0x18 = 3.27 kΩ 0x19 = 3.14 kΩ 0x1A = 3.01 kΩ 0x1B = 2.9 kΩ 0x1C = 2.81 kΩ 0x1D = 2.71 kΩ 0x1E = 2.62 kΩ 0x1F = 2.53 kΩ 0x20 = 2.4 kΩ 0x21 = 2.33 kΩ 0x22 = 2.26 kΩ 0x23 = 2.2 kΩ 0x24 = 2.14 kΩ 0x25 = 2.09 kΩ 0x26 = 2.03 kΩ 0x27 = 1.98 kΩ 0x28 = 1.93 kΩ 0x29 = 1.88 kΩ 0x2A = 1.84 kΩ 0x2B = 1.79 kΩ 0x2C = 1.76 kΩ 0x2D = 1.72 kΩ 0x2E = 1.68 kΩ 0x2F = 1.65 kΩ 0x30 = 1.61 kΩ 0x31 = 1.58 kΩ 0x32 = 1.55 kΩ 0x33 = 1.52 kΩ 0x34 = 1.49 kΩ 0x35 = 1.46 kΩ 0x36 = 1.44 kΩ 0x37 = 1.41 kΩ 0x38 = 1.38 kΩ 0x39 = 1.36 kΩ 0x3A = 1.34 kΩ 0x3B = 1.31 kΩ 0x3C = 1.29 kΩ 0x3D = 1.27 kΩ 0x3E = 1.25 kΩ 0x3F = 1.23 kΩ 0x40 = 1.2 kΩ 0x41 = 1.18 kΩ

Table 1-452. R840 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x42 = 1.16 kΩ 0x43 = 1.15 kΩ 0x44 = 1.13 kΩ 0x45 = 1.12 kΩ 0x46 = 1.1 kΩ 0x47 = 1.08 kΩ 0x48 = 1.07 kΩ 0x49 = 1.05 kΩ 0x4A = 1.04 kΩ 0x4B = 1.03 kΩ 0x4C = 1.01 kΩ 0x4D = 1 kΩ 0x4E = 0.989 kΩ 0x4F = 0.977 kΩ 0x50 = 0.964 kΩ 0x51 = 0.952 kΩ 0x52 = 0.941 kΩ 0x53 = 0.929 kΩ 0x54 = 0.92 kΩ 0x55 = 0.909 kΩ 0x56 = 0.898 kΩ 0x57 = 0.888 kΩ 0x58 = 0.878 kΩ 0x59 = 0.868 kΩ 0x5A = 0.858 kΩ 0x5B = 0.849 kΩ 0x5C = 0.841 kΩ 0x5D = 0.832 kΩ 0x5E = 0.823 kΩ 0x5F = 0.814 kΩ 0x60 = 0.8 kΩ 0x61 = 0.792 kΩ 0x62 = 0.784 kΩ 0x63 = 0.776 kΩ 0x64 = 0.769 kΩ 0x65 = 0.762 kΩ 0x66 = 0.754 kΩ 0x67 = 0.747 kΩ 0x68 = 0.74 kΩ 0x69 = 0.733 kΩ 0x6A = 0.726 kΩ 0x6B = 0.719 kΩ 0x6C = 0.713 kΩ 0x6D = 0.707 kΩ 0x6E = 0.7 kΩ 0x6F = 0.694 kΩ 0x70 = 0.688 kΩ 0x71 = 0.682 kΩ 0x72 = 0.676 kΩ 0x73 = 0.67 kΩ 0x74 = 0.665 kΩ 0x75 = 0.659 kΩ 0x76 = 0.654 kΩ 0x77 = 0.648 kΩ 0x78 = 0.643 kΩ 0x79 = 0.637 kΩ 0x7A = 0.632 kΩ 0x7B = 0.627 kΩ 0x7C = 0.623 kΩ 0x7D = 0.618 kΩ 0x7E = 0.613 kΩ 0x7F = 0.608 kΩ 0x80 = 0.6 kΩ 0x81 = 0.595 kΩ 0x82 = 0.591 kΩ 0x83 = 0.586 kΩ 0x84 = 0.583 kΩ 0x85 = 0.578 kΩ

Table 1-452. R840 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x86 = 0.574 kΩ 0x87 = 0.57 kΩ 0x88 = 0.565 kΩ 0x89 = 0.561 kΩ 0x8A = 0.557 kΩ 0x8B = 0.553 kΩ 0x8C = 0.55 kΩ 0x8D = 0.546 kΩ 0x8E = 0.542 kΩ 0x8F = 0.538 kΩ 0x90 = 0.535 kΩ 0x91 = 0.531 kΩ 0x92 = 0.527 kΩ 0x93 = 0.524 kΩ 0x94 = 0.521 kΩ 0x95 = 0.517 kΩ 0x96 = 0.514 kΩ 0x97 = 0.51 kΩ 0x98 = 0.507 kΩ 0x99 = 0.504 kΩ 0x9A = 0.5 kΩ 0x9B = 0.497 kΩ 0x9C = 0.494 kΩ 0x9D = 0.491 kΩ 0x9E = 0.488 kΩ 0x9F = 0.485 kΩ 0xA0 = 0.48 kΩ 0xA1 = 0.477 kΩ 0xA2 = 0.474 kΩ 0xA3 = 0.471 kΩ 0xA4 = 0.469 kΩ 0xA5 = 0.466 kΩ 0xA6 = 0.463 kΩ 0xA7 = 0.46 kΩ 0xA8 = 0.458 kΩ 0xA9 = 0.455 kΩ 0xAA = 0.452 kΩ 0xAB = 0.45 kΩ 0xAC = 0.447 kΩ 0xAD = 0.445 kΩ 0xAE = 0.442 kΩ 0xAF = 0.44 kΩ 0xB0 = 0.437 kΩ 0xB1 = 0.435 kΩ 0xB2 = 0.432 kΩ 0xB3 = 0.43 kΩ 0xB4 = 0.428 kΩ 0xB5 = 0.425 kΩ 0xB6 = 0.423 kΩ 0xB7 = 0.421 kΩ 0xB8 = 0.419 kΩ 0xB9 = 0.416 kΩ 0xBA = 0.414 kΩ 0xBB = 0.412 kΩ 0xBC = 0.41 kΩ 0xBD = 0.408 kΩ 0xBE = 0.406 kΩ 0xBF = 0.404 kΩ 0xC0 = 0.4 kΩ 0xC1 = 0.398 kΩ 0xC2 = 0.396 kΩ 0xC3 = 0.394 kΩ 0xC4 = 0.392 kΩ 0xC5 = 0.39 kΩ 0xC6 = 0.388 kΩ 0xC7 = 0.386 kΩ 0xC8 = 0.384 kΩ 0xC9 = 0.382 kΩ

Table 1-452. R840 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xCA = 0.381 kΩ 0xCB = 0.379 kΩ 0xCC = 0.377 kΩ 0xCD = 0.375 kΩ 0xCE = 0.373 kΩ 0xCF = 0.372 kΩ 0xD0 = 0.37 kΩ 0xD1 = 0.368 kΩ 0xD2 = 0.366 kΩ 0xD3 = 0.365 kΩ 0xD4 = 0.363 kΩ 0xD5 = 0.361 kΩ 0xD6 = 0.36 kΩ 0xD7 = 0.358 kΩ 0xD8 = 0.356 kΩ 0xD9 = 0.355 kΩ 0xDA = 0.353 kΩ 0xDB = 0.352 kΩ 0xDC = 0.35 kΩ 0xDD = 0.349 kΩ 0xDE = 0.347 kΩ 0xDF = 0.345 kΩ 0xE0 = 0.343 kΩ 0xE1 = 0.341 kΩ 0xE2 = 0.34 kΩ 0xE3 = 0.338 kΩ 0xE4 = 0.337 kΩ 0xE5 = 0.336 kΩ 0xE6 = 0.334 kΩ 0xE7 = 0.333 kΩ 0xE8 = 0.331 kΩ 0xE9 = 0.33 kΩ 0xEA = 0.328 kΩ 0xEB = 0.327 kΩ 0xEC = 0.326 kΩ 0xED = 0.325 kΩ 0xEE = 0.323 kΩ 0xEF = 0.322 kΩ 0xF0 = 0.32 kΩ 0xF1 = 0.319 kΩ 0xF2 = 0.318 kΩ 0xF3 = 0.317 kΩ 0xF4 = 0.315 kΩ 0xF5 = 0.314 kΩ 0xF6 = 0.313 kΩ 0xF7 = 0.312 kΩ 0xF8 = 0.31 kΩ 0xF9 = 0.309 kΩ 0xFA = 0.308 kΩ 0xFB = 0.307 kΩ 0xFC = 0.306 kΩ 0xFD = 0.304 kΩ 0xFE = 0.303 kΩ 0xFF = 0.302 kΩ

1.451 R841 Register (Offset = 0x349) [Reset = 0xB]

R841 is shown in Table 1-453.

Return to the Summary Table.

Table 1-453. R841 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved

Table 1-453. R841 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	PLL3_CPG	R/W	0xB	PLL charge pump gain ROM=Y, EEPROM=N 0x0 = 0 mA 0x1 = 0.4 mA 0x2 = 0.8 mA 0x3 = 1.2 mA 0x4 = 1.6 mA 0x5 = 2.0 mA 0x6 = 2.4 mA 0x7 = 2.8 mA 0x8 = 3.0 mA 0x9 = 3.4 mA 0xA = 3.8 mA 0xB = 4.2 mA 0xC = 4.6 mA 0xD = 5.0 mA 0xE = 5.4 mA 0xF = 5.8 mA

1.452 R842 Register (Offset = 0x34A) [Reset = 0x1]

R842 is shown in Table 1-454.

Return to the Summary Table.

Table 1-454. R842 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-454. R842 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL3_LF_R2	R/W	0x1	PLL Loop Filter R2 setting ROM=Y, EEPROM=N 0x0 = 0.0139 kΩ 0x1 = 0.51 kΩ 0x2 = 0.985 kΩ 0x3 = 1.39 kΩ 0x4 = 1.72 kΩ 0x5 = 2.12 kΩ 0x6 = 2.6 kΩ 0x7 = 3 kΩ 0x8 = 3.3 kΩ 0x9 = 3.75 kΩ 0xA = 4.23 kΩ 0xB = 4.63 kΩ 0xC = 4.96 kΩ 0xD = 5.36 kΩ 0xE = 5.84 kΩ 0xF = 6.24 kΩ 0x10 = 6.57 kΩ 0x11 = 7.01 kΩ 0x12 = 7.49 kΩ 0x13 = 7.89 kΩ 0x14 = 8.22 kΩ 0x15 = 8.63 kΩ 0x16 = 9.1 kΩ 0x17 = 9.5 kΩ 0x18 = 9.81 kΩ 0x19 = 10.3 kΩ 0x1A = 10.7 kΩ 0x1B = 11.1 kΩ 0x1C = 11.5 kΩ 0x1D = 11.9 kΩ 0x1E = 12.3 kΩ 0x1F = 12.7 kΩ 0x20 = 13 kΩ 0x21 = 13.5 kΩ 0x22 = 14 kΩ 0x23 = 14.4 kΩ 0x24 = 14.7 kΩ 0x25 = 15.1 kΩ 0x26 = 15.6 kΩ 0x27 = 16 kΩ 0x28 = 16.3 kΩ 0x29 = 16.7 kΩ 0x2A = 17.2 kΩ 0x2B = 17.6 kΩ 0x2C = 17.9 kΩ 0x2D = 18.3 kΩ 0x2E = 18.8 kΩ 0x2F = 19.2 kΩ 0x30 = 19.6 kΩ 0x31 = 20 kΩ 0x32 = 20.5 kΩ 0x33 = 20.9 kΩ 0x34 = 21.2 kΩ 0x35 = 21.6 kΩ 0x36 = 22.1 kΩ 0x37 = 22.5 kΩ 0x38 = 22.8 kΩ 0x39 = 23.2 kΩ 0x3A = 23.7 kΩ 0x3B = 24.1 kΩ 0x3C = 24.4 kΩ 0x3D = 24.9 kΩ 0x3E = 25.3 kΩ 0x3F = 25.7 kΩ

1.453 R843 Register (Offset = 0x34B) [Reset = 0xE]

R843 is shown in Table 1-455.

Return to the Summary Table.

Table 1-455. R843 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-455. R843 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL3_LF_R3	R/W	0xE	PLL Loop Filter R3 setting ROM=Y, EEPROM=N 0x0 = 0.0139 kΩ 0x1 = 0.51 kΩ 0x2 = 0.826 kΩ 0x3 = 1.23 kΩ 0x4 = 1.85 kΩ 0x5 = 2.26 kΩ 0x6 = 2.57 kΩ 0x7 = 2.97 kΩ 0x8 = 3.3 kΩ 0x9 = 3.75 kΩ 0xA = 4.07 kΩ 0xB = 4.47 kΩ 0xC = 5.09 kΩ 0xD = 5.5 kΩ 0xE = 5.81 kΩ 0xF = 6.22 kΩ 0x10 = 6.57 kΩ 0x11 = 7.01 kΩ 0x12 = 7.33 kΩ 0x13 = 7.73 kΩ 0x14 = 8.36 kΩ 0x15 = 8.76 kΩ 0x16 = 9.08 kΩ 0x17 = 9.48 kΩ 0x18 = 9.81 kΩ 0x19 = 10.3 kΩ 0x1A = 10.6 kΩ 0x1B = 11 kΩ 0x1C = 11.6 kΩ 0x1D = 12 kΩ 0x1E = 12.3 kΩ 0x1F = 12.7 kΩ 0x20 = 13 kΩ 0x21 = 13.5 kΩ 0x22 = 13.8 kΩ 0x23 = 14.2 kΩ 0x24 = 14.8 kΩ 0x25 = 15.2 kΩ 0x26 = 15.6 kΩ 0x27 = 16 kΩ 0x28 = 16.3 kΩ 0x29 = 16.7 kΩ 0x2A = 17.1 kΩ 0x2B = 17.5 kΩ 0x2C = 18.1 kΩ 0x2D = 18.5 kΩ 0x2E = 18.8 kΩ 0x2F = 19.2 kΩ 0x30 = 19.6 kΩ 0x31 = 20 kΩ 0x32 = 20.3 kΩ 0x33 = 20.7 kΩ 0x34 = 21.3 kΩ 0x35 = 21.7 kΩ 0x36 = 22.1 kΩ 0x37 = 22.5 kΩ 0x38 = 22.8 kΩ 0x39 = 23.2 kΩ 0x3A = 23.6 kΩ 0x3B = 24 kΩ 0x3C = 24.6 kΩ 0x3D = 25 kΩ 0x3E = 25.3 kΩ 0x3F = 25.7 kΩ

1.454 R844 Register (Offset = 0x34C) [Reset = 0xE]

R844 is shown in Table 1-456.

Return to the Summary Table.

Table 1-456. R844 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-456. R844 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL3_LF_R4	R/W	0xE	PLL Loop Filter R4 setting ROM=Y, EEPROM=N 0x0 = 0.0139 kΩ 0x1 = 0.51 kΩ 0x2 = 0.826 kΩ 0x3 = 1.23 kΩ 0x4 = 1.85 kΩ 0x5 = 2.26 kΩ 0x6 = 2.57 kΩ 0x7 = 2.97 kΩ 0x8 = 3.3 kΩ 0x9 = 3.75 kΩ 0xA = 4.07 kΩ 0xB = 4.47 kΩ 0xC = 5.09 kΩ 0xD = 5.5 kΩ 0xE = 5.81 kΩ 0xF = 6.22 kΩ 0x10 = 6.57 kΩ 0x11 = 7.01 kΩ 0x12 = 7.33 kΩ 0x13 = 7.73 kΩ 0x14 = 8.36 kΩ 0x15 = 8.76 kΩ 0x16 = 9.08 kΩ 0x17 = 9.48 kΩ 0x18 = 9.81 kΩ 0x19 = 10.3 kΩ 0x1A = 10.6 kΩ 0x1B = 11 kΩ 0x1C = 11.6 kΩ 0x1D = 12 kΩ 0x1E = 12.3 kΩ 0x1F = 12.7 kΩ 0x20 = 13 kΩ 0x21 = 13.5 kΩ 0x22 = 13.8 kΩ 0x23 = 14.2 kΩ 0x24 = 14.8 kΩ 0x25 = 15.2 kΩ 0x26 = 15.6 kΩ 0x27 = 16 kΩ 0x28 = 16.3 kΩ 0x29 = 16.7 kΩ 0x2A = 17.1 kΩ 0x2B = 17.5 kΩ 0x2C = 18.1 kΩ 0x2D = 18.5 kΩ 0x2E = 18.8 kΩ 0x2F = 19.2 kΩ 0x30 = 19.6 kΩ 0x31 = 20 kΩ 0x32 = 20.3 kΩ 0x33 = 20.7 kΩ 0x34 = 21.3 kΩ 0x35 = 21.7 kΩ 0x36 = 22.1 kΩ 0x37 = 22.5 kΩ 0x38 = 22.8 kΩ 0x39 = 23.2 kΩ 0x3A = 23.6 kΩ 0x3B = 24 kΩ 0x3C = 24.6 kΩ 0x3D = 25 kΩ 0x3E = 25.3 kΩ 0x3F = 25.7 kΩ

1.455 R845 Register (Offset = 0x34D) [Reset = 0x3F]

R845 is shown in Table 1-457.

Return to the Summary Table.

Table 1-457. R845 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	PLL3_LF_C3	R/W	0x7	PLL Loop Filter C3 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF
2:0	PLL3_LF_C4	R/W	0x7	PLL Loop Filter C4 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF

1.456 R846 Register (Offset = 0x34E) [Reset = 0x0]

R846 is shown in Table 1-458.

Return to the Summary Table.

Table 1-458. R846 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL3_RDIV_8:8	R/W	0x0	See Register 847

1.457 R847 Register (Offset = 0x34F) [Reset = 0x1]

R847 is shown in Table 1-459.

Return to the Summary Table.

Table 1-459. R847 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_RDIV	R/W	0x1	PLL R Divider ROM=Y, EEPROM=Y

1.458 R848 Register (Offset = 0x350) [Reset = 0x1C]

R848 is shown in Table 1-460.

Return to the Summary Table.

Table 1-460. R848 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-460. R848 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	PLL3_RDIV_XO_EN	R/W	0x1	APLL reference source is from XO. Must also enable XO to drive this APLL with XO_OUT_BUF_EN[3] = 1 ROM=Y, EEPROM=Y
3	PLL3_RDIV_XO_DBLR_EN	R/W	0x1	Enables XO Doubler ROM=Y, EEPROM=Y
2	PLL3_RDIV_BYPASS_EN	R/W	0x1	Bypass R Divider ROM=Y, EEPROM=Y
1:0	PLL3_RDIV_MUX_SEL	R/W	0x0	Select R Divider input: 0=XO, 1=VCO1 feedback divider, 2=VCO2 feedback divider ROM=Y, EEPROM=Y 0x0 = XO 0x1 = VCO1 feedback divider 0x2 = VCO2 feedback divider

1.459 R849 Register (Offset = 0x351) [Reset = 0x0]

R849 is shown in Table 1-461.

Return to the Summary Table.

Table 1-461. R849 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL3_NDIV_8:8	R/W	0x0	See Register 850

1.460 R850 Register (Offset = 0x352) [Reset = 0x1F]

R850 is shown in Table 1-462.

Return to the Summary Table.

Table 1-462. R850 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NDIV	R/W	0x1F	PLL N Divider ROM=Y, EEPROM=Y

1.461 R851 Register (Offset = 0x353) [Reset = 0x4C]

R851 is shown in Table 1-463.

Return to the Summary Table.

Table 1-463. R851 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM_MSB	R/W	0x4C	PLL Numerator MSB's when DPLL is disabled and MASH is 24 bit programmable Denominator ROM=Y, EEPROM=Y

1.462 R852 Register (Offset = 0x354) [Reset = 0x9A]

R852 is shown in Table 1-464.

Return to the Summary Table.

Table 1-464. R852 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM_39:32	R/W	0x9A	See Register 856

1.463 R853 Register (Offset = 0x355) [Reset = 0xDD]

R853 is shown in Table 1-465.

Return to the Summary Table.

Table 1-465. R853 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM_31:24	R/W	0xDD	See Register 856

1.464 R854 Register (Offset = 0x356) [Reset = 0x3C]

R854 is shown in Table 1-466.

Return to the Summary Table.

Table 1-466. R854 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM_23:16	R/W	0x3C	See Register 856

1.465 R855 Register (Offset = 0x357) [Reset = 0xC]

R855 is shown in Table 1-467.

Return to the Summary Table.

Table 1-467. R855 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM_15:8	R/W	0xC	See Register 856

1.466 R856 Register (Offset = 0x358) [Reset = 0xA4]

R856 is shown in Table 1-468.

Return to the Summary Table.

Table 1-468. R856 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM	R/W	0xA4	PLL Numerator in DPLL Mode, PLL Denominator when DPLL mode is disabled ROM=Y, EEPROM=Y

1.467 R857 Register (Offset = 0x359) [Reset = 0x5]

R857 is shown in Table 1-469.

Return to the Summary Table.

Table 1-469. R857 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-469. R857 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	PLL3_DTHRMODE	R/W	0x0	PLL MASH Dither Mode ROM=Y, EEPROM=N 0x0 = Constant Dither MACC2 0x1 = Constant Dither MACC2 and MACC3 0x2 = LFSR Dither MACC2 0x3 = Dither Disabled
3:1	PLL3_ORDER	R/W	0x2	PLL MASH Order ROM=Y, EEPROM=N 0x0 = Integer Mode Divider 0x1 = 1st 0x2 = 2nd 0x3 = 3rd
0	PLL3_MODE	R/W	0x1	In APLL 24-bit num/den mode, APLL denominator is programmable. Recommended not for use with DPLL mode. In 24-bit mode, the denominator is stored in PLL3_NUM[23:0] The numerator is stored in (PLL3_NUM_MSB << 16) + PLL3_NUM[39:24]. In APLL 40-bit mode, APLL denominator is fixed. For use with DPLL. ROM=Y, EEPROM=Y 0x0 = APLL 24-bit num/den 0x1 = APLL 40-bit num (Req for DPLL)

1.468 R858 Register (Offset = 0x35A) [Reset = 0x0]

R858 is shown in Table 1-470.

Return to the Summary Table.

Table 1-470. R858 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM_STAT_39:32	R	0x0	See Register 862

1.469 R859 Register (Offset = 0x35B) [Reset = 0x0]

R859 is shown in Table 1-471.

Return to the Summary Table.

Table 1-471. R859 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM_STAT_31:24	R	0x0	See Register 862

1.470 R860 Register (Offset = 0x35C) [Reset = 0x0]

R860 is shown in Table 1-472.

Return to the Summary Table.

Table 1-472. R860 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM_STAT_23:16	R	0x0	See Register 862

1.471 R861 Register (Offset = 0x35D) [Reset = 0x0]

R861 is shown in Table 1-473.

Return to the Summary Table.

Table 1-473. R861 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM_STAT_15:8	R	0x0	See Register 862

1.472 R862 Register (Offset = 0x35E) [Reset = 0x0]

R862 is shown in Table 1-474.

Return to the Summary Table.

Table 1-474. R862 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM_STAT	R	0x0	Readback current MASH Numerator after FDEV and or DPLL correction ROM=N, EEPROM=N

1.473 R864 Register (Offset = 0x360) [Reset = 0x44]

R864 is shown in Table 1-475.

Return to the Summary Table.

Table 1-475. R864 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	PLL3_PRI_DIV	R/W	0x4	Sets the VCO3 primary divider divide value from 1 to 7 ROM=Y, EEPROM=Y 0x0 = 1 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7
3:0	PLL3_CHAN_EN	R/W	0x4	Enables the VCO3 to Outputs output buffer outputs: [0] -> OUT0_1, [1] -> OUT4_5 and OUT6_7, and [2] -> OUT8_9, OUT10_11, and OUT12_13 [3] -> OUT14 and OUT15 ROM=Y, EEPROM=Y

1.474 R865 Register (Offset = 0x361) [Reset = 0x30]

R865 is shown in Table 1-476.

Return to the Summary Table.

Table 1-476. R865 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	PLL3_DIV_SYNC_EN	R/W	0x1	PLL3 Divider Sync Enable. Enables synchronization of post-dividers and reference dividers at startup for PLL3. ROM=Y, EEPROM=N
4	PLL3_CHAN_SEL_DIV1TO7	R/W	0x1	Selects the VCO3 to Outputs output buffer to be driven by VCO3 Div By 1 to 7 divide block. If selected, Div By 5 block must be deselected. ROM=Y, EEPROM=Y
3	RESERVED	R	0x0	Reserved

Table 1-476. R865 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	PLL3_CLKDRVRBYP46_SEL	R/W	0x0	Selects the VCO3 divide value for OUT4/OUT6 CML Output Drivers from: [0] -> VCO3, or [2] -> VCO3 Div By 1 to 7. ROM=Y, EEPROM=Y 0x0 = Disabled 0x1 = Bypass 0x2 = Reserved 0x4 = Div By 1 to 7

1.475 R866 Register (Offset = 0x362) [Reset = 0x5C]

R866 is shown in Table 1-477.

Return to the Summary Table.

Table 1-477. R866 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	PLL3_VCO_BUF_2REF_EN	R/W	0x1	Enables the VCO3 Div By 2 buffer output driver to [0] -> APLL1 and [1] -> APLL2 reference input for cascade mode. ROM=Y, EEPROM=Y
5	PLL3_2X_PLLN_EN	R/W	0x0	Enables the frequency doubler available in the VCO3 to APLL3 N-divider/DPLL3 feedback clock path. ROM=Y, EEPROM=N
4:3	PLL3_PLLN_OUT_EN	R/W	0x3	Enables the VCO3 output buffer driver to [0] -> APLL3 N-divider and [1] -> DPLL3 feedback clock input mux. ROM=Y, EEPROM=Y
2	PLL3_WIN_DET_DRVR_EN	R/W	0x1	Enables the VCO3 Div By 2 Buffer output driver to reference window detectors input buffer, ROM=Y, EEPROM=N
1:0	PLL3_VCO_BUF_FB_TDC_EN	R/W	0x0	Enables VCO3 Div By 4 Buffer output driver to TDC1 and TDC2 for cascade mode [0] = TDC1 driver enable [1] = TDC2 driver enable ROM=Y, EEPROM=N

1.476 R961 Register (Offset = 0x3C1) [Reset = 0x10]

R961 is shown in Table 1-478.

Return to the Summary Table.

Table 1-478. R961 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_0_HSDSBOOST	R/W	0x0	OUT0 HSDS Mode Boosted Amplitude. When this bit is set to 0, OUT_0_AMP can select from 300mVpp to 600mVpp. When this bit is set to 1, OUT_0_AMP can select from 600mVpp to 900mVpp. ROM=Y, EEPROM=Y
6:5	OUT_0_AMP	R/W	0x0	OUT0 Amplitude Select. Selects one of four available single-ended Vpp amplitudes for LVDS, LVPECL, and HSDS outputs. For CMOS mode only: Enables individual terminals for CMOS output, which will otherwise be in high-Z state ([Bit 0] enables -> OUT0_P as CMOS, [Bit 1] enables OUT0_N as CMOS). ROM=Y, EEPROM=Y 0x0 = 00 0x1 = 01 0x2 = 10 0x3 = 11
4	OUT_0_LDO_EN	R/W	0x1	Except for current savings this bit should always be 1. This bit must be set to enable Vcm output LDO on OUT0. ROM=Y, EEPROM=Y

Table 1-478. R961 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OUT_0_STATIC_LOW	R/W	0x0	When OUT0 is forced to a static output, this bit determines if the output voltage will be 0: Static Low 1: Static High ROM=Y, EEPROM=N 0x0 = L 0x1 = H
2:0	OUT_0_FMT	R/W	0x0	Selects the output type which the multimode output driver will generate. ROM=Y, EEPROM=Y 0x0 = DISABLED 0x1 = LVDS 0x2 = LVPECL 0x3 = HSDS 0x4 = CMOS

1.477 R962 Register (Offset = 0x3C2) [Reset = 0x0]

R962 is shown in Table 1-479.

Return to the Summary Table.

Table 1-479. R962 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	OUT_0_P_INVERT_POLARITY	R/W	0x0	OUT0P CMOS Invert Polarity. Setting this bit inverts the polarity of the positive terminal of OUT0 for CMOS outputs. ROM=Y, EEPROM=N
2	OUT_0_N_INVERT_POLARITY	R/W	0x0	OUT0N CMOS Invert Polarity. Setting this bit inverts the polarity of the negative terminal of OUT0 for CMOS outputs. ROM=Y, EEPROM=N
1	OUT_0_P_FORCELOW	R/W	0x0	OUT0P CMOS Force Low. Setting this bit forces the positive terminal of OUT0 low. ROM=Y, EEPROM=N
0	OUT_0_N_FORCELOW	R/W	0x0	OUT0N CMOS Force Low. Setting this bit forces the negative terminal of OUT0 low. ROM=Y, EEPROM=N

1.478 R963 Register (Offset = 0x3C3) [Reset = 0x0]

R963 is shown in Table 1-480.

Return to the Summary Table.

Table 1-480. R963 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_CONFIGURATION	R/W	0x0	OUT0 Configuration. Selects from CH0 Bypass, CH1 Bypass, CHDIV0, CHDIV1, CH0/2 low-noise divide by two path, SYSREF, SYSREF + Analog Delay, or static DC H/L. ROM=N, EEPROM=N 0x0 = CH0/2 0x14 = CHDIV1 0x20 = SYSREF+ADLY 0x21 = SYSREF 0x22 = Static DC 0x28 = CHDIV0 0x40 = CH1 Bypass 0x80 = CH0 Bypass

1.479 R964 Register (Offset = 0x3C4) [Reset = 0x70]

R964 is shown in Table 1-481.

Return to the Summary Table.

Table 1-481. R964 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_1_HSDSBOOST	R/W	0x0	OUT1 HSDS Mode Boosted Amplitude. When this bit is set to 0, OUT_1_AMP can select from 300mVpp to 600mVpp. When this bit is set to 1, OUT_1_AMP can select from 600mVpp to 900mVpp. ROM=Y, EEPROM=Y
6:5	OUT_1_AMP	R/W	0x3	OUT1 Amplitude Select. Selects one of four available single-ended Vpp amplitudes for LVDS, LVPECL, and HSDS outputs. For CMOS mode only: Enables individual terminals for CMOS output, which will otherwise be in high-Z state ([0] -> OUT1P, [1] -> OUT1N). ROM=Y, EEPROM=Y 0x0 = 00 0x1 = 01 0x2 = 10 0x3 = 11
4	OUT_1_LDO2_SEL	R/W	0x1	Except for current savings this bit should always be 1. Rename to OUT_1_LDO_EN. This bit must be set to enable Vcm output LDO on OUT1. ROM=Y, EEPROM=Y
3	OUT_1_STATIC_LOW	R/W	0x0	When OUT1 is forced to a static output, this bit determines if the output voltage will be 0=Static Low or 1=Static High ROM=Y, EEPROM=N 0x0 = L 0x1 = H
2:0	OUT_1_FMT	R/W	0x0	Selects the output type which the multimode output driver will generate. ROM=Y, EEPROM=Y 0x0 = DISABLED 0x1 = LVDS 0x2 = LVPECL 0x3 = HSDS 0x4 = CMOS

1.480 R965 Register (Offset = 0x3C5) [Reset = 0x0]

R965 is shown in Table 1-482.

Return to the Summary Table.

Table 1-482. R965 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	OUT_1_P_INVERT_POLARITY	R/W	0x0	OUT1P CMOS Invert Polarity. Setting this bit inverts the polarity of the positive terminal of OUT1 for CMOS outputs. ROM=Y, EEPROM=N
2	OUT_1_N_INVERT_POLARITY	R/W	0x0	OUT1N CMOS Invert Polarity. Setting this bit inverts the polarity of the negative terminal of OUT1 for CMOS outputs. ROM=Y, EEPROM=N
1	OUT_1_P_FORCELOW	R/W	0x0	OUT1P CMOS Force Low. Setting this bit forces the positive terminal of OUT1 low. ROM=Y, EEPROM=N
0	OUT_1_N_FORCELOW	R/W	0x0	OUT1N CMOS Force Low. Setting this bit forces the negative terminal of OUT1 low. ROM=Y, EEPROM=N

1.481 R966 Register (Offset = 0x3C6) [Reset = 0x0]

R966 is shown in Table 1-483.

Return to the Summary Table.

Table 1-483. R966 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_1_CONFIGURATION	R/W	0x0	OUT1 Configuration. Selects from CH0 Bypass, CH1 Bypass, CHDIV0, CHDIV1, CH0/2 low-noise divide by two path, SYSREF, SYSREF + Analog Delay, or static DC H/L. ROM=N, EEPROM=N 0x0 = CH0/2 0x14 = CHDIV1 0x20 = SYSREF+ADLY 0x21 = SYSREF 0x22 = Static DC 0x28 = CHDIV0 0x40 = CH1 Bypass 0x80 = CH0 Bypass

1.482 R967 Register (Offset = 0x3C7) [Reset = 0x0]

R967 is shown in Table 1-484.

Return to the Summary Table.

Table 1-484. R967 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	OUT_0_1_CMOS_OUT_VOLTAGE_SEL	R/W	0x0	CMOS LDO Voltage. Selects CMOS LDO voltage. ROM=Y, EEPROM=Y 0x0 = 1.8V 0x1 = 2.65V
0	OUT_0_1_CMOS_OUT_LDO_EN	R/W	0x0	CMOS LDO Enable. Enables LDO used for CMOS outputs. Must be enabled for CMOS mode. ROM=Y, EEPROM=Y

1.483 R968 Register (Offset = 0x3C8) [Reset = 0x0]

R968 is shown in Table 1-485.

Return to the Summary Table.

Table 1-485. R968 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:1	OUT_0_1_ZDM_TDC_SEL	R/W	0x0	Select zero delay output to TDC's ROM=Y, EEPROM=N 0x0 = None 0x1 = TDC1 0x2 = TDC2 0x4 = TDC3
0	OUT_0_1_ZDM_EN	R/W	0x0	Enable the output from CH_DIV0_1 to be used as DPLL feedback input for zero delay mode ROM=Y, EEPROM=N

1.484 R969 Register (Offset = 0x3C9) [Reset = 0x30]

R969 is shown in Table 1-486.

Return to the Summary Table.

Table 1-486. R969 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_0_1_DIV_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
5	OUT_0_1_DIV_SYNC_EN	R/W	0x1	OUT0_1 Divider Sync Enable. Enables synchronization of chandiv and div2 dividers at startup for OUT0_1. ROM=Y, EEPROM=N
4	OUT_0_1_SR_DIV_SYNC_EN	R/W	0x1	OUT0_1 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers at startup for OUT0_1. ROM=Y, EEPROM=N
3	OUT_0_1_CH0_CHAN_POL_SEL	R/W	0x0	OUT0_1 Ch0 ChanDiv Polarity Select. When cleared, this bit inverts the polarity of the input to the Ch0 channel divider. ROM=Y, EEPROM=N
2	OUT_0_1_CH1_CHAN_POL_SEL	R/W	0x0	OUT0_1 Ch1 ChanDiv Polarity Select. When cleared, this bit inverts the polarity of the input to the Ch1 channel divider. ROM=Y, EEPROM=N
1	OUT_0_1_CH0_DIV_EN	R/W	0x0	OUT0_1 Ch0 ChanDiv Enable. Enables the Ch0 channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y
0	OUT_0_1_CH1_DIV_EN	R/W	0x0	OUT0_1 Ch1 ChanDiv Enable. Enables the Ch1 channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.485 R972 Register (Offset = 0x3CC) [Reset = 0x2]

R972 is shown in Table 1-487.

Return to the Summary Table.

Table 1-487. R972 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	OUT_0_1_CH0_CH_DIV_SR_MUX_CLK_SEL	R/W	0x1	OUT0_1 Ch0 ChanDiv to SYSREF Input Clock Select. When set, the Ch0 channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N 0x0 = POS POL to SR_DIV 0x1 = NEG POL to SR_DIV
0	RESERVED	R	0x0	Reserved

1.486 R973 Register (Offset = 0x3CD) [Reset = 0x0]

R973 is shown in Table 1-488.

Return to the Summary Table.

Table 1-488. R973 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	OUT_0_1_CLK_IN_FANOUT	R/W	0x0	OUT0_1 input clock fanout. Distributes the input clock to the channel dividers and the standalone divide-by-2s. ROM=Y, EEPROM=Y 0x0 = DISABLED 0x3 = IN1 to CHDIV1 0x4 = IN0 to SYSREF 0x7 = IN0 to SYSREF, IN1 to CHDIV1 0xC = IN0 to CHDIV0 0xF = IN0 to CHDIV0, IN1 to CHDIV1 0x10 = IN0 to CH0/2 (OUT0) 0x13 = IN0 to CH0/2 (OUT0), IN1 to CHDIV1 (OUT1) 0x14 = IN0 to CH0/2 (OUT0) and SYSREF (OUT1) 0x1C = IN0 to CH0/2 (OUT0) and CHDIV0 (OUT1) 0x20 = IN0 to CH0/2 (OUT1) 0x23 = IN0 to CH0/2 (OUT1), IN1 to CHDIV1 (OUT0) 0x24 = IN0 to CH0/2 (OUT1) and SYSREF (OUT0) 0x2C = IN0 to CH0/2 (OUT1) and CHDIV0 (OUT0) 0x30 = IN0 to CH0/2 (OUT0 and OUT1)
1:0	RESERVED	R	0x0	Reserved

1.487 R974 Register (Offset = 0x3CE) [Reset = 0x0]

R974 is shown in Table 1-489.

Return to the Summary Table.

Table 1-489. R974 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_0_1_CH0_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 975

1.488 R975 Register (Offset = 0x3CF) [Reset = 0x0]

R975 is shown in Table 1-490.

Return to the Summary Table.

Table 1-490. R975 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_CH0_CH_STATIC_OFFSET	R/W	0x0	OUT0_1 Ch0 ChanDiv Static Offset. Code which delays the output of the Ch0 channel divider. ROM=Y, EEPROM=Y

1.489 R976 Register (Offset = 0x3D0) [Reset = 0x0]

R976 is shown in Table 1-491.

Return to the Summary Table.

Table 1-491. R976 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_0_1_CH1_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 977

1.490 R977 Register (Offset = 0x3D1) [Reset = 0x0]

R977 is shown in Table 1-492.

Return to the Summary Table.

Table 1-492. R977 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_CH1_CH_STATIC_OFFSET	R/W	0x0	OUT0_1 Ch1 ChanDiv Static Offset. Code which delays the output of the Ch1 channel divider. ROM=Y, EEPROM=Y

1.491 R978 Register (Offset = 0x3D2) [Reset = 0x0]

R978 is shown in Table 1-493.

Return to the Summary Table.

Table 1-493. R978 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_0_1_CH0_CH_DIV_11:8	R/W	0x0	See Register 979

1.492 R979 Register (Offset = 0x3D3) [Reset = 0x8]

R979 is shown in Table 1-494.

Return to the Summary Table.

Table 1-494. R979 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_CH0_CH_DIV	R/W	0x8	OUT0_1 Ch0 Channel Divider (ChanDiv) Divide Value. ROM=Y, EEPROM=Y

1.493 R980 Register (Offset = 0x3D4) [Reset = 0x0]

R980 is shown in Table 1-495.

Return to the Summary Table.

Table 1-495. R980 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_0_1_CH1_CH_DIV_11:8	R/W	0x0	See Register 981

1.494 R981 Register (Offset = 0x3D5) [Reset = 0x8]

R981 is shown in Table 1-496.

Return to the Summary Table.

Table 1-496. R981 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_CH1_CH_DIV	R/W	0x8	OUT0_1 Ch1 Channel Divider (ChanDiv) Divide Value. ROM=Y, EEPROM=Y

1.495 R982 Register (Offset = 0x3D6) [Reset = 0x0]

R982 is shown in Table 1-497.

Return to the Summary Table.

Table 1-497. R982 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_0_1_SR_ANA_DELAY	R/W	0x0	OUT0_1 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.496 R983 Register (Offset = 0x3D7) [Reset = 0x0]

R983 is shown in Table 1-498.

Return to the Summary Table.

Table 1-498. R983 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_0_1_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT0_1 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_0_1_SR_ANA_DELAY_EN	R/W	0x0	OUT0_1 SYSREF Analog Delay Enable. ROM=Y, EEPROM=N
3	OUT_0_1_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x0	OUT0_1 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N
2:0	OUT_0_1_SR_ANA_DELAY_RANGE	R/W	0x0	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calcualted as (OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / SYSREF source frequency. For OUT_x_y_SR_CH_DIV_BYPASS = 1 SYSREF source frequency = VCO post divider frequency up to maximum of 1500 MHz if or OUT_x_y_SR_CH_DIV_BYPASS = 0 the channel divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.497 R984 Register (Offset = 0x3D8) [Reset = 0x0]

R984 is shown in Table 1-499.

Return to the Summary Table.

Table 1-499. R984 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-499. R984 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	OUT_0_1_SR_DDLY	R/W	0x0	OUT0_1 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.498 R985 Register (Offset = 0x3D9) [Reset = 0x0]

R985 is shown in Table 1-500.

Return to the Summary Table.

Table 1-500. R985 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_0_1_SR_DIV_19:16	R/W	0x0	See Register 987

1.499 R986 Register (Offset = 0x3DA) [Reset = 0x0]

R986 is shown in Table 1-501.

Return to the Summary Table.

Table 1-501. R986 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_SR_DIV_15:8	R/W	0x0	See Register 987

1.500 R987 Register (Offset = 0x3DB) [Reset = 0x2]

R987 is shown in Table 1-502.

Return to the Summary Table.

Table 1-502. R987 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_SR_DIV	R/W	0x2	OUT0_1 SYSREF Divide Value. ROM=Y, EEPROM=N

1.501 R988 Register (Offset = 0x3DC) [Reset = 0x0]

R988 is shown in Table 1-503.

Return to the Summary Table.

Table 1-503. R988 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_0_1_SR_DIV_STATIC_OFFSET_14:8	R/W	0x0	See Register 989

1.502 R989 Register (Offset = 0x3DD) [Reset = 0x0]

R989 is shown in Table 1-504.

Return to the Summary Table.

Table 1-504. R989 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_SR_DIV_STATIC_OFFSET	R/W	0x0	OUT0_1 SYSREF Divider Static Offset. Static offset code which delays the output of the SYSREF divider. ROM=Y, EEPROM=N

1.503 R990 Register (Offset = 0x3DE) [Reset = 0x0]

R990 is shown in Table 1-505.

Return to the Summary Table.

Table 1-505. R990 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_0_1_SR_GPIO_EN	R/W	0x0	Enable SYSREF to digtop used for 1PPS phase validation, SYSREF_REQ and SYSREF GPIO output ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:2	OUT_0_1_PULSE_COUNT	R/W	0x0	OUT0_1 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
1:0	OUT_0_1_SR_MODE	R/W	0x0	OUT0_1 SYSREF Mode. Selects Pulser mode, Continuous mode, or None. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.504 R991 Register (Offset = 0x3DF) [Reset = 0x0]

R991 is shown in Table 1-506.

Return to the Summary Table.

Table 1-506. R991 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_0_1_SR_CH0_DIV_BYPASS	R/W	0x0	OUT0_1 cascaded SYSREF bypass mux. If set, bypasses CHDIV0 for the SYSREF input clock. This is useful for minimizing the step size of the digital delay adjustments on the SYSREF clock. ROM=Y, EEPROM=N 0x0 = ChanDiv input to SysRef 0x1 = Bypass ChanDiv
4:0	RESERVED	R	0x0	Reserved

1.505 R1024 Register (Offset = 0x400) [Reset = 0x33]

R1024 is shown in Table 1-507.

Return to the Summary Table.

Table 1-507. R1024 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_2_HSDSBOOST	R/W	0x0	OUT2 HSDS Mode Boosted Amplitude. When this bit is set to 0, OUT_2_AMP can select from 300mVpp to 600mVpp. When this bit is set to 1, OUT_2_AMP can select from 600mVpp to 900mVpp. ROM=Y, EEPROM=Y

Table 1-507. R1024 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	OUT_2_AMP	R/W	0x3	OUT2 Amplitude Select. Selects one of four available single-ended Vpp amplitudes for LVDS, LVPECL, and HSDS outputs. ROM=Y, EEPROM=Y
3	RESERVED	R	0x0	Reserved
2:0	OUT_2_FMT	R/W	0x3	Selects the output type which the multimode output driver will generate. ROM=Y, EEPROM=Y 0x0 = DISABLED 0x1 = LVDS 0x2 = LVPECL 0x3 = HSDS

1.506 R1025 Register (Offset = 0x401) [Reset = 0x0]

R1025 is shown in Table 1-508.

Return to the Summary Table.

Table 1-508. R1025 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:3	RESERVED	R	0x0	Reserved
2:0	OUT_2_CONFIGURATION	R/W	0x0	OUT2 Mode Configuration ROM=N, EEPROM=N 0x2 = Static DC 0x3 = CHDIV 0x4 = BYPASS

1.507 R1026 Register (Offset = 0x402) [Reset = 0xB]

R1026 is shown in Table 1-509.

Return to the Summary Table.

Table 1-509. R1026 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_2_CHAN_POL_SEL	R/W	0x0	OUT2 ChanDiv Polarity Select. When cleared, this bit inverts the polarity of the input to the channel divider. ROM=Y, EEPROM=N
6:5	OUT_2_CLK_MUX	R/W	0x0	OUT2 Input Clock Select. Selects the input clock which will be used to drive the output. ROM=N, EEPROM=N 0x0 = PLL1_SEC 0x1 = PLL2 0x2 = PLL1_PRI
4	RESERVED	R	0x0	Reserved
3	OUT_2_DIV_EN	R/W	0x1	OUT2 ChanDiv Enable. Enables the channel divider. Note: SYSREF/ chandiv mode must be configured separately. ROM=Y, EEPROM=Y
2:0	OUT_2_CH_MUX_SEL	R/W	0x3	OUT2 Clock Enable. Bit 2, if set, passes the selected VCO1 clock (VCO1P or VCO1S), to the second stage of clock selection. Bit 1 and Bit0 enable the selected clock to drive the channel divider and the channel divider retimer respectively. ROM=Y, EEPROM=Y 0x0 = PLL2->BYPASS 0x3 = PLL2->CHDIV 0x4 = PLL1->BYPASS 0x7 = PLL1->CHDIV

1.508 R1027 Register (Offset = 0x403) [Reset = 0x8]

R1027 is shown in Table 1-510.

Return to the Summary Table.

Table 1-510. R1027 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	OUT_2_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
3	OUT_2_SYNC_EN	R/W	0x1	OUT2 ChanDiv Sync Enable. Enables synchronization of chandiv dividers at startup for OUT2. ROM=Y, EEPROM=N
2:0	RESERVED	R	0x0	Reserved

1.509 R1028 Register (Offset = 0x404) [Reset = 0x0]

R1028 is shown in Table 1-511.

Return to the Summary Table.

Table 1-511. R1028 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_2_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1029

1.510 R1029 Register (Offset = 0x405) [Reset = 0x0]

R1029 is shown in Table 1-512.

Return to the Summary Table.

Table 1-512. R1029 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_2_CH_STATIC_OFFSET	R/W	0x0	OUT2 ChanDiv Static Offset. Static offset code which delays the output of the channel divider. ROM=Y, EEPROM=Y

1.511 R1030 Register (Offset = 0x406) [Reset = 0x0]

R1030 is shown in Table 1-513.

Return to the Summary Table.

Table 1-513. R1030 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_2_CH_DIV_11:8	R/W	0x0	See Register 1031

1.512 R1031 Register (Offset = 0x407) [Reset = 0x5]

R1031 is shown in Table 1-514.

Return to the Summary Table.

Table 1-514. R1031 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_2_CH_DIV	R/W	0x5	OUT2 ChanDiv Divide Value. ROM=Y, EEPROM=Y

1.513 R1056 Register (Offset = 0x420) [Reset = 0x1]

R1056 is shown in Table 1-515.

Return to the Summary Table.

Table 1-515. R1056 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_3_HSDSBOOST	R/W	0x0	OUT3 HSDS Mode Boosted Amplitude. When this bit is set to 0, OUT_3_AMP can select from 300mVpp to 600mVpp. When this bit is set to 1, OUT_3_AMP can select from 600mVpp to 900mVpp. ROM=Y, EEPROM=Y
5:4	OUT_3_AMP	R/W	0x0	OUT3 Amplitude Select. Selects one of four available single-ended Vpp amplitudes for LVDS, LVPECL, and HSDS outputs. ROM=Y, EEPROM=Y
3	RESERVED	R	0x0	Reserved
2:0	OUT_3_FMT	R/W	0x1	Selects the output type which the multimode output driver will generate. ROM=Y, EEPROM=Y 0x0 = DISABLED 0x1 = LVDS 0x2 = LVPECL 0x3 = HSDS

1.514 R1057 Register (Offset = 0x421) [Reset = 0x0]

R1057 is shown in Table 1-516.

Return to the Summary Table.

Table 1-516. R1057 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:3	RESERVED	R	0x0	Reserved
2:0	OUT_3_CONFIGURATION	R/W	0x0	OUT3 Mode Configuration. ROM=Y, EEPROM=Y 0x2 = Static DC 0x3 = CHDIV 0x4 = BYPASS

1.515 R1058 Register (Offset = 0x422) [Reset = 0xB]

R1058 is shown in Table 1-517.

Return to the Summary Table.

Table 1-517. R1058 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_3_CHAN_POL_SEL	R/W	0x0	OUT3 ChanDiv Polarity Select. When cleared, this bit inverts the polarity of the input to the channel divider. ROM=Y, EEPROM=N

Table 1-517. R1058 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:5	OUT_3_CLK_MUX	R/W	0x0	OUT3 Input Clock Select. Selects the input clock which will be used to drive the output. ROM=N, EEPROM=N 0x0 = PLL1_SEC 0x1 = PLL2 0x2 = PLL1_PRI
4	RESERVED	R	0x0	Reserved
3	OUT_3_DIV_EN	R/W	0x1	OUT3 ChanDiv Enable. Enables the channel divider. Note: SYSREF/ chandiv mode must be configured separately. ROM=Y, EEPROM=Y
2:0	OUT_3_CH_MUX_SEL	R/W	0x3	OUT3 Clock Enable. Bit 2, if set, passes the selected VCO1 clock (VCO1P or VCO1S), to the second stage of clock selection. Bit 1 and Bit0 enable the selected clock to drive the channel divider and the channel divider retimer respectively. ROM=Y, EEPROM=Y 0x0 = PLL2->BYPASS 0x3 = PLL2->CHDIV 0x4 = PLL1->BYPASS 0x7 = PLL1->CHDIV

1.516 R1059 Register (Offset = 0x423) [Reset = 0x8]

R1059 is shown in Table 1-518.

Return to the Summary Table.

Table 1-518. R1059 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	OUT_3_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
3	OUT_3_SYNC_EN	R/W	0x1	OUT3 ChanDiv Sync Enable. Enables synchronization of chandiv dividers at startup for OUT3. ROM=Y, EEPROM=N
2:0	RESERVED	R	0x0	Reserved

1.517 R1060 Register (Offset = 0x424) [Reset = 0x0]

R1060 is shown in Table 1-519.

Return to the Summary Table.

Table 1-519. R1060 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_3_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1061

1.518 R1061 Register (Offset = 0x425) [Reset = 0x0]

R1061 is shown in Table 1-520.

Return to the Summary Table.

Table 1-520. R1061 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_3_CH_STATIC_OFFSET	R/W	0x0	OUT3 ChanDiv Static Offset. Static offset code which delays the output of the channel divider. ROM=Y, EEPROM=Y

1.519 R1062 Register (Offset = 0x426) [Reset = 0x0]

R1062 is shown in Table 1-521.

Return to the Summary Table.

Table 1-521. R1062 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_3_CH_DIV_11:8	R/W	0x0	See Register 1063

1.520 R1063 Register (Offset = 0x427) [Reset = 0x4]

R1063 is shown in Table 1-522.

Return to the Summary Table.

Table 1-522. R1063 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_3_CH_DIV	R/W	0x4	OUT3 ChanDiv Divide Value. ROM=Y, EEPROM=Y

1.521 R1088 Register (Offset = 0x440) [Reset = 0x4]

R1088 is shown in Table 1-523.

Return to the Summary Table.

Table 1-523. R1088 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:0	OUT_4_5_SR_ANA_DLY_BIASTRIM	R/W	0x4	Channel Analog Delay Bias Trim ROM=N, EEPROM=Y

1.522 R1089 Register (Offset = 0x441) [Reset = 0x0]

R1089 is shown in Table 1-524.

Return to the Summary Table.

Table 1-524. R1089 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_4_HSDSBOOST	R/W	0x0	OUT4 HSDS Mode Boosted Amplitude. When this bit is set to 0, OUT_4_AMP can select from 300mVpp to 600mVpp. When this bit is set to 1, OUT_4_AMP can select from 600mVpp to 900mVpp. ROM=Y, EEPROM=Y
6:5	OUT_4_AMP	R/W	0x0	OUT4 Amplitude Select. Selects one of four available single-ended Vpp amplitudes for LVDS, LVPECL, HSDS, and CML outputs. ROM=Y, EEPROM=Y
4:3	RESERVED	R	0x0	Reserved

Table 1-524. R1089 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	OUT_4_FMT	R/W	0x0	Selects the output type which the multimode output driver will generate. ROM=Y, EEPROM=Y 0x0 = DISABLED 0x1 = LVDS 0x2 = LVPECL 0x3 = HSDS 0x4 = Reserved 0x5 = CML

1.523 R1090 Register (Offset = 0x442) [Reset = 0x0]

R1090 is shown in Table 1-525.

Return to the Summary Table.

Table 1-525. R1090 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4:0	OUT_4_CONFIGURATION		0x0	0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.524 R1091 Register (Offset = 0x443) [Reset = 0x60]

R1091 is shown in Table 1-526.

Return to the Summary Table.

Table 1-526. R1091 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_5_HSDSBOOST	R/W	0x0	OUT5 HSDS Mode Boosted Amplitude. When this bit is set to 0, OUT_5_AMP can select from 300mVpp to 600mVpp. When this bit is set to 1, OUT_5_AMP can select from 600mVpp to 900mVpp. ROM=Y, EEPROM=Y
6:5	OUT_5_AMP	R/W	0x3	OUT5 Amplitude Select. Selects one of four available single-ended Vpp amplitudes for LVDS, LVPECL, and HSDS outputs. ROM=Y, EEPROM=Y
4:3	OUT_5_PREPWR	R/W	0x0	Output buffer predriver power setting ROM=Y, EEPROM=Y
2:0	OUT_5_FMT	R/W	0x0	Selects the output type which the multimode output driver will generate. ROM=Y, EEPROM=Y 0x0 = DISABLED 0x1 = LVDS 0x2 = LVPECL 0x3 = HSDS

1.525 R1092 Register (Offset = 0x444) [Reset = 0x0]

R1092 is shown in Table 1-527.

Return to the Summary Table.

Table 1-527. R1092 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4:0	OUT_5_CONFIGURATION		0x0	0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.526 R1093 Register (Offset = 0x445) [Reset = 0x0]

R1093 is shown in Table 1-528.

Return to the Summary Table.

Table 1-528. R1093 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_4_5_DIV_SYNC_EN	R/W	0x0	OUT4_5 Divider Sync Enable. Enables synchronization of chandiv dividers at startup for OUT4_5. ROM=Y, EEPROM=N
4	OUT_4_5_SR_DIV_SYNC_EN	R/W	0x0	OUT4_5 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers at startup for OUT4_5. ROM=Y, EEPROM=N
3:2	RESERVED	R	0x0	Reserved
1	OUT_4_5_CHAN_POL_SEL	R/W	0x0	OUT4_5 ChanDiv Polarity Select. When cleared, this bit inverts the polarity of the input to the channel divider. ROM=Y, EEPROM=N
0	OUT_4_5_DIV_EN	R/W	0x0	OUT4_5 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.527 R1094 Register (Offset = 0x446) [Reset = 0xC]

R1094 is shown in Table 1-529.

Return to the Summary Table.

Table 1-529. R1094 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_4_5_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
6	OUT_4_5_ZDM_EN	R/W	0x0	OUT4_5 zero delay output enable ROM=Y, EEPROM=N
5	OUT_4_5_CLK_IN_SEL	R/W	0x0	OUT4_5 Input Clock Select. Selects the input clock which will be used to drive the output: 0 = VCO2, 1 = VCO3 ROM=Y, EEPROM=Y 0x0 = PLL2 0x1 = PLL3
4	OUT_4_5_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT4_5 ChanDiv to SYSREF Clock Select. When set, the channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N

Table 1-529. R1094 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	OUT_4_5_CH_MUX_SEL	R/W	0xC	OUT4_5 Input Clock Enable. Enables the selected clock to various inputs: [0] -> ChanDiv, [1] -> ChanDiv Retimer, [2] -> Div2 to OUT4, [3] -> Div2 to OUT5 ROM=Y, EEPROM=Y 0x0 = OFF 0x1 = SYSREF 0x3 = CHDIV 0x4 = DIV2->OUT8 0x5 = DIV2->OUT8, SYSREF->OUT9 0x7 = DIV2->OUT8, CHDIV->OUT9 0x8 = DIV2->OUT9 0x9 = SYSREF->OUT8, DIV2->OUT9 0xB = CHDIV->OUT8, DIV2->OUT9 0xC = DIV2->OUT8, DIV2->OUT9

1.528 R1095 Register (Offset = 0x447) [Reset = 0x0]

R1095 is shown in Table 1-530.

Return to the Summary Table.

Table 1-530. R1095 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_4_5_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1096

1.529 R1096 Register (Offset = 0x448) [Reset = 0x0]

R1096 is shown in Table 1-531.

Return to the Summary Table.

Table 1-531. R1096 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_4_5_CH_STATIC_OFFSET	R/W	0x0	OUT4_5 ChanDiv Static Offset. Static offset code which delays the output of the channel divider. ROM=Y, EEPROM=Y

1.530 R1097 Register (Offset = 0x449) [Reset = 0x0]

R1097 is shown in Table 1-532.

Return to the Summary Table.

Table 1-532. R1097 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_4_5_CH_DIV_11:8	R/W	0x0	See Register 1098

1.531 R1098 Register (Offset = 0x44A) [Reset = 0x2]

R1098 is shown in Table 1-533.

Return to the Summary Table.

Table 1-533. R1098 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_4_5_CH_DIV	R/W	0x2	OUT4_5 ChanDiv Divide Value. ROM=Y, EEPROM=Y

1.532 R1099 Register (Offset = 0x44B) [Reset = 0x10]

R1099 is shown in Table 1-534.

Return to the Summary Table.

Table 1-534. R1099 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_4_5_SR_ANA_DELAY	R/W	0x10	OUT4_5 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.533 R1100 Register (Offset = 0x44C) [Reset = 0x4]

R1100 is shown in Table 1-535.

Return to the Summary Table.

Table 1-535. R1100 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_4_5_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT4_5 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_4_5_SR_ANA_DELAY_EN	R/W	0x0	OUT4_5 SYSREF Analog Delay Enable. Enables the analog delay generator. Set to a 0 to save power if analog delay generator is not needed. ROM=Y, EEPROM=N
3	OUT_4_5_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x0	OUT4_5 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N
2:0	OUT_4_5_SR_ANA_DELAY_RANGE	R/W	0x4	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calcualted as (OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / SYSREF source frequency. For OUT_x_y_SR_CH_DIV_BYPASS = 1 SYSREF source frequency = VCO post divider frequency up to maximum of 1500 MHz if or OUT_x_y_SR_CH_DIV_BYPASS = 0 the channel divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.534 R1101 Register (Offset = 0x44D) [Reset = 0x0]

R1101 is shown in Table 1-536.

Return to the Summary Table.

Table 1-536. R1101 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_4_5_SR_DDLY	R/W	0x0	OUT4_5 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.535 R1102 Register (Offset = 0x44E) [Reset = 0x0]

R1102 is shown in Table 1-537.

Return to the Summary Table.

Table 1-537. R1102 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_4_5_SR_DIV_19:16	R/W	0x0	See Register 1104

1.536 R1103 Register (Offset = 0x44F) [Reset = 0x0]

R1103 is shown in Table 1-538.

Return to the Summary Table.

Table 1-538. R1103 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_4_5_SR_DIV_15:8	R/W	0x0	See Register 1104

1.537 R1104 Register (Offset = 0x450) [Reset = 0x2]

R1104 is shown in Table 1-539.

Return to the Summary Table.

Table 1-539. R1104 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_4_5_SR_DIV	R/W	0x2	OUT4_5 SYSREF Divide Value. ROM=Y, EEPROM=N

1.538 R1105 Register (Offset = 0x451) [Reset = 0x0]

R1105 is shown in Table 1-540.

Return to the Summary Table.

Table 1-540. R1105 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_4_5_SR_DIV_STATIC_OFFSET_14:8	R/W	0x0	See Register 1106

1.539 R1106 Register (Offset = 0x452) [Reset = 0x0]

R1106 is shown in Table 1-541.

Return to the Summary Table.

Table 1-541. R1106 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_4_5_SR_DIV_STATIC_OFFSET	R/W	0x0	OUT4_5 SYSREF Divider Static Offset. Static offset code which delays the output of the SYSREF divider. ROM=Y, EEPROM=N

1.540 R1107 Register (Offset = 0x453) [Reset = 0x0]

R1107 is shown in Table 1-542.

Return to the Summary Table.

Table 1-542. R1107 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	OUT_4_5_PULSE_COUNT	R/W	0x0	OUT4_5 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
2	OUT_4_5_SR_GPIO_EN	R/W	0x0	Enables SYSREF to digital for SYSREF_req and GPIO output ROM=Y, EEPROM=N
1:0	OUT_4_5_SR_MODE	R/W	0x0	OUT4_5 SYSREF Mode. When this bit is set, the SYSREF operates in Continuous Mode. When cleared, the SYSREF operates in Pulse Mode. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.541 R1108 Register (Offset = 0x454) [Reset = 0x0]

R1108 is shown in Table 1-543.

Return to the Summary Table.

Table 1-543. R1108 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4	OUT_4_5_SR_CH_DIV_BYPASS	R/W	0x0	OUT4_5 cascaded SYSREF bypass mux. If set, bypasses OUT4_5 channel divider for the SYSREF input clock. This is useful for minimizing the step size of the digital delay adjustments on the SYSREF clock. ROM=Y, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.542 R1121 Register (Offset = 0x461) [Reset = 0x0]

R1121 is shown in Table 1-544.

Return to the Summary Table.

Table 1-544. R1121 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_6_HSDSBOOST	R/W	0x0	OUT6 HSDS Mode Boosted Amplitude. When this bit is set to 0, OUT_6_AMP can select from 300mVpp to 600mVpp. When this bit is set to 1, OUT_6_AMP can select from 600mVpp to 900mVpp. ROM=Y, EEPROM=Y
6:5	OUT_6_AMP	R/W	0x0	OUT6 Amplitude Select. Selects one of four available single-ended Vpp amplitudes for LVDS, LVPECL, HSDS, and CML outputs. ROM=Y, EEPROM=Y
4:3	RESERVED	R	0x0	Reserved
2:0	OUT_6_FMT	R/W	0x0	Selects the output type which the multimode output driver will generate. ROM=Y, EEPROM=Y 0x0 = DISABLED 0x1 = LVDS 0x2 = LVPECL 0x3 = HSDS 0x4 = Reserved 0x5 = CML

1.543 R1122 Register (Offset = 0x462) [Reset = 0x0]

R1122 is shown in Table 1-545.

Return to the Summary Table.

Table 1-545. R1122 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4:0	OUT_6_CONFIGURATION		0x0	0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.544 R1123 Register (Offset = 0x463) [Reset = 0x60]

R1123 is shown in Table 1-546.

Return to the Summary Table.

Table 1-546. R1123 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_7_HSDSBOOST	R/W	0x0	OUT7 HSDS Mode Boosted Amplitude. When this bit is set to 0, OUT_7_AMP can select from 300mVpp to 600mVpp. When this bit is set to 1, OUT_7_AMP can select from 600mVpp to 900mVpp. ROM=Y, EEPROM=Y
6:5	OUT_7_AMP	R/W	0x3	OUT7 Amplitude Select. Selects one of four available single-ended Vpp amplitudes for LVDS, LVPECL, and HSDS outputs. ROM=Y, EEPROM=Y
4:3	OUT_7_PREPWR	R/W	0x0	Output buffer predriver power setting ROM=Y, EEPROM=Y

Table 1-546. R1123 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	OUT_7_FMT	R/W	0x0	Selects the output type which the multimode output driver will generate. ROM=Y, EEPROM=Y 0x0 = DISABLED 0x1 = LVDS 0x2 = LVPECL 0x3 = HSDS

1.545 R1124 Register (Offset = 0x464) [Reset = 0x0]

R1124 is shown in Table 1-547.

Return to the Summary Table.

Table 1-547. R1124 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4:0	OUT_7_CONFIGURATION		0x0	0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.546 R1125 Register (Offset = 0x465) [Reset = 0x0]

R1125 is shown in Table 1-548.

Return to the Summary Table.

Table 1-548. R1125 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_6_7_DIV_SYNC_EN	R/W	0x0	OUT6_7 Divider Sync Enable. Enables synchronization of chandiv dividers at startup for OUT6_7. ROM=Y, EEPROM=N
4	OUT_6_7_SR_DIV_SYNC_EN	R/W	0x0	OUT6_7 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers at startup for OUT6_7. ROM=Y, EEPROM=N
3:2	RESERVED	R	0x0	Reserved
1	OUT_6_7_CHAN_POL_SEL	R/W	0x0	OUT6_7 ChanDiv Polarity Select. When cleared, this bit inverts the polarity of the input to the channel divider. ROM=Y, EEPROM=N
0	OUT_6_7_DIV_EN	R/W	0x0	OUT6_7 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.547 R1126 Register (Offset = 0x466) [Reset = 0xC]

R1126 is shown in Table 1-549.

Return to the Summary Table.

Table 1-549. R1126 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_6_7_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
6	RESERVED	R	0x0	Reserved
5	OUT_6_7_CLK_IN_SEL	R/W	0x0	OUT6_7 Input Clock Select. Selects the input clock which will be used to drive the output: 0 = VCO2, 1 = VCO3 ROM=Y, EEPROM=Y 0x0 = PLL2 0x1 = PLL3
4	OUT_6_7_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT6_7 ChanDiv to SYSREF Clock Select. When set, the channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N
3:0	OUT_6_7_CH_MUX_SEL	R/W	0xC	OUT6_7 Input Clock Enable. Enables the selected clock to various inputs: [0] -> ChanDiv, [1] -> ChanDiv Retimer, [2] -> Div2 to OUT6, [3] -> Div2 to OUT7 ROM=Y, EEPROM=Y 0x0 = OFF 0x1 = SYSREF 0x3 = CHDIV 0x4 = DIV2->OUT8 0x5 = DIV2->OUT8, SYSREF->OUT9 0x7 = DIV2->OUT8, CHDIV->OUT9 0x8 = DIV2->OUT9 0x9 = SYSREF->OUT8, DIV2->OUT9 0xB = CHDIV->OUT8, DIV2->OUT9 0xC = DIV2->OUT8, DIV2->OUT9

1.548 R1127 Register (Offset = 0x467) [Reset = 0x0]

R1127 is shown in Table 1-550.

Return to the Summary Table.

Table 1-550. R1127 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_6_7_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1128

1.549 R1128 Register (Offset = 0x468) [Reset = 0x0]

R1128 is shown in Table 1-551.

Return to the Summary Table.

Table 1-551. R1128 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_6_7_CH_STATIC_OFFSET	R/W	0x0	OUT6_7 ChanDiv Static Offset. Static offset code which delays the output of the channel divider. ROM=Y, EEPROM=Y

1.550 R1129 Register (Offset = 0x469) [Reset = 0x0]

R1129 is shown in Table 1-552.

Return to the Summary Table.

Table 1-552. R1129 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved

Table 1-552. R1129 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	OUT_6_7_CH_DIV_11:8	R/W	0x0	See Register 1130

1.551 R1130 Register (Offset = 0x46A) [Reset = 0x2]

R1130 is shown in Table 1-553.

Return to the Summary Table.

Table 1-553. R1130 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_6_7_CH_DIV	R/W	0x2	OUT6_7 ChanDiv Divide Value. ROM=Y, EEPROM=Y

1.552 R1131 Register (Offset = 0x46B) [Reset = 0x0]

R1131 is shown in Table 1-554.

Return to the Summary Table.

Table 1-554. R1131 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_6_7_SR_ANA_DELAY	R/W	0x0	OUT6_7 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.553 R1132 Register (Offset = 0x46C) [Reset = 0x4]

R1132 is shown in Table 1-555.

Return to the Summary Table.

Table 1-555. R1132 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_6_7_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT6_7 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_6_7_SR_ANA_DELAY_EN	R/W	0x0	OUT6_7 SYSREF Analog Delay Enable. Enables the analog delay generator. Set to a 0 to save power if analog delay generator is not needed. ROM=Y, EEPROM=N
3	OUT_6_7_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x0	OUT6_7 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N

Table 1-555. R1132 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	OUT_6_7_SR_ANA_DELAY_RANGE	R/W	0x4	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calcualted as (OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / SYSREF source frequency. For OUT_x_y_SR_CH_DIV_BYPASS = 1 SYSREF source frequency = VCO post divider frequency up to maximum of 1500 MHz if or OUT_x_y_SR_CH_DIV_BYPASS = 0 the channel divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.554 R1133 Register (Offset = 0x46D) [Reset = 0x0]

R1133 is shown in Table 1-556.

Return to the Summary Table.

Table 1-556. R1133 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_6_7_SR_DDLY	R/W	0x0	OUT6_7 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.555 R1134 Register (Offset = 0x46E) [Reset = 0x0]

R1134 is shown in Table 1-557.

Return to the Summary Table.

Table 1-557. R1134 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_6_7_SR_DIV_19:16	R/W	0x0	See Register 1136

1.556 R1135 Register (Offset = 0x46F) [Reset = 0x0]

R1135 is shown in Table 1-558.

Return to the Summary Table.

Table 1-558. R1135 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_6_7_SR_DIV_15:8	R/W	0x0	See Register 1136

1.557 R1136 Register (Offset = 0x470) [Reset = 0x2]

R1136 is shown in Table 1-559.

Return to the Summary Table.

Table 1-559. R1136 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_6_7_SR_DIV	R/W	0x2	OUT6_7 SYSREF Divide Value. ROM=Y, EEPROM=N

1.558 R1137 Register (Offset = 0x471) [Reset = 0x0]

R1137 is shown in Table 1-560.

Return to the Summary Table.

Table 1-560. R1137 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_6_7_SR_DIV_STATIC_OFFSET_14:8	R/W	0x0	See Register 1138

1.559 R1138 Register (Offset = 0x472) [Reset = 0x0]

R1138 is shown in Table 1-561.

Return to the Summary Table.

Table 1-561. R1138 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_6_7_SR_DIV_STATIC_OFFSET	R/W	0x0	OUT6_7 SYSREF Divider Static Offset. Static offset code which delays the output of the SYSREF divider. ROM=Y, EEPROM=N

1.560 R1139 Register (Offset = 0x473) [Reset = 0x0]

R1139 is shown in Table 1-562.

Return to the Summary Table.

Table 1-562. R1139 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	OUT_6_7_PULSE_COUNT	R/W	0x0	OUT6_7 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
2	OUT_6_7_SR_GPIO_EN	R/W	0x0	Enable SYSREF to digital for sysre_req and GPIO output ROM=Y, EEPROM=N
1:0	OUT_6_7_SR_MODE	R/W	0x0	OUT6_7 SYSREF Mode. When this bit is set, the SYSREF operates in Continuous Mode. When cleared, the SYSREF operates in PULSE MODE. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.561 R1140 Register (Offset = 0x474) [Reset = 0x0]

R1140 is shown in Table 1-563.

Return to the Summary Table.

Table 1-563. R1140 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4	OUT_6_7_SR_CH_DIV_BYPASS	R/W	0x0	OUT6_7 cascaded SYSREF bypass mux. If set, bypasses OUT6_7 channel divider for the SYSREF input clock. This is useful for minimizing the step size of the digital delay adjustments on the SYSREF clock. ROM=Y, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.562 R1153 Register (Offset = 0x481) [Reset = 0x1]

R1153 is shown in Table 1-564.

Return to the Summary Table.

Table 1-564. R1153 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_8_HSDSBOOST	R/W	0x0	OUT8 HSDS Mode Boosted Amplitude. When this bit is set to 0, OUT_8_AMP can select from 300mVpp to 600mVpp. When this bit is set to 1, OUT_8_AMP can select from 600mVpp to 900mVpp. ROM=Y, EEPROM=Y
6:5	OUT_8_AMP	R/W	0x0	OUT8 Amplitude Select. Selects one of four available single-ended Vpp amplitudes for LVDS, LVPECL, and HSDS outputs. ROM=Y, EEPROM=Y
4:3	RESERVED	R	0x0	Reserved
2:0	OUT_8_FMT	R/W	0x1	Selects the output type which the multimode output driver will generate. ROM=Y, EEPROM=Y 0x0 = DISABLED 0x1 = LVDS 0x2 = LVPECL 0x3 = HSDS

1.563 R1154 Register (Offset = 0x482) [Reset = 0x0]

R1154 is shown in Table 1-565.

Return to the Summary Table.

Table 1-565. R1154 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4:0	OUT_8_CONFIGURATION		0x0	0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.564 R1155 Register (Offset = 0x483) [Reset = 0x19]

R1155 is shown in Table 1-566.

Return to the Summary Table.

Table 1-566. R1155 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_9_HSDSBOOST	R/W	0x0	OUT9 HSDS Mode Boosted Amplitude. When this bit is set to 0, OUT_9_AMP can select from 300mVpp to 600mVpp. When this bit is set to 1, OUT_9_AMP can select from 600mVpp to 900mVpp. ROM=Y, EEPROM=Y
6:5	OUT_9_AMP	R/W	0x0	OUT9 Amplitude Select. Selects one of four available single-ended Vpp amplitudes for LVDS, LVPECL, and HSDS outputs. ROM=Y, EEPROM=Y
4:3	OUT_9_PREPWR	R/W	0x3	Output buffer predriver power setting ROM=Y, EEPROM=Y
2:0	OUT_9_FMT	R/W	0x1	Selects the output type which the multimode output driver will generate. ROM=Y, EEPROM=Y 0x0 = DISABLED 0x1 = LVDS 0x2 = LVPECL 0x3 = HSDS

1.565 R1156 Register (Offset = 0x484) [Reset = 0x0]

R1156 is shown in Table 1-567.

Return to the Summary Table.

Table 1-567. R1156 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4:0	OUT_9_CONFIGURATION		0x0	0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.566 R1157 Register (Offset = 0x485) [Reset = 0x31]

R1157 is shown in Table 1-568.

Return to the Summary Table.

Table 1-568. R1157 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_8_9_DIV_SYNC_EN	R/W	0x1	OUT8_9 Divider Sync Enable. Enables synchronization of chandiv dividers at startup for OUT8_9. ROM=Y, EEPROM=N
4	OUT_8_9_SR_DIV_SYNC_EN	R/W	0x1	OUT8_9 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers at startup for OUT8_9. ROM=Y, EEPROM=N
3:2	RESERVED	R	0x0	Reserved
1	OUT_8_9_CHAN_POL_SEL	R/W	0x0	OUT8_9 ChanDiv Polarity Select. When cleared, this bit inverts the polarity of the input to the channel divider. ROM=Y, EEPROM=N
0	OUT_8_9_DIV_EN	R/W	0x1	OUT8_9 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.567 R1158 Register (Offset = 0x486) [Reset = 0x23]

R1158 is shown in Table 1-569.

Return to the Summary Table.

Table 1-569. R1158 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_8_9_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
6	RESERVED	R	0x0	Reserved
5	OUT_8_9_CLK_IN_SEL	R/W	0x1	OUT8_9 Input Clock Select. Selects the input clock which will be used to drive the output: 0 = VCO2, 1 = VCO3 ROM=Y, EEPROM=Y 0x0 = PLL2 0x1 = PLL3
4	OUT_8_9_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT8_9 ChanDiv to SYSREF Clock Select. When set, the channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N
3:0	OUT_8_9_CH_MUX_SEL	R/W	0x3	OUT8_9 Input Clock Enable. Enables the selected clock to various inputs: [0] -> ChanDiv, [1] -> ChanDiv Retimer, [2] -> Div2 to OUT8, [3] -> Div2 to OUT9 ROM=Y, EEPROM=Y 0x0 = OFF 0x1 = SYSREF 0x3 = CHDIV 0x4 = DIV2->OUT8 0x5 = DIV2->OUT8, SYSREF->OUT9 0x7 = DIV2->OUT8, CHDIV->OUT9 0x8 = DIV2->OUT9 0x9 = SYSREF->OUT8, DIV2->OUT9 0xB = CHDIV->OUT8, DIV2->OUT9 0xC = DIV2->OUT8, DIV2->OUT9

1.568 R1159 Register (Offset = 0x487) [Reset = 0x0]

R1159 is shown in Table 1-570.

Return to the Summary Table.

Table 1-570. R1159 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_8_9_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1160

1.569 R1160 Register (Offset = 0x488) [Reset = 0x0]

R1160 is shown in Table 1-571.

Return to the Summary Table.

Table 1-571. R1160 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_8_9_CH_STATIC_OFFSET	R/W	0x0	OUT8_9 ChanDiv Static Offset. Static offset code which delays the output of the channel divider. ROM=Y, EEPROM=Y

1.570 R1161 Register (Offset = 0x489) [Reset = 0x0]

R1161 is shown in Table 1-572.

Return to the Summary Table.

Table 1-572. R1161 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_8_9_CH_DIV_11:8	R/W	0x0	See Register 1162

1.571 R1162 Register (Offset = 0x48A) [Reset = 0x4]

R1162 is shown in Table 1-573.

Return to the Summary Table.

Table 1-573. R1162 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_8_9_CH_DIV	R/W	0x4	OUT8_9 ChanDiv Divide Value. ROM=Y, EEPROM=Y

1.572 R1163 Register (Offset = 0x48B) [Reset = 0x0]

R1163 is shown in Table 1-574.

Return to the Summary Table.

Table 1-574. R1163 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_8_9_SR_ANA_DELAY	R/W	0x0	OUT8_9 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.573 R1164 Register (Offset = 0x48C) [Reset = 0x0]

R1164 is shown in Table 1-575.

Return to the Summary Table.

Table 1-575. R1164 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_8_9_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT8_9 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_8_9_SR_ANA_DELAY_EN	R/W	0x0	OUT8_9 SYSREF Analog Delay Enable. Enables the analog delay generator. Set to a 0 to save power if analog delay generator is not needed. ROM=Y, EEPROM=N
3	OUT_8_9_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x0	OUT8_9 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N

Table 1-575. R1164 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	OUT_8_9_SR_ANA_DELAY_RANGE	R/W	0x0	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calcualted as (OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / SYSREF source frequency. For OUT_x_y_SR_CH_DIV_BYPASS = 1 SYSREF source frequency = VCO post divider frequency up to maximum of 1500 MHz if or OUT_x_y_SR_CH_DIV_BYPASS = 0 the channel divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.574 R1165 Register (Offset = 0x48D) [Reset = 0x6]

R1165 is shown in Table 1-576.

Return to the Summary Table.

Table 1-576. R1165 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_8_9_SR_DDLY	R/W	0x6	OUT8_9 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.575 R1166 Register (Offset = 0x48E) [Reset = 0x0]

R1166 is shown in Table 1-577.

Return to the Summary Table.

Table 1-577. R1166 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_8_9_SR_DIV_19:16	R/W	0x0	See Register 1168

1.576 R1167 Register (Offset = 0x48F) [Reset = 0x1]

R1167 is shown in Table 1-578.

Return to the Summary Table.

Table 1-578. R1167 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_8_9_SR_DIV_15:8	R/W	0x1	See Register 1168

1.577 R1168 Register (Offset = 0x490) [Reset = 0x0]

R1168 is shown in Table 1-579.

Return to the Summary Table.

Table 1-579. R1168 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_8_9_SR_DIV	R/W	0x0	OUT8_9 SYSREF Divide Value. ROM=Y, EEPROM=N

1.578 R1169 Register (Offset = 0x491) [Reset = 0x0]

R1169 is shown in Table 1-580.

Return to the Summary Table.

Table 1-580. R1169 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_8_9_SR_DIV_STATIC_OFFSET_14:8	R/W	0x0	See Register 1170

1.579 R1170 Register (Offset = 0x492) [Reset = 0x0]

R1170 is shown in Table 1-581.

Return to the Summary Table.

Table 1-581. R1170 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_8_9_SR_DIV_STATIC_OFFSET	R/W	0x0	OUT8_9 SYSREF Divider Static Offset. Static offset code which delays the output of the SYSREF divider. ROM=Y, EEPROM=N

1.580 R1171 Register (Offset = 0x493) [Reset = 0x0]

R1171 is shown in Table 1-582.

Return to the Summary Table.

Table 1-582. R1171 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	OUT_8_9_PULSE_COUNT	R/W	0x0	OUT8_9 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
2	OUT_8_9_SR_GPIO_EN	R/W	0x0	Enable SYSREF to digital for sysre_req and GPIO output ROM=Y, EEPROM=N
1:0	OUT_8_9_SR_MODE	R/W	0x0	OUT8_9 SYSREF Mode. When this bit is set, the SYSREF operates in Continuous Mode. When cleared, the SYSREF operates in PULSE MODE. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.581 R1185 Register (Offset = 0x4A1) [Reset = 0x1]

R1185 is shown in Table 1-583.

Return to the Summary Table.

Table 1-583. R1185 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_10_HSDSBOOST	R/W	0x0	OUT10 HSDS Mode Boosted Amplitude. When this bit is set to 0, OUT_10_AMP can select from 300mVpp to 600mVpp. When this bit is set to 1, OUT_10_AMP can select from 600mVpp to 900mVpp. ROM=Y, EEPROM=Y
6:5	OUT_10_AMP	R/W	0x0	OUT10 Amplitude Select. Selects one of four available single-ended Vpp amplitudes for LVDS, LVPECL, and HSDS outputs. ROM=Y, EEPROM=Y
4:3	RESERVED	R	0x0	Reserved
2:0	OUT_10_FMT	R/W	0x1	Selects the output type which the multimode output driver will generate. ROM=Y, EEPROM=Y 0x0 = DISABLED 0x1 = LVDS 0x2 = LVPECL 0x3 = HSDS

1.582 R1186 Register (Offset = 0x4A2) [Reset = 0x0]

R1186 is shown in Table 1-584.

Return to the Summary Table.

Table 1-584. R1186 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4:0	OUT_10_CONFIGURATION		0x0	0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.583 R1187 Register (Offset = 0x4A3) [Reset = 0x19]

R1187 is shown in Table 1-585.

Return to the Summary Table.

Table 1-585. R1187 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_11_HSDSBOOST	R/W	0x0	OUT11 HSDS Mode Boosted Amplitude. When this bit is set to 0, OUT_11_AMP can select from 300mVpp to 600mVpp. When this bit is set to 1, OUT_11_AMP can select from 600mVpp to 900mVpp. ROM=Y, EEPROM=Y
6:5	OUT_11_AMP	R/W	0x0	OUT11 Amplitude Select. Selects one of four available single-ended Vpp amplitudes for LVDS, LVPECL, and HSDS outputs. ROM=Y, EEPROM=Y
4:3	OUT_11_PREPWR	R/W	0x3	Output buffer predriver power setting ROM=Y, EEPROM=Y
2:0	OUT_11_FMT	R/W	0x1	Selects the output type which the multimode output driver will generate. ROM=Y, EEPROM=Y 0x0 = DISABLED 0x1 = LVDS 0x2 = LVPECL 0x3 = HSDS

1.584 R1188 Register (Offset = 0x4A4) [Reset = 0x0]

R1188 is shown in Table 1-586.

Return to the Summary Table.

Table 1-586. R1188 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4:0	OUT_11_CONFIGURATION		0x0	0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.585 R1189 Register (Offset = 0x4A5) [Reset = 0x30]

R1189 is shown in Table 1-587.

Return to the Summary Table.

Table 1-587. R1189 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_10_11_DIV_SYNC_EN	R/W	0x1	OUT10_11 Divider Sync Enable. Enables synchronization of chandiv dividers at startup for OUT10_11. ROM=Y, EEPROM=N
4	OUT_10_11_SR_DIV_SYNC_EN	R/W	0x1	OUT10_11 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers at startup for OUT10_11. ROM=Y, EEPROM=N
3:2	RESERVED	R	0x0	Reserved
1	OUT_10_11_CHAN_POL_SEL	R/W	0x0	OUT10_11 ChanDiv Polarity Select. When cleared, this bit inverts the polarity of the input to the channel divider. ROM=Y, EEPROM=N
0	OUT_10_11_DIV_EN	R/W	0x0	OUT10_11 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.586 R1190 Register (Offset = 0x4A6) [Reset = 0x21]

R1190 is shown in Table 1-588.

Return to the Summary Table.

Table 1-588. R1190 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_10_11_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
6	OUT_10_11_ZDM_EN	R/W	0x0	OUT10_11 zero delay output enable. ROM=Y, EEPROM=N
5	OUT_10_11_CLK_IN_SEL	R/W	0x1	OUT10_11 Input Clock Select. Selects the input clock which will be used to drive the output: 0 = VCO2, 1 = VCO3 ROM=Y, EEPROM=Y 0x0 = PLL2 0x1 = PLL3
4	OUT_10_11_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT10_11 ChanDiv to SYSREF Clock Select. When set, the channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N

Table 1-588. R1190 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	OUT_10_11_CH_MUX_SEL	R/W	0x1	OUT10_11 Input Clock Enable. Enables the selected clock to various inputs: [0] -> ChanDiv, [1] -> ChanDiv Retimer, [2] -> Div2 to OUT10, [3] -> Div2 to OUT11 ROM=Y, EEPROM=Y 0x0 = OFF 0x1 = SYSREF 0x3 = CHDIV 0x4 = DIV2->OUT8 0x5 = DIV2->OUT8, SYSREF->OUT9 0x7 = DIV2->OUT8, CHDIV->OUT9 0x8 = DIV2->OUT9 0x9 = SYSREF->OUT8, DIV2->OUT9 0xB = CHDIV->OUT8, DIV2->OUT9 0xC = DIV2->OUT8, DIV2->OUT9

1.587 R1191 Register (Offset = 0x4A7) [Reset = 0x0]

R1191 is shown in Table 1-589.

Return to the Summary Table.

Table 1-589. R1191 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_10_11_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1192

1.588 R1192 Register (Offset = 0x4A8) [Reset = 0x0]

R1192 is shown in Table 1-590.

Return to the Summary Table.

Table 1-590. R1192 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_10_11_CH_STATIC_OFFSET	R/W	0x0	OUT10_11 ChanDiv Static Offset. Static offset code which delays the output of the channel divider. ROM=Y, EEPROM=Y

1.589 R1193 Register (Offset = 0x4A9) [Reset = 0x0]

R1193 is shown in Table 1-591.

Return to the Summary Table.

Table 1-591. R1193 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_10_11_CH_DIV_11:8	R/W	0x0	See Register 1194

1.590 R1194 Register (Offset = 0x4AA) [Reset = 0x4]

R1194 is shown in Table 1-592.

Return to the Summary Table.

Table 1-592. R1194 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_10_11_CH_DIV	R/W	0x4	OUT10_11 ChanDiv Divide Value. ROM=Y, EEPROM=Y

1.591 R1195 Register (Offset = 0x4AB) [Reset = 0x0]

R1195 is shown in Table 1-593.

Return to the Summary Table.

Table 1-593. R1195 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_10_11_SR_ANA_DELAY	R/W	0x0	OUT10_11 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.592 R1196 Register (Offset = 0x4AC) [Reset = 0x0]

R1196 is shown in Table 1-594.

Return to the Summary Table.

Table 1-594. R1196 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_10_11_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT10_11 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_10_11_SR_ANA_DELAY_EN	R/W	0x0	OUT10_11 SYSREF Analog Delay Enable. Enables the analog delay generator. Set to a 0 to save power if analog delay generator is not needed. ROM=Y, EEPROM=N
3	OUT_10_11_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x0	OUT10_11 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N
2:0	OUT_10_11_SR_ANA_DELAY_RANGE	R/W	0x0	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calcualted as (OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / SYSREF source frequency. For OUT_x_y_SR_CH_DIV_BYPASS = 1 SYSREF source frequency = VCO post divider frequency up to maximum of 1500 MHz if or OUT_x_y_SR_CH_DIV_BYPASS = 0 the channel divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.593 R1197 Register (Offset = 0x4AD) [Reset = 0x6]

R1197 is shown in Table 1-595.

Return to the Summary Table.

Table 1-595. R1197 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_10_11_SR_DDLY	R/W	0x6	OUT10_11 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.594 R1198 Register (Offset = 0x4AE) [Reset = 0x0]

R1198 is shown in Table 1-596.

Return to the Summary Table.

Table 1-596. R1198 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_10_11_SR_DIV_19:16	R/W	0x0	See Register 1200

1.595 R1199 Register (Offset = 0x4AF) [Reset = 0x1]

R1199 is shown in Table 1-597.

Return to the Summary Table.

Table 1-597. R1199 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_10_11_SR_DIV_15:8	R/W	0x1	See Register 1200

1.596 R1200 Register (Offset = 0x4B0) [Reset = 0x0]

R1200 is shown in Table 1-598.

Return to the Summary Table.

Table 1-598. R1200 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_10_11_SR_DIV	R/W	0x0	OUT10_11 SYSREF Divide Value. ROM=Y, EEPROM=N

1.597 R1201 Register (Offset = 0x4B1) [Reset = 0x0]

R1201 is shown in Table 1-599.

Return to the Summary Table.

Table 1-599. R1201 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_10_11_SR_DIV_STATIC_OFFSET_14:8	R/W	0x0	See Register 1202

1.598 R1202 Register (Offset = 0x4B2) [Reset = 0x0]

R1202 is shown in Table 1-600.

Return to the Summary Table.

Table 1-600. R1202 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_10_11_SR_DIV_STATIC_OFFSET	R/W	0x0	OUT10_11 SYSREF Divider Static Offset. Static offset code which delays the output of the SYSREF divider. ROM=Y, EEPROM=N

1.599 R1203 Register (Offset = 0x4B3) [Reset = 0x0]

R1203 is shown in Table 1-601.

Return to the Summary Table.

Table 1-601. R1203 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	OUT_10_11_PULSE_COUNT	R/W	0x0	OUT10_11 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
2	OUT_10_11_SR_GPIO_EN	R/W	0x0	Enable SYSREF to digital for sysre_req and GPIO output ROM=Y, EEPROM=N
1:0	OUT_10_11_SR_MODE	R/W	0x0	OUT10_11 SYSREF Mode. When this bit is set, the SYSREF operates in Continuous Mode. When cleared, the SYSREF operates in PULSE MODE. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.600 R1204 Register (Offset = 0x4B4) [Reset = 0x10]

R1204 is shown in Table 1-602.

Return to the Summary Table.

Table 1-602. R1204 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4	OUT_10_11_SR_CH_DIV_BYPASS	R/W	0x1	OUT10_11 cascaded SYSREF bypass mux. If set, bypasses OUT10_11 channel divider for the SYSREF input clock. This is useful for minimizing the step size of the digital delay adjustments on the SYSREF clock. ROM=Y, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.601 R1217 Register (Offset = 0x4C1) [Reset = 0x0]

R1217 is shown in Table 1-603.

Return to the Summary Table.

Table 1-603. R1217 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_12_HSDSBOOST	R/W	0x0	OUT12 HSDS Mode Boosted Amplitude. When this bit is set to 0, OUT_12_AMP can select from 300mVpp to 600mVpp. When this bit is set to 1, OUT_12_AMP can select from 600mVpp to 900mVpp. ROM=Y, EEPROM=Y
6:5	OUT_12_AMP	R/W	0x0	OUT12 Amplitude Select. Selects one of four available single-ended Vpp amplitudes for LVDS, LVPECL, and HSDS outputs. ROM=Y, EEPROM=Y
4:3	RESERVED	R	0x0	Reserved
2:0	OUT_12_FMT	R/W	0x0	Selects the output type which the multimode output driver will generate. ROM=Y, EEPROM=Y 0x0 = DISABLED 0x1 = LVDS 0x2 = LVPECL 0x3 = HSDS

1.602 R1218 Register (Offset = 0x4C2) [Reset = 0x0]

R1218 is shown in Table 1-604.

Return to the Summary Table.

Table 1-604. R1218 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4:0	OUT_12_CONFIGURATION		0x0	0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.603 R1219 Register (Offset = 0x4C3) [Reset = 0x60]

R1219 is shown in Table 1-605.

Return to the Summary Table.

Table 1-605. R1219 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_13_HSDSBOOST	R/W	0x0	OUT13 HSDS Mode Boosted Amplitude. When this bit is set to 0, OUT_13_AMP can select from 300mVpp to 600mVpp. When this bit is set to 1, OUT_13_AMP can select from 600mVpp to 900mVpp. ROM=Y, EEPROM=Y
6:5	OUT_13_AMP	R/W	0x3	OUT13 Amplitude Select. Selects one of four available single-ended Vpp amplitudes for LVDS, LVPECL, and HSDS outputs. ROM=Y, EEPROM=Y
4:3	OUT_13_PREPWR	R/W	0x0	Output buffer predriver power setting ROM=Y, EEPROM=Y
2:0	OUT_13_FMT	R/W	0x0	Selects the output type which the multimode output driver will generate. ROM=Y, EEPROM=Y 0x0 = DISABLED 0x1 = LVDS 0x2 = LVPECL 0x3 = HSDS

1.604 R1220 Register (Offset = 0x4C4) [Reset = 0x0]

R1220 is shown in Table 1-606.

Return to the Summary Table.

Table 1-606. R1220 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4:0	OUT_13_CONFIGURATION		0x0	0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.605 R1221 Register (Offset = 0x4C5) [Reset = 0x0]

R1221 is shown in Table 1-607.

Return to the Summary Table.

Table 1-607. R1221 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_12_13_DIV_SYNC_EN	R/W	0x0	OUT12_13 Divider Sync Enable. Enables synchronization of chandiv dividers at startup for OUT12_13. ROM=Y, EEPROM=N
4	OUT_12_13_SR_DIV_SYNC_EN	R/W	0x0	OUT12_13 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers at startup for OUT12_13. ROM=Y, EEPROM=N
3:2	RESERVED	R	0x0	Reserved
1	OUT_12_13_CHAN_POL_SEL	R/W	0x0	OUT12_13 ChanDiv Polarity Select. When cleared, this bit inverts the polarity of the input to the channel divider. ROM=Y, EEPROM=N
0	OUT_12_13_DIV_EN	R/W	0x0	OUT12_13 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.606 R1222 Register (Offset = 0x4C6) [Reset = 0x20]

R1222 is shown in Table 1-608.

Return to the Summary Table.

Table 1-608. R1222 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_12_13_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
6	RESERVED	R	0x0	Reserved
5	OUT_12_13_CLK_IN_SEL	R/W	0x1	OUT12_13 Input Clock Select. Selects the input clock which will be used to drive the output: 0 = VCO2, 1 = VCO3 ROM=Y, EEPROM=Y 0x0 = PLL2 0x1 = PLL3
4	OUT_12_13_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT12_13 ChanDiv to SYSREF Clock Select. When set, the channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N

Table 1-608. R1222 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	OUT_12_13_CH_MUX_SEL	R/W	0x0	OUT12_13 Input Clock Enable. Enables the selected clock to various inputs: [0] -> ChanDiv, [1] -> ChanDiv Retimer, [2] -> Div2 to OUT12, [3] -> Div2 to OUT13 ROM=Y, EEPROM=Y 0x0 = OFF 0x1 = SYSREF 0x3 = CHDIV 0x4 = DIV2->OUT8 0x5 = DIV2->OUT8, SYSREF->OUT9 0x7 = DIV2->OUT8, CHDIV->OUT9 0x8 = DIV2->OUT9 0x9 = SYSREF->OUT8, DIV2->OUT9 0xB = CHDIV->OUT8, DIV2->OUT9 0xC = DIV2->OUT8, DIV2->OUT9

1.607 R1223 Register (Offset = 0x4C7) [Reset = 0x0]

R1223 is shown in Table 1-609.

Return to the Summary Table.

Table 1-609. R1223 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_12_13_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1224

1.608 R1224 Register (Offset = 0x4C8) [Reset = 0x0]

R1224 is shown in Table 1-610.

Return to the Summary Table.

Table 1-610. R1224 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_12_13_CH_STATIC_OFFSET	R/W	0x0	OUT12_13 ChanDiv Static Offset. Static offset code which delays the output of the channel divider. ROM=Y, EEPROM=Y

1.609 R1225 Register (Offset = 0x4C9) [Reset = 0x0]

R1225 is shown in Table 1-611.

Return to the Summary Table.

Table 1-611. R1225 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_12_13_CH_DIV_11:8	R/W	0x0	See Register 1226

1.610 R1226 Register (Offset = 0x4CA) [Reset = 0x4]

R1226 is shown in Table 1-612.

Return to the Summary Table.

Table 1-612. R1226 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_12_13_CH_DIV	R/W	0x4	OUT12_13 ChanDiv Divide Value. ROM=Y, EEPROM=Y

1.611 R1227 Register (Offset = 0x4CB) [Reset = 0x0]

R1227 is shown in Table 1-613.

Return to the Summary Table.

Table 1-613. R1227 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_12_13_SR_ANA_DELAY	R/W	0x0	OUT12_13 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.612 R1228 Register (Offset = 0x4CC) [Reset = 0x0]

R1228 is shown in Table 1-614.

Return to the Summary Table.

Table 1-614. R1228 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_12_13_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT12_13 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_12_13_SR_ANA_DELAY_EN	R/W	0x0	OUT12_13 SYSREF Analog Delay Enable. Enables the analog delay generator. Set to a 0 to save power if analog delay generator is not needed. ROM=Y, EEPROM=N
3	OUT_12_13_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x0	OUT12_13 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N
2:0	OUT_12_13_SR_ANA_DELAY_RANGE	R/W	0x0	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calcualted as (OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / SYSREF source frequency. For OUT_x_y_SR_CH_DIV_BYPASS = 1 SYSREF source frequency = VCO post divider frequency up to maximum of 1500 MHz if or OUT_x_y_SR_CH_DIV_BYPASS = 0 the channel divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.613 R1229 Register (Offset = 0x4CD) [Reset = 0x0]

R1229 is shown in Table 1-615.

Return to the Summary Table.

Table 1-615. R1229 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_12_13_SR_DDLY	R/W	0x0	OUT12_13 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.614 R1230 Register (Offset = 0x4CE) [Reset = 0x0]

R1230 is shown in Table 1-616.

Return to the Summary Table.

Table 1-616. R1230 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_12_13_SR_DIV_19:16	R/W	0x0	See Register 1232

1.615 R1231 Register (Offset = 0x4CF) [Reset = 0x0]

R1231 is shown in Table 1-617.

Return to the Summary Table.

Table 1-617. R1231 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_12_13_SR_DIV_15:8	R/W	0x0	See Register 1232

1.616 R1232 Register (Offset = 0x4D0) [Reset = 0x1]

R1232 is shown in Table 1-618.

Return to the Summary Table.

Table 1-618. R1232 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_12_13_SR_DIV	R/W	0x1	OUT12_13 SYSREF Divide Value. ROM=Y, EEPROM=N

1.617 R1233 Register (Offset = 0x4D1) [Reset = 0x0]

R1233 is shown in Table 1-619.

Return to the Summary Table.

Table 1-619. R1233 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_12_13_SR_DIV_STATIC_OFFSET_14:8	R/W	0x0	See Register 1234

1.618 R1234 Register (Offset = 0x4D2) [Reset = 0x0]

R1234 is shown in Table 1-620.

Return to the Summary Table.

Table 1-620. R1234 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_12_13_SR_DIV_STATIC_OFFSET	R/W	0x0	OUT12_13 SYSREF Divider Static Offset. Static offset code which delays the output of the SYSREF divider. ROM=Y, EEPROM=N

1.619 R1235 Register (Offset = 0x4D3) [Reset = 0x0]

R1235 is shown in Table 1-621.

Return to the Summary Table.

Table 1-621. R1235 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	OUT_12_13_PULSE_COUNT	R/W	0x0	OUT12_13 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
2	OUT_12_13_SR_GPIO_EN	R/W	0x0	Enable SYSREF to digital for sysre_req and GPIO output ROM=Y, EEPROM=N
1:0	OUT_12_13_SR_MODE	R/W	0x0	OUT12_13 SYSREF Mode. When this bit is set, the SYSREF operates in Continuous Mode. When cleared, the SYSREF operates in PULSE MODE. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.620 R1236 Register (Offset = 0x4D4) [Reset = 0x0]

R1236 is shown in Table 1-622.

Return to the Summary Table.

Table 1-622. R1236 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4	OUT_12_13_SR_CH_DIV_BYPASS	R/W	0x0	OUT12_13 cascaded SYSREF bypass mux. If set, bypasses OUT12_13 channel divider for the SYSREF input clock. This is useful for minimizing the step size of the digital delay adjustments on the SYSREF clock. ROM=Y, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.621 R1248 Register (Offset = 0x4E0) [Reset = 0x0]

R1248 is shown in Table 1-623.

Return to the Summary Table.

Table 1-623. R1248 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-623. R1248 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	OUT_14_HSDSBOOST	R/W	0x0	OUT14 HSDS Mode Boosted Amplitude. When this bit is set to 0, OUT_14_AMP can select from 300mVpp to 600mVpp. When this bit is set to 1, OUT_14_AMP can select from 600mVpp to 900mVpp. ROM=Y, EEPROM=Y
5:4	OUT_14_AMP	R/W	0x0	OUT14 Amplitude Select. Selects one of four available single-ended Vpp amplitudes for LVDS, LVPECL, and HSDS outputs. ROM=Y, EEPROM=Y
3	RESERVED	R	0x0	Reserved
2:0	OUT_14_FMT	R/W	0x0	Selects the output type which the multimode output driver will generate. ROM=Y, EEPROM=Y 0x0 = DISABLED 0x1 = LVDS 0x2 = LVPECL 0x3 = HSDS

1.622 R1249 Register (Offset = 0x4E1) [Reset = 0x0]

R1249 is shown in Table 1-624.

Return to the Summary Table.

Table 1-624. R1249 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:3	RESERVED	R	0x0	Reserved
2:0	OUT_14_CONFIGURATION	R/W	0x0	OUT14 Configuration. 0x2 = Static DC 0x3 = CHDIV 0x4 = BYPASS

1.623 R1250 Register (Offset = 0x4E2) [Reset = 0xF]

R1250 is shown in Table 1-625.

Return to the Summary Table.

Table 1-625. R1250 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_14_CHAN_POL_SEL	R/W	0x0	OUT14 ChanDiv Polarity Select. When cleared, this bit inverts the polarity of the input to the channel divider. ROM=Y, EEPROM=N
6:5	OUT_14_CLK_MUX	R/W	0x0	OUT14 Input Clock Select. Selects the input clock which will be used to drive the output. ROM=N, EEPROM=N 0x0 = VCO3 0x1 = VCO2 0x2 = VCO1_PRI
4	RESERVED	R	0x0	Reserved
3	OUT_14_DIV_EN	R/W	0x1	OUT14 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

Table 1-625. R1250 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	OUT_14_CH_MUX_SEL	R/W	0x7	OUT14 Clock Enable. Bit 2, if set, passes the selected clock (VCO3 or VCO1P), to the second stage of clock selection. Bit 1 and Bit0 enable the selected clock to drive the channel divider and the channel divider retimer respectively. ROM=Y, EEPROM=Y 0x0 = PLL2->BYPASS 0x3 = PLL2->CHDIV 0x4 = PLL1,3->BYPASS 0x7 = PLL1,3->CHDIV

1.624 R1251 Register (Offset = 0x4E3) [Reset = 0x8]

R1251 is shown in Table 1-626.

Return to the Summary Table.

Table 1-626. R1251 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	OUT_14_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
3	OUT_14_SYNC_EN	R/W	0x1	OUT14 ChanDiv Sync Enable. Enables synchronization of chandiv dividers at startup for OUT14. ROM=Y, EEPROM=N
2:0	RESERVED	R	0x0	Reserved

1.625 R1252 Register (Offset = 0x4E4) [Reset = 0x0]

R1252 is shown in Table 1-627.

Return to the Summary Table.

Table 1-627. R1252 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_14_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1253

1.626 R1253 Register (Offset = 0x4E5) [Reset = 0x0]

R1253 is shown in Table 1-628.

Return to the Summary Table.

Table 1-628. R1253 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_14_CH_STATIC_OFFSET	R/W	0x0	OUT14 ChanDiv Static Offset. Static offset code which delays the output of the channel divider. ROM=Y, EEPROM=Y

1.627 R1254 Register (Offset = 0x4E6) [Reset = 0x0]

R1254 is shown in Table 1-629.

Return to the Summary Table.

Table 1-629. R1254 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_14_CH_DIV_11:8	R/W	0x0	See Register 1255

1.628 R1255 Register (Offset = 0x4E7) [Reset = 0xA]

R1255 is shown in Table 1-630.

Return to the Summary Table.

Table 1-630. R1255 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_14_CH_DIV	R/W	0xA	OUT14 ChanDiv Divide Value. ROM=Y, EEPROM=Y

1.629 R1280 Register (Offset = 0x500) [Reset = 0x0]

R1280 is shown in Table 1-631.

Return to the Summary Table.

Table 1-631. R1280 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_15_HSDSBOOST	R/W	0x0	OUT15 HSDS Mode Boosted Amplitude. When this bit is set to 0, OUT_15_AMP can select from 300mVpp to 600mVpp. When this bit is set to 1, OUT_15_AMP can select from 600mVpp to 900mVpp. ROM=Y, EEPROM=Y
5:4	OUT_15_AMP	R/W	0x0	OUT15 Amplitude Select. Selects one of four available single-ended Vpp amplitudes for LVDS, LVPECL, and HSDS outputs. ROM=Y, EEPROM=Y
3	RESERVED	R	0x0	Reserved
2:0	OUT_15_FMT	R/W	0x0	Selects the output type which the multimode output driver will generate. ROM=Y, EEPROM=Y 0x0 = DISABLED 0x1 = LVDS 0x2 = LVPECL 0x3 = HSDS

1.630 R1281 Register (Offset = 0x501) [Reset = 0x0]

R1281 is shown in Table 1-632.

Return to the Summary Table.

Table 1-632. R1281 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:3	RESERVED	R	0x0	Reserved
2:0	OUT_15_CONFIGURATION		0x0	0x2 = Static DC 0x3 = CHDIV 0x4 = BYPASS

1.631 R1282 Register (Offset = 0x502) [Reset = 0xF]

R1282 is shown in Table 1-633.

Return to the Summary Table.

Table 1-633. R1282 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_15_CHAN_POL_SEL	R/W	0x0	OUT15 ChanDiv Polarity Select. When cleared, this bit inverts the polarity of the input to the channel divider. ROM=Y, EEPROM=N
6:5	OUT_15_CLK_MUX	R/W	0x0	OUT15 Input Clock Select. Selects the input clock which will be used to drive the output. ROM=N, EEPROM=N 0x0 = VCO3 0x1 = VCO2 0x2 = VCO1_PRI
4	RESERVED	R	0x0	Reserved
3	OUT_15_DIV_EN	R/W	0x1	OUT15 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y
2:0	OUT_15_CH_MUX_SEL	R/W	0x7	OUT15 Clock Enable. Bit 2, if set, passes the selected VCO1 clock (VCO1P or VCO1S), to the second stage of clock selection. Bit 1 and Bit0 enable the selected clock to drive the channel divider and the channel divider retimer respectively. ROM=Y, EEPROM=Y 0x0 = PLL2->BYPASS 0x3 = PLL2->CHDIV 0x4 = PLL1,3->BYPASS 0x7 = PLL1,3->CHDIV

1.632 R1283 Register (Offset = 0x503) [Reset = 0x8]

R1283 is shown in Table 1-634.

Return to the Summary Table.

Table 1-634. R1283 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	OUT_15_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
3	OUT_15_SYNC_EN	R/W	0x1	OUT15 ChanDiv Sync Enable. Enables synchronization of chandiv dividers at startup for OUT15. ROM=Y, EEPROM=N
2:0	RESERVED	R	0x0	Reserved

1.633 R1284 Register (Offset = 0x504) [Reset = 0x0]

R1284 is shown in Table 1-635.

Return to the Summary Table.

Table 1-635. R1284 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_15_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1285

1.634 R1285 Register (Offset = 0x505) [Reset = 0x0]

R1285 is shown in Table 1-636.

Return to the Summary Table.

Table 1-636. R1285 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_15_CH_STATIC_OFFSET	R/W	0x0	OUT15 ChanDiv Static Offset. Static offset code which delays the output of the channel divider. ROM=Y, EEPROM=Y

1.635 R1286 Register (Offset = 0x506) [Reset = 0x0]

R1286 is shown in Table 1-637.

Return to the Summary Table.

Table 1-637. R1286 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_15_CH_DIV_11:8	R/W	0x0	See Register 1287

1.636 R1287 Register (Offset = 0x507) [Reset = 0xA]

R1287 is shown in Table 1-638.

Return to the Summary Table.

Table 1-638. R1287 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_15_CH_DIV	R/W	0xA	OUT15 ChanDiv Divide Value. ROM=Y, EEPROM=Y

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