Application Note

DS90UB941AS-Q1 DSI Bringup Guide

ABSTRACT

The DS90UB941AS-Q1 FPD-Link III serializer enables low latency, and highly flexible bridging from MIPI DSI to FPD-Link III in order to carry video data, audio data, control data, and other communications protocols such as I2C, and SPI over longer cable distances when paired with a DSI source.

The MIPI DSI protocol contains a wide feature set and flexibility in order fit as many applications as possible. As a result, system designers may struggle to understand how to properly configure and verify a complex DSI source in conjunction with FPD-Link. This guide will provide a common bring-up flow to help with DSI source configuration considerations and insight on how to resolve common system level problems when implementing a solution with DS90UB941AS-Q1

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1 Introduction

The DS90UB941AS-Q1 MIPI DSI serializer enables low latency bridging of a processor video source to a remote display panel or SoC across twisted pair or coaxial cabling. Since the DS90UB941AS-Q1 serializer is compatible with multiple FPD-Link deserializer products, it also enables easy video format conversion from MIPI DSI to MIPI CSI-2, OpenLDI, RGB, or other protocols depending on the application requirement.

When working with multiple video protocols and high speed serializer/deserializer devices, it is important for the system designer to have a systematic approach to determining the root cause of application issues so that they can be quickly resolved. This guide will walk through some of the key considerations that the system designer should be aware of, specifically regarding the MIPI DSI interface between the video source, and the DS90UB941AS-Q1 FPD-Link III serializer. Some examples will be provided for common issue symptoms and the approach to resolving the problem.

2 MIPI DSI Source Requirements

2.1 Supported DSI Modes

Before attempting to link a DSI source with DS90UB941AS-Q1, it is important to understand the supported MIPI DSI modes for the serializer. DS90UB941AS-Q1 supports MIPI DSI video mode only. It does not support MIPI DSI command mode for low speed communications with displays that use integrated video memory. The serializer supports four different RGB video formats:

- RGB888 (Packed Pixel Stream, 24-bit Format, Data Type 0x3E)
- RGB666 (Loosely Packed Pixel Stream, 18-bit format in Three Bytes, Data Type 0x2E)
- RGB666 (Packed Pixel Stream, 18-bit Format, Data Type 0x1E)
- RGB565 (Packed Pixel Stream, 16-bit Format, Data Type 0x0E)

The RGB video formats are automatically converted, if necessary, to 3-byte RGB888 for transmission over FPD-Link III. The DSI_BYTES_PER_PIXEL bits in DS90UB941AS-Q1 register 0x54 should be configured to match the expected pixel packing for the DSI port prior to enabling the DSI receiver. The default setting is 3 bytes-per-pixel which matches the RGB888 video format.

The DS90UB941AS-Q1 also supports pass-through of four DSI YCbCr video formats:

- Packed Pixel Stream, 12-bit YCbCr 4:2:0 Format, Data Type 0x3D
- Packed Pixel Stream, 16-bit YCbCr 4:2:2 Format, Data Type 0x2C
- Packed Pixel Stream, 24-bit YCbCr 4:2:2 Format, Data Type 0x1C
- Loosely Packed Pixel Stream, 20-bit YCbCr 4:2:2 Format, Data Type 0x0C

Each of these formats is aligned to the 3-bytes-per-pixel forward channel but is not converted to RGB888.

Most common display applications utilize RGB888 video format for 24 bits per pixel. It is important to note the expected video data type hex code based on the source configuration before progressing with the system bring-up. This will be useful to know as the received packet data type for the MIPI DSI input can be reported by the status registers of DS90UB941AS-Q1 in real time. If there are unexpected issues with the video output colors or there is no video at the display, this provides a quick way to check if the video format from the source is properly recognized by the DS90UB941AS-Q1 receiver.

DS90UB941AS-Q1 supports all three video mode operating configurations:

- Non-burst mode with sync pulses
- Non-burst mode with sync events
- Burst mode

2.2 Clocking Rates and Clock Type

DS90UB941AS-Q1 supports 25-105MHz PCLK rate over single FPD-Link, or 50-210 MHz PCLK rate over dual FPD-Link. For the MIPI DSI interface, DS90UB941AS-Q1 can support up to 1.5Gbps/lane data rate with up to 4 data lanes. Since MIPI DSI utilizes a DDR (Double Data Rate) clock, the DSI clock speed is typically expressed in MHz where the clock speed is 1/2 the per-lane data rate in Mbps. For example, with a DSI lane speed of 400 Mbps/lane, the MIPI D-PHY clock rate will be 200 MHz. The supported DSI clock rate range for DS90UB941AS-Q1 is 75 MHz-750 MHz.

DS90UB941AS-Q1 supports both continuous and non-continuous clock modes, but care must be taken to select the correct clocking configuration based on the DSI clock type.

Since the supported data formats for DS90UB941AS-Q1 all use a 3-bytes per pixel format, the conversion between DSI clock rate and the video PCLK can be described with a single formula:

$$f_{PCLK} = (f_{DSI} * N_{Lanes})/12 \quad (1)$$

DS90UB941AS-Q1 supports three different clocking configurations to set the FPD-Link PCLK rate for the serializer output.

- DSI Reference Clock Mode
- External Reference Clock Mode
- Internal Reference Clock Mode (typically used for debug purposes only)

DSI Reference Clock Mode is the most straightforward and commonly used configuration for the serializer. In this mode, the serializer will use the incoming video PCLK derived from Equation 1 as the output PCLK to set the output PCLK speed for the serializer. This configuration eliminates the need for any external clock sources at the serializer, aside from the MIPI D-PHY clock from the video source. In this mode, the DSI clock source must meet the stability requirements of the MIPI D-PHY CTS, and the DSI clock must be continuous.

External Reference Clock Mode utilizes an external clock source connected via the REFCLK0 or REFCLK1 pins to source the output PCLK rate from the serializer. In External Reference Clock mode it is recommended that the REFCLK frequency is matched to the DSI PCLK frequency from Equation 1 unless the DSI source utilizes Burst Mode. This will ensure that the incoming video rate is equal to the outgoing video rate. Although it is possible to apply different clock rates between REFCLK and DSI clock in this mode, the implications for such a configuration are outside the scope of this document. In External Reference Clock Mode, the DSI clock may be either continuous or non-continuous.

Internal Reference Clock Mode utilizes an internal oscillator clock inside DS90UB941AS-Q1 to generate the output video PCLK. This mode is typically utilized for debug purposes, as the stability requirements of the internal oscillator clock are not guaranteed over the entire operating range for voltage and temperature of the device. In Internal Reference Clock mode, the DSI clock may be either continuous or non-continuous.

Note that regardless of operating mode, both the minimum/maximum DSI clock rate and the minimum/maximum PCLK rate for the DS90UB941AS-Q1 must be observed at all times. For example, with f_{DSI} = 75 MHz, 2 DSI data lanes, and DSI Reference Clock Mode, the output video PCLK rate would be 12.5 MHz. However DS90UB941AS-Q1 has a minimum PCLK rate of 25 MHz per FPD-Link channel, so this configuration would not be supported. Likewise, with f_{DSI} = 750 MHz, 4 DSI data lanes, and DSI reference clock mode, the output video PCLK rate would be 250 MHz, which is greater than the maximum support dual FPD-Link PCLK of 210MHz.

2.3 Blanking or Low Power Modes (BLLP)

The Blanking or Low Power period (BLLP) period is defined as a time during which video or video synchronization packets are not transmitted. During the BLLP period, the DSI source may enter Idle Mode (LP-11), stay in HS mode (LP-00) and transmit HS blanking packets, or transmit non-video packets to the DSI receiver. Typically the DSI source configuration will allow flexibility in configuring BLLP behavior during the various video blanking intervals.

According to the MIPI DSI v1.3.1 standard section 8.11.1, a DSI source should periodically end HS transmission and drive the data lanes to the LP-11 state at least once per frame to enable PHY synchronization. Correspondingly, DS90UB941AS-Q1 uses this LP to HS transition as a signal to initialize its DSI receiver after power up. (Note this only applies to the data lanes and not the clock). Some common DSI source drivers do not

follow the MIPI DSI standard closely with regards to this requirement and will remain in HS (LP-00) mode during all BLLP periods. This poses a common pitfall for system bring-up, as the DS90UB941AS-Q1 cannot initialize if it does not see any LP to HS transitions on the data lanes. It is important to ensure that the DSI source follows the MIPI DSI standard closely, and enables LP-11 during at least one of the BLLP periods of the video frame.

2.4 DSI Packet Timing

DS90UB941AS-Q1 utilizes received MIPI DSI packet timing in order to reconstruct horizontal and vertical sync timing along with the video data enable signal. This allows the serializer to convert the DSI input into a generic 24 bit + sync signal DPI (Display Parallel Interface) format which can then be converted to a number of other protocols by the partner deserializer device in the system (eg. CSI-2, OpenLDI, RGB). Four types of DSI short packets are used to define the horizontal and vertical sync signal boundaries:

- **HSS (Horizontal Sync Start)** - Establishes the rising edge of the horizontal sync signal
- **HSE (Horizontal Sync End)** - Establishes the falling edge of the horizontal sync signal.

Note

HSE is only utilized in DSI Pulse Mode, not Event Mode or Burst mode

- **VSS (Vertical Sync Start)** - Establishes the rising edge of the vertical sync signal
- **VSE (Vertical Sync End)** - Established the falling edge of the vertical sync signal.

Note

VSE is only utilized in DSI Pulse Mode, not Event Mode or Burst Mode

The Data Enable (DE) signal is automatically generated from each received DSI long packet which corresponds to an active video data line. By default, the data enable signal will be logic high during the active portion of the video line and logic low during the video blanking, but this can also be inverted through register control.

In order to accurately generate video timing for the display, a MIPI DSI transmitter must ensure that DSI packet timing matches the DPI pixel transmission rates and widths of all timing events like sync pulses according to the DSI mode which is used:

2.4.1 Non-Burst Mode With Sync Pulses

- The DSI transmitter must convey accurate DPI-type timing for the HSS, HSE, VSS, and VSE packets, as well as the pixel transmission rate for each active line to match the desired video timing.
- All video timing can be extracted from the DSI packet stream directly including sync widths and porch widths
- The output pixel rate can be defined by the DSI clock rate in continuous clock mode or by the REFCLK source applied to the DS90UB941AS-Q1

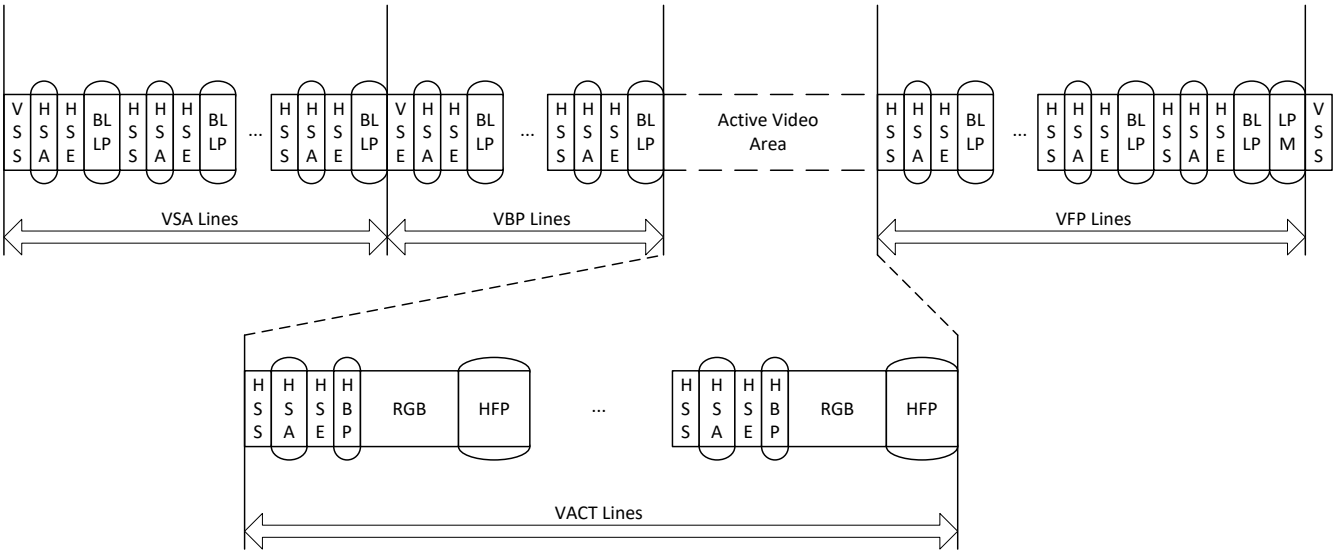

Figure 2-1. Non-Burst Mode with Sync Pulses Packet Structure

2.4.2 Non-Burst Mode With Sync Events

- The DSI transmitter must convey accurate DPI-type timing for HSS, and VSS packets as well as the pixel transmission rate for each active line to match the desired video timing.
- Since Event Mode does not utilize HSE and VSE packets to define the falling edge of the HSYNC/VSYNC signals, the serializer must be programmed to generate the desired sync widths with the DSI_HSW_CFG and DSI_VSW_CFG registers.
- The timing of the rising edge of each sync signal is defined by the received timing of the HSS/VSS DSI short packets (which also defines the horizontal and vertical back porch value for the video).
- The output pixel rate can be defined by the DSI clock rate in continuous clock mode or by the REFCLK source applied to the DS90UB941AS-Q1.

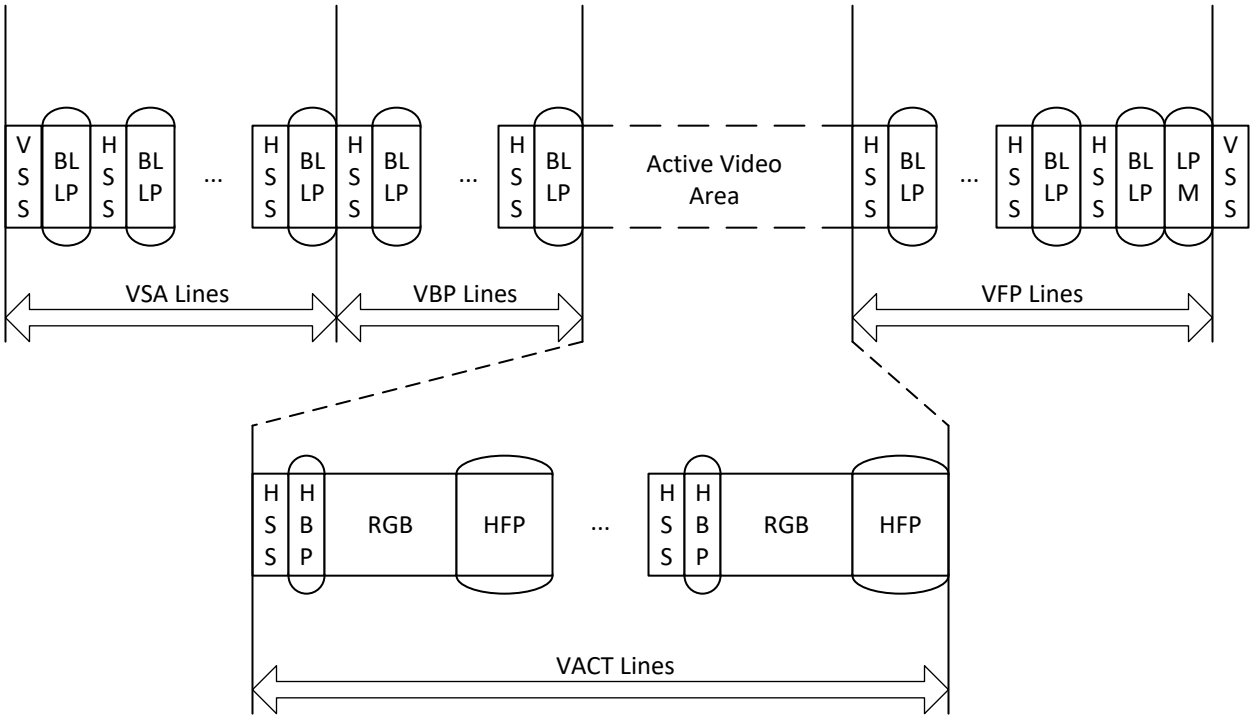

Figure 2-2. Non-Burst Mode with Sync Events Packet Structure

2.4.3 Burst Mode

- The DSI transmitter must convey accurate DPI-type timing for HSS, and VSS packets only.
- Since Burst Mode does not utilize HSE and VSE packets to define the falling edge of the HSYNC/VSYNC signals, the serializer must be programmed to generate the desired sync widths with the DSI_HSW_CFG and DSI_VSW_CFG registers.
- The timing of the rising edge of each sync signal is defined by the received timing of the HSS/VSS DSI short packets (which also defines the horizontal and vertical back porch value for the video).
- The pixel transmission rate can be time compressed for each active video line. This allows sending each line at an arbitrarily high lane speed (within the maximum capability of the DSI receiver).
- The output pixel rate is defined by the REFCLK source applied to the DS90UB941AS-Q1.

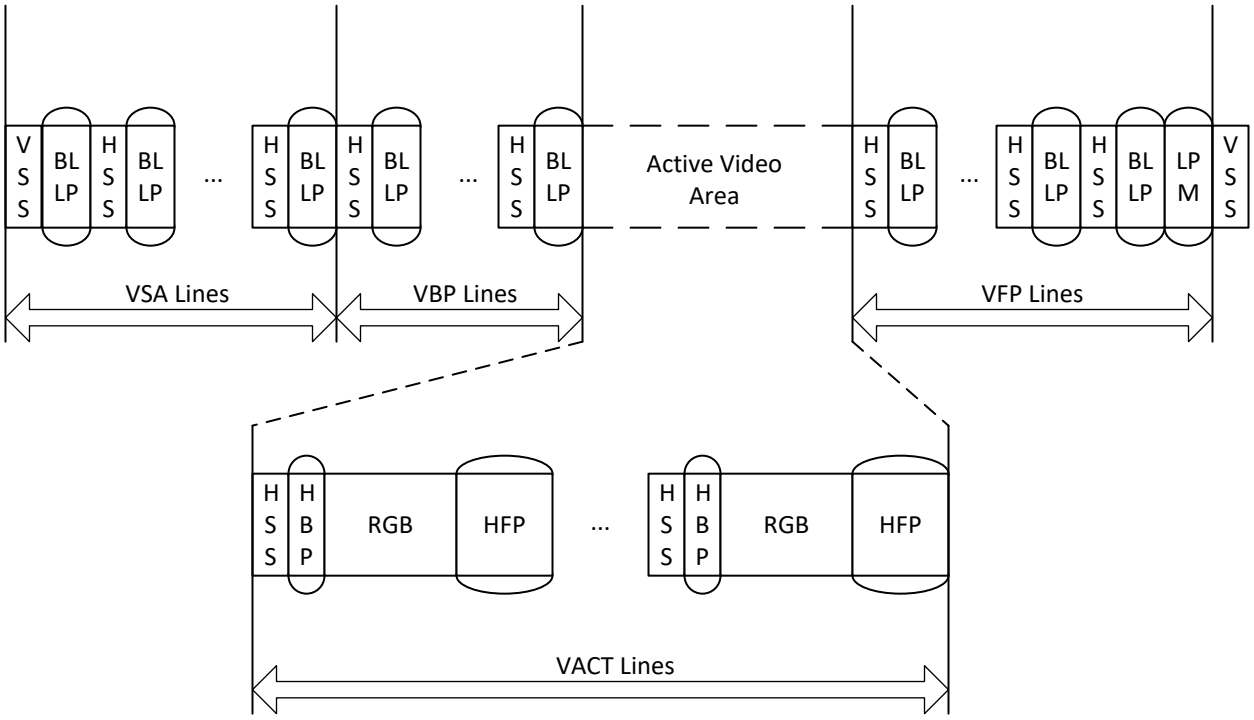

Figure 2-3. Burst Mode Packet Structure

It is important to note that the DSI source driver may need to be adjusted if it cannot meet the requirements of the DSI v1.3.1 standard for a given video configuration. For example, it is possible that a DSI source may send the correct packet structure for the selected DSI mode and video configuration, but does not meet the DPI timing requirements outlined above. In this case, output DPI timing may not meet expectations which can lead to timing errors at the display. It is important to verify the DSI source configuration with a MIPI DSI analyzer prior to applying the source to DS90UB941AS-Q1 in order to ensure that both the packet structure and packet timing are correct.

3 Bring-Up and Debug Flow

The following section describes a common debug flow that can be applied to bring-up for the interface between DS90UB941AS-Q1 and a DSI source. The focus of this debug is on the MIPI DSI interface and assumes that the FPD-Link channel between DS90UB941AS-Q1 and the partner deserializer has been properly established.

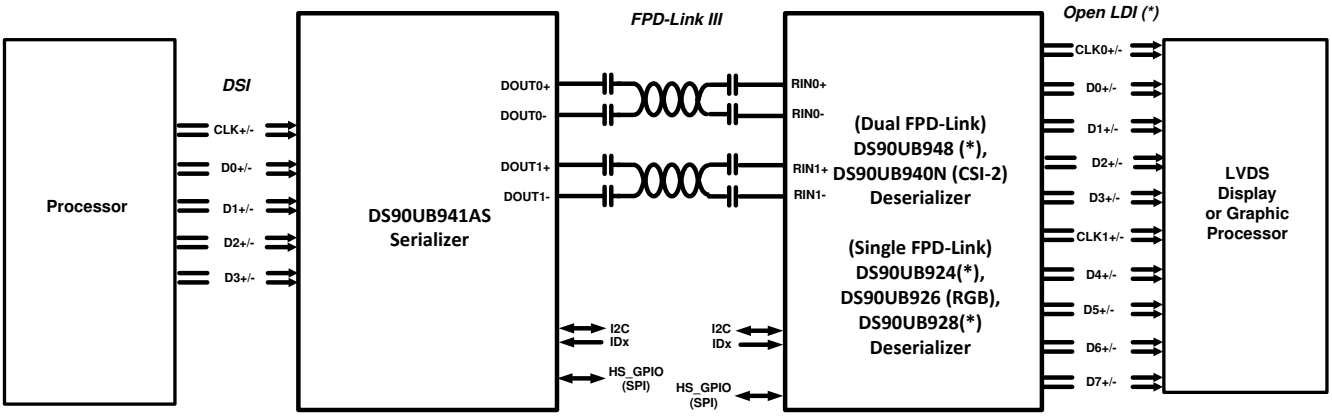

Figure 3-1. Example DS90UB941AS-Q1 System

In this example, the DS90UB941AS-Q1 is configured for DSI reference clock mode. For more information on configuring PATGEN from the DS90UB941AS-Q1, see Exploring the Int Test Pattern Generation Feature of FPDLink III IVI Devices.

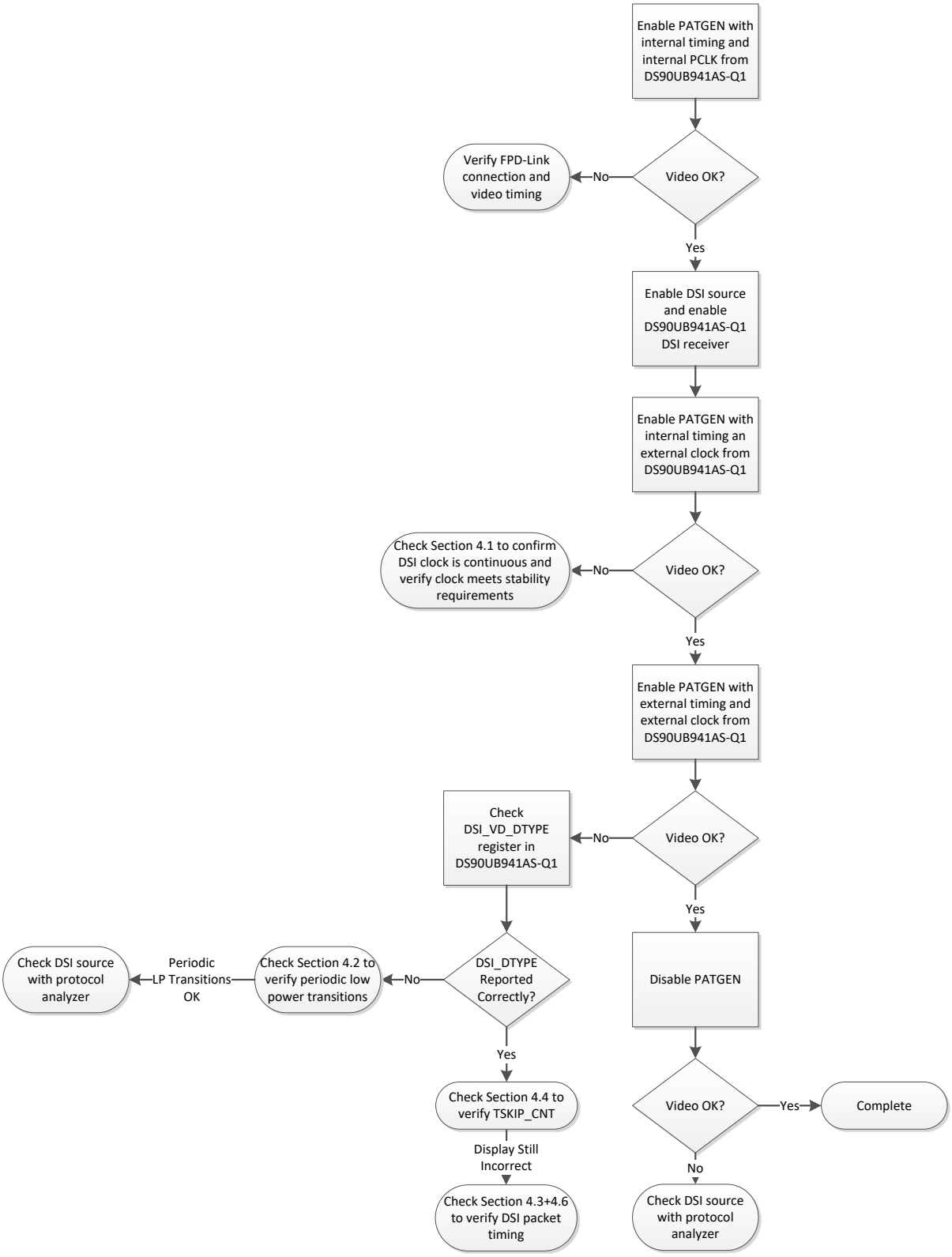

Figure 3-2. Recommended DS90UB941AS-Q1 Bring-Up Flow

4 Example Bringup Scenarios

4.1 Discontinuous Clock

When DS90UB941AS-Q1 is operated in DSI Reference Clock Mode, the DSI clock from the source is used to directly set the FPD-Link forward channel frequency and video PCLK rate. It is important to ensure that the DSI clock is continuous (no LP-11 transitions) at all times. For continuous clock mode, the clock lane remains in high-speed mode with a constant frequency at all times. For non-continuous clock mode, the clock lane may enter the LP-11 low power state between HS data packet transmissions.

Symptoms:

- DSI_VC_DTYPE register reports correct data type for the video and:
  - Periodic flickering screen
  - Periodic loss of LOCK from the deserializer
  - Black screen

How to Verify:

1. Check the DSI_VC_DTYPE register via I2C:
   a. Write 0x40 = 0x04 for DSI Port 0 or 0x40 = 0x08 for DSI Port 1
   b. Write 0x41 = 0x2A
   c. Read 0x42 (DSI_VC_DTYPE)
   d. The DSI_DTYPE is contained in bits 5:0

To verify that the DSI clock is continuous, the system designer can probe the DSI clock lane during video transmission. This can be done with a single ended probe attached between one of the data lane P/N nets and GND. The goal is to set the oscilloscope trigger to capture the LPTX amplitude only, while ignoring the HS data transmission.

During HS mode transmission, the clock is expected to have a common mode voltage between 150 mV-250 mV and a differential swing of 140 mV-270 mV.

During Low Power Mode (LP-11), the P/N clock lanes will no longer be differential. They will both transition to the LPTX high level output voltage of 0.95 V-1.3 V.

Set the oscilloscope trigger level to 800mV and monitor the clock lane activity. If the scope does not trigger from the 800mV level, then the DSI clock is continuous. The clock should show continuous toggling activity with a differential swing of ~140 mV - 27 0 mV and a common mode of ~150 mV-250 mV

Resolution:

The DSI source must be configured to enable DSI continuous clock mode. Consult the kernel driver manual for the DSI source for options to enable this behavior which is sometimes referred to a "High Power Mode". Some examples of flags in the DSI source driver pertaining to this configuration are:

- sDeviceConfig.bEnableClkLaneHighPwrMode
- dsi-video-clock-mode

4.2 Missing Periodic Low Power Transitions

A common cause for failure to receive video during end to end bring-up with DS90UB941AS-Q1 is due to DSI source configuration for BLLP behavior. As described in section 1.3, a DSI source is required by the DSI v1.3.1 specification to periodically enter LP11 (Low Power Mode) on the data lanes (not the clock) at least once per frame. Some common DSI driver examples in the market do not enable LP11 mode by default during any of BLLP periods in the video stream. This will result in the DS90UB941AS-Q1 not initializing the DSI receiver to start forwarding video through the FPD-Link output*.

Symptoms:

- Black screen
- DSI clock is detected and the FPD-Link is running at-speed according to the desired video rate but there is no video data present at the deserializer
- No data type is reported by the DS90UB941AS-Q1 in the DSI_VC_DTYPE register

How to Verify:

Verify the detected DSI pixel frequency by reading the DSI_FREQ register 0x5F via I2C. In this system state, the DSI pixel frequency should match expectations based on the video rate and should not report 0MHz.

1. Check the DSI_VC_DTYPE register via I2C:
   a. Write 0x40 = 0x04 for DSI Port 0 or 0x40 = 0x08 for DSI Port 1
   b. Write 0x41 = 0x2A
   c. Read 0x42 (DSI_VC_DTYPE)
   d. The DSI_DTYPE is contained in bits 5:0

To verify that LP-11 is being entered periodically by the DSI source, the system designer can probe one of the active DSI data lanes during video transmission. This can be done with a single ended probe attached between one of the data lane P/N nets and GND. The goal is to set the oscilloscope trigger to capture the LPTX signal amplitude only, while ignoring the HS data transmission.

During HS mode transmission, each data lane is expected to have a common mode voltage between 150-250mVm and a differential swing of 140-270mV.

During Low Power Mode (LP-11), the P/N data lanes will no longer be differential. They will both transition to the LPTX high level output voltage of 0.95-1.3V.

Set the oscilloscope trigger level to 800mV and monitor the data lane activity. If the DSI source is properly configured to output periodic LP-11 pulses, then the scope should trigger at least once per frame. The period of the frame is defined by the video refresh rate - commonly 16.6ms for 60Hz refresh. If the scope does not trigger from the 800mV level, then the DSI source driver has not been properly configured.

Example:

Figure 4-1. Example DSI Data Lane With No Periodic Low Power States

Resolution:

The DSI source driver must be configured to enter Low Power Mode (LP-11) at least once per frame during one of the available BLLP periods. Consult the kernel driver manual for the DSI source for options to enable periodic Low Power Mode. Some examples of flags in the DSI source driver pertaining to this configuration are:

- mdss-dsi-bllp-eof-power-mode
- mdss-dsi-bllp-power-mode

Note

If the DS90UB941AS-Q1 DSI receiver is enabled prior to enabling the DSI TX source, it may be possible for the DS90UB941AS-Q1 DSI receiver to initialize during the first and only LP to HS transition that occurs when the video output starts. After the DSI receiver is initialized, the video will continue to output as normal unless the DS90UB941AS-Q1 device is reset at any point later. This should not be considered a solution to the source of the issue, as the DSI driver should be adjusted to avoid any loss of video during various power-up/down conditions. Also, there is no way to manually initialize the DSI receiver if it does not see at least one LP to HS transition.

4.3 Incorrect DSI Packet Timing

While most standard DSI interfaces typically ensure MIPI compliance from a D-PHY physical layer perspective (DC/AC Electrical Parameters), problems related to DSI packet order/timing can still occur during the driver development phase, especially when implementing non-standard video timings or clock rates for custom video solutions*. As stated in section 1.4, DS90UB941AS-Q1 utilizes the timing received from incoming DSI packets in order to reconstruct DPI timing for the output video stream. This means the received timing of video packets, especially synchronization packets is critical to ensuring that the system will function correctly.

Symptoms:

- Flickering screen/jittering screen
- Cropped/torn video
- Video roll over top/bottom or left/right
- Black screen

How to Verify:

In order to verify DSI packet timing, the DSI source must be connected to MIPI analyzer test equipment which can decode DSI packets and log bus activity with time stamps. Several different options are available to allows for analysis of DSI protocol activity at the data packet level:

- Dedicated DSI analyzer equipment
  - Typically best for direct connection between DSI source and protocol analyzer without DS90UB941AS-Q1 connected
  - Good for connections to processor dev kits where MIPI DSI signals can be broken out to SMA cables for easy connection to the analyzer
- High speed oscilloscope with DSI analyzer software package
  - Required for in-line analysis of DSI activity in a full system where DSI is connected between the source and DS90UB941AS-Q1
  - Requires high speed probes for the data and clock lanes to be soldered into the board

The first step in the verification process is to determine the expected MIPI packet timing by calculating expected horizontal/vertical timing parameters for the video in terms of seconds. First determine the pixel time based on the video PCLK, and then multiply each horizontal timing parameter by the pixel time to find the expected duration of each horizontal timing event.

Example

- Horizontal Active (HACT) = 1920 pixels
- Horizontal Front Porch (HFP) = 92 pixels
- Horizontal Sync (HSYNC) = 14 pixels
- Horizontal Back Porch (HBP) = 62 pixels
- Pixel clock (PCLK) = 148 MHz

Pixel time = 1/PCLK = 6.76 ns (2)

HACT = 6.76 ns*1920 = 12.9 µs (3)

HFP = 6.76 ns*92 = 621.9 ns (4)

HSYNC = 6.76 ns*14= 94.6 ns (5)

HBP = 6.76 ns*62 = 419.1 ns (6)

Next, the DSI video source should be captured for analysis:

1. Activate the DSI source and power the DS90UB941AS-Q1 device (if connected)
2. Activate the DS90UB941AS-Q1 DSI receiver to allow for dynamic DPHY termination (if connected)
3. Capture DSI protocol activity for all lanes utilized over a period of at least 2 video frames

The DSI analyzer may report horizontal timing parameters in terms of bytes, which is related to the video packet structure (number of bytes per pixel which is typically 3 for 24-bit RGB). Although this data provides useful info about the source configuration, the most important factor to analyze is the time (in seconds) between the different synchronization packets which define the video DPI timing during the active video frame. By checking the time stamps for each video event (decoded from the DSI packet data), the horizontal timing for HACT, HFP, HSYNC, and HBP can be measured and compared against the expected values.

Time Stamp	Time (s)	Packet Data Type	Detailed Decode
t0	0	0x21	"H Sync Start VC0 "
t1	1E-08	0x19	"Blanking Packet Payload Size: 38 bytes VC0 "
t2	1.1E-07	0x31	"H Sync End VC0 "
t3	1.18E-07	0x19	"Blanking Packet Payload Size: 182 bytes VC0 "
t4	5.4E-07	0x3e	"24 Bit RGB 8-8-8 Payload Size: 5760 bytes VC0 "
t5	1.3488E-05	0x19	"Blanking Packet Payload Size: 276 bytes VC0 "
t6	1.4415E-05	0x21	"H Sync Start VC0 "
t7	1.4423E-05	0x19	"Blanking Packet Payload Size: 38 bytes VC0 "
t8	1.4522E-05	0x31	"H Sync End VC0 "
t9	1.4532E-05	0x19	"Blanking Packet Payload Size: 182 bytes VC0 "
t10	1.4955E-05	0x3e	"24 Bit RGB 8-8-8 Payload Size: 5760 bytes VC0 "
t11	2.7898E-05	0x19	"Blanking Packet Payload Size: 276 bytes VC0 "
t12	2.883E-05	0x21	"H Sync Start VC0 "

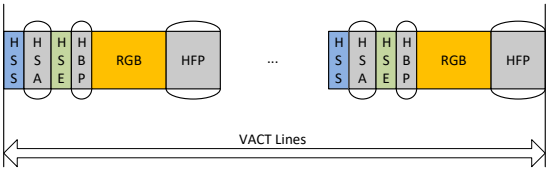

Figure 4-2. Example DSI Trace Decode - Horizontal Line (RGB888)

Finally, calculate the measured timing parameters based on the decoder time stamps:

$$HACT = t_5 - t_4 = 12.9\ \mu s \quad (7)$$

$$HFP = t_6 - t_5 = 627\ ns \quad (8)$$

$$HSYNC = t_2 - t_1 = 100\ ns \quad (9)$$

$$HBP = t_4 - t_3 = 422\ ns \quad (10)$$

In this example, the calculated timing matches the measured timing to within 1 pixel's time for HACT, HBP, and HSYNC parameters, however the HFP measured value is significantly higher than expected (621.9ns vs 927ns). This difference equates to around 45 extra pixels in the horizontal front porch for the video which may result in visual errors at the display if the display timing controller cannot tolerate the incorrect input.

Note that HSS/HSE packets are 4 bytes long, so to accurately account for the packet length, bytes are removed from the proceeding blanking packet byte count between sync events. For example in this video source, the horizontal sync signal is 14 pixels long which should correspond to 42 bytes with a 3 byte-per-pixel packing structure. In the DSI decode, the blanking packet payload between HSS and HSE packets is only 38 bytes because 4 bytes were already sent during the HSS packet transmission.

While video timing errors are more likely to occur in the horizontal timing configuration, it is important to verify the vertical video timing as well by checking the number of received lines in the packet decode during vertical active and blanking portions of the DSI stream. The same method can be applied to count the number of vertical lines and to verify that the line time remains consistent during vertical blanking.

Example analysis of vertical sync period:

- Vertical Sync (VSYNC) = 2 lines

To calculate the expected line time, sum the total number of pixels per horizontal line, and multiply by the pixel time from Equation 2.

$$Line\ Time = (HACT + HFP + HBP + HSYNC) * Pixel\ Time \quad (11)$$

$$Expected\ line\ time = (1920+92+62+14) * 6.76\ ns = 14.1\ \mu s \quad (12)$$

Time Stamp	Time	Packet Data Type	Detailed Decode
t0	0	0x1	"V Sync Start VC0 "
t1	8E-09	0x19	"Blanking Packet Payload Size: 38 bytes VC0 "
t2	1.08E-07	0x31	"H Sync End VC0 "
t3	1.16E-07	0x19	"Blanking Packet Payload Size: 6218 bytes VC0 "
t4	1.4085E-05	0x21	"H Sync Start VC0 "
t5	1.4093E-05	0x19	"Blanking Packet Payload Size: 38 bytes VC0 "
t6	1.4196E-05	0x31	"H Sync End VC0 "
t7	1.4203E-05	0x19	"Blanking Packet Payload Size: 6218 bytes VC0 "
t8	2.8173E-05	0x11	"V Sync End VC0 "

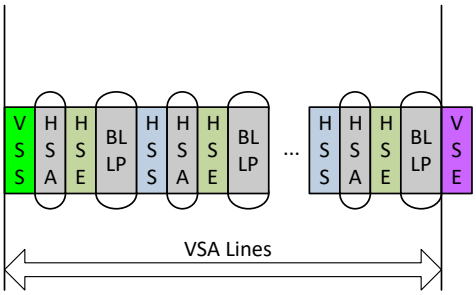

Figure 4-3. Example DSI Trace Decode - Vertical Sync (RGB888)

The line time can be measured from VSS to HSS, HSE to HSE, or HSS to VSE during the vertical sync period.

$$\text{Line time} = t_4\text{-}t_0 = 14.1\ \mu s \quad (13)$$

Note that two complete lines are logged between VSS and VSE which matches expectations for the video timing. (t_0 ->t_4 and t_4->t_8). This analysis technique can also be used to verify DSI packet timing in the vertical front and back porch regions of the video.

Note

One potential reason for the DSI packet timing deviating from expectations could be related to the driver implementation for positioning periodic LP-11 low power pulses within the various BLLP portions of the video frame. While the DSI standard requires the source to provide periodic LP-11 transitions at least once per frame, it allows for flexibility in which BLLP region that the pulse is inserted, based on the video timing and clock rate.

VSS	BLLP-1	HSE	BLLP-2		
HSS	BLLP-1	HSE	BLLP-2		
VSE	BLLP-1	HSE	BLLP-2		
HSS	BLLP-1	HSE	BLLP-2		
HSS	BLLP-1	HSE	BLLP-3	DATA	BLLP-4
HSS	BLLP-1	HSE	BLLP-3	DATA	BLLP-4
HSS	BLLP-1	HSE	BLLP-3	DATA	BLLP-4
HSS	BLLP-1	HSE	BLLP-3	DATA	BLLP-4
HSS	BLLP-1	HSE	BLLP-3	DATA	BLLP-4
HSS	BLLP-1	HSE	BLLP-3	DATA	BLLP-4
HSS	BLLP-1	HSE	BLLP-3	DATA	BLLP-4
HSS	BLLP-1	HSE	BLLP-2		
HSS	BLLP-1	HSE	BLLP-2		

Figure 4-4. Example DSI Frame Format With BLLP Regions

The minimum time duration of an LP-11 pulse is bounded by the MIPI D-PHY 1.2 specification, which defines minimum/maximum AC specifications for Global Operation Timing Parameters (t_{LPX}, $t_{HS\text{-}PREP}$, $t_{TD\text{-}TERM\text{-}EN}$, $t_{HS\text{-}ZERO}$, and so forth). These parameters define time intervals for how long the transition process takes to

move from LP to HS mode or vice-versa. Depending on the DSI lane speed and video timing parameters, it may be possible for the duration of a LP-11 pulse from the transmitter to exceed the time between sync events for the video. For example, with a short pixel time and small horizontal front porch time, the DSI source may not have enough time to transition between HS->LP->HS between ending the video line long packet and sending the HSS packet. In the case where the LP-11 pulse is applies anyways, the resultant HFP timing value may be stretched to a larger value than expected.

Example:

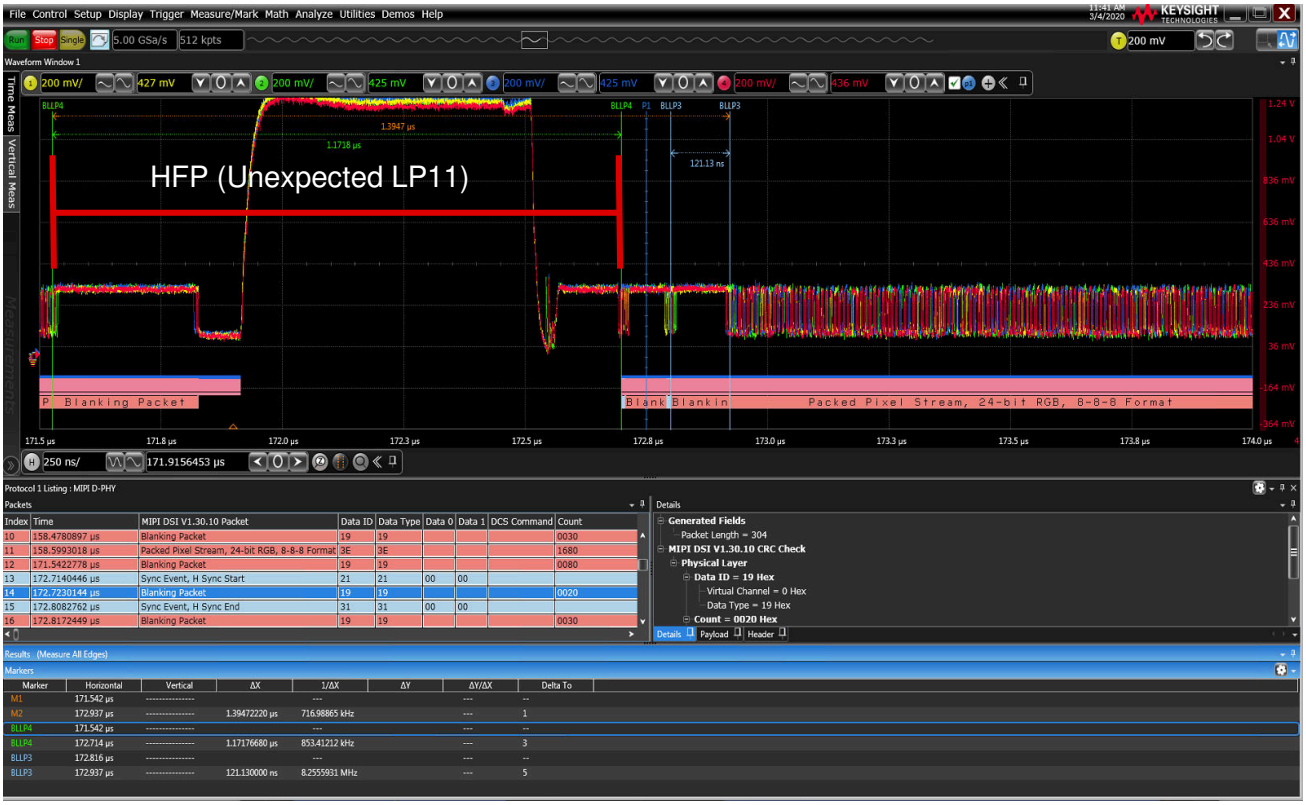

Figure 4-5. Unexpected LP Transition During HFP (BLLP-4)

To avoid this issue, the driver should be modified to ensure that the DSI source stays in HS mode (it can send HS blanking packets to fill time), during the HFP time. The LP-11 pulse can be moved to a BLLP location in the video frame which has enough time duration to allow the pulse without disrupting the expected DPI timing (for example in the vertical blanking area, BLLP-2).

4.4 $T_{HS-SKIP}$ Configuration

The MIPI D-PHY v1.2 receiver specification requires the sink device to ignore activity on the DSI data lanes at the end of high speed packet transmission prior to re-entering the low power state (LP-11) in order to mask transition effects during the End of Transmission (EoT) sequence. If the $T_{HS-SKIP}$ timing parameter is mis-configured, it may result in data errors in the DSI video stream.

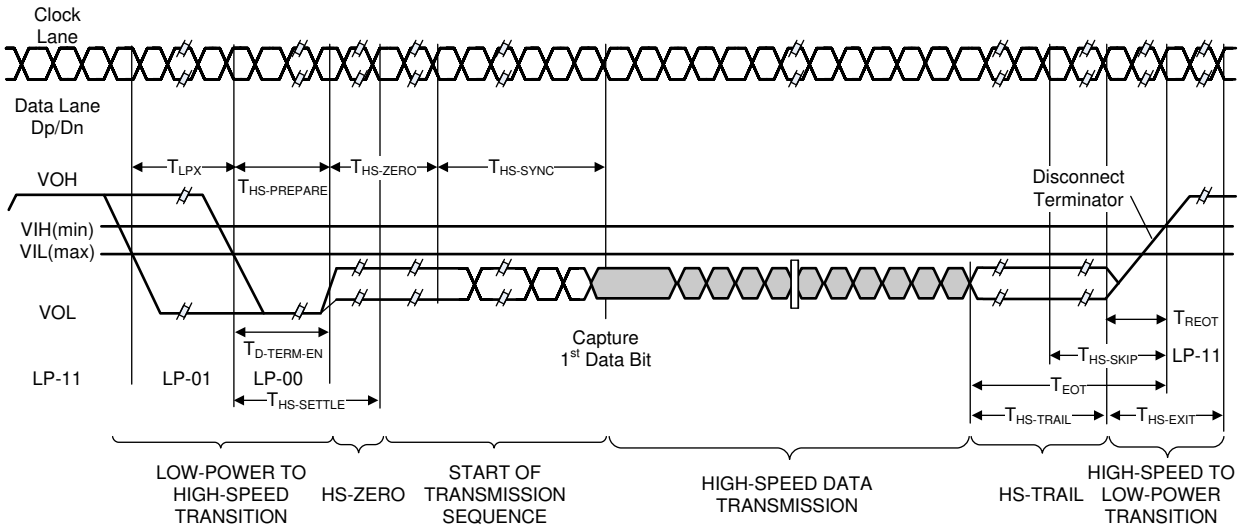

Figure 4-6. High-Speed Data Transmission in Bursts

Symptoms:

- Random/intermittent pixel errors
- DSI error flags in the DS90UB941AS-Q1 registers
- Jittering or flickering display

Resolution:

DS90UB941AS-Q1 requires user configuration of the $t_{HS-SKIP}$ timing parameter based on the DSI clock speed applied. The T_{SKIP_CNT} (dec) value is defined in Equation 14, where f_{DSI} is the DSI clock frequency in GHz.

$$TSKIP\_CNT = Round(65*f_{DSI}-5) \quad (14)$$

This value must get loaded into DS90UB941AS-Q1 register 0x05[6:1] (in hex) prior to enabling the DSI receiver.

Note

The TSKIP_CNT register field is bit shifted left by one bit in the register field.

To program TSKIP_CNT, use the following programming steps via I2C:

1. Write 0x40 = 0x04 for DSI Port 0 or 0x40 = 0x08 for DSI Port 1
2. Write 0x41 = 0x05.
3. Write 0x42 = hex(TSKIP_CNT<<1) from Equation 14.

The DS90Ux941AS-Q1 Superframe Design Calculator tool is available in the DS90UB941AS-Q1 product folder, which also includes calculations for TSKIP_CNT.

4.5 End of Transmission Packets (EoTp)

DSI devices compliant to the MIPI DSI v1.0 specification and later are required to generate End of Transmission Packets (EoTp) following any HS data transmission. The main objective of the EoTp is to enhance the robustness of the DSI interface during transition from HS to LP mode so that the receiver can clearly detect the end of HS transmission even in the presence of non-optimal signaling conditions. To support backwards compatibility and interop between DSI peripherals, the standard mandates that the transmitter and receiver devices should have optional capability to utilize or not utilize EoTp functionality. DS90UB941AS-Q1 expects the DSI source to send EoTp by default since it is a DSI v1.3.1 compliant receiver, so if the source does not generate EoTp, then DS90UB941AS-Q1 will report an error condition.

Symptoms:

- DS90UB941AS-Q1 reports DSI_EOT_ERR in the DSI_STATUS register

How to Verify:

1. Check the DSI_EOT_ERR flag via I2C:
   a. Write 0x40 = 0x04 for DSI Port 0 or 0x40 = 0x08 for DSI Port 1
   b. Write 0x41 = 28
   c. Read 0x42 and check for bit 2, which indicates DSI_EOT_ERR when bit 2 = 1. This flag is cleared on read.

Resolution:

It is recommended to enable EoTp generation from the source device if possible. This should be a configurable option in the DSI source kernel driver. If the source does not support EoTp generation, then enable DSI_NO_EOTPKT = 1 in the DSI_CONFIG_1 register which will mask EoTp errors in the DSI_STATUS register.

Typically, this error condition does not cause any visual impact to the display, but it may affect the DS90UB941AS-Q1's capability to detect a true EoT error in a system which does not utilize EoTp.

4.6 Configuration of Sync Width for Event Mode/Burst Mode

As described in Section 2.4.2, DSI Non-Burst Mode with Sync Events, and Burst Mode configurations do not utilize horizontal or vertical sync end packets to convey DPI timing to the sink. When these modes are used with DS90UB941AS-Q1, it is required to configure the horizontal and vertical sync widths for the video through the device registers. Without configuring desired sync widths and enabling Event Mode, the display output timing may not meet expectations.

Symptoms:

- Black screen
- Jittering/flickering screen
- Horizontal or vertical rollover

Resolution:

If the DSI source is configured for Event Mode or Burst Mode, first set DSI_SYNC_PULSES = 0 in the DSI_CONFIG_0 register. This will inform the DS90UB941AS-Q1 receiver that it should expect only horizontal/vertical sync start packets, and enable override controls for HSYNC and VSYNC signal generation.

Next, set the DSI_HSW_CFG_HI/DSI_HSW_CFG_LO and DSI_VSW_CFG_HI/DSI_VSW_CFG_LO registers to the desired parameters for the video signal. The horizontal/vertical front porch widths will be defined by the number or pixels/lines following the active data to the start of the HSS or VSS signals.

Example Source Signal:

- HACT = 1920
- HFP = 92
- HTOTAL = 2088
- VACT = 1080
- VFP = 35
- VTOTAL = 1150

Desired Sync Widths:

- HSYNC = 14 pixels = 0x0E
- VSYNC = 2 lines = 0x02

Set the DS90UB941AS-Q1 indirect DSI registers:

1. DSI_HSYNC_WIDTH_HI = 0x00
2. DSI_HSYNC_WIDTH_LO = 0x0E
3. DSI_VSYNC_WIDTH_HI = 0x00
4. DSI_VSYNC_WIDTH_LO = 0x02

First, select the DSI indirect registers corresponding to the desired DSI port:

1. Write 0x40 = 0x04 for DSI Port 0 or 0x40 = 0x08 for DSI Port 1.
2. Write 0x41 = 0x30 (DSI_HSW_CFG_HI).
3. Write 0x42 = 0x00.
4. Write 0x41 = 0x31 (DSI_HSW_CFG_LO).
5. Write 0x42 = 0x0E.
6. Write 0x41 = 0x32 (DSI_VSW_CFG_HI).
7. Write 0x42 = 0x00.
8. Write 0x41 = 0x33 (DSI_VSW_CFG_LO).
9. Write 0x42 = 0x02.

The HBP and VBP signals will be automatically generated based on the number of total pixels/lines, the HFP/VFP widths, and the sync signal override widths:

$$HBP = HTOTAL - HACT - HFP - HSYNC = 2088 - 1920 - 92 - 14 = 62 \text{ pixels} \quad (15)$$

$$VBP = VTOTAL - VACT - VFP - VSYNC = 33 \text{ lines} \quad (16)$$

5 Summary

This application report provides a systematic approach to DSI bringup with DS90UB941AS-Q1 and walks through some of the most common pitfalls in DSI video applications.

6 References

- Texas Instruments *DS90UB941AS-Q1 2K DSI to FPD-Link III Bridge Serializer with Video Splitting*
- Texas Instruments *DS90UH941AS-Q1 2K DSI to FPD-Link III Bridge Serializer with Video Splitting and HDCP*
- MIPI Alliance Specification for D-PHY v1.2
- MIPI Alliance Specification for DSI v1.3.1

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