

Improving the Performance of Arc Fault Detection with High-Speed Comparators

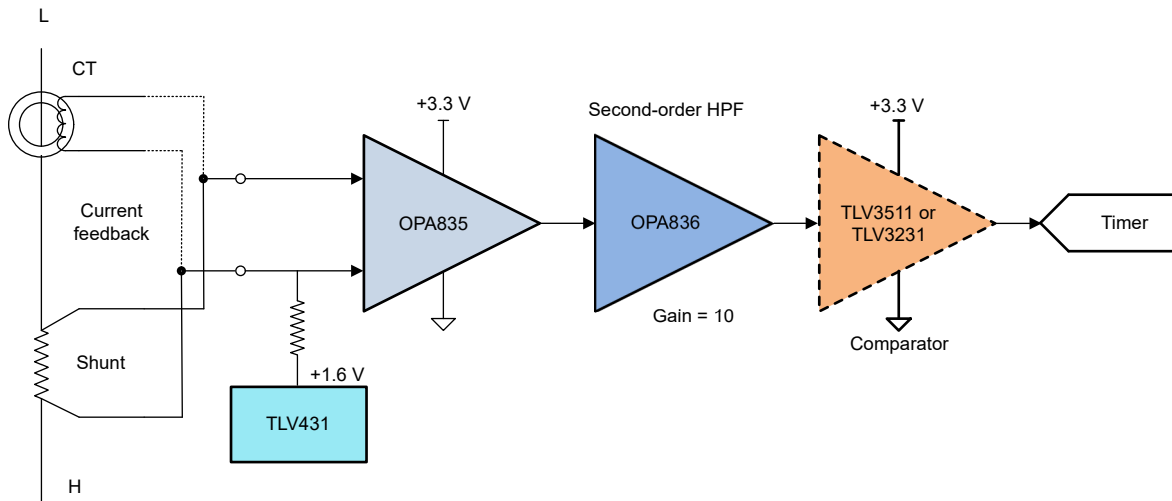


Figure 1. Concept Diagram for Arc Fault Detection Systems

Arc fault detection requires translation of analog fault signature, high-frequency noise into time domain as a series of pulse trains. Additional post-processing is used to verify the fault condition.

Design Challenges

- Wide-frequency spectrum, up to 10MHz
- Symmetrical timing on low-to-high and high-to-low signal edges
- Low input offset to maintain minimal timing error from amplifier output to comparator input
- Minimal power consumption

How High-Speed Comparators Benefit the Systems

- A comparator's fast response time enables the capturing of waveforms with spectrum up to 10MHz and beyond without loss of signal integrity.
- Symmetrical prop delay and rise-fall times of a push-pull output stage enables the arc fault signal to be digitized without distortion and with minimal timing error.
- Low power consumption is necessary due to the *always-on* nature of arc fault detectors and minimizes power drain on building power systems.
- Low input offset voltage maintains the integrity of an arc fault signature by triggering the comparator output at the precise threshold voltage, rendering an accurate digital waveform for post-processing.

Part Number	Propagation Delay	Toggle Frequency	Quiescent Current	Input Offset Voltage	Channel Count
TLV351x	6ns	180MHz	1.1mA	5mV	1/2
TLV323x	15ns	55MHz	200µA	4mV	1/2
LMV7219	7ns	N/A	600ps	6mV	1

If you have more questions please ask them on TI's [E2E forum](#).

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