Preliminary

TMS320C6452 Telecom Serial Interface Port (TSIP)

User's Guide

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Read This First

About This Manual

This document describes the operation of the Telecom Serial Interface Port (TSIP) in the TMS320C6452.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Note: Acronyms 3PSW, CPSW, CPSW_3G, and 3pGSw are interchangeable and all refer to the 3 port gigabit switch.

Related Documents From Texas Instruments

The following documents describe the TMS320C6452 Digital Signal Processor (DSP). Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

Data Manual—

SPRS371 —***TMS320C6452 Digital Signal Processor Data Manual*** describes the signals, specifications and electrical characteristics of the device.

CPU—

SPRU732 — ***TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide*** describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C64x and TMS320C64x+ digital signal processors (DSPs) of the TMS320C6000 DSP family. The C64x/C64x+ DSP generation comprises fixed-point devices in the C6000 DSP platform. The C64x+ DSP is an enhancement of the C64x DSP with added functionality and an expanded instruction set.

Reference Guides—

SPRUF85 —***C6452 DSP DDR2 Memory Controller User's Guide*** describes the DDR2 memory controller in the TMS320C6452 Digital Signal Processor (DSP). The DDR2/mDDR memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM devices and standard Mobile DDR SDRAM devices.

SPRUF86 —***C6452 Peripheral Component Interconnect (PCI) User's Guide*** describes the peripheral component interconnect (PCI) port in the TMS320C6452 Digital Signal Processor (DSP). The PCI port supports connection of the C642x DSP to a PCI host via the integrated PCI master/slave bus interface. The PCI port interfaces to the DSP via the enhanced DMA (EDMA) controller. This architecture allows for both PCI master and slave transactions, while keeping the EDMA channel resources available for other applications.

SPRUF87 — ***C6452 DSP Host Port Interface (UHPI) User's Guide*** describes the host port interface (HPI) in the TMS320C6452 Digital Signal Processor (DSP). The HPI is a parallel port through which a host processor can directly access the CPU memory space. The host device functions as a master to the interface, which increases ease of access. The host and CPU can exchange information via internal or external memory. The host also has direct access to memory-mapped peripherals. Connectivity to the CPU memory space is provided through the enhanced direct memory access (EDMA) controller.

SPRUF89 — ***C6452 DSP VLYNQ Port User's Guide*** describes the VLYNQ port in the TMS320C6452 Digital Signal Processor (DSP). The VLYNQ port is a high-speed point-to-point serial interface for connecting to host processors and other VLYNQ compatible devices. It is a full-duplex serial bus where transmit and receive operations occur separately and simultaneously without interference.

SPRUF90 — ***C6452 DSP 64-Bit Timer User's Guide*** describes the operation of the 64-bit timer in the C6452 Digital Signal Processor (DSP). The timer can be configured as a general-purpose 64-bit timer, dual general-purpose 32-bit timers, or a watchdog timer.

SPRUF91 — ***C6452 DSP Multichannel Audio Serial Port (McASP) User's Guide*** describes the multichannel audio serial port (McASP) in the C6452 Digital Signal Processor (DSP). The McASP functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I2S) protocols, and intercomponent digital audio interface transmission (DIT).

SPRUF92 — ***C6452 DSP Serial Port Interface (SPI) User's Guide*** discusses the Serial Port Interface (SPI) in the C6452 Digital Signal Processor (DSP). This reference guide provides the specifications for a 16-bit configurable, synchronous serial peripheral interface. The SPI is a programmable-length shift register, used for high speed communication between external peripherals or other DSPs.

SPRUF93 — ***C6452 DSP Universal Asynchronous Receiver/Transmitter (UART) User's Guide*** describes the universal asynchronous receiver/transmitter (UART) peripheral in the C6452 Digital Signal Processor (DSP). The UART peripheral performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data received from the CPU.

SPRUF94 — ***C6452 DSP Inter-Integrated Circuit (I2C) Module User's Guide*** describes the inter-integrated circuit (I2C) peripheral in the C6452 Digital Signal Processor (DSP). The I2C peripheral provides an interface between the DSP and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus. External components attached to this 2-wire serial bus can transmit and receive up to 8-bit wide data to and from the DSP through the I2C peripheral. This document assumes the reader is familiar with the I2C-bus specification.

SPRUF95 — ***C6452 DSP General-Purpose Input/Output (GPIO) User's Guide*** describes the general-purpose input/output (GPIO) peripheral in the C6452 Digital Signal Processor (DSP). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an input, you can detect the state of the input by reading the state of an internal register. When configured as an output, you can write to an internal register to control the state driven on the output pin.

SPRUF96 — ***C6452 DSP Telecom Serial Interface Port (TSIP) User's Guide*** is a multi-link serial interface consisting of a maximum of two transmit data signals (or links), two receive data signals (or links), two frame sync input signals, and two serial clock inputs. Internally the TSIP offers single channel of timeslot data management and single DMA capability that allow individual timeslots to be selectively processed.

SPRUF97 — ***TMS320C6452 DSP 3 Port Switch (3PSW) Ethernet Subsystem User's Guide*** describes the operation of the 3 port switch (3PSW) ethernet subsystem in the TMS320C6452 Digital Signal Processor (DSP). The 3 port switch gigabit ethernet subsystem provides ethernet packet communication and can be configured as an ethernet switch. It provides the serial gigabit media independent interface (SGMII), the management data input output (MDIO) for physical layer device (PHY) management.

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TMS320C6452 TSIP

1 Introduction/Feature Overview

This document describes the operation of the Telecom Serial Interface Port (TSIP).

1.1 Overview/Purpose of the Peripheral

The TSIP is a multi-link serial interface consisting of a maximum of two transmit data signals (or links), two receive data signals (or links), two frame sync input signals, and two serial clock inputs. Internally, the TSIP offers single channel of timeslot data management and single direct memory access (DMA) capability that allow individual timeslots to be processed selectively.

The module can be configured to use the frame sync signals and the serial clocks as redundant sources for all transmit and receive data signals, or one frame sync and serial clock for transmit and the second frame sync and clock for receive. The standard serial data rate for each TSIP transmit and receive data signal is 8.192 Mbps. The standard frame sync is a one or more bit-wide pulse that occurs once every 125 µs or a minimum of one serial clock period every 1024 serial clocks.

At the standard rate and default configuration there are two transmit and two receive links that are active. Each serial interface link supports up to 128 8-bit timeslots. This corresponds to an H-MVIP or H.110 serial data rate interface. The serial interface clock frequency can be either 16.384 MHz (default) or 8.192 MHz. The data rate for the serial interface links can also be set to 16.384 Mbps. The maximum number of active serial links is reduced to two in this configuration. The serial interface clock frequency can be either 32.768 MHz or 16.384 MHz for 16.384 Mbps serial links. Maximum occupation of the serial interface links for the entire TSIP is 1024 transmit and receive timeslots in all configurations.

1.2 Features

The TSIP is a serial interface peripheral that connects directly to TEMUX devices with timeslot data management and an integrated DMA capability. The peripheral provides a glueless interface to common telecom serial data streams and efficient internal routing of the data to designated memories in a multi-CPU device. The TSIP provides these functions:

- Direct interface to H-MVIP devices such as TEMUX, ST BUS devices, TSI devices and H.110 compatible devices
- Dual Transmit and Receive Telecom Serial Interface Ports (TSIP)
  - Each TSIP module supports a transmit/receive data rate of 16.384Mbps
    - One transmit/receive data lane per module at 16.384Mbps each
    - Two transmit/receive data lane per module at 8.192Mbps each
  - Each TSIP supports 256 TDM timeslots for voice data or signaling data
- Flexible Clock and Frame Sync Inputs
  - Configurable for independent TX and RX clock and frame Sync
  - Configurable for common TX and RX clock and Frame Sync
    - Second clock and Frame Sync can be used as a redundant source
  - Independent clock polarity selection for data and frame Sync
  - Selection of 2X or 1X data clock frequency
- Timeslot Data Management and Multi-Channel DMA Capability

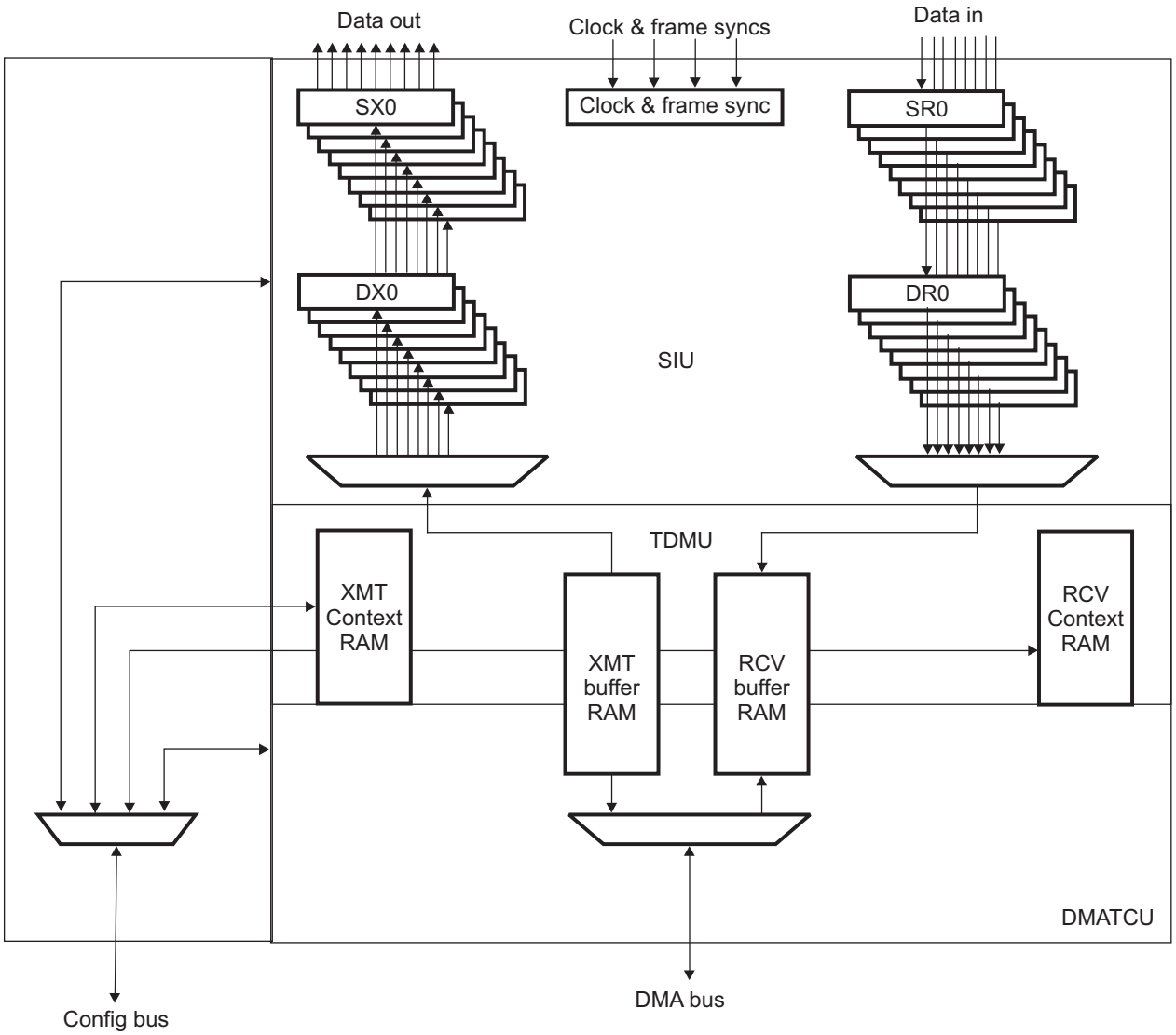
  - Independent timeslot enable/disable per DMA channel
  - Selectively unpacks and packs timelot data for transmit and receive based on a channel timeslot definition
  - A-law and μ-law support on a per timeslot basis
- Frame and SuperFrame Interrupts
- 12 pin External Interface(6 pins/TSIP x 2 ports)

1.3 Functional Block Diagram

The TSIP consists of three functional sub-modules as shown in Figure 1:

- *Serial Interface Unit (SIU)* - The SIU provides parallel to serial and serial to parallel conversion for transmit and receive, respectively.
- *Timeslot Data Management Unit (TDMU)* - The TDMU selectively packs and unpacks timeslot data for receive and transmit based on a channel timeslot definition. There is one transmit and one receive TDMU channel. Each channel is capable of selecting and transferring all of the possible 1024 timeslots in the respective direction.
- *DMA Transfer Control Unit (DMATCU)* - The DMATCU initiates the data transfers between the channel buffers used by the TDMU and the memory buffers used by the CPU.

Figure 1. TSIP Block Diagram



1.4 Terminology Used

The following are brief explanations of some terms used in this document:

Term	Meaning
DMA	Direct Memory Access
DMATCU	DMA Transfer Control Unit
SIU	Serial Interface Unit
TDM	Timeslot Data Management
TDMU	Timeslot Data Management Unit
TEMUX	T1-E1 Mux Device
TSIP	Telecom Serial Interface Port

1.5 Memory Map

Table 1 lists the summary memory map for the registers for the TSIP.

Table 1. TSIP Memory Map

Offset Address	Register Description
0x00000000 -- 0x0000007C	TSIP Module Registers
0x00000080 -- 0x000000FC	Serial Interface Registers
0x00000100 -- 0x0000017C	TDMU Registers
0x00000180 -- 0x000001FC	DMATCU Registers
0x00000200 -- 0x000003FC	TDMU channel Error Log Registers
0x00000400 -- 0x000007FC	Reserved
0x00000800 -- 0x00000FFC	TDMU channel Registers
0x00001000 -- 0x00001FFC	DMATCU channel Registers
0x00002000 -- 0x00007FFC	Reserved
0x00008000 -- 0x0000FFFC	TDMU channel Bitmaps
0x00010000 -- 0x0001FFFC	TDMU channel Buffers
0x00020000 -- 0x0003FFFC	Reserved

2 Features/Common Architecture

This section describes the major features of the TSIP and how it works.

2.1 Interface

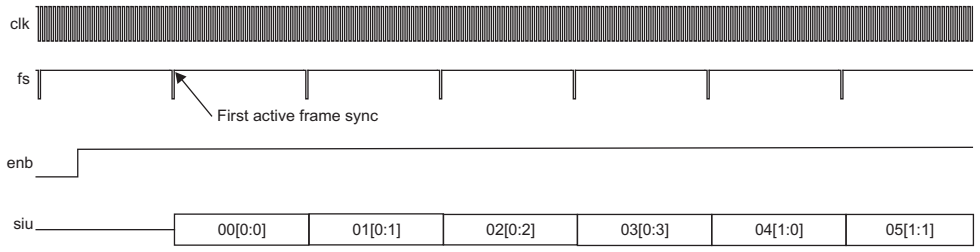
The external pin interface of TSIP consists of eight pins: two clock input pins, two frame sync input pins, two data input pins, and two data output pins. The pins are listed in Table 2. The module has eight additional control signals to control the output state of the eight data output pins.

Table 2. Interface Pins

Pin	Direction	Description
CLK_A	Input	TSIP serial data clock A
CLK_B	Input	TSIP serial data clock B
FS_A	Input	TSIP frame sync A
FS_B	Input	TSIP frame sync B
TR[1:0]	Input	TSIP serial data receive. Up to two serial data streams may be received simultaneously. The serial data clock and frame sync is common for all two.
TX[1:0]	Output	TSIP serial data transmit. Up to two serial data streams may be transmitted simultaneously. The serial data clock and frame sync is common for all two.

On the first frame sync, after the TSIP is enabled, the TSIP starts receiving/transmitting on the TR/TX data lane as denoted by the SIU data lanes in Figure 2.

Figure 2. First Active Frame Sync



2.2 Receive Operation

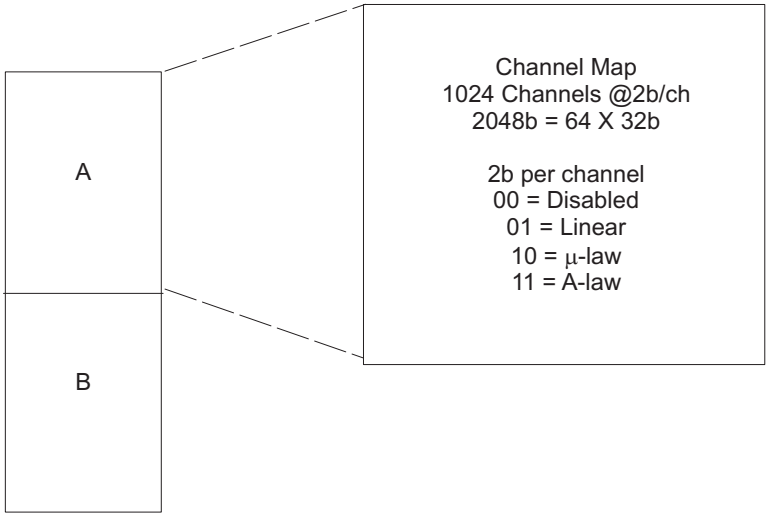
Data that is received by the TSIP is assembled in a serial-to-parallel register (DRn) with the most significant bit first, one 8-bit register per serial interface input. The data for timeslot 0 is recognized on the first eight serial data clocks following the recognition of the frame sync signal that signals the start of the frame and the programmed delay. The data for timeslot 1 is recognized on the next eight serial data clocks immediately following timeslot 0. Data for successive timeslots is continuously received and recognized on subsequent serial data clocks. The number of data samples processed and buffered depends on the timeslot enable/disable definition in the channel bitmap for each of the receive channels.

2.3 Bitmap Context

The receive operation of the TSIP reads and processes the data in the DRn registers and stores the results in the channel buffer based on the channel bitmap context. The registers are read sequentially with the sequence order defined in the SIU by the selected data rate option. Data received on each of the receive serial links can be stored in none, some, or all of the channel buffers. On reaching a watermark in the channel buffer, its DMA engine transfers the data from the channel buffers to the memory buffers outside the system. Each transmit/receive channel has dual buffers, PING and PONG, that are shared with the DMATCU. Each of the buffers is managed as a FIFO memory and consists of 64 32-bit words of memory. During the processing of a given frame the TSIP processes the data from one of the FIFO memories based on whether the PING or PONG buffer is active. The channel buffers are not software accessible once the TDMU has been enabled.

The channel bitmap consists of 64 32-bit words of memory for a total of 2048 bits. Each pair of bits controls the enable/disable state of a physical timeslot. When a given di-bit value is 00b the corresponding physical timeslot is disabled for that channel. Any other di-bit value represents an enabled channel: 01b indicates that the data is 8-bit linear, 10b indicates that the data should be μ-law expanded, and 11b indicates that the data should be A-law expanded.

Figure 3. Channel Bitmap



For a given physical timeslot the corresponding di-bits are read from the channel bitmap for each of the channels. If the physical timeslot is enabled for the channel the data, either 8 or 16 bits, is read from the FIFO memory. If 16-bit data is read from the FIFO memory, the data is compressed to 8 bits using either μ-law or A-law compression. depending on the enable selection. At the transmit side, data samples from multiple timeslots can be loaded from the channel buffer (FIFO memory) into a channel register and unpacked for enabled timeslots. The resulting 8-bit sample data for each of the enabled channels is then OR'd together to create a single 8-bit sample value that is written to the appropriate transmit data register (DXn). Any 8-bit data is read/written from/to the next byte location in the FIFO memory. Any 16-bit data is read/written from/to the next 16-bit word location in the FIFO memory.

2.3.1 A-law and μ-law Companding

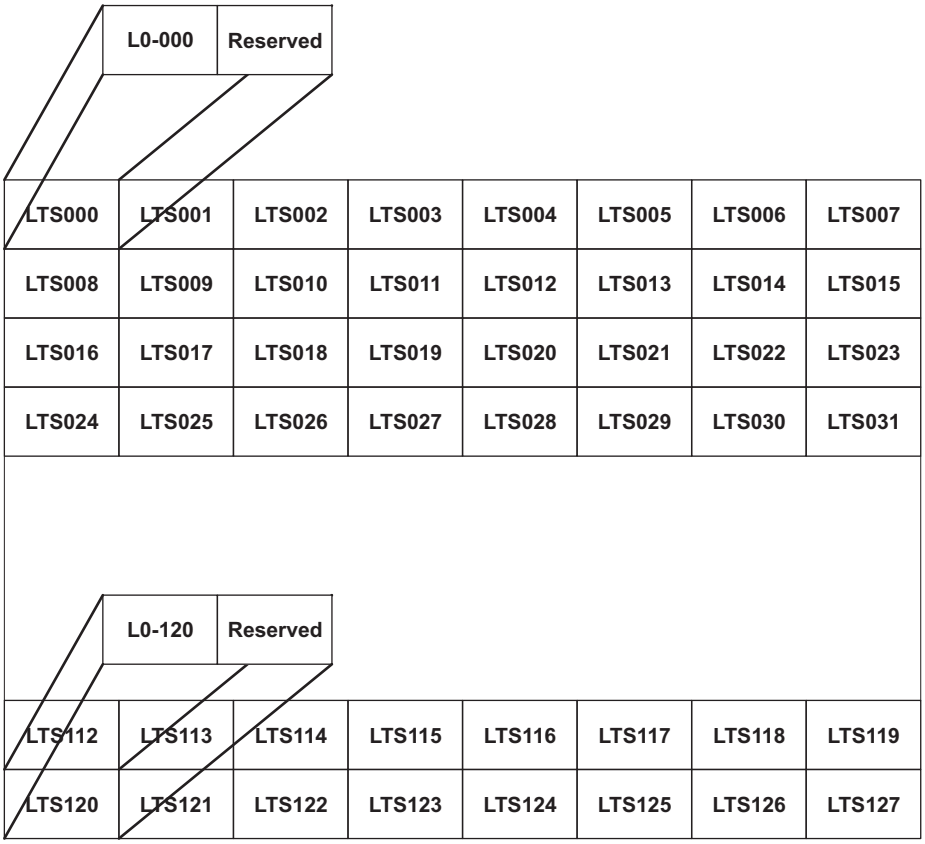
When receive data is μ-law or A-law expanded it is stored left-justified in a 16-bit word. The two or three least significant bits are always zero for μ-law and A-law, respectively. Likewise, transmit data that is to be μ-law or A-law compressed should be left justified. The two or three least significant bits are truncated for the compression. Expansion and compression is completed based on the G.711 standard including the channel coding (bit inversions for ones density).

Since the G.711 standard does not distinguish the μ-law expansion of 0xFF and 0x7F, a special case is created in the TSIP. Both normally result in a 16-bit linear value of 0x0000. For data that undergoes signal processing, this is not a problem. However, for data that is compressed and looped back, the compression results in 0xFF and the original 0x7F code is lost wherever it existed. To prevent this from occurring, the expansion of 0x7F is redefined to be 0xFFFF and the algorithmic compression of the 16-bit value 0xFFFF, which normally results in 0x7E, is treated as a special case to allow 0x7F to be produced. This does not result in any loss in the coding based on the G.711 standard since the G.711 standard only defines the data conversion for 14-bit linear data values and the two least significant bits of the left-justified value in a 16-bit linear format otherwise would be truncated.

2.4 Serial Link Processing and Buffering

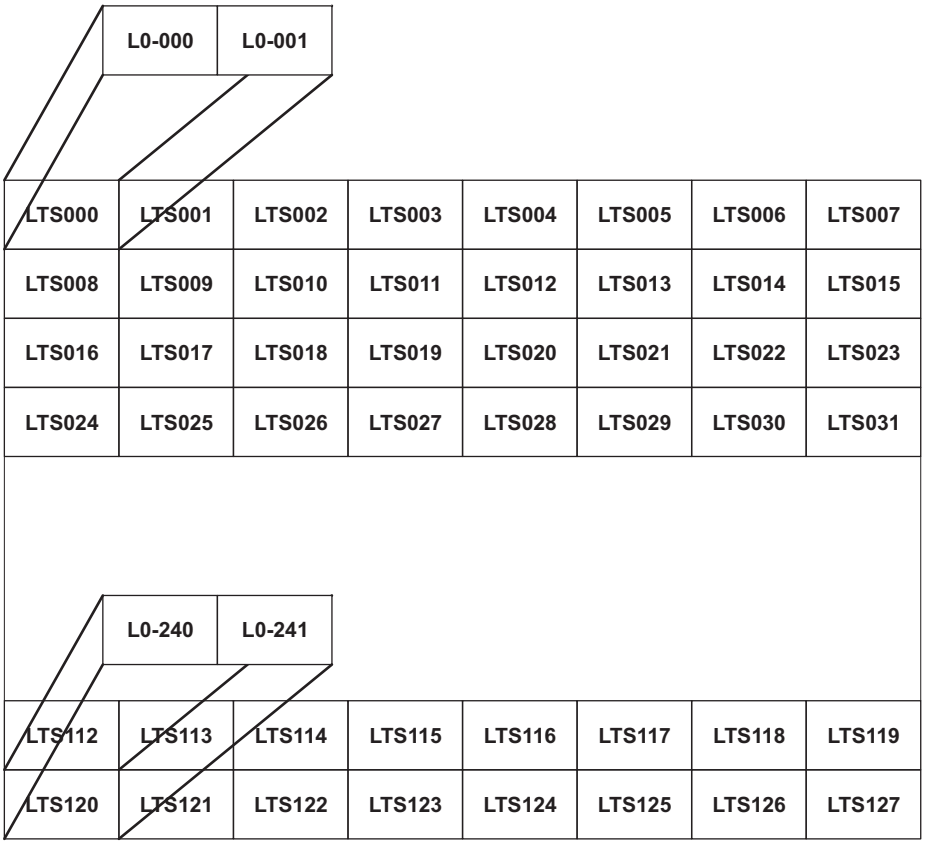
When the selected data rate option is one of the 8 Mbps options, both the two serial interface inputs are active. Links refer to the number of transmit and receive I/Os supported by the TSIP module. Active links refer to the number of transmit and receive I/Os that are usable at a given data rate. Figure 4 illustrates the channel bitmap definition for both 8 Mbps data rate options. The nomenclature defines the logical timeslot, LTSxxx, and physical timeslot, Ln-xxx, where n represents the link number and xxx represents the physical timeslot. When the selected data rate option is the 16 Mbps option one serial interface inputs is active, but data is read from all of the DRn/Dxn registers.

Figure 4. 8 Mbps Channel Definition (2 Links with 2 Active Links)



Di-bit Definition
00b = Disabled
01b = Enabled 8-bit linear
10b = Enabled μ-law
11b = Enabled A-law

Figure 5. 16-Mbps Channel Bitmap Definition (Two Links With One Active Link)



Di-bit Definition
00b = Disabled
01b = Enabled 8-bit linear
10b = Enabled μ-law
11b = Enabled A-law

2.5 Multi-Channel Operation

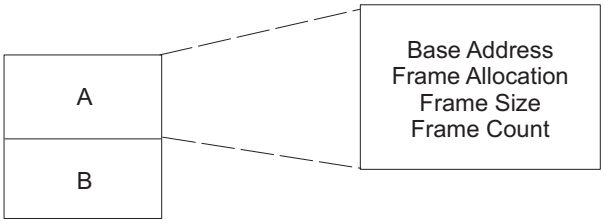
The timeslot data management unit (TDMU) of the TSIP is a multi-channel unit that manages the data for the SIU. There is one transmit and one receive channel for a total of two channels. For each transmit channel, the timeslot context is defined to support enable/disable control of all timeslots on all of the serial outputs operating at an 8.192 Mbps data rate or 128 8-bit timeslots. For each receive channel, the timeslot context control is defined to support enable/disable control of all timeslots on all of the serial inputs operating at an 8.192 Mbps data rate or 128 8-bit timeslots.

Each DMA channel has dual buffers, PING and PONG, that are shared with the TDMU. The use of the dual buffers allows memory buffers, including each frame of data within the memory buffer, to begin at designated locations in memory. When the next frame sync event occurs, the DMATCU flushes the remaining contents of the current channel buffer and then switches focus to the second channel buffer. The channel buffers are not software accessible once the DMATCU has been enabled.

2.5.1 Transmit and Receive Channel Context

The context control for each channel consists of a dual set of configuration registers (A and B). These sets of four configuration registers each become active in direct relationship to the active channel bitmap of the TDMU. The registers define the memory address for the data buffers (Base Address), frame size allocations (Frame Allocation and Frame Size), and number of frames allocated (Frame Count) within the memory buffers, as shown in Figure 6.

Figure 6. Channel Configuration



Each base address register is a 32-bit register representing the base address of a frame buffer in memory. Since data is transferred from the TSIP to memory in 32-bit elements and addresses correspond to byte addresses, the two least significant address bits of the base address must always be zero. The frame buffer in memory consists of storage for multiple frames of data. The number of live frames that can be stored in the frame buffer is defined by the frame count. Frames of data are stored in the frame buffer with the first frame beginning at the base address. When a context switch occurs, the storage based on the new context always begins at the base address defined by that context.

The next frame is stored in the frame buffer beginning at the location defined by the base address plus the frame allocation. When the number of frames defined by the frame count have been stored in memory, the next frame is stored beginning at the base address. Since data transfers are always in 32-bit elements and the frame allocation is an address offset to the base address, the two least significant bits of the frame allocation must be zero.

The frame size is not used explicitly in receive channel transfers. It is present for context consistency and is described with the transmit channel context. With respect to the context, the frame size represents the amount of storage a single frame of data actually occupies, including the 32-bit CID/FRFC synchronization values at the beginning and end of the frame. Realistic frame size values begin at twelve when there is at least one timeslot enabled. The minimum acceptable value for frame size is eight, which implies that there are no real data samples for the frame since eight bytes are required for the two 32-bit synchronization values. A frame size that is less than eight is logged as an error for a channel. In the event that the frame size exceeds the frame allocation there is a potential overlap in the frame data of two frames. The DMATCU detects this condition and logs an error. The DMATCU continues to function using the defined values.

A channel active status register consisting of pairs of bits for each channel (CHn) identifies which channel configuration registers (A or B) is active at any given time for each channel. When a channel configuration (A or B) is active, those configuration registers are write protected. A channel configuration (A or B) that is pending active also is write protected. Write accesses to the inactive configuration registers update the inactive registers. Read accesses from either the active or inactive configuration complete as normal. The status of each CHn field is defined in Table 3. The complete Receive Channel Configuration Active Status Register is shown in Section 7 with the other registers.

Table 3. Channel Configuration Active Status

Bit	Field Name	Value	Description
11:0	CHnCS		Receive channel n (where n is the channel number) active status. Defines whether A and B configurations are in active status.
		00	Both A and B configurations are in active status.
		01	A configuration is active. B configuration is inactive.
		10	A configuration is inactive. B configuration is active.
		11	Reserved

When the channel is disabled, both bitmaps are inactive and can be modified. The least significant bit of the CnID value determines which of the two channel bitmaps is made pending and becomes active on the next superframe. A channel bitmap can be designated as pending active at any time. When a bitmap becomes pending active, both it and the active bitmap are protected until the pending active bitmap is made active and the active bitmap is made inactive. Changes in the actual active assignment always occur on a superframe. Writes to the channel enable register to set the A or B bitmap as pending active must have the CHnENB set to enable the channel or to keep the channel enabled if it is already running. Writes to the channel enable register with a new CnID value in which the least significant bit is identical to the previous CnID value causes the CID value used beginning with the next superframe to be the new value. However, the channel bitmap and DMA context that are currently active remain unchanged. Writes to the channel enable register that clear the channel enable bit take effect on the next frame event.

Table 4. Channel Enable Register

Bit	Field Name	Value	Description
15 - 8	CnID	0x00	Configuration identification. Defines the configuration selection that takes effect on the next superframe synchronization event. The least significant bit determines whether the A or B channel bitmap and configuration registers are used.
0	CHnENB		Channel n enable
		0	Channel n is disabled/stopped.
		1	Channel n is enabled/running.

2.5.2 Frame Format

The first 32-bit location in the frame in the channel buffer is filled with a 32-bit synchronization value. This 32-bit value consists of an 8-bit channel configuration ID (CnID) and the lower 24 bits from the free running frame counter. The channel configuration ID is defined by the software in the corresponding channel enable register. At the end of a receive frame, the beginning of the next frame, when the channel buffer is flushed to memory the same 32-bit value is written once again to the channel buffer. At the same time, a new 32-bit value with at least the incremented free running frame counter is written to the other half of the channel buffer. The presence of the synchronization value at the beginning of the frame in memory provides a way for software to recognize and track the configuration that was used for that frame. The presence of the same value at the end of the frame provides a way for software to confirm that the entire frame has been written to memory.

Figure 7, Figure 8, and Figure 9 illustrate the way the data packing takes place within the channel buffer based on the enabled channels. Figure 7 is a list of enabled physical timeslots for a single receive channel. In this example, the receive data on serial link 1 (TR1) is to be expanded using either μ-law or A-law expansion. The receive data from other serial link is to be stored as 8-bit linear. The first 32-bit location in the channel buffer is filled with a 32-bit synchronization value.

The data for the first three enabled timeslots that are received is 8-bit linear and the data is packed in the channel buffer on successive bytes. As the example illustrates in Figure 8 and Figure 9, when timeslot 8 for TR1 (L1-008) is received, expanded, and stored the next available location is an odd byte location so a dummy byte is inserted and L1-008 is stored on a 16-bit boundary. When L1-045 and L1-046 are received, the next available location is already 16-bit aligned resulting in no extra dummy bytes. However, when L1-050 arrives, the next available location is once again an odd byte resulting in the insertion of a dummy byte to allow L1-050 to be stored on a 16-bit boundary. At the end of a frame, pad bytes are used to align the final 32-bit synchronization value. The actual content of the dummy bytes and pad bytes is undefined.

Figure 7. Example Timeslot List by the TSIP Serial Link for 1 Channel

Link 0	Link 1
004	
005	
008	008
009	
024	
039	
040	
	045
	046
047	
048	
049	
	050
052	
063	
074	
075	
076	
077	
	079
	083
087	
089	
095	
	099
101	
102	

Figure 8. Channel Buffer (BEND=1)

0			31
L0-004	L0-005	L0-008	dummy
L1-008		L0-009	L0-024
L0-039	L0-040	L1-045	
L1-046		L0-047	L0-048
L0-049	dummy	L1-050	
L0-052	L0-063	L0-074	L0-075
L0-076	L0-077	L1-079	
L1-083		L0-087	L0-089
L0-095	dummy	L1-099	
L0-101	L0-102	pad	pad
CID	FRFC		

Figure 9. Channel Buffer (BEND=0)

0 31

dummy	L0-008	L0-005	L0-004
L0-024	L0-009	L1-008	
L1-045		L0-040	L0-039
L0-048	L0-047	L1-046	
L1-050		dummy	L0-049
L0-075	L0-074	L0-063	L0-052
L1-079		L0-077	L0-076
L0-089	L0-087	L1-083	
L1-099		dummy	L0-095
pad	pad	L0-102	L0-101
CID	FRFC		

2.6 Transmit Operation

Once the TSIP is configured for transmission, on the first frame sync after the TSIP is enabled, its DMA engine reads the data from the memory buffers and stores it in internal channel buffers. It starts transmitting from the very next frame sync, depending on the timeslots enabled in the channel. The data for timeslot 0 is sent on the first eight serial data clocks following the recognition of the frame sync signal that signals the start of the frame and the programmed delay. Data that is transmitted by the TSIP is output from a parallel-to-serial register with the most significant bit first, one 8-bit register per serial interface output. The data for timeslot 1 is sent on the next eight serial data clocks immediately following timeslot 0. Data for successive timeslots are continuously transmitted on subsequent serial data clocks. The two transmit data registers, one for each serial interface signal, means that the TSIP executes its load operation up to two times for each timeslot. The number of actual data samples loaded depends on the timeslot enable/disable definition in the channel bitmap for each of the channels. With the data for each timeslot, an enable/disable indication is also provided. The enable/disable indication is used by the serial interface to control the state of the output. Three output states for disabled timeslots are supported: driven high, driven low, and high impedance. The disabled timeslot output state selection is defined by XMTDIS as shown in Table 5.

Table 5. Transmit Disabled State

Bit	Field Name	Value	Description
9-8	XMTDIS(1)		Transmit output disable state
		00	High impedance
		01	Reserved
		10	Driven low
		11	Driven high

(1) This field is write protected when SIU transmit is enabled.

When an enabled timeslot immediately follows a disabled timeslot, it is sometimes desirable to delay the enable of the output buffer for the first bit transmitted on the enabled timeslot. The delay is defined by XMTDLY as shown in Table 6. The selection determines whether the output buffer is turn on immediately for the first bit of the enabled timeslot or whether it is turned on after a delay of one-half serial clock period.

Table 6. Enable Output Delay Selection (XCR)

Bit	Field Name	Value	Description
10	XMTDLY[1]		Transmit output enable delay. Defines a fixed delay for enabling the output buffer on the first bit of an enabled timeslot that immediately follows a disabled timeslot. This control applies only when the disable state for the output buffer is high impedance.
		0	No added delay
		1	Output enable is delayed by one-half serial clock period.

(1) This field is write protected when SIU transmit is enabled.

2.7 Interrupts

2.7.1 Frame Interrupts

Each time the timeslot counter rolls over for the transmit serial links or the receive serial links, the corresponding frame interrupt is made pending. For receive, part of the data for the frame that was just completed prior to the frame sync is in the channel buffer. At least one additional transfer needs to be made to flush the data from the buffer. An acknowledgment of the transfer completion, assuring that the data has actually been written to memory is returned to the TSIP. The TSIP offers the option of asserting the frame interrupt that has been made pending as a result of the frame sync upon receipt of acknowledge for the final transfer, shown in Table 7. A programmable timeslot delay, shown in Table 8, is also available to determine when the interrupt is actually asserted. Based on the telecom interface timing references, this offers the option of generating an interrupt every 125 µs.

Table 7. Frame Interrupt Control (RTDR and XTDR)

Bit	Field Name	Value	Description
13-12	RCVFRINT[1]		Receive frame interrupt selection
		00	Interrupt asserted on transfer acknowledge only.
		01	Interrupt asserted on delay count only.
		10	Interrupt asserted on either transfer acknowledge or delay count.
		11	Interrupt asserted on both transfer acknowledge and delay count.
13-12	XMTFRINT[1]		Transmit frame interrupt selection
		00	Interrupt asserted on transfer acknowledge only.
		01	Interrupt asserted on delay count only.
		10	Interrupt asserted on either transfer acknowledge or delay count.
		11	Interrupt asserted on both transfer acknowledge and delay count.

(1) This field is write protected once DMA is enabled.

Table 8. Timeslot Delay Counter (RTDR and XTDR)

Bit	Field Name	Value	Description
6-0	RCVFDLY[1]	0x07F	Receive frame interrupt delay [0-127]
		n + 1	Number of logical timeslots the frame interrupt is delayed after going pending.
6-0	XMTFDLY[1]	0x07F	Transmit frame interrupt delay
		n + 1	Number of logical timeslots the frame interrupt is delayed after going pending.

(1) This field is write protected once DMA is enabled.

2.7.2 Superframe Interrupt

The frequency of this interrupt is independently programmable with the frame sync counter. The superframe interrupt is made pending on the frame sync counter rollover. The same programmable timeslot delay used with the frame interrupt determines when the interrupt is actually asserted. The actual assertion of the superframe interrupt can be determined solely by the delay, by acknowledgment that the final data transfer for the last frame in the superframe is complete or a combination of both as shown in Table 9.

Table 9. Superframe Interrupt Control (RTDR and XTDR)

Bit	Field Name	Value	Description
15-14	RCVSFINT(1)		Receive superframe interrupt selection
		00	Interrupt asserted on transfer acknowledge only.
		01	Interrupt asserted on delay count only.
		10	Interrupt asserted on either transfer acknowledge or delay count.
		11	Interrupt asserted on both transfer acknowledge and delay count.
15-14	XMTSFINT(1)		Transmit superframe interrupt selection
		00	Interrupt asserted on transfer acknowledge only.
		01	Interrupt asserted on delay count only.
		10	Interrupt asserted on either transfer acknowledge or delay count.
		11	Interrupt asserted on both transfer acknowledge and delay count.

(1) This field is write protected once DMA is enabled.

2.7.3 Error Interrupt

Error interrupts are asserted when certain fault conditions occur. There is one error interrupt per channel. An error interrupt queue for each channel provides a history of up to sixteen error interrupts per channel. Each item in the queue includes an 8-bit error code and 24 bits of additional information. Error codes are listed in Table 10.

2.7.4 Exception Conditions

Table 10. Error Codes

Error Code	Info Field	Category	Description
0x00			No Error
0x01	RCVFRFC	1	Receive Overrun at the beginning of frame
0x02	RCVFRFC	1	Receive Overrun during the frame
0x03	CIDA	3	Receive Overrun - enable channel bitmap greater than Size
0x05	CIDA	3	Receive Size less than 8
0x10	CIDA and CIDF	2	Transmit configuration ID mismatch
0x11	XMTFRFC	1	Transmit Underrun at the beginning of frame
0x12	XMTFRFC	1	Transmit Underrun during the frame
0x13	CIDA	3	Transmit Underrun - enabled channel bitmap greater than Size
0x15	CIDA	3	Transmit Size less than 8
0xF1 - 0xF7			Read status (status) errors.
0xf9 - 0xFF			Write status (status) errors.

2.7.4.1 Receive Errors

Error interrupts are generated on DMATCU and TDMU receive channels due to buffer overrun and context mismatch conditions. A buffer overrun occurs anytime there is no space in the channel buffer for an enabled timeslot.

- **Error Code = 0x01**. This code indicates that the channel buffer is not empty at the beginning of the frame. It is the most serious overrun condition because it indicates that there is receive data in both the PING and PONG buffers. The additional information is the current value of the receive free running frame counter RCVFRFC).
- **Error Code = 0x02**. This code indicates that the channel buffer is full during a frame transfer and the TDMU is unable to add data for an enabled receive timeslot. The additional information is the current value in the receive free running frame counter (RCVFRFC).
- **Error Code = 0x03**. This code indicates that the number of enabled timeslots in the channel bitmap

results in a buffer requirement that exceeds the frame allocation or frame size. The additional information is the current (active) channel configuration ID (CIDA). Also at receive side, if there is a CID mismatch, the TSIP propagates this error.

- **Error Code = 0x05**. This code indicates that the frame size is less than 8, which is the minimum for a channel with no timeslots enabled. The additional information is the current (active) channel configuration ID (CIDA).

2.7.4.2 Transmit Errors

Error interrupts are generated on transmit channels due to buffer underrun and context mismatch conditions. A buffer underrun occurs anytime there is no data in the channel buffer for an enabled timeslot.

- **Error Code = 0x10**. This code indicates that the configuration identity in the transferred frame data does not match the configuration identity in the active context. The additional information is the current (active) channel configuration ID (CIDA) and the transferred frame data channel configuration ID (CIDF).
- **Error Code = 0x11**. This code indicates that the channel buffer is empty at the beginning of the frame. It is the most serious underrun condition because it indicates that both the PING and PONG buffers are empty. The additional information is the current value in the transmit free running frame counter (XMTFRFC).
- **Error Code = 0x12**. This code indicates that the channel buffer is empty during a frame transfer and the TDMU is unable to provide data for an enabled transmit timeslot. The additional information is the current value in the transmit free running frame counter (XMTFRFC).
- **Error Code = 0x13**. This code indicates that the number of enabled timeslots in the channel bitmap results in a buffer requirement that exceeds the frame allocation or frame size. The additional information is the current (active) channel configuration ID (CIDA).
- **Error Code = 0x15**. This code indicates that the frame size is less than 8, which is the minimum for a channel with no timeslots enabled. The additional information is the current (active) channel configuration ID (CIDA).

2.7.4.3 Bus Errors

When a bus error occurs, a 3-bit status code is returned by the slave to the master. The master for the TSIP is the DMA interface, which is driven by the DMATCU. The status codes are provided for read and write transactions independently. A status code of 0 is an indication of success for both reads and writes, and no entry is made in the error interrupt queue. When any other status code is returned the code is added to 0xF0 for reads and 0xF8 for writes and stored in the error interrupt queue.

2.7.5 Error Queue Management

The error queue for each channel is maintained in FIFO format with a write to pop requirement. The write to pop an entry from the queue allows the top of the queue to be inspected in a watch window during an emulation halt without removing the entry from the queue. For each queue two memory mapped registers are used to support queries of the queue. The first register is a control or queue management register. The second register includes a count of the number of errors on a given queue. A third register location is used to represent the top of the error queue, or the oldest error on the queue. When an error occurs, the error code and information are added to the queue for the appropriate channel and the error interrupt is asserted. If the queue is full, the new error is discarded and an overflow is indicated. Once the overflow indication is set, all subsequent errors are discarded, even if there is space on the queue, until the CPU (user) clears the overflow condition. When a CPU responds to an error interrupt, it performs the following steps.

1. The count register for the channel error queue is read and the number of error entries on the queue is obtained.
2. The error queue register is read to obtain the top (oldest) error entry on the queue.
3. The entry is removed or popped off the queue by doing a write to the error queue register.
4. If the count read in step 1 is greater than 1, then steps 2 and 3 should be repeated until all error entries have been read from the queue.

Reading the error queue register when the count register is zero returns an error entry value of zero.

2.7.6 Error Recovery

In the case where a frame sync pulse occurs before the frame period (1024 serial data clocks for the default configuration) has completed that frame sync pulse is ignored. The 1024 serial data clocks in the default configuration represent 128 8-bit timeslots. Once all of the required timeslots have been counted, the next frame sync pulse defines the beginning of a new frame. In the case where a frame sync pulse does not occur until some number of clock periods after the frame period has completed, the additional serial data clocks are ignored. During the time when the serial data clocks are ignored, no timeslot events are created and no data is clocked in or out of the SIU. When the frame sync pulse does occur, the bit counter begins counting from its initial value with the appropriate delay to the frame sync input. In the case where the serial data clock is removed or aborted in some other way, the data for at most one frame is corrupted although there may be one or more frame periods of missing data. When the serial data clock is restored, the number of clock periods needed to complete the frame that was in progress when the serial data clock was removed are counted. Any data received and transmitted during this period is considered corrupted. The elapsed time also corresponds to additional missing frames of data. Any frame sync pulses that occur during that time are ignored. Once enough serial data clocks have occurred to correspond to the frame period the serial interface recognizes, the next frame sync input and data is received and transmitted starting with that frame sync.

2.8 Endianness

The way in which the time ordered data is packed and unpacked in the channel buffer is determined by the endian mode selection (BEND), as shown in Table 11. The 32-bit synchronization value that is also included in the channel buffer is not affected by the endian mode selection. Figure 8 and Figure 9 show the resulting packed data in the channel buffer for the two endian modes. The 32-bit synchronization value (CID+FRFC) is stored in the same manner independent of the endian selection. In addition, the 16-bit expanded data samples are stored in the same manner within a 16-bit field independent of the endian selection. There is no byte swapping within the designated fields for either 32-bit or 16-bit values.

Table 11. Endian Mode Selection

Bit	Field Name	Value	Description
0	BEND[1]		Endian mode selection. Bend = iso bend + 1.
		0	Little Endian format
		1	Big Endian format

(1) This field is write protected once DMA is enabled.

2.9 Priority Control

More than one channel can have its transfer request flag set. When there are multiple transfer request flags set, round-robin arbitration is used to select the next channel for transfer. To sequence all transfers (reads and writes), the winning receive channel may also need to win arbitration with a transmit channel. Priority for contested receive and transmit channel requests within the TSIP is traded back and forth with each contested request. The priority of the transfer request made by the TSIP to access memory is defined by PRI as shown in Table 12. The priority is escalated by one additional level; if possible, each time the channel buffer fills to the point that another transfer request could be generated while an existing request remains outstanding. Escalation is limited by MAXPRI, also shown in Table 12. MAXPRI is expected to be a value that is less than or equal to PRI. When MAXPRI and PRI are equal, no escalation is made. If MAXPRI is greater than PRI, the programmed value is ignored and MAXPRI is treated as though it is equal to PRI. When the last transfer request has been generated (that is, when the completion of the transfer request leaves fewer than eight 32-bit words in the channel buffer), the normal priority, defined by PRI, is restored. For example, a transfer request is made at the normal priority when the channel buffer initially contains eight 32-bit words to be transferred to memory. In the event that an additional eight 32-bit words are added to the same channel buffer before the transfer is completed for the first request, the priority is escalated one additional level. If there are fewer than eight 32-bit words remaining in the channel buffer when the second request has been generated, the priority is reduced back to the normal priority level for the next request.

Table 12. DMATCU Transfer Priority (DMATCU_CGR)

Bit	Field Name	Value	Description
6-4	MAXPRI(1)		Maximum transfer priority
		0	Priority 0 - Highest priority
		1	Priority 1
		...	...
		7	Priority 7 - Lowest priority
2-0	PRI(1)		Transfer priority
		0	Priority 0 - Highest priority
		1	Priority 1
		...	...
		7	Priority 7 - Lowest priority

(1) This field is write protected once DMA is enabled.

3 Clocks, Frames and Data

3.1 Frame and Clock Operation

The clock is expected to be a continuously running clock with uniform clock periods and with exactly the timeslot count times the bit count number of clock periods between frame sync pulses. With the default counter values that are used with 8.192 Mbps links this period is exactly 1024 clocks. The TSIP anticipates the frame sync pulses to come at that interval. When the frame sync pulse occurs early or late the response of the TSIP is defined to assure that the operation recovers gracefully.

3.2 Data Rate Options

The TSIP offers two data rate options. The data rate options are listed in Table 13 with some corresponding information. Data rate options are available to support double clocking (default) or single clocking of the serial data for 8.192, 16.384 Mbps serial links. When the serial data rate changes, the maximum number of active serial data links is also changed. There is an inverse relationship between the two: 2 active links at 8.192 Mbps, 1 active link at 16.384 Mbps. However, the total number of 8-bit timeslots is constant for all data rate options. When the number of active links is reduced, the output buffers for the inactive links are put in the defined disabled state. The defined disabled state for inactive links is the same as the one defined for disabled timeslots.

Table 13. Data Rate Options

Option	Name	Active Links	Data Rate	Clock Frequency	Timeslots/Link
000	8M16	8	8.192 Mbps	16.384 MHz	128
001	8M8	8	8.192 Mbps	8.192 MHz	128
101	16M32	4	16.384 Mbps	32.768 MHz	256
011	16M16	4	16.384 Mbps	16.384 MHz	256

3.3 Clock and Frame Sync Redundancy

The receive and transmit interfaces share a clock, frame sync, and data rate by default. This setup offers the option of redundant (primary and secondary) clock and frame sync sources that can be switched when the primary source fails. An option allows the receive and transmit interfaces to be configured independently with each having its own clock and frame sync and possibly data rates. The default configuration uses one clock and frame sync as the primary and the second clock and frame sync as the secondary. This configuration uses the primary clock and frame sync to control the transmit data on all two data outputs and the receive data on all two data inputs. The use of a primary and secondary serial clock and frame sync allows the serial links to be maintained with a small impact on the data. The impact is limited to the loss of a few frames of data when a switchover is required. Transitions between the use of the primary clock and frame sync and the backup clock and frame sync are handled by software changing the configuration based on a message that it receives. The selection of the clock and frame sync also can be independent for the transmit serial links and the receive serial links. This provides a second configuration option in which the clock and frame sync used for transmit is different from the clock and frame sync used for receive. In this configuration there is no secondary or backup source. The selection of redundant or independent clocking is made using CLKD as shown in Table 14.

Table 14. Clock Redundancy Selection (SIU_GCR)

Bit	Field Name	Value	Description
4	CLKD		Clock redundancy selection.
		0	Redundant clock mode. Transmit and receive share the same clock and frame sync. The common selections are those defined by XMTSRC, SMTCLKM, and MTDATR in the transmit select and enable register. The RCVSRC, RCVCLKM, and RCVDATR fields are ignored.
		1	Dual clock mode. Transmit and receive are specified totally independently.

3.4 Single and Double Data Rate

Data rate options are independent for receive (RCVCLKM and RCVDATR) and transmit (XMTCLKM and XMTDATR) when CLKD is 1. RCVCLKM and XMTCLKM define whether a double-rate or single-rate clock is being provided for receive and transmit, respectively. For a double-rate clock there are two sample clock edges per data bit. Data is sampled on any of the two edges, depending on the edge that frame sync is detected and also on the polarities of the data sampling clock edge configuration. RCVDATR and XMTDATR define the actual data rate (or timeslots per link) for receive and transmit as shown in Table 15.

Table 15. Single Rate and Double Rate Clock Options

Bit	Field Name	Value	Description
0	RCVCLKM		Receive clock mode
		0	TCLK_x is a double-rate clock.
		1	TCLK_x is a single-rate clock
0	XMTCLKM		Transmit clock mode
		0	TCLK_x is a double-rate clock.
		1	TCLK_x is a single-rate clock
2-1	RCVDATR		Receive data rate
		00	8.192 Mbps
		01	16.384 Mbps
		10	32.768 Mbps
		11	Reserved
2-1	RCVDATR		Transmit data rate
		00	8.192 Mbps
		01	16.384 Mbps
		10	32.768 Mbps
		11	Reserved

3.5 Clock and Frame Sync Selection and Polarity

Clock selection is independent for receive (RCVSRC) and transmit (XMTSRC) when CLKD is 1. RCVSRC and XMTSRC select both the source clock and frame sync for receive and transmit respectively, as shown in Table 16. All receive serial links use a common clock and frame sync. All transmit serial links use a common clock and frame sync.

Table 16. Clock and Frame Sync Source Selection (RCLKR and XCLKR)

Bit	Field Name	Value	Description
0	RCVSRC		Receive data clock and frame sync selection
		0	TCLK_A and TFS_A
		1	TCLK_B and TFS_B
0	XMTSRC		Transmit clock and frame sync selection
		0	TCLK_A and TFS_A
		1	TCLK_B and TFS_B

The polarity of the clock and frame sync is software selectable and can be defined independently for data and frame sync as well as receive and transmit. Table 17 provides a description of the clock polarity for data (RCVDCLKP and XMTDCLKP) and frame sync (RCVFCLKP and XMTFCLKP).

The polarity of the frame sync is software selectable and can be defined independently for receive and transmit. RCVFSYNCP and XMTFSYNCP determine the polarity of frame sync for receive and transmit respectively, as shown in Table 17.

Table 17. Frame Sync Polarity (RCR and XCR)

Bit	Field Name	Value	Description
7	RCVFSYNCP[1]		Receive frame sync polarity
		0	Receive frame sync is active low.
		1	Receive frame sync is active high.
7	XMTFSYNCP[2]		Transmit frame sync polarity
		0	Transmit frame sync is active low.
		1	Transmit frame sync is active high.

(1) This field is write protected when SIU receive is enabled.
(2) This field is write protected when SIU transmit is enabled.

3.6 Data Delay

Data delay is configurable for receive and transmit data. Data delay determines the delay, in sample clock edges, to the first data sample clock edge for timeslot 0 following the sampled recognition of frame sync, as shown in Table 18. With a double-rate clock, the first data bit for timeslot 0 cannot be driven on the same edge that frame sync is sampled and recognized, or on the first edge following the edge following sampling and recognition of frame sync when the frame sync clock and data clock polarities differ.

To affect a data delay of zero, the delay value must be programmed to the exact number of serial clocks between the sampled recognition of successive frame syncs. The number of serial clocks between successive frame syncs is data rate dependent. For a single-rate 8 Mbps serial link with exactly 128 timeslots, there are 1024 clocks and XMTDATD should be programmed to 1023. For a double-rate 8 Mbps serial link with exactly 128 timeslots, there are 2048 clocks and XMTDATD should be programmed to 2047. Values larger than those just defined allow a serial clock to be defined with one or more additional clock periods between frame syncs for zero-data-delay operation. Programming XMTDATD to 1024 for a single rate 8 Mbps serial link with 128 timeslots to create an actual delay of 1025 clock cycles is not equivalent to a data delay of 1 (which is defined by setting XMTDATD to 0). The ability to independently select the clock polarity for frame sync and data, along with the additional ability to configure operation for data delay from the recognition of frame sync to the first bit of timeslot 0 in the corresponding frame offers the flexibility to define delays in half-cycle increments. The shortest supported delay is 1.5 cycles.

Table 18. Data Delay (RCR and XCR)

Bit	Field Name	Value	Description
29-16	RCVDATD[1]	0x0000	Receive data delay [0-16383]
		n + 1.5	When clock polarity for data and frame sync differs
		n + 2	When clock polarity for data and frame sync is identical
29-16	XMTDATD[2]	0x0000	Transmit data delay [0-16383]
		n + 1.5	When clock polarity for data and frame sync differs
		n + 2	When clock polarity for data and frame sync is identical

(1) This field is write protected when SIU receive is enabled.
(2) This field is write protected when SIU transmit is enabled.

3.7 Data and Frames

3.7.1 Frame Size

A timeslot counter (10 bits) counts the timeslot events (or logical timeslots) that make up a frame. The RCVFSIZ bit in the Receive Size register (see Section 7.2.10) and the XMTFSIZ bit in the Transmit Size register (see Section 7.2.7) provide the rollover counts. The default rollover count for the timeslot counter is 127. In the default configuration the timeslot counter defines a frame size of 128 logical timeslots, which is the minimum number of timeslots for the frame. Because the 16.384 Mbps data rate options combine the shift registers in sets of two, there is two physical timeslots per logical timeslot. This typically means that the number of logical timeslots per frame is the same for all data rate options.

Is the following table necessary since I added references to the actual registers for these bits?

Table 19. Timeslot Counter (RSR and XSR)[(1)]

Bit	Field Name	Value	Description
6-0	RCVFSIZ[(2)]	0x7F	Receive frame size [0-127]
		n + 1	Number of logical timeslots per frame. Minimum number of logical timeslot periods per frame.
		≤6	Values of 6 and less are reserved. Attempts to write a value of 6 or less results in a value of 0x7F being registered.
6-0	XMTFSIZ[(3)]	0x7F	Transmit frame size [0-127]
		n + 1	Number of logical timeslots per frame. Minimum number of logical timeslot periods per frame.
		≤6	Values of 6 and less are reserved. Attempts to write a value of 6 or less results in a value of 0x7F being registered.

(1) If CLKD is programmed to 0 or RCVSRC and XMTSRC will be written with the same value, then RCVFSIZ and XMTFSIZ must be programmed with the same value.
(2) This field is write protected when SIU receive is enabled.
(3) This field is write protected when SIU transmit is enabled.

3.7.2 Frame Count

A frame sync counter (8 bits) counts the frame sync input pulses (frame sync events) that make up a superframe. It outputs a superframe event on every Nth frame sync event. The RCVFCNT bit in the Receive register (see Section 7.2.10) and the XMTFCNT bit in the Transmit Size register (see Section 7.2.7) provide the rollover counts. The default rollover count for the frame sync counter is 3 which defines a superframe size of 4 frames. The frame sync counter is synchronized with the first valid frame sync input. The superframe event is provided to the TDMU, DMATCU, and interrupt generator.

Is the following table necessary since I added references to the actual registers for these bits?

Table 20. Frame Sync Counter (RSR and XSR)

Bit	Field Name	Value	Description
23-16	RCVFCNT[(1)]	0x3	Receive frame count [0-255]
		n + 1	Number of frames per superframe
23-16	XMTFCNT[(2)]	0x3	Transmit frame count [0-255]
		n + 1	Number of frames per superframe.

(1) This field is write protected when SIU receive is enabled.
(2) This field is write protected when SIU transmit is enabled.

3.8 Data Synchronization

3.8.1 Transmit and Receive Synchronization

The frame sync and timeslot counter described in Section 3.7 is synchronized with the first valid frame sync input. A timeslot counter rollover event is used to switch from using the channel PING buffer to the channel PONG buffer for each channel, or to switch from using the channel PONG buffer to the channel PING buffer for each channel. Channel buffer switching is locked together for receive channel. It is also locked together for transmit channel although the receive and transmit channels are not necessarily locked with each other. For receive this means that if the TDMU has been using the channel PING (or PONG) buffer while processing timeslots from frame N, it begins using the channel PONG (or PING) buffer while processing timeslots from frame N+1. If the DMATCU has not emptied the channel PONG buffer by the start of frame N+1, the TDMU does not overwrite the channel PONG buffer until it is emptied. Instead the data is discarded, frame N+1 is lost, and the buffer overrun flag is set. For transmit this means that if the transmit process logic has been using the channel PING (or PONG) buffer while processing timeslots for frame N, it begins using the channel PONG (or PING) buffer while processing timeslots for frame N+1. If the DMATCU has not transferred any timeslot data into the channel PONG buffer by the start of frame N+1, there is no new data for the TDMU to process and send to the SIU. Due to the lack of data, the TDMU sends an all ones (0xFF) value for all enabled timeslots. This means that frame N+1 went out with erroneous data and the actual data for frame N+1 is never transmitted. The buffer underrun flag is set also.

3.8.2 TDMU Control Operation

The control operation of the TDMU provides and verifies synchronization information in each of the channel buffers. This includes data synchronization signatures and the FIFO read and write pointers.

At the beginning of a receive frame, the control operation writes a 32-bit synchronization value to each of the receive channel buffers for that frame. The 32-bit value consists of an 8-bit channel configuration configuration ID and the lower 24 bits from the free running frame counter. The channel configuration ID is defined by the software in the corresponding channel enable register. The receive free running frame counter is described in Section 7.2.13.

At the end of a receive frame, the beginning of the next frame, when the channel buffer will be flushed to memory, the same 32-bit value is written once again to the channel buffer. At the same time, a new 32-bit value, with at least the incremented free running frame counter, is written to the other half of the channel buffer. The presence of the synchronization value at the beginning of the frame in memory provides a way for software to recognize and track the configuration that was used for that frame. The presence of the same value at the end of the frame provides a way for software to confirm that the entire frame has been written to memory.

At the beginning of a transmit frame, the control operation reads the first 32-bit value in the transmit channel buffers for that frame. Only the upper 8 bits are significant and represent the channel configuration ID. The value read is expected to match the active channel configuration ID. If it does not, an error interrupt is generated.

At the end of a transmit frame, a 32-bit value including the channel configuration ID and free running frame counter are recorded. This 32-bit value, which the DMATCU is responsible for writing back to memory, can be used by software to confirm its frame sequencing and synchronization. The transmit free running frame counter is described in Section 7.2.12.

3.8.3 Context Synchronization

Context switches between the A and B context definitions on each respective channel is made at the completion of a superframe. Each time a superframe event occurs, the channel context for the channel can be switched from A to B or from B to A. For the channel dedicated to the transmit serial links, the superframe event occurs at the beginning of the Nth frame period. For the channel dedicated to the receive serial links, the superframe event occurs at the end of the Nth frame period. In both transmit and receive, the context switch takes place so that it is in effect for frame N+1.

4 Reset and Powerdown Modes

4.1 SIU Reset and Shutdown Operation

The entire SIU can be reset with a single reset bit (SIURST), as shown in Table 21. Asserting the SIU reset causes both receive and transmit serial interfaces to halt operation.

Table 21. SIU Reset

Bit	Field Name	Value	Description
0	SIURST		SIU reset
			Reads:
		0	Reset is complete. SIU can be enabled for operation.
		1	Reset is in progress.
			Writes:
		0	Writes of 0 have no affect.
		1	Reset the SIU.

4.1.1 SIU Reset

When SIURST is set, the entire SIU module is reset. All registers that define SIU operation or provide the status for SIU operation are initialized to their predefined state. When read, SIURST indicates the status of the reset operation. SIURST remains 1 until the SIU has been shut down and all SIU control registers have been initialized to their predefined state. When the reset initialization is complete, SIURST becomes 0. Writing 0 to SIURST has no effect.

4.1.2 Receive SIU Shutdown

When the receive interface is stopped, RCVENB is written as 0 after being 1, and all of the serial-to parallel registers, data registers, and counters used for the receive operation are cleared. The programmed configuration defining the operation of the receive interface is not affected when the receive interface is disabled. No events or interrupts are generated while the receive interface is disabled. When RCVENB is written as 1 after being 0, the operation of the receive interface is enabled, and the first active frame sync input is recognized and serial data capture begins immediately. The first active frame sync is recognized only when the enabled SIU receive is able to first detect the frame sync input in an inactive state.

4.1.3 Transmit SIU Shutdown

When the transmit interface is stopped, XMTENB is written as 0 after being 1, and all of the parallel to-serial registers, data registers, and counters used for the transmit operation are cleared. The output state of the output buffers is controlled by the output state configuration for disabled timeslots. The programmed configuration defining the operation of the transmit interface is not affected when the transmit interface is disabled. No events or interrupts are generated while the transmit interface is disabled. When XMTENB is written as 1 after being 0 the operation of the transmit interface is enabled, and the first active frame sync input is recognized but data transmission does not begin until the second active frame sync input is recognized. This assures sufficient time for the serial interface to signal the DMA controller and for the DMA controller to respond with timeslot 0 data prior to the second active frame sync pulse. The first active frame sync is recognized only when the enabled SIU transmit is able to first detect the frame sync input in an inactive state. During the period between the first and second active frame syncs, the data output is in the disabled state, as defined in Section 2.6, for all timeslots.

4.2 TDMU and DMATCU Software Reset and Shutdown Operation

The TDMU and DMATCU can be reset or stopped (disabled) entirely. Individual channels can be stopped (disabled) independently as well. Resetting the entire TDMU and DMATCU causes all channels to be placed into a stopped (disabled) state. Stopping the TDMU and DMATCU causes the operation to be stopped but does not necessarily alter the state of the individual channels.

Stopping individual channels results in those channels not responding to the timeslot, frame, and superframe events generated by the serial interface. Stopping the TDMU channels does not affect the operation of the SIU.

Reset of the TDMU and DMATCU occurs when DMARST is written as a 1. There is one DMAENB bit for the TDMU and DMATCU together. There is XMTCHnENB bit and RCVCHnENB bit for the channel.

4.3 Powerdown

The TSIP supports clock stop handshaking with the use of the local powerdown and sleep controller (LPSC).

Automatic powerdown and sleep is not supported. The TSIP indicates its state (idle or active) through tsip_idle_po. The idle state is indicated only when all enable bits in the TSIP control registers (RCVENB, XMTENB, DMAENB, CHnENB) are cleared to the disabled state and all pending bus transactions have completed. The LPSC can be configured to make clock stop requests to the TSIP. If the TSIP is in an idle state the clock stop request is acknowledged and the gated clock can then be stopped. If TSIP is in an active state the clock stop request is not acknowledged.

5 Emulation and Loopback Modes

Two control bits, FREE and SOFT, determine the response of the serial interface to the emulation input. Table 22 provides the definitions of FREE and SOFT.

Table 22. Emulation Control (ETR)

Bit	Field Name	Value	Description
0	FREE[1]		Free run selection
		0	SOFT takes effect.
		1	Ignore emulation input. Continue to function normally.
1	SOFT[1]		Halt selection
		0	Halt receive and transmit SIU, TDMU, and DMATCU at the completion of the current frame.
		1	Halt receive TDMU and DMATCU at the completion of the current frame. Transmit continues to function normally.

(1) This field is write protected once DMA is enabled.

5.1 Emulation - Free Run

When FREE=1 it defines the operation to be free running even under emulation halt conditions. The TSIP continues to operate as normal with data being received, buffered, and transferred to memory and data being transferred from memory, buffered, and transmitted based on the presence of the necessary external serial data clock and frame sync inputs.

5.2 Emulation - Halt

When FREE=0 the operation is defined by SOFT. The presence of the necessary external serial data clock and frame sync inputs is assumed as well.

For SOFT=0, the operation of the TSIP continues as normal until the end of the current frame. At the end of the current frame the TSIP operation gets halted. The frame interrupt/event for the beginning of the next frame and the possible superframe interrupt/event is generated.

For SOFT=1, the operation of the TSIP continues as normal until the end of the current frame. Receive operation is halted from very next frame, transmit continues to work normally in this mode. But as the DMA controller is not functional, transmit memory buffers are not updated during this time, since the same data for the sequence of frames that is currently in the memory buffer continues to be sent over and over.

5.3 Loopback Modes

Internal loopback modes are provided to test the functionality of the TSIP. These loopback test modes allow the functionality to be tested with a minimum of external stimulus or with a minimal amount of internal software to support data processing.

5.3.1 Serial Interface Loopback Modes

The TSIP SIU offers operational test supports data loopback (DLB) and link loop back (LLB), as illustrated in Figure 10. The loopback test modes, when enabled, are mutually exclusive. Control bits, SIUTST, and LBS determine the operation of the serial interface for test loopback. The definitions of SIUTST and LBS are found in Table 23. A common external clock and frame sync for receive and transmit are required for loopback testing to be successful.

Figure 10. Loopback Test Modes

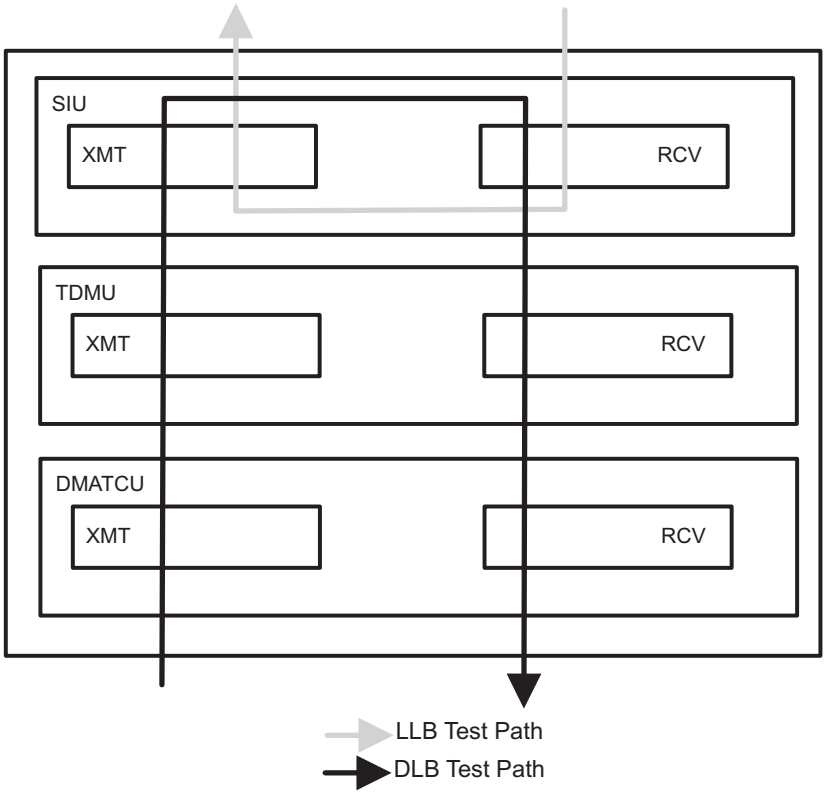


Table 23. SIU Loopback Test Control (ETR)

Bit	Field Name	Value	Description
16	SIUTST[1]		Serial loopback test mode enable
		0	Normal operating mode is enabled. LBS is ignored.
		1	Serial loopback test is enabled.
17	LBS[1]		Serial loopback test mode selection
		0	DLB is selected.
		1	LLB is selected.

(1) This field is write protected once DMA is enabled.

5.3.2 DLB Loopback Testing

DLB enables the serial link interface to be tested from inside the device. In this loopback test configuration, the SXn outputs are internally connected to the corresponding SRn inputs. The TXn output pins are disabled. The TRn input pins are ignored. Corresponding timeslots for transmit and receive should be enabled in the TSIP DMA. Successful operation is determined by comparing a receive frame buffer in memory with the corresponding transmit frame buffer in memory.

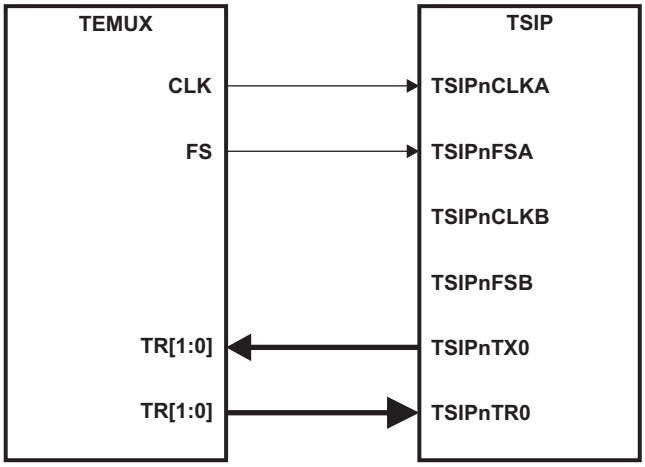
5.3.3 LLB Loopback Testing

LLB enables the serial link interface to be tested from outside the device. In this loopback test configuration, the DRn outputs are internally connected to the corresponding DXn inputs. Successful operation is determined by comparing the transmit serial links with a delayed version of the receive serial links.

6 TSIP Initialization Procedure

Depending on the system requirements, the TSIP data rate, clock settings, frame sync settings and the DMA channel configurations need to be set. The following example is for a typical case where the TSIP is used in a system configuration in which it is connected to a TEMUX device with 8 Mbps data rate and 16 MHz clock frequency, with the same clock and frame sync being used for transmit and receive.

Figure 11. TSIP Connected to TEMUX



In this configuration, CLKA and FSA are used by the transmit and receive logic for clock and frame synchronization.

1. Ensure that XMTENB, RCVENB, DMA channel enable, and DMAENB are cleared to make certain that the TSIP is in reset. Reset SIU and DMA in case the TSIP is not shut down properly.
2. As the same clock and frame sync is being used by the TSIP TX and RX, configure CLKD to select the redundant clock.
3. If redundant clock mode is used, XMTSRC, XMTCLKM and XMTDATR must be configured to select the clock source and clock rate. If redundant clock mode is not used, configure both transmit and receive registers for the same. The XMTSRC field has to be cleared for the TSIP to use the clock source A and FSA. For 8 Mbps data rate, XMTDATR has to be set to 0x0. As the TSIP data clock rate is at 16 MHz for this system, XMTCLKM sound be configured to 0x0 for selecting the double data rate clock mode.
4. Clock and frame sync polarities must be configured depending on whether the TEMUX device is driving active low or active high signal for frame sync and depending on the clock-edge at which it is driving the data.
5. Configure the XMTDIS state depending on how the transmit lanes have to be tri-stated in the system.
6. XMTDATD and RCVDATD need to be set based on the delay in the system for the first valid data to be received by the TSIP after the frame sync is detected. SIU is set to transmit/receive the data on its TX and TR lanes.
7. Based on the call setup and teardown messages from the host, the system should be configured for the transmit and receive frame size after determining the number of logical timeslots that need to be enabled in a frame. Depending on the system, Determine the frame count that needs to be there in each superframe.
8. Configure the endianness and priority of the TSIP master in the system as per the system requirements.
9. Enable the interrupts required to the system from the TSIP.
10. Configure the DMA channel context registers depending on the channels to be enabled. Once DMA context is written, configure the CnID and enable the channel by writing into the CHnENB bit.
11. Enable the DMA by setting DMAENB and enable SIU by setting the XMTENB and RCVENB bits.
12. The TSIP is set to receive and transmit data on the next Frame Sync.
13. The TSIP switches between the PING and PONG buffers on every superframe. Hence, the system can configure the DMA channel parameters for a context switch while the TSIP transfer is going on.

Bitmap slots can be re-enabled depending on the call setup messages received for the next superframe using the ping-pong buffer mechanism.

7 Registers

This section includes the TSIP memory map information and registers.

7.1 TSIP Memory Map

Table 24 to Table 36 provide additional register memory map information. Table 1 lists the summary memory map for the registers for the TSIP.

Table 24. TSIP Module Registers

Offset Address	Type	Reset Value	Reset By(1)	Description
0x00000000	Constant	0x0060MMmm	H	PID Register
0x00000004	Configuration	0x00000001	H, S	Emulation and Test Register
0x00000008	Configuration	0x00000000	H	Reset Register
0x0000000C -- 0x0000007C				Reserved

(1) H=Hardware reset, S=SIURST, D=DMARST

Table 25. Serial Interface Registers

Offset Address	Type	Reset Value	Reset By(1)	Description
0x00000080	Configuration	0x00000000	H, S	SIU Global Control Register
0x00000084 -- 0x0000009C				Reserved
0x000000A0	Configuration	0x00000000	H, S	Transmit Clock Source Register
0x000000A4	Configuration	0x00000000	H, S	Transmit Control Register
0x000000A8	Configuration	0x0000007F	H, S	Transmit Size Register
0x0000000AC -- 0x000000BC				Reserved
0x0000000C0	Configuration	0x00000000	H, S	Receive Clock Source Register
0x000000C4	Configuration	0x00000000	H, S	Receive Control Register
0x000000C8	Configuration	0x0000007F	H, S	Receive Size Register
0x0000000CC -- 0x000000FC				Reserved

(1) H=Hardware reset, S=SIURST, D=DMARST

Table 26. TDMU Global Registers

Offset Address	Type	Reset Value	Reset By (1)	Description
0x00000100	Configuration	0x00000000	H, D	TDMU Global Control Register
0x00000104	Status	0x00000000	H, D	Transmit Free Running Frame Counter
0x00000108	Status	0x00000000	H, D	Receive Free Running Frame Counter
0x0000010C	Configuration	0x00000000	H, D	TDMU Global Configuration Register
0x0000010	Status	0x00000000	H, D	Transmit Channel Active Status Register
0x000000114	Status	0x00000000	H, D	Receive Channel Active Status Register
0x000000118 -- 0x0000017C				Reserved

(1) H=Hardware reset, S=SIURST, D=DMARST

Table 27. DMATCU Global Registers

Offset Address	Type	Reset Value	Reset By[1]	Description
0x00000180	Configuration	0x00000077	H, D	DMATCU Global Control Register
0x00000184	Configuration	0x0000007F	H, D	Transmit Timeslot Delay Counter
0x00000188	Configuration	0x0000007F	H, D	Receive Timeslot Delay Counter
0x0000018C				Reserved
0x00000190	Status	0x00000000	H, D	Transmit Channel Active Status Register
0x000000194	Status	0x00000000	H, D	Receive Channel Active Status Register
0x000000198 -- 0x000001FC				Reserved

(1) H=Hardware reset, S=SIURST, D=DMARST

Table 28. TDMU Channel Error Registers

Offset Address	Type	Reset Value	Reset By [1]	Description
0x00000200	Configuration	0x00000000	H, D	TX/RX Channel 0 Error Control Register
0x00000204	Status	0x00000000	H, D	TX/RX Channel 0 Error Count Register
0x00000208	Status	0x00000000	H, D	TX/RX Channel 0 Error Queue Register
0x0000020C				Reserved

(1) H=Hardware reset, S=SIURST, D=DMARST

Table 29. TX/RX Channel 0 Error Registers

Offset Address	Register Description
0x00000200 -- 0x0000020C	TX/RX channel 0 error log registers
0x00000210 -- 0x000003FC	Reserved

Table 30. TDMU Channel Registers

Offset Address	Register Description
0x00000800 -- 0x0000081C	Transmit channel 0 registers
0x00000820 -- 0x00000BFC	Reserved
0x00000C00 -- 0x00000C1C	Receive channel 0 registers
0x00000C20 -- 0x00000FFC	Reserved

Table 31. TDMU Transmit Channel 0 Registers

Offset Address	Type	Reset Value	Reset By [1]	Description
0x00000800	Configuration	0x00000000	H, D	Transmit channel 0 enable register
0x00000804 -- 0x0000081C				Reserved

(1) H=Hardware reset, S=SIURST, D=DMARST

Table 32. TDMU Receive Channel 0 Registers

Offset Address	Type	Reset Value	Reset By [1]	Description
0x00000C00	Configuration	0x00000000	H, D	Receive channel 0 enable register
0x00000C04 -- 0x00000C1C				Reserved

(1) H=Hardware reset, S=SIURST, D=DMARST

Table 33. DMATCU Channel Registers

Offset Address	Register Description
0x00001000 -- 0x0000101C	Transmit channel 0 configuration A Registers
0x00001020 -- 0x0000103C	Transmit channel 0 configuration B registers
0x00001040 -- 0x000017FC	Reserved
0x00001800 -- 0x0000181C	Receive channel 0 configuration A registers

Table 33. DMATCU Channel Registers (continued)

Offset Address	Register Description
0x00001820 -- 0x0000183C	Receive channel 0 configuration B registers
0x00001840 -- 0x00001FFC	Reserved

Table 34. DMATCU Transmit Channel 0 Registers

Offset Address	Type	Reset Value	Reset By (1)	Description
0x00001000	Configuration	0x00000000	H, D	Memory Base Address Register A
0x00001004	Configuration	0x00000000	H, D	Frame Allocation Register A
0x00001008	Configuration	0x00000000	H, D	Frame Size Register A
0x0000100C	Configuration	0x00000000	H, D	Frame Count Register A
0x000001010 -- 0x0000101C				Reserved
0x000001020	Configuration	0x00000000	H, D	Memory Base Address Register B
0x000001024	Configuration	0x00000000	H, D	Frame Allocation Register B
0x000001028	Configuration	0x00000000	H, D	Frame Size Register B
0x00000102C	Configuration	0x00000000	H, D	Frame Count Register B
0x000001030 -- 0x00000103C				Reserved

(1) H=Hardware reset, S=SIURST, D=DMARST

Table 35. DMATCU Receive Channel 0 Registers

Offset Address	Type	Reset Value	Reset By(1)	Description
0x00001800	Configuration	0x00000000	H, D	Memory Base Address Register A
0x00001804	Configuration	0x00000000	H, D	Frame Allocation Register A
0x00001808	Configuration	0x00000000	H, D	Frame Size Register A
0x0000180C	Configuration	0x00000000	H, D	Frame Count Register A
0x000001810 -- 0x0000181C				Reserved
0x000001820	Configuration	0x00000000	H, D	Memory Base Address Register B
0x000001824	Configuration	0x00000000	H, D	Frame Allocation Register B
0x000001828	Configuration	0x00000000	H, D	Frame Size Register B
0x00001820C	Configuration	0x00000000	H, D	Frame Count Register B
0x000001830 -- 0x00000183C				Reserved

(1) H=Hardware reset, S=SIURST, D=DMARST

Table 36. TDMU Channel Bitmap Registers

Offset Address	Register Description
0x00008000 -- 0x0000801C	Transmit channel 0 bitmap A
0x00008020 – 0x000080FC	Reserved
0x00008100 -- 0x0000811C	Transmit channel 0 bitmap B
0x00008120 -- 0x0000BFFC	Reserved
0x0000C000 -- 0x0000C01C	Receive channel 0 bitmap A
0x0000C020 – 0x0000C0FC	Reserved
0x0000C100 -- 0x0000C11C	Receive channel 0 bitmap B
0x0000C120 -- 0x0000FFFC	Reserved

7.2 Register Description

This section provides a detailed definition of the peripheral module constant registers.

7.2.1 PID Register

The PID register is shown in Figure 12 and described in Table 37.

Figure 12. PID Register (0x00000000)

31 16	15 8	7 0
MODID	MAJOR	MINOR
R-0x0060	R-0x01	R-1x00

LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 37. PID Register Field Descriptions

Bit	Field Name	Value	Description
31 - 16	MODID	0x0060	Module ID
15 - 8	MAJOR	0x01	Major Version Value
7 - 0	MINOR	0x00	Minor Version Value

7.2.2 Emulation and Test Register

The emulation and test register is shown in Figure 13 and described in Table 38.

Figure 13. Emulation and Test Register (0x00000004)

31 25	24 20	19 18	17	16
Reserved	Reserved		LBS	SIU TST
R-0	R/W-0		R/W-0	R/W-0

15 8	7 2	1	0
Reserved	Reserved	SOFT	FREE
R-0	R-0		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 38. Emulation and Test Register Field Descriptions

Bit	Field Name	Value	Description
31 - 25	Reserved	0x0000	Reserved
17	LBS[1]		Serial test mode selection
		0	External
		1	Internal
16	SIUTST[1]		Serial test mode enable
		0	Normal operating mode is enabled. LBS is ignored.
		1	Serial loopback test mode is enabled.
15 - 2	Reserved	0x00	Reserved
1	SOFT[1]		Halt selection
		0	Halt SIU, TDMU, and DMTCU at the completion of the current frame.
		1	Halt receive TDMU and DMATCU at the completion of the current frame.
0	Free[1]		Free run selection
		0	SOFT takes effect.
		1	Ignore emulation input. Continue to function normally.

(1) This field is write protected once DMA is enabled.

7.2.3 Reset Register

The reset register is shown in Figure 14 and described in Table 39.

Figure 14. Reset Register (0x00000008)

31	2	1	0
Reserved		DMA	SIU
R-0x00000000		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = Value after reset

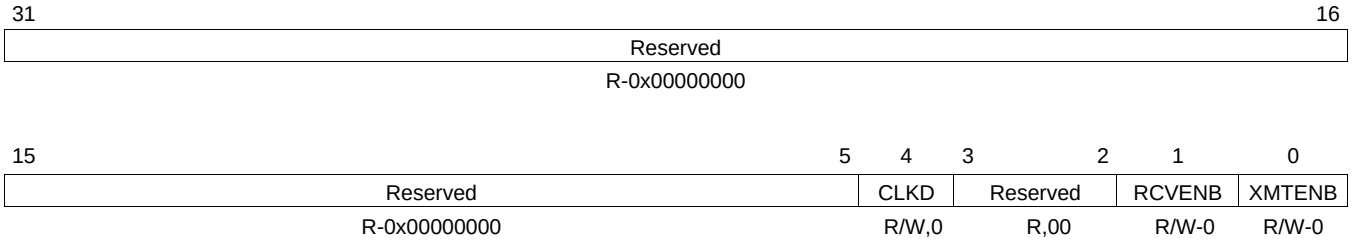
Table 39. Reset Register Field Descriptions

Bit	Field Name	Value	Description
31 - 2	Reserved	0x00000000	Reserved
1	DMA		TDMU and DMATCU reset
			Reads:
		0	Reset is complete. TDMU and DMATCU can be enabled for operation.
		1	Reset is in progress.
			Writes:
		0	Writes of 0 have no affect.
		1	Reset the TDMU and DMATCU.
0	SIU		SIU reset
			Reads:
		0	Reset is complete. SIU can be enabled for operation.
		1	Reset is in progress.
			Writes:
		0	Writes of 0 have no affect.
		1	Reset the SIU.

7.2.4 SIU Global Control Register

The SIU global control register is shown in Figure 15 and described in Table 40.

Figure 15. SIU Global Control Register (0x00000080)



LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

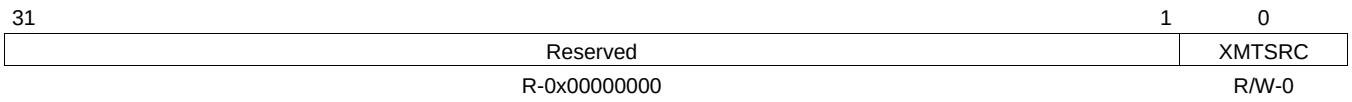
Table 40. SIU Global Control Register Field Descriptions

Bit	Field Name	Value	Description
31 - 5	Reserved	0x00000000	Reserved
4	CLKD		Clock redundancy selection
		0	Redundant clock mode. Transmit and receive share the same clock and frame sync. The common selections are those defined by SMTSRC, SMTCLKM, and SMTDATR in the transmit select and enable register. The RCVSRC, RCVCLKM, and RCVDATR fields are ignored.
		1	Dual clock mode. Transmit and receive are specified totally independently.
3-2	Reserved	0	Reserved
1	RCVENB		Receive enable
		0	Receive serial interface is disabled/stopped.
		1	Receive serial interface is enabled/running.
0	XMTENB		Transmit enable
		0	Transmit serial interface is disabled/stopped.
		1	Transmit serial interface is enabled/running.

7.2.5 Transmit Clock Source Register

The transmit clock source register is shown in Figure 16 and described in Table 41.

Figure 16. Transmit Clock Source Register (0x000000A0)



LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

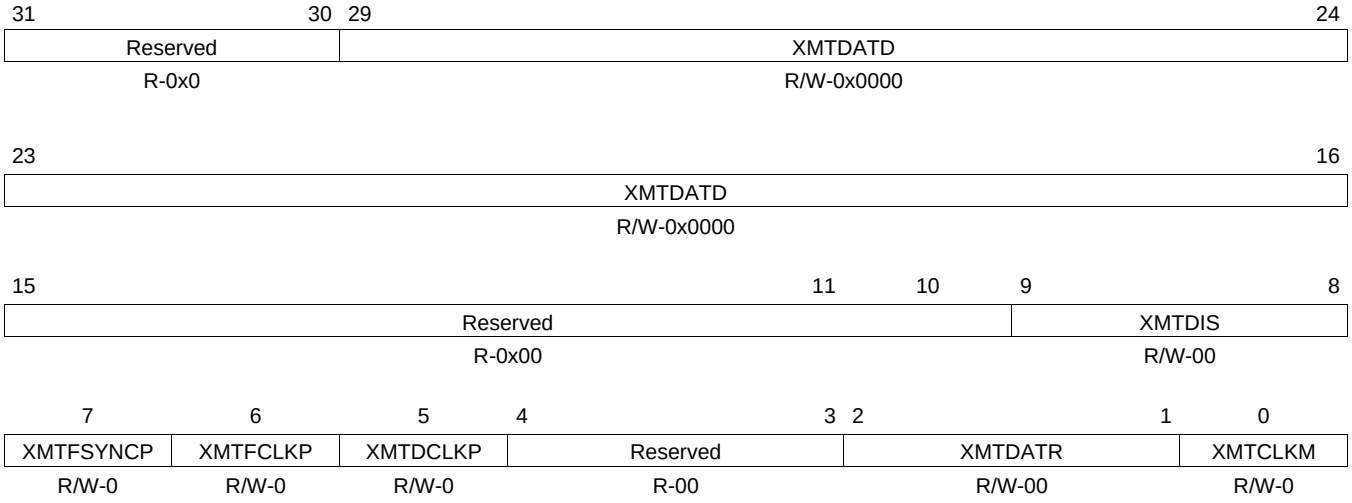
Table 41. Transmit Clock Source Register Field Descriptions

Bit	Field Name	Value	Description
31 - 1	Reserved	0x00000000	Reserved
0	XMTSRC		Transmit clock and frame sync selection
		0	TCLK_A and TFS_A
		1	TCLK_B and TFS_B

7.2.6 Transmit Control Register

The transmit control register is shown in Figure 17 and described in Table 42.

Figure 17. Transmit Control Register (0x000000A4)



LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 42. Transmit Control Register Field Descriptions[1]

Bit	Field Name	Value	Description
31 - 30	Reserved	0x0	Reserved
29 - 16	XMTDATD[2]	0x0000	Transmit data delay [0-16383]
		n + 1.5	When clock polarity for data and frame sync differs.
		n + 2	When clock polarity for data and frame sync is identical.
15 - 10	Reserved	0x00	Reserved
9-8	XMTDIS[2]		Transmit output disable state
		00	High impedance
		01	Reserved
		10	Driven low
		11	Driven high
7	XMTFSYNCP[2]		Transmit frame sync polarity
		0	Transmit frame sync is active low.
		1	Transmit frame sync is active high.
6	XMTFCLKP[2]		Transmit frame sync clock polarity
		0	Transmit frame sync is sampled on the rising edge of TCLK_x.
		1	Transmit frame sync is sampled on the falling edge of TCLK_x.
5	XMTDCLKP[2]		Transmit data clock polarity
		0	Transmit data is driven on the rising edge of TCLK_x.
		1	Transmit data is driven on the falling edge of TCLK_x.
4-3	Reserved	0	Reserved

(1) If XMTCLKD is programmed to 0 or RCVSRC and XMTSRC will be written with the same value, then RCVFSYNCP and XMTFSYNCP must be programmed with the same value. Likewise, RCVFCLKP and XMTFCLKP must be programmed with the same value.

(2) This field is write protected when SIU transmit is enabled.

Table 42. Transmit Control Register Field Descriptions (continued)

Bit	Field Name	Value	Description
2-1	XMTDATR[2]		Transmit data rate
		00	8.192 Mbps
		01	16.384 Mbps
		10	Reserved
		11	Reserved
0	XMTCLKM[2]		Transmit clock mode
		0	TCLK_x is a double rate clock.
		1	TCLK_x is a single rate clock.

7.2.7 Transmit Size Register

The transmit size register is shown in Figure 18 and described in Table 43.

Figure 18. Transmit Size Register (0x000000A8)

31 24	23 16	15 7	6 0
Reserved	XMTFCNT	Reserved	XMTFSIZ
R-0x000	R/W-0x3	R-0x00	R/W-0x07F

LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 43. Transmit Size Register Field Descriptions[1]

Bit	Field Name	Value	Description
31 - 24	Reserved	0x000	Reserved
23 - 16	XMTFCNT[2]	0x3	Transmit frame count [0-255] n + 1 Number of frames per superframe
15 - 7	Reserved	0x00	Reserved
6 - 0	XMTFSIZ[2]	0x7F	Transmit frame size [0-27] n + 1 Number of logical timeslots per frame. Minimum number of logical timeslot periods per frame. ≤6 Values of 6 and less are reserved. Attempts to write a value of 6 or less result in a value of 0x7F being registered.

(1) If CLKD is programmed to 0 or RCVSRC and XMTSRC will be written with the same value, then RCVFSIZ and XMTFSIZ must be programmed with the same value.
(2) This field is write protected when SIU transmit is enabled.

7.2.8 Receive Clock Source Register

The receive clock source register is shown in Figure 19 and described in Table 44.

Figure 19. Receive Clock Source Register (0x000000C0)

31 1	0
Reserved	RCVSRC
R-0x00000000	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 44. Transmit Clock Source Register Field Descriptions

Bit	Field Name	Value	Description
31 - 1	Reserved	0x00000000	Reserved
0	RCVSRC		Receive clock and frame sync selection
		0	TCLK_A and TFS_A
		1	TCLK_B and TFS_B

7.2.9 Receive Control Register

The receive control register is shown in Figure 20 and described in Table 45.

Figure 20. Receive Control Register (0x000000C4)

31	30	29	16	15	8
Reserved		RCVDATD		Reserved	
R-0x0		R/W-0x0000		R-0x00	

7	6	5	4	3	2	1	0
RCVFSYNCP	RCVFCLKP	RCVDCLKP	Reserved		RCVDATR		RCVCLKM
R/W-0	R/W-0	R/W-0	R-00		R/W-00		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 45. Receive Control Register Field Descriptions[1]

Bit	Field Name	Value	Description
31 - 30	Reserved	0x0	Reserved
29 - 16	RCVDATD[2]	0x0000	Receive data delay [0-16383]
		n + 1.5	When clock polarity for data and frame sync differs.
		n + 2	When clock polarity for data and frame sync is identical.
15 -8	Reserved	0x00	Reserved
7	RCVFSYNCP[2]		Receive frame sync polarity
		0	Receive frame sync is active low.
		1	Receive frame sync is active high.
6	RCVFCLKP[2]		Receive frame sync clock polarity
		0	Receive frame sync is sampled on the rising edge of TCLK_x.
		1	Receive frame sync is sampled on the falling edge of TCLK_x.
5	RCVDCLKP[2]		Receive data clock polarity
		0	Receive data is sampled on the rising edge of TCLK_x.
		1	Receive data is sampled on the falling edge of TCLK_x.
4-3	Reserved	0	Reserved
2-1	RCVDATR[2]		Receive data rate
		00	8.192 Mbps
		01	16.384 Mbps
		10	Reserved
		11	Reserved
0	RCVCLKM[2]		Receive clock mode
		0	TCLK_x is a double rate clock.
		1	TCLK_x is a single rate clock.

(1) If CLKD is programmed to 0 or RCVSRC and XMTSRC will be written with the same value, then RCVFSYNCP and XMTFSYNCP must be programmed with the same value. Likewise, RCVFCLKP and XMTFCLKP must be programmed with the same value.

(2) This field is write protected when SIU receive is enabled.

7.2.10 Receive Size Register

The receive size register is shown in Figure 21 and described in Table 46.

Figure 21. Receive Size Register (0x000000C8)

31 24	23 16	15 7	6 0
Reserved	RCVFCNT	Reserved	RCVFSIZ
R-0x000	R/W-0x3	R-0x00	R/W-0x07F

LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 46. Receive Size Register Field Descriptions[1]

Bit	Field Name	Value	Description
31 - 24	Reserved	0x000	Reserved
23 - 16	RCVFCNT[2]	0x3	Receive frame count [0-255] n + 1 Number of frames per superframe
15 - 7	Reserved	0x00	Reserved
6 - 0	RCVFSIZ[2]	0x7F	Receive frame size [0-27] n + 1 Number of logical timeslots per frame. Minimum number of logical timeslot periods per frame. ≤6 Values of 6 and less are reserved. Attempts to write a value of 6 or less will result in a value of 0x7F being registered.

(1) If CLKD is programmed to 0 or RCVSRC and XMTSRC will be written with the same value, then RCVFSIZ and XMTFSIZ must be programmed with the same value.
(2) This field is write protected when SIU receive is enabled.

7.2.11 TDMU Global Control Register

The TDMU global control register is shown in Figure 22 and described in Table 47.

Figure 22. TDMU Global Control Register (0x000000C0)

31 1	0
Reserved	DMAENB
R-0x00000000	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 47. TDMU Global Control Register Field Descriptions

Bit	Field Name	Value	Description
31 - 1	Reserved	0	Reserved
0	DMAENB		TDMU and DMATCU enable
		0	TDMU and DMATCU is disabled/stopped.
		1	TDMU and DMATCU is enabled/running.

7.2.12 Transmit Free Running Frame Counter

The transmit free running frame counter is shown in Figure 23 and described in Table 48.

Figure 23. Transmit Free Running Frame Counter (0x00000104)

31	24	23	0
Reserved		FRFC	
R-0x00		R-0x000000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 48. Transmit Free Running Frame Counter Field Descriptions

Bit	Field Name	Value	Description
31 - 24	Reserved	0x00	Reserved
23 - 0	FRFC	0x000000	Free running frame counter

7.2.13 Receive Free Running Frame Counter

The receive free running frame counter is shown in Figure 24 and described in Table 49.

Figure 24. Receive Free Running Frame Counter (0x00000108)

31	24	23	0
Reserved		FRFC	
R-0x00		R-0x000000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 49. Receive Free Running Frame Counter Field Descriptions

Bit	Field Name	Value	Description
31 - 24	Reserved	0x00	Reserved
23 - 0	FRFC	0x000000	Free running frame counter

7.2.14 TDMU Global Configuration Register

The TDMU global configuration register is shown in Figure 25 and described in Table 50.

Figure 25. TDMU Global Configuration Register (0x0000010C)

31	1	0
Reserved		BEND
R-0x00000000		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 50. TDMU Global Configuration Register Field Descriptions

Bit	Field Name	Value	Description
31 - 1	Reserved	0x00000000	Reserved
0	BEND[(1)]		Endian mode selection
		0	Little endian format
		1	Big endian format

(1) This field is write protected once DMA is enabled.

7.2.15 Transmit Channel Bitmap Active Status Register

The transmit channel bitmap active status register is shown in Figure 26 and described in Table 51.

Figure 26. Transmit Channel Bitmap Active Status Register (0x00000110)

31	16
Reserved	
R-0	

15	2	1	0
Reserved		CH0BMS	
R-0		R-00	

LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 51. Transmit Channel Bitmap Active Status Register Field Descriptions

Bit	Field Name	Value	Description
31:2	Reserved		Reserved
1:0	CH0BMS		Transmit channel 0 active status. Defines whether A and B bitmap is active or inactive.
		00	Both A and B bitmaps are inactive.
		01	A bitmap is active. B bitmap is inactive.
		10	A bitmap is inactive. B bitmap is active
		11	Reserved

7.2.16 Receive Channel Bitmap Active Status Register

The receive channel bitmap active status register is shown in Figure 27 and described in Table 52.

Figure 27. Receive Channel Bitmap Active Status Register (0x00000114)

31	16
Reserved	
R-0	

15	2	1	0
Reserved		CH0BMS	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 52. Receive Channel Bitmap Active Status Register Field Descriptions

Bit	Field Name	Value	Description
31 - 2	Reserved	0	Reserved
1 - 0	CH0BMS		Receive channel 0 active status. Defines whether A and B bitmap is active or inactive.
		00	Both A and B bitmaps are inactive.
		01	A bitmap is active. B bitmap is inactive.
		10	A bitmap is inactive. B bitmap is active.
		11	Reserved

7.2.17 DMATCU Global Control Register

The DMATCU global control register is shown in Figure 28 and described in Table 53.

Figure 28. DMATCU Global Control Register (0x00000180)

31	16
Reserved	
R-0x000000	

15	7	6	4	3	2	0
Reserved		MAXPRI		Reserved	PRI	
R-0		R/W-0x7		R-0b	R/W-0x7	

LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 53. DMATCU Global Control Register Field Descriptions

Bit	Field Name	Value	Description
31 - 7	Reserved	0x000000	Reserved
6 - 4	MAXPRI(1)		Maximum Transfer Priority. MAXPRI is expected to be programmed with a value less than or equal to PRI. When MAXPRI is greater than PRI, it is treated as if it were equal and no escalation or de-escalation takes place.
		0	Priority 0 - Highest priority
		1	Priority 1
		...	Priority 2-6
		7	Priority 7 - Lowest priority.
3	Reserved	0b	Reserved
2 - 0	PRI(1)		Transfer Priority.
		0	Priority 0 - Highest priority
		1	Priority 1
		...	Priority 2-6
		7	Priority 7 - Lowest priority

(1) This field is write protected once DMA is enabled.

7.2.18 Transmit Timeslot Delay Register

The transmit timeslot delay register is shown in Figure 29 and described in Table 54.

Figure 29. Transmit Timeslot Delay Register (0x00000184)

31	16
Reserved	
R-0x000000	

15	14	13	12	11	9	8	7	6	0
XMTSFINT		XMTFRINT		Reserved	XMTFDLY				
R-00b		R-00b		R-00000b	R/W-0x07F				

LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 54. Transmit Timeslot Register Field Descriptions

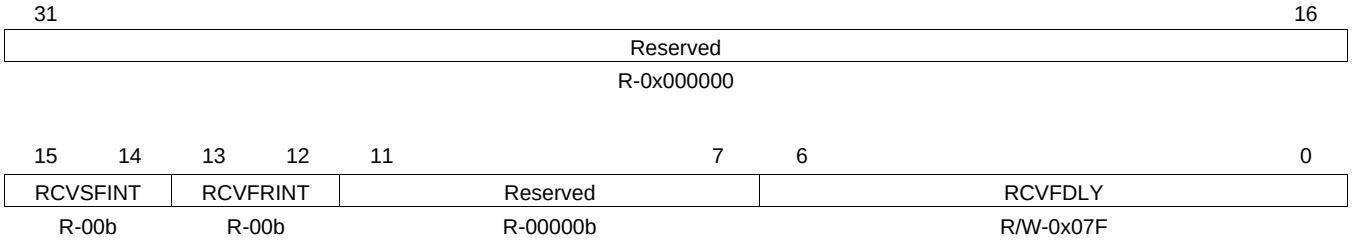
Bit	Field Name	Value	Description
31 - 16	Reserved	0x000000	Reserved
15 - 14	XMTSFINT[1]		Transmit superframe interrupt selection
		00	Interrupt asserted on transfer acknowledge only.
		01	Interrupt asserted on delay count only.
		10	Interrupt asserted on either transfer acknowledge or delay count.
		11	Interrupt asserted on both transfer acknowledge and delay count.
13 - 12	XMTFRINT[1]		Transmit frame interrupt selection
		00	Interrupt asserted on transfer acknowledge only.
		01	Interrupt asserted on delay count only.
		10	Interrupt asserted on either transfer acknowledge or delay count.
		11	Interrupt asserted on both transfer acknowledge and delay count.
11 - 10	Reserved	00000b	Reserved
9 - 0	XMTFDLY[1]	0x07F	Transfer frame interrupt delay [0-127]
		n + 1	Number of logical timeslots the frame interrupt is delayed after going pending.

(1) This field is write protected once DMA is enabled.

7.2.19 Receive Timeslot Delay Register

The receive timeslot delay register is shown in Figure 30 and described in Table 55.

Figure 30. Receive Timeslot Delay Register (0x00000188)



LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 55. Receive Timeslot Delay Register Field Descriptions

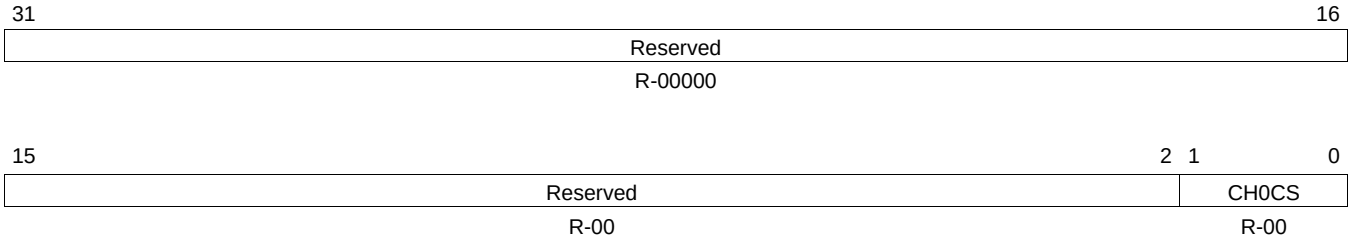
Bit	Field Name	Value	Description
31 - 16	Reserved	0x000000	Reserved
15 - 14	RCVSFINT[1]		Receive superframe interrupt selection
		00	Interrupt asserted on transfer acknowledge only.
		01	Interrupt asserted on delay count only.
		10	Interrupt asserted on either transfer acknowledge or delay count.
		11	Interrupt asserted on both transfer acknowledge and delay count.
13 - 12	RCVFRINT[1]		Receive frame interrupt selection
		00	Interrupt asserted on transfer acknowledge only.
		01	Interrupt asserted on delay count only.
		10	Interrupt asserted on either transfer acknowledge or delay count.
		11	Interrupt asserted on both transfer acknowledge and delay count.
11 - 7	Reserved	00000b	Reserved
6 - 0	RCVFDLY[1]	0x07F	Receive frame interrupt delay [0-127]
		n + 1	Number of logical timeslots the frame interrupt is delayed after going pending.

(1) This field is write protected once DMA is enabled.

7.2.20 Transmit Channel Configuration Active Status Register

The transmit channel configuration active status register is shown in Figure 31 and described in Table 56.

Figure 31. Transmit Channel Configuration Active Status Register (0x00000190)



LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

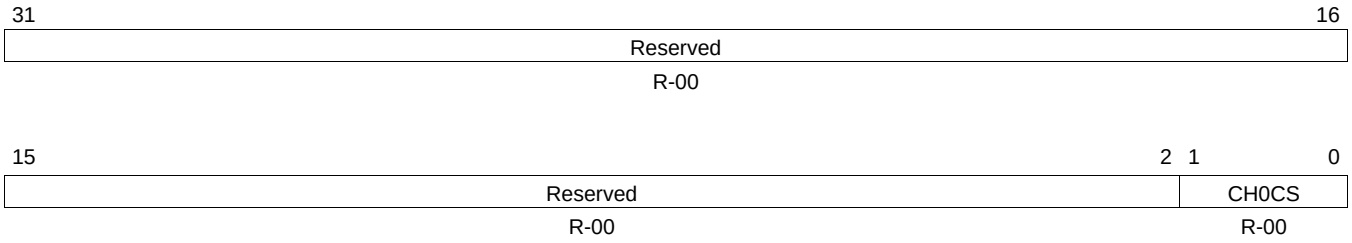
Table 56. Transmit Channel Configuration Active Status Register Field Descriptions

Bit	Field Name	Value	Description
31 - 2	Reserved	0x00000	Reserved
1 - 0	CH0CS		Transmit channel 5 active status. Defines whether the A and B configurations are active or inactive.
		00	Both A and B configurations are inactive.
		01	A configuration is active. B configuration is inactive.
		10	A configuration is inactive. B configuration is active.
		11	Reserved

7.2.21 Receive Channel Configuration Active Status Register

The receive channel configuration active status register is shown in Figure 32 and described in Table 57.

Figure 32. Receive Channel Configuration Active Status Register (0x00000194)



LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 57. Receive Channel Configuration Active Status Register Field Descriptions

Bit	Field Name	Value	Description
31 - 2	Reserved	0x000000	Reserved
1 - 0	CH0CS		Receive channel 5 active status. Defines whether A and Configuration is active or inactive.
		00	Both A and B configurations are inactive.
		01	A configuration is active. B configuration is inactive.
		10	A configuration is inactive. B configuration is active.
		11	Reserved

7.2.22 Channel *n* Error Control Register

The channel *n* error control register is shown in Figure 33 and described in Table 58.

Figure 33. Channel *n* Error Control Register

31	16
Reserved	
R-0x000000	

15	9	8	7	2	1	0
Reserved		CLRQOV	Reserved		CLRQ	POPQ
R-0x000000		R/W-0	R-0x00		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 58. Channel *n* Error Control Register Field Descriptions

Bit	Field Name	Value	Description
31 - 9	Reserved	0x000000	Reserved
8	CLRQOV		Clear error queue overflow flag. This bit is always read as 0.
		0	Write 0 has no effect.
		1	Write 1 to clear the error queue overflow flag in the error count register.
7 - 2	Reserved	0x00	Reserved
1	CLRQ		Clear error queue. This bit is always read as 0.
		0	Write 0 has no effect.
		1	Write 1 to clear the error queue of all error entries.
0	POPQ		Pop the top entry off the queue. This bit is always read as 0.
		0	Write 0 has no effect.
		1	Write 1 to pop the top error entry off the error queue.

7.2.23 Channel *n* Error Count Register

The channel *n* error count register is shown in Figure 34 and described in Table 59.

Figure 34. Channel *n* Error Count Register

31	16
Reserved	
R-0x000000	

15	9	8	7	5	4	0
Reserved		EQOV	Reserved		ECNT	
R-0x000000		R-0b	R-0x0		R-0x00	

LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 59. Channel *n* Error Count Register Field Descriptions

Bit	Field Name	Value	Description
31 - 9	Reserved	0x000000	Reserved
8	EQOV		Error Queue Overflow. The overflow flag is set to indicate that the error detection logic was unable to add at least one error entry to the error queue. Once the overflow flag is set it remains set until it is cleared by a write to the overflow clear bit in the error queue control register. Reading entries from the queue does not automatically clear the overflow flag.
7 - 5	Reserved	0x0	Reserved
4 - 0	ECNT		Error Count, the number of unread entries on the error queue.

7.2.24 Channel *n* Error Queue Register

The channel *n* error queue register is shown in Figure 35 and described in Table 60.

Figure 35. Channel *n* Error Queue Register

31	24	23	0
ERRCODE		INFO	
R-0x00		R-0x000000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

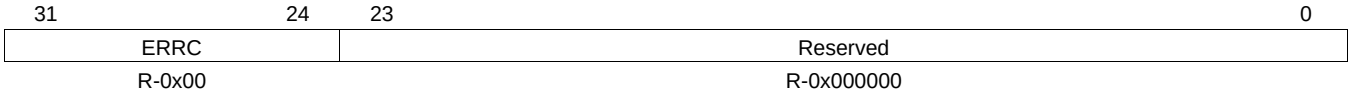
Table 60. Channel *n* Error Queue Register Field Descriptions

Bit	Field Name	Value	Description
31 - 24	ERRCODE		Error Code
23 - 0	INFO		Error Information Field. Information specific to the cause of the error is provided in this field. The specific format is error specific as defined by the following error code figures.

7.2.25 CAT-0 Error Code Format Register

The CAT-0 error code format register is shown in Figure 36 and described in Table 61.

Figure 36. CAT-0 Error Code Format Register



LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

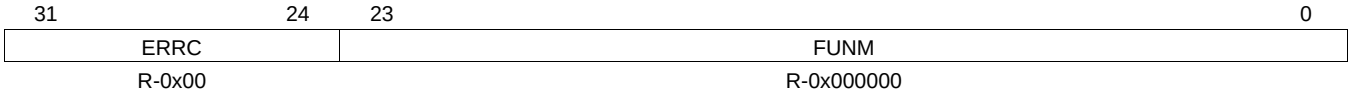
Table 61. CAT-0 Error Code Format Register Field Descriptions

Bit	Field Name	Value	Description
31 - 24	ERRC		Error code
23 - 0	Reserved	0x000000	Reserved

7.2.26 CAT-1 Error Code Format Register

The CAT-1 error code format register is shown in Figure 37 and described in Table 62.

Figure 37. CAT-1 Error Code Format Register



LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

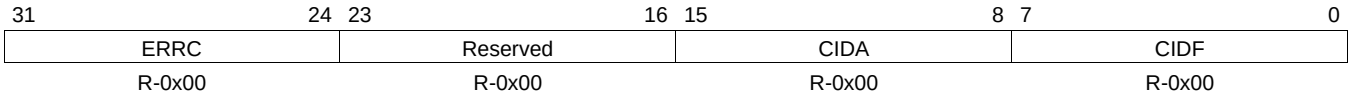
Table 62. CAT-1 Error Code Format Register Field Descriptions

Bit	Field Name	Reset Value	Description
31 - 24	ERRC	0x00	Error code
23 - 0	FNUM	0x000000	Free running frame counter value

7.2.27 CAT-2 Error Code Format Register

The CAT-2 error code format register is shown in Figure 38 and described in Table 63.

Figure 38. CAT-2 Error Code Format Register



LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

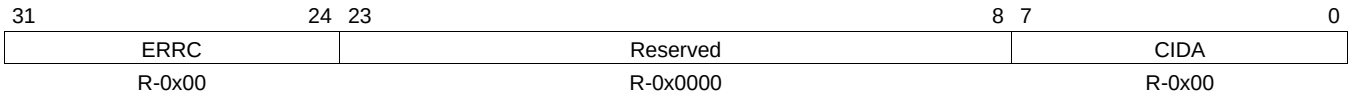
Table 63. CAT-2 Error Code Format Register Field Descriptions

Bit	Field Name	Value	Description
31 - 24	ERRC	0x00	Error code
23 - 16	Reserved	0x00	Reserved
15 - 8	CIDA	0x00	Active configuration ID
7 - 0	CIDF	0x00	Data buffer configuration ID

7.2.28 CAT-3 Error Code Format Register

The CAT-3 error code format register is shown in Figure 39 and described in Table 64.

Figure 39. CAT-3 Error Code Format Register



LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

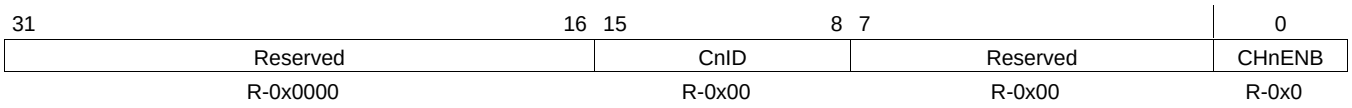
Table 64. CAT-3 Error Code Format Register Field Descriptions

Bit	Field Name	Value	Description
31 - 24	ERRC	0x00	Error code
23 - 8	Reserved	0x0000	Reserved
7 - 0	CIDA	0x00	Active configuration ID

7.2.29 Channel *n* Enable Register

The channel *n* enable register is shown in Figure 40 and described in Table 65.

Figure 40. Channel *n* Enable Register



LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 65. Channel *n* Enable Register Field Descriptions

Bit	Field Name	Value	Description
31 - 16	Reserved	0x0000	Reserved
16 - 8	CnID		Configuration Identification. Defines the configuration selection that takes effect on the next superframe synchronization event. The least significant bit determines whether the A or the B channel bitmap and configuration registers are used.
7 - 1	Reserved	0x00b	Reserved
0	CHnENB		Channel n enable.
		0	Channel n is disabled/stopped.
		1	Channel n is enabled/running.

7.2.30 Channel n Memory Address Register

The channel *n* memory address register is shown in Figure 41 and described in Table 66.

Figure 41. Channel n Memory Address Register

31	2	1	0
BADDR		00	
R/W-0x00000000		R-00b	

LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 66. Channel n Memory Address Register Field Descriptions

Bit	Field Name	Value	Description
31 - 0	BADDR	0x00000000	Memory Buffer Base Address. The two least significant bits are always forced to zero.

7.2.31 Channel *n* Frame Allocation Register

The channel *n* frame allocation register is shown in Figure 42 and described in Table 67.

Figure 42. Channel *n* Frame Allocation Register

31	12	11	2	1	0
Reserved		FALLOC		00	
R-0x00000		R/W-0x000		R-00b	

LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 67. Channel *n* Frame Allocation Register Field Descriptions

Bit	Field Name	Value	Description
31 - 12	Reserved	0x00000	Reserved
11 - 0	FALLOC		Frame buffer allocation. Each frame in the memory buffer begins on successive increments of FALLOC from BADDR. The two least significant bits are always forced to zero.

7.2.32 Channel *n* Frame Size Register

The channel *n* frame size register is shown in Figure 43 and described in Table 68.

Figure 43. Channel *n* Frame Size Register

31	12	11	2	1	0
Reserved		FSIZE		00	
R-0x00000		R/W-0x000		R-00b	

LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 68. Channel *n* Frame Size Register Field Descriptions

Bit	Field Name	Value	Description
31 - 12	Reserved	0x00000	Reserved
11 - 0	FSIZE		Frame size. Number of bytes to transfer for each frame. Applies only to transmit channels; ignored for receive channels. The two least significant bits are always forced to zero.

7.2.33 Channel *n* Frame Count Register

The channel *n* frame count register is shown in Figure 44 and described in Table 69.

Figure 44. Channel *n* Frame Count Register

31	8	7	0
Reserved		FCOUNT	
R-0x000000		R/W-0x00	

LEGEND: R/W = Read/Write; R = Read only; -*n* = Value after reset

Table 69. Channel *n* Frame Count Register Field Descriptions

Bit	Field Name	Value	Description
31 - 8	Reserved	0x000000	Reserved
7 - 0	FCOUNT		Frame Count. Number of frames in a buffer. Appropriate values are 1 through 255. Every FCOUNT frames the location of the frame in the memory buffer wraps back to BADDR.

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