Technical Article

Brief Comparison of DLPC84xx and DLPC6540 Chip Specifications

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This document was translated from a simplified Chinese source. (ZHCTA14)

The DLPC84xx, TI's latest family of DLP driver controllers, supports a range of DMD variants from .23 1080p to .39/.47 4K. The following sections compare the specifications of the DLPC84xx family with those of the previous-generation DLP 4K driver controller, the DLPC6540.

I. Comparison of Basic Parameters for DLPC84xx and DLPC6540

Table 1. Comparison of Key Parameters for DLPC84xx and DLPC6540

Parameter/ Characteristic	DLPC6540	DLPC84xx	DLPC84xx Notes
Resolution	Supports up to 4K UHD	Supports up to 4K UHD	
Max. source frame rate	4K @ 60Hz / 1080p @ 240Hz	4K @ 60Hz / 1080p @ 240Hz	
Source type	External video signal, internal test pattern, splash screen	External video signal, internal test pattern, splash screen	Both support custom internal test patterns
Video interface	Vx1	Vx1, FPD-Link	
Light source type	LED, RGB laser, laser phosphor color wheel (LPCW)	LED, RGB laser, laser phosphor color wheel (LPCW)	
Compatible DMD variants	DLP471TP	DLP472TP, DLP472NP, DLP39XTP, DLP230NP, DLP473TE, DLP473NE	The DLPC84xx supports more DMD variants
DMD interface type	High-speed serial interface (HSSI)	Sub-LVDS interface	Sub-LVDS interface consumes less power
Flash model	Parallel NOR Flash, supporting a second Flash for splash screen capture and image warping correction	SPI Serial Flash	The DLPC84xx supports a wider range of SPI Flash types
Auto-lock	Supported	Not supported	The front-end master chip configures the external source parameters of the DLPC84xx
Max. color cycle rate	4cc (typical) (up to 8cc)	Up to 20cc	A higher color cycle rate reduces color breakup, trailing, and other artifacts, but may introduce greater picture noise
Display latency	At least one frame	Less than 1ms	
Variable refresh rate (VRR)	Not supported	Supported	Compatible with FreeSync, G-SYNC standard
3D	Supports 3D mode with DMD native resolution	Supports 3D mode with DMD native resolution	GPIO_21 requires the 3D L/R reference to be connected

Similarities:

Both the DLPC84xx chip and the DLPC6540 system have a maximum resolution of 4K @60Hz or 1080p @240Hz. The display signal channel includes the internal test pattern generator (TPG) on the chip, splash

image, and external source input. Both chips support a variety of light source types, such as RGB LED, RGB Laser, and LPCW laser color wheel, as well as 3D display modes based on the physical resolution of the DMD.

Differences:

The DLPC6540 only supports the Vx1 input interface, while the DLPC84xx family has FPD-Link and DSI input interfaces in addition to the Vx1 interface (depending on the chip model and software version). The DLPC84xx supports VRR, ultra-low display latency (< 1ms), and a higher color cycle rate. The display latency of the DLPC6540 is approximately the duration of one frame. For example, an input signal at 60Hz features a latency of approximately 16.6ms. The DLPC84xx is capable of driving many more DMD variants, including the .23 1080p, .39 4K, .47 4K, and .47 SST DMDs. These two chips have different DMD interfaces. Specifically, the DLPC6540 supports the High-Speed Serial Interface (HSSI) for the DMD, while the DLPC84xx uses a Sub-LVDS interface for the DMD (the same as the DLPC343x family). The DLPC6540 uses an external parallel NOR Flash, while the DLPC84xx uses an SPI Flash. In addition, the DLPC6540 supports an Auto-lock feature for external sources, whereas the DLPC84xx requires the front-end signal to be configured before being output to the chip.

II. Comparison of Image Processing and Image Quality Specifications

Table 2. Image Processing and Image Quality Specifications of DLPC84xx versus DLPC6540

Parameter/ Characteristic	DLPC6540	DLPC84XX	DLPC84XX Notes
Overlap algorithm	Brilliant Color™ I & II	New overlap algorithm	The performance of the new overlap algorithm is slightly different from that of the previous BC algorithm
Overlap-supported colors	Yellow, Cyan, Magenta & White (spokes only)	Yellow, Cyan & Magenta	The DLPC84xx does not support white spokes of a laser phosphor color wheel, such as BY or YB spokes The DLPC84xx has lower spoke processing capability compared to the DLPC6540
Max. overlap percentage	30%	30%	
Max. overlap percentage per single color	20%	20%	
PWM performance	Excellent	Close to or slightly better than the DLPC6540	
Image quality	Excellent	Good	The following parameters can be improved individually, but the associated image quality factors must be considered together • Low-order image quality noise • White balance color point accuracy • System color coordinate calibration • Max. system brightness • Higher color cycle rate Image quality is related to factors including overlap color, percentage, and light source characteristics
DynamicBlack™	Supported	Supported	DB is supported in software versions since v2.3.0, and the DB Brightness Table must be calibrated
HDR10 (PQ)	Supported	Limited support	Color gamut mapping and HDR strength are not supported
HLG	Supported	Limited support	Relative RGB proportion adjustment, color gamut mapping, and HDR strength are not supported
Manual blending	Supported	Supported	

Both the DLPC84xx and DLPC6540 support the overlap mode (turning on two or more non-primary color light sources simultaneously to increase system brightness) with a maximum percentage of 30% for both and up to 20% overlap per single color. Both support image stitching, or manual blending. The DLPC84xx uses a new overlap algorithm, which offers fewer options for adjustment compared to the Brilliant Color used by the

DLPC6540. In addition, the DLPC84xx supports up to two-color Y/C/M overlap, while the DLPC6540 supports W (white) overlap in addition to Y/C/M. The DLPC84xx system software includes options for image dither noise, brightness priority, white balance adjustment, and color coordinate calibration, enabling its image quality to reach or closely approach that of the DLPC6540. In addition, the DLPC84xx simplifies the Dynamic Black feature, achieving a result close to the CAIC algorithm used in the DLPC343x system.

III. Comparison of Image Warping Compensation Algorithms

The warping algorithm refers to the adjustment of the geometric coordinates of the input signal pixels, which achieves the purpose of correcting image distortion. For example, when the projected screen or curtain is not a standard plane, when the projection orientation is not perpendicular to the screen, or when optical lens distortion causes the projected image to be distorted, the DLPC chip uses the warping function to set the image coordinate points, thereby correcting the displayed image into a regular rectangle shape, as shown in the figure below.

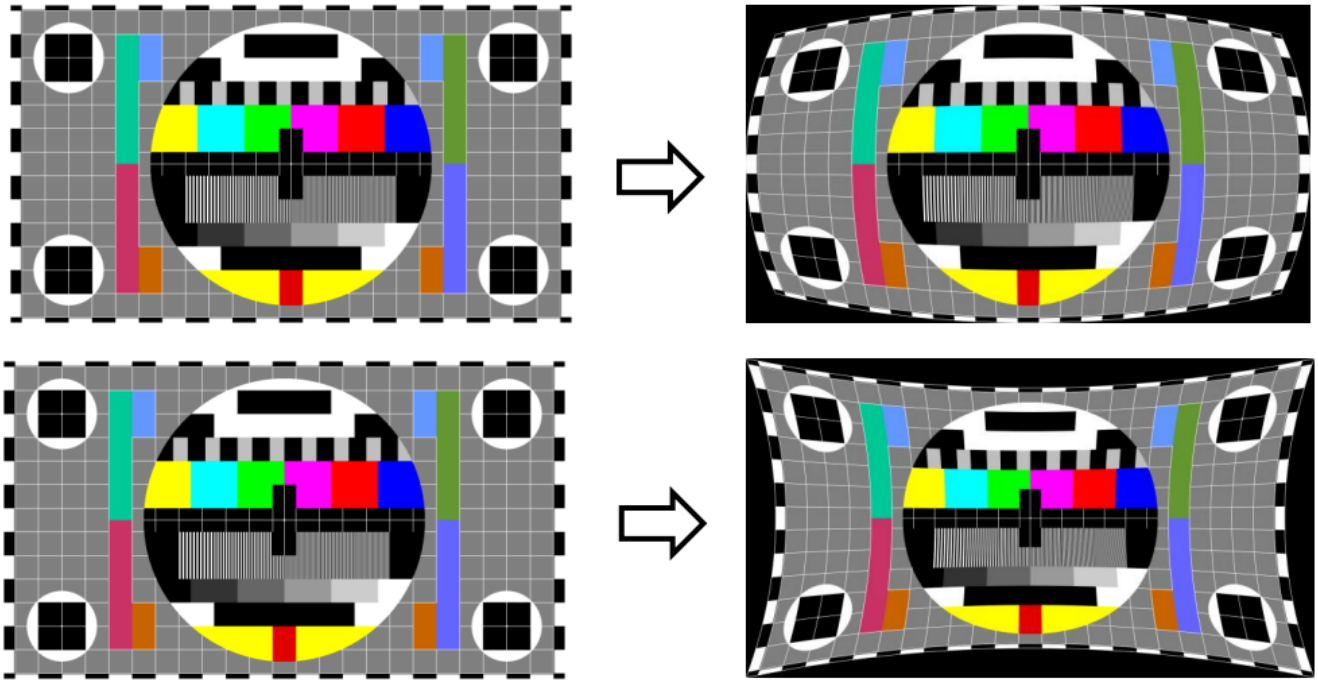
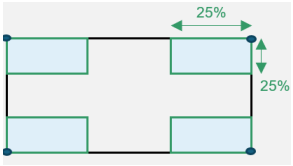


Figure 1. Diagram of Warping Correction

Table 3. Keystone Correction/Warping Correction Capabilities of DLPC84xx versus DLPC6540

Parameter	DLPC6540	DLPC84XX	DLPC84xx Notes
Warping hardware accelerator	Full-frame buffering achieves the max. warping correction resolution, but introduces an additional latency of two frames or more	The new algorithm adopts partial-frame buffering, thereby optimizing image display latency	The warping algorithm produces a display latency proportional to the number of lines buffered in the vertical direction. The DLPC84xx does not need to buffer a full frame. For small warping adjustments, the resulting display latency is very low
MxN manual warping	Up to 62x32 controllable points	Up to 32x18 controllable points	Fewer adjustable control points compared to the DLPC6540

Table 3. Keystone Correction/Warping Correction Capabilities of DLPC84xx versus DLPC6540 (continued)

Parameter	DLPC6540	DLPC84XX	DLPC84xx Notes
Four-corner keystone correction	The max. single-point adjustment range is 50% in the horizontal/ vertical direction	The max. single-point adjustment range is 25%. Refer to the figure below 	Even within the supported adjustment range, some extreme warping of geometric coordinates may cause display anomalies Adjustment coordinates that cannot be implemented are quantized to the nearest valid coordinates, and the original image aspect ratio is maintained It is recommended to set the coordinates of the four vertices simultaneously during four-corner keystone correction

To reduce image display latency, the DLPC84xx has an optimized internal buffering design, resulting in a slightly smaller number of controllable point grid elements and a narrower adjustment range for the warping function compared to the DLPC6540. The DLPC6540 uses a two-frame image buffering mode. Its advantage is a larger adjustment range for keystone/warping correction, but it introduces longer display latency. The DLPC6540 supports a maximum of 62x32 warping point-grid coordinate adjustments, while the DLPC84xx supports only 32x18. In addition, for four-corner keystone correction, the DLPC6540 can achieve a maximum single-point displacement of 50%, while the DLPC84xx supports a maximum of only 25% for the four-corner keystone adjustment. It is important to note that when simultaneously adjusting the coordinates of the four vertices, consider whether the adjustment ranges are appropriate for both the DLPC84xx and the DLPC6540. In some special cases, the DLPC chip may not be able to implement the set coordinates; the algorithm may choose the closest achievable position. Warping correction may degrade image quality or cause display artifacts within certain unsupported adjustment ranges.

Summary

Compared to the previous-generation DLP 4K driver chip, the DLPC84xx offers a smaller package size and lower power consumption, further reducing system BOM costs. It also supports display latency of less than 1ms and variable refresh rate (VRR). Based on a low-latency design architecture, the DLPC84xx family is not a simple upgrade of the DLPC6540, but a new design platform compatible with a wider range of DMD variants, capable of driving the majority of DMDs using a Sub-LVDS interface. When designing a DLP system, we should consider the weights of various parameters and metrics and choose the appropriate DLPC chip.

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Last updated 10/2025