CC35xx SimpleLink™ Wi-Fi 6 and Bluetooth® Low Energy Wireless MCU

Technical Reference Manual

Literature Number: SWRU626
DECEMBER 2025

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Chapter 1

Read This First

1.1 About This Manual

This document is organized into sections that correspond to each major feature; it explains the features and functionality of each module, and it also explains how to use them. For each feature, references are given to the documentation for the driver of the corresponding operating systems. This document does not contain performance characteristics of the device or modules, which are gathered in the corresponding device data sheets. This manual is intended for system software developers, hardware designers, and application developers.

1.2 Register, Field, and Bit Calls

The naming convention applied for a call consists of:

- For a register call: <Module Name>.<Register Name>; for example: UART.UASR
- For a bit field call:
  - <Module Name>.<Register Name>[End:Start]<Field name> field; for example, UART.UASR[4:0] SPEED bit field
  - <Field name>field<Module name>.<Register name>[End:Start]; for example, SPEED bit field UART.UASR[4:0]
- For a bit call:
  - <Module name>.<Register name>[pos]<Bit name> bit; for example, UART.UASR[5] BIT_BY_CHAR bit
  - <Bit name>bit<Module name>.<Register name>[pos]; for example, BIT_BY_CHAR bit UART.UASR[5]

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Chapter 2

Architecture Overview

The CC35xx SimpleLink™ Wi-Fi 6 and Bluetooth® Low Energy wireless MCUs provide solutions for a wide range of applications. To help the user develop these applications, this technical reference manual (TRM) focuses on the use of the different building blocks of the devices. For detailed device descriptions, complete feature lists, and electrical specifications, see the datasheet for the specific device. The following subsections provide easy access to relevant information and guide the reader to the different chapters in this document. This document should be read in conjuction with the CC35xx Software Development Kit documents which explain the TI software interface and API's which control the hardware describes in this TRM.

The CC35xx SimpleLink™ Wi-Fi 6 and Bluetooth® Low Energy wireless MCUs are ideal for use in cost-sensitive embedded applications with RTOS software. CC35xx brings the efficiency of Wi-Fi 6 to embedded device applications for the internet of things (IoT), with a small PCB footprint and highly optimized bill of materials. The combination of an Arm® Cortex®-M33 processing core at 160 MHz, RF core running WLAN/BLE, and a wide selection of peripherals makes the CC35xx specifically designed for single-chip implementation.

2.1 Target Applications

- Building Automation
  - Thermostat
  - HVAC motor control
  - Wireless security camera
  - Video Doorbell
  - Garage door system
- Appliances
  - Refrigerator & freezer
  - Oven
  - Washer & dryer
  - Residential water heater
  - Air conditioner indoor unit
  - Coffee machine
  - Vacuum robot
  - Robotic lawn mower
- Grid Infrastructure
  - Electricity meter
  - String Inverter
  - Micro Inverter
  - Battery energy storage systems
  - EV charging infrastructure
- Medical
  - Infusion pump
  - Electronic hospital bed & bed control
  - Multiparameter patient monitor
  - CPAP machine
  - Telehealth systems
  - Ultrasound scanner
  - Ultrasound smart probe
  - Electric toothbrush
- Retail Automation & Payment
- Connected Peripherals & Printers
- Factory Automation & Control
- Asset Tracking

2.2 Introduction

Figure 2-1 shows the building blocks of the CC35xx platform. The following sections provide an overview of the features of the CC35xx.

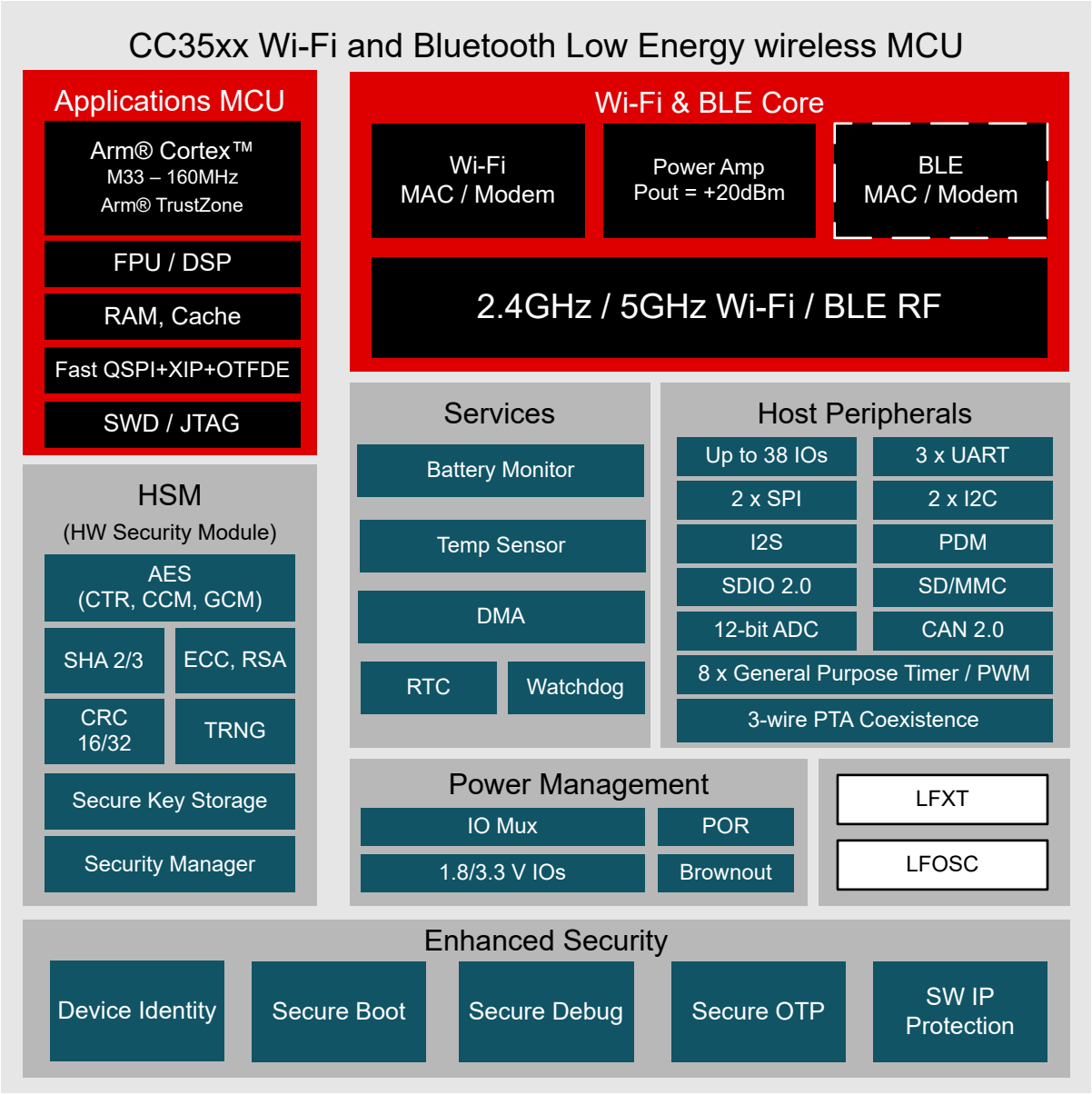

Figure 2-1. CC35xx Block Diagram

CC35xx devices have the following features:

- Arm Cortex-M33 processor core
  - Arm Cortex SysTick timer
  - Nested Vectored Interrupt Controller (NVIC)
  - Trustzone™
  - AI instruction extensions (TINIECDE)
- On chip memories

  - Low latency TCM and Cache for code excecution
  - Low latency TCM for data
  - over 1MB SRAM for application data
  - Support for additional external PSRAM
- Clocks
  - 160MHz processor core
  - 52MHz XTAL fast clock
  - Internal low-frequency oscillator, 32.768 kHz XTAL, or external slow clock options
- External memory interface
  - High speed Quad-SPI/Octal-SPI for XiP flash interface
  - Optional to add additional in-package PSRAM
  - µDMA
- Power management
  - 1.8V V_{MAIN} supply
  - 3.3V V_{PA} supply
  - Support for 3.3V or 1.8V V_{IO}'s
- System Services
  - Direct memory access (DMA)
  - One-time-programmable memory (OTP)
  - Real-time clock (RTC)
  - Watchdog timer (WDT)
  - System timer
- Peripherals
  - Up to 38 I/O's with flexible multiplexing options
  - 8 x General-Purpose Timers / Pulse-Width Modulation (PWM)
  - 3 x Universal Asynchronous Receiver-Transmitter (UART)
  - 2 x Serial Peripheral Interface (SPI)
  - 2 x Inter-Integrated Circuit (I2C)
  - Inter-IC Sound (I2S)
  - Pulse Density Modulation (PDM)
  - Secure Digital / Multimedia Card (SD/MMC)
  - Secure Digital Input Output (SDIO) 2.0
  - Controller Area Network (CAN) 2.0
  - 8 channel, 12-bit Analog to Digital Converter (ADC)
- WLAN Radio
  - Wi-Fi 6 (802.11ax)
  - Single-stream 20-MHz channels with application throughput up to 20Mbps (UDP)
  - Compatible with IEEE 802.11 b/g/a/n/ax
  - Orthogonal Frequency-Division Multiple Access (OFDMA)
  - Target Wake Time (TWT)
  - Trigger Frames Basic Service Set (BSS)
  - Color Integrated PA for complete WLAN Solution with up to 20.5dBm output power at 1DSSS
  - Role support: STA, softAP, Wi-Fi Direct, Multi-role AP + STA
  - Support for Personal and Enterprise Wi-Fi Security: WPA / WPA2 PSK, WPA2 Enterprise, WPA3 Personal or Enterprise
  - Wi-Fi TX Power:
    - 20.5dBm at 1DSSS
    - 17.8dBm at 54OFDM
  - Wi-Fi RX Sensitivity:
    - 98.7dBm at 1DSSS
    - 76.6dBm at 54OFDM
- Bluetooth low energy
  - Bluetooth low energy 5.4 certified stack

  - Supports long-range and high-speed PHYs (up to 2 Mbps)
- Security Features
  - ARM TrustZone
  - Hardware Security Module supporting all of the following:
    - ECC, RSA, AES, SHA2/3, MD5, CRC 16/32, and TRNG
    - Secure key storage
  - Initial Secure Programming
  - Secure Boot
  - Software IP and Cloning Protection
  - Debug security through JTAG and Debug port lock
  - OTP with ability to program root-of-trust public key
  - Secure Over-the-Air (OTA) updates
  - Anti-rollback protection
- SWD debug interface
- Complete Software Development Kit with opensource TCP/IP and TLS stacks
- Operating temperature: -40°C to +105°C
- Support for 3-wire PTA coexistence interface for use with external 2.4GHz radios (for example Thread or Zigbee®)
- Antenna selection capability
- Package
  - Easy to design with 56 pin, 7-mm x 7-mm quad flat noleaded (QFN) package

TI offers a complete support package to assist in getting to market quickly, with evaluation and development boards, white papers and application notes, an easy-to-use peripheral driver library, a Software Development Kit (SDK) with qualified wireless protocols, and a strong support, sales, and distributor network.

2.3 Internal System Diagram

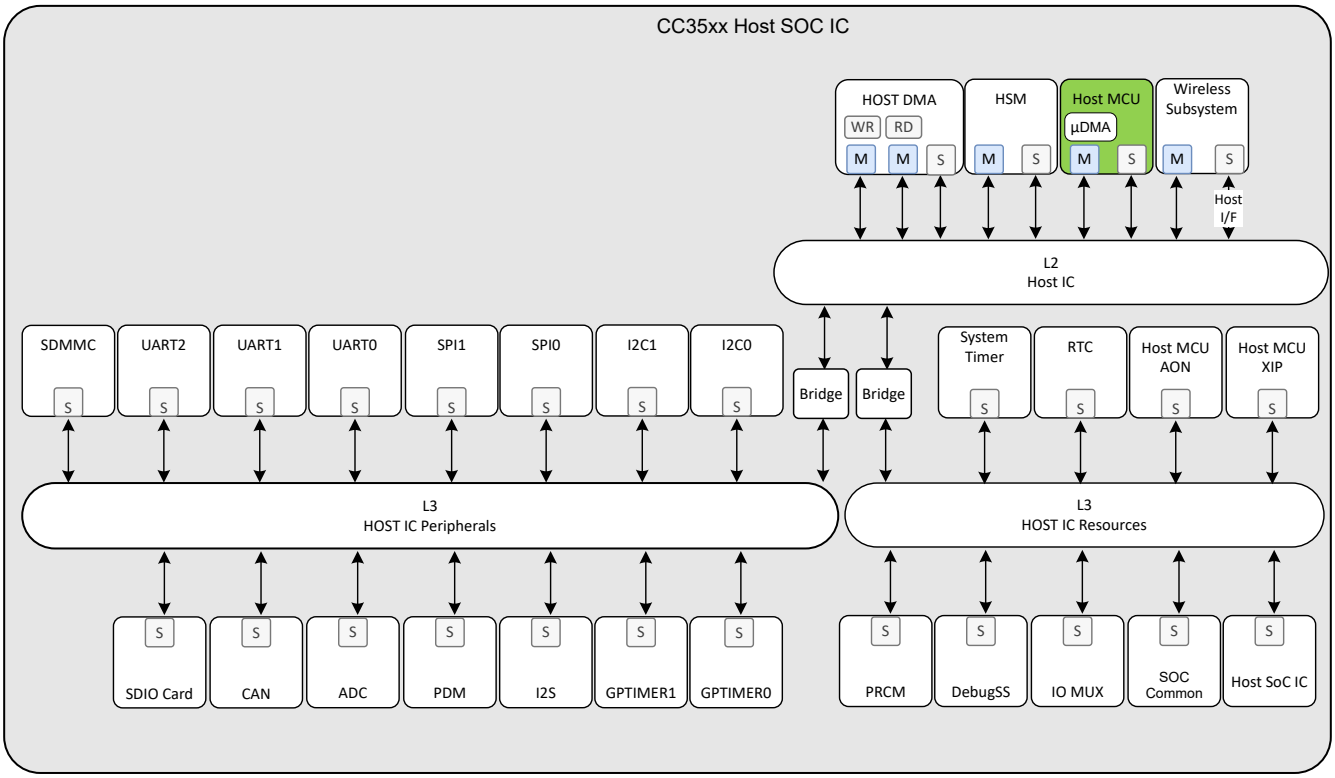

Figure 2-2. CC35xx Internal System Diagram

The image above describes the basic connections between the Internal modules of the CC35xx.

The Interconnect between these modules is called the SOC IC.

Interconnect description:

- Host Interconnect Layer 2 (L2): targets(S) can be access simultaneously by different initiators (M)
- Interconnect Layer 3 (L3): targets(S) can be access one at a time. No simultaneous access is supported.

The device Host interconnect is comprised of 6 Initiators (M), 4 targets (S) on Layer 2, and 2 bridges connect it to layer 3. These bridges connect it L2 to L3 targets: Host IC Peripherals and Host IC Resources.

Address Map and range for each target can be found in Section 4.1.

2.4 Arm Cortex M33

The following subsections provide an overview of the Arm Cortex M33 , the integrated system timer (SysTick), and the NVIC.

2.4.1 Processor Core

The CC35xx device is designed around an Arm Cortex M33 processor core.

Features of the processor core are as follows:

- Armv8-M architecture with mainline extension.
- Thumb/Thumb-2 subset instruction support.
- 3-stage pipeline.
- Software security:
  - TrustZoneTM for Armv8-M, with Security Attribution Unit of up to 8 regions.
  - Stack limit boundaries and checking.
- DSP extension: including all the V8.1-M DSP/SIMD instructions.
- Floating Point Unit (FPU): single precision floating point unit, IEEE 754 compliant.
- Memory Protection Unit (MPU) with 8 regions for secure state (MPU_S) and 8 regions for non-secure state(MPU_NS).
- 24-bit SysTick timer for each security domain.
- Integrated Nested Vectored Interrupt Controller (NVIC) supporting Non-maskable Interrupt (NMI).
- Low power sleep modes
  - ARM SLEEP maps to device idle power mode.
  - ARM DEEPSLEEP maps to device standby power mode.
- Serial Wire Debug ports with up to 8 breakpoints and 4 watchpoints.
- Data Trace (DWT), and Instrumentation Trace (ITM).
- 160 MHz operation with 1.41DMIPS/MHz and 3.85 CoreMark/MHz (running CoreMark from flash)performance.
- TINIECDE instruction extensions for Neural Network processing.

2.4.2 SysTick Timer

The Arm Cortex M33 processor includes an integrated Sytick Timer. SysTick provides a simple, 24-bit, clearon-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in several different ways, for example:

- A variable rate alarm or signal timer—the duration is range-dependent on the reference clock used and the dynamic range of the counter
- A simple counter used to measure time to completion and time used
- An internal clock-source control based on missing or meeting durations

2.4.3 Nested Vectored Interrupt Controller

The CC35xx device controller includes the Arm NVIC. The NVIC and Arm Cortex M33 prioritize and handle all exceptions in handler mode. The processor state is automatically stored to the stack on an exception

and automatically restored from the stack at the end of the interrupt service routine (ISR). The processor supports tail-chaining, that is, back-to-back interrupts can be performed without the overhead of state saving and restoration. Software can set priority/preemption grouping in eight levels on internal CPU exceptions and interrupts.

Features of the NVIC include:

- Deterministic, fast interrupt processing
- External non-maskable interrupt (NMI) signal available for immediate execution of NMI handler
- Dynamically reprioritizable interrupts
- Exceptional interrupt handling through hardware implementation of required register manipulations
- TrustZone TM security attribuition

2.4.4 System Control Block (SCB)

The system control block (SCB) provides system implementation information and system control (configuration, control, and reporting of system exceptions).

2.4.5 TI AI instruction extensions

The M33 core has extended neural net instructions to support TINIE.

2.5 Power Management

There are multiple voltage levels in use on the device to effectively optimize the power consumption of various modules operating in different power modes.

The external power supplies are as follows:

- V_{Main}, V_{PP}: 1.8V
- VIO_1, VIO_2, VDDSF : 1.8V/ 3.3V
- V_{PA}: 3.3V

2.5.1 VDD_MAIN

The main supply of the device generating the digital and memories supplies

2.5.2 VDD_IO

This VDDIO supply powers for the split rails IO supply for device GPIOs (VIO1, VIO2). VDDIO split rail I/O supply enables using a different I/O supply rail compared to the main VDDMAIN supply rail. This enables applications to interface with other system components at a different voltage level compared to the main VDDMAIN power supply level.

2.5.3 VDDSF

The VDDSF supply powers the IO supply for external Flash GPIOs only.VDDSF split rail I/O supply (independent from VIO1 + VIO2) enables using a different I/O supply rail compared to the main VDDMAIN supply rail.This enables applications to interface with external Flash at a different voltage level compared tothe main VDDMAIN power supply level.

2.5.4 VDD_PA

The input supply to the Power Amplifier of the device.

2.6 Debug Subsystem (DEBUGSS)

The debug subsystem (DEBUGSS) interfaces the serial wire debug (SWD) two-wire physical interface to multiple debug functions within the device. Debugging of processor execution and the device state are supported. The DEBUGSS also provides a mailbox system for communicating with software through SWD.

2.7 Memory Subsystem (MEMSS)

The CC35xx device supports on-chip and off-chip memories. The memories are used for execution, data and non volatile memory. The on-chip memory includes SRAM and the off-chip memories supported are serial Flash (connected externally or stacked inside device package) and optional serial PSRAM (stacked inside device package).

The SRAM is used for execution and data. It is divided into instruction and data partitions, as well as secure and non-secure. The instruction memory partition is split into Instruction Tightly Coupled Memory (ITCM) and Instruction Cache memory (I-Cache). I-Cache allows for execution from Flash and the PSRAM. Data memory is divided into Data Tightly Coupled Memory (DTCM), Data non-Tightly Coupled Memory (DMEM), and Data Cache Memory (D-Cache). The D-Cache is designed to access the PSRAM.

Each of the memories can be accessed by the M33 MCU, Host DMA and the µDMA. The host DMA is used for data transfer between peripherals and the device on-chip SRAM. The µDMA is used for data transfer between the external Flash/PSRAM and on-chip SRAM.

2.7.1 External Memory Interface

The device supports external Flash/PSRAM interface (XIP) and support the following features:

- High speed Quad/ Octal xSPI interface
- Encrypt/Decrypt external memory data
- Logical to physical address translator
- Secured/Non-Secured partitioning

2.8 Hardware Security Module

The CC35xx devices have an integrated hardware security module (HSM) which act as an on-chip secure element. The HSM supports an isolated environmentfor cryptographic, key management, secure counters, and random number generation operations. Selected algorithms are protected from differential power analysis (DPA) side channel attacks. Together with a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), the system supports secure and future proof IoT applications to be easily built on the platform.

2.9 General Purpose Timers (GPT)

The General Purpose Timer (GPT) is used to count or time external or internal events, generate Pulse-Width Modulation (PWM) signals, and generate IR modulated codes. There are two general purpose timers available, each with 4 channels. See the device specific data sheet for available timers and features.

2.10 Real Time Clock (RTC)

The RTC can be used to wake the CC35xx device from any state where the RTC is active. The RTC contains one capture and one compare channel. With software support, the RTC can be used for clock and calendar operation. The RTC is clocked from the 32 kHz RC oscillator or the 32 kHz crystal oscillator. The RTC has a recovery mechanism to keep the clock through software initiated resets.

2.11 Direct Memory Access

The CC35xx includes a direct memory access (DMA) controller, known as Host DMA. The Host DMA controller provides a way to offload data transfer tasks from the Arm® Cortex®-M33 processor, allowing for more efficient use of the processor and the available bus bandwidth. The Host DMA controller can perform transfers between on-chip memory (SRAM) and peripherals. The Host DMA includes multiple channels and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data.

2.12 GPIOs

I/O pins offer flexibility for a variety of connections. The CC35xx device supports configurable I/O pins (GPIOx) that can be multiplexed to digital and analog peripherals through the I/O Mux. For information on what pins can be multiplexed to what peripherals see the device specific data sheet.

- Each pin can be mapped to a specific set of peripherals with wide variety in the pinmux
- GPIOn (GPIO0 to GPIO37) are the logical names of the different I/O pins on the specific package, see the device specific data sheet for more information on package pin designation
- 8 of these GPIOs also have analog capabilities
- Pins can also be mapped to the digital test bus (DTB) to bring out clocks or physical signals like interrupts

2.13 Communication Peripherals

The CC35xx device platform supports both asynchronous and synchronous communication including:

- UART module
- I2C module
- SPI module
- I2S module
- PDM module
- SD/MMC module
- SDIO module
- CAN module
- ADC module

The following subsections provide more detail on each of the communication modules.

2.13.1 UART

UART is an integrated circuit used for TTL serial communications. A UART contains a transmitter (parallel-toserial converter) and a receiver (serial-to-parallel converter). The CC35xx device includes 3 fully programmable UART modules. The UART can generate individually masked interrupts from the receive (RX), transmit (TX), modem flow control, and error conditions. The module generates one combined interrupt when any of the interrupts are asserted and are unmasked.

2.13.2 I^2C

The I2C bus provides bidirectional data transfer through a 2-wire design, a serial data line (SDA) and a serial clock line (SCL), and interfaces to external I2C devices such as serial memory (RAM and ROM), networking devices, LCDs, tone generators, and so on. The I2C bus can also be used for system testing and diagnostic purposes in product development and manufacture.

2.13.3 SPI

The SPI module is a 3-wire or 4-wire bidirectional communication interface that converts data between parallel and serial formats. The SPI performs serial-to-parallel conversion on data received from a target device and performs parallel-to-serial conversion on data transmitted to a target device.

The SPI can be configured as either a controller or peripheral device. As a peripheral device, the SPI can be configured to disable the SPI output, which allows coupling of a controller device with multiple peripheral devices. The TX and RX paths are buffered with separate internal FIFOs. The SPI also includes a programmable bit rate clock divider and prescaler to generate the output serial clock derived from the input clock of the SPI. Bit rates are generated based on the input clock, see the device specific data sheet for maximum bit rates.

2.13.4 I^2S

The I2S interface is used to handle digital audio and can also be used to interface pulse-density modulation microphones (PDM).

2.13.5 SDMMC

The CC35xx contains a Secure Digital Multimedia Card (SDMMC) module which provides interface to an SD memory card.

2.13.6 SDIO

The CC35xx contains a Secure Digital Input/Output (SDIO) peripheral used for interfacing to an external SDIO host.

2.13.7 CAN

The CC35xx has a Controller Area Network (CAN) module, which conforms with CAN protocol 2.0 A/B.

2.13.8 ADC

The purpose of the ADC is to measure analog signals and convert them to a digital representation with minimal CPU intervention providing for lower power and greater task integration. The ADC supports fast 12-, 10-, and 8-bit analog-to-digital conversions. The ADC implements a 12-bit Successive Approximation Register (SAR) core, sample/conversion mode control, and up to 6 independent conversion-and-control buffers. This means the ADC allows up to 6 independent analog-to-digital converter (ADC) samples to be converted and stored without any CPU intervention.

Chapter 3

Arm® Cortex®-M33 Processor

The Arm Cortex-M33 core brings high-performance 32- bit computing to cost-sensitive embedded microcontroller applications, such as factory automation and control, industrial control power devices, building and home automation.

This chapter provides information on the Arm Cortex-M33 processor.

3.1 Arm Cortex-M33 Processor Introduction

The Cortex-M33 processor is a high performance, low gate count, highly configurable, and energy efficient processor. It is intended for microcontroller and embedded applications that require an efficient mix of control capability and signal processing instructions. The processor is based on the Armv8-M architecture and is primarily for use in environments where security is an important consideration.

The following features are included:

- 160 MHz Operation
- Arm TrustZone® technology, using the Armv8-M Security Extension supporting Secure and Nonsecure states
- The Floating-point Extension (FPU)
- The Digital Signal Processing (DSP) Extension
- Enhanced system debug with up to 4 watchpoints and 8 breakpoints
- The Memory Protection Unit Extension (MPU)
- Programmable Security Attribution Unit (SAU)
- Micro Trace Buffer (MTB)
- Wakeup interrupt controller (WIC)
- Arm Custom Instructions (ACI)
- The Instruction Trace Macrocell Extension (ITM)
- A Nested Vectored Interrupt Controller (NVIC) that is closely integrated with the processor
- A low-cost debug solution with the ability to implement breakpoints, watchpoints, tracing
- Passing on-chip data through a Trace Port Interface Unit (TPIU) to a Trace Port Analyzer (TPA) using Serial Wire Output (SWO) mode
- A ROM table to allow debuggers to determine which components are implemented in the Cortex-M33 processor
- In-order pipeline processor
- Incorporates the Thumb-2 technology
- Data accesses in little endian
- Harvard architecture characterized by separate buses for instruction and data
- Saturating arithmetic and dedicated hardware division
- Standard trace support
  - ITM
  - TPIU with asynchronous serial wire output (SWO)
  - Full debug with data matching for watchpoint generation
  - DWT
  - SWD (Serial Wire Debug) port

3.2 Block Diagram

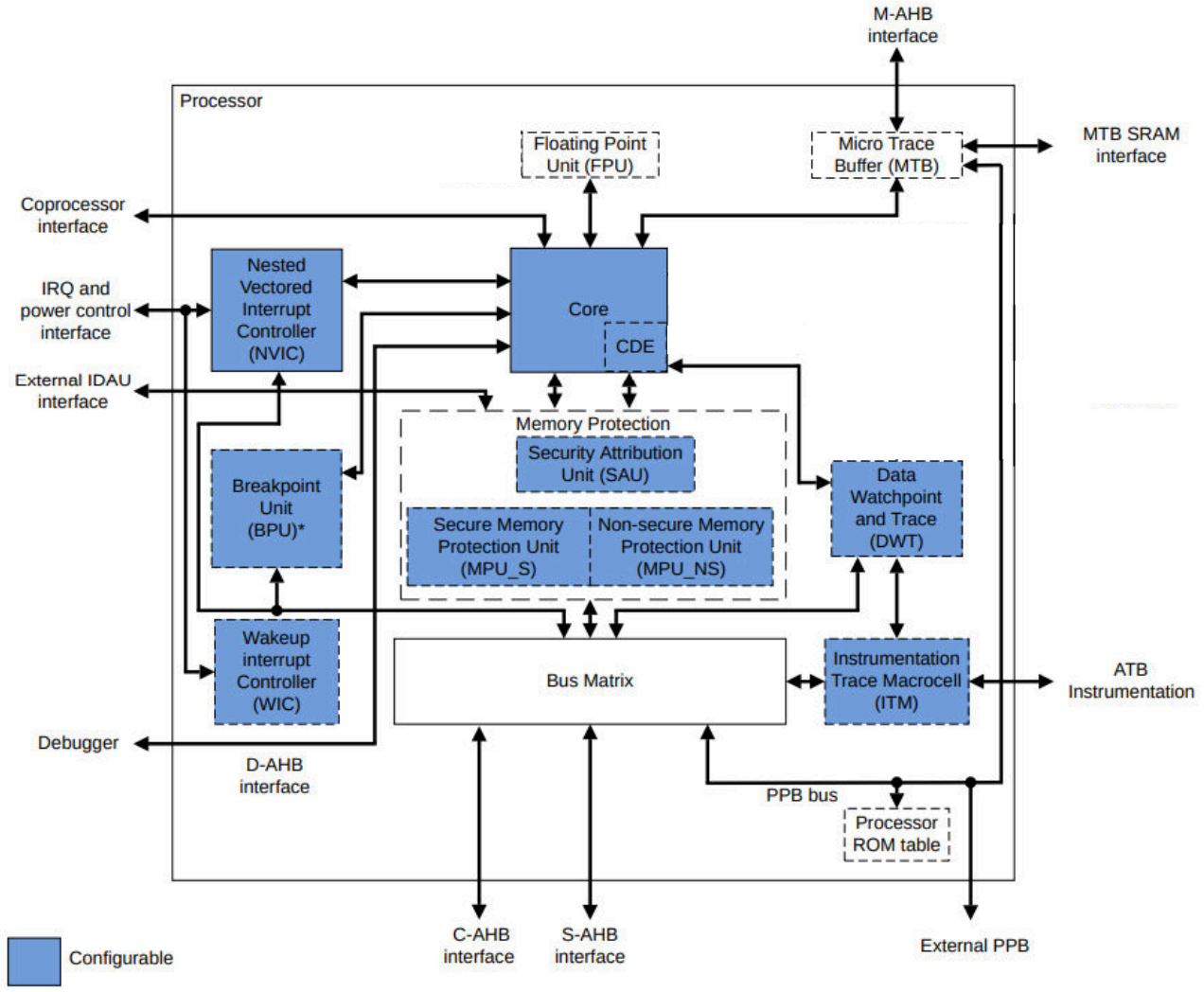

Figure 3-1. Cortex-M33 Block Diagram

3.3 M33 instantiation parameters

M33 instantiation parameters are as follows:

Parameter	Value
FPU	1
DSP	1
SECEXT	1
CPIF	0
MPU_NS	8
MPU_S	8

Parameter	Value
SAU	8
IRQLVL	4
NUMIRQ	49
IRQLATENCY	{{445{1'b0}}, {35{1'b1}}}
DBGLVL	2
ITM	1
ETM	0
MTB	1
WIC	1
CTI	0
RAR	1
SBIST	0
CDERTLID	16
CDEMAPPEDONCP0	1
CDEMAPPEDONCP1	0
CDEMAPPEDONCP2	0
CDEMAPPEDONCP3	0
CDEMAPPEDONCP4	0
CDEMAPPEDONCP5	0
CDEMAPPEDONCP6	0
CDEMAPPEDONCP7	0

Other important paramters of CPUSS:

Parameter	Value
JEPID	7'b0010111
JEPCONT	4'b0000
PARTNUM	12'h000
MCU ROM table address	32'hE00FE000
Processor ROM Table address	32'hE00FF000
TPIU Base address	32'hE0040000
VTOR address (Both secure and non-secure)	25'h01E0000

3.4 Arm Cortex-M33 System Peripheral Details

The Arm Cortex-M33 includes the following system components:

3.4.1 Floating Point Unit (FPU)

The Cortex-M33 FPU is an implementation of the single precision variant of the Armv8-M Floating point extension, FPv5 architecture. It provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard. The FPU supports all single-precision data-processing instructions and data types described in the Arm®v8-M Architecture Reference Manual.

3.4.2 Memory Protection Unit (MPU)

The MPU improves system reliability by defining the memory attributes for different memory regions. There can be two MPUs, one Secure and one Non-secure. Each MPU can define memory attributes independently. There are 8 secure and 8 non-secure memory regions.

3.4.3 Digital Signal Processing (DSP)

The DSP adds support for SIMD instructions.

3.4.4 Security Attribution Unit (SAU)

It is a hardware inside the processor which allow Secure software to define Non-secure and Non-Secure Callable (NSC) regions. Regions that are not mapped to any SAU regions are Secure by default. The results from SAU and Implementation Defined Attribution Unit (IDAU) are compared, and higher security attribute is selected. For example, if SAU indicates a memory location is Secure and IDAU indicate the same address as Non-secure, the processor treats it as Secure. The order of security levels from low to high is Non-secure < N-Secure Callable < Secure.

3.4.5 System Timer

The processor has two 24-bit system timers, a Non-secure SysTick timer and a Secure SysTick timer. When enabled, each timer counts down from the reload value to zero, reloads (wraps to) the value in the SYST_RVR on the next clock cycle, then decrements on subsequent clock cycles. When the processor is halted for debugging, the counter does not decrement.

3.4.6 Nested Vectored Interrupt Controller

An embedded interrupt controller (INTC) that supports low-latency interrupt processing. A programmable priority level of 0-255. A higher level corresponds to a lower priority, so level 0 is the highest interrupt priority. There is also an external non-maskable interrupt. For more information see Section 5.1.4.

3.4.7 System Control Block

It is an address region in the System Control Space. The System Control Block (SCB) provides system implementation information and system control that includes configuration, control, and reporting of system exceptions.

3.4.8 System Control Space

The System Control Space (SCS) is the programmer's model interface to the processor. It provides system implementation information and system control. The processor provides debug through registers in the SCS.

3.5 CPU Sub-System Peripheral Details

The CPU Sub System (CPUSS) has the following peripherals:

1. ARM Cortex M33
2. Trace Port Interface Unit (TPIU)
3. DAP Bridge and Debug Authentication
4. Implementation Defined Attribution Unit (IDAU)
5. Custom Datapath Extension (CDE) instructions

3.5.1 Trace Port Interface Unit (TPIU)

The Trace Port Interface Unit (TPIU) drives trace data to external pins on a target, so that the Trace Port Analyzer (TPA), which is often part of a debug unit, can capture the trace data.

The TPIU:

- Coordinates the stopping of trace capture when it receives a trigger
- Inserts source identification information into the trace stream so that trace data can be re-associated with its trace source
- Outputs the trace data over trace port pins

- Outputs patterns over the trace port. This pattern output is often referred to as TPIU pattern generation. This allows a TPA to tune its capture logic to the trace port, which maximizes the trace data output frequency on the trace port.

TPIU implementation details are found in the Arm CoreSight System-on-Chip SoC-600 Technical Reference Manual.

3.5.2 DAP Bridge and Debug Authentication

The DAP bridge serves as a connection between Serial Wire (SW) Debug Port and AHB-AP Access Port. There are 4 debug authentication control signals driven from DEBUGSS to CPUSS:

1. DBGEN (Invasive debug enable)
2. NIDEN (Non-Invasive debug enable)
3. SPNIDEN (Secure Peripheral Non-Invasive Debug Enable)
4. SPIDEN (Secure Peripheral Invasive Debug Enable)

- SPNIDEN and SPIDEN can be overwritten by CPUSS by writing to the DAUTHCTRL MMR of M33.
- For invasive debug enable, DBGEN must be set. For non-invasive debug enable, NIDEN must be set.
- For TPIU to function, NIDEN must be set. Only single wire trace is enabled for TPIU. 4 wire trace is not supported.

Table 3-1. Invasive Debug Access Control

DBGEN	SPIDEN	Invasive Debug Status	Invasive debug permitted states
LOW	X	DISABLED	None
HIGH	LOW	ENABLED	All None Secure States
HIGH	HIGH	ENABLED	All States

Table 3-2. Non Invasive Debug Access Control

NIDEN	SPNIDEN	States in which non-invasive debug is permitted
LOW	X	None
HIGH	LOW	All Non Secure States
HIGH	HIGH	All States

3.5.3 Implementation Defined Attribution Unit (IDAU)

IDAU along with SAU determines the security attribution of the M33 core. IDAU have been configured such that if address bit [26] is 0, the address is a Non-Secure callable region. This region cannot be downgraded to a non-secure region but can be upgraded to a secure region using SAU.

The IDAU region ID for the entire Memory Map is mentioned below:

Address [31:0]	IDAU Region	Region Type
32'h0000_0000 - 32'h03FF_FFFF	0	Non-secure
32'h0400_0000 - 32'h07FF_FFFF	1	Non-secure callable
32'h0800_0000 - 32'h0BFF_FFFF	2	Non-secure
32'h0C00_0000 - 32'h0FFF_FFFF	3	Non-secure callable
32'h1000_0000 - 32'h13FF_FFFF	4	Non-secure
32'h1400_0000 - 32'h17FF_FFFF	5	Non-secure callable
32'h2000_0000 - 32'h23FF_FFFF	8	Non-secure
32'h2400_0000 - 32'h27FF_FFFF	9	Non-secure callable
32'h2800_0000 - 32'h2BFF_FFFF	10	Non-secure
32'h2C00_0000 - 32'h2FFF_FFFF	11	Non-secure callable
32'h4000_0000 - 32'h43FF_FFFF	16	Non-secure
32'h4400_0000 - 32'h47FF_FFFF	17	Secure

Address [31:0]	IDAU Region	Region Type
32'h6000_0000 - 32'h63FF_FFFF	24	Non-secure
32'h6400_0000 - 32'h67FF_FFFF	25	Secure
32'hA000_0000 - 32'hA3FF_FFFF	40	Non-secure
32'hA400_0000 - 32'A7FFF_FFFF	41	Non-secure callable
32'hE000_0000 - 32'hE00F_FFFF	-	-

3.6 Programming Model

The Cortex-M33 programmer's model is an implementation of the Armv8-M Main Extension architecture. For a complete description of the programmer's model, refer to the Arm®v8-M Architecture Reference Manual, which also contains the Armv8-M Thumb® instructions.

3.6.1 Modes of operation and execution

The Cortex-M33 processor supports Secure and Non-secure security states, Thread and Handler operating modes, and can run in either Thumb or Debug operating states. In addition, the processor can limit or exclude access to some resources by executing code in privileged or unprivileged mode. See the Arm®v8-M Architecture Reference Manual for more information about the modes of operation and execution.

3.6.1.1 Security states

When the Armv8-M Security Extension is included in the processor, the programmers model includes two orthogonal security states, Secure state and Non-secure state. The CC35xx M33 Security Extension is implemented dy default, hence the processor always resets into Secure state. Each security state includes a set of independent operating modes and supports both privileged and unprivileged user access. Registers in the System Control Space are banked across Secure and Non-secure state, with the Non-secure register view available at an aliased address to Secure state.

3.6.1.2 Operating modes

For each security state, the processor can operate in Thread or Handler mode. The conditions which cause the processor to enter Thread or Handler mode are as follows:

- The processor enters Thread mode on reset, or as a result of an exception return to Thread mode. Privileged and Unprivileged code can run in Thread mode.
- The processor enters Handler mode as a result of an exception. All code is privileged in Handler mode.

The processor can change security state on taking an exception, for example when a Secure exception is taken from Non-secure state, the Thread mode enters the Secure state Handler mode. The processor can also call Secure functions from Non-secure state and Non-secure functions from Secure state. The Security Extension includes requirements for these calls to prevent secure data from being accessed in Non-secure state.

3.6.1.3 Operating states

The processor can operate in Thumb or Debug state:

- Thumb state is the state of normal execution running 16-bit and 32-bit halfword-aligned Thumb instructions.
- Debug state is the state when the processor is in Halting debug.

3.6.1.4 Privileged access and unprivileged user access

Code can execute as privileged or unprivileged. Unprivileged execution limits or excludes access to some resources appropriate to the current security state. Privileged execution has access to all resources available to the security state. Handler mode is always privileged. Thread mode can be privileged or unprivileged.

3.6.2 Instruction set summary

The processor implements the following instruction from Armv8-M:

- All base instructions.
- All instructions in the Main Extension.
- All instructions in the Security Extension.

- All instructions in the DSP Extension.
- All single-precision instructions and double precision load and store instructions in the Floating-point Extension.

For more information about Armv8-M instructions, see the Arm ®v8-M Architecture Reference Manual.

3.6.3 Memory model

The processor contains a bus matrix that arbitrates instruction fetches and memory accesses from the processor core between the external memory system and the internal *System Control Space* (SCS) and debug components. Priority is usually given to the processor to ensure that any debug accesses are as non-intrusive as possible. The system memory map is Armv8-M Main Extension compliant, and is common both to the debugger and processor accesses. The default memory map provides user and privileged access to all regions except for the *Private Peripheral Bus* (PPB). The PPB space is privileged access only.

The following table shows the default memory map.

Address Range	Region	Interface
0x00000000-0x1FFFFFFF	Code	Instruction and data accesses performed on C-AHB.
0x20000000-0x3FFFFFFF	SRAM	Instruction and data accesses performed on S-AHB. Any attempt to execute instructions from the peripheral and external device region results in a MemManage fault.
0x40000000-0x4FFFFFFF	Peripheral	
0x60000000-0x9FFFFFFF	External RAM	
0xA0000000-0xDFFFFFFF	External Device	
0xE0000000-0xE00FFFFF	PPB	Reserved for system control and debug. Cannot be used for exception vector tables. Data accesses are either performed internally or on EPPB. Accesses in the range: 0xE0000000-0xE0043FFF Are handled within the processor. 0xE0044000-0xE00FFFFF Appear as APB transactions on the EPPB interface of the processor. Any attempt to execute instructions from the region results in a MemManage fault.
0xE0100000-0xFFFFFFFF	Vendor_SYS	Partly reserved for future processor feature expansion. Any attempt to execute instructions from the region results in a MemManage fault. Data accesses are performed on S-AHB

The security level associated with an address is determined by either the internal *Secure Attribution Unit* (SAU) or an external *Implementation Defined Attribution Unit* (IDAU) in the system. Some internal peripherals have memory-mapped registers in the PPB region which are banked between Secure and Non-secure state. When the processor is in Secure state, software can access both the Secure and Non-secure versions of these registers. The Non-secure versions are accessed using an aliased address. See the *Arm®v8-M Architecture Reference Manual* for more information about the memory model.

3.6.3.1 Private Peripheral Bus

The *Private Peripheral Bus* (PPB) memory region provides access to internal and external processor resources. The internal PPB provides access to:

- The *System Control Space* (SCS), including the *Memory Protection Unit* (MPU), *Secure Attribution Unit* (SAU), and the *Nested Vectored Interrupt Controller* (NVIC).
- The *Data Watchpoint and Trace* (DWT)
- The *Breakpoint Unit* (BPU)
- The ROM table

The *external PPB* (EPPB) provides access to implementation-specific external areas of the PPB memory map.

3.6.3.2 Unaligned accesses

The Cortex-M33 processor supports unaligned accesses. They are converted into two or more aligned AHB transactions on the C-AHB or S-AHB master ports on the processor. Unaligned support is only available for load/store singles (LDR, LDRH, STR, STRH, TBH) to addresses in Normal memory. Load/store double and load/store multiple instructions already support word aligned accesses, but do not permit other unaligned accesses, and generate a fault if this is attempted. Unaligned accesses in Device memory are not permitted and fault. Unaligned accesses that cross memory map boundaries are architecturally UNPREDICTABLE.

Note

If CCR.UNALIGN_TRP for the current Security state is set, any unaligned accesses generate a fault.

3.6.4 Processor core registers summary

The following table shows the processor core register set summary. Each of these registers is 32 bits wide. Some of the registers are banked. The Secure view of these registers is available when the Cortex-M33 processor is in Secure state and the Non-secure view when Cortex-M33 processor is in Non-secure state.

Name	Description
R0-R12	R0-R12 are general-purpose registers for data operations.
MSP (R13) PSP (R13)	The Stack Pointer (SP) is register R13. In Thread mode, the CONTROL register indicates the stack pointer to use, *Main Stack Pointer* (MSP) or *Process Stack Pointer* (PSP). There are two MSP registers in the Cortex-M33 processor: • MSP_NS for the Non-secure state. • MSP_S for the Secure state. There are two PSP registers in the Cortex-M33 processor: • PSP_NS for the Non-secure state. • PSP_S for the Secure state.
MSPLIM PSPLIM	The stack limit registers limit the extent to which the MSP and PSP registers can descend respectively. There are two MSPLIM registers in the Cortex-M33 processor: • MSPLIM_NS for the Non-secure state. • MSPLIM_S for the Secure state. There are two PSPLIM registers in the Cortex-M33 processor: • PSPLIM_NS for the Non-secure state. • PSPLIM_S for the Secure state.
LR (R14)	The *Link Register* (LR) is register R14. It stores the return information for subroutines, function calls, and exceptions.
PC (R15)	The *Program Counter* (PC) is register R15. It contains the current program address.
PSR	The *Program Status Register* (PSR) combines: • *Application Program Status Register* (APSR). • *Interrupt Program Status Register* (IPSR). • *Execution Program Status Register* (EPSR). These registers provide different views of the PSR.
PRIMASK	The PRIMASK register prevents activation of exceptions with configurable priority. There are two PRIMASK registers in the Cortex-M33 processor: • PRIMASK_NS for the Non-secure state. • PRIMASK_S for the Secure state.

Name	Description
BASEPRI	The BASEPRI register defines the minimum priority for exception processing. There are two BASEPRI registers in the Cortex-M33 processor: • BASEPRI_NS for the Non-secure state. • BASEPRI_S for the Secure state.
FAULTMASK	The FAULTMASK register prevents activation of all exceptions except for NON-MASKABLE INTERRUPT (NMI) and optionally Secure HardFault. There are two FAULTMASK registers in the Cortex-M33 processor: • FAULTMASK_NS for the Non-secure state. • FAULTMASK_S for the Secure state.
CONTROL	The CONTROL register controls the stack used, and optionally the privilege level, when the processor is in Thread mode. There are two CONTROL registers in the Cortex-M33 processor: • CONTROL_NS for the Non-secure state. • CONTROL_S for the Secure state.

Note

See the Arm®v8-M Architecture Reference Manual for information about the processor core registers and their addresses, access types, and reset values.

3.6.5 Exceptions

Exceptions are handled and prioritized by the processor and the NVIC. In addition to architecturally defined behavior, the processor implements advanced exception and interrupt handling that reduces interrupt latency and includes implementation defined behavior.

3.6.5.1 Exception handling and prioritization

The processor core and the *Nested Vectored Interrupt Controller* (NVIC) together prioritize and handle all exceptions.

When handling exceptions:

- All exceptions are handled in Handler mode.
- Processor state is automatically stored to the stack on an exception, and automatically restored from the stack at the end of the *Interrupt Service Routine* (ISR).
- The vector is fetched in parallel to the state saving, enabling efficient interrupt entry. The processor supports tail-chaining that enables back-to-back interrupts without the overhead of state saving and restoration.

Software can configure the priorities of these interrupts. Exceptions can be specified as either Secure or Nonsecure. When an exception is taken the processor switches to the associated security state. The priority of Secure and Non-secure exceptions can be programmed independently. It is possible to deprioritize Nonsecure configurable exceptions using the AIRCR.PRIS bit field to enable Secure interrupts to take priority.

When taking and returning from an exception, the register state is always stored using the stack pointer associated with the background security state. When taking a Non-secure exception from Secure state, all the register state is stacked and then registers are cleared to prevent Secure data being available to the Non-secure handler. The vector base address is banked between Secure and Non-secure state. VTOR_S contains the Secure vector base address, and VTOR_NS contains the Non-secure vector base address. These registers can be programmed by software, and also initialized at reset by the system.

Note

Vector table entries are compatible with interworking between Arm and Thumb instructions. This causes bit[0] of the vector value to load into the *Execution Program Status Register* (EPSR) T-bit on exception entry. All populated vectors in the vector table entries must have bit[0] set. Creating a table entry with bit[0] clear generates an INVSTATE fault on the first instruction of the handler corresponding to this vector.

3.7 TrustZone-M

The system implements a ARM cortex M33 with security extensions, Secure and Non-secure MPU with 8 regions each and SAU with 8 regions.

3.7.1 Overview

The TrustZone-M consist of the following elements:

- IDAU configuration of background security memory attribution
- Trustzone Control Module (TCM), holding registers to control other TrustZone related features
- Periphery and control gaskets to enforce restrictions and enable selectable attribution of memory mapped registers
- Structures in memories to allocated memory to Secure and Non Secure memory region

3.7.2 M33 Configuration

M33 configuration:

- Floating Point Unit (FPU)
- Digital signal processing instructions
- Security extensions (Trustzone)
- NS MPU regions: 8
- S MPU regions 8
- SAU regions: 8
- IRQ priority levels: 8 (3 bits)
- 2 software interrupts
- Debug
  - 4 watchpoints
  - 8 breakpoint comparators
  - Data watchpoint and instrumentation trace (DWT/ITM)

3.7.3 Description of elements

3.7.3.1 IDAU (Implementation Defined Attribution Unit)

The IDAU defines a background memory map as follows:

If Address bit 26 (hereafter A[26]) is 0 then the address is attributed Non-Secure Callable (NSC).

For Peripherals if A[26] = 1, then the address is attributed as Secure.

Note

NSC attributed addresses are also Secure addresses

If A[26] = 0, then the address is attributed as Non Secure.

3.7.3.1.1 Expected use

The IDAU does not attribute any region directly as secure (S) because it is not allowed to change a S region to NSC. For addresses attributed Execute-never (XN) the distinction does not matter but for executable memory the user is responsible to use the SAU to mark regions not intended to be NSC as S. Best practice is to mark all Flash and SRAM that does not explicitly hold the SG (Secure Gateway) instructions as S or NS. I.e. mark all but

a region of the Flash and SRAM NSC regions as S where the remaining region holds all the SG instructions. If you do not execute secure code with SG calls from NS in SRAM mark all of SRAM NSC region as S.

3.8 CC35xx Host MCU Registers

3.8.1 HOSTMCU_AON Registers

Table 3-3 lists the memory-mapped registers for the HOSTMCU_AON registers. All register offset addresses not listed in Table 3-3 should be considered as reserved locations and the register contents should not be modified.

Table 3-3. HOSTMCU_AON Registers

Offset	Acronym	Register Name	Section
8h	CFGWICSNS	Host Wakup Interript Controller	Section 3.8.1.1
Ch	CFGWUTP	Wakeup Type Configuration	Section 3.8.1.2
10h	ELPTMREN	Timer Enable	Section 3.8.1.3
14h	CFGTMRWU	Timer Wakeup Configuration	Section 3.8.1.4
18h	TMRWUREQ	Timer Wake up Request Clear Register	Section 3.8.1.5
1Ch	CFGWDT	Watchdog Timer Configuration	Section 3.8.1.6
20h	WDTREQ	Watchdog Timer Req Register	Section 3.8.1.7
28h	GPWUAND	Wake Interrupt Configuration	Section 3.8.1.8
2Ch	GPWUOR	GPIO Configuration Register	Section 3.8.1.9
30h	GPWUAND1	GPIO Interrupt Configuration	Section 3.8.1.10
34h	GPWUOR1	GPIO Wakeup Configuration	Section 3.8.1.11
38h	FCLKARM	ARM Clock Command	Section 3.8.1.12
3Ch	SLPTIMES	Slow Clock Sleep	Section 3.8.1.13
40h	SLPTIMEF	Fast Sleep Timer	Section 3.8.1.14
4Ch	WUREQ	Wakeup Request Status	Section 3.8.1.15
5Ch	WUC	Wake-up Control State.	Section 3.8.1.16

Complex bit access types are encoded to fit into small table cells. Table 3-4 shows the codes that are used for access types in this section.

Table 3-4. HOSTMCU_AON Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

3.8.1.1 CFGWICSNS Register (Offset = 8h) [Reset = 00000000h]

CFGWICSNS is shown in Table 3-5.

Return to the Summary Table.

Configure WIC SENSE

Table 3-5. CFGWICSNS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17-0	VAL	R/W	0h	Field to control wake up source Set 1 - Enable wake up source. Set 0 - Disable wake up source. Bit 0 : ELP TMR Wake up request Bit 1 : GPIO wake up src 0 Bit 2 : GPIO wake up src 1 Bit 3 : doorbell 0 Bit 4 : doorbell 1 Bit 5 : doorbell 2 Bit 6 : doorbell 3 Bit 7 : doorbell 4 Bit 8 : doorbell 5 Bit 9 : doorbell 6 Bit 10 : doorbell 7 Bit 11 : nab_host_irq Bit 12 : ble_rfc_gpo_8_irq Bit 13 : RTC Bit 14 : DebugSS Csyspwrupreq Bit 15 : DebugSS Forceactive Bit 16 : secured_error_irq Bit 17 : core wdt irq Note: GPIO wakeup src 0 is AND of wakeup sources and GPIO wakup src 1 is OR of wakeup sources 0h = Disable wakeup source 1h = ELP timer wakeup request 2h = AND of wakeup sources 4h = OR of wakeup sources 8h = Doorbell 0 10h = Doorbell 1 20h = Doorbell 2 40h = Doorbell 3 80h = Doorbell 4 100h = Doorbell 5 200h = Doorbell 6 400h = Doorbell 7 800h = NAB host irq 1000h = BLE RFC GPO 9 irq 2000h = RTC 4000h = Debugss Csyspwrupreq 8000h = Debugss forecactive 00010000h = Secure error irq 00020000h = Core WDT request

3.8.1.2 CFGWUTP Register (Offset = Ch) [Reset = 00000000h]

CFGWUTP is shown in Table 3-6.

Return to the Summary Table.

ELP Wake-up Type Configuration. Register to configure wake up type

Table 3-6. CFGWUTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17-0	VAL	R/W	0h	Field to configure wake up type Set 0 - Slow Wake up (precise WU). Set 1 - Fast Wake up (assume system is already active when event is triggered). Bit 0 : ELP TMR Wake up request Bit 1 : GPIO wake up src 0 Bit 2 : GPIO wake up src 1 Bit 3 : doorbell 0 Bit 4 : doorbell 1 Bit 5 : doorbell 2 Bit 6 : doorbell 3 Bit 7 : doorbell 4 Bit 8 : doorbell 5 Bit 9 : doorbell 6 Bit 10 : doorbell 7 Bit 11 : nab_host_irq Bit 12 : ble_rfc_gpo_8_irq Bit 13 : RTC Bit 14 : DebugSS Csyspwrupreq Bit 15 : DebugSS Forceactive Bit 16 : secured_error_irq Bit 17 : core wdt irq Note: GPIO wakeup src 0 is AND of wakeup sources and GPIO wakup src 1 is OR of wakeup sources 0h = Slow wakeup(precise wakup) 1h = Fast Wake up 2h = Fast Wake up 4h = Fast Wake up 8h = Fast Wake up 10h = Fast Wake up 20h = Fast Wake up 40h = Fast Wake up 80h = Fast Wake up 100h = Fast Wake up 200h = Fast Wake up 400h = Fast Wake up 800h = Fast Wake up 1000h = Fast Wake up 2000h = Fast Wake up 4000h = Fast Wake up 8000h = Fast Wake up 00010000h = Fast Wake up 00020000h = Fast Wake up

3.8.1.3 ELPTMREN Register (Offset = 10h) [Reset = 00000002h]

ELPTMREN is shown in Table 3-7.

Return to the Summary Table.

ELP Timer Enable. Register to configure ELP Timer enable

Table 3-7. ELPTMREN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	ELPTMRLD	W	0h	ELP TIMER LOAD setting this bit will load the value 2 to the timer
15-4	RESERVED	R	0h	Reserved
3	ELPTMRRST	R/W	0h	ELP TIMER RESET setting this bit will stop the timer
2	ELPTMRSET	R/W	0h	ELP TIMER SET starts the timer
1	TMRSWCTL	R/W	1h	Field to configure the type of timer control 0h = Hardware control 1h = Software control
0	VAL	R/W	0h	Field to enable ELP Timer 0h = Disable 1h = Enable

3.8.1.4 CFGTMRWU Register (Offset = 14h) [Reset = 00000000h]

CFGTMRWU is shown in Table 3-8.

Return to the Summary Table.

Timer Wake-up Configuration. Register to configure Timer wake up

Table 3-8. CFGTMRWU Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	Field to enable timer wake up Set 1 - Enable BCN threshold IRQ. Set 0 - Otherwise. Timer is kicked upon moving from ACTIVE to POWER DOWN. 0h = otherwise 1h = Enable BCN threshold IRQ
30-0	THR	R/W	0h	Field to configure the Threshold of timer wake up Upon reaching this value wake up event is generated towards the WUC (if not masked in WICSENSE). Resolution slow clock cycles. value must be greater than 1

3.8.1.5 TMRWUREQ Register (Offset = 18h) [Reset = 00000000h]

TMRWUREQ is shown in Table 3-9.

Return to the Summary Table.

Timer Wake-up Request Clear. Register to configure timer wake up request

Table 3-9. TMRWUREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CLR	R/W	0h	Field to clear timer wake up request. Set this bit to clear

3.8.1.6 CFGWDT Register (Offset = 1Ch) [Reset = 800EA600h]

CFGWDT is shown in Table 3-10.

Return to the Summary Table.

Watch Dog Timer Configuration. Register to configure watchdog timer

Table 3-10. CFGWDT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	1h	Field to enable watchdog timer 0h = 0x0 1h = 0x1
30-8	THR	R/W	EA6h	Field to configure watchdog timer threshold Upon reaching this value wake up event is generated towards the WUC (if not masked in WICSENSE). Resolution slow clock cycles (min val ~8ms). value must be greater than 1
7-0	RESERVED	R	0h	Reserved

3.8.1.7 WDTREQ Register (Offset = 20h) [Reset = 00000000h]

WDTREQ is shown in Table 3-11.

Return to the Summary Table.

Watch Dog Timer Request Clear. Register to clear watchdog timer request

Table 3-11. WDTREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CLR	R/W	0h	Field to clear watchdog timer request. Set this bet to clear

3.8.1.8 GPWUAND Register (Offset = 28h) [Reset = FFFFFFFFh]

GPWUAND is shown in Table 3-12.

Return to the Summary Table.

GPIO Wake-up AND IRQ Configuration. Field to configure *GPIO* wake up AND *IRQ* 0 to 31

Table 3-12. GPWUAND Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BM0T31	R/W	FFFFFFFFh	Field to bit mask GPIO 0 to 31 select 0-31 GPIOs as wake up source.

3.8.1.9 GPWUOR Register (Offset = 2Ch) [Reset = FFFFFFFFh]

GPWUOR is shown in Table 3-13.

Return to the Summary Table.

GPIO Wake-up OR IRQ Configuration. Field to configure *GPIO* wake up OR gate *IRQ*

Table 3-13. GPWUOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BM0T31	R/W	FFFFFFFFh	Field to bit mask GPIO 0 to 31 select 0-31 GPIOs as wake up source.

3.8.1.10 GPWUAND1 Register (Offset = 30h) [Reset = 000FFFFFh]

GPWUAND1 is shown in Table 3-14.

Return to the Summary Table.

GPIO Wake-up AND IRQ Configuration. Field to configure *GPIO* wake up AND *IRQ* 32 to 44

Table 3-14. GPWUAND1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	BM32T44	R/W	1FFFh	Field to bit mask 32 to 44 select 32-44 GPIOs as wake up source.

3.8.1.11 GPWUOR1 Register (Offset = 34h) [Reset = 000FFFFFh]

GPWUOR1 is shown in Table 3-15.

Return to the Summary Table.

GPIO Wake-up OR IRQ Configuration. Field to configure *GPIO* wake up OR *IRQ* 32 to 44

Table 3-15. GPWUOR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	BM32T44	R/W	1FFFh	Field to bit mask 32 to 44 select 32-44 GPIOs as wake up source.

3.8.1.12 FCLKARM Register (Offset = 38h) [Reset = 00000000h]

FCLKARM is shown in Table 3-16.

Return to the Summary Table.

Fast Clock From ARM Command

Table 3-16. FCLKARM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CMD	R/W	0h	Command Latched counter value reflecting the number of fast clocks (host_clk) from rise of SLEEPDEEP indication until ELP WUC start power down sequence. This value should capture the uncertainty of 2-3 slow clocks of synchronization of ARM CMD

3.8.1.13 SLPTIMES Register (Offset = 3Ch) [Reset = 00000000h]

SLPTIMES is shown in Table 3-17.

Return to the Summary Table.

Sleep Time Slow Clock. Register for sleep time on slow clock

Table 3-17. SLPTIMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLK	R/W	0h	Sleep time value from last ELP sleep entry (slow clock synced ARM CMD). Slow Clock - Reflects the number of slow clocks in ELP timer.

3.8.1.14 SLPTIMEF Register (Offset = 40h) [Reset = 00000000h]

SLPTIMEF is shown in Table 3-18.

Return to the Summary Table.

Sleep Time Fast Clock. Register for sleep time on fast clock

Table 3-18. SLPTIMEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	CLK	R/W	0h	Sleep time value from last ELP sleep entry (slow clock synced ARM CMD). Fast Clock - Reflects the number of fast clocks from last Slow clock rise until OCP Read. Note, fast counter value is latched upon OCP Read of ELP_SLEEP_TIME_SLOW. Counts up t0 51 microsecond.

3.8.1.15 WUREQ Register (Offset = 4Ch) [Reset = 00000000h]

WUREQ is shown in Table 3-19.

Return to the Summary Table.

Wake up Request Status

Table 3-19. WUREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17-0	VAL	R/W	0h	Field to show the event request Bit 0 : ELP TMR Wake up request Bit 1 : GPIO wake up src 0 Bit 2 : GPIO wake up src 1 Bit 3 : doorbell 0 Bit 4 : doorbell 1 Bit 5 : doorbell 2 Bit 6 : doorbell 3 Bit 7 : doorbell 4 Bit 8 : doorbell 5 Bit 9 : doorbell 6 Bit 10 : doorbell 7 Bit 11 : nab_host_irq Bit 12 : ble_rfc_gpo_8_irq Bit 13 : RTC Bit 14 : DebugSS Csyspwrupreq Bit 15 : DebugSS Force-active Bit 16 : secured_error_irq Bit 17 : core wdt irq Note: GPIO wakeup src 0 is AND of wakeup sources and GPIO wakup src 1 is OR of wakeup sources 0h = No event request 1h = ELP timer wakeup request 2h = AND of wakeup sources 4h = OR of wakeup sources 8h = Doorbell 0 10h = Doorbell 1 20h = Doorbell 2 40h = Doorbell 3 80h = Doorbell 4 100h = Doorbell 5 200h = Doorbell 6 400h = Doorbell 7 800h = NAB host irq 1000h = BLE RFC GPO 9 irq 2000h = RTC 4000h = Debugss Csyspwrupreq 8000h = Debugss forecactive 00010000h = Secure error irq 00020000h = Core WDT request

3.8.1.16 WUC Register (Offset = 5Ch) [Reset = 00000004h]

WUC is shown in Table 3-20.

Return to the Summary Table.

Wake-up Control State.

Table 3-20. WUC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	STA	R	4h	Field showing the host wake up state 3'b000 - PD_PWR_DN 3'b001 - SHARED_UP 3'b010 - PD_PWR_UP 3'b011 - ACTIVE 3'b100 - DEEPSLEEP 0h = PD power down 1h = Shared domain up 2h = PD power up 3h = Active

3.8.2 HOST_MCU Registers

Table 3-21 lists the memory-mapped registers for the HOST_MCU registers. All register offset addresses not listed in Table 3-21 should be considered as reserved locations and the register contents should not be modified.

Table 3-21. HOST_MCU Registers

Offset	Acronym	Register Name	Section
0h	TRACECFG	Trace Configuration	Section 3.8.2.1
18h	SWIRQ	Software Timestamp Interrupt	Section 3.8.2.2
1Ch	NSSWIRQ	Software Interrupt Trigger	Section 3.8.2.3
20h	SWIRQCM3	M3 Software Interrupt	Section 3.8.2.4
24h	ARBPOL	Arbitration Policy	Section 3.8.2.5
28h	DBGSS	Debug Subsystem Control	Section 3.8.2.6
2Ch	DBGSSLCK	Debug Interface Lock	Section 3.8.2.7
30h	DBGSSLM	Lock Condition Mask	Section 3.8.2.8
34h	DBGSSLS	Lock Condition Status	Section 3.8.2.9

Complex bit access types are encoded to fit into small table cells. Table 3-22 shows the codes that are used for access types in this section.

Table 3-22. HOST_MCU Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

3.8.2.1 TRACECFG Register (Offset = 0h) [Reset = 00000000h]

TRACECFG is shown in Table 3-23.

Return to the Summary Table.

Trace Configuration. Configuration register for CortexM3-TPIU (TRACE ports i/o unit)

Table 3-23. TRACECFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CLKDIVEN	W	0h	Set this register to load [CLKDIVVAL] 0h = 0x0 1h = Disable
7-2	RESERVED	R	0h	Reserved
1-0	CLKDIVVAL	R/W	2h	Configure TRACE-CLOCK divider value, for (TPIU - input clock) [1] - Divide by 2 - 'tpiu_trace_clk_in' = 40MHz [2] - Divide by 4 - 'tpiu_trace_clk_in' = 20MHz (Default) [0,3] - are not supported (do not use) AFTER setting this value - set [CLKDIVEN] to active this value 0h = Divide by 2 1h = Divide by 4

3.8.2.2 SWIRQ Register (Offset = 18h) [Reset = 00000000h]

SWIRQ is shown in Table 3-24.

Return to the Summary Table.

Software Timestamp Interrupt Register

Table 3-24. SWIRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	TIMESTAMP	R/W	0h	Field to write timestamp for ET bus.

3.8.2.3 NSSWIRQ Register (Offset = 1Ch) [Reset = 00000000h]

NSSWIRQ is shown in Table 3-25.

Return to the Summary Table.

Non Secure Software Interrupt

Table 3-25. NSSWIRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	EN	R/W	0h	Non Secure context of CM33 can use this register to interrupt secure context of CM33.

3.8.2.4 SWIRQCM3 Register (Offset = 20h) [Reset = 00000000h]

SWIRQCM3 is shown in Table 3-26.

Return to the Summary Table.

Software Interrupt to CM3

Table 3-26. SWIRQCM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EN	R/W	0h	Non Secure context of CM33 can use this register to interrupt CM3.

3.8.2.5 ARBPOL Register (Offset = 24h) [Reset = 00000000h]

ARBPOL is shown in Table 3-27.

Return to the Summary Table.

Arbiter Policy. Arbiter Policy for the arbiters(x2) located just before MEMSS Portion A and Portion B

Table 3-27. ARBPOL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-8	S1PRIM1	R/W	0h	This bit field takes affect when Fixed Priority is selected for the arbiter before MEMSS Portion B. This field is used to configure the priority of ocp.
7-6	S1PRIM0	R/W	0h	This bit field takes affect when Fixed Priority is selected for the arbiter before MEMSS Portion B. This field is used to configure the priority of udma/sahb.
5-4	S0PRIM1	R/W	0h	This bit field takes affect when Fixed Priority is selected for the arbiter before MEMSS Portion A. This field is used to configure the priority of ocp.
3-2	S0PRIM0	R/W	0h	This bit field takes affect when Fixed Priority is selected for the arbiter before MEMSS Portion A. This field is used to configure the priority of udma/sahb.
1	RNDRBNS1	R/W	1h	Field to select the arbitration policy of second arbiter (MEMSS Portion) 1 -> Round Robin is enabled 0 -> Fixed priority is enabled 0h = Fixed priority 1h = Round Robin priority
0	RNDRBNS0	R/W	1h	Field to select the arbitration policy of second arbiter (MEMSS Portion A) 1 -> Round Robin is enabled 0 -> Fixed priority is enabled 0h = Fixed priority 1h = Round Robin priority

3.8.2.6 DBGSS Register (Offset = 28h) [Reset = 00000000h]

DBGSS is shown in Table 3-28.

Return to the Summary Table.

DEBUGSS Control Register.

Table 3-28. DBGSS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EN	R/W	0h	Non Secure context of CM33 can use this register to interrupt CM3.

3.8.2.7 DBGSSLCK Register (Offset = 2Ch) [Reset = 00000000h]

DBGSSLCK is shown in Table 3-29.

Return to the Summary Table.

DEBUGSS Interface Lock.

Table 3-29. DBGSSLCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	LOCK	R/W	0h	The method: Obtain lock by Read. Following are all s/w operation possibilities: When reading '1' - lock is obtained. (i.e. no debugss request was active during the rd transaction). When reading '0' - lock is not obtained. Try to read again. (i.e. at least debugss request event was active during the rd transaction). when writing '1' - lock will be obtained regardless to debugss request status when writing '0' - lock will be released. Type: Write/Read-Clear

3.8.2.8 DBGSSLM Register (Offset = 30h) [Reset = 00000000h]

DBGSSLM is shown in Table 3-30.

Return to the Summary Table.

DEBUGSS Interface Lock Condition Mask

Table 3-30. DBGSSLM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	MASK	R/W	0h	Masks Debugss Force-active Set 1 - Mask request during lock check. Set 0 - O.W. 0h = O.W 1h = Mask request during lock check
0	RESERVED	R	0h	Reserved

3.8.2.9 DBGSSLS Register (Offset = 34h) [Reset = 00000000h]

DBGSSLS is shown in Table 3-31.

Return to the Summary Table.

DEBUGSS Interface Lock Condition Status

Table 3-31. DBGSSLS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	FRCACT	R	0h	DEBUGSS HOST Force Active 0h = Not in use 1h = Debugss host force active is set
0	CSYSPWRREQ	R	0h	DEBUGSS HOST C SYS Power Request 0h = Not in use 1h = Debugss host c sys power requested

3.8.3 HOST_MCU_SEC Registers

Table 3-32 lists the memory-mapped registers for the HOST_MCU_SEC registers. All register offset addresses not listed in Table 3-32 should be considered as reserved locations and the register contents should not be modified.

Table 3-32. HOST_MCU_SEC Registers

Offset	Acronym	Register Name	Section
0h	SSWIRQ2NS	Secure To Non Secure Software Interrupt	Section 3.8.3.1
4h	SWIRQ2CM3	SW Cortex-M3 Interrupt	Section 3.8.3.2
8h	LCKUP	Host Lockup Trigger	Section 3.8.3.3

Complex bit access types are encoded to fit into small table cells. Table 3-33 shows the codes that are used for access types in this section.

Table 3-33. HOST_MCU_SEC Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

3.8.3.1 SSWIRQ2NS Register (Offset = 0h) [Reset = 00000000h]

SSWIRQ2NS is shown in Table 3-34.

Return to the Summary Table.

Secure Software Interrupt

Table 3-34. SSWIRQ2NS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	EN	R/W	0h	Secure context of CM33 can use this register to interrupt non secure context of CM33.

3.8.3.2 SWIRQ2CM3 Register (Offset = 4h) [Reset = 00000000h]

SWIRQ2CM3 is shown in Table 3-35.

Return to the Summary Table.

Software Interrupt to CM3

Table 3-35. SWIRQ2CM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EN	R/W	0h	Secure context of CM33 can use this register to interrupt CM3.

3.8.3.3 LCKUP Register (Offset = 8h) [Reset = 00000000h]

LCKUP is shown in Table 3-36.

Return to the Summary Table.

Software Interrupt to CM3

Table 3-36. LCKUP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	VAL	R	0h	The processor enters a lockup state if a fault occurs when it cannot be serviced or escalated. When the processor is in lockup state, it does not execute any instructions. The processor remains in lockup state until either: * It is reset. * Preemption by a higher priority exception occurs. * It is halted by a debugger.

3.9 Arm® Cortex®-M33 Registers

3.9.1 CPU_ROM_TABLE Registers

Table 3-37 lists the memory-mapped registers for the CPU_ROM_TABLE registers. All register offset addresses not listed in Table 3-37 should be considered as reserved locations and the register contents should not be modified.

Table 3-37. CPU_ROM_TABLE Registers

Offset	Acronym	Register Name	Section
0h	SCS_ENTRY	SCS component	Section 3.9.1.1
4h	DWT_ENTRY	Data watchpoint unit	Section 3.9.1.2
8h	FPB_ENTRY	Flash Patch and Breakpoint unit	Section 3.9.1.3
Ch	ITM_ENTRY	never implemented	Section 3.9.1.4
10h	TPIU_ENTRY	Trace Port Interface unit	Section 3.9.1.5
14h	ETM_ENTRY	Embedded Trace Macrocell	Section 3.9.1.6
18h	CTI_ENTRY	Cross Trigger Interface	Section 3.9.1.7
1Ch	MTB_ENTRY	Micro Trace Buffer	Section 3.9.1.8
20h	END_MARKER	end of the rom for discovery	Section 3.9.1.9
FCCh	SYSTEM_ACCESS_ENTRY	SYSTEM ACCESS	Section 3.9.1.10
FD0h	PIDR4	CoreSight Peripheral ID4	Section 3.9.1.11
FD4h	PIDR5	CoreSight Peripheral ID5	Section 3.9.1.12
FD8h	PIDR6	CoreSight Peripheral ID6	Section 3.9.1.13
FDCh	PIDR7	CoreSight Peripheral ID7	Section 3.9.1.14
FE0h	PIDR0	CoreSight Peripheral ID0	Section 3.9.1.15
FE4h	PIDR1	CoreSight Peripheral ID1	Section 3.9.1.16
FE8h	PIDR2	CoreSight Peripheral ID2	Section 3.9.1.17
FECh	PIDR3	CoreSight Peripheral ID3	Section 3.9.1.18
FF0h	CIDR0	CoreSight Component ID0	Section 3.9.1.19
FF4h	CIDR1	CoreSight Component ID1	Section 3.9.1.20
FF8h	CIDR2	CoreSight Component ID2	Section 3.9.1.21
FFCh	CIDR3	CoreSight Component ID3	Section 3.9.1.22

Complex bit access types are encoded to fit into small table cells. Table 3-38 shows the codes that are used for access types in this section.

Table 3-38. CPU_ROM_TABLE Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

3.9.1.1 SCS_ENTRY Register (Offset = 0h) [Reset = 00000000h]

SCS_ENTRY is shown in Table 3-39.

Return to the Summary Table.

SCS component

Table 3-39. SCS_ENTRY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	BASE_ADDR	R	000FFF0Fh	Base address for master interface 0. Bit[31] is always 0.
11-9	RES0_1	R	0h	Reserved, RES0
8-4	POWER_DOMAIN_ID	R	0h	Indicates the power domain ID of the component. This field is only valid when bit[2] of this register is 0b1. Otherwise this field is 0b1.
3	RES0_0	R	0h	Reserved, RES0
2	POWER_DOMAIN_ID_VALID	R	0h	Indicates whether there is a power domain ID specified in the ROM Table entry
1	FORMAT	R	1h	Indicates the ROM table entry format
0	ENTRY_PRESENT	R	1h	Indicates whether there is a valid ROM entry at this location.

3.9.1.2 DWT_ENTRY Register (Offset = 4h) [Reset = 00000000h]

DWT_ENTRY is shown in Table 3-40.

Return to the Summary Table.

Data watchpoint unit

Table 3-40. DWT_ENTRY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	BASE_ADDR	R	000FFF02h	Base address for master interface 0. Bit[31] is always 0.
11-9	RES0_1	R	0h	Reserved, RES0
8-4	POWER_DOMAIN_ID	R	0h	Indicates the power domain ID of the component. This field is only valid when bit[2] of this register is 0b1. Otherwise this field is 0b1.
3	RES0_0	R	0h	Reserved, RES0
2	POWER_DOMAIN_ID_VALID	R	0h	Indicates whether there is a power domain ID specified in the ROM Table entry
1	FORMAT	R	1h	Indicates the ROM table entry format
0	ENTRY_PRESENT	R	1h	Indicates whether there is a valid ROM entry at this location.

3.9.1.3 FPB_ENTRY Register (Offset = 8h) [Reset = 00000000h]

FPB_ENTRY is shown in Table 3-41.

Return to the Summary Table.

Flash Patch and Breakpoint unit

Table 3-41. FPB_ENTRY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	BASE_ADDR	R	000FFF03h	Base address for master interface 0. Bit[31] is always 0.
11-9	RES0_1	R	0h	Reserved, RES0
8-4	POWER_DOMAIN_ID	R	0h	Indicates the power domain ID of the component. This field is only valid when bit[2] of this register is 0b1. Otherwise this field is 0b1.
3	RES0_0	R	0h	Reserved, RES0
2	POWER_DOMAIN_ID_VALID	R	0h	Indicates whether there is a power domain ID specified in the ROM Table entry
1	FORMAT	R	1h	Indicates the ROM table entry format
0	ENTRY_PRESENT	R	1h	Indicates whether there is a valid ROM entry at this location.

3.9.1.4 ITM_ENTRY Register (Offset = Ch) [Reset = 00000000h]

ITM_ENTRY is shown in Table 3-42.

Return to the Summary Table.

never implemented

Table 3-42. ITM_ENTRY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	BASE_ADDR	R	000FFF01h	Base address for master interface 0. Bit[31] is always 0.
11-9	RES0_1	R	0h	Reserved, RES0
8-4	POWER_DOMAIN_ID	R	0h	Indicates the power domain ID of the component. This field is only valid when bit[2] of this register is 0b1. Otherwise this field is 0b1.
3	RES0_0	R	0h	Reserved, RES0
2	POWER_DOMAIN_ID_VALID	R	0h	Indicates whether there is a power domain ID specified in the ROM Table entry
1	FORMAT	R	1h	Indicates the ROM table entry format
0	ENTRY_PRESENT	R	1h	Indicates whether there is a valid ROM entry at this location.

3.9.1.5 TPIU_ENTRY Register (Offset = 10h) [Reset = 00000000h]

TPIU_ENTRY is shown in Table 3-43.

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Trace Port Interface unit

Table 3-43. TPIU_ENTRY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	BASE_ADDR	R	000FFF41h	Base address for master interface 0. Bit[31] is always 0.
11-9	RES0_1	R	0h	Reserved, RES0
8-4	POWER_DOMAIN_ID	R	0h	Indicates the power domain ID of the component. This field is only valid when bit[2] of this register is 0b1. Otherwise this field is 0b1.
3	RES0_0	R	0h	Reserved, RES0
2	POWER_DOMAIN_ID_VALID	R	0h	Indicates whether there is a power domain ID specified in the ROM Table entry
1	FORMAT	R	1h	Indicates the ROM table entry format
0	ENTRY_PRESENT	R	0h	Indicates whether there is a valid ROM entry at this location.

3.9.1.6 ETM_ENTRY Register (Offset = 14h) [Reset = 00000000h]

ETM_ENTRY is shown in Table 3-44.

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Embedded Trace Macrocell

Table 3-44. ETM_ENTRY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	BASE_ADDR	R	000FFF42h	Base address for master interface 0. Bit[31] is always 0.
11-9	RES0_1	R	0h	Reserved, RES0
8-4	POWER_DOMAIN_ID	R	0h	Indicates the power domain ID of the component. This field is only valid when bit[2] of this register is 0b1. Otherwise this field is 0b1.
3	RES0_0	R	0h	Reserved, RES0
2	POWER_DOMAIN_ID_VALID	R	0h	Indicates whether there is a power domain ID specified in the ROM Table entry
1	FORMAT	R	1h	Indicates the ROM table entry format
0	ENTRY_PRESENT	R	0h	Indicates whether there is a valid ROM entry at this location.

3.9.1.7 CTI_ENTRY Register (Offset = 18h) [Reset = 00000000h]

CTI_ENTRY is shown in Table 3-45.

Return to the Summary Table.

Cross Trigger Interface

Table 3-45. CTI_ENTRY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	BASE_ADDR	R	000FFF43h	Base address for master interface 0. Bit[31] is always 0.
11-9	RES0_1	R	0h	Reserved, RES0
8-4	POWER_DOMAIN_ID	R	0h	Indicates the power domain ID of the component. This field is only valid when bit[2] of this register is 0b1. Otherwise this field is 0b1.
3	RES0_0	R	0h	Reserved, RES0
2	POWER_DOMAIN_ID_VALID	R	0h	Indicates whether there is a power domain ID specified in the ROM Table entry
1	FORMAT	R	1h	Indicates the ROM table entry format
0	ENTRY_PRESENT	R	0h	Indicates whether there is a valid ROM entry at this location.

3.9.1.8 MTB_ENTRY Register (Offset = 1Ch) [Reset = 00000000h]

MTB_ENTRY is shown in Table 3-46.

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Micro Trace Buffer

Table 3-46. MTB_ENTRY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	BASE_ADDR	R	000FFF44h	Base address for master interface 0. Bit[31] is always 0.
11-9	RES0_1	R	0h	Reserved, RES0
8-4	POWER_DOMAIN_ID	R	0h	Indicates the power domain ID of the component. This field is only valid when bit[2] of this register is 0b1. Otherwise this field is 0b1.
3	RES0_0	R	0h	Reserved, RES0
2	POWER_DOMAIN_ID_VALID	R	0h	Indicates whether there is a power domain ID specified in the ROM Table entry
1	FORMAT	R	1h	Indicates the ROM table entry format
0	ENTRY_PRESENT	R	0h	Indicates whether there is a valid ROM entry at this location.

3.9.1.9 END_MARKER Register (Offset = 20h) [Reset = 00000000h]

END_MARKER is shown in Table 3-47.

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end of the rom for discovery

Table 3-47. END_MARKER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

3.9.1.10 SYSTEM_ACCESS_ENTRY Register (Offset = FCCh) [Reset = 00000000h]

SYSTEM_ACCESS_ENTRY is shown in Table 3-48.

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SYSTEM ACCESS

Table 3-48. SYSTEM_ACCESS_ENTRY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	1h	Reserved, RES0

3.9.1.11 PIDR4 Register (Offset = FD0h) [Reset = 00000000h]

PIDR4 is shown in Table 3-49.

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CoreSight Peripheral ID4

Table 3-49. PIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	SIZE	R	0h	Always 0b0000. Indicates that the device only occupies 4KB of memory
3-0	DES_2	R	4h	Together, PIDR1.DES_0, PIDR2.DES_1, and PIDR4.DES_2 identify the designer of the component.

3.9.1.12 PIDR5 Register (Offset = FD4h) [Reset = 00000000h]

PIDR5 is shown in Table 3-50.

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CoreSight Peripheral ID5

Table 3-50. PIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

3.9.1.13 PIDR6 Register (Offset = FD8h) [Reset = 00000000h]

PIDR6 is shown in Table 3-51.

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CoreSight Peripheral ID6

Table 3-51. PIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

3.9.1.14 PIDR7 Register (Offset = FDCh) [Reset = 00000000h]

PIDR7 is shown in Table 3-52.

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CoreSight Peripheral ID7

Table 3-52. PIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

3.9.1.15 PIDR0 Register (Offset = FE0h) [Reset = 00000000h]

PIDR0 is shown in Table 3-53.

Return to the Summary Table.

CoreSight Peripheral ID0

Table 3-53. PIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PART_0	R	C9h	Bits[7:0] of the 12-bit part number of the component. The designer of the component assigns this part number.

3.9.1.16 PIDR1 Register (Offset = FE4h) [Reset = 00000000h]

PIDR1 is shown in Table 3-54.

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CoreSight Peripheral ID1

Table 3-54. PIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	DES_0	R	Bh	Together, PIDR1.DES_0, PIDR2.DES_1, and PIDR4.DES_2 identify the designer of the component.
3-0	PART_1	R	4h	Bits[11:8] of the 12-bit part number of the component. The designer of the component assigns this part number.

3.9.1.17 PIDR2 Register (Offset = FE8h) [Reset = 00000000h]

PIDR2 is shown in Table 3-55.

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CoreSight Peripheral ID2

Table 3-55. PIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	REVISION	R	0h	This device is at r1p0
3	JEDEC	R	1h	Always 1. Indicates that the JEDEC-assigned designer ID is used.
2-0	DES_1	R	3h	Together, PIDR1.DES_0, PIDR2.DES_1, and PIDR4.DES_2 identify the designer of the component.

3.9.1.18 PIDR3 Register (Offset = FECh) [Reset = 00000000h]

PIDR3 is shown in Table 3-56.

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CoreSight Peripheral ID3

Table 3-56. PIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	REVAND	R	0h	Indicates minor errata fixes specific to the revision of the component being used, for example metal fixes after implementation. In most cases, this field is 0b0000. ARM recommends that the component designers ensure that a metal fix can change this field if required, for example, by driving it from registers that reset to 0b0000.
3-0	CMOD	R	0h	Customer Modified. Indicates whether the customer has modified the behavior of the component. In most cases, this field is 0b0000. Customers change this value when they make authorized modifications to this component.

3.9.1.19 CIDR0 Register (Offset = FF0h) [Reset = 00000000h]

CIDR0 is shown in Table 3-57.

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CoreSight Component ID0

Table 3-57. CIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PRMBL_0	R	Dh	Preamble[0]. Contains bits[7:0] of the component identification code

3.9.1.20 CIDR1 Register (Offset = FF4h) [Reset = 00000000h]

CIDR1 is shown in Table 3-58.

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CoreSight Component ID1

Table 3-58. CIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	CLASS	R	1h	Class of the component, for example, whether the component is a ROM table or a generic CoreSight component. Contains bits[15:12] of the component identification code.
3-0	PRMBL_1	R	0h	Preamble[1]. Contains bits[11:8] of the component identification code.

3.9.1.21 CIDR2 Register (Offset = FF8h) [Reset = 00000000h]

CIDR2 is shown in Table 3-59.

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CoreSight Component ID2

Table 3-59. CIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PRMBL_2	R	5h	Preamble[2]. Contains bits[23:16] of the component identification code.

3.9.1.22 CIDR3 Register (Offset = FFCh) [Reset = 00000000h]

CIDR3 is shown in Table 3-60.

Return to the Summary Table.

CoreSight Component ID3

Table 3-60. CIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PRMBL_3	R	B1h	Preamble[3]. Contains bits[31:24] of the component identification code.

3.9.2 TPIU Registers

Table 3-61 lists the memory-mapped registers for the TPIU registers. All register offset addresses not listed in Table 3-61 should be considered as reserved locations and the register contents should not be modified.

Table 3-61. TPIU Registers

Offset	Acronym	Register Name	Section
0h	SSPSR	Supported Sync Port Sizes	Section 3.9.2.1
4h	CSPSR	Current Sync Port Size	Section 3.9.2.2
10h	ACPR	Async Clock Prescaler	Section 3.9.2.3
F0h	SPPR	Selected Pin Protocol	Section 3.9.2.4
300h	FFSR	Formatter and Flush Status	Section 3.9.2.5
304h	FFCR	Formatter and Flush Control	Section 3.9.2.6
308h	PSCR	Formatter Synchronization Counter	Section 3.9.2.7
FA0h	CLAIMMASK	Claim Tag Mask	Section 3.9.2.8
FA0h	CLAIMSET	Claim Tag Set	Section 3.9.2.9
FA4h	CLAIMTAG	Current Claim Tag	Section 3.9.2.10
FA4h	CLAIMCLR	Claim Tag Clear	Section 3.9.2.11
FC8h	DEVID	Device ID	Section 3.9.2.12

Complex bit access types are encoded to fit into small table cells. Table 3-62 shows the codes that are used for access types in this section.

Table 3-62. TPIU Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

3.9.2.1 SSPSR Register (Offset = 0h) [Reset = 00000000h]

SSPSR is shown in Table 3-63.

Return to the Summary Table.

Supported Sync Port Sizes
This register represents a single port size that is supported on the device, that is, 4, 2 or 1. This is to ensure that tools do not attempt to select a port width that an attached TPA cannot capture.

Table 3-63. SSPSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	FOUR	R	1h	4-bit port size support 0x0: Not supported 0x1: Supported
2	THREE	R	0h	3-bit port size support 0x0: Not supported 0x1: Supported
1	TWO	R	1h	2-bit port size support 0x0: Not supported 0x1: Supported
0	ONE	R	1h	1-bit port size support 0x0: Not supported 0x1: Supported

3.9.2.2 CSPSR Register (Offset = 4h) [Reset = 00000000h]

CSPSR is shown in Table 3-64.

Return to the Summary Table.

Current Sync Port Size
This register has the same format as SSPSR but only one bit can be set, and all others must be zero. Writing values with more than one bit set, or setting a bit that is not indicated as supported can cause Unpredictable behavior. On reset this defaults to the smallest possible port size, 1 bit.

Table 3-64. CSPSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	FOUR	R/W	0h	4-bit port enable Writing values with more than one bit set in CSPSR, or setting a bit that is not indicated as supported in SSPSR can cause Unpredictable behavior.
2	THREE	R/W	0h	3-bit port enable Writing values with more than one bit set in CSPSR, or setting a bit that is not indicated as supported in SSPSR can cause Unpredictable behavior.
1	TWO	R/W	0h	2-bit port enable Writing values with more than one bit set in CSPSR, or setting a bit that is not indicated as supported in SSPSR can cause Unpredictable behavior.
0	ONE	R/W	1h	1-bit port enable Writing values with more than one bit set in CSPSR, or setting a bit that is not indicated as supported in SSPSR can cause Unpredictable behavior.

3.9.2.3 ACPR Register (Offset = 10h) [Reset = 00000000h]

ACPR is shown in Table 3-65.

Return to the Summary Table.

Async Clock Prescaler
This register scales the baud rate of the asynchronous output.

Table 3-65. ACPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
12-0	PRESCALER	R/W	0h	Divisor for input trace clock is (PRESCALER + 1).

3.9.2.4 SPPR Register (Offset = F0h) [Reset = 00000000h]

SPPR is shown in Table 3-66.

Return to the Summary Table.

Selected Pin Protocol
This register selects the protocol to be used for trace output.
Note: If this register is changed while trace data is being output, data corruption occurs.

Table 3-66. SPPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	PROTOCOL	R/W	1h	Trace output protocol 0h = TracePort mode 1h = SerialWire Output (Manchester). This is the reset value. 2h = SerialWire Output (NRZ)

3.9.2.5 FFSR Register (Offset = 300h) [Reset = 00000000h]

FFSR is shown in Table 3-67.

Return to the Summary Table.

Formatter and Flush Status

Table 3-67. FFSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	FTNONSTOP	R	1h	0: Formatter can be stopped 1: Formatter cannot be stopped
2-0	RESERVED	R	0h	This field always reads as zero

3.9.2.6 FFCR Register (Offset = 304h) [Reset = 00000000h]

FFCR is shown in Table 3-68.

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Formatter and Flush Control
When one of the two single wire output (SWO) modes is selected, ENFCONT enables the formatter to be bypassed. If the formatter is bypassed, only the ITM/DWT trace source (ATDATA2) passes through. The TPIU accepts and discards data that is presented on the ETM port (ATDATA1). This function is intended to be used when it is necessary to connect a device containing an ETM to a trace capture device that is only able to capture Serial Wire Output (SWO) data. Enabling or disabling the formatter causes momentary data corruption.
Note: If the selected pin protocol register (SPPR.PROTOCOL) is set to 0x00 (TracePort mode), this register always reads 0x102, because the formatter is automatically enabled. If one of the serial wire modes is then selected, the register reverts to its previously programmed value.

Table 3-68. FFCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
8	TRIGIN	R/W	1h	Indicates that triggers are inserted when a trigger pin is asserted.
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	ENFCONT	R/W	1h	Enable continuous formatting: 0: Continuous formatting disabled 1: Continuous formatting enabled
0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

3.9.2.7 PSCR Register (Offset = 308h) [Reset = 00000000h]

PSCR is shown in Table 3-69.

Return to the Summary Table.

Periodic Synchronization Control Registers

Table 3-69. PSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	PSCOUNT	R/W	0h	Periodic Synchronization Count. Determines the reload value of the Periodic Synchronization Counter. The reload value takes effect the next time the counter reaches zero. Reads from this register return the reload value programmed into this register 0b00000 Synchronization disabled. 0b00111 128 bytes 0b01000 256 bytes 0b11111 2^{31} bytes

3.9.2.8 CLAIMMASK Register (Offset = FA0h) [Reset = 00000000h]

CLAIMMASK is shown in Table 3-70.

Return to the Summary Table.

Claim Tag Mask

Table 3-70. CLAIMMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLAIMMASK	R	Fh	This register forms one half of the Claim Tag value. When reading this register returns the number of bits that can be set (each bit is considered separately): 0: This claim tag bit is not implemented 1: This claim tag bit is not implemented The behavior when writing to this register is described in CLAIMSET.

3.9.2.9 CLAIMSET Register (Offset = FA0h) [Reset = 00000000h]

CLAIMSET is shown in Table 3-71.

Return to the Summary Table.

Claim Tag Set

Table 3-71. CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLAIMSET	W	Fh	This register forms one half of the Claim Tag value. Writing to this location allows individual bits to be set (each bit is considered separately): 0: No effect 1: Set this bit in the claim tag The behavior when reading from this location is described in CLAIMMASK.

3.9.2.10 CLAIMTAG Register (Offset = FA4h) [Reset = 00000000h]

CLAIMTAG is shown in Table 3-72.

Return to the Summary Table.

Current Claim Tag

Table 3-72. CLAIMTAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLAIMTAG	R	0h	This register forms one half of the Claim Tag value. Reading this register returns the current Claim Tag value. Reading CLAIMMASK determines how many bits from this register must be used. The behavior when writing to this register is described in CLAIMCLR.

3.9.2.11 CLAIMCLR Register (Offset = FA4h) [Reset = 00000000h]

CLAIMCLR is shown in Table 3-73.

Return to the Summary Table.

Claim Tag Clear

Table 3-73. CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLAIMCLR	W	0h	This register forms one half of the Claim Tag value. Writing to this location enables individual bits to be cleared (each bit is considered separately): 0: No effect 1: Clear this bit in the claim tag. The behavior when reading from this location is described in CLAIMTAG.

3.9.2.12 DEVID Register (Offset = FC8h) [Reset = 00000000h]

DEVID is shown in Table 3-74.

Return to the Summary Table.

Device ID

Table 3-74. DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEVID	R	CA0h	This field returns: 0xCA1 if there is an ETM present. 0xCA0 if there is no ETM present.

3.9.3 DCB Registers

Table 3-75 lists the memory-mapped registers for the DCB registers. All register offset addresses not listed in Table 3-75 should be considered as reserved locations and the register contents should not be modified.

Table 3-75. DCB Registers

Offset	Acronym	Register Name	Section
10h	DHCSR	Controls halting debug	Section 3.9.3.1
14h	DCRSR	With the DCRDR, provides debug access to the general-purpose registers, special-purpose registers, and the FP extension registers. A write to the DCRSR specifies the register to transfer, whether the transfer is a read or write, and starts the transfer	Section 3.9.3.2
18h	DCRDR	With the DCRSR, provides debug access to the general-purpose registers, special-purpose registers, and the FP Extension registers. If the Main Extension is implemented, it can also be used for message passing between an external debugger and a debug agent running on the PE	Section 3.9.3.3
1Ch	DEMCR	Manages vector catch behavior and DebugMonitor handling when debugging	Section 3.9.3.4
24h	DAUTHCTRL	This register allows the external authentication interface to be overridden from software.	Section 3.9.3.5
28h	DSCSR	Provides control and status information for Secure debug	Section 3.9.3.6

Complex bit access types are encoded to fit into small table cells. Table 3-76 shows the codes that are used for access types in this section.

Table 3-76. DCB Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

3.9.3.1 DHCSR Register (Offset = 10h) [Reset = 00000000h]

DHCSR is shown in Table 3-77.

Return to the Summary Table.

Controls halting debug

Table 3-77. DHCSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RES0	R	0h	Reserved, RES0
26	S_RESTART_ST	R	0h	Indicates the PE has processed a request to clear DHCSR.C_HALT to 0. That is, either a write to DHCSR that clears DHCSR.C_HALT from 1 to 0, or an External Restart Request
25	S_RESET_ST	R	0h	Indicates whether the PE has been reset since the last read of the DHCSR
24	S_RETIRE_ST	R	0h	Set to 1 every time the PE retires one of more instructions
23-21	RES0_1	R	0h	Reserved, RES0
20	S_SDE	R	0h	Indicates whether Secure invasive debug is allowed
19	S_LOCKUP	R	0h	Indicates whether the PE is in Lockup state
18	S_SLEEP	R	0h	Indicates whether the PE is sleeping
17	S_HALT	R	0h	Indicates whether the PE is in Debug state
31-16	DBGKEY	W	0h	A debugger must write 0xA05F to this field to enable write access to the remaining bits, otherwise the PE ignores the write access
16	S_REGRDY	R	0h	Handshake flag to transfers through the DCRDR
15-6	RES0_2	R	0h	Reserved, RES0
5	C_SNAPSTALL	R/W	0h	Allow imprecise entry to Debug state
4	RES0_3	R	0h	Reserved, RES0
3	C_MASKINTS	R/W	0h	When debug is enabled, the debugger can write to this bit to mask PendSV, SysTick and external configurable interrupts
2	C_STEP	R/W	0h	Enable single instruction step
1	C_HALT	R/W	0h	PE enter Debug state halt request
0	C_DEBUGEN	R/W	0h	Enable Halting debug

3.9.3.2 DCRSR Register (Offset = 14h) [Reset = 00000000h]

DCRSR is shown in Table 3-78.

Return to the Summary Table.

With the DCRDR, provides debug access to the general-purpose registers, special-purpose registers, and the FP extension registers. A write to the DCRSR specifies the register to transfer, whether the transfer is a read or write, and starts the transfer

Table 3-78. DCRSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RES0	R	0h	Reserved, RES0
16	REGWnR	W	0h	Specifies the access type for the transfer
15-7	RES0_1	R	0h	Reserved, RES0
6-0	REGSEL	W	0h	Specifies the general-purpose register, special-purpose register, or FP register to transfer

3.9.3.3 DCRDR Register (Offset = 18h) [Reset = 00000000h]

DCRDR is shown in Table 3-79.

Return to the Summary Table.

With the DCRSR, provides debug access to the general-purpose registers, special-purpose registers, and the FP Extension registers. If the Main Extension is implemented, it can also be used for message passing between an external debugger and a debug agent running on the PE

Table 3-79. DCRDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DBGTMP	R/W	0h	Provides debug access for reading and writing the general-purpose registers, special-purpose registers, and Floating-point Extension registers

3.9.3.4 DEMCR Register (Offset = 1Ch) [Reset = 00000000h]

DEMCR is shown in Table 3-80.

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Manages vector catch behavior and DebugMonitor handling when debugging

Table 3-80. DEMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RES0	R	0h	Reserved, RES0
24	TRCENA	R/W	0h	Global enable for all DWT and ITM features
23-21	RES0_1	R	0h	Reserved, RES0
20	SDME	R	0h	Indicates whether the DebugMonitor targets the Secure or the Non-secure state and whether debug events are allowed in Secure state
19	MON_REQ	R/W	0h	DebugMonitor semaphore bit
18	MON_STEP	R/W	0h	Enable DebugMonitor stepping
17	MON_PEND	R/W	0h	Sets or clears the pending state of the DebugMonitor exception
16	MON_EN	R/W	0h	Enable the DebugMonitor exception
15-12	RES0_2	R	0h	Reserved, RES0
11	VC_SFERR	R/W	0h	SecureFault exception halting debug vector catch enable
10	VC_HARDERR	R/W	0h	HardFault exception halting debug vector catch enable
9	VC_INTERR	R/W	0h	Enable halting debug vector catch for faults during exception entry and return
8	VC_BUSERR	R/W	0h	BusFault exception halting debug vector catch enable
7	VC_STATERR	R/W	0h	Enable halting debug trap on a UsageFault exception caused by a state information error, for example an Undefined Instruction exception
6	VC_CHKERR	R/W	0h	Enable halting debug trap on a UsageFault exception caused by a checking error, for example an alignment check error
5	VC_NOCPERR	R/W	0h	Enable halting debug trap on a UsageFault caused by an access to a coprocessor
4	VC_MMERR	R/W	0h	Enable halting debug trap on a MemManage exception
3-1	RES0_3	R	0h	Reserved, RES0
0	VC_CORERESET	R/W	0h	Enable Reset Vector Catch. This causes a warm reset to halt a running system

3.9.3.5 DAUTHCTRL Register (Offset = 24h) [Reset = 00000000h]

DAUTHCTRL is shown in Table 3-81.

Return to the Summary Table.

This register allows the external authentication interface to be overridden from software.

Table 3-81. DAUTHCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	INTSPNIDEN	R/W	0h	Internal Secure non-invasive debug enable. Overrides the external Secure non-invasive debug authentication interface
2	SPNIDENSEL	R/W	0h	Secure non-invasive debug enable select. Selects between DAUTHCTRL and the external authentication interface for control of Secure non-invasive debug
1	INTSPIDEN	R/W	0h	Internal Secure invasive debug enable. Overrides the external Secure invasive debug authentication Interfaces.
0	SPIDENSEL	R/W	0h	Secure invasive debug enable select. Selects between DAUTHCTRL and the external authentication interface for control of Secure invasive debug.

3.9.3.6 DSCSR Register (Offset = 28h) [Reset = 00000000h]

DSCSR is shown in Table 3-82.

Return to the Summary Table.

Provides control and status information for Secure debug

Table 3-82. DSCSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RES0	R	0h	Reserved, RES0
17	CDSKEY	R/W	0h	Writes to the CDS bit are ignored unless CDSKEY is concurrently written to zero
16	CDS	R/W	0h	This field indicates the current Security state of the processor
15-2	RES0_1	R	0h	Reserved, RES0
1	SBRSEL	R/W	0h	If SBRSELEN is 1 this bit selects whether the Non-secure or the Secure version of the memory-mapped Banked registers are accessible to the debugger
0	SBRSELEN	R/W	0h	Controls whether the SBRSEL field or the current Security state of the processor selects which version of the memory-mapped Banked registers are accessed to the debugger

3.9.4 DIB Registers

Table 3-83 lists the memory-mapped registers for the DIB registers. All register offset addresses not listed in Table 3-83 should be considered as reserved locations and the register contents should not be modified.

Table 3-83. DIB Registers

Offset	Acronym	Register Name	Section
0h	DLAR	Provides CoreSight discovery information for the SCS	Section 3.9.4.1
4h	DLSR	Provides CoreSight discovery information for the SCS	Section 3.9.4.2
8h	DAUTHSTATUS	Provides CoreSight discovery information for the SCS	Section 3.9.4.3
Ch	DDEVARCH	Provides CoreSight discovery information for the SCS	Section 3.9.4.4
1Ch	DDEVTYPE	Provides CoreSight discovery information for the SCS	Section 3.9.4.5
20h	DPIDR4	Provides CoreSight discovery information for the SCS	Section 3.9.4.6
24h	DPIDR5	Provides CoreSight discovery information for the SCS	Section 3.9.4.7
28h	DPIDR6	Provides CoreSight discovery information for the SCS	Section 3.9.4.8
2Ch	DPIDR7	Provides CoreSight discovery information for the SCS	Section 3.9.4.9
30h	DPIDR0	Provides CoreSight discovery information for the SCS	Section 3.9.4.10
34h	DPIDR1	Provides CoreSight discovery information for the SCS	Section 3.9.4.11
38h	DPIDR2	Provides CoreSight discovery information for the SCS	Section 3.9.4.12
3Ch	DPIDR3	Provides CoreSight discovery information for the SCS	Section 3.9.4.13
40h	DCIDR0	Provides CoreSight discovery information for the SCS	Section 3.9.4.14
44h	DCIDR1	Provides CoreSight discovery information for the SCS	Section 3.9.4.15
48h	DCIDR2	Provides CoreSight discovery information for the SCS	Section 3.9.4.16
4Ch	DCIDR3	Provides CoreSight discovery information for the SCS	Section 3.9.4.17

Complex bit access types are encoded to fit into small table cells. Table 3-84 shows the codes that are used for access types in this section.

Table 3-84. DIB Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

3.9.4.1 DLAR Register (Offset = 0h) [Reset = 00000000h]

DLAR is shown in Table 3-85.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 3-85. DLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	KEY	R	0h	Indicates whether Non-secure invasive debug is allowed

3.9.4.2 DLSR Register (Offset = 4h) [Reset = 00000000h]

DLSR is shown in Table 3-86.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 3-86. DLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	08EE0540h	Defines the architect of the component. Bits [31:28] are the JEP106 continuation code (JEP106 bank ID, minus 1) and bits [27:21] are the JEP106 ID code.
2	nTT	R	1h	Indicates whether Secure invasive debug is implemented and allowed
1	SLK	R	0h	Indicates whether Non-secure non-invasive debug is allowed
0	SLI	R	0h	Indicates whether Non-secure invasive debug is allowed

3.9.4.3 DAUTHSTATUS Register (Offset = 8h) [Reset = 00000000h]

DAUTHSTATUS is shown in Table 3-87.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 3-87. DAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	047702A0h	Defines the architect of the component. Bits [31:28] are the JEP106 continuation code (JEP106 bank ID, minus 1) and bits [27:21] are the JEP106 ID code.
3	SNID	R	0h	Indicates whether Secure non-invasive debug is implemented and allowed
2	SID	R	1h	Indicates whether Secure invasive debug is implemented and allowed
1	NSNID	R	0h	Indicates whether Non-secure non-invasive debug is allowed
0	NSID	R	0h	Indicates whether Non-secure invasive debug is allowed

3.9.4.4 DDEVARCH Register (Offset = Ch) [Reset = 00000000h]

DDEVARCH is shown in Table 3-88.

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Provides CoreSight discovery information for the SCS

Table 3-88. DDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	ARCHITECT	R	23Bh	Defines the architect of the component. Bits [31:28] are the JEP106 continuation code (JEP106 bank ID, minus 1) and bits [27:21] are the JEP106 ID code.
20	PRESENT	R	1h	Defines that the DEVARCH register is present
19-16	REVISION	R	0h	Defines the architecture revision of the component
15-12	ARCHVER	R	2h	Defines the architecture version of the component
11-0	ARCHPART	R	A04h	Defines the architecture of the component

3.9.4.5 DDEVTYPE Register (Offset = 1Ch) [Reset = 00000000h]

DDEVTYPE is shown in Table 3-89.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 3-89. DDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	SUB	R	0h	Component sub-type
3-0	MAJOR	R	0h	CoreSight major type

3.9.4.6 DPIDR4 Register (Offset = 20h) [Reset = 00000000h]

DPIDR4 is shown in Table 3-90.

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Provides CoreSight discovery information for the SCS

Table 3-90. DPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	SIZE	R	0h	See CoreSight Architecture Specification
3-0	DES_2	R	4h	See CoreSight Architecture Specification

3.9.4.7 DPIDR5 Register (Offset = 24h) [Reset = 00000000h]

DPIDR5 is shown in Table 3-91.

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Provides CoreSight discovery information for the SCS

Table 3-91. DPIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

3.9.4.8 DPIDR6 Register (Offset = 28h) [Reset = 00000000h]

DPIDR6 is shown in Table 3-92.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 3-92. DPIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

3.9.4.9 DPIDR7 Register (Offset = 2Ch) [Reset = 00000000h]

DPIDR7 is shown in Table 3-93.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 3-93. DPIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

3.9.4.10 DPIDR0 Register (Offset = 30h) [Reset = 00000000h]

DPIDR0 is shown in Table 3-94.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 3-94. DPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PART_0	R	21h	See CoreSight Architecture Specification

3.9.4.11 DPIDR1 Register (Offset = 34h) [Reset = 00000000h]

DPIDR1 is shown in Table 3-95.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 3-95. DPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	DES_0	R	Bh	See CoreSight Architecture Specification
3-0	PART_1	R	Dh	See CoreSight Architecture Specification

3.9.4.12 DPIDR2 Register (Offset = 38h) [Reset = 00000000h]

DPIDR2 is shown in Table 3-96.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 3-96. DPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	REVISION	R	0h	See CoreSight Architecture Specification
3	JEDEC	R	1h	See CoreSight Architecture Specification
2-0	DES_1	R	3h	See CoreSight Architecture Specification

3.9.4.13 DPIDR3 Register (Offset = 3Ch) [Reset = 00000000h]

DPIDR3 is shown in Table 3-97.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 3-97. DPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	REVAND	R	0h	See CoreSight Architecture Specification
3-0	CMOD	R	0h	See CoreSight Architecture Specification

3.9.4.14 DCIDR0 Register (Offset = 40h) [Reset = 00000000h]

DCIDR0 is shown in Table 3-98.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 3-98. DCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PRMBL_0	R	Dh	See CoreSight Architecture Specification

3.9.4.15 DCIDR1 Register (Offset = 44h) [Reset = 00000000h]

DCIDR1 is shown in Table 3-99.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 3-99. DCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	CLASS	R	9h	See CoreSight Architecture Specification
3-0	PRMBL_1	R	0h	See CoreSight Architecture Specification

3.9.4.16 DCIDR2 Register (Offset = 48h) [Reset = 00000000h]

DCIDR2 is shown in Table 3-100.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 3-100. DCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PRMBL_2	R	5h	See CoreSight Architecture Specification

3.9.4.17 DCIDR3 Register (Offset = 4Ch) [Reset = 00000000h]

DCIDR3 is shown in Table 3-101.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 3-101. DCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PRMBL_3	R	B1h	See CoreSight Architecture Specification

3.9.5 DWT Registers

Table 3-102 lists the memory-mapped registers for the DWT registers. All register offset addresses not listed in Table 3-102 should be considered as reserved locations and the register contents should not be modified.

Table 3-102. DWT Registers

Offset	Acronym	Register Name	Section
0h	DWT Control Register	Provides configuration and status information for the DWT unit, and used to control features of the unit	Section 3.9.5.1
4h	DWT Cycle Count Register	Shows or sets the value of the processor cycle counter, CYCCNT	Section 3.9.5.2
8h	DWT CPI Count Register	Counts additional cycles required to execute multicycle instructions and instruction fetch stalls.	Section 3.9.5.3
Ch	DWT Exception Overhead Count Register	Counts the total cycles spent in exception processing	Section 3.9.5.4
10h	DWT Sleep Count Register	Counts the total number of cycles that the processor is sleeping.	Section 3.9.5.5
14h	DWT LSU Count Register	Increments on the additional cycles required to execute all load or store instructions	Section 3.9.5.6
18h	DWT Folded Instruction Count Register	Increments on the additional cycles required to execute all load or store instructions	Section 3.9.5.7
1Ch	DWT Program Counter Sample Register	Samples the current value of the Program Counter.	Section 3.9.5.8
20h	DWT Comparator Register 0	Provides a reference value for use by watchpoint comparator 0	Section 3.9.5.9
28h	DWT Comparator Function Register 0	Controls the operation of watchpoint comparator 0	Section 3.9.5.10
30h	DWT Comparator Register 1	Provides a reference value for use by watchpoint comparator 1	Section 3.9.5.11
38h	DWT Comparator Function Register 1	Controls the operation of watchpoint comparator 1	Section 3.9.5.12
40h	DWT Comparator Register 2	Provides a reference value for use by watchpoint comparator 2	Section 3.9.5.13
48h	DWT Comparator Function Register 2	Controls the operation of watchpoint comparator 2	Section 3.9.5.14
50h	DWT Comparator Register 3	Provides a reference value for use by watchpoint comparator 3	Section 3.9.5.15
58h	DWT Comparator Function Register 3	Controls the operation of watchpoint comparator 3	Section 3.9.5.16
FBCh	DWT Device Architecture Register	Provides CoreSight discovery information for the DWT	Section 3.9.5.17
FCCh	DWT Device Type Register	Provides CoreSight discovery information for the DWT	Section 3.9.5.18
FD0h	DWT Peripheral Identification Register 4	Provides CoreSight discovery information for the DWT	Section 3.9.5.19
FD4h	DWT Peripheral Identification Register 5	Provides CoreSight discovery information for the DWT	Section 3.9.5.20
FD8h	DWT Peripheral Identification Register 6	Provides CoreSight discovery information for the DWT	Section 3.9.5.21
FDCh	DWT Peripheral Identification Register 7	Provides CoreSight discovery information for the DWT	Section 3.9.5.22
FE0h	DWT Peripheral Identification Register 0	Provides CoreSight discovery information for the DWT	Section 3.9.5.23
FE4h	DWT Peripheral Identification Register 1	Provides CoreSight discovery information for the DWT	Section 3.9.5.24
FE8h	DWT Peripheral Identification Register 2	Provides CoreSight discovery information for the DWT	Section 3.9.5.25
FECh	DWT Peripheral Identification Register 3	Provides CoreSight discovery information for the DWT	Section 3.9.5.26
FF0h	DWT Component Identification Register 0	Provides CoreSight discovery information for the DWT	Section 3.9.5.27
FF4h	DWT Component Identification Register 1	Provides CoreSight discovery information for the DWT	Section 3.9.5.28
FF8h	DWT Component Identification Register 2	Provides CoreSight discovery information for the DWT	Section 3.9.5.29
FFCh	DWT Component Identification Register 3	Provides CoreSight discovery information for the DWT	Section 3.9.5.30

Complex bit access types are encoded to fit into small table cells. Table 3-103 shows the codes that are used for access types in this section.

Table 3-103. DWT Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

3.9.5.1 DWT Control Register (Offset = 0h) [Reset = 02000000h]

DWT Control Register is shown in Table 3-104.

Return to the Summary Table.

Provides configuration and status information for the DWT unit, and used to control features of the unit

Table 3-104. DWT Control Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	Number of comparators	R	0h	Number of DWT comparators implemented
27	No trace packets	R	0h	Indicates whether the implementation does not support trace
26	RESERVED	R	0h	Reserved, RAZ
25	No cycle count	R	1h	Indicates whether the implementation does not include a cycle counter
24	No profile counters	R	0h	Indicates whether the implementation does not include the profiling counters
23	Cycle counter disabled secure	R/W	0h	Controls whether the cycle counter is disabled in Secure state
22	Cycle event enable	R/W	0h	Enables Event Counter packet generation on POSTCNT underflow
21	Fold event enable	R/W	0h	Enables DWT_FOLDCNT counter
20	LSU event enable	R/W	0h	Enables DWT_LSUCNT counter
19	Sleep event enable	R/W	0h	Enable DWT_SLEEPCNT counter
18	Exception event enable	R/W	0h	Enables DWT_EXCCNT counter
17	CPI event enable	R/W	0h	Enables DWT_CPICNT counter
16	Exception trace enable	R/W	0h	Enables generation of Exception Trace packets
15-13	RESERVED	R	0h	Reserved, RES0
12	PC sample enable	R/W	0h	Enables use of POSTCNT counter as a timer for Periodic PC Sample packet generation
11-10	Synchronization tap	R/W	0h	Selects the position of the synchronization packet counter tap on the CYCCNT counter. This determines the Synchronization packet rate
9	Cycle count tap	R/W	0h	Selects the position of the POSTCNT tap on the CYCCNT counter
8-5	POSTCNT initial	R/W	0h	Initial value for the POSTCNT counter
4-1	POSTCNT preset	R/W	0h	Reload value for the POSTCNT counter
0	CYCCNT enable	R/W	0h	Enables CYCCNT

3.9.5.2 DWT Cycle Count Register (Offset = 4h) [Reset = 00000000h]

DWT Cycle Count Register is shown in Table 3-105.

Return to the Summary Table.

Shows or sets the value of the processor cycle counter, CYCCNT

Table 3-105. DWT Cycle Count Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Incrementing cycle counter value	R/W	0h	Increments one on each processor clock cycle when DWT_CTRL.CYCCNTENA == 1 and DEMCR.TRCENA == 1. On overflow, CYCCNT wraps to zero

3.9.5.3 DWT CPI Count Register (Offset = 8h) [Reset = 00000000h]

DWT CPI Count Register is shown in Table 3-106.

Return to the Summary Table.

Counts additional cycles required to execute multicycle instructions and instruction fetch stalls.

Table 3-106. DWT CPI Count Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	Base instruction overhead counter	R/W	0h	Counts one on each cycle when all of the following are true: - DWT_CTRL.CPIEVTENA == 1 and DEMCR.TRCENA == 1. - No instruction is executed. - No load-store operation is in progress, see DWT_LSUCNT. - No exception-entry or exception-exit operation is in progress, see DWT_EXCCNT. - The PE is not in a power saving mode, see DWT_SLEEPCNT. - Either SecureNoninvasiveDebugAllowed() == TRUE, or the PE is in Non-secure state and NoninvasiveDebugAllowed() == TRUE.

3.9.5.4 DWT Exception Overhead Count Register (Offset = Ch) [Reset = 00000000h]

DWT Exception Overhead Count Register is shown in Table 3-107.

Return to the Summary Table.

Counts the total cycles spent in exception processing

Table 3-107. DWT Exception Overhead Count Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	The exception overhead counter	R/W	0h	Counts one on each cycle when all of the following are true: - DWT_CTRL.EXCEVTENA == 1 and DEMCR.TRCENA == 1. - No instruction is executed, see DWT_CPICNT. - An exception-entry or exception-exit related operation is in progress. - Either SecureNoninvasiveDebugAllowed() == TRUE, or NS-Req for the operation is set to Non-secure and NoninvasiveDebugAllowed() == TRUE.

3.9.5.5 DWT Sleep Count Register (Offset = 10h) [Reset = 00000000h]

DWT Sleep Count Register is shown in Table 3-108.

Return to the Summary Table.

Counts the total number of cycles that the processor is sleeping.

Table 3-108. DWT Sleep Count Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	Sleep counter	R/W	0h	Counts one on each cycle when all of the following are true: - DWT_CTRL.SLEEPEVTENA == 1 and DEMCR.TRCENA == 1. - No instruction is executed, see DWT_CPICNT. - No load-store operation is in progress, see DWT_LSUCNT. - No exception-entry or exception-exit operation is in progress, see DWT_EXCCNT. - The PE is in a power saving mode. - Either SecureNoninvasiveDebugAllowed() == TRUE, or the PE is in Non-secure state and NoninvasiveDebugAllowed() == TRUE.

3.9.5.6 DWT LSU Count Register (Offset = 14h) [Reset = 00000000h]

DWT LSU Count Register is shown in Table 3-109.

Return to the Summary Table.

Increments on the additional cycles required to execute all load or store instructions

Table 3-109. DWT LSU Count Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	Load-store overhead counter	R/W	0h	Counts one on each cycle when all of the following are true: - DWT_CTRL.LSUEVTENA == 1 and DEMCR.TRCENA == 1. - No instruction is executed, see DWT_CPICNT. - No exception-entry or exception-exit operation is in progress, see DWT_EXCCNT. - A load-store operation is in progress. - Either SecureNoninvasiveDebugAllowed() == TRUE, or NS-Req for the operation is set to Non-secure and NoninvasiveDebugAllowed() == TRUE.

3.9.5.7 DWT Folded Instruction Count Register (Offset = 18h) [Reset = 00000000h]

DWT Folded Instruction Count Register is shown in Table 3-110.

Return to the Summary Table.

Increments on the additional cycles required to execute all load or store instructions

Table 3-110. DWT Folded Instruction Count Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	Folded instruction counter	R/W	0h	Counts on each cycle when all of the following are true: - DWT_CTRL.FOLDEVTENA == 1 and DEMCR.TRCENA == 1. - At least two instructions are executed, see DWT_CPICNT. - Either SecureNoninvasiveDebugAllowed() == TRUE, or the PE is in Non-secure state and NoninvasiveDebugAllowed() == TRUE. The counter is incremented by the number of instructions executed, minus one

3.9.5.8 DWT Program Counter Sample Register (Offset = 1Ch) [Reset = 00000000h]

DWT Program Counter Sample Register is shown in Table 3-111.

Return to the Summary Table.

Samples the current value of the Program Counter.

Table 3-111. DWT Program Counter Sample Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Executed instruction address sample. Recently executed instruction address sample value	R	0h	The possible values of this field are: 0xFFFFFFFF One of the following is true: - The PE is halted in Debug state. - The Security Extension is implemented, the sampled instruction was executed in Secure state, and SecureNoninvasiveDebugAllowed() == FALSE. - NoninvasiveDebugAllowed() == FALSE. - DEMCR.TRCENA == 0. - The address of a recently-executed instruction is not available. Not 0xFFFFFFFF Instruction address of a recently executed instruction. Bit [0] of the sample instruction address is 0.

3.9.5.9 DWT Comparator Register 0 (Offset = 20h) [Reset = 00000000h]

DWT Comparator Register 0 is shown in Table 3-112.

Return to the Summary Table.

Provides a reference value for use by watchpoint comparator 0

Table 3-112. DWT Comparator Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Cycle, PC, address or data value	R/W	0h	Reference value for comparison. Behaviour depends on the value of DWT_FUNCTIONn.MATCH

3.9.5.10 DWT Comparator Function Register 0 (Offset = 28h) [Reset = 58000000h]

DWT Comparator Function Register 0 is shown in Table 3-113.

Return to the Summary Table.

Controls the operation of watchpoint comparator 0

Table 3-113. DWT Comparator Function Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Identify capability	R	Bh	Identifies the capabilities for MATCH for comparator *n
26-25	RESERVED	R	0h	Reserved, RES0
24	Comparator matched	RC	0h	Set to 1 when the comparator matches
23-12	RESERVED	R	0h	Reserved, RES0
11-10	Data value size	R/W	0h	Defines the size of the object being watched for by Data Value and Data Address comparators
9-6	RESERVED	R	0h	Reserved, RES0
5-4	Action on match	R/W	0h	Defines the action on a match. This field is ignored and the comparator generates no actions if it is disabled by MATCH
3-0	Match type	R/W	0h	Controls the type of match generated by this comparator

3.9.5.11 DWT Comparator Register 1 (Offset = 30h) [Reset = 00000000h]

DWT Comparator Register 1 is shown in Table 3-114.

Return to the Summary Table.

Provides a reference value for use by watchpoint comparator 1

Table 3-114. DWT Comparator Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Cycle, PC, address or data value	R/W	0h	Reference value for comparison. Behaviour depends on the value of DWT_FUNCTIONn.MATCH

3.9.5.12 DWT Comparator Function Register 1 (Offset = 38h) [Reset = D0000000h]

DWT Comparator Function Register 1 is shown in Table 3-115.

Return to the Summary Table.

Controls the operation of watchpoint comparator 1

Table 3-115. DWT Comparator Function Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Identify capability	R	1Ah	Identifies the capabilities for MATCH for comparator *n
26-25	RESERVED	R	0h	Reserved, RES0
24	Comparator matched	RC	0h	Set to 1 when the comparator matches
23-12	RESERVED	R	0h	Reserved, RES0
11-10	Data value size	R/W	0h	Defines the size of the object being watched for by Data Value and Data Address comparators
9-6	RESERVED	R	0h	Reserved, RES0
5-4	Action on match	R/W	0h	Defines the action on a match. This field is ignored and the comparator generates no actions if it is disabled by MATCH
3-0	Match type	R/W	0h	Controls the type of match generated by this comparator

3.9.5.13 DWT Comparator Register 2 (Offset = 40h) [Reset = 00000000h]

DWT Comparator Register 2 is shown in Table 3-116.

Return to the Summary Table.

Provides a reference value for use by watchpoint comparator 2

Table 3-116. DWT Comparator Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Cycle, PC, address or data value	R/W	0h	Reference value for comparison. Behaviour depends on the value of DWT_FUNCTIONn.MATCH

3.9.5.14 DWT Comparator Function Register 2 (Offset = 48h) [Reset = 50000000h]

DWT Comparator Function Register 2 is shown in Table 3-117.

Return to the Summary Table.

Controls the operation of watchpoint comparator 2

Table 3-117. DWT Comparator Function Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Identify capability	R	Ah	Identifies the capabilities for MATCH for comparator *n
26-25	RESERVED	R	0h	Reserved, RES0
24	Comparator matched	RC	0h	Set to 1 when the comparator matches
23-12	RESERVED	R	0h	Reserved, RES0
11-10	Data value size	R/W	0h	Defines the size of the object being watched for by Data Value and Data Address comparators
9-6	RESERVED	R	0h	Reserved, RES0
5-4	Action on match	R/W	0h	Defines the action on a match. This field is ignored and the comparator generates no actions if it is disabled by MATCH
3-0	Match type	R/W	0h	Controls the type of match generated by this comparator

3.9.5.15 DWT Comparator Register 3 (Offset = 50h) [Reset = 00000000h]

DWT Comparator Register 3 is shown in Table 3-118.

Return to the Summary Table.

Provides a reference value for use by watchpoint comparator 3

Table 3-118. DWT Comparator Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Cycle, PC, address or data value	R/W	0h	Reference value for comparison. Behaviour depends on the value of DWT_FUNCTIONn.MATCH

3.9.5.16 DWT Comparator Function Register 3 (Offset = 58h) [Reset = 50000000h]

DWT Comparator Function Register 3 is shown in Table 3-119.

Return to the Summary Table.

Controls the operation of watchpoint comparator 3

Table 3-119. DWT Comparator Function Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Identify capability	R	Ah	Identifies the capabilities for MATCH for comparator *n
26-25	RESERVED	R	0h	Reserved, RES0
24	Comparator matched	RC	0h	Set to 1 when the comparator matches
23-12	RESERVED	R	0h	Reserved, RES0
11-10	Data value size	R/W	0h	Defines the size of the object being watched for by Data Value and Data Address comparators
9-6	RESERVED	R	0h	Reserved, RES0
5-4	Action on match	R/W	0h	Defines the action on a match. This field is ignored and the comparator generates no actions if it is disabled by MATCH
3-0	Match type	R/W	0h	Controls the type of match generated by this comparator

3.9.5.17 DWT Device Architecture Register (Offset = FBCh) [Reset = 47701A02h]

DWT Device Architecture Register is shown in Table 3-120.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 3-120. DWT Device Architecture Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	Architect	R	23Bh	Defines the architect of the component. Bits [31:28] are the JEP106 continuation code (JEP106 bank ID, minus 1) and bits [27:21] are the JEP106 ID code.
20	DEVARCH Present	R	1h	Defines that the DEVARCH register is present
19-16	Revision	R	0h	Defines the architecture revision of the component
15-12	Architecture Version	R	1h	Defines the architecture version of the component
11-0	Architecture Part	R	A02h	Defines the architecture of the component

3.9.5.18 DWT Device Type Register (Offset = FCCh) [Reset = 00000000h]

DWT Device Type Register is shown in Table 3-121.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 3-121. DWT Device Type Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	Sub-type	R	0h	Component sub-type
3-0	Major type	R	0h	Component major type

3.9.5.19 DWT Peripheral Identification Register 4 (Offset = FD0h) [Reset = 00000004h]

DWT Peripheral Identification Register 4 is shown in Table 3-122.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 3-122. DWT Peripheral Identification Register 4 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	4KB count	R	0h	See CoreSight Architecture Specification
3-0	JEP106 continuation code	R	4h	See CoreSight Architecture Specification

3.9.5.20 DWT Peripheral Identification Register 5 (Offset = FD4h) [Reset = 00000000h]

DWT Peripheral Identification Register 5 is shown in Table 3-123.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 3-123. DWT Peripheral Identification Register 5 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved, RES0

3.9.5.21 DWT Peripheral Identification Register 6 (Offset = FD8h) [Reset = 00000000h]

DWT Peripheral Identification Register 6 is shown in Table 3-124.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 3-124. DWT Peripheral Identification Register 6 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved, RES0

3.9.5.22 DWT Peripheral Identification Register 7 (Offset = FDCh) [Reset = 00000000h]

DWT Peripheral Identification Register 7 is shown in Table 3-125.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 3-125. DWT Peripheral Identification Register 7 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved, RES0

3.9.5.23 DWT Peripheral Identification Register 0 (Offset = FE0h) [Reset = 00000021h]

DWT Peripheral Identification Register 0 is shown in Table 3-126.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 3-126. DWT Peripheral Identification Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	Part number bits [7:0]	R	21h	See CoreSight Architecture Specification

3.9.5.24 DWT Peripheral Identification Register 1 (Offset = FE4h) [Reset = 000000BDh]

DWT Peripheral Identification Register 1 is shown in Table 3-127.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 3-127. DWT Peripheral Identification Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	JEP106 identification code bits [3:0]	R	Bh	See CoreSight Architecture Specification
3-0	Part number bits [11:8]	R	Dh	See CoreSight Architecture Specification

3.9.5.25 DWT Peripheral Identification Register 2 (Offset = FE8h) [Reset = 0000000Bh]

DWT Peripheral Identification Register 2 is shown in Table 3-128.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 3-128. DWT Peripheral Identification Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	Component revision	R	0h	See CoreSight Architecture Specification
3	JEDEC assignee value is used	R	1h	See CoreSight Architecture Specification
2-0	JEP106 identification code bits [6:4]	R	3h	See CoreSight Architecture Specification

3.9.5.26 DWT Peripheral Identification Register 3 (Offset = FECh) [Reset = 00000000h]

DWT Peripheral Identification Register 3 is shown in Table 3-129.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 3-129. DWT Peripheral Identification Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	RevAnd	R	0h	See CoreSight Architecture Specification
3-0	Customer Modified	R	0h	See CoreSight Architecture Specification

3.9.5.27 DWT Component Identification Register 0 (Offset = FF0h) [Reset = 0000000Dh]

DWT Component Identification Register 0 is shown in Table 3-130.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 3-130. DWT Component Identification Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	CoreSight component identification preamble	R	Dh	See CoreSight Architecture Specification

3.9.5.28 DWT Component Identification Register 1 (Offset = FF4h) [Reset = 00000090h]

DWT Component Identification Register 1 is shown in Table 3-131.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 3-131. DWT Component Identification Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	CoreSight component class	R	9h	See CoreSight Architecture Specification
3-0	CoreSight component identification preamble	R	0h	See CoreSight Architecture Specification

3.9.5.29 DWT Component Identification Register 2 (Offset = FF8h) [Reset = 00000005h]

DWT Component Identification Register 2 is shown in Table 3-132.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 3-132. DWT Component Identification Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	CoreSight component identification preamble	R	5h	See CoreSight Architecture Specification

3.9.5.30 DWT Component Identification Register 3 (Offset = FFCh) [Reset = 000000B1h]

DWT Component Identification Register 3 is shown in Table 3-133.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 3-133. DWT Component Identification Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	CoreSight component identification preamble	R	B1h	See CoreSight Architecture Specification

3.9.6 FPB Registers

Table 3-134 lists the memory-mapped registers for the FPB registers. All register offset addresses not listed in Table 3-134 should be considered as reserved locations and the register contents should not be modified.

Table 3-134. FPB Registers

Offset	Acronym	Register Name	Section
0h	FP_CTRL	Provides FPB implementation information, and the global enable for the FPB unit	Section 3.9.6.1
4h	FP_REMAP	Indicates whether the implementation supports Flash Patch remap and, if it does, holds the target address for remap	Section 3.9.6.2
8h	FP_COMP0	Holds an address for comparison.	Section 3.9.6.3
Ch	FP_COMP1	Holds an address for comparison.	Section 3.9.6.4
10h	FP_COMP2	Holds an address for comparison.	Section 3.9.6.5
14h	FP_COMP3	Holds an address for comparison.	Section 3.9.6.6
18h	FP_COMP4	Holds an address for comparison.	Section 3.9.6.7
1Ch	FP_COMP5	Holds an address for comparison.	Section 3.9.6.8
20h	FP_COMP6	Holds an address for comparison.	Section 3.9.6.9
24h	FP_COMP7	Holds an address for comparison.	Section 3.9.6.10
FBCh	FP_DEVARCH	Provides CoreSight discovery information for the FPB	Section 3.9.6.11
FCCh	FP_DEVTYPE	Provides CoreSight discovery information for the FPB	Section 3.9.6.12
FD0h	FP_PIDR4	Provides CoreSight discovery information for the FP	Section 3.9.6.13
FD4h	FP_PIDR5	Provides CoreSight discovery information for the FP	Section 3.9.6.14
FD8h	FP_PIDR6	Provides CoreSight discovery information for the FP	Section 3.9.6.15
FDCh	FP_PIDR7	Provides CoreSight discovery information for the FP	Section 3.9.6.16
FE0h	FP_PIDR0	Provides CoreSight discovery information for the FP	Section 3.9.6.17
FE4h	FP_PIDR1	Provides CoreSight discovery information for the FP	Section 3.9.6.18
FE8h	FP_PIDR2	Provides CoreSight discovery information for the FP	Section 3.9.6.19
FECh	FP_PIDR3	Provides CoreSight discovery information for the FP	Section 3.9.6.20
FF0h	FP_CIDR0	Provides CoreSight discovery information for the FP	Section 3.9.6.21
FF4h	FP_CIDR1	Provides CoreSight discovery information for the FP	Section 3.9.6.22
FF8h	FP_CIDR2	Provides CoreSight discovery information for the FP	Section 3.9.6.23
FFCh	FP_CIDR3	Provides CoreSight discovery information for the FP	Section 3.9.6.24

Complex bit access types are encoded to fit into small table cells. Table 3-135 shows the codes that are used for access types in this section.

Table 3-135. FPB Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

3.9.6.1 FP_CTRL Register (Offset = 0h) [Reset = 00000000h]

FP_CTRL is shown in Table 3-136.

Return to the Summary Table.

Provides FPB implementation information, and the global enable for the FPB unit

Table 3-136. FP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	REV	R	1h	Flash Patch and Breakpoint Unit architecture revision
27-15	RES0	R	0h	Reserved, RES0
14-12	NUM_CODE_14_12_	R	0h	Indicates the number of implemented instruction address comparators. Zero indicates no Instruction Address comparators are implemented. The Instruction Address comparators are numbered from 0 to NUM_CODE - 1
11-8	NUM_LIT	R	0h	Indicates the number of implemented literal address comparators. The Literal Address comparators are numbered from NUM_CODE to NUM_CODE + NUM_LIT - 1
7-4	NUM_CODE_7_4_	R	8h	Indicates the number of implemented instruction address comparators. Zero indicates no Instruction Address comparators are implemented. The Instruction Address comparators are numbered from 0 to NUM_CODE - 1
3-2	RES0_1	R	0h	Reserved, RES0
1	KEY	R/W	0h	Writes to the FP_CTRL are ignored unless KEY is concurrently written to one
0	ENABLE	R/W	0h	Enables the FPB

3.9.6.2 FP_REMAP Register (Offset = 4h) [Reset = 00000000h]

FP_REMAP is shown in Table 3-137.

Return to the Summary Table.

Indicates whether the implementation supports Flash Patch remap and, if it does, holds the target address for remap

Table 3-137. FP_REMAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RES0	R	0h	Reserved, RES0
29	RMPSPT	R	0h	Indicates whether the FPB unit supports the Flash Patch remap function
28-5	REMAP	R	Xh	Holds the bits[28:5] of the Flash Patch remap address
4-0	RES0_1	R	0h	Reserved, RES0

3.9.6.3 FP_COMP0 Register (Offset = 8h) [Reset = 00000000h]

FP_COMP0 is shown in Table 3-138.

Return to the Summary Table.

Holds an address for comparison.

Table 3-138. FP_COMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	BPADDR	R/W	0h	Specifies bits[31:1] of the breakpoint instruction address
0	BE	R/W	0h	Selects between remapping and breakpoint functionality

3.9.6.4 FP_COMP1 Register (Offset = Ch) [Reset = 00000000h]

FP_COMP1 is shown in Table 3-139.

Return to the Summary Table.

Holds an address for comparison.

Table 3-139. FP_COMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	BPADDR	R/W	0h	Specifies bits[31:1] of the breakpoint instruction address
0	BE	R/W	0h	Selects between remapping and breakpoint functionality

3.9.6.5 FP_COMP2 Register (Offset = 10h) [Reset = 00000000h]

FP_COMP2 is shown in Table 3-140.

Return to the Summary Table.

Holds an address for comparison.

Table 3-140. FP_COMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	BPADDR	R/W	0h	Specifies bits[31:1] of the breakpoint instruction address
0	BE	R/W	0h	Selects between remapping and breakpoint functionality

3.9.6.6 FP_COMP3 Register (Offset = 14h) [Reset = 00000000h]

FP_COMP3 is shown in Table 3-141.

Return to the Summary Table.

Holds an address for comparison.

Table 3-141. FP_COMP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	BPADDR	R/W	0h	Specifies bits[31:1] of the breakpoint instruction address
0	BE	R/W	0h	Selects between remapping and breakpoint functionality

3.9.6.7 FP_COMP4 Register (Offset = 18h) [Reset = 00000000h]

FP_COMP4 is shown in Table 3-142.

Return to the Summary Table.

Holds an address for comparison.

Table 3-142. FP_COMP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	BPADDR	R/W	0h	Specifies bits[31:1] of the breakpoint instruction address
0	BE	R/W	0h	Selects between remapping and breakpoint functionality

3.9.6.8 FP_COMP5 Register (Offset = 1Ch) [Reset = 00000000h]

FP_COMP5 is shown in Table 3-143.

Return to the Summary Table.

Holds an address for comparison.

Table 3-143. FP_COMP5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	BPADDR	R/W	0h	Specifies bits[31:1] of the breakpoint instruction address
0	BE	R/W	0h	Selects between remapping and breakpoint functionality

3.9.6.9 FP_COMP6 Register (Offset = 20h) [Reset = 00000000h]

FP_COMP6 is shown in Table 3-144.

Return to the Summary Table.

Holds an address for comparison.

Table 3-144. FP_COMP6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	BPADDR	R/W	0h	Specifies bits[31:1] of the breakpoint instruction address
0	BE	R/W	0h	Selects between remapping and breakpoint functionality

3.9.6.10 FP_COMP7 Register (Offset = 24h) [Reset = 00000000h]

FP_COMP7 is shown in Table 3-145.

Return to the Summary Table.

Holds an address for comparison.

Table 3-145. FP_COMP7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	BPADDR	R/W	0h	Specifies bits[31:1] of the breakpoint instruction address
0	BE	R/W	0h	Selects between remapping and breakpoint functionality

3.9.6.11 FP_DEVARCH Register (Offset = FBCh) [Reset = 00000000h]

FP_DEVARCH is shown in Table 3-146.

Return to the Summary Table.

Provides CoreSight discovery information for the FPB

Table 3-146. FP_DEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	ARCHITECT	R	23Bh	Defines the architect of the component. Bits [31:28] are the JEP106 continuation code (JEP106 bank ID, minus 1) and bits [27:21] are the JEP106 ID code.
20	PRESENT	R	1h	Defines that the DEVARCH register is present
19-16	REVISION	R	0h	Defines the architecture revision of the component
15-12	ARCHVER	R	1h	Defines the architecture version of the component
11-0	ARCHPART	R	A03h	Defines the architecture of the component

3.9.6.12 FP_DEVTYPE Register (Offset = FCCh) [Reset = 00000000h]

FP_DEVTYPE is shown in Table 3-147.

Return to the Summary Table.

Provides CoreSight discovery information for the FPB

Table 3-147. FP_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	SUB	R	0h	Component sub-type
3-0	MAJOR	R	0h	Component major type

3.9.6.13 FP_PIDR4 Register (Offset = FD0h) [Reset = 00000000h]

FP_PIDR4 is shown in Table 3-148.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 3-148. FP_PIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	SIZE	R	0h	See CoreSight Architecture Specification
3-0	DES_2	R	4h	See CoreSight Architecture Specification

3.9.6.14 FP_PIDR5 Register (Offset = FD4h) [Reset = 00000000h]

FP_PIDR5 is shown in Table 3-149.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 3-149. FP_PIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

3.9.6.15 FP_PIDR6 Register (Offset = FD8h) [Reset = 00000000h]

FP_PIDR6 is shown in Table 3-150.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 3-150. FP_PIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

3.9.6.16 FP_PIDR7 Register (Offset = FDCh) [Reset = 00000000h]

FP_PIDR7 is shown in Table 3-151.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 3-151. FP_PIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

3.9.6.17 FP_PIDR0 Register (Offset = FE0h) [Reset = 00000000h]

FP_PIDR0 is shown in Table 3-152.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 3-152. FP_PIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PART_0	R	21h	See CoreSight Architecture Specification

3.9.6.18 FP_PIDR1 Register (Offset = FE4h) [Reset = 00000000h]

FP_PIDR1 is shown in Table 3-153.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 3-153. FP_PIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	DES_0	R	Bh	See CoreSight Architecture Specification
3-0	PART_1	R	Dh	See CoreSight Architecture Specification

3.9.6.19 FP_PIDR2 Register (Offset = FE8h) [Reset = 00000000h]

FP_PIDR2 is shown in Table 3-154.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 3-154. FP_PIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	REVISION	R	0h	See CoreSight Architecture Specification
3	JEDEC	R	1h	See CoreSight Architecture Specification
2-0	DES_1	R	3h	See CoreSight Architecture Specification

3.9.6.20 FP_PIDR3 Register (Offset = FECh) [Reset = 00000000h]

FP_PIDR3 is shown in Table 3-155.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 3-155. FP_PIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	REVAND	R	0h	See CoreSight Architecture Specification
3-0	CMOD	R	0h	See CoreSight Architecture Specification

3.9.6.21 FP_CIDR0 Register (Offset = FF0h) [Reset = 00000000h]

FP_CIDR0 is shown in Table 3-156.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 3-156. FP_CIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PRMBL_0	R	Dh	See CoreSight Architecture Specification

3.9.6.22 FP_CIDR1 Register (Offset = FF4h) [Reset = 00000000h]

FP_CIDR1 is shown in Table 3-157.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 3-157. FP_CIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	CLASS	R	9h	See CoreSight Architecture Specification
3-0	PRMBL_1	R	0h	See CoreSight Architecture Specification

3.9.6.23 FP_CIDR2 Register (Offset = FF8h) [Reset = 00000000h]

FP_CIDR2 is shown in Table 3-158.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 3-158. FP_CIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PRMBL_2	R	5h	See CoreSight Architecture Specification

3.9.6.24 FP_CIDR3 Register (Offset = FFCh) [Reset = 00000000h]

FP_CIDR3 is shown in Table 3-159.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 3-159. FP_CIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PRMBL_3	R	B1h	See CoreSight Architecture Specification

3.9.7 FPE Registers

Table 3-160 lists the memory-mapped registers for the FPE registers. All register offset addresses not listed in Table 3-160 should be considered as reserved locations and the register contents should not be modified.

Table 3-160. FPE Registers

Offset	Acronym	Register Name	Section
4h	FPCCR	Holds control data for the Floating-point extension	Section 3.9.7.1
8h	FPCAR	Holds the location of the unpopulated floating-point register space allocated on an exception stack frame	Section 3.9.7.2
Ch	FPDSCR	Holds the default values for the floating-point status control data that the PE assigns to the FPSCR when it creates a new floating-point context	Section 3.9.7.3
10h	MVFR0	Describes the features provided by the Floating-point Extension	Section 3.9.7.4
14h	MVFR1	Describes the features provided by the Floating-point Extension	Section 3.9.7.5
18h	MVFR2	Describes the features provided by the Floating-point Extension	Section 3.9.7.6

Complex bit access types are encoded to fit into small table cells. Table 3-161 shows the codes that are used for access types in this section.

Table 3-161. FPE Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

3.9.7.1 FPCCR Register (Offset = 4h) [Reset = 00000000h]

FPCCR is shown in Table 3-162.

Return to the Summary Table.

Holds control data for the Floating-point extension

Table 3-162. FPCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ASPEN	R/W	1h	When this bit is set to 1, execution of a floating-point instruction sets the CONTROL.FPCA bit to 1
30	LSPEN	R/W	1h	Enables lazy context save of floating-point state
29	LSPENS	R/W	0h	This bit controls whether the LSPEN bit is writeable from the Non-secure state
28	CLRONRET	R/W	0h	Clear floating-point caller saved registers on exception return
27	CLRONRETS	R/W	0h	This bit controls whether the CLRONRET bit is writeable from the Non-secure state
26	TS	R/W	0h	Treat floating-point registers as Secure enable
25-11	RES0	R	0h	Reserved, RES0
10	UFRDY	R/W	0h	Indicates whether the software executing when the PE allocated the floating-point stack frame was able to set the UsageFault exception to pending
9	SPLIMVIOL	R/W	0h	This bit is banked between the Security states and indicates whether the floating-point context violates the stack pointer limit that was active when lazy state preservation was activated. SPLIMVIOL modifies the lazy floating-point state preservation behavior
8	MONRDY	R/W	0h	Indicates whether the software executing when the PE allocated the floating-point stack frame was able to set the DebugMonitor exception to pending
7	SFRDY	R/W	0h	Indicates whether the software executing when the PE allocated the floating-point stack frame was able to set the SecureFault exception to pending. This bit is only present in the Secure version of the register, and behaves as RAZ/WI when accessed from the Non-secure state
6	BFRDY	R/W	0h	Indicates whether the software executing when the PE allocated the floating-point stack frame was able to set the BusFault exception to pending
5	MMRDY	R/W	0h	Indicates whether the software executing when the PE allocated the floating-point stack frame was able to set the MemManage exception to pending
4	HFRDY	R/W	0h	Indicates whether the software executing when the PE allocated the floating-point stack frame was able to set the HardFault exception to pending
3	THREAD	R/W	0h	Indicates the PE mode when it allocated the floating-point stack frame
2	S	R/W	0h	Security status of the floating-point context. This bit is only present in the Secure version of the register, and behaves as RAZ/WI when accessed from the Non-secure state. This bit is updated whenever lazy state preservation is activated, or when a floating-point instruction is executed
1	USER	R/W	0h	Indicates the privilege level of the software executing when the PE allocated the floating-point stack frame
0	LSPACT	R/W	0h	Indicates whether lazy preservation of the floating-point state is active

3.9.7.2 FPCAR Register (Offset = 8h) [Reset = 00000000h]

FPCAR is shown in Table 3-163.

Return to the Summary Table.

Holds the location of the unpopulated floating-point register space allocated on an exception stack frame

Table 3-163. FPCAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	ADDRESS	R/W	0h	The location of the unpopulated floating-point register space allocated on an exception stack frame
2-0	RES0	R	0h	Reserved, RES0

3.9.7.3 FPDSCR Register (Offset = Ch) [Reset = 00000000h]

FPDSCR is shown in Table 3-164.

Return to the Summary Table.

Holds the default values for the floating-point status control data that the PE assigns to the FPSCR when it creates a new floating-point context

Table 3-164. FPDSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RES0	R	0h	Reserved, RES0
26	AHP	R/W	0h	Default value for FPSCR.AHP
25	DN	R/W	0h	Default value for FPSCR.DN
24	FZ	R/W	0h	Default value for FPSCR.FZ
23-22	RMode	R/W	0h	Default value for FPSCR.RMode
21-0	RES0_1	R	Xh	Reserved, RES0

3.9.7.4 MVFR0 Register (Offset = 10h) [Reset = 00000000h]

MVFR0 is shown in Table 3-165.

Return to the Summary Table.

Describes the features provided by the Floating-point Extension

Table 3-165. MVFR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	FPRound	R	1h	Indicates the rounding modes supported by the FP Extension
27-24	RES0	R	0h	Reserved, RES0
23-20	FPSqrt	R	1h	Indicates the support for FP square root operations
19-16	FPDivide	R	1h	Indicates the support for FP divide operations
15-12	RES0_1	R	0h	Reserved, RES0
11-8	FPDP	R	0h	Indicates support for FP double-precision operations
7-4	FPSP	R	2h	Indicates support for FP single-precision operations
3-0	SIMDReg	R	1h	Indicates size of FP register file

3.9.7.5 MVFR1 Register (Offset = 14h) [Reset = 00000000h]

MVFR1 is shown in Table 3-166.

Return to the Summary Table.

Describes the features provided by the Floating-point Extension

Table 3-166. MVFR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	FMAC	R	1h	Indicates whether the FP Extension implements the fused multiply accumulate instructions
27-24	FPHP	R	1h	Indicates whether the FP Extension implements half-precision FP conversion instructions
23-8	RES0	R	0h	Reserved, RES0
7-4	FPDNaN	R	1h	Indicates whether the FP hardware implementation supports NaN propagation
3-0	FPFtZ	R	1h	Indicates whether subnormals are always flushed-to-zero

3.9.7.6 MVFR2 Register (Offset = 18h) [Reset = 00000000h]

MVFR2 is shown in Table 3-167.

Return to the Summary Table.

Describes the features provided by the Floating-point Extension

Table 3-167. MVFR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	FPMisc	R	4h	Indicates support for miscellaneous FP features
3-0	RES0_1	R	0h	Reserved, RES0

3.9.8 ICB Registers

Table 3-168 lists the memory-mapped registers for the ICB registers. All register offset addresses not listed in Table 3-168 should be considered as reserved locations and the register contents should not be modified.

Table 3-168. ICB Registers

Offset	Acronym	Register Name	Section
4h	ICTR	Provides information about the interrupt controller	Section 3.9.8.1
8h	ACTLR	Provides IMPLEMENTATION DEFINED configuration and control options	Section 3.9.8.2

Complex bit access types are encoded to fit into small table cells. Table 3-169 shows the codes that are used for access types in this section.

Table 3-169. ICB Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

3.9.8.1 ICTR Register (Offset = 4h) [Reset = 00000000h]

ICTR is shown in Table 3-170.

Return to the Summary Table.

Provides information about the interrupt controller

Table 3-170. ICTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RES0	R	Xh	Reserved, RES0
3-0	INTLINESNUM	R	0h	Indicates the number of the highest implemented register in each of the NVIC control register sets, or in the case of NVIC_IPR*n, 4×INTLINESNUM

3.9.8.2 ACTLR Register (Offset = 8h) [Reset = 00000000h]

ACTLR is shown in Table 3-171.

Return to the Summary Table.

Provides IMPLEMENTATION DEFINED configuration and control options

Table 3-171. ACTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RES0	R	0h	Reserved, RES0
29	EXTEXCLALL	R/W	0h	External Exclusives Allowed with no MPU
28-14	RES0_1	R	0h	Reserved, RES0
13	SBIST	R/W	0h	Bit used internally by Software Test Library (STL)
12	DISITMATBFLUSH	R/W	0h	Disable ATB Flush
11	RES0_2	R	0h	Reserved, RES0
10	FPEXCODIS	R/W	0h	Disable FPU exception outputs
9	DISOOFP	R/W	0h	Disable out-of-order FP instruction completion
8-3	RES0_3	R	0h	Reserved, RES0
2	DISFOLD	R/W	0h	Disable dual-issue.
1	RES0_4	R	0h	Reserved, RES0
0	DISMCYCINT	R/W	0h	Disable dual-issue.

3.9.9 ITM Registers

Table 3-172 lists the memory-mapped registers for the ITM registers. All register offset addresses not listed in Table 3-172 should be considered as reserved locations and the register contents should not be modified.

Table 3-172. ITM Registers

Offset	Acronym	Register Name	Section
0h	ITM Stimulus Port Register 0	Provides the interface for generating Instrumentation packets	Section 3.9.9.1
4h	ITM Stimulus Port Register 1	Provides the interface for generating Instrumentation packets	Section 3.9.9.2
8h	ITM Stimulus Port Register 2	Provides the interface for generating Instrumentation packets	Section 3.9.9.3
Ch	ITM Stimulus Port Register 3	Provides the interface for generating Instrumentation packets	Section 3.9.9.4
10h	ITM Stimulus Port Register 4	Provides the interface for generating Instrumentation packets	Section 3.9.9.5
14h	ITM Stimulus Port Register 5	Provides the interface for generating Instrumentation packets	Section 3.9.9.6
18h	ITM Stimulus Port Register 6	Provides the interface for generating Instrumentation packets	Section 3.9.9.7
1Ch	ITM Stimulus Port Register 7	Provides the interface for generating Instrumentation packets	Section 3.9.9.8
20h	ITM Stimulus Port Register 8	Provides the interface for generating Instrumentation packets	Section 3.9.9.9
24h	ITM Stimulus Port Register 9	Provides the interface for generating Instrumentation packets	Section 3.9.9.10
28h	ITM Stimulus Port Register 10	Provides the interface for generating Instrumentation packets	Section 3.9.9.11
2Ch	ITM Stimulus Port Register 11	Provides the interface for generating Instrumentation packets	Section 3.9.9.12
30h	ITM Stimulus Port Register 12	Provides the interface for generating Instrumentation packets	Section 3.9.9.13
34h	ITM Stimulus Port Register 13	Provides the interface for generating Instrumentation packets	Section 3.9.9.14
38h	ITM Stimulus Port Register 14	Provides the interface for generating Instrumentation packets	Section 3.9.9.15
3Ch	ITM Stimulus Port Register 15	Provides the interface for generating Instrumentation packets	Section 3.9.9.16
40h	ITM Stimulus Port Register 16	Provides the interface for generating Instrumentation packets	Section 3.9.9.17
44h	ITM Stimulus Port Register 17	Provides the interface for generating Instrumentation packets	Section 3.9.9.18
48h	ITM Stimulus Port Register 18	Provides the interface for generating Instrumentation packets	Section 3.9.9.19
4Ch	ITM Stimulus Port Register 19	Provides the interface for generating Instrumentation packets	Section 3.9.9.20
50h	ITM Stimulus Port Register 20	Provides the interface for generating Instrumentation packets	Section 3.9.9.21
54h	ITM Stimulus Port Register 21	Provides the interface for generating Instrumentation packets	Section 3.9.9.22
58h	ITM Stimulus Port Register 22	Provides the interface for generating Instrumentation packets	Section 3.9.9.23
5Ch	ITM Stimulus Port Register 23	Provides the interface for generating Instrumentation packets	Section 3.9.9.24

Table 3-172. ITM Registers (continued)

Offset	Acronym	Register Name	Section
60h	ITM Stimulus Port Register 24	Provides the interface for generating Instrumentation packets	Section 3.9.9.25
64h	ITM Stimulus Port Register 25	Provides the interface for generating Instrumentation packets	Section 3.9.9.26
68h	ITM Stimulus Port Register 26	Provides the interface for generating Instrumentation packets	Section 3.9.9.27
6Ch	ITM Stimulus Port Register 27	Provides the interface for generating Instrumentation packets	Section 3.9.9.28
70h	ITM Stimulus Port Register 28	Provides the interface for generating Instrumentation packets	Section 3.9.9.29
74h	ITM Stimulus Port Register 29	Provides the interface for generating Instrumentation packets	Section 3.9.9.30
78h	ITM Stimulus Port Register 30	Provides the interface for generating Instrumentation packets	Section 3.9.9.31
7Ch	ITM Stimulus Port Register 31	Provides the interface for generating Instrumentation packets	Section 3.9.9.32
80h	ITM Stimulus Port Register 32	Provides the interface for generating Instrumentation packets	Section 3.9.9.33
84h	ITM Stimulus Port Register 33	Provides the interface for generating Instrumentation packets	Section 3.9.9.34
88h	ITM Stimulus Port Register 34	Provides the interface for generating Instrumentation packets	Section 3.9.9.35
8Ch	ITM Stimulus Port Register 35	Provides the interface for generating Instrumentation packets	Section 3.9.9.36
90h	ITM Stimulus Port Register 36	Provides the interface for generating Instrumentation packets	Section 3.9.9.37
94h	ITM Stimulus Port Register 37	Provides the interface for generating Instrumentation packets	Section 3.9.9.38
98h	ITM Stimulus Port Register 38	Provides the interface for generating Instrumentation packets	Section 3.9.9.39
9Ch	ITM Stimulus Port Register 39	Provides the interface for generating Instrumentation packets	Section 3.9.9.40
A0h	ITM Stimulus Port Register 40	Provides the interface for generating Instrumentation packets	Section 3.9.9.41
A4h	ITM Stimulus Port Register 41	Provides the interface for generating Instrumentation packets	Section 3.9.9.42
A8h	ITM Stimulus Port Register 42	Provides the interface for generating Instrumentation packets	Section 3.9.9.43
ACh	ITM Stimulus Port Register 43	Provides the interface for generating Instrumentation packets	Section 3.9.9.44
B0h	ITM Stimulus Port Register 44	Provides the interface for generating Instrumentation packets	Section 3.9.9.45
B4h	ITM Stimulus Port Register 45	Provides the interface for generating Instrumentation packets	Section 3.9.9.46
B8h	ITM Stimulus Port Register 46	Provides the interface for generating Instrumentation packets	Section 3.9.9.47
BCh	ITM Stimulus Port Register 47	Provides the interface for generating Instrumentation packets	Section 3.9.9.48
C0h	ITM Stimulus Port Register 48	Provides the interface for generating Instrumentation packets	Section 3.9.9.49
C4h	ITM Stimulus Port Register 49	Provides the interface for generating Instrumentation packets	Section 3.9.9.50

Table 3-172. ITM Registers (continued)

Offset	Acronym	Register Name	Section
C8h	ITM Stimulus Port Register 50	Provides the interface for generating Instrumentation packets	Section 3.9.9.51
CCh	ITM Stimulus Port Register 51	Provides the interface for generating Instrumentation packets	Section 3.9.9.52
D0h	ITM Stimulus Port Register 52	Provides the interface for generating Instrumentation packets	Section 3.9.9.53
D4h	ITM Stimulus Port Register 53	Provides the interface for generating Instrumentation packets	Section 3.9.9.54
D8h	ITM Stimulus Port Register 54	Provides the interface for generating Instrumentation packets	Section 3.9.9.55
DCh	ITM Stimulus Port Register 55	Provides the interface for generating Instrumentation packets	Section 3.9.9.56
E0h	ITM Stimulus Port Register 56	Provides the interface for generating Instrumentation packets	Section 3.9.9.57
E4h	ITM Stimulus Port Register 57	Provides the interface for generating Instrumentation packets	Section 3.9.9.58
E8h	ITM Stimulus Port Register 58	Provides the interface for generating Instrumentation packets	Section 3.9.9.59
ECh	ITM Stimulus Port Register 59	Provides the interface for generating Instrumentation packets	Section 3.9.9.60
F0h	ITM Stimulus Port Register 60	Provides the interface for generating Instrumentation packets	Section 3.9.9.61
F4h	ITM Stimulus Port Register 61	Provides the interface for generating Instrumentation packets	Section 3.9.9.62
F8h	ITM Stimulus Port Register 62	Provides the interface for generating Instrumentation packets	Section 3.9.9.63
FCh	ITM Stimulus Port Register 63	Provides the interface for generating Instrumentation packets	Section 3.9.9.64
100h	ITM Stimulus Port Register 64	Provides the interface for generating Instrumentation packets	Section 3.9.9.65
104h	ITM Stimulus Port Register 65	Provides the interface for generating Instrumentation packets	Section 3.9.9.66
108h	ITM Stimulus Port Register 66	Provides the interface for generating Instrumentation packets	Section 3.9.9.67
10Ch	ITM Stimulus Port Register 67	Provides the interface for generating Instrumentation packets	Section 3.9.9.68
110h	ITM Stimulus Port Register 68	Provides the interface for generating Instrumentation packets	Section 3.9.9.69
114h	ITM Stimulus Port Register 69	Provides the interface for generating Instrumentation packets	Section 3.9.9.70
118h	ITM Stimulus Port Register 70	Provides the interface for generating Instrumentation packets	Section 3.9.9.71
11Ch	ITM Stimulus Port Register 71	Provides the interface for generating Instrumentation packets	Section 3.9.9.72
120h	ITM Stimulus Port Register 72	Provides the interface for generating Instrumentation packets	Section 3.9.9.73
124h	ITM Stimulus Port Register 73	Provides the interface for generating Instrumentation packets	Section 3.9.9.74
128h	ITM Stimulus Port Register 74	Provides the interface for generating Instrumentation packets	Section 3.9.9.75
12Ch	ITM Stimulus Port Register 75	Provides the interface for generating Instrumentation packets	Section 3.9.9.76

Table 3-172. ITM Registers (continued)

Offset	Acronym	Register Name	Section
130h	ITM Stimulus Port Register 76	Provides the interface for generating Instrumentation packets	Section 3.9.9.77
134h	ITM Stimulus Port Register 77	Provides the interface for generating Instrumentation packets	Section 3.9.9.78
138h	ITM Stimulus Port Register 78	Provides the interface for generating Instrumentation packets	Section 3.9.9.79
13Ch	ITM Stimulus Port Register 79	Provides the interface for generating Instrumentation packets	Section 3.9.9.80
140h	ITM Stimulus Port Register 80	Provides the interface for generating Instrumentation packets	Section 3.9.9.81
144h	ITM Stimulus Port Register 81	Provides the interface for generating Instrumentation packets	Section 3.9.9.82
148h	ITM Stimulus Port Register 82	Provides the interface for generating Instrumentation packets	Section 3.9.9.83
14Ch	ITM Stimulus Port Register 83	Provides the interface for generating Instrumentation packets	Section 3.9.9.84
150h	ITM Stimulus Port Register 84	Provides the interface for generating Instrumentation packets	Section 3.9.9.85
154h	ITM Stimulus Port Register 85	Provides the interface for generating Instrumentation packets	Section 3.9.9.86
158h	ITM Stimulus Port Register 86	Provides the interface for generating Instrumentation packets	Section 3.9.9.87
15Ch	ITM Stimulus Port Register 87	Provides the interface for generating Instrumentation packets	Section 3.9.9.88
160h	ITM Stimulus Port Register 88	Provides the interface for generating Instrumentation packets	Section 3.9.9.89
164h	ITM Stimulus Port Register 89	Provides the interface for generating Instrumentation packets	Section 3.9.9.90
168h	ITM Stimulus Port Register 90	Provides the interface for generating Instrumentation packets	Section 3.9.9.91
16Ch	ITM Stimulus Port Register 91	Provides the interface for generating Instrumentation packets	Section 3.9.9.92
170h	ITM Stimulus Port Register 92	Provides the interface for generating Instrumentation packets	Section 3.9.9.93
174h	ITM Stimulus Port Register 93	Provides the interface for generating Instrumentation packets	Section 3.9.9.94
178h	ITM Stimulus Port Register 94	Provides the interface for generating Instrumentation packets	Section 3.9.9.95
17Ch	ITM Stimulus Port Register 95	Provides the interface for generating Instrumentation packets	Section 3.9.9.96
180h	ITM Stimulus Port Register 96	Provides the interface for generating Instrumentation packets	Section 3.9.9.97
184h	ITM Stimulus Port Register 97	Provides the interface for generating Instrumentation packets	Section 3.9.9.98
188h	ITM Stimulus Port Register 98	Provides the interface for generating Instrumentation packets	Section 3.9.9.99
18Ch	ITM Stimulus Port Register 99	Provides the interface for generating Instrumentation packets	Section 3.9.9.100
190h	ITM Stimulus Port Register 100	Provides the interface for generating Instrumentation packets	Section 3.9.9.101
194h	ITM Stimulus Port Register 101	Provides the interface for generating Instrumentation packets	Section 3.9.9.102

Table 3-172. ITM Registers (continued)

Offset	Acronym	Register Name	Section
198h	ITM Stimulus Port Register 102	Provides the interface for generating Instrumentation packets	Section 3.9.9.103
19Ch	ITM Stimulus Port Register 103	Provides the interface for generating Instrumentation packets	Section 3.9.9.104
1A0h	ITM Stimulus Port Register 104	Provides the interface for generating Instrumentation packets	Section 3.9.9.105
1A4h	ITM Stimulus Port Register 105	Provides the interface for generating Instrumentation packets	Section 3.9.9.106
1A8h	ITM Stimulus Port Register 106	Provides the interface for generating Instrumentation packets	Section 3.9.9.107
1ACh	ITM Stimulus Port Register 107	Provides the interface for generating Instrumentation packets	Section 3.9.9.108
1B0h	ITM Stimulus Port Register 108	Provides the interface for generating Instrumentation packets	Section 3.9.9.109
1B4h	ITM Stimulus Port Register 109	Provides the interface for generating Instrumentation packets	Section 3.9.9.110
1B8h	ITM Stimulus Port Register 110	Provides the interface for generating Instrumentation packets	Section 3.9.9.111
1BCh	ITM Stimulus Port Register 111	Provides the interface for generating Instrumentation packets	Section 3.9.9.112
1C0h	ITM Stimulus Port Register 112	Provides the interface for generating Instrumentation packets	Section 3.9.9.113
1C4h	ITM Stimulus Port Register 113	Provides the interface for generating Instrumentation packets	Section 3.9.9.114
1C8h	ITM Stimulus Port Register 114	Provides the interface for generating Instrumentation packets	Section 3.9.9.115
1CCh	ITM Stimulus Port Register 115	Provides the interface for generating Instrumentation packets	Section 3.9.9.116
1D0h	ITM Stimulus Port Register 116	Provides the interface for generating Instrumentation packets	Section 3.9.9.117
1D4h	ITM Stimulus Port Register 117	Provides the interface for generating Instrumentation packets	Section 3.9.9.118
1D8h	ITM Stimulus Port Register 118	Provides the interface for generating Instrumentation packets	Section 3.9.9.119
1DCh	ITM Stimulus Port Register 119	Provides the interface for generating Instrumentation packets	Section 3.9.9.120
1E0h	ITM Stimulus Port Register 120	Provides the interface for generating Instrumentation packets	Section 3.9.9.121
1E4h	ITM Stimulus Port Register 121	Provides the interface for generating Instrumentation packets	Section 3.9.9.122
1E8h	ITM Stimulus Port Register 122	Provides the interface for generating Instrumentation packets	Section 3.9.9.123
1ECh	ITM Stimulus Port Register 123	Provides the interface for generating Instrumentation packets	Section 3.9.9.124
1F0h	ITM Stimulus Port Register 124	Provides the interface for generating Instrumentation packets	Section 3.9.9.125
1F4h	ITM Stimulus Port Register 125	Provides the interface for generating Instrumentation packets	Section 3.9.9.126
1F8h	ITM Stimulus Port Register 126	Provides the interface for generating Instrumentation packets	Section 3.9.9.127
1FCh	ITM Stimulus Port Register 127	Provides the interface for generating Instrumentation packets	Section 3.9.9.128

Table 3-172. ITM Registers (continued)

Offset	Acronym	Register Name	Section
200h	ITM Stimulus Port Register 128	Provides the interface for generating Instrumentation packets	Section 3.9.9.129
204h	ITM Stimulus Port Register 129	Provides the interface for generating Instrumentation packets	Section 3.9.9.130
208h	ITM Stimulus Port Register 130	Provides the interface for generating Instrumentation packets	Section 3.9.9.131
20Ch	ITM Stimulus Port Register 131	Provides the interface for generating Instrumentation packets	Section 3.9.9.132
210h	ITM Stimulus Port Register 132	Provides the interface for generating Instrumentation packets	Section 3.9.9.133
214h	ITM Stimulus Port Register 133	Provides the interface for generating Instrumentation packets	Section 3.9.9.134
218h	ITM Stimulus Port Register 134	Provides the interface for generating Instrumentation packets	Section 3.9.9.135
21Ch	ITM Stimulus Port Register 135	Provides the interface for generating Instrumentation packets	Section 3.9.9.136
220h	ITM Stimulus Port Register 136	Provides the interface for generating Instrumentation packets	Section 3.9.9.137
224h	ITM Stimulus Port Register 137	Provides the interface for generating Instrumentation packets	Section 3.9.9.138
228h	ITM Stimulus Port Register 138	Provides the interface for generating Instrumentation packets	Section 3.9.9.139
22Ch	ITM Stimulus Port Register 139	Provides the interface for generating Instrumentation packets	Section 3.9.9.140
230h	ITM Stimulus Port Register 140	Provides the interface for generating Instrumentation packets	Section 3.9.9.141
234h	ITM Stimulus Port Register 141	Provides the interface for generating Instrumentation packets	Section 3.9.9.142
238h	ITM Stimulus Port Register 142	Provides the interface for generating Instrumentation packets	Section 3.9.9.143
23Ch	ITM Stimulus Port Register 143	Provides the interface for generating Instrumentation packets	Section 3.9.9.144
240h	ITM Stimulus Port Register 144	Provides the interface for generating Instrumentation packets	Section 3.9.9.145
244h	ITM Stimulus Port Register 145	Provides the interface for generating Instrumentation packets	Section 3.9.9.146
248h	ITM Stimulus Port Register 146	Provides the interface for generating Instrumentation packets	Section 3.9.9.147
24Ch	ITM Stimulus Port Register 147	Provides the interface for generating Instrumentation packets	Section 3.9.9.148
250h	ITM Stimulus Port Register 148	Provides the interface for generating Instrumentation packets	Section 3.9.9.149
254h	ITM Stimulus Port Register 149	Provides the interface for generating Instrumentation packets	Section 3.9.9.150
258h	ITM Stimulus Port Register 150	Provides the interface for generating Instrumentation packets	Section 3.9.9.151
25Ch	ITM Stimulus Port Register 151	Provides the interface for generating Instrumentation packets	Section 3.9.9.152
260h	ITM Stimulus Port Register 152	Provides the interface for generating Instrumentation packets	Section 3.9.9.153
264h	ITM Stimulus Port Register 153	Provides the interface for generating Instrumentation packets	Section 3.9.9.154

Table 3-172. ITM Registers (continued)

Offset	Acronym	Register Name	Section
268h	ITM Stimulus Port Register 154	Provides the interface for generating Instrumentation packets	Section 3.9.9.155
26Ch	ITM Stimulus Port Register 155	Provides the interface for generating Instrumentation packets	Section 3.9.9.156
270h	ITM Stimulus Port Register 156	Provides the interface for generating Instrumentation packets	Section 3.9.9.157
274h	ITM Stimulus Port Register 157	Provides the interface for generating Instrumentation packets	Section 3.9.9.158
278h	ITM Stimulus Port Register 158	Provides the interface for generating Instrumentation packets	Section 3.9.9.159
27Ch	ITM Stimulus Port Register 159	Provides the interface for generating Instrumentation packets	Section 3.9.9.160
280h	ITM Stimulus Port Register 160	Provides the interface for generating Instrumentation packets	Section 3.9.9.161
284h	ITM Stimulus Port Register 161	Provides the interface for generating Instrumentation packets	Section 3.9.9.162
288h	ITM Stimulus Port Register 162	Provides the interface for generating Instrumentation packets	Section 3.9.9.163
28Ch	ITM Stimulus Port Register 163	Provides the interface for generating Instrumentation packets	Section 3.9.9.164
290h	ITM Stimulus Port Register 164	Provides the interface for generating Instrumentation packets	Section 3.9.9.165
294h	ITM Stimulus Port Register 165	Provides the interface for generating Instrumentation packets	Section 3.9.9.166
298h	ITM Stimulus Port Register 166	Provides the interface for generating Instrumentation packets	Section 3.9.9.167
29Ch	ITM Stimulus Port Register 167	Provides the interface for generating Instrumentation packets	Section 3.9.9.168
2A0h	ITM Stimulus Port Register 168	Provides the interface for generating Instrumentation packets	Section 3.9.9.169
2A4h	ITM Stimulus Port Register 169	Provides the interface for generating Instrumentation packets	Section 3.9.9.170
2A8h	ITM Stimulus Port Register 170	Provides the interface for generating Instrumentation packets	Section 3.9.9.171
2ACh	ITM Stimulus Port Register 171	Provides the interface for generating Instrumentation packets	Section 3.9.9.172
2B0h	ITM Stimulus Port Register 172	Provides the interface for generating Instrumentation packets	Section 3.9.9.173
2B4h	ITM Stimulus Port Register 173	Provides the interface for generating Instrumentation packets	Section 3.9.9.174
2B8h	ITM Stimulus Port Register 174	Provides the interface for generating Instrumentation packets	Section 3.9.9.175
2BCh	ITM Stimulus Port Register 175	Provides the interface for generating Instrumentation packets	Section 3.9.9.176
2C0h	ITM Stimulus Port Register 176	Provides the interface for generating Instrumentation packets	Section 3.9.9.177
2C4h	ITM Stimulus Port Register 177	Provides the interface for generating Instrumentation packets	Section 3.9.9.178
2C8h	ITM Stimulus Port Register 178	Provides the interface for generating Instrumentation packets	Section 3.9.9.179
2CCh	ITM Stimulus Port Register 179	Provides the interface for generating Instrumentation packets	Section 3.9.9.180

Table 3-172. ITM Registers (continued)

Offset	Acronym	Register Name	Section
2D0h	ITM Stimulus Port Register 180	Provides the interface for generating Instrumentation packets	Section 3.9.9.181
2D4h	ITM Stimulus Port Register 181	Provides the interface for generating Instrumentation packets	Section 3.9.9.182
2D8h	ITM Stimulus Port Register 182	Provides the interface for generating Instrumentation packets	Section 3.9.9.183
2DCh	ITM Stimulus Port Register 183	Provides the interface for generating Instrumentation packets	Section 3.9.9.184
2E0h	ITM Stimulus Port Register 184	Provides the interface for generating Instrumentation packets	Section 3.9.9.185
2E4h	ITM Stimulus Port Register 185	Provides the interface for generating Instrumentation packets	Section 3.9.9.186
2E8h	ITM Stimulus Port Register 186	Provides the interface for generating Instrumentation packets	Section 3.9.9.187
2ECh	ITM Stimulus Port Register 187	Provides the interface for generating Instrumentation packets	Section 3.9.9.188
2F0h	ITM Stimulus Port Register 188	Provides the interface for generating Instrumentation packets	Section 3.9.9.189
2F4h	ITM Stimulus Port Register 189	Provides the interface for generating Instrumentation packets	Section 3.9.9.190
2F8h	ITM Stimulus Port Register 190	Provides the interface for generating Instrumentation packets	Section 3.9.9.191
2FCh	ITM Stimulus Port Register 191	Provides the interface for generating Instrumentation packets	Section 3.9.9.192
300h	ITM Stimulus Port Register 192	Provides the interface for generating Instrumentation packets	Section 3.9.9.193
304h	ITM Stimulus Port Register 193	Provides the interface for generating Instrumentation packets	Section 3.9.9.194
308h	ITM Stimulus Port Register 194	Provides the interface for generating Instrumentation packets	Section 3.9.9.195
30Ch	ITM Stimulus Port Register 195	Provides the interface for generating Instrumentation packets	Section 3.9.9.196
310h	ITM Stimulus Port Register 196	Provides the interface for generating Instrumentation packets	Section 3.9.9.197
314h	ITM Stimulus Port Register 197	Provides the interface for generating Instrumentation packets	Section 3.9.9.198
318h	ITM Stimulus Port Register 198	Provides the interface for generating Instrumentation packets	Section 3.9.9.199
31Ch	ITM Stimulus Port Register 199	Provides the interface for generating Instrumentation packets	Section 3.9.9.200
320h	ITM Stimulus Port Register 200	Provides the interface for generating Instrumentation packets	Section 3.9.9.201
324h	ITM Stimulus Port Register 201	Provides the interface for generating Instrumentation packets	Section 3.9.9.202
328h	ITM Stimulus Port Register 202	Provides the interface for generating Instrumentation packets	Section 3.9.9.203
32Ch	ITM Stimulus Port Register 203	Provides the interface for generating Instrumentation packets	Section 3.9.9.204
330h	ITM Stimulus Port Register 204	Provides the interface for generating Instrumentation packets	Section 3.9.9.205
334h	ITM Stimulus Port Register 205	Provides the interface for generating Instrumentation packets	Section 3.9.9.206

Table 3-172. ITM Registers (continued)

Offset	Acronym	Register Name	Section
338h	ITM Stimulus Port Register 206	Provides the interface for generating Instrumentation packets	Section 3.9.9.207
33Ch	ITM Stimulus Port Register 207	Provides the interface for generating Instrumentation packets	Section 3.9.9.208
340h	ITM Stimulus Port Register 208	Provides the interface for generating Instrumentation packets	Section 3.9.9.209
344h	ITM Stimulus Port Register 209	Provides the interface for generating Instrumentation packets	Section 3.9.9.210
348h	ITM Stimulus Port Register 210	Provides the interface for generating Instrumentation packets	Section 3.9.9.211
34Ch	ITM Stimulus Port Register 211	Provides the interface for generating Instrumentation packets	Section 3.9.9.212
350h	ITM Stimulus Port Register 212	Provides the interface for generating Instrumentation packets	Section 3.9.9.213
354h	ITM Stimulus Port Register 213	Provides the interface for generating Instrumentation packets	Section 3.9.9.214
358h	ITM Stimulus Port Register 214	Provides the interface for generating Instrumentation packets	Section 3.9.9.215
35Ch	ITM Stimulus Port Register 215	Provides the interface for generating Instrumentation packets	Section 3.9.9.216
360h	ITM Stimulus Port Register 216	Provides the interface for generating Instrumentation packets	Section 3.9.9.217
364h	ITM Stimulus Port Register 217	Provides the interface for generating Instrumentation packets	Section 3.9.9.218
368h	ITM Stimulus Port Register 218	Provides the interface for generating Instrumentation packets	Section 3.9.9.219
36Ch	ITM Stimulus Port Register 219	Provides the interface for generating Instrumentation packets	Section 3.9.9.220
370h	ITM Stimulus Port Register 220	Provides the interface for generating Instrumentation packets	Section 3.9.9.221
374h	ITM Stimulus Port Register 221	Provides the interface for generating Instrumentation packets	Section 3.9.9.222
378h	ITM Stimulus Port Register 222	Provides the interface for generating Instrumentation packets	Section 3.9.9.223
37Ch	ITM Stimulus Port Register 223	Provides the interface for generating Instrumentation packets	Section 3.9.9.224
380h	ITM Stimulus Port Register 224	Provides the interface for generating Instrumentation packets	Section 3.9.9.225
384h	ITM Stimulus Port Register 225	Provides the interface for generating Instrumentation packets	Section 3.9.9.226
388h	ITM Stimulus Port Register 226	Provides the interface for generating Instrumentation packets	Section 3.9.9.227
38Ch	ITM Stimulus Port Register 227	Provides the interface for generating Instrumentation packets	Section 3.9.9.228
390h	ITM Stimulus Port Register 228	Provides the interface for generating Instrumentation packets	Section 3.9.9.229
394h	ITM Stimulus Port Register 229	Provides the interface for generating Instrumentation packets	Section 3.9.9.230
398h	ITM Stimulus Port Register 230	Provides the interface for generating Instrumentation packets	Section 3.9.9.231
39Ch	ITM Stimulus Port Register 231	Provides the interface for generating Instrumentation packets	Section 3.9.9.232

Table 3-172. ITM Registers (continued)

Offset	Acronym	Register Name	Section
3A0h	ITM Stimulus Port Register 232	Provides the interface for generating Instrumentation packets	Section 3.9.9.233
3A4h	ITM Stimulus Port Register 233	Provides the interface for generating Instrumentation packets	Section 3.9.9.234
3A8h	ITM Stimulus Port Register 234	Provides the interface for generating Instrumentation packets	Section 3.9.9.235
3ACh	ITM Stimulus Port Register 235	Provides the interface for generating Instrumentation packets	Section 3.9.9.236
3B0h	ITM Stimulus Port Register 236	Provides the interface for generating Instrumentation packets	Section 3.9.9.237
3B4h	ITM Stimulus Port Register 237	Provides the interface for generating Instrumentation packets	Section 3.9.9.238
3B8h	ITM Stimulus Port Register 238	Provides the interface for generating Instrumentation packets	Section 3.9.9.239
3BCh	ITM Stimulus Port Register 239	Provides the interface for generating Instrumentation packets	Section 3.9.9.240
3C0h	ITM Stimulus Port Register 240	Provides the interface for generating Instrumentation packets	Section 3.9.9.241
3C4h	ITM Stimulus Port Register 241	Provides the interface for generating Instrumentation packets	Section 3.9.9.242
3C8h	ITM Stimulus Port Register 242	Provides the interface for generating Instrumentation packets	Section 3.9.9.243
3CCh	ITM Stimulus Port Register 243	Provides the interface for generating Instrumentation packets	Section 3.9.9.244
3D0h	ITM Stimulus Port Register 244	Provides the interface for generating Instrumentation packets	Section 3.9.9.245
3D4h	ITM Stimulus Port Register 245	Provides the interface for generating Instrumentation packets	Section 3.9.9.246
3D8h	ITM Stimulus Port Register 246	Provides the interface for generating Instrumentation packets	Section 3.9.9.247
3DCh	ITM Stimulus Port Register 247	Provides the interface for generating Instrumentation packets	Section 3.9.9.248
3E0h	ITM Stimulus Port Register 248	Provides the interface for generating Instrumentation packets	Section 3.9.9.249
3E4h	ITM Stimulus Port Register 249	Provides the interface for generating Instrumentation packets	Section 3.9.9.250
3E8h	ITM Stimulus Port Register 250	Provides the interface for generating Instrumentation packets	Section 3.9.9.251
3ECh	ITM Stimulus Port Register 251	Provides the interface for generating Instrumentation packets	Section 3.9.9.252
3F0h	ITM Stimulus Port Register 252	Provides the interface for generating Instrumentation packets	Section 3.9.9.253
3F4h	ITM Stimulus Port Register 253	Provides the interface for generating Instrumentation packets	Section 3.9.9.254
3F8h	ITM Stimulus Port Register 254	Provides the interface for generating Instrumentation packets	Section 3.9.9.255
3FCh	ITM Stimulus Port Register 255	Provides the interface for generating Instrumentation packets	Section 3.9.9.256
E00h	ITM Trace Enable Register 0	Provide an individual enable bit for each ITM_STIM register	Section 3.9.9.257
E04h	ITM Trace Enable Register 1	Provide an individual enable bit for each ITM_STIM register	Section 3.9.9.258

Table 3-172. ITM Registers (continued)

Offset	Acronym	Register Name	Section
E08h	ITM Trace Enable Register 2	Provide an individual enable bit for each ITM_STIM register	Section 3.9.9.259
E0Ch	ITM Trace Enable Register 3	Provide an individual enable bit for each ITM_STIM register	Section 3.9.9.260
E10h	ITM Trace Enable Register 4	Provide an individual enable bit for each ITM_STIM register	Section 3.9.9.261
E14h	ITM Trace Enable Register 5	Provide an individual enable bit for each ITM_STIM register	Section 3.9.9.262
E18h	ITM Trace Enable Register 6	Provide an individual enable bit for each ITM_STIM register	Section 3.9.9.263
E1Ch	ITM Trace Enable Register 7	Provide an individual enable bit for each ITM_STIM register	Section 3.9.9.264
E40h	ITM Trace Privilege Register	Controls which stimulus ports can be accessed by unprivileged code	Section 3.9.9.265
E80h	ITM Trace Control Register	Configures and controls transfers through the ITM interface	Section 3.9.9.266
EF0h	INT_ATREADY	Integration Mode: Read ATB Ready	Section 3.9.9.267
EF8h	INT_ATVALID	Integration Mode: Write ATB Valid	Section 3.9.9.268
F00h	ITM_ITCTRL	Integration Mode Control Register	Section 3.9.9.269
FBCh	ITM Device Architecture Register	Provides CoreSight discovery information for the ITM	Section 3.9.9.270
FCCh	ITM Device Type Register	Provides CoreSight discovery information for the ITM	Section 3.9.9.271
FD0h	ITM Peripheral Identification Register 4	Provides CoreSight discovery information for the ITM	Section 3.9.9.272
FD4h	ITM Peripheral Identification Register 5	Provides CoreSight discovery information for the ITM	Section 3.9.9.273
FD8h	ITM Peripheral Identification Register 6	Provides CoreSight discovery information for the ITM	Section 3.9.9.274
FDCh	ITM Peripheral Identification Register 7	Provides CoreSight discovery information for the ITM	Section 3.9.9.275
FE0h	ITM Peripheral Identification Register 0	Provides CoreSight discovery information for the ITM	Section 3.9.9.276
FE4h	ITM Peripheral Identification Register 1	Provides CoreSight discovery information for the ITM	Section 3.9.9.277
FE8h	ITM Peripheral Identification Register 2	Provides CoreSight discovery information for the ITM	Section 3.9.9.278
FECh	ITM Peripheral Identification Register 3	Provides CoreSight discovery information for the ITM	Section 3.9.9.279
FF0h	ITM Component Identification Register 0	Provides CoreSight discovery information for the ITM	Section 3.9.9.280
FF4h	ITM Component Identification Register 1	Provides CoreSight discovery information for the ITM	Section 3.9.9.281
FF8h	ITM Component Identification Register 2	Provides CoreSight discovery information for the ITM	Section 3.9.9.282
FFCh	ITM Component Identification Register 3	Provides CoreSight discovery information for the ITM	Section 3.9.9.283

Complex bit access types are encoded to fit into small table cells. Table 3-173 shows the codes that are used for access types in this section.

Table 3-173. ITM Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

3.9.9.1 ITM Stimulus Port Register 0 (Offset = 0h) [Reset = 00000002h]

ITM Stimulus Port Register 0 is shown in Table 3-174.

Return to the Summary Table.

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Table 3-174. ITM Stimulus Port Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.2 ITM Stimulus Port Register 1 (Offset = 4h) [Reset = 00000002h]

ITM Stimulus Port Register 1 is shown in Table 3-175.

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Table 3-175. ITM Stimulus Port Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.3 ITM Stimulus Port Register 2 (Offset = 8h) [Reset = 00000002h]

ITM Stimulus Port Register 2 is shown in Table 3-176.

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Table 3-176. ITM Stimulus Port Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.4 ITM Stimulus Port Register 3 (Offset = Ch) [Reset = 00000002h]

ITM Stimulus Port Register 3 is shown in Table 3-177.

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Table 3-177. ITM Stimulus Port Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.5 ITM Stimulus Port Register 4 (Offset = 10h) [Reset = 00000002h]

ITM Stimulus Port Register 4 is shown in Table 3-178.

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Table 3-178. ITM Stimulus Port Register 4 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.6 ITM Stimulus Port Register 5 (Offset = 14h) [Reset = 00000002h]

ITM Stimulus Port Register 5 is shown in Table 3-179.

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Table 3-179. ITM Stimulus Port Register 5 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.7 ITM Stimulus Port Register 6 (Offset = 18h) [Reset = 00000002h]

ITM Stimulus Port Register 6 is shown in Table 3-180.

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Table 3-180. ITM Stimulus Port Register 6 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.8 ITM Stimulus Port Register 7 (Offset = 1Ch) [Reset = 00000002h]

ITM Stimulus Port Register 7 is shown in Table 3-181.

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Table 3-181. ITM Stimulus Port Register 7 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.9 ITM Stimulus Port Register 8 (Offset = 20h) [Reset = 00000002h]

ITM Stimulus Port Register 8 is shown in Table 3-182.

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Table 3-182. ITM Stimulus Port Register 8 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.10 ITM Stimulus Port Register 9 (Offset = 24h) [Reset = 00000002h]

ITM Stimulus Port Register 9 is shown in Table 3-183.

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Table 3-183. ITM Stimulus Port Register 9 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.11 ITM Stimulus Port Register 10 (Offset = 28h) [Reset = 00000002h]

ITM Stimulus Port Register 10 is shown in Table 3-184.

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Table 3-184. ITM Stimulus Port Register 10 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.12 ITM Stimulus Port Register 11 (Offset = 2Ch) [Reset = 00000002h]

ITM Stimulus Port Register 11 is shown in Table 3-185.

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Table 3-185. ITM Stimulus Port Register 11 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.13 ITM Stimulus Port Register 12 (Offset = 30h) [Reset = 00000002h]

ITM Stimulus Port Register 12 is shown in Table 3-186.

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Table 3-186. ITM Stimulus Port Register 12 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.14 ITM Stimulus Port Register 13 (Offset = 34h) [Reset = 00000002h]

ITM Stimulus Port Register 13 is shown in Table 3-187.

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Table 3-187. ITM Stimulus Port Register 13 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.15 ITM Stimulus Port Register 14 (Offset = 38h) [Reset = 00000002h]

ITM Stimulus Port Register 14 is shown in Table 3-188.

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Table 3-188. ITM Stimulus Port Register 14 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.16 ITM Stimulus Port Register 15 (Offset = 3Ch) [Reset = 00000002h]

ITM Stimulus Port Register 15 is shown in Table 3-189.

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Table 3-189. ITM Stimulus Port Register 15 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.17 ITM Stimulus Port Register 16 (Offset = 40h) [Reset = 00000002h]

ITM Stimulus Port Register 16 is shown in Table 3-190.

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Table 3-190. ITM Stimulus Port Register 16 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.18 ITM Stimulus Port Register 17 (Offset = 44h) [Reset = 00000002h]

ITM Stimulus Port Register 17 is shown in Table 3-191.

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Table 3-191. ITM Stimulus Port Register 17 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.19 ITM Stimulus Port Register 18 (Offset = 48h) [Reset = 00000002h]

ITM Stimulus Port Register 18 is shown in Table 3-192.

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Table 3-192. ITM Stimulus Port Register 18 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.20 ITM Stimulus Port Register 19 (Offset = 4Ch) [Reset = 00000002h]

ITM Stimulus Port Register 19 is shown in Table 3-193.

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Table 3-193. ITM Stimulus Port Register 19 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.21 ITM Stimulus Port Register 20 (Offset = 50h) [Reset = 00000002h]

ITM Stimulus Port Register 20 is shown in Table 3-194.

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Table 3-194. ITM Stimulus Port Register 20 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.22 ITM Stimulus Port Register 21 (Offset = 54h) [Reset = 00000002h]

ITM Stimulus Port Register 21 is shown in Table 3-195.

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Table 3-195. ITM Stimulus Port Register 21 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.23 ITM Stimulus Port Register 22 (Offset = 58h) [Reset = 00000002h]

ITM Stimulus Port Register 22 is shown in Table 3-196.

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Table 3-196. ITM Stimulus Port Register 22 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.24 ITM Stimulus Port Register 23 (Offset = 5Ch) [Reset = 00000002h]

ITM Stimulus Port Register 23 is shown in Table 3-197.

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Table 3-197. ITM Stimulus Port Register 23 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.25 ITM Stimulus Port Register 24 (Offset = 60h) [Reset = 00000002h]

ITM Stimulus Port Register 24 is shown in Table 3-198.

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Table 3-198. ITM Stimulus Port Register 24 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.26 ITM Stimulus Port Register 25 (Offset = 64h) [Reset = 00000002h]

ITM Stimulus Port Register 25 is shown in Table 3-199.

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Table 3-199. ITM Stimulus Port Register 25 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.27 ITM Stimulus Port Register 26 (Offset = 68h) [Reset = 00000002h]

ITM Stimulus Port Register 26 is shown in Table 3-200.

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Table 3-200. ITM Stimulus Port Register 26 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.28 ITM Stimulus Port Register 27 (Offset = 6Ch) [Reset = 00000002h]

ITM Stimulus Port Register 27 is shown in Table 3-201.

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Table 3-201. ITM Stimulus Port Register 27 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.29 ITM Stimulus Port Register 28 (Offset = 70h) [Reset = 00000002h]

ITM Stimulus Port Register 28 is shown in Table 3-202.

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Table 3-202. ITM Stimulus Port Register 28 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.30 ITM Stimulus Port Register 29 (Offset = 74h) [Reset = 00000002h]

ITM Stimulus Port Register 29 is shown in Table 3-203.

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Table 3-203. ITM Stimulus Port Register 29 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.31 ITM Stimulus Port Register 30 (Offset = 78h) [Reset = 00000002h]

ITM Stimulus Port Register 30 is shown in Table 3-204.

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Table 3-204. ITM Stimulus Port Register 30 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.32 ITM Stimulus Port Register 31 (Offset = 7Ch) [Reset = 00000002h]

ITM Stimulus Port Register 31 is shown in Table 3-205.

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Table 3-205. ITM Stimulus Port Register 31 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.33 ITM Stimulus Port Register 32 (Offset = 80h) [Reset = 00000000h]

ITM Stimulus Port Register 32 is shown in Table 3-206.

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Table 3-206. ITM Stimulus Port Register 32 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.34 ITM Stimulus Port Register 33 (Offset = 84h) [Reset = 00000000h]

ITM Stimulus Port Register 33 is shown in Table 3-207.

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Table 3-207. ITM Stimulus Port Register 33 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.35 ITM Stimulus Port Register 34 (Offset = 88h) [Reset = 00000000h]

ITM Stimulus Port Register 34 is shown in Table 3-208.

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Table 3-208. ITM Stimulus Port Register 34 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.36 ITM Stimulus Port Register 35 (Offset = 8Ch) [Reset = 00000000h]

ITM Stimulus Port Register 35 is shown in Table 3-209.

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Table 3-209. ITM Stimulus Port Register 35 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.37 ITM Stimulus Port Register 36 (Offset = 90h) [Reset = 00000000h]

ITM Stimulus Port Register 36 is shown in Table 3-210.

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Table 3-210. ITM Stimulus Port Register 36 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.38 ITM Stimulus Port Register 37 (Offset = 94h) [Reset = 00000000h]

ITM Stimulus Port Register 37 is shown in Table 3-211.

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Table 3-211. ITM Stimulus Port Register 37 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.39 ITM Stimulus Port Register 38 (Offset = 98h) [Reset = 00000000h]

ITM Stimulus Port Register 38 is shown in Table 3-212.

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Table 3-212. ITM Stimulus Port Register 38 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.40 ITM Stimulus Port Register 39 (Offset = 9Ch) [Reset = 00000000h]

ITM Stimulus Port Register 39 is shown in Table 3-213.

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Table 3-213. ITM Stimulus Port Register 39 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.41 ITM Stimulus Port Register 40 (Offset = A0h) [Reset = 00000000h]

ITM Stimulus Port Register 40 is shown in Table 3-214.

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Table 3-214. ITM Stimulus Port Register 40 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.42 ITM Stimulus Port Register 41 (Offset = A4h) [Reset = 00000000h]

ITM Stimulus Port Register 41 is shown in Table 3-215.

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Table 3-215. ITM Stimulus Port Register 41 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.43 ITM Stimulus Port Register 42 (Offset = A8h) [Reset = 00000000h]

ITM Stimulus Port Register 42 is shown in Table 3-216.

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Table 3-216. ITM Stimulus Port Register 42 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.44 ITM Stimulus Port Register 43 (Offset = ACh) [Reset = 00000000h]

ITM Stimulus Port Register 43 is shown in Table 3-217.

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Table 3-217. ITM Stimulus Port Register 43 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.45 ITM Stimulus Port Register 44 (Offset = B0h) [Reset = 00000000h]

ITM Stimulus Port Register 44 is shown in Table 3-218.

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Table 3-218. ITM Stimulus Port Register 44 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.46 ITM Stimulus Port Register 45 (Offset = B4h) [Reset = 00000000h]

ITM Stimulus Port Register 45 is shown in Table 3-219.

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Table 3-219. ITM Stimulus Port Register 45 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.47 ITM Stimulus Port Register 46 (Offset = B8h) [Reset = 00000000h]

ITM Stimulus Port Register 46 is shown in Table 3-220.

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Table 3-220. ITM Stimulus Port Register 46 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.48 ITM Stimulus Port Register 47 (Offset = BCh) [Reset = 00000000h]

ITM Stimulus Port Register 47 is shown in Table 3-221.

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Table 3-221. ITM Stimulus Port Register 47 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.49 ITM Stimulus Port Register 48 (Offset = C0h) [Reset = 00000000h]

ITM Stimulus Port Register 48 is shown in Table 3-222.

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Table 3-222. ITM Stimulus Port Register 48 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.50 ITM Stimulus Port Register 49 (Offset = C4h) [Reset = 00000000h]

ITM Stimulus Port Register 49 is shown in Table 3-223.

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Table 3-223. ITM Stimulus Port Register 49 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.51 ITM Stimulus Port Register 50 (Offset = C8h) [Reset = 00000000h]

ITM Stimulus Port Register 50 is shown in Table 3-224.

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Table 3-224. ITM Stimulus Port Register 50 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.52 ITM Stimulus Port Register 51 (Offset = CCh) [Reset = 00000000h]

ITM Stimulus Port Register 51 is shown in Table 3-225.

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Table 3-225. ITM Stimulus Port Register 51 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.53 ITM Stimulus Port Register 52 (Offset = D0h) [Reset = 00000000h]

ITM Stimulus Port Register 52 is shown in Table 3-226.

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Table 3-226. ITM Stimulus Port Register 52 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.54 ITM Stimulus Port Register 53 (Offset = D4h) [Reset = 00000000h]

ITM Stimulus Port Register 53 is shown in Table 3-227.

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Table 3-227. ITM Stimulus Port Register 53 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.55 ITM Stimulus Port Register 54 (Offset = D8h) [Reset = 00000000h]

ITM Stimulus Port Register 54 is shown in Table 3-228.

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Table 3-228. ITM Stimulus Port Register 54 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.56 ITM Stimulus Port Register 55 (Offset = DCh) [Reset = 00000000h]

ITM Stimulus Port Register 55 is shown in Table 3-229.

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Table 3-229. ITM Stimulus Port Register 55 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.57 ITM Stimulus Port Register 56 (Offset = E0h) [Reset = 00000000h]

ITM Stimulus Port Register 56 is shown in Table 3-230.

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Table 3-230. ITM Stimulus Port Register 56 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.58 ITM Stimulus Port Register 57 (Offset = E4h) [Reset = 00000000h]

ITM Stimulus Port Register 57 is shown in Table 3-231.

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Table 3-231. ITM Stimulus Port Register 57 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.59 ITM Stimulus Port Register 58 (Offset = E8h) [Reset = 00000000h]

ITM Stimulus Port Register 58 is shown in Table 3-232.

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Table 3-232. ITM Stimulus Port Register 58 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.60 ITM Stimulus Port Register 59 (Offset = ECh) [Reset = 00000000h]

ITM Stimulus Port Register 59 is shown in Table 3-233.

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Table 3-233. ITM Stimulus Port Register 59 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.61 ITM Stimulus Port Register 60 (Offset = F0h) [Reset = 00000000h]

ITM Stimulus Port Register 60 is shown in Table 3-234.

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Table 3-234. ITM Stimulus Port Register 60 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.62 ITM Stimulus Port Register 61 (Offset = F4h) [Reset = 00000000h]

ITM Stimulus Port Register 61 is shown in Table 3-235.

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Table 3-235. ITM Stimulus Port Register 61 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.63 ITM Stimulus Port Register 62 (Offset = F8h) [Reset = 00000000h]

ITM Stimulus Port Register 62 is shown in Table 3-236.

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Table 3-236. ITM Stimulus Port Register 62 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.64 ITM Stimulus Port Register 63 (Offset = FCh) [Reset = 00000000h]

ITM Stimulus Port Register 63 is shown in Table 3-237.

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Table 3-237. ITM Stimulus Port Register 63 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.65 ITM Stimulus Port Register 64 (Offset = 100h) [Reset = 00000000h]

ITM Stimulus Port Register 64 is shown in Table 3-238.

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Table 3-238. ITM Stimulus Port Register 64 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.66 ITM Stimulus Port Register 65 (Offset = 104h) [Reset = 00000000h]

ITM Stimulus Port Register 65 is shown in Table 3-239.

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Table 3-239. ITM Stimulus Port Register 65 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.67 ITM Stimulus Port Register 66 (Offset = 108h) [Reset = 00000000h]

ITM Stimulus Port Register 66 is shown in Table 3-240.

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Table 3-240. ITM Stimulus Port Register 66 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.68 ITM Stimulus Port Register 67 (Offset = 10Ch) [Reset = 00000000h]

ITM Stimulus Port Register 67 is shown in Table 3-241.

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Table 3-241. ITM Stimulus Port Register 67 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.69 ITM Stimulus Port Register 68 (Offset = 110h) [Reset = 00000000h]

ITM Stimulus Port Register 68 is shown in Table 3-242.

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Table 3-242. ITM Stimulus Port Register 68 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.70 ITM Stimulus Port Register 69 (Offset = 114h) [Reset = 00000000h]

ITM Stimulus Port Register 69 is shown in Table 3-243.

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Table 3-243. ITM Stimulus Port Register 69 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.71 ITM Stimulus Port Register 70 (Offset = 118h) [Reset = 00000000h]

ITM Stimulus Port Register 70 is shown in Table 3-244.

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Table 3-244. ITM Stimulus Port Register 70 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.72 ITM Stimulus Port Register 71 (Offset = 11Ch) [Reset = 00000000h]

ITM Stimulus Port Register 71 is shown in Table 3-245.

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Table 3-245. ITM Stimulus Port Register 71 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.73 ITM Stimulus Port Register 72 (Offset = 120h) [Reset = 00000000h]

ITM Stimulus Port Register 72 is shown in Table 3-246.

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Table 3-246. ITM Stimulus Port Register 72 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.74 ITM Stimulus Port Register 73 (Offset = 124h) [Reset = 00000000h]

ITM Stimulus Port Register 73 is shown in Table 3-247.

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Table 3-247. ITM Stimulus Port Register 73 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.75 ITM Stimulus Port Register 74 (Offset = 128h) [Reset = 00000000h]

ITM Stimulus Port Register 74 is shown in Table 3-248.

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Table 3-248. ITM Stimulus Port Register 74 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.76 ITM Stimulus Port Register 75 (Offset = 12Ch) [Reset = 00000000h]

ITM Stimulus Port Register 75 is shown in Table 3-249.

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Table 3-249. ITM Stimulus Port Register 75 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.77 ITM Stimulus Port Register 76 (Offset = 130h) [Reset = 00000000h]

ITM Stimulus Port Register 76 is shown in Table 3-250.

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Table 3-250. ITM Stimulus Port Register 76 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.78 ITM Stimulus Port Register 77 (Offset = 134h) [Reset = 00000000h]

ITM Stimulus Port Register 77 is shown in Table 3-251.

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Table 3-251. ITM Stimulus Port Register 77 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.79 ITM Stimulus Port Register 78 (Offset = 138h) [Reset = 00000000h]

ITM Stimulus Port Register 78 is shown in Table 3-252.

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Table 3-252. ITM Stimulus Port Register 78 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.80 ITM Stimulus Port Register 79 (Offset = 13Ch) [Reset = 00000000h]

ITM Stimulus Port Register 79 is shown in Table 3-253.

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Table 3-253. ITM Stimulus Port Register 79 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.81 ITM Stimulus Port Register 80 (Offset = 140h) [Reset = 00000000h]

ITM Stimulus Port Register 80 is shown in Table 3-254.

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Table 3-254. ITM Stimulus Port Register 80 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.82 ITM Stimulus Port Register 81 (Offset = 144h) [Reset = 00000000h]

ITM Stimulus Port Register 81 is shown in Table 3-255.

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Table 3-255. ITM Stimulus Port Register 81 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.83 ITM Stimulus Port Register 82 (Offset = 148h) [Reset = 00000000h]

ITM Stimulus Port Register 82 is shown in Table 3-256.

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Table 3-256. ITM Stimulus Port Register 82 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.84 ITM Stimulus Port Register 83 (Offset = 14Ch) [Reset = 00000000h]

ITM Stimulus Port Register 83 is shown in Table 3-257.

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Table 3-257. ITM Stimulus Port Register 83 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.85 ITM Stimulus Port Register 84 (Offset = 150h) [Reset = 00000000h]

ITM Stimulus Port Register 84 is shown in Table 3-258.

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Table 3-258. ITM Stimulus Port Register 84 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.86 ITM Stimulus Port Register 85 (Offset = 154h) [Reset = 00000000h]

ITM Stimulus Port Register 85 is shown in Table 3-259.

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Table 3-259. ITM Stimulus Port Register 85 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.87 ITM Stimulus Port Register 86 (Offset = 158h) [Reset = 00000000h]

ITM Stimulus Port Register 86 is shown in Table 3-260.

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Table 3-260. ITM Stimulus Port Register 86 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.88 ITM Stimulus Port Register 87 (Offset = 15Ch) [Reset = 00000000h]

ITM Stimulus Port Register 87 is shown in Table 3-261.

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Table 3-261. ITM Stimulus Port Register 87 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.89 ITM Stimulus Port Register 88 (Offset = 160h) [Reset = 00000000h]

ITM Stimulus Port Register 88 is shown in Table 3-262.

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Table 3-262. ITM Stimulus Port Register 88 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.90 ITM Stimulus Port Register 89 (Offset = 164h) [Reset = 00000000h]

ITM Stimulus Port Register 89 is shown in Table 3-263.

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Table 3-263. ITM Stimulus Port Register 89 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.91 ITM Stimulus Port Register 90 (Offset = 168h) [Reset = 00000000h]

ITM Stimulus Port Register 90 is shown in Table 3-264.

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Table 3-264. ITM Stimulus Port Register 90 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.92 ITM Stimulus Port Register 91 (Offset = 16Ch) [Reset = 00000000h]

ITM Stimulus Port Register 91 is shown in Table 3-265.

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Table 3-265. ITM Stimulus Port Register 91 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.93 ITM Stimulus Port Register 92 (Offset = 170h) [Reset = 00000000h]

ITM Stimulus Port Register 92 is shown in Table 3-266.

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Table 3-266. ITM Stimulus Port Register 92 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.94 ITM Stimulus Port Register 93 (Offset = 174h) [Reset = 00000000h]

ITM Stimulus Port Register 93 is shown in Table 3-267.

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Table 3-267. ITM Stimulus Port Register 93 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.95 ITM Stimulus Port Register 94 (Offset = 178h) [Reset = 00000000h]

ITM Stimulus Port Register 94 is shown in Table 3-268.

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Table 3-268. ITM Stimulus Port Register 94 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.96 ITM Stimulus Port Register 95 (Offset = 17Ch) [Reset = 00000000h]

ITM Stimulus Port Register 95 is shown in Table 3-269.

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Table 3-269. ITM Stimulus Port Register 95 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.97 ITM Stimulus Port Register 96 (Offset = 180h) [Reset = 00000000h]

ITM Stimulus Port Register 96 is shown in Table 3-270.

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Table 3-270. ITM Stimulus Port Register 96 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.98 ITM Stimulus Port Register 97 (Offset = 184h) [Reset = 00000000h]

ITM Stimulus Port Register 97 is shown in Table 3-271.

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Table 3-271. ITM Stimulus Port Register 97 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.99 ITM Stimulus Port Register 98 (Offset = 188h) [Reset = 00000000h]

ITM Stimulus Port Register 98 is shown in Table 3-272.

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Table 3-272. ITM Stimulus Port Register 98 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.100 ITM Stimulus Port Register 99 (Offset = 18Ch) [Reset = 00000000h]

ITM Stimulus Port Register 99 is shown in Table 3-273.

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Table 3-273. ITM Stimulus Port Register 99 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.101 ITM Stimulus Port Register 100 (Offset = 190h) [Reset = 00000000h]

ITM Stimulus Port Register 100 is shown in Table 3-274.

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Table 3-274. ITM Stimulus Port Register 100 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.102 ITM Stimulus Port Register 101 (Offset = 194h) [Reset = 00000000h]

ITM Stimulus Port Register 101 is shown in Table 3-275.

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Table 3-275. ITM Stimulus Port Register 101 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.103 ITM Stimulus Port Register 102 (Offset = 198h) [Reset = 00000000h]

ITM Stimulus Port Register 102 is shown in Table 3-276.

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Table 3-276. ITM Stimulus Port Register 102 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.104 ITM Stimulus Port Register 103 (Offset = 19Ch) [Reset = 00000000h]

ITM Stimulus Port Register 103 is shown in Table 3-277.

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Table 3-277. ITM Stimulus Port Register 103 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.105 ITM Stimulus Port Register 104 (Offset = 1A0h) [Reset = 00000000h]

ITM Stimulus Port Register 104 is shown in Table 3-278.

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Table 3-278. ITM Stimulus Port Register 104 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.106 ITM Stimulus Port Register 105 (Offset = 1A4h) [Reset = 00000000h]

ITM Stimulus Port Register 105 is shown in Table 3-279.

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Table 3-279. ITM Stimulus Port Register 105 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.107 ITM Stimulus Port Register 106 (Offset = 1A8h) [Reset = 00000000h]

ITM Stimulus Port Register 106 is shown in Table 3-280.

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Table 3-280. ITM Stimulus Port Register 106 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.108 ITM Stimulus Port Register 107 (Offset = 1ACh) [Reset = 00000000h]

ITM Stimulus Port Register 107 is shown in Table 3-281.

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Table 3-281. ITM Stimulus Port Register 107 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.109 ITM Stimulus Port Register 108 (Offset = 1B0h) [Reset = 00000000h]

ITM Stimulus Port Register 108 is shown in Table 3-282.

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Table 3-282. ITM Stimulus Port Register 108 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.110 ITM Stimulus Port Register 109 (Offset = 1B4h) [Reset = 00000000h]

ITM Stimulus Port Register 109 is shown in Table 3-283.

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Table 3-283. ITM Stimulus Port Register 109 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.111 ITM Stimulus Port Register 110 (Offset = 1B8h) [Reset = 00000000h]

ITM Stimulus Port Register 110 is shown in Table 3-284.

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Table 3-284. ITM Stimulus Port Register 110 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.112 ITM Stimulus Port Register 111 (Offset = 1BCh) [Reset = 00000000h]

ITM Stimulus Port Register 111 is shown in Table 3-285.

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Table 3-285. ITM Stimulus Port Register 111 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.113 ITM Stimulus Port Register 112 (Offset = 1C0h) [Reset = 00000000h]

ITM Stimulus Port Register 112 is shown in Table 3-286.

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Table 3-286. ITM Stimulus Port Register 112 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.114 ITM Stimulus Port Register 113 (Offset = 1C4h) [Reset = 00000000h]

ITM Stimulus Port Register 113 is shown in Table 3-287.

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Table 3-287. ITM Stimulus Port Register 113 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.115 ITM Stimulus Port Register 114 (Offset = 1C8h) [Reset = 00000000h]

ITM Stimulus Port Register 114 is shown in Table 3-288.

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Table 3-288. ITM Stimulus Port Register 114 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.116 ITM Stimulus Port Register 115 (Offset = 1CCh) [Reset = 00000000h]

ITM Stimulus Port Register 115 is shown in Table 3-289.

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Table 3-289. ITM Stimulus Port Register 115 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.117 ITM Stimulus Port Register 116 (Offset = 1D0h) [Reset = 00000000h]

ITM Stimulus Port Register 116 is shown in Table 3-290.

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Table 3-290. ITM Stimulus Port Register 116 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.118 ITM Stimulus Port Register 117 (Offset = 1D4h) [Reset = 00000000h]

ITM Stimulus Port Register 117 is shown in Table 3-291.

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Table 3-291. ITM Stimulus Port Register 117 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.119 ITM Stimulus Port Register 118 (Offset = 1D8h) [Reset = 00000000h]

ITM Stimulus Port Register 118 is shown in Table 3-292.

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Table 3-292. ITM Stimulus Port Register 118 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.120 ITM Stimulus Port Register 119 (Offset = 1DCh) [Reset = 00000000h]

ITM Stimulus Port Register 119 is shown in Table 3-293.

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Table 3-293. ITM Stimulus Port Register 119 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.121 ITM Stimulus Port Register 120 (Offset = 1E0h) [Reset = 00000000h]

ITM Stimulus Port Register 120 is shown in Table 3-294.

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Table 3-294. ITM Stimulus Port Register 120 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.122 ITM Stimulus Port Register 121 (Offset = 1E4h) [Reset = 00000000h]

ITM Stimulus Port Register 121 is shown in Table 3-295.

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Table 3-295. ITM Stimulus Port Register 121 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.123 ITM Stimulus Port Register 122 (Offset = 1E8h) [Reset = 00000000h]

ITM Stimulus Port Register 122 is shown in Table 3-296.

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Table 3-296. ITM Stimulus Port Register 122 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.124 ITM Stimulus Port Register 123 (Offset = 1ECh) [Reset = 00000000h]

ITM Stimulus Port Register 123 is shown in Table 3-297.

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Table 3-297. ITM Stimulus Port Register 123 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.125 ITM Stimulus Port Register 124 (Offset = 1F0h) [Reset = 00000000h]

ITM Stimulus Port Register 124 is shown in Table 3-298.

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Table 3-298. ITM Stimulus Port Register 124 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.126 ITM Stimulus Port Register 125 (Offset = 1F4h) [Reset = 00000000h]

ITM Stimulus Port Register 125 is shown in Table 3-299.

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Table 3-299. ITM Stimulus Port Register 125 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.127 ITM Stimulus Port Register 126 (Offset = 1F8h) [Reset = 00000000h]

ITM Stimulus Port Register 126 is shown in Table 3-300.

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Table 3-300. ITM Stimulus Port Register 126 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.128 ITM Stimulus Port Register 127 (Offset = 1FCh) [Reset = 00000000h]

ITM Stimulus Port Register 127 is shown in Table 3-301.

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Table 3-301. ITM Stimulus Port Register 127 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.129 ITM Stimulus Port Register 128 (Offset = 200h) [Reset = 00000000h]

ITM Stimulus Port Register 128 is shown in Table 3-302.

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Table 3-302. ITM Stimulus Port Register 128 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.130 ITM Stimulus Port Register 129 (Offset = 204h) [Reset = 00000000h]

ITM Stimulus Port Register 129 is shown in Table 3-303.

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Table 3-303. ITM Stimulus Port Register 129 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.131 ITM Stimulus Port Register 130 (Offset = 208h) [Reset = 00000000h]

ITM Stimulus Port Register 130 is shown in Table 3-304.

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Table 3-304. ITM Stimulus Port Register 130 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.132 ITM Stimulus Port Register 131 (Offset = 20Ch) [Reset = 00000000h]

ITM Stimulus Port Register 131 is shown in Table 3-305.

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Table 3-305. ITM Stimulus Port Register 131 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.133 ITM Stimulus Port Register 132 (Offset = 210h) [Reset = 00000000h]

ITM Stimulus Port Register 132 is shown in Table 3-306.

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Table 3-306. ITM Stimulus Port Register 132 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.134 ITM Stimulus Port Register 133 (Offset = 214h) [Reset = 00000000h]

ITM Stimulus Port Register 133 is shown in Table 3-307.

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Table 3-307. ITM Stimulus Port Register 133 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.135 ITM Stimulus Port Register 134 (Offset = 218h) [Reset = 00000000h]

ITM Stimulus Port Register 134 is shown in Table 3-308.

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Table 3-308. ITM Stimulus Port Register 134 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.136 ITM Stimulus Port Register 135 (Offset = 21Ch) [Reset = 00000000h]

ITM Stimulus Port Register 135 is shown in Table 3-309.

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Table 3-309. ITM Stimulus Port Register 135 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.137 ITM Stimulus Port Register 136 (Offset = 220h) [Reset = 00000000h]

ITM Stimulus Port Register 136 is shown in Table 3-310.

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Table 3-310. ITM Stimulus Port Register 136 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.138 ITM Stimulus Port Register 137 (Offset = 224h) [Reset = 00000000h]

ITM Stimulus Port Register 137 is shown in Table 3-311.

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Table 3-311. ITM Stimulus Port Register 137 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.139 ITM Stimulus Port Register 138 (Offset = 228h) [Reset = 00000000h]

ITM Stimulus Port Register 138 is shown in Table 3-312.

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Table 3-312. ITM Stimulus Port Register 138 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.140 ITM Stimulus Port Register 139 (Offset = 22Ch) [Reset = 00000000h]

ITM Stimulus Port Register 139 is shown in Table 3-313.

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Table 3-313. ITM Stimulus Port Register 139 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.141 ITM Stimulus Port Register 140 (Offset = 230h) [Reset = 00000000h]

ITM Stimulus Port Register 140 is shown in Table 3-314.

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Table 3-314. ITM Stimulus Port Register 140 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.142 ITM Stimulus Port Register 141 (Offset = 234h) [Reset = 00000000h]

ITM Stimulus Port Register 141 is shown in Table 3-315.

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Table 3-315. ITM Stimulus Port Register 141 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.143 ITM Stimulus Port Register 142 (Offset = 238h) [Reset = 00000000h]

ITM Stimulus Port Register 142 is shown in Table 3-316.

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Table 3-316. ITM Stimulus Port Register 142 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.144 ITM Stimulus Port Register 143 (Offset = 23Ch) [Reset = 00000000h]

ITM Stimulus Port Register 143 is shown in Table 3-317.

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Table 3-317. ITM Stimulus Port Register 143 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.145 ITM Stimulus Port Register 144 (Offset = 240h) [Reset = 00000000h]

ITM Stimulus Port Register 144 is shown in Table 3-318.

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Table 3-318. ITM Stimulus Port Register 144 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.146 ITM Stimulus Port Register 145 (Offset = 244h) [Reset = 00000000h]

ITM Stimulus Port Register 145 is shown in Table 3-319.

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Table 3-319. ITM Stimulus Port Register 145 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.147 ITM Stimulus Port Register 146 (Offset = 248h) [Reset = 00000000h]

ITM Stimulus Port Register 146 is shown in Table 3-320.

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Table 3-320. ITM Stimulus Port Register 146 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.148 ITM Stimulus Port Register 147 (Offset = 24Ch) [Reset = 00000000h]

ITM Stimulus Port Register 147 is shown in Table 3-321.

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Table 3-321. ITM Stimulus Port Register 147 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.149 ITM Stimulus Port Register 148 (Offset = 250h) [Reset = 00000000h]

ITM Stimulus Port Register 148 is shown in Table 3-322.

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Table 3-322. ITM Stimulus Port Register 148 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.150 ITM Stimulus Port Register 149 (Offset = 254h) [Reset = 00000000h]

ITM Stimulus Port Register 149 is shown in Table 3-323.

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Table 3-323. ITM Stimulus Port Register 149 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.151 ITM Stimulus Port Register 150 (Offset = 258h) [Reset = 00000000h]

ITM Stimulus Port Register 150 is shown in Table 3-324.

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Table 3-324. ITM Stimulus Port Register 150 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.152 ITM Stimulus Port Register 151 (Offset = 25Ch) [Reset = 00000000h]

ITM Stimulus Port Register 151 is shown in Table 3-325.

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Table 3-325. ITM Stimulus Port Register 151 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.153 ITM Stimulus Port Register 152 (Offset = 260h) [Reset = 00000000h]

ITM Stimulus Port Register 152 is shown in Table 3-326.

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Table 3-326. ITM Stimulus Port Register 152 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.154 ITM Stimulus Port Register 153 (Offset = 264h) [Reset = 00000000h]

ITM Stimulus Port Register 153 is shown in Table 3-327.

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Table 3-327. ITM Stimulus Port Register 153 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.155 ITM Stimulus Port Register 154 (Offset = 268h) [Reset = 00000000h]

ITM Stimulus Port Register 154 is shown in Table 3-328.

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Table 3-328. ITM Stimulus Port Register 154 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.156 ITM Stimulus Port Register 155 (Offset = 26Ch) [Reset = 00000000h]

ITM Stimulus Port Register 155 is shown in Table 3-329.

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Table 3-329. ITM Stimulus Port Register 155 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.157 ITM Stimulus Port Register 156 (Offset = 270h) [Reset = 00000000h]

ITM Stimulus Port Register 156 is shown in Table 3-330.

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Table 3-330. ITM Stimulus Port Register 156 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.158 ITM Stimulus Port Register 157 (Offset = 274h) [Reset = 00000000h]

ITM Stimulus Port Register 157 is shown in Table 3-331.

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Table 3-331. ITM Stimulus Port Register 157 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.159 ITM Stimulus Port Register 158 (Offset = 278h) [Reset = 00000000h]

ITM Stimulus Port Register 158 is shown in Table 3-332.

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Table 3-332. ITM Stimulus Port Register 158 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.160 ITM Stimulus Port Register 159 (Offset = 27Ch) [Reset = 00000000h]

ITM Stimulus Port Register 159 is shown in Table 3-333.

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Table 3-333. ITM Stimulus Port Register 159 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.161 ITM Stimulus Port Register 160 (Offset = 280h) [Reset = 00000000h]

ITM Stimulus Port Register 160 is shown in Table 3-334.

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Table 3-334. ITM Stimulus Port Register 160 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.162 ITM Stimulus Port Register 161 (Offset = 284h) [Reset = 00000000h]

ITM Stimulus Port Register 161 is shown in Table 3-335.

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Table 3-335. ITM Stimulus Port Register 161 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.163 ITM Stimulus Port Register 162 (Offset = 288h) [Reset = 00000000h]

ITM Stimulus Port Register 162 is shown in Table 3-336.

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Table 3-336. ITM Stimulus Port Register 162 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.164 ITM Stimulus Port Register 163 (Offset = 28Ch) [Reset = 00000000h]

ITM Stimulus Port Register 163 is shown in Table 3-337.

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Table 3-337. ITM Stimulus Port Register 163 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.165 ITM Stimulus Port Register 164 (Offset = 290h) [Reset = 00000000h]

ITM Stimulus Port Register 164 is shown in Table 3-338.

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Table 3-338. ITM Stimulus Port Register 164 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.166 ITM Stimulus Port Register 165 (Offset = 294h) [Reset = 00000000h]

ITM Stimulus Port Register 165 is shown in Table 3-339.

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Table 3-339. ITM Stimulus Port Register 165 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.167 ITM Stimulus Port Register 166 (Offset = 298h) [Reset = 00000000h]

ITM Stimulus Port Register 166 is shown in Table 3-340.

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Table 3-340. ITM Stimulus Port Register 166 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.168 ITM Stimulus Port Register 167 (Offset = 29Ch) [Reset = 00000000h]

ITM Stimulus Port Register 167 is shown in Table 3-341.

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Table 3-341. ITM Stimulus Port Register 167 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.169 ITM Stimulus Port Register 168 (Offset = 2A0h) [Reset = 00000000h]

ITM Stimulus Port Register 168 is shown in Table 3-342.

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Table 3-342. ITM Stimulus Port Register 168 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.170 ITM Stimulus Port Register 169 (Offset = 2A4h) [Reset = 00000000h]

ITM Stimulus Port Register 169 is shown in Table 3-343.

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Table 3-343. ITM Stimulus Port Register 169 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.171 ITM Stimulus Port Register 170 (Offset = 2A8h) [Reset = 00000000h]

ITM Stimulus Port Register 170 is shown in Table 3-344.

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Table 3-344. ITM Stimulus Port Register 170 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.172 ITM Stimulus Port Register 171 (Offset = 2ACh) [Reset = 00000000h]

ITM Stimulus Port Register 171 is shown in Table 3-345.

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Table 3-345. ITM Stimulus Port Register 171 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.173 ITM Stimulus Port Register 172 (Offset = 2B0h) [Reset = 00000000h]

ITM Stimulus Port Register 172 is shown in Table 3-346.

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Table 3-346. ITM Stimulus Port Register 172 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.174 ITM Stimulus Port Register 173 (Offset = 2B4h) [Reset = 00000000h]

ITM Stimulus Port Register 173 is shown in Table 3-347.

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Table 3-347. ITM Stimulus Port Register 173 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.175 ITM Stimulus Port Register 174 (Offset = 2B8h) [Reset = 00000000h]

ITM Stimulus Port Register 174 is shown in Table 3-348.

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Table 3-348. ITM Stimulus Port Register 174 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.176 ITM Stimulus Port Register 175 (Offset = 2BCh) [Reset = 00000000h]

ITM Stimulus Port Register 175 is shown in Table 3-349.

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Table 3-349. ITM Stimulus Port Register 175 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.177 ITM Stimulus Port Register 176 (Offset = 2C0h) [Reset = 00000000h]

ITM Stimulus Port Register 176 is shown in Table 3-350.

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Table 3-350. ITM Stimulus Port Register 176 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.178 ITM Stimulus Port Register 177 (Offset = 2C4h) [Reset = 00000000h]

ITM Stimulus Port Register 177 is shown in Table 3-351.

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Table 3-351. ITM Stimulus Port Register 177 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.179 ITM Stimulus Port Register 178 (Offset = 2C8h) [Reset = 00000000h]

ITM Stimulus Port Register 178 is shown in Table 3-352.

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Table 3-352. ITM Stimulus Port Register 178 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.180 ITM Stimulus Port Register 179 (Offset = 2CCh) [Reset = 00000000h]

ITM Stimulus Port Register 179 is shown in Table 3-353.

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Table 3-353. ITM Stimulus Port Register 179 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.181 ITM Stimulus Port Register 180 (Offset = 2D0h) [Reset = 00000000h]

ITM Stimulus Port Register 180 is shown in Table 3-354.

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Table 3-354. ITM Stimulus Port Register 180 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.182 ITM Stimulus Port Register 181 (Offset = 2D4h) [Reset = 00000000h]

ITM Stimulus Port Register 181 is shown in Table 3-355.

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Table 3-355. ITM Stimulus Port Register 181 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.183 ITM Stimulus Port Register 182 (Offset = 2D8h) [Reset = 00000000h]

ITM Stimulus Port Register 182 is shown in Table 3-356.

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Table 3-356. ITM Stimulus Port Register 182 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.184 ITM Stimulus Port Register 183 (Offset = 2DCh) [Reset = 00000000h]

ITM Stimulus Port Register 183 is shown in Table 3-357.

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Table 3-357. ITM Stimulus Port Register 183 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.185 ITM Stimulus Port Register 184 (Offset = 2E0h) [Reset = 00000000h]

ITM Stimulus Port Register 184 is shown in Table 3-358.

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Table 3-358. ITM Stimulus Port Register 184 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.186 ITM Stimulus Port Register 185 (Offset = 2E4h) [Reset = 00000000h]

ITM Stimulus Port Register 185 is shown in Table 3-359.

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Table 3-359. ITM Stimulus Port Register 185 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.187 ITM Stimulus Port Register 186 (Offset = 2E8h) [Reset = 00000000h]

ITM Stimulus Port Register 186 is shown in Table 3-360.

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Table 3-360. ITM Stimulus Port Register 186 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.188 ITM Stimulus Port Register 187 (Offset = 2ECh) [Reset = 00000000h]

ITM Stimulus Port Register 187 is shown in Table 3-361.

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Table 3-361. ITM Stimulus Port Register 187 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.189 ITM Stimulus Port Register 188 (Offset = 2F0h) [Reset = 00000000h]

ITM Stimulus Port Register 188 is shown in Table 3-362.

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Table 3-362. ITM Stimulus Port Register 188 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.190 ITM Stimulus Port Register 189 (Offset = 2F4h) [Reset = 00000000h]

ITM Stimulus Port Register 189 is shown in Table 3-363.

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Table 3-363. ITM Stimulus Port Register 189 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.191 ITM Stimulus Port Register 190 (Offset = 2F8h) [Reset = 00000000h]

ITM Stimulus Port Register 190 is shown in Table 3-364.

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Table 3-364. ITM Stimulus Port Register 190 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.192 ITM Stimulus Port Register 191 (Offset = 2FCh) [Reset = 00000000h]

ITM Stimulus Port Register 191 is shown in Table 3-365.

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Table 3-365. ITM Stimulus Port Register 191 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.193 ITM Stimulus Port Register 192 (Offset = 300h) [Reset = 00000000h]

ITM Stimulus Port Register 192 is shown in Table 3-366.

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Table 3-366. ITM Stimulus Port Register 192 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.194 ITM Stimulus Port Register 193 (Offset = 304h) [Reset = 00000000h]

ITM Stimulus Port Register 193 is shown in Table 3-367.

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Table 3-367. ITM Stimulus Port Register 193 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.195 ITM Stimulus Port Register 194 (Offset = 308h) [Reset = 00000000h]

ITM Stimulus Port Register 194 is shown in Table 3-368.

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Table 3-368. ITM Stimulus Port Register 194 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.196 ITM Stimulus Port Register 195 (Offset = 30Ch) [Reset = 00000000h]

ITM Stimulus Port Register 195 is shown in Table 3-369.

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Table 3-369. ITM Stimulus Port Register 195 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.197 ITM Stimulus Port Register 196 (Offset = 310h) [Reset = 00000000h]

ITM Stimulus Port Register 196 is shown in Table 3-370.

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Table 3-370. ITM Stimulus Port Register 196 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.198 ITM Stimulus Port Register 197 (Offset = 314h) [Reset = 00000000h]

ITM Stimulus Port Register 197 is shown in Table 3-371.

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Table 3-371. ITM Stimulus Port Register 197 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.199 ITM Stimulus Port Register 198 (Offset = 318h) [Reset = 00000000h]

ITM Stimulus Port Register 198 is shown in Table 3-372.

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Table 3-372. ITM Stimulus Port Register 198 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.200 ITM Stimulus Port Register 199 (Offset = 31Ch) [Reset = 00000000h]

ITM Stimulus Port Register 199 is shown in Table 3-373.

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Table 3-373. ITM Stimulus Port Register 199 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.201 ITM Stimulus Port Register 200 (Offset = 320h) [Reset = 00000000h]

ITM Stimulus Port Register 200 is shown in Table 3-374.

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Table 3-374. ITM Stimulus Port Register 200 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.202 ITM Stimulus Port Register 201 (Offset = 324h) [Reset = 00000000h]

ITM Stimulus Port Register 201 is shown in Table 3-375.

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Table 3-375. ITM Stimulus Port Register 201 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.203 ITM Stimulus Port Register 202 (Offset = 328h) [Reset = 00000000h]

ITM Stimulus Port Register 202 is shown in Table 3-376.

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Table 3-376. ITM Stimulus Port Register 202 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.204 ITM Stimulus Port Register 203 (Offset = 32Ch) [Reset = 00000000h]

ITM Stimulus Port Register 203 is shown in Table 3-377.

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Table 3-377. ITM Stimulus Port Register 203 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.205 ITM Stimulus Port Register 204 (Offset = 330h) [Reset = 00000000h]

ITM Stimulus Port Register 204 is shown in Table 3-378.

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Table 3-378. ITM Stimulus Port Register 204 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.206 ITM Stimulus Port Register 205 (Offset = 334h) [Reset = 00000000h]

ITM Stimulus Port Register 205 is shown in Table 3-379.

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Table 3-379. ITM Stimulus Port Register 205 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.207 ITM Stimulus Port Register 206 (Offset = 338h) [Reset = 00000000h]

ITM Stimulus Port Register 206 is shown in Table 3-380.

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Table 3-380. ITM Stimulus Port Register 206 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.208 ITM Stimulus Port Register 207 (Offset = 33Ch) [Reset = 00000000h]

ITM Stimulus Port Register 207 is shown in Table 3-381.

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Table 3-381. ITM Stimulus Port Register 207 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.209 ITM Stimulus Port Register 208 (Offset = 340h) [Reset = 00000000h]

ITM Stimulus Port Register 208 is shown in Table 3-382.

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Table 3-382. ITM Stimulus Port Register 208 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.210 ITM Stimulus Port Register 209 (Offset = 344h) [Reset = 00000000h]

ITM Stimulus Port Register 209 is shown in Table 3-383.

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Table 3-383. ITM Stimulus Port Register 209 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.211 ITM Stimulus Port Register 210 (Offset = 348h) [Reset = 00000000h]

ITM Stimulus Port Register 210 is shown in Table 3-384.

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Table 3-384. ITM Stimulus Port Register 210 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.212 ITM Stimulus Port Register 211 (Offset = 34Ch) [Reset = 00000000h]

ITM Stimulus Port Register 211 is shown in Table 3-385.

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Table 3-385. ITM Stimulus Port Register 211 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.213 ITM Stimulus Port Register 212 (Offset = 350h) [Reset = 00000000h]

ITM Stimulus Port Register 212 is shown in Table 3-386.

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Table 3-386. ITM Stimulus Port Register 212 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.214 ITM Stimulus Port Register 213 (Offset = 354h) [Reset = 00000000h]

ITM Stimulus Port Register 213 is shown in Table 3-387.

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Table 3-387. ITM Stimulus Port Register 213 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.215 ITM Stimulus Port Register 214 (Offset = 358h) [Reset = 00000000h]

ITM Stimulus Port Register 214 is shown in Table 3-388.

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Table 3-388. ITM Stimulus Port Register 214 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.216 ITM Stimulus Port Register 215 (Offset = 35Ch) [Reset = 00000000h]

ITM Stimulus Port Register 215 is shown in Table 3-389.

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Table 3-389. ITM Stimulus Port Register 215 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.217 ITM Stimulus Port Register 216 (Offset = 360h) [Reset = 00000000h]

ITM Stimulus Port Register 216 is shown in Table 3-390.

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Table 3-390. ITM Stimulus Port Register 216 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.218 ITM Stimulus Port Register 217 (Offset = 364h) [Reset = 00000000h]

ITM Stimulus Port Register 217 is shown in Table 3-391.

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Table 3-391. ITM Stimulus Port Register 217 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.219 ITM Stimulus Port Register 218 (Offset = 368h) [Reset = 00000000h]

ITM Stimulus Port Register 218 is shown in Table 3-392.

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Table 3-392. ITM Stimulus Port Register 218 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.220 ITM Stimulus Port Register 219 (Offset = 36Ch) [Reset = 00000000h]

ITM Stimulus Port Register 219 is shown in Table 3-393.

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Table 3-393. ITM Stimulus Port Register 219 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.221 ITM Stimulus Port Register 220 (Offset = 370h) [Reset = 00000000h]

ITM Stimulus Port Register 220 is shown in Table 3-394.

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Table 3-394. ITM Stimulus Port Register 220 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.222 ITM Stimulus Port Register 221 (Offset = 374h) [Reset = 00000000h]

ITM Stimulus Port Register 221 is shown in Table 3-395.

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Table 3-395. ITM Stimulus Port Register 221 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.223 ITM Stimulus Port Register 222 (Offset = 378h) [Reset = 00000000h]

ITM Stimulus Port Register 222 is shown in Table 3-396.

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Table 3-396. ITM Stimulus Port Register 222 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.224 ITM Stimulus Port Register 223 (Offset = 37Ch) [Reset = 00000000h]

ITM Stimulus Port Register 223 is shown in Table 3-397.

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Table 3-397. ITM Stimulus Port Register 223 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.225 ITM Stimulus Port Register 224 (Offset = 380h) [Reset = 00000000h]

ITM Stimulus Port Register 224 is shown in Table 3-398.

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Table 3-398. ITM Stimulus Port Register 224 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.226 ITM Stimulus Port Register 225 (Offset = 384h) [Reset = 00000000h]

ITM Stimulus Port Register 225 is shown in Table 3-399.

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Table 3-399. ITM Stimulus Port Register 225 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.227 ITM Stimulus Port Register 226 (Offset = 388h) [Reset = 00000000h]

ITM Stimulus Port Register 226 is shown in Table 3-400.

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Table 3-400. ITM Stimulus Port Register 226 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.228 ITM Stimulus Port Register 227 (Offset = 38Ch) [Reset = 00000000h]

ITM Stimulus Port Register 227 is shown in Table 3-401.

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Table 3-401. ITM Stimulus Port Register 227 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.229 ITM Stimulus Port Register 228 (Offset = 390h) [Reset = 00000000h]

ITM Stimulus Port Register 228 is shown in Table 3-402.

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Table 3-402. ITM Stimulus Port Register 228 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.230 ITM Stimulus Port Register 229 (Offset = 394h) [Reset = 00000000h]

ITM Stimulus Port Register 229 is shown in Table 3-403.

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Table 3-403. ITM Stimulus Port Register 229 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.231 ITM Stimulus Port Register 230 (Offset = 398h) [Reset = 00000000h]

ITM Stimulus Port Register 230 is shown in Table 3-404.

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Table 3-404. ITM Stimulus Port Register 230 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.232 ITM Stimulus Port Register 231 (Offset = 39Ch) [Reset = 00000000h]

ITM Stimulus Port Register 231 is shown in Table 3-405.

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Table 3-405. ITM Stimulus Port Register 231 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.233 ITM Stimulus Port Register 232 (Offset = 3A0h) [Reset = 00000000h]

ITM Stimulus Port Register 232 is shown in Table 3-406.

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Table 3-406. ITM Stimulus Port Register 232 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.234 ITM Stimulus Port Register 233 (Offset = 3A4h) [Reset = 00000000h]

ITM Stimulus Port Register 233 is shown in Table 3-407.

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Table 3-407. ITM Stimulus Port Register 233 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.235 ITM Stimulus Port Register 234 (Offset = 3A8h) [Reset = 00000000h]

ITM Stimulus Port Register 234 is shown in Table 3-408.

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Table 3-408. ITM Stimulus Port Register 234 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.236 ITM Stimulus Port Register 235 (Offset = 3ACh) [Reset = 00000000h]

ITM Stimulus Port Register 235 is shown in Table 3-409.

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Table 3-409. ITM Stimulus Port Register 235 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.237 ITM Stimulus Port Register 236 (Offset = 3B0h) [Reset = 00000000h]

ITM Stimulus Port Register 236 is shown in Table 3-410.

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Table 3-410. ITM Stimulus Port Register 236 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.238 ITM Stimulus Port Register 237 (Offset = 3B4h) [Reset = 00000000h]

ITM Stimulus Port Register 237 is shown in Table 3-411.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 3-411. ITM Stimulus Port Register 237 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.239 ITM Stimulus Port Register 238 (Offset = 3B8h) [Reset = 00000000h]

ITM Stimulus Port Register 238 is shown in Table 3-412.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 3-412. ITM Stimulus Port Register 238 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.240 ITM Stimulus Port Register 239 (Offset = 3BCh) [Reset = 00000000h]

ITM Stimulus Port Register 239 is shown in Table 3-413.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 3-413. ITM Stimulus Port Register 239 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.241 ITM Stimulus Port Register 240 (Offset = 3C0h) [Reset = 00000000h]

ITM Stimulus Port Register 240 is shown in Table 3-414.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 3-414. ITM Stimulus Port Register 240 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.242 ITM Stimulus Port Register 241 (Offset = 3C4h) [Reset = 00000000h]

ITM Stimulus Port Register 241 is shown in Table 3-415.

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Provides the interface for generating Instrumentation packets

Table 3-415. ITM Stimulus Port Register 241 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.243 ITM Stimulus Port Register 242 (Offset = 3C8h) [Reset = 00000000h]

ITM Stimulus Port Register 242 is shown in Table 3-416.

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Provides the interface for generating Instrumentation packets

Table 3-416. ITM Stimulus Port Register 242 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.244 ITM Stimulus Port Register 243 (Offset = 3CCh) [Reset = 00000000h]

ITM Stimulus Port Register 243 is shown in Table 3-417.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 3-417. ITM Stimulus Port Register 243 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.245 ITM Stimulus Port Register 244 (Offset = 3D0h) [Reset = 00000000h]

ITM Stimulus Port Register 244 is shown in Table 3-418.

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Provides the interface for generating Instrumentation packets

Table 3-418. ITM Stimulus Port Register 244 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.246 ITM Stimulus Port Register 245 (Offset = 3D4h) [Reset = 00000000h]

ITM Stimulus Port Register 245 is shown in Table 3-419.

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Provides the interface for generating Instrumentation packets

Table 3-419. ITM Stimulus Port Register 245 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.247 ITM Stimulus Port Register 246 (Offset = 3D8h) [Reset = 00000000h]

ITM Stimulus Port Register 246 is shown in Table 3-420.

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Provides the interface for generating Instrumentation packets

Table 3-420. ITM Stimulus Port Register 246 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.248 ITM Stimulus Port Register 247 (Offset = 3DCh) [Reset = 00000000h]

ITM Stimulus Port Register 247 is shown in Table 3-421.

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Provides the interface for generating Instrumentation packets

Table 3-421. ITM Stimulus Port Register 247 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.249 ITM Stimulus Port Register 248 (Offset = 3E0h) [Reset = 00000000h]

ITM Stimulus Port Register 248 is shown in Table 3-422.

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Provides the interface for generating Instrumentation packets

Table 3-422. ITM Stimulus Port Register 248 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.250 ITM Stimulus Port Register 249 (Offset = 3E4h) [Reset = 00000000h]

ITM Stimulus Port Register 249 is shown in Table 3-423.

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Provides the interface for generating Instrumentation packets

Table 3-423. ITM Stimulus Port Register 249 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.251 ITM Stimulus Port Register 250 (Offset = 3E8h) [Reset = 00000000h]

ITM Stimulus Port Register 250 is shown in Table 3-424.

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Provides the interface for generating Instrumentation packets

Table 3-424. ITM Stimulus Port Register 250 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.252 ITM Stimulus Port Register 251 (Offset = 3ECh) [Reset = 00000000h]

ITM Stimulus Port Register 251 is shown in Table 3-425.

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Provides the interface for generating Instrumentation packets

Table 3-425. ITM Stimulus Port Register 251 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.253 ITM Stimulus Port Register 252 (Offset = 3F0h) [Reset = 00000000h]

ITM Stimulus Port Register 252 is shown in Table 3-426.

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Provides the interface for generating Instrumentation packets

Table 3-426. ITM Stimulus Port Register 252 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.254 ITM Stimulus Port Register 253 (Offset = 3F4h) [Reset = 00000000h]

ITM Stimulus Port Register 253 is shown in Table 3-427.

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Provides the interface for generating Instrumentation packets

Table 3-427. ITM Stimulus Port Register 253 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.255 ITM Stimulus Port Register 254 (Offset = 3F8h) [Reset = 00000000h]

ITM Stimulus Port Register 254 is shown in Table 3-428.

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Provides the interface for generating Instrumentation packets

Table 3-428. ITM Stimulus Port Register 254 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.256 ITM Stimulus Port Register 255 (Offset = 3FCh) [Reset = 00000000h]

ITM Stimulus Port Register 255 is shown in Table 3-429.

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Provides the interface for generating Instrumentation packets

Table 3-429. ITM Stimulus Port Register 255 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

3.9.9.257 ITM Trace Enable Register 0 (Offset = E00h) [Reset = 00000000h]

ITM Trace Enable Register 0 is shown in Table 3-430.

Return to the Summary Table.

Provide an individual enable bit for each ITM_STIM register

Table 3-430. ITM Trace Enable Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Stimulus enable	R/W	0h	For STIMENA[m] in ITM_TER*n, controls whether ITM_STIM(32*n + m) is enabled

3.9.9.258 ITM Trace Enable Register 1 (Offset = E04h) [Reset = 00000000h]

ITM Trace Enable Register 1 is shown in Table 3-431.

Return to the Summary Table.

Provide an individual enable bit for each ITM_STIM register

Table 3-431. ITM Trace Enable Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Stimulus enable	R/W	0h	For STIMENA[m] in ITM_TER*n, controls whether ITM_STIM(32*n + m) is enabled

3.9.9.259 ITM Trace Enable Register 2 (Offset = E08h) [Reset = 00000000h]

ITM Trace Enable Register 2 is shown in Table 3-432.

Return to the Summary Table.

Provide an individual enable bit for each ITM_STIM register

Table 3-432. ITM Trace Enable Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Stimulus enable	R/W	0h	For STIMENA[m] in ITM_TER*n, controls whether ITM_STIM(32*n + m) is enabled

3.9.9.260 ITM Trace Enable Register 3 (Offset = E0Ch) [Reset = 00000000h]

ITM Trace Enable Register 3 is shown in Table 3-433.

Return to the Summary Table.

Provide an individual enable bit for each ITM_STIM register

Table 3-433. ITM Trace Enable Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Stimulus enable	R/W	0h	For STIMENA[m] in ITM_TER*n, controls whether ITM_STIM(32*n + m) is enabled

3.9.9.261 ITM Trace Enable Register 4 (Offset = E10h) [Reset = 00000000h]

ITM Trace Enable Register 4 is shown in Table 3-434.

Return to the Summary Table.

Provide an individual enable bit for each ITM_STIM register

Table 3-434. ITM Trace Enable Register 4 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Stimulus enable	R/W	0h	For STIMENA[m] in ITM_TER*n, controls whether ITM_STIM(32*n + m) is enabled

3.9.9.262 ITM Trace Enable Register 5 (Offset = E14h) [Reset = 00000000h]

ITM Trace Enable Register 5 is shown in Table 3-435.

Return to the Summary Table.

Provide an individual enable bit for each ITM_STIM register

Table 3-435. ITM Trace Enable Register 5 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Stimulus enable	R/W	0h	For STIMENA[m] in ITM_TER*n, controls whether ITM_STIM(32*n + m) is enabled

3.9.9.263 ITM Trace Enable Register 6 (Offset = E18h) [Reset = 00000000h]

ITM Trace Enable Register 6 is shown in Table 3-436.

Return to the Summary Table.

Provide an individual enable bit for each ITM_STIM register

Table 3-436. ITM Trace Enable Register 6 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Stimulus enable	R/W	0h	For STIMENA[m] in ITM_TER*n, controls whether ITM_STIM(32*n + m) is enabled

3.9.9.264 ITM Trace Enable Register 7 (Offset = E1Ch) [Reset = 00000000h]

ITM Trace Enable Register 7 is shown in Table 3-437.

Return to the Summary Table.

Provide an individual enable bit for each ITM_STIM register

Table 3-437. ITM Trace Enable Register 7 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Stimulus enable	R/W	0h	For STIMENA[m] in ITM_TER*n, controls whether ITM_STIM(32*n + m) is enabled

3.9.9.265 ITM Trace Privilege Register (Offset = E40h) [Reset = 00000000h]

ITM Trace Privilege Register is shown in Table 3-438.

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Controls which stimulus ports can be accessed by unprivileged code

Table 3-438. ITM Trace Privilege Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved, RES0
3-0	Privilege mask	R/W	0h	Bit mask to enable tracing on ITM stimulus ports

3.9.9.266 ITM Trace Control Register (Offset = E80h) [Reset = 00000000h]

ITM Trace Control Register is shown in Table 3-439.

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Configures and controls transfers through the ITM interface

Table 3-439. ITM Trace Control Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved, RES0
23	ITM busy	R	0h	Indicates whether the ITM is currently processing events
22-16	Trace bus identity	R/W	0h	Identifier for multi-source trace stream formatting. If multi-source trace is in use, the debugger must write a unique non-zero trace ID value to this field
15-12	RESERVED	R	0h	Reserved, RES0
11-10	Global timestamp frequency	R/W	0h	Defines how often the ITM generates a global timestamp, based on the global timestamp clock frequency, or disables generation of global timestamps
9-8	Timestamp prescale	R/W	0h	Local timestamp prescaler, used with the trace packet reference clock
7-6	RESERVED	R	0h	Reserved, RES0
5	Stall enable	R/W	0h	Stall the PE to guarantee delivery of Data Trace packets.
4	SWO enable	R/W	0h	Enables asynchronous clocking of the timestamp counter
3	Transmit enable	R/W	0h	Enables forwarding of hardware event packet from the DWT unit to the ITM for output to the TPIU
2	Synchronization enable	R/W	0h	Enables Synchronization packet transmission for a synchronous TPIU
1	Timestamp enable	R/W	0h	Enables Local timestamp generation
0	ITM enable	R/W	0h	Enables the ITM

3.9.9.267 INT_ATREADY Register (Offset = EF0h) [Reset = 00000000h]

INT_ATREADY is shown in Table 3-440.

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Integration Mode: Read ATB Ready

Table 3-440. INT_ATREADY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	AFVALID	R	0h	A read of this bit returns the value of AFVALID
0	ATREADY	R	0h	A read of this bit returns the value of ATREADY

3.9.9.268 INT_ATVALID Register (Offset = EF8h) [Reset = 00000000h]

INT_ATVALID is shown in Table 3-441.

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Integration Mode: Write ATB Valid

Table 3-441. INT_ATVALID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	AFREADY	W	0h	A write to this bit gives the value of AFREADY
0	ATVALID	W	0h	A write to this bit gives the value of ATVALID

3.9.9.269 ITM_ITCTRL Register (Offset = F00h) [Reset = 00000000h]

ITM_ITCTRL is shown in Table 3-442.

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Integration Mode Control Register

Table 3-442. ITM_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved, RES0
0	Integration mode enable bit	R/W	0h	Integration mode enable bit - The possible values are: 0 - The trace unit is not in integration mode. 1 - The trace unit is in integration mode. This mode enables: A debug agent to perform topology detection. SoC test software to perform integration testing.

3.9.9.270 ITM Device Architecture Register (Offset = FBCh) [Reset = 47701A01h]

ITM Device Architecture Register is shown in Table 3-443.

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Provides CoreSight discovery information for the ITM

Table 3-443. ITM Device Architecture Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	Architect	R	23Bh	Defines the architect of the component. Bits [31:28] are the JEP106 continuation code (JEP106 bank ID, minus 1) and bits [27:21] are the JEP106 ID code.
20	DEVARCH Present	R	1h	Defines that the DEVARCH register is present
19-16	Revision	R	0h	Defines the architecture revision of the component
15-12	Architecture Version	R	1h	Defines the architecture version of the component
11-0	Architecture Part	R	A01h	Defines the architecture of the component

3.9.9.271 ITM Device Type Register (Offset = FCCh) [Reset = 00000043h]

ITM Device Type Register is shown in Table 3-444.

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Provides CoreSight discovery information for the ITM

Table 3-444. ITM Device Type Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	Sub-type	R	4h	Component sub-type
3-0	Major type	R	3h	Component major type

3.9.9.272 ITM Peripheral Identification Register 4 (Offset = FD0h) [Reset = 00000004h]

ITM Peripheral Identification Register 4 is shown in Table 3-445.

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Provides CoreSight discovery information for the ITM

Table 3-445. ITM Peripheral Identification Register 4 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	4KB count	R	0h	See CoreSight Architecture Specification
3-0	JEP106 continuation code	R	4h	See CoreSight Architecture Specification

3.9.9.273 ITM Peripheral Identification Register 5 (Offset = FD4h) [Reset = 00000000h]

ITM Peripheral Identification Register 5 is shown in Table 3-446.

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Provides CoreSight discovery information for the ITM

Table 3-446. ITM Peripheral Identification Register 5 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved, RES0

3.9.9.274 ITM Peripheral Identification Register 6 (Offset = FD8h) [Reset = 00000000h]

ITM Peripheral Identification Register 6 is shown in Table 3-447.

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Provides CoreSight discovery information for the ITM

Table 3-447. ITM Peripheral Identification Register 6 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved, RES0

3.9.9.275 ITM Peripheral Identification Register 7 (Offset = FDCh) [Reset = 00000000h]

ITM Peripheral Identification Register 7 is shown in Table 3-448.

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Provides CoreSight discovery information for the ITM

Table 3-448. ITM Peripheral Identification Register 7 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved, RES0

3.9.9.276 ITM Peripheral Identification Register 0 (Offset = FE0h) [Reset = 00000021h]

ITM Peripheral Identification Register 0 is shown in Table 3-449.

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Provides CoreSight discovery information for the ITM

Table 3-449. ITM Peripheral Identification Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	Part number bits [7:0]	R	21h	See CoreSight Architecture Specification

3.9.9.277 ITM Peripheral Identification Register 1 (Offset = FE4h) [Reset = 000000BDh]

ITM Peripheral Identification Register 1 is shown in Table 3-450.

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Provides CoreSight discovery information for the ITM

Table 3-450. ITM Peripheral Identification Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	JEP106 identification code bits [3:0]	R	Bh	See CoreSight Architecture Specification
3-0	Part number bits [11:8]	R	Dh	See CoreSight Architecture Specification

3.9.9.278 ITM Peripheral Identification Register 2 (Offset = FE8h) [Reset = 0000000Bh]

ITM Peripheral Identification Register 2 is shown in Table 3-451.

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Provides CoreSight discovery information for the ITM

Table 3-451. ITM Peripheral Identification Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	Component revision	R	0h	See CoreSight Architecture Specification
3	JEDEC assignee value is used	R	1h	See CoreSight Architecture Specification
2-0	JEP106 identification code bits [6:4]	R	3h	See CoreSight Architecture Specification

3.9.9.279 ITM Peripheral Identification Register 3 (Offset = FECh) [Reset = 00000000h]

ITM Peripheral Identification Register 3 is shown in Table 3-452.

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Provides CoreSight discovery information for the ITM

Table 3-452. ITM Peripheral Identification Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	RevAnd	R	0h	See CoreSight Architecture Specification
3-0	Customer Modified	R	0h	See CoreSight Architecture Specification

3.9.9.280 ITM Component Identification Register 0 (Offset = FF0h) [Reset = 0000000Dh]

ITM Component Identification Register 0 is shown in Table 3-453.

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Provides CoreSight discovery information for the ITM

Table 3-453. ITM Component Identification Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	CoreSight component identification preamble	R	Dh	See CoreSight Architecture Specification

3.9.9.281 ITM Component Identification Register 1 (Offset = FF4h) [Reset = 00000090h]

ITM Component Identification Register 1 is shown in Table 3-454.

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Provides CoreSight discovery information for the ITM

Table 3-454. ITM Component Identification Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	CoreSight component class	R	9h	See CoreSight Architecture Specification
3-0	CoreSight component identification preamble	R	0h	See CoreSight Architecture Specification

3.9.9.282 ITM Component Identification Register 2 (Offset = FF8h) [Reset = 00000005h]

ITM Component Identification Register 2 is shown in Table 3-455.

Return to the Summary Table.

Provides CoreSight discovery information for the ITM

Table 3-455. ITM Component Identification Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	CoreSight component identification preamble	R	5h	See CoreSight Architecture Specification

3.9.9.283 ITM Component Identification Register 3 (Offset = FFCh) [Reset = 000000B1h]

ITM Component Identification Register 3 is shown in Table 3-456.

Return to the Summary Table.

Provides CoreSight discovery information for the ITM

Table 3-456. ITM Component Identification Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	CoreSight component identification preamble	R	B1h	See CoreSight Architecture Specification

3.9.10 MPU Registers

Table 3-457 lists the memory-mapped registers for the MPU registers. All register offset addresses not listed in Table 3-457 should be considered as reserved locations and the register contents should not be modified.

Table 3-457. MPU Registers

Offset	Acronym	Register Name	Section
0h	MPU_TYPE	The MPU Type Register indicates how many regions the MPU `FTSSS supports	Section 3.9.10.1
4h	MPU_CTRL	Enables the MPU and, when the MPU is enabled, controls whether the default memory map is enabled as a background region for privileged accesses, and whether the MPU is enabled for HardFaults, NMIs, and exception handlers when FAULTMASK is set to 1	Section 3.9.10.2
8h	MPU_RNR	Selects the region currently accessed by MPU_RBAR and MPU_RLAR	Section 3.9.10.3
Ch	MPU_RBAR	Provides indirect read and write access to the base address of the currently selected MPU region `FTSSS	Section 3.9.10.4
10h	MPU_RLAR	Provides indirect read and write access to the limit address of the currently selected MPU region `FTSSS	Section 3.9.10.5
14h	MPU_RBAR_A1	Provides indirect read and write access to the base address of the MPU region selected by MPU_RNR[7:2]:(1[1:0]) `FTSSS	Section 3.9.10.6
18h	MPU_RLAR_A1	Provides indirect read and write access to the limit address of the currently selected MPU region selected by MPU_RNR[7:2]:(1[1:0]) `FTSSS	Section 3.9.10.7
1Ch	MPU_RBAR_A2	Provides indirect read and write access to the base address of the MPU region selected by MPU_RNR[7:2]:(2[1:0]) `FTSSS	Section 3.9.10.8
20h	MPU_RLAR_A2	Provides indirect read and write access to the limit address of the currently selected MPU region selected by MPU_RNR[7:2]:(2[1:0]) `FTSSS	Section 3.9.10.9
24h	MPU_RBAR_A3	Provides indirect read and write access to the base address of the MPU region selected by MPU_RNR[7:2]:(3[1:0]) `FTSSS	Section 3.9.10.10
28h	MPU_RLAR_A3	Provides indirect read and write access to the limit address of the currently selected MPU region selected by MPU_RNR[7:2]:(3[1:0]) `FTSSS	Section 3.9.10.11
30h	MPU_MAIR0	Along with MPU_MAIR1, provides the memory attribute encodings corresponding to the AttrIndex values	Section 3.9.10.12
34h	MPU_MAIR1	Along with MPU_MAIR0, provides the memory attribute encodings corresponding to the AttrIndex values	Section 3.9.10.13

Complex bit access types are encoded to fit into small table cells. Table 3-458 shows the codes that are used for access types in this section.

Table 3-458. MPU Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

3.9.10.1 MPU_TYPE Register (Offset = 0h) [Reset = 00000000h]

MPU_TYPE is shown in Table 3-459.

Return to the Summary Table.

The MPU Type Register indicates how many regions the MPU `FTSSS supports

Table 3-459. MPU_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RES0	R	0h	Reserved, RES0
15-8	DREGION	R	8h	Number of regions supported by the MPU
7-1	RES0_1	R	0h	Reserved, RES0
0	SEPARATE	R	0h	Indicates support for separate instructions and data address regions

3.9.10.2 MPU_CTRL Register (Offset = 4h) [Reset = 00000000h]

MPU_CTRL is shown in Table 3-460.

Return to the Summary Table.

Enables the MPU and, when the MPU is enabled, controls whether the default memory map is enabled as a background region for privileged accesses, and whether the MPU is enabled for HardFaults, NMIs, and exception handlers when FAULTMASK is set to 1

Table 3-460. MPU_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RES0	R	0h	Reserved, RES0
2	PRIVDEFENA	R/W	0h	Controls whether the default memory map is enabled for privileged software
1	HFNMIENA	R/W	0h	Controls whether handlers executing with priority less than 0 access memory with the MPU enabled or disabled. This applies to HardFaults, NMIs, and exception handlers when FAULTMASK is set to 1
0	ENABLE	R/W	0h	Enables the MPU

3.9.10.3 MPU_RNR Register (Offset = 8h) [Reset = 00000000h]

MPU_RNR is shown in Table 3-461.

Return to the Summary Table.

Selects the region currently accessed by MPU_RBAR and MPU_RLAR

Table 3-461. MPU_RNR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RES0	R	Xh	Reserved, RES0
3	RES0_3	R	0h	Reserved, RES0
2-0	REGION	R/W	0h	Indicates the memory region accessed by MPU_RBAR and MPU_RLAR

3.9.10.4 MPU_RBAR Register (Offset = Ch) [Reset = 00000000h]

MPU_RBAR is shown in Table 3-462.

Return to the Summary Table.

Provides indirect read and write access to the base address of the currently selected MPU region `FTSSS

Table 3-462. MPU_RBAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	BASE	R/W	Xh	Contains bits [31:5] of the lower inclusive limit of the selected MPU memory region. This value is zero extended to provide the base address to be checked against
4-3	SH	R/W	0h	Defines the Shareability domain of this region for Normal memory
2-1	AP	R/W	0h	Defines the access permissions for this region
0	XN	R/W	0h	Defines whether code can be executed from this region

3.9.10.5 MPU_RLAR Register (Offset = 10h) [Reset = 00000000h]

MPU_RLAR is shown in Table 3-463.

Return to the Summary Table.

Provides indirect read and write access to the limit address of the currently selected MPU region `FTSSS

Table 3-463. MPU_RLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	LIMIT	R/W	Xh	Contains bits [31:5] of the upper inclusive limit of the selected MPU memory region. This value is postfixed with 0x1F to provide the limit address to be checked against
4	RES0	R	0h	Reserved, RES0
3-1	AttrIndx	R/W	0h	Associates a set of attributes in the MPU_MAIR0 and MPU_MAIR1 fields
0	EN	R/W	0h	Region enable

3.9.10.6 MPU_RBAR_A1 Register (Offset = 14h) [Reset = 00000000h]

MPU_RBAR_A1 is shown in Table 3-464.

Return to the Summary Table.

Provides indirect read and write access to the base address of the MPU region selected by MPU_RNR[7:2]: (1[1:0]) `FTSSS

Table 3-464. MPU_RBAR_A1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	BASE	R/W	Xh	Contains bits [31:5] of the lower inclusive limit of the selected MPU memory region. This value is zero extended to provide the base address to be checked against
4-3	SH	R/W	0h	Defines the Shareability domain of this region for Normal memory
2-1	AP	R/W	0h	Defines the access permissions for this region
0	XN	R/W	0h	Defines whether code can be executed from this region

3.9.10.7 MPU_RLAR_A1 Register (Offset = 18h) [Reset = 00000000h]

MPU_RLAR_A1 is shown in Table 3-465.

Return to the Summary Table.

Provides indirect read and write access to the limit address of the currently selected MPU region selected by MPU_RNR[7:2]:(1[1:0]) `FTSSS

Table 3-465. MPU_RLAR_A1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	LIMIT	R/W	Xh	Contains bits [31:5] of the upper inclusive limit of the selected MPU memory region. This value is postfixed with 0x1F to provide the limit address to be checked against
4	RES0	R	0h	Reserved, RES0
3-1	AttrIndx	R/W	0h	Associates a set of attributes in the MPU_MAIR0 and MPU_MAIR1 fields
0	EN	R/W	0h	Region enable

3.9.10.8 MPU_RBAR_A2 Register (Offset = 1Ch) [Reset = 00000000h]

MPU_RBAR_A2 is shown in Table 3-466.

Return to the Summary Table.

Provides indirect read and write access to the base address of the MPU region selected by MPU_RNR[7:2]: (2[1:0]) `FTSSS

Table 3-466. MPU_RBAR_A2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	BASE	R/W	Xh	Contains bits [31:5] of the lower inclusive limit of the selected MPU memory region. This value is zero extended to provide the base address to be checked against
4-3	SH	R/W	0h	Defines the Shareability domain of this region for Normal memory
2-1	AP	R/W	0h	Defines the access permissions for this region
0	XN	R/W	0h	Defines whether code can be executed from this region

3.9.10.9 MPU_RLAR_A2 Register (Offset = 20h) [Reset = 00000000h]

MPU_RLAR_A2 is shown in Table 3-467.

Return to the Summary Table.

Provides indirect read and write access to the limit address of the currently selected MPU region selected by MPU_RNR[7:2]:(2[1:0]) `FTSSS

Table 3-467. MPU_RLAR_A2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	LIMIT	R/W	Xh	Contains bits [31:5] of the upper inclusive limit of the selected MPU memory region. This value is postfixed with 0x1F to provide the limit address to be checked against
4	RES0	R	0h	Reserved, RES0
3-1	AttrIndx	R/W	0h	Associates a set of attributes in the MPU_MAIR0 and MPU_MAIR1 fields
0	EN	R/W	0h	Region enable

3.9.10.10 MPU_RBAR_A3 Register (Offset = 24h) [Reset = 00000000h]

MPU_RBAR_A3 is shown in Table 3-468.

Return to the Summary Table.

Provides indirect read and write access to the base address of the MPU region selected by MPU_RNR[7:2]: (3[1:0]) `FTSSS

Table 3-468. MPU_RBAR_A3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	BASE	R/W	Xh	Contains bits [31:5] of the lower inclusive limit of the selected MPU memory region. This value is zero extended to provide the base address to be checked against
4-3	SH	R/W	0h	Defines the Shareability domain of this region for Normal memory
2-1	AP	R/W	0h	Defines the access permissions for this region
0	XN	R/W	0h	Defines whether code can be executed from this region

3.9.10.11 MPU_RLAR_A3 Register (Offset = 28h) [Reset = 00000000h]

MPU_RLAR_A3 is shown in Table 3-469.

Return to the Summary Table.

Provides indirect read and write access to the limit address of the currently selected MPU region selected by MPU_RNR[7:2]:(3[1:0]) `FTSSS

Table 3-469. MPU_RLAR_A3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	LIMIT	R/W	Xh	Contains bits [31:5] of the upper inclusive limit of the selected MPU memory region. This value is postfixed with 0x1F to provide the limit address to be checked against
4	RES0	R	0h	Reserved, RES0
3-1	AttrIndx	R/W	0h	Associates a set of attributes in the MPU_MAIR0 and MPU_MAIR1 fields
0	EN	R/W	0h	Region enable

3.9.10.12 MPU_MAIR0 Register (Offset = 30h) [Reset = 00000000h]

MPU_MAIR0 is shown in Table 3-470.

Return to the Summary Table.

Along with MPU_MAIR1, provides the memory attribute encodings corresponding to the AttrIndex values

Table 3-470. MPU_MAIR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Attr3	R/W	0h	Memory attribute encoding for MPU regions with an AttrIndex of 3
23-16	Attr2	R/W	0h	Memory attribute encoding for MPU regions with an AttrIndex of 2
15-8	Attr1	R/W	0h	Memory attribute encoding for MPU regions with an AttrIndex of 1
7-0	Attr0	R/W	0h	Memory attribute encoding for MPU regions with an AttrIndex of 0

3.9.10.13 MPU_MAIR1 Register (Offset = 34h) [Reset = 00000000h]

MPU_MAIR1 is shown in Table 3-471.

Return to the Summary Table.

Along with MPU_MAIR0, provides the memory attribute encodings corresponding to the AttrIndex values

Table 3-471. MPU_MAIR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Attr7	R/W	0h	Memory attribute encoding for MPU regions with an AttrIndex of 7
23-16	Attr6	R/W	0h	Memory attribute encoding for MPU regions with an AttrIndex of 6
15-8	Attr5	R/W	0h	Memory attribute encoding for MPU regions with an AttrIndex of 5
7-0	Attr4	R/W	0h	Memory attribute encoding for MPU regions with an AttrIndex of 4

3.9.11 NVIC Registers

Table 3-472 lists the memory-mapped registers for the NVIC registers. All register offset addresses not listed in Table 3-472 should be considered as reserved locations and the register contents should not be modified.

Table 3-472. NVIC Registers

Offset	Acronym	Register Name	Section
0h	NVIC_ISER0	Enables or reads the enabled state of each group of 32 interrupts	Section 3.9.11.1
4h	NVIC_ISER1	Enables or reads the enabled state of each group of 32 interrupts	Section 3.9.11.2
80h	NVIC_ICER0	Clears or reads the enabled state of each group of 32 interrupts	Section 3.9.11.3
84h	NVIC_ICER1	Clears or reads the enabled state of each group of 32 interrupts	Section 3.9.11.4
100h	NVIC_ISPR0	Enables or reads the pending state of each group of 32 interrupts	Section 3.9.11.5
104h	NVIC_ISPR1	Enables or reads the pending state of each group of 32 interrupts	Section 3.9.11.6
180h	NVIC_ICPR0	Clears or reads the pending state of each group of 32 interrupts	Section 3.9.11.7
184h	NVIC_ICPR1	Clears or reads the pending state of each group of 32 interrupts	Section 3.9.11.8
200h	NVIC_IABR0	For each group of 32 interrupts, shows the active state of each interrupt	Section 3.9.11.9
204h	NVIC_IABR1	For each group of 32 interrupts, shows the active state of each interrupt	Section 3.9.11.10
280h	NVIC_ITNS0	For each group of 32 interrupts, determines whether each interrupt targets Non-secure or Secure state	Section 3.9.11.11
284h	NVIC_ITNS1	For each group of 32 interrupts, determines whether each interrupt targets Non-secure or Secure state	Section 3.9.11.12
300h	NVIC_IPR0	Sets or reads interrupt priorities	Section 3.9.11.13
304h	NVIC_IPR1	Sets or reads interrupt priorities	Section 3.9.11.14
308h	NVIC_IPR2	Sets or reads interrupt priorities	Section 3.9.11.15
30Ch	NVIC_IPR3	Sets or reads interrupt priorities	Section 3.9.11.16
310h	NVIC_IPR4	Sets or reads interrupt priorities	Section 3.9.11.17
314h	NVIC_IPR5	Sets or reads interrupt priorities	Section 3.9.11.18
318h	NVIC_IPR6	Sets or reads interrupt priorities	Section 3.9.11.19
31Ch	NVIC_IPR7	Sets or reads interrupt priorities	Section 3.9.11.20
320h	NVIC_IPR8	Sets or reads interrupt priorities	Section 3.9.11.21

Complex bit access types are encoded to fit into small table cells. Table 3-473 shows the codes that are used for access types in this section.

Table 3-473. NVIC Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

3.9.11.1 NVIC_ISER0 Register (Offset = 0h) [Reset = 00000000h]

NVIC_ISER0 is shown in Table 3-474.

Return to the Summary Table.

Enables or reads the enabled state of each group of 32 interrupts

Table 3-474. NVIC_ISER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SETENA	R	0h	For SETENA[m] in NVIC_ISER*n, indicates whether interrupt 32*n + m is enabled

3.9.11.2 NVIC_ISER1 Register (Offset = 4h) [Reset = 00000000h]

NVIC_ISER1 is shown in Table 3-475.

Return to the Summary Table.

Enables or reads the enabled state of each group of 32 interrupts

Table 3-475. NVIC_ISER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SETENA	R	0h	For SETENA[m] in NVIC_ISER*n, indicates whether interrupt 32*n + m is enabled

3.9.11.3 NVIC_ICER0 Register (Offset = 80h) [Reset = 00000000h]

NVIC_ICER0 is shown in Table 3-476.

Return to the Summary Table.

Clears or reads the enabled state of each group of 32 interrupts

Table 3-476. NVIC_ICER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLRENA	R	0h	For CLRENA[m] in NVIC_ICER*n, indicates whether interrupt 32*n + m is enabled

3.9.11.4 NVIC_ICER1 Register (Offset = 84h) [Reset = 00000000h]

NVIC_ICER1 is shown in Table 3-477.

Return to the Summary Table.

Clears or reads the enabled state of each group of 32 interrupts

Table 3-477. NVIC_ICER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLRENA	R	0h	For CLRENA[m] in NVIC_ICER*n, indicates whether interrupt 32*n + m is enabled

3.9.11.5 NVIC_ISPR0 Register (Offset = 100h) [Reset = 00000000h]

NVIC_ISPR0 is shown in Table 3-478.

Return to the Summary Table.

Enables or reads the pending state of each group of 32 interrupts

Table 3-478. NVIC_ISPR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SETPEND	R	0h	For SETPEND[m] in NVIC_ISPR*n, indicates whether interrupt 32*n + m is pending

3.9.11.6 NVIC_ISPR1 Register (Offset = 104h) [Reset = 00000000h]

NVIC_ISPR1 is shown in Table 3-479.

Return to the Summary Table.

Enables or reads the pending state of each group of 32 interrupts

Table 3-479. NVIC_ISPR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SETPEND	R	0h	For SETPEND[m] in NVIC_ISPR*n, indicates whether interrupt 32*n + m is pending

3.9.11.7 NVIC_ICPR0 Register (Offset = 180h) [Reset = 00000000h]

NVIC_ICPR0 is shown in Table 3-480.

Return to the Summary Table.

Clears or reads the pending state of each group of 32 interrupts

Table 3-480. NVIC_ICPR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLRPEND	R	0h	For CLRPEND[m] in NVIC_ICPR*n, indicates whether interrupt 32*n + m is pending

3.9.11.8 NVIC_ICPR1 Register (Offset = 184h) [Reset = 00000000h]

NVIC_ICPR1 is shown in Table 3-481.

Return to the Summary Table.

Clears or reads the pending state of each group of 32 interrupts

Table 3-481. NVIC_ICPR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLRPEND	R	0h	For CLRPEND[m] in NVIC_ICPR*n, indicates whether interrupt 32*n + m is pending

3.9.11.9 NVIC_IABR0 Register (Offset = 200h) [Reset = 00000000h]

NVIC_IABR0 is shown in Table 3-482.

Return to the Summary Table.

For each group of 32 interrupts, shows the active state of each interrupt

Table 3-482. NVIC_IABR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ACTIVE	R	0h	For ACTIVE[m] in NVIC_IABR*n, indicates the active state for interrupt 32*n+m

3.9.11.10 NVIC_IABR1 Register (Offset = 204h) [Reset = 00000000h]

NVIC_IABR1 is shown in Table 3-483.

Return to the Summary Table.

For each group of 32 interrupts, shows the active state of each interrupt

Table 3-483. NVIC_IABR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ACTIVE	R	0h	For ACTIVE[m] in NVIC_IABR*n, indicates the active state for interrupt 32*n+m

3.9.11.11 NVIC_ITNS0 Register (Offset = 280h) [Reset = 00000000h]

NVIC_ITNS0 is shown in Table 3-484.

Return to the Summary Table.

For each group of 32 interrupts, determines whether each interrupt targets Non-secure or Secure state

Table 3-484. NVIC_ITNS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ITNS	R/W	0h	For ITNS[m] in NVIC_ITNS*n, `IAAMO the target Security state for interrupt 32*n+m

3.9.11.12 NVIC_ITNS1 Register (Offset = 284h) [Reset = 00000000h]

NVIC_ITNS1 is shown in Table 3-485.

Return to the Summary Table.

For each group of 32 interrupts, determines whether each interrupt targets Non-secure or Secure state

Table 3-485. NVIC_ITNS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ITNS	R/W	0h	For ITNS[m] in NVIC_ITNS*n, `IAAMO the target Security state for interrupt 32*n+m

3.9.11.13 NVIC_IPR0 Register (Offset = 300h) [Reset = 00000000h]

NVIC_IPR0 is shown in Table 3-486.

Return to the Summary Table.

Sets or reads interrupt priorities

Table 3-486. NVIC_IPR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-24	PRI_N3	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
23-19	RESERVED	R	0h	Reserved
18-16	PRI_N2	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
15-11	RESERVED	R	0h	Reserved
10-8	PRI_N1	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+1, or is RES0 if the PE does not implement this interrupt
7-3	RESERVED	R	0h	Reserved
2-0	PRI_N0	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+0, or is RES0 if the PE does not implement this interrupt

3.9.11.14 NVIC_IPR1 Register (Offset = 304h) [Reset = 00000000h]

NVIC_IPR1 is shown in Table 3-487.

Return to the Summary Table.

Sets or reads interrupt priorities

Table 3-487. NVIC_IPR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-24	PRI_N3	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
23-19	RESERVED	R	0h	Reserved
18-16	PRI_N2	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
15-11	RESERVED	R	0h	Reserved
10-8	PRI_N1	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+1, or is RES0 if the PE does not implement this interrupt
7-3	RESERVED	R	0h	Reserved
2-0	PRI_N0	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+0, or is RES0 if the PE does not implement this interrupt

3.9.11.15 NVIC_IPR2 Register (Offset = 308h) [Reset = 00000000h]

NVIC_IPR2 is shown in Table 3-488.

Return to the Summary Table.

Sets or reads interrupt priorities

Table 3-488. NVIC_IPR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-24	PRI_N3	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
23-19	RESERVED	R	0h	Reserved
18-16	PRI_N2	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
15-11	RESERVED	R	0h	Reserved
10-8	PRI_N1	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+1, or is RES0 if the PE does not implement this interrupt
7-3	RESERVED	R	0h	Reserved
2-0	PRI_N0	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+0, or is RES0 if the PE does not implement this interrupt

3.9.11.16 NVIC_IPR3 Register (Offset = 30Ch) [Reset = 00000000h]

NVIC_IPR3 is shown in Table 3-489.

Return to the Summary Table.

Sets or reads interrupt priorities

Table 3-489. NVIC_IPR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-24	PRI_N3	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
23-19	RESERVED	R	0h	Reserved
18-16	PRI_N2	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
15-11	RESERVED	R	0h	Reserved
10-8	PRI_N1	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+1, or is RES0 if the PE does not implement this interrupt
7-3	RESERVED	R	0h	Reserved
2-0	PRI_N0	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+0, or is RES0 if the PE does not implement this interrupt

3.9.11.17 NVIC_IPR4 Register (Offset = 310h) [Reset = 00000000h]

NVIC_IPR4 is shown in Table 3-490.

Return to the Summary Table.

Sets or reads interrupt priorities

Table 3-490. NVIC_IPR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-24	PRI_N3	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
23-19	RESERVED	R	0h	Reserved
18-16	PRI_N2	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
15-11	RESERVED	R	0h	Reserved
10-8	PRI_N1	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+1, or is RES0 if the PE does not implement this interrupt
7-3	RESERVED	R	0h	Reserved
2-0	PRI_N0	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+0, or is RES0 if the PE does not implement this interrupt

3.9.11.18 NVIC_IPR5 Register (Offset = 314h) [Reset = 00000000h]

NVIC_IPR5 is shown in Table 3-491.

Return to the Summary Table.

Sets or reads interrupt priorities

Table 3-491. NVIC_IPR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-24	PRI_N3	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
23-19	RESERVED	R	0h	Reserved
18-16	PRI_N2	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
15-11	RESERVED	R	0h	Reserved
10-8	PRI_N1	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+1, or is RES0 if the PE does not implement this interrupt
7-3	RESERVED	R	0h	Reserved
2-0	PRI_N0	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+0, or is RES0 if the PE does not implement this interrupt

3.9.11.19 NVIC_IPR6 Register (Offset = 318h) [Reset = 00000000h]

NVIC_IPR6 is shown in Table 3-492.

Return to the Summary Table.

Sets or reads interrupt priorities

Table 3-492. NVIC_IPR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-24	PRI_N3	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
23-19	RESERVED	R	0h	Reserved
18-16	PRI_N2	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
15-11	RESERVED	R	0h	Reserved
10-8	PRI_N1	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+1, or is RES0 if the PE does not implement this interrupt
7-3	RESERVED	R	0h	Reserved
2-0	PRI_N0	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+0, or is RES0 if the PE does not implement this interrupt

3.9.11.20 NVIC_IPR7 Register (Offset = 31Ch) [Reset = 00000000h]

NVIC_IPR7 is shown in Table 3-493.

Return to the Summary Table.

Sets or reads interrupt priorities

Table 3-493. NVIC_IPR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-24	PRI_N3	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
23-19	RESERVED	R	0h	Reserved
18-16	PRI_N2	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
15-11	RESERVED	R	0h	Reserved
10-8	PRI_N1	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+1, or is RES0 if the PE does not implement this interrupt
7-3	RESERVED	R	0h	Reserved
2-0	PRI_N0	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+0, or is RES0 if the PE does not implement this interrupt

3.9.11.21 NVIC_IPR8 Register (Offset = 320h) [Reset = 00000000h]

NVIC_IPR8 is shown in Table 3-494.

Return to the Summary Table.

Sets or reads interrupt priorities

Table 3-494. NVIC_IPR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18-16	PRI_N2	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
15-11	RESERVED	R	0h	Reserved
10-8	PRI_N1	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+1, or is RES0 if the PE does not implement this interrupt
7-3	RESERVED	R	0h	Reserved
2-0	PRI_N0	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+0, or is RES0 if the PE does not implement this interrupt

3.9.12 SAU Registers

Table 3-495 lists the memory-mapped registers for the SAU registers. All register offset addresses not listed in Table 3-495 should be considered as reserved locations and the register contents should not be modified.

Table 3-495. SAU Registers

Offset	Acronym	Register Name	Section
0h	SAU_CTRL	Allows enabling of the Security Attribution Unit	Section 3.9.12.1
4h	SAU_TYPE	Indicates the number of regions implemented by the Security Attribution Unit	Section 3.9.12.2
8h	SAU_RNR	Selects the region currently accessed by SAU_RBAR and SAU_RLAR	Section 3.9.12.3
Ch	SAU_RBAR	Provides indirect read and write access to the base address of the currently selected SAU region	Section 3.9.12.4
10h	SAU_RLAR	Provides indirect read and write access to the limit address of the currently selected SAU region	Section 3.9.12.5
14h	SFSR	Provides information about any security related faults	Section 3.9.12.6
18h	SFAR	Shows the address of the memory location that caused a Security violation	Section 3.9.12.7

Complex bit access types are encoded to fit into small table cells. Table 3-496 shows the codes that are used for access types in this section.

Table 3-496. SAU Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

3.9.12.1 SAU_CTRL Register (Offset = 0h) [Reset = 00000000h]

SAU_CTRL is shown in Table 3-497.

Return to the Summary Table.

Allows enabling of the Security Attribution Unit

Table 3-497. SAU_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RES0	R	0h	Reserved, RES0
1	ALLNS	R/W	0h	When SAU_CTRL.ENABLE is 0 this bit controls if the memory is marked as Non-secure or Secure
0	ENABLE	R/W	0h	Enables the SAU

3.9.12.2 SAU_TYPE Register (Offset = 4h) [Reset = 00000000h]

SAU_TYPE is shown in Table 3-498.

Return to the Summary Table.

Indicates the number of regions implemented by the Security Attribution Unit

Table 3-498. SAU_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	SREGION	R	4h	The number of implemented SAU regions

3.9.12.3 SAU_RNR Register (Offset = 8h) [Reset = 00000000h]

SAU_RNR is shown in Table 3-499.

Return to the Summary Table.

Selects the region currently accessed by SAU_RBAR and SAU_RLAR

Table 3-499. SAU_RNR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	REGION	R/W	0h	Indicates the SAU region accessed by SAU_RBAR and SAU_RLAR

3.9.12.4 SAU_RBAR Register (Offset = Ch) [Reset = 00000000h]

SAU_RBAR is shown in Table 3-500.

Return to the Summary Table.

Provides indirect read and write access to the base address of the currently selected SAU region

Table 3-500. SAU_RBAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	BADDR	R/W	Xh	Holds bits [31:5] of the base address for the selected SAU region
4-0	RES0	R	0h	Reserved, RES0

3.9.12.5 SAU_RLAR Register (Offset = 10h) [Reset = 00000000h]

SAU_RLAR is shown in Table 3-501.

Return to the Summary Table.

Provides indirect read and write access to the limit address of the currently selected SAU region

Table 3-501. SAU_RLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	LADDR	R/W	Xh	Holds bits [31:5] of the limit address for the selected SAU region
4-2	RES0	R	0h	Reserved, RES0
1	NSC	R/W	0h	Controls whether Non-secure state is permitted to execute an SG instruction from this region
0	ENABLE	R/W	0h	SAU region enable

3.9.12.6 SFSR Register (Offset = 14h) [Reset = 00000000h]

SFSR is shown in Table 3-502.

Return to the Summary Table.

Provides information about any security related faults

Table 3-502. SFSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7	LSERR	R/W	0h	Sticky flag indicating that an error occurred during lazy state activation or deactivation
6	SFARVALID	R/W	0h	This bit is set when the SFAR register contains a valid value. As with similar fields, such as BFSR.BFARVALID and MMFSR.MMARVALID, this bit can be cleared by other exceptions, such as BusFault
5	LSPERR	R/W	0h	Stick flag indicating that an SAU or IDAU violation occurred during the lazy preservation of floating-point state
4	INVTRAN	R/W	0h	Sticky flag indicating that an exception was raised due to a branch that was not flagged as being domain crossing causing a transition from Secure to Non-secure memory
3	AUVIOL	R/W	0h	Sticky flag indicating that an attempt was made to access parts of the address space that are marked as Secure with NS-Req for the transaction set to Non-secure. This bit is not set if the violation occurred during lazy state preservation. See LSPERR
2	INVER	R/W	0h	This can be caused by EXC_RETURN.DCRS being set to 0 when returning from an exception in the Non-secure state, or by EXC_RETURN.ES being set to 1 when returning from an exception in the Non-secure state
1	INVIS	R/W	0h	This bit is set if the integrity signature in an exception stack frame is found to be invalid during the unstacking operation
0	INVEP	R/W	0h	This bit is set if a function call from the Non-secure state or exception targets a non-SG instruction in the Secure state. This bit is also set if the target address is a SG instruction, but there is no matching SAU/IDAU region with the NSC flag set

3.9.12.7 SFAR Register (Offset = 18h) [Reset = 00000000h]

SFAR is shown in Table 3-503.

Return to the Summary Table.

Shows the address of the memory location that caused a Security violation

Table 3-503. SFAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS	R/W	0h	The address of an access that caused a attribution unit violation. This field is only valid when SFSR.SFARVALID is set. This allows the actual flip flops associated with this register to be shared with other fault address registers. If an implementation chooses to share the storage in this way, care must be taken to not leak Secure address information to the Non-secure state. One way of achieving this is to share the SFAR register with the MMFAR_S register, which is not accessible to the Non-secure state

3.9.13 SCB Registers

Table 3-504 lists the memory-mapped registers for the SCB registers. All register offset addresses not listed in Table 3-504 should be considered as reserved locations and the register contents should not be modified.

Table 3-504. SCB Registers

Offset	Acronym	Register Name	Section
0h	REVIDR	Provides implementation-specific minor revision information	Section 3.9.13.1
4h	CPUID	Provides identification information for the PE, including an implementer code for the device and a device ID number	Section 3.9.13.2
8h	ICSR	Controls and provides status information for NMI, PendSV, SysTick and interrupts	Section 3.9.13.3
Ch	VTOR	Indicates the offset of the vector table base address from memory address 0x00000000	Section 3.9.13.4
10h	AIRCR	This register is used to determine data endianness, clear all active state information for debug or to recover from a hard failure, execute a system reset, alter the priority grouping position (binary point).	Section 3.9.13.5
14h	SCR	This register is used for power-management functions, i.e., signaling to the system when the processor can enter a low power state, controlling how the processor enters and exits low power states.	Section 3.9.13.6
18h	CCR	Sets or returns configuration and control data	Section 3.9.13.7
1Ch	SHPR1	Sets or returns priority for system handlers 4 - 7	Section 3.9.13.8
20h	SHPR2	Sets or returns priority for system handlers 8 - 11	Section 3.9.13.9
24h	SHPR3	Sets or returns priority for system handlers 12 - 15	Section 3.9.13.10
28h	SHCSR	Provides access to the active and pending status of system exceptions	Section 3.9.13.11
2Ch	CFSR	Contains the three Configurable Fault Status Registers	Section 3.9.13.12
30h	HFSR	Shows the cause of any HardFaults	Section 3.9.13.13
34h	DFSR	Shows which debug event occurred	Section 3.9.13.14
38h	MMFAR	Shows the address of the memory location that caused an MPU fault	Section 3.9.13.15
3Ch	BFAR	Shows the address associated with a precise data access BusFault	Section 3.9.13.16
40h	AFSR	This register is used to determine additional system fault information to software. Single-cycle high level on an auxiliary faults is latched as one. The bit can only be cleared by writing a one to the corresponding bit. Auxiliary fault inputs to the **CPU** are tied to 0.	Section 3.9.13.17
44h	ID_PFR0	Gives top-level information about the instruction set supported by the PE	Section 3.9.13.18
48h	ID_PFR1	Gives information about the programmers' model and Extensions support	Section 3.9.13.19
4Ch	ID_DFR0	Provides top level information about the debug system	Section 3.9.13.20
50h	ID_AFR0	Provides information about the IMPLEMENTATION DEFINED features of the PE	Section 3.9.13.21
54h	ID_MMFR0	Provides information about the implemented memory model and memory management support	Section 3.9.13.22
58h	ID_MMFR1	Provides information about the implemented memory model and memory management support	Section 3.9.13.23
5Ch	ID_MMFR2	Provides information about the implemented memory model and memory management support	Section 3.9.13.24
60h	ID_MMFR3	Provides information about the implemented memory model and memory management support	Section 3.9.13.25

Table 3-504. SCB Registers (continued)

Offset	Acronym	Register Name	Section
64h	ID_ISAR0	Provides information about the instruction set implemented by the PE	Section 3.9.13.26
68h	ID_ISAR1	Provides information about the instruction set implemented by the PE	Section 3.9.13.27
6Ch	ID_ISAR2	Provides information about the instruction set implemented by the PE	Section 3.9.13.28
70h	ID_ISAR3	Provides information about the instruction set implemented by the PE	Section 3.9.13.29
74h	ID_ISAR4	Provides information about the instruction set implemented by the PE	Section 3.9.13.30
78h	ID_ISAR5	Provides information about the instruction set implemented by the PE	Section 3.9.13.31
7Ch	CLIDR	Identifies the type of caches implemented and the level of coherency and unification	Section 3.9.13.32
80h	CTR	The CTR provides information about the architecture of the currently selected cache	Section 3.9.13.33
84h	CCSIDR	Provides information about the architecture of the caches. CCSIDR is RES0 if CLIDR is zero.	Section 3.9.13.34
88h	CSSELR	Selects the current Cache Size ID Register, CCSIDR, by specifying the required cache level and the cache	Section 3.9.13.35
8Ch	CPACR	Specifies the access privileges for coprocessors and the FP Extension	Section 3.9.13.36
90h	NSACR	Defines the Non-secure access permissions for both the FP Extension and coprocessors CP0 to CP7	Section 3.9.13.37

Complex bit access types are encoded to fit into small table cells. Table 3-505 shows the codes that are used for access types in this section.

Table 3-505. SCB Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

3.9.13.1 REVIDR Register (Offset = 0h) [Reset = 00000000h]

REVIDR is shown in Table 3-506.

Return to the Summary Table.

Provides implementation-specific minor revision information

Table 3-506. REVIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IMPLEMENTAION_DEFINED	R	411FD210h	The contents of this field are IMPLEMENTATION DEFINED

3.9.13.2 CPUID Register (Offset = 4h) [Reset = 00000000h]

CPUID is shown in Table 3-507.

Return to the Summary Table.

Provides identification information for the PE, including an implementer code for the device and a device ID number

Table 3-507. CPUID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Implementer	R	41h	This field must hold an implementer code that has been assigned by ARM
23-20	Variant	R	1h	IMPLEMENTATION DEFINED variant number. Typically, this field is used to distinguish between different product variants, or major revisions of a product
19-16	Architecture	R	Fh	Defines the Architecture implemented by the PE
15-4	PartNo	R	D21h	IMPLEMENTATION DEFINED primary part number for the device
3-0	Revision	R	0h	IMPLEMENTATION DEFINED revision number for the device

3.9.13.3 ICSR Register (Offset = 8h) [Reset = 00000000h]

ICSR is shown in Table 3-508.

Return to the Summary Table.

Controls and provides status information for NMI, PendSV, SysTick and interrupts

Table 3-508. ICSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PENDNMISET	R	0h	Indicates whether the NMI exception is pending
30	PENDNMICLR	W	0h	Allows the NMI exception pend state to be cleared
29	RES0	R	0h	Reserved, RES0
28	PENDSVSET	R	0h	Indicates whether the PendSV `FTSSS exception is pending
27	PENDSVCLR	W	0h	Allows the PendSV exception pend state to be cleared `FTSSS
26	PENDSTSET	R	0h	Indicates whether the SysTick `FTSSS exception is pending
25	PENDSTCLR	W	0h	Allows the SysTick exception pend state to be cleared `FTSSS
24	STTNS	R/W	0h	Controls whether in a single SysTick implementation, the SysTick is Secure or Non-secure
23	ISRPREEMPT	R	0h	Indicates whether a pending exception will be serviced on exit from debug halt state
22	ISRPENDING	R	0h	Indicates whether an external interrupt, generated by the NVIC, is pending
21	RES0_1	R	0h	Reserved, RES0
20-12	VECTPENDING	R	0h	The exception number of the highest priority pending and enabled interrupt
11	RETTOBASE	R	0h	In Handler mode, indicates whether there is more than one active exception
10-9	RES0_2	R	0h	Reserved, RES0
8-0	VECTACTIVE	R	0h	The exception number of the current executing exception

3.9.13.4 VTOR Register (Offset = Ch) [Reset = 00000000h]

VTOR is shown in Table 3-509.

Return to the Summary Table.

Indicates the offset of the vector table base address from memory address 0x00000000

Table 3-509. VTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	TBLOFF	R	00823FA4h	Bits 31 down to 7 of the vector table base offset.
6-0	RES0	R	10h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

3.9.13.5 AIRCR Register (Offset = 10h) [Reset = 00000000h]

AIRCR is shown in Table 3-510.

Return to the Summary Table.

This register is used to determine data endianness, clear all active state information for debug or to recover from a hard failure, execute a system reset, alter the priority grouping position (binary point).

Table 3-510. AIRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VECTKEY	R/W	FA05h	Register key. Writing to this register (AIRCR) requires 0x05FA in VECTKEY. Otherwise the write value is ignored. Read always returns 0xFA05.
15	ENDIANESS	R	0h	Data endianness bit 0 Little-endian. 1 Big-endian.
14	PRIS	R	0h	Prioritize Secure exceptions. The value of this bit defines whether Secure exception priority boosting is enabled.
13	BFHFNMINS	R/W	0h	BusFault, HardFault, and NMI Non-secure enable. The value of this bit defines whether BusFault and NMI exceptions are Non-secure, and whether exceptions target the Non-secure HardFault exception 0x0 BusFault, HardFault, and NMI are Secure. 0x1 BusFault and NMI are Non-secure and exceptions can target Non-secure HardFault.
12-11	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
10-8	PRIGROUP	R/W	0h	Interrupt priority grouping field. This field determines the split of group priority from subpriority
7-4	RES4	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	SYSRESETREQS	R/W	0h	System reset request Secure only. The value of this bit defines whether the SYSRESETREQ bit is functional for Non-secure use
2	SYSRESETREQ	W	0h	System reset request. This bit allows software or a debugger to request a system reset: 0 Do not request a system reset. 1 Request a system reset. This bit is not banked between Security states.
1	VECTCLRACTIVE	W	0h	Reserved for Debug use. This bit reads as 0. When writing to the register you must write 0 to this bit, otherwise behavior is UNPREDICTABLE.
1	RESERVED	R	0h	Reserved
0	RES0	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

3.9.13.6 SCR Register (Offset = 14h) [Reset = 00000000h]

SCR is shown in Table 3-511.

Return to the Summary Table.

This register is used for power-management functions, i.e., signaling to the system when the processor can enter a low power state, controlling how the processor enters and exits low power states.

Table 3-511. SCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4	SEVONPEND	R/W	0h	Send Event on Pending bit: 0 Only enabled interrupts or events can wakeup the processor, disabled interrupts are excluded. 1 Enabled events and all interrupts, including disabled interrupts, can wakeup the processor. When an event or interrupt enters pending state, the event signal wakes up the processor from WFE. If the processor is not waiting for an event, the event is registered and affects the next WFE. The processor also wakes up on execution of an SEV instruction or an external event. This bit is banked between Security states.
3	SLEEPDEEPS	R/W	0h	Controls whether the SLEEPDEEP bit is only accessible from the Secure state: 0 The SLEEPDEEP bit accessible from both Security states. 1 The SLEEPDEEP bit behaves as RAZ/WI when accessed from the Non-secure state. This bit in only accessible from the Secure state, and behaves as RAZ/WI when accessed from the Nonsecure state. This bit is not banked between Security states.
2	SLEEPDEEP	R/W	0h	Controls whether the processor uses sleep or deep sleep as its low power mode. 0 Sleep. 1 Deep sleep. This bit is not banked between Security states.
1	SLEEPONEXIT	R/W	0h	Indicates sleep-on-exit when returning from Handler mode to Thread mode: 0 Do not sleep when returning to Thread mode. 1 Enter sleep, or deep sleep, on return from an ISR. Setting this bit to 1 enables an interrupt driven application to avoid returning to an empty main application. This bit is banked between Security states.
0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

3.9.13.7 CCR Register (Offset = 18h) [Reset = 00000000h]

CCR is shown in Table 3-512.

Return to the Summary Table.

Sets or returns configuration and control data

Table 3-512. CCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RES0	R	0h	Reserved, RES0
18	BP	R	0h	Enables program flow prediction `FTSSS
17	IC	R	0h	This is a global enable bit for instruction caches in the selected Security state
16	DC	R	0h	Enables data caching of all data accesses to Normal memory `FTSSS
15-11	RES0_1	R	0h	Reserved, RES0
10	STKOFHFNMIGN	R/W	0h	Controls the effect of a stack limit violation while executing at a requested priority less than 0
9	RES1	R	1h	Reserved, RES1
8	BFHFNMIGN	R/W	0h	Determines the effect of precise BusFaults on handlers running at a requested priority less than 0
7-5	RES0_2	R	0h	Reserved, RES0
4	DIV_0_TRP	R/W	0h	Controls the generation of a DIVBYZERO UsageFault when attempting to perform integer division by zero
3	UNALIGN_TRP	R/W	0h	Controls the trapping of unaligned word or halfword accesses
2	RES0_3	R	0h	Reserved, RES0
1	USERSETMPEND	R/W	0h	Determines whether unprivileged accesses are permitted to pend interrupts via the STIR
0	RES1_1	R	1h	Reserved, RES1

3.9.13.8 SHPR1 Register (Offset = 1Ch) [Reset = 00000000h]

SHPR1 is shown in Table 3-513.

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Sets or returns priority for system handlers 4 - 7

Table 3-513. SHPR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PRI_7	R/W	0h	Priority of system handler 7, SecureFault
23-16	PRI_6	R/W	0h	Priority of system handler 6, UsageFault
15-8	PRI_5	R/W	0h	Priority of system handler 5, BusFault
7-0	PRI_4	R/W	0h	Priority of system handler 4, MemManage

3.9.13.9 SHPR2 Register (Offset = 20h) [Reset = 00000000h]

SHPR2 is shown in Table 3-514.

Return to the Summary Table.

Sets or returns priority for system handlers 8 - 11

Table 3-514. SHPR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PRI_11	R/W	0h	Priority of system handler 11, SVCall
23-0	RES0	R	Xh	Reserved, RES0

3.9.13.10 SHPR3 Register (Offset = 24h) [Reset = 00000000h]

SHPR3 is shown in Table 3-515.

Return to the Summary Table.

Sets or returns priority for system handlers 12 - 15

Table 3-515. SHPR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PRI_15	R/W	0h	Priority of system handler 15, SysTick
23-16	PRI_14	R/W	0h	Priority of system handler 14, PendSV
15-0	RES0_0	R	0h	Reserved, RES0

3.9.13.11 SHCSR Register (Offset = 28h) [Reset = 00000000h]

SHCSR is shown in Table 3-516.

Return to the Summary Table.

Provides access to the active and pending status of system exceptions

Table 3-516. SHCSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RES0	R	0h	Reserved, RES0
21	HARDFAULTPENDED	R/W	0h	`IAAMO the pending state of the HardFault exception `CTTSSS
20	SECUREFAULTPENDED	R/W	0h	`IAAMO the pending state of the SecureFault exception
19	SECUREFAULTENA	R/W	0h	`DW the SecureFault exception is enabled
18	USGFAULTENA	R/W	0h	`DW the UsageFault exception is enabled `FTSSS
17	BUSFAULTENA	R/W	0h	`DW the BusFault exception is enabled
16	MEMFAULTENA	R/W	0h	`DW the MemManage exception is enabled `FTSSS
15	SVCALLPENDED	R/W	0h	`IAAMO the pending state of the SVCall exception `FTSSS
14	BUSFAULTPENDED	R/W	0h	`IAAMO the pending state of the BusFault exception
13	MEMFAULTPENDED	R/W	0h	`IAAMO the pending state of the MemManage exception `FTSSS
12	USGFAULTPENDED	R/W	0h	The UsageFault exception is banked between Security states, `IAAMO the pending state of the UsageFault exception `FTSSS
11	SYSTICKACT	R/W	0h	`IAAMO the active state of the SysTick exception `FTSSS
10	PENDSVACT	R/W	0h	`IAAMO the active state of the PendSV exception `FTSSS
9	RES0_1	R	0h	Reserved, RES0
8	MONITORACT	R/W	0h	`IAAMO the active state of the DebugMonitor exception
7	SVCALLACT	R/W	0h	`IAAMO the active state of the SVCall exception `FTSSS
6	RES0_2	R	0h	Reserved, RES0
5	NMIACT	R/W	0h	`IAAMO the active state of the NMI exception
4	SECUREFAULTACT	R/W	0h	`IAAMO the active state of the SecureFault exception
3	USGFAULTACT	R/W	0h	`IAAMO the active state of the UsageFault exception `FTSSS
2	HARDFAULTACT	R/W	0h	Indicates and allows limited modification of the active state of the HardFault exception `FTSSS
1	BUSFAULTACT	R/W	0h	`IAAMO the active state of the BusFault exception
0	MEMFAULTACT	R/W	0h	`IAAMO the active state of the MemManage exception `FTSSS

3.9.13.12 CFSR Register (Offset = 2Ch) [Reset = 00000000h]

CFSR is shown in Table 3-517.

Return to the Summary Table.

Contains the three Configurable Fault Status Registers

Table 3-517. CFSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RES0_3	R	0h	Reserved, RES0
25	DIVBYZERO	R/W	0h	Sticky flag indicating whether an integer division by zero error has occurred
24	UNALIGNED	R/W	0h	Sticky flag indicating whether an unaligned access error has occurred
23-21	RES0_1_2	R	0h	Reserved, RES0
20	STKOF	R/W	0h	Sticky flag indicating whether a stack overflow error has occurred
19	NOCP	R/W	0h	Sticky flag indicating whether a coprocessor disabled or not present error has occurred
18	INVPC	R/W	0h	Sticky flag indicating whether an integrity check error has occurred
17	INVSTATE	R/W	0h	Sticky flag indicating whether an EPSR.T or EPSR.IT validity error has occurred
16	UNDEFINSTR	R/W	0h	Sticky flag indicating whether an undefined instruction error has occurred
15	BFARVALID	R/W	0h	Indicates validity of the contents of the BFAR register
14	RES0_2	R	0h	Reserved, RES0
13	LSPERR	R/W	0h	Records whether a BusFault occurred during FP lazy state preservation
12	STKERR	R/W	0h	Records whether a derived BusFault occurred during exception entry stacking
11	UNSTKERR	R/W	0h	Records whether a derived BusFault occurred during exception return unstacking
10	IMPRECISERR	R/W	0h	Records whether an imprecise data access error has occurred
9	PRECISERR	R/W	0h	Records whether a precise data access error has occurred
8	IBUSERR	R/W	0h	Records whether a BusFault on an instruction prefetch has occurred
7	MMARVALID	R/W	0h	Indicates validity of the MMFAR register
6	RES0	R	0h	Reserved, RES0
5	MLSPERR	R/W	0h	Records whether a MemManage fault occurred during FP lazy state preservation
4	MSTKERR	R/W	0h	Records whether a derived MemManage fault occurred during exception entry stacking
3	MUNSTKERR	R/W	0h	Records whether a derived MemManage fault occurred during exception return unstacking
2	RES0_1	R	0h	Reserved, RES0
1	DACCVIOL	R/W	0h	Records whether a data access violation has occurred
0	IACCVIOL	R/W	0h	Records whether an instruction related memory access violation has occurred

3.9.13.13 HFSR Register (Offset = 30h) [Reset = 00000000h]

HFSR is shown in Table 3-518.

Return to the Summary Table.

Shows the cause of any HardFaults

Table 3-518. HFSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DEBUGEVT	R/W	0h	Indicates when a Debug event has occurred
30	FORCED	R/W	0h	Indicates that a fault with configurable priority has been escalated to a HardFault exception, because it could not be made active, because of priority, or because it was disabled
29-2	RES0	R	Xh	Reserved, RES0
1	VECTTBL	R/W	0h	Indicates when a fault has occurred because of a vector table read error on exception processing
0	RES0_1	R	0h	Reserved, RES0

3.9.13.14 DFSR Register (Offset = 34h) [Reset = 00000000h]

DFSR is shown in Table 3-519.

Return to the Summary Table.

Shows which debug event occurred

Table 3-519. DFSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RES0	R	Xh	Reserved, RES0
4	EXTERNAL	R/W	0h	Sticky flag indicating whether an External debug request debug event has occurred
3	VCATCH	R/W	0h	Sticky flag indicating whether a Vector catch debug event has occurred
2	DWTTRAP	R/W	0h	Sticky flag indicating whether a Watchpoint debug event has occurred
1	BKPT	R/W	0h	Sticky flag indicating whether a Breakpoint debug event has occurred
0	HALTED	R/W	0h	Sticky flag indicating that a Halt request debug event or Step debug event has occurred

3.9.13.15 MMFAR Register (Offset = 38h) [Reset = 00000000h]

MMFAR is shown in Table 3-520.

Return to the Summary Table.

Shows the address of the memory location that caused an MPU fault

Table 3-520. MMFAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS	R/W	0h	This register is updated with the address of a location that produced a MemManage fault. The MMFSR shows the cause of the fault, and whether this field is valid. This field is valid only when MMFSR.MMARVALID is set, otherwise it is UNKNOWN

3.9.13.16 BFAR Register (Offset = 3Ch) [Reset = 00000000h]

BFAR is shown in Table 3-521.

Return to the Summary Table.

Shows the address associated with a precise data access BusFault

Table 3-521. BFAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS	R/W	0h	This register is updated with the address of a location that produced a BusFault. The BFSR shows the reason for the fault. This field is valid only when BFSR.BFARVALID is set, otherwise it is UNKNOWN

3.9.13.17 AFSR Register (Offset = 40h) [Reset = 00000000h]

AFSR is shown in Table 3-522.

Return to the Summary Table.

This register is used to determine additional system fault information to software. Single-cycle high level on an auxiliary faults is latched as one. The bit can only be cleared by writing a one to the corresponding bit. Auxiliary fault inputs to the CPU are tied to 0.

Table 3-522. AFSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	IMPDEF	R/W	0h	Implementation defined. The bits map directly onto the signal assignment to the auxiliary fault inputs. Tied to 0

3.9.13.18 ID_PFR0 Register (Offset = 44h) [Reset = 00000000h]

ID_PFR0 is shown in Table 3-523.

Return to the Summary Table.

Gives top-level information about the instruction set supported by the PE

Table 3-523. ID_PFR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	State1	R	3h	T32 instruction set support
3-0	State0	R	0h	A32 instruction set support

3.9.13.19 ID_PFR1 Register (Offset = 48h) [Reset = 00000000h]

ID_PFR1 is shown in Table 3-524.

Return to the Summary Table.

Gives information about the programmers' model and Extensions support

Table 3-524. ID_PFR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RES0	R	Xh	Reserved, RES0
11-8	MProgMod	R	2h	Identifies support for the M-Profile programmers' model support
7-4	Security	R	1h	Identifies whether the Security Extension is implemented
3-0	RES0_1	R	0h	Reserved, RES0

3.9.13.20 ID_DFR0 Register (Offset = 4Ch) [Reset = 00000000h]

ID_DFR0 is shown in Table 3-525.

Return to the Summary Table.

Provides top level information about the debug system

Table 3-525. ID_DFR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RES0	R	0h	Reserved, RES0
23-20	MProfDbg	R	2h	Indicates the supported M-profile debug architecture
19-0	RES0_1	R	Xh	Reserved, RES0

3.9.13.21 ID_AFR0 Register (Offset = 50h) [Reset = 00000000h]

ID_AFR0 is shown in Table 3-526.

Return to the Summary Table.

Provides information about the IMPLEMENTATION DEFINED features of the PE

Table 3-526. ID_AFR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RES0	R	0h	Reserved, RES0
15-12	IMPDEF3	R	0h	IMPLEMENTATION DEFINED meaning
11-8	IMPDEF2	R	0h	IMPLEMENTATION DEFINED meaning
7-4	IMPDEF1	R	0h	IMPLEMENTATION DEFINED meaning
3-0	IMPDEF0	R	0h	IMPLEMENTATION DEFINED meaning

3.9.13.22 ID_MMFR0 Register (Offset = 54h) [Reset = 00000000h]

ID_MMFR0 is shown in Table 3-527.

Return to the Summary Table.

Provides information about the implemented memory model and memory management support

Table 3-527. ID_MMFR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RES0	R	0h	Reserved, RES0
23-20	AuxReg	R	1h	Indicates support for Auxiliary Control Registers
19-16	TCM	R	0h	Indicates support for tightly coupled memories (TCMs)
15-12	ShareLvl	R	1h	Indicates the number of shareability levels implemented
11-8	OuterShr	R	Fh	Indicates the outermost shareability domain implemented
7-4	PMSA	R	4h	Indicates support for the protected memory system architecture (PMSA)
3-0	RES0_1	R	0h	Reserved, RES0

3.9.13.23 ID_MMFR1 Register (Offset = 58h) [Reset = 00000000h]

ID_MMFR1 is shown in Table 3-528.

Return to the Summary Table.

Provides information about the implemented memory model and memory management support

Table 3-528. ID_MMFR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

3.9.13.24 ID_MMFR2 Register (Offset = 5Ch) [Reset = 00000000h]

ID_MMFR2 is shown in Table 3-529.

Return to the Summary Table.

Provides information about the implemented memory model and memory management support

Table 3-529. ID_MMFR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RES0	R	0h	Reserved, RES0
27-24	WFIStall	R	1h	Indicates the support for Wait For Interrupt (WFI) stalling
23-0	RES0_1	R	Xh	Reserved, RES0

3.9.13.25 ID_MMFR3 Register (Offset = 60h) [Reset = 00000000h]

ID_MMFR3 is shown in Table 3-530.

Return to the Summary Table.

Provides information about the implemented memory model and memory management support

Table 3-530. ID_MMFR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RES0	R	Xh	Reserved, RES0
11-8	BPMaint	R	0h	Indicates the supported branch predictor maintenance
7-4	CMaintSW	R	0h	Indicates the supported cache maintenance operations by set/way
3-0	CMaintVA	R	0h	Indicates the supported cache maintenance operations by address

3.9.13.26 ID_ISAR0 Register (Offset = 64h) [Reset = 00000000h]

ID_ISAR0 is shown in Table 3-531.

Return to the Summary Table.

Provides information about the instruction set implemented by the PE

Table 3-531. ID_ISAR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RES0	R	0h	Reserved, RES0
27-24	Divide	R	1h	Indicates the supported Divide instructions
23-20	Debug	R	1h	Indicates the implemented Debug instructions
19-16	Coproc	R	4h	Indicates the supported Coprocessor instructions
15-12	CmpBranch	R	1h	Indicates the supported combined Compare and Branch instructions
11-8	BitField	R	1h	Indicates the supported bit field instructions
7-4	BitCount	R	1h	Indicates the supported bit count instructions
3-0	RES0_1	R	0h	Reserved, RES0

3.9.13.27 ID_ISAR1 Register (Offset = 68h) [Reset = 00000000h]

ID_ISAR1 is shown in Table 3-532.

Return to the Summary Table.

Provides information about the instruction set implemented by the PE

Table 3-532. ID_ISAR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RES0	R	0h	Reserved, RES0
27-24	Interwork	R	2h	Indicates the implemented Interworking instructions
23-20	Immediate	R	2h	Indicates the implemented for data-processing instructions with long immediates
19-16	IfThen	R	1h	Indicates the implemented If-Then instructions
15-12	Extend	R	2h	Indicates the implemented Extend instructions
11-0	RES0_1	R	0h	Reserved, RES0

3.9.13.28 ID_ISAR2 Register (Offset = 6Ch) [Reset = 00000000h]

ID_ISAR2 is shown in Table 3-533.

Return to the Summary Table.

Provides information about the instruction set implemented by the PE

Table 3-533. ID_ISAR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	Reversal	R	2h	Indicates the implemented Reversal instructions
27-24	RES0	R	0h	Reserved, RES0
23-20	MultU	R	2h	Indicates the implemented advanced unsigned Multiply instructions
19-16	MultS	R	3h	Indicates the implemented advanced signed Multiply instructions
15-12	Mult	R	2h	Indicates the implemented additional Multiply instructions
11-8	MultiAccessInt	R	2h	Indicates the support for interruptible multi-access instructions
7-4	MemHint	R	3h	Indicates the implemented Memory Hint instructions
3-0	LoadStore	R	2h	Indicates the implemented additional load/store instructions

3.9.13.29 ID_ISAR3 Register (Offset = 70h) [Reset = 00000000h]

ID_ISAR3 is shown in Table 3-534.

Return to the Summary Table.

Provides information about the instruction set implemented by the PE

Table 3-534. ID_ISAR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RES0	R	0h	Reserved, RES0
27-24	TrueNOP	R	1h	Indicates the implemented true NOP instructions
23-20	T32Copy	R	1h	Indicates the support for T32 non flag-setting MOV instructions
19-16	TabBranch	R	1h	Indicates the implemented Table Branch instructions
15-12	SynchPrim	R	1h	Used in conjunction with ID_ISAR4.SynchPrim_frac to indicate the implemented Synchronization Primitive instructions
11-8	SVC	R	1h	Indicates the implemented SVC instructions
7-4	SIMD	R	3h	Indicates the implemented SIMD instructions
3-0	Saturate	R	1h	Indicates the implemented saturating instructions

3.9.13.30 ID_ISAR4 Register (Offset = 74h) [Reset = 00000000h]

ID_ISAR4 is shown in Table 3-535.

Return to the Summary Table.

Provides information about the instruction set implemented by the PE

Table 3-535. ID_ISAR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RES0	R	0h	Reserved, RES0
27-24	PSR_M	R	1h	Indicates the implemented M profile instructions to modify the PSRs
23-20	SyncPrim_frac	R	3h	Used in conjunction with ID_ISAR3.SynchPrim to indicate the implemented Synchronization Primitive instructions
19-16	Barrier	R	1h	Indicates the implemented Barrier instructions
15-12	RES0_1	R	0h	Reserved, RES0
11-8	Writeback	R	1h	Indicates the support for writeback addressing modes
7-4	WithShifts	R	3h	Indicates the support for writeback addressing modes
3-0	Unpriv	R	2h	Indicates the implemented unprivileged instructions

3.9.13.31 ID_ISAR5 Register (Offset = 78h) [Reset = 00000000h]

ID_ISAR5 is shown in Table 3-536.

Return to the Summary Table.

Provides information about the instruction set implemented by the PE

Table 3-536. ID_ISAR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

3.9.13.32 CLIDR Register (Offset = 7Ch) [Reset = 00000000h]

CLIDR is shown in Table 3-537.

Return to the Summary Table.

Identifies the type of caches implemented and the level of coherency and unification

Table 3-537. CLIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	ICB	R	0h	This field indicates the boundary between inner and outer domain 0h = Not disclosed in this mechanism 1h = L1 cache is the highest inner level 2h = L2 cache is the highest inner level 3h = L3 cache is the highest inner level
29-27	LoUU	R	0h	This field indicates the Level of Unification Uniprocessor for the cache hierarchy
26-24	LoC	R	0h	This field indicates the Level of Coherence for the cache hierarchy
23-21	LoUIS	R	0h	Enables Non-secure access to coprocessor CP0
20-18	Ctype7	R	0h	Cache type field 7. Indicates the type of cache implemented at level 7. 0h = No cache 1h = Instruction cache only 2h = Data cache only 3h = Separate instruction and data caches 4h = Unified cache
17-15	Ctype6	R	0h	Cache type field 6. Indicates the type of cache implemented at level 6. 0h = No cache 1h = Instruction cache only 2h = Data cache only 3h = Separate instruction and data caches 4h = Unified cache
14-12	Ctype5	R	0h	Cache type field 5. Indicates the type of cache implemented at level 5. 0h = No cache 1h = Instruction cache only 2h = Data cache only 3h = Separate instruction and data caches 4h = Unified cache
11-9	Ctype4	R	0h	Cache type field 4. Indicates the type of cache implemented at level 4. 0h = No cache 1h = Instruction cache only 2h = Data cache only 3h = Separate instruction and data caches 4h = Unified cache
8-6	Ctype3	R	0h	Cache type field 3. Indicates the type of cache implemented at level 3. 0h = No cache 1h = Instruction cache only 2h = Data cache only 3h = Separate instruction and data caches 4h = Unified cache
5-3	Ctype2	R	0h	Cache type field 2. Indicates the type of cache implemented at level 2. 0h = No cache 1h = Instruction cache only 2h = Data cache only 3h = Separate instruction and data caches 4h = Unified cache

Table 3-537. CLIDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	Ctype1	R	0h	Cache type field 1. Indicates the type of cache implemented at level 1. 0h = No cache 1h = Instruction cache only 2h = Data cache only 3h = Separate instruction and data caches 4h = Unified cache

3.9.13.33 CTR Register (Offset = 80h) [Reset = 00000000h]

CTR is shown in Table 3-538.

Return to the Summary Table.

The CTR provides information about the architecture of the currently selected cache

Table 3-538. CTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES1	R	1h	Reserved, RES1
30-28	RES0	R	0h	Reserved, RES0
27-24	CWG	R	0h	Log2 of the number of words of the maximum size of memory that can be overwritten as a result of the eviction of a cache entry that has had a memory location in it modified
23-20	ERG	R	0h	Log2 of the number of words of the maximum size of the reservation granule that has been implemented for the Load-Exclusive and Store-Exclusive instructions
19-16	DminLine	R	0h	Log2 of the number of words in the smallest cache line of all the data caches and unified caches that are controlled by the PE
15-14	RES1_1	R	3h	Reserved, RES1
13-4	RES0_1	R	0h	Reserved, RES0
3-0	IminLine	R	0h	Log2 of the number of words in the smallest cache line of all the instruction caches that are controlled by the PE

3.9.13.34 CCSIDR Register (Offset = 84h) [Reset = 00000000h]

CCSIDR is shown in Table 3-539.

Return to the Summary Table.

Provides information about the architecture of the caches. CCSIDR is RES0 if CLIDR is zero.

Table 3-539. CCSIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WT	R	1h	Indicates whether the currently selected cache level supports Write-Through 0h = Not supported 1h = Supported
30	WB	R	0h	Indicates whether the currently selected cache level supports Write-Back 0h = Not supported 1h = Supported
29	RA	R	0h	Indicates whether the currently selected cache level supports read-allocation 0h = Not supported 1h = Supported
28	WA	R	0h	Indicates whether the currently selected cache level supports write-allocation 0h = Not supported 1h = Supported
27-13	NumSets	R	6h	Indicates (Number of sets in the currently selected cache) - 1. Therefore, a value of 0 indicates that 1 is set in the cache. The number of sets does not have to be a power of 2
12-3	Associativity	R	0h	Indicates (Associativity of cache) - 1. A value of 0 indicates an associativity of 1. The associativity does not have to be a power of 2
2-0	LineSize	R	0h	Indicates (Log2(Number of words per line in the currently selected cache)) - 2.

3.9.13.35 CSSELR Register (Offset = 88h) [Reset = 00000000h]

CSSELR is shown in Table 3-540.

Return to the Summary Table.

Selects the current Cache Size ID Register, CCSIDR, by specifying the required cache level and the cache type (either instruction or data cache)

Table 3-540. CSSELR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	Res0	R	08000C00h	Reserved,Res0
3-1	Level	R	0h	Selects which cache level is to be identified. Permitted values are from 0b000, indicating Level 1 cache, to 0b110 indicating Level 7 cache 0h = Level 1 cache 1h = Level 2 cache 2h = Level 3 cache 3h = Level 4 cache 4h = Level 5 cache 5h = Level 6 cache 6h = Level 7 cache
0	InD	R	0h	Selects whether the instruction or the data cache is to be identified 0h = Data or unified cache 1h = Instruction cache

3.9.13.36 CPACR Register (Offset = 8Ch) [Reset = 00000000h]

CPACR is shown in Table 3-541.

Return to the Summary Table.

Specifies the access privileges for coprocessors and the FP Extension

Table 3-541. CPACR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RES0	R	0h	Reserved, RES0
23-22	CP11	R/W	0h	The value in this field is ignored. If the implementation does not include the FP Extension, this field is RAZ/WI. If the value of this bit is not programmed to the same value as the CP10 field, then the value is UNKNOWN
21-20	CP10	R/W	0h	Defines the access rights for the floating-point functionality
19-16	RES0_1	R	0h	Reserved, RES0
15-14	CP7	R/W	0h	Controls access privileges for coprocessor 7
13-12	CP6	R/W	0h	Controls access privileges for coprocessor 6
11-10	CP5	R/W	0h	Controls access privileges for coprocessor 5
9-8	CP4	R/W	0h	Controls access privileges for coprocessor 4
7-6	CP3	R/W	0h	Controls access privileges for coprocessor 3
5-4	CP2	R/W	0h	Controls access privileges for coprocessor 2
3-2	CP1	R/W	0h	Controls access privileges for coprocessor 1
1-0	CP0	R/W	0h	Controls access privileges for coprocessor 0

3.9.13.37 NSACR Register (Offset = 90h) [Reset = 00000000h]

NSACR is shown in Table 3-542.

Return to the Summary Table.

Defines the Non-secure access permissions for both the FP Extension and coprocessors CP0 to CP7

Table 3-542. NSACR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RES0	R	Xh	Reserved, RES0
11	CP11	R/W	0h	Enables Non-secure access to the Floating-point Extension
10	CP10	R/W	0h	Enables Non-secure access to the Floating-point Extension
9-8	RES0_1	R	0h	Reserved, RES0
7	CP7	R/W	0h	Enables Non-secure access to coprocessor CP7
6	CP6	R/W	0h	Enables Non-secure access to coprocessor CP6
5	CP5	R/W	0h	Enables Non-secure access to coprocessor CP5
4	CP4	R/W	0h	Enables Non-secure access to coprocessor CP4
3	CP3	R/W	0h	Enables Non-secure access to coprocessor CP3
2	CP2	R/W	0h	Enables Non-secure access to coprocessor CP2
1	CP1	R/W	0h	Enables Non-secure access to coprocessor CP1
0	CP0	R/W	0h	Enables Non-secure access to coprocessor CP0

3.9.14 SYSTIMER Registers

Table 3-543 lists the memory-mapped registers for the SYSTIMER registers. All register offset addresses not listed in Table 3-543 should be considered as reserved locations and the register contents should not be modified.

Table 3-543. SYSTIMER Registers

Offset	Acronym	Register Name	Section
0h	SysTick Control and Status Register	Controls and provides status date for the SysTick timer	Section 3.9.14.1
4h	SysTick Reload Value Register	Specifies the SysTick timer counter reload value	Section 3.9.14.2
8h	SysTick Current Value Register	Contains the current value of the SysTick counter	Section 3.9.14.3
Ch	SysTick Calibration Value Register	Indicates the SysTick calibration value and parameters for the selected security state	Section 3.9.14.4

Complex bit access types are encoded to fit into small table cells. Table 3-544 shows the codes that are used for access types in this section.

Table 3-544. SYSTIMER Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

3.9.14.1 SysTick Control and Status Register (Offset = 0h) [Reset = 00000000h]

SysTick Control and Status Register is shown in Table 3-545.

Return to the Summary Table.

Controls and provides status date for the SysTick timer

Table 3-545. SysTick Control and Status Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RES17	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
16	COUNTFLAG	R/W	0h	Indicates whether the counter has counted to zero since the last read of this register
15-3	RES3	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
2	CLKSOURCE	R/W	0h	Indicates the SysTick clock source
1	TICKINT	R/W	0h	Indicates whether counting to 0 causes the status of the SysTick exception to change to pending
0	ENABLE	R/W	0h	Indicates the enabled status of the SysTick counter

3.9.14.2 SysTick Reload Value Register (Offset = 4h) [Reset = 00000000h]

SysTick Reload Value Register is shown in Table 3-546.

Return to the Summary Table.

Specifies the SysTick timer counter reload value

Table 3-546. SysTick Reload Value Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RES24	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
23-0	RELOAD	R/W	0h	Value to load into the SYST_CVR when the counter is enabled and when it reaches 0

3.9.14.3 SysTick Current Value Register (Offset = 8h) [Reset = 00000000h]

SysTick Current Value Register is shown in Table 3-547.

Return to the Summary Table.

Contains the current value of the SysTick counter

Table 3-547. SysTick Current Value Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RES24	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
23-0	CURRENT	W	0h	Reads the current value of the SysTick counter. A write of any value clears the field to 0, and also clears the SYST_CSR.COUNTFLAG bit to 0.

3.9.14.4 SysTick Calibration Value Register (Offset = Ch) [Reset = 00000000h]

SysTick Calibration Value Register is shown in Table 3-548.

Return to the Summary Table.

Indicates the SysTick calibration value and parameters for the selected security state

Table 3-548. SysTick Calibration Value Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES24_2	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
30	SKEW	R	0h	Indicates whether the TENMS value is exact
29-24	RES24	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
23-0	TENMS	R	0h	Reload value for 10ms (100Hz) timing, subject to system clock skew errors. If the value reads as zero, the calibration value is not known.

3.9.15 SYSTICK Registers

Table 3-549 lists the memory-mapped registers for the SYSTICK registers. All register offset addresses not listed in Table 3-549 should be considered as reserved locations and the register contents should not be modified.

Table 3-549. SYSTICK Registers

Offset	Acronym	Register Name	Section
0h	SYST_CSR	Controls and provides status date for the SysTick timer	Section 3.9.15.1
4h	SYST_RVR	Specifies the SysTick timer counter reload value	Section 3.9.15.2
8h	SYST_CVR	Contains the current value of the SysTick counter	Section 3.9.15.3
Ch	SYST_CALIB	Indicates the SysTick calibration value and parameters for the selected security state	Section 3.9.15.4

Complex bit access types are encoded to fit into small table cells. Table 3-550 shows the codes that are used for access types in this section.

Table 3-550. SYSTICK Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

3.9.15.1 SYST_CSR Register (Offset = 0h) [Reset = 00000000h]

SYST_CSR is shown in Table 3-551.

Return to the Summary Table.

Controls and provides status date for the SysTick timer

Table 3-551. SYST_CSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RES17	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
16	COUNTFLAG	R/W	0h	Indicates whether the counter has counted to zero since the last read of this register
15-3	RES3	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
2	CLKSOURCE	R/W	0h	Indicates the SysTick clock source
1	TICKINT	R/W	0h	Indicates whether counting to 0 causes the status of the SysTick exception to change to pending
0	ENABLE	R/W	0h	Indicates the enabled status of the SysTick counter

3.9.15.2 SYST_RVR Register (Offset = 4h) [Reset = 00000000h]

SYST_RVR is shown in Table 3-552.

Return to the Summary Table.

Specifies the SysTick timer counter reload value

Table 3-552. SYST_RVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RES24	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
23-0	RELOAD	R/W	Xh	Value to load into the SYST_CVR when the counter is enabled and when it reaches 0

3.9.15.3 SYST_CVR Register (Offset = 8h) [Reset = 00000000h]

SYST_CVR is shown in Table 3-553.

Return to the Summary Table.

Contains the current value of the SysTick counter

Table 3-553. SYST_CVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RES24	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
23-0	CURRENT	W	Xh	Reads the current value of the SysTick counter. A write of any value clears the field to 0, and also clears the SYST_CSR.COUNTFLAG bit to 0.

3.9.15.4 SYST_CALIB Register (Offset = Ch) [Reset = 00000000h]

SYST_CALIB is shown in Table 3-554.

Return to the Summary Table.

Indicates the SysTick calibration value and parameters for the selected security state

Table 3-554. SYST_CALIB Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES24_2	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
30	SKEW	R	0h	Indicates whether the TENMS value is exact
29-24	RES24	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
23-0	TENMS	R	Xh	Reload value for 10ms (100Hz) timing, subject to system clock skew errors. If the value reads as zero, the calibration value is not known.

4.1 Memory Map

All CC35xx devices share a common platform memory map. Peripherals are assigned a fixed address space and have the same address space on all devices within the family. The memory map is compliant with the standard Arm Cortex-M memory regions.

This table presents a summary of the hardware interface for the CC35xx. Each module instance within the design is shown below, together with the module register map and bit definitions for each bitfield.

For more information on the internal structure of the CC35xx and connections between the modules, please see Section 2.3.

Table 4-1. Memory Map

Module [1]	Module Name	Base Address
ITCM_NS (TCM_CRAM)	Instruction Tightly Coupled Memory, Non-Secured	0x00000000
ITCM_S (TCM_CRAM_SEC)	Instruction Tightly Coupled Memory, Secured	0x04000000
EXTERNAL_CODE_FLASH_NS (EXT_FLASH)	External Code Flash, Non-Secured	0x10000000
EXTERNAL_CODE_FLASH_S (EXT_FLASH_SEC)	External Code Flash, Secured	0x14000000
DTCM_NS (TCM_DRAM)	Data Tightly Coupled Memory, Non-Secured	0x20000000
DTCM_S (TCM_DRAM_SEC)	Data Tightly Coupled Memory, Secured	0x24000000
DMEM_NS (DRAM)	Data Memory, Non-Secured	0x28000000
DMEM_S (DRAM_SEC)	Data Memory, Secured	0x2C000000
HIF	Wireless Subsystem Host Interface	0x408A0000
PRCM_AON	Power, Reset, Clock Managment	0x41090000
PRCM_SCRATCHPAD		0x41098000
SOC_DEBUGSS	DEBUGSS	0x410D0000
SOC_IC	SOC Interconnect	0x410F0000
SOC_AON	SOC Always On	0x41100000
SOC_AAON	SOC Almost Always On	0x41104000
RTC	Real Time Clock	0x41108000
IOMUX	IOMUX	0x41140000
HOSTMCU_AON	Host MCU Always On	0x411D0000
SYSRESOURCES	System Timer	0x411E0000
SYSTIM	System Timer	0x411E2000
I2C0	I2C Peripheral 0	0x41200000
I2C1	I2C Peripheral 1	0x41210000
SPI0	SPI Peripheral 0	0x41220000
SPI1	SPI Peripheral 1	0x41230000
UARTLIN0	UART Peripheral 0	0x41240000
UARTLIN1	UART Peripheral 1	0x41250000

Table 4-1. Memory Map (continued)

Module [1]	Module Name	Base Address
GPTIMER0	General Purpose Timer 0	0x41260000
GPTIMER1	General Purpose Timer 1	0x41268000
I2S	I2S Peripheral	0x41270000
PDM	PDM Peripheral	0x41280000
DCAN	DCAN Peripheral	0x412A0000
ADC	Analog to Digital Converter Peripheral	0x412B0000
SDMMC	SDMMC Peripheral	0x412C0000
SDIO_CARD_FN1	SDIO Card Peripheral	0x412D0000
SDIO_CORE		0x412E0000
UARTLIN2	UART Peripheral 2	0x41300000
HOST MCU	HOST MCU	0x41900000
ICACHE	Instruction Cache Memory	0x41902000
DCACHE	Data Cache Memory	0x41902400
HOST_MCU_SEC	HOST MCU, Secured	0x41903000
OSPI	Octal xSPI Interface	0x41910000
HOST_XIP	Quad xSPI Interface	0x41912000
HOST_DMA	Host DMA Interface	0x41A00000
HSM	Hardware Security Module	0x41B00000
HSM_NON_SEC		0x41B04000
HSM_SEC		0x41B05000
EXTERNAL_PSRAM_NS (EXT_PSRAM)	External PSRAM, Non-Secured	0x60000000
EXTERNAL_PSRAM_S (EXT_PSRAM_SEC)	External PSRAM, Secured	0x64000000
EXTERNAL_NVS_FLASH_NS	Non-Nolatile Storage External Flash, Non-Secured	0xA0000000
EXTERNAL_NVS_FLASH_S	Non-Nolatile Storage External Flash, Secured	0xA4000000

(1) The module names in parentheses are the names for these modules in the software header files - these names are interchangeable.

Chapter 5

Interrupts and Events

This chapter describes interrupts and events for the CC35xx device platform and the different Arm® documentation listed in Chapter 3 are used as reference.

5.1 Exception Model

The Arm® Cortex®-M33 processor and the nested vectored interrupt controller (NVIC) prioritize and handle all exceptions in handler mode. The state of the processor is automatically stored to the stack on an exception and automatically restored from the stack at the end of the interrupt service routine (ISR). The vector is fetched in parallel to state saving, thus enabling efficient interrupt entry. The processor supports tail-chaining, which enables performance of back-to-back interrupts without the overhead of state saving and restoration.

Section 5.1.2 lists all exception types. Software can set eight priority levels on all the exceptions except reset and hard fault.

Internally, the highest user-programmable priority (0) is treated as third priority, after a reset, and a hard fault, in that order.

Note

The default priority is 0 for all the programmable priorities.

CAUTION

After a write to clear an interrupt source, it can take several processor cycles for the NVIC to detect the interrupt source de-assertion due to the write buffer. Thus, if the interrupt clear is done as the last action in an interrupt handler, it is possible for the interrupt handler to complete while the NVIC detects the interrupt as still asserted, causing the interrupt handler to be re-entered errantly. This situation can be avoided by either clearing the interrupt source at the beginning of the interrupt handler or by performing a read from the same address after the write to clear the interrupt source (and flush the write buffer).

5.1.1 Exception States

Each exception is in one of the following states:

- **Inactive:** The exception is not active and not pending.
- **Pending:** The exception is waiting to be serviced by the processor. An interrupt request from a peripheral or from software can change the state of the corresponding interrupt to pending.
- **Active:** An exception is being serviced by the processor but has not completed. An exception handler can interrupt the execution of another exception handler. In this case, both exceptions are in the active state.
- **Active and Pending:** The exception is being serviced by the processor, and there is a pending exception from the same source

5.1.2 Exception Types

The exception types are:

- **Reset:** The exception model treats reset as a special form of exception. When reset is asserted, the operation of the processor stops, potentially at any point in an instruction. When either power-on or warm reset is de-asserted, execution restarts from the address provided by the reset entry in the ROM vector table. Execution restarts as privileged execution in Secure state in Thread mode. This exception is not banked between security states.
- **NMI:** A Non-Maskable Interrupt (NMI) can be signaled by a peripheral or triggered by software. It is permanently enabled and has a fixed priority of -2. NMI can only be preempted by reset and, when it is Non-secure, by a Secure HardFault. If SCB.AIRCR[13] BFHFNMINS = 0, then the NMI is Secure. If SCB.AIRCR[13] BFHFNMINS = 1, then NMI is Non-secure.
- **HardFault:** A HardFault is an exception that occurs because of an error during normal or exception processing. HardFaults have a fixed priority of at least -1, meaning they have higher priority than any exception with configurable priority. This exception is not banked between security states

If SCB.AIRCR[13] BFHFNMINS = 0, HardFault handles all faults that are unable to preempt the current execution. The HardFault handler is always Secure.

If SCB.AIRCR[13] BFHFNMINS = 1, HardFault handles faults that target Non-secure state that are unable to preempt the current execution.

HardFaults that specifically target the Secure state when SCB.AIRCR[13] BFHFNMINS is set to 1 have a priority of -3 to ensure they can preempt any execution. A Secure HardFault at priority -3 is only enabled when SCB.AIRCR[13] BFHFNMINS is set to 1. Secure HardFault handles Secure faults that are unable to preempt current execution.

- **MemManage:** A MemManage fault is an exception that occurs because of a memory protection violation, compared to the MPU or the fixed memory protection constraints, for both instruction and data memory transactions. This fault is always used to abort instruction accesses to Execute Never (XN) memory regions. This exception is banked between security states.
- **BusFault:** A BusFault is an exception that occurs because of a memory-related violation for an instruction or data memory transaction. This might be from an error that is detected on a bus in the memory system. This exception is not banked between security states.

  If SCB.AIRCR[13] BFHFNMINS = 0, BusFaults target the Secure state.

  If SCB.AIRCR[13] BFHFNMINS = 1, BusFaults target the Non-secure state.

- **UsageFault:** A UsageFault is an exception that occurs because of a fault related to instruction execution.

  This includes:

  – An undefined instruction
  – An illegal unaligned access
  – Invalid state on instruction execution
  – An error on exception return The following can cause a usage fault:
  – An unaligned address on word and halfword memory access
  – Division by zero

  This exception is banked between security states.

- **SecureFault:** This exception is triggered by the various security checks that are performed. It is triggered, for example, when jumping from Non-secure code to an address in Secure code that is not marked as a valid entry point. Most systems choose to treat a Secure fault as a terminal condition that either halts or restarts the system. Any other handling of the SecureFault must be checked carefully to make sure that it does not inadvertently introduce a security vulnerability. SecureFaults always target the Secure state.
- **SVCall:** A Supervisor Call (SVC) is an exception that is triggered by the SVC instruction. In an OS environment, applications can use SVC instructions to access OS kernel functions and device drivers. This exception is banked between security states.
- **DebugMonitor:** A DebugMonitor exception. If halting debug is disabled and the debug monitor is enabled, a debug event causes a debug monitor exception when the group priority of the debug monitor exception is greater than the current execution priority.
- **PendSV:** PendSV is an asynchronous request for system-level service. In an OS environment, use PendSV for context switching when no other exception is active. This exception is banked between Security states.
- **SysTick:** A SysTick exception is an exception the system timer generates when it reaches zero. Software can also generate a SysTick exception. In an OS environment, the processor can use this exception as a system tick. This exception is banked between Security states.
- **Interrupt (IRQ):** An interrupt, or IRQ, is an exception signaled by a peripheral, or generated by a software request. All interrupts are asynchronous to instruction execution. In the system, peripherals use interrupts to communicate with the processor. This exception is not banked between security states. Secure code can assign each interrupt to Secure or Non-secure state. By default, all interrupts are assigned to Secure state.

For an asynchronous exception, other than reset, the processor can execute extra instructions between the moment the exception is triggered and the moment the processor enters the exception handler. Privileged

software can disable the exceptions that have configurable priority, as shown in the table above. An exception that targets Secure state cannot be disabled by Non-secure code.

Table 5-1. Exception Types

Exception Number	IRQ Number	Exception Type	Priority	Vector Address	Activation
1	-	Reset	-4, the highest	0x00000004	Asynchronous
2	-14	NMI	-2	0x00000008	Asynchronous
3	-13	Secure HardFault when SCB:AIRCR.BFHFNMINS is 1	-3	0x0000000C	Synchronous
		Secure HardFault when SCB:AIRCR.BFHFNMINS is 0	-1		
		HardFault	-1		
4	-12	MemManage	Configurable	0x00000010	Synchronous
5	-11	BusFault	Configurable	0x00000014	Synchronous
6	-10	UsageFault	Configurable	0x00000018	Synchronous
7	-9	SecureFault	Configurable	0x0000001C	Synchronous
8-10	-	Reserved	-	-	-
11	-5	SVCall	Configurable	0x0000002C	Synchronous
12	-4	DebugMonitor	Configurable	0x00000030	Synchronous
13	-	Reserved	-	-	-
14	-2	PendSV	Configurable	0x00000038	Asynchronous
15	-1	SysTick	Configurable	0x0000003C	Asynchronous
16 and above	0 and above	Interrupt (IRQ)	Configurable	0x00000040 and above (increasing in steps of 4)	Asynchronous

Note

To simplify the software layer, the CMSIS only uses IRQ numbers. It uses negative values for exceptions other than interrupts. The IPSR returns the Exception number.

5.1.3 Exception Handlers

The exception handlers are the following:

- **Interrupt Service Routine (ISRs):** Interrupts IRQ0-IRQ46 are the exceptions that are handled by ISRs. Each interrupt is configured by Secure software in Secure or Non-secure state, using NVIC.NVIC_ITNS0 and NVIC.NVIC_ITNS1.
- **Fault Handler:** The fault handler handles the following exceptions:
  - HardFault
  - MemManage
  - BusFault
  - UsageFault
  - SecureFault

  There can be separate MemManage and UsageFault handlers in Secure and Non-secure state. The SCB.AIRCR[13] BFHFNMINS bit controls the target state for HardFault and BusFault. SecureFault always targets Secure state.
- **System Handlers:** The system handlers handle the following system exceptions:
  - NMI

- PendSV
- SVCall
- SysTick

Most system handlers can be banked with separate handlers between Secure and Non-secure state. The SCB.AIRCR[13] BFHFNMINS bit controls the target state for NMI.

5.1.4 Vector Table

The Vector Table Offset Register (SCB.VTOR) in the System Control Block (SCB) determines the starting address of the vector table. The VTOR is banked so there is a VTOR_S and a VTOR_NS. The initial values of VTOR_Sand VTOR_NS are 0. The vector table used depends on the target state of the exception. For exceptions targeting the Secure state, VTOR_S is used. For exceptions targeting the Non-secure state, VTOR_NS is used.

Table 5-2 shows the order of the exception vectors in the Secure and Non-secure vector tables. The leastsignificant bit of each vector is 1, indicating that the exception handler is written in Thumb® code.

Table 5-2. Vector Table With Security Extension

Exception Number	IRQ Number	Secure Vector	Non-secure Vector	Offset
68	52	IRQ52		
.		.	.	.
.		.	.	.
.		.	.	.
18	2	IRQ2	IRQ2	0x48
17	1	IRQ1	IRQ1	0x44
16	0	IRQ0	IRQ0	0x40
15	-1	SysTick_S	SysTick_NS	0x3C
14	-2	PendSV_S	PendSV_NS	0x38
13		Reserved	Reserved	0x30
12	-3	DebugMonitor	DebugMonitor	
11	-5	SVCall_S	SVCall_NS	0x2C
10		Reserved	Reserved	
9				
8				
7	-9	SecureFault	Reserved	0x1C
6	-11	UsageFault_S	UsageFault_NS	0x18
5	-12	BusFault_S	BusFault_NS	0x14
4	-13	MemManage_S	MemManage_NS	0x10
3	-13	HardFault_S	HardFault_NS	0x0C
2	-14	NMI_S	NMI_NS	0x08
1		Reset	Reset	0x04
		Initial SP Value	Initial SP Value	0x00

Because reset always targets Secure state, the Non-secure reset and Non-secure initial SP value are ignored by the hardware.

5.1.5 Exception Priorities

All exceptions have an assigned priority that is used to control both pre-emption and prioritization between pending exceptions. A lower priority value indicates a higher priority. You can configure priorities for all exceptions except Reset, HardFault, and NMI.

If software does not configure any priorities, then all exceptions with a configurable priority have a priority of 0.

Note

Configurable priorities are in the range 0-255. The Reset, HardFault, and NMI exceptions, with fixed negative priority values always have higher priority than any other exception.

For configurable priority exceptions, the target Security state also affects the programmed priority. Depending on the value of SCB.AIRCR[14] PRIS, the priority can be extended.

Table 5-3, the values in columns 2 and 3 must match, and increase from zero in increments of 32. The values in column 4 start from 128 and increase in increments of 16.

Table 5-3. Extended Priority

Priority Value [7:5]	Secure Priority	Non-secure priority when SCB.AIRCR[14] PRIS = 0	Non-secure priority when SCB.AIRCR[14] PRIS = 1
0	0	0	128
1	32	32	144
2	64	64	160
3	96	96	176
4	128	128	192
5	160	160	208
6	192	192	224
7	224	224	240

Assigning a higher priority value to IRQ[0] and a lower priority value to IRQ[1] means that IRQ[1] has higher priority than IRQ[0]. If both IRQ[1] and IRQ[0] are asserted, IRQ[1] is processed before IRQ[0].

If multiple pending exceptions have the same priority, the pending exception with the lowest exception number takes precedence. For example, if both IRQ[0] and IRQ[1] are pending and have the same priority, then IRQ[0] is processed before IRQ[1].

When the processor is executing an exception handler, the exception handler is preempted if a higher priority exception occurs. If an exception occurs with the same priority as the exception being handled, the handler is not preempted, irrespective of the exception number. However, the status of the new interrupt changes to pending.

5.1.6 Interrupt Priority Grouping

The NVIC supports software assigned priority levels. A priority level from 0 to 8 can be assign to an interrupt by writing to the most significant bits of the PRI_N field in the NVIC.NVIC_IPRn register corresponding to the interrupt, see Section 3.9.11.

Only the group priority determines pre-emption of interrupt exceptions. When the processor is executing an interrupt exception handler, another interrupt with the same group priority as the interrupt being handled does not pre-empt the handler.

If multiple pending interrupts have the same group priority, the subpriority field determines the order in which the interrupts are processed. If multiple pending interrupts have the same group priority and subpriority, the interrupt with the lowest IRQ number is processed first.

If a pending Secure exception and a pending Non-secure exception both have the same group priority field value, the same subpriority field value, and the same exception number, the Secure exception takes precedence.

5.1.7 Exception Entry and Return

Descriptions of exception handling use the following terms.

- **Preemption:** An exception can preempt the current execution if its priority is higher than the current execution priority. When one exception preempts another, the exceptions are called nested exceptions.
- **Return:** This occurs when the exception handler is completed. The processor pops the stack and restores the processor state to the state it had before the interrupt occurred.
- **Tail-Chaining:** This mechanism speeds up exception servicing. On completion of an exception handler or during the return operation, if there is a pending exception that meets the requirements for exception entry, then the stack pop is skipped and control transfers directly to the new exception handler.
- **Late Arriving Interrupts:** This mechanism speeds up preemption. If a higher priority exception occurs during state saving for a previous exception, the processor switches to handle the higher priority exception and initiates the vector fetch for that exception. State saving may be affected by the late arrival depending on the stacking requirements of the original exception and the late-arriving exception. On return from the exception handler of the late-arriving exception, the normal tail-chaining rules apply.

5.1.7.1 Exception Entry

Exception entry occurs when there is a pending exception with sufficient priority and either the processor is in Thread mode, or the new exception is of higher priority than the exception being handled, in which case the new exception preempts the original exception.

When one exception preempts another, the exceptions are nested.

Sufficient priority means that the exception has higher priority than any limits set by the mask registers. An exception with lower priority than this is pending but is not handled by the processor.

When the processor takes an exception, unless the exception is a tail-chained or a late-arriving exception, the processor pushes information onto the current stack. This operation is referred to as stacking and the structure of the data stacked is referred as the stack frame.

The Cortex-M33 processor can automatically stack the architected floating-point state on exception entry.

5.1.7.2 Exception Return

Exception return occurs when the processor is in Handler mode and execution of one of the following instructions attempts to set the PC to an EXC_RETURN value:

- A POP or LDM instruction that loads the PC
- An LDR instruction that loads the PC
- A BX instruction using any register

The processor saves an EXC_RETURN value to the LR on exception entry. The exception mechanism relies on this value to detect when the processor has completed an exception handler. When the processor loads a value matching this pattern to the PC it detects that the operation is not a normal branch operation and, instead, that the exception is complete. As a result, it starts the exception return sequence. Bits[6:0] of the EXC_RETURN value indicate the required return stack, processor mode, Security state, and stack frame as shown in Table 5-4.

Table 5-4. Exception Return Behavior

Bits	Name	Description
[31:24]	PREFIX	Indicates that this is an EXC_RETURN value. This field reads as 0b11111111
[23:7]	-	Reserved, RES1

Table 5-4. Exception Return Behavior (continued)

Bits	Name	Description
[6]	S	Indicates whether registers have been pushed to a Secure or Non-secure stack. 0: Non-secure stack used 1: Secure stack used.
[5]	DCRS	Indicates whether the default stacking rules apply, or whether the called registers are already on the stack. 0: Stacking of the called saved registers is skipped 1: Default rules for stacking the called registers are followed
[4]	FType	In a PE with the Main and Floating-point Extensions: 0: The PE allocated space on the stack for FP context 1: The PE did not allocate space on the stack for FP context. In a PE without the Floating-point Extension, this bit is Reserved, RES1
[3]	Mode	Indicates the mode that was stacked from. 0: Handler mode 1: Thread mode
[2]	SPSEL	Indicates which stack contains the exception stack frame. 0: Main stack pointer 1: Process stack pointer
[1]	-	Reserved, RES0
[0]	ES	Indicates the Security state the exception was taken to. 0: Non-secure 1: Secure

5.2 Fault Handling

Faults can occur on instruction fetches, instruction execution, and data accesses. When a fault occurs, information about the cause of the fault is recorded in various registers, according to the type of fault. Faults are a subset of the exceptions.

Faults are generated by:

- A bus error on:
  - An instruction fetches or vector table load
  - A data access
- An internally-detected error such as an undefined instruction
- Attempting to execute an instruction from a memory region marked as Execute Never (XN)
- A privilege violation or an attempt to access an unmanaged region causing an MPU fault
- A security violation

5.2.1 Fault Types

Table 5-5 shows the types of fault, the handler used for the fault, the corresponding fault status register, and the register bit that indicates that the fault has occurred.

Table 5-5. Fault Types

Fault	Handler	Bit Name	Fault Status Register
Bus error on a vector read	HardFault	VECTTBL	HardFault Status Register (HFSR)
Fault escalated to a hard fault		FORCED	

Table 5-5. Fault Types (continued)

Fault	Handler	Bit Name	Fault Status Register
MPU or default memory map mismatch:	MemManage	-	MemManage Fault Status Register (MMFSR)
On instruction access		IACCVIOL	
On data access		DACCVIOL	
During exception stacking		MSTKERR	
During exception unstacking		MUNSKERR	
During lazy floating-point state preservation		MLSPERR	
Bus error:	BusFault	-	-
During exception stacking		STKERR	BusFault Status Register (BFSR)
During exception unstacking		UNSTKERR	
During instruction prefetch		IBUSERR	
During lazy floating-point state preservation		LSPERR	
Precise data bus error		PRECISERR	
Imprecise data bus error		IMPRECISERR	
Attempt to access a coprocessor	UsageFault	NOCP	UsageFault Status Register (UFSR)
Undefined instruction		UNDEFINSTR	
Attempt to enter an invalid instruction set state		INVSTATE	
Invalid EXC_RETURN value		INVPC	
Illegal unaligned load or store		UNALIGNED	
Stack overflow flag		STKOF	
Divide By 0		DIVBYZERO	
Lazy state error flag	SecureFault	LSERR	SecureFault Status Register (SFSR)
Lazy state preservation error flag		LSPERR	
Invalid transition flag		INVTRAN	
Attribution unit violation flag		AUVIOL	
Invalid exception return flag		INVER	
Invalid integrity signature flag		INVIS	
Invalid integrity signature flag		INVEP	

5.2.2 Fault Escalation to HardFault

All fault exceptions other than HardFault have configurable exception priority. Software can disable execution of the handlers for these faults.

Usually, the exception priority, together with the values of the exception mask registers, determines whether the processor enters the fault handler, and whether a fault handler can preempt another fault handler.

In some situations, a fault with configurable priority is treated as a HardFault. This is called priority escalation, and the fault is described as escalated to HardFault. Escalation to HardFault occurs when:

- A fault handler causes the same kind of fault as the one it is servicing. This escalation to HardFault occurs because a fault handler cannot preempt itself; it must have the same priority as the current execution priority level.

- A fault handler causes a fault with the same or lower priority as the fault it is servicing. This is because the handler for the new fault cannot preempt the currently executing fault handler.
- An exception handler causes a fault for which the priority is the same as or lower than the currently executing exception.
- A fault occurs and the handler for that fault is not enabled. If a BusFault occurs during a stack push when entering a BusFault handler, the BusFault does not escalate to a HardFault. This means that if a corrupted stack causes a fault, the fault handler executes even though the stack push for the handler failed. The fault handler operates but the stack contents are corrupted.

If a BusFault occurs during a stack push when entering a BusFault handler, the BusFault does not escalate to a HardFault. This means that if a corrupted stack causes a fault, the fault handler executes even though the stack push for the handler failed. The fault handler operates but the stack contents are corrupted.

BusFaults and fixed priority exceptions can be designated as Secure or Non-secure under the control of SCB.AIRCR[13] BFHFNMINS. When SCB.AIRCR[13] BFHFMNINS is set to:

- 0: BusFaults and fixed priority exceptions are designated as Secure. The exceptions retain the prioritization of HardFault at -1 and NMI at -2.
- 1: BusFaults and fixed priority exceptions are designated as Non-secure. In this case, Secure HardFault is introduced at priority -3 to ensure that faults that target Secure state are recognized.

The Non-secure state cannot inhibit BusFaults and fixed priority exceptions which target Secure state. Therefore when faults and fixed priority exceptions are Secure, Non-secure FAULTMASK (FAULTMASK_NS) only inhibits programmable priority exceptions, making it equivalent to Non-secure PRIMASK (PRIMASK_NS).

Non-secure programmable priority exceptions are mapped to the regular priority range 0-255, if SCB.AIRCR[14] PRIS is clear. Non-secure programmable priority exceptions are mapped to the bottom half the regular priority range, 128-255, if AIRCR.PRIS is set to 1. Therefore, the FAULTMASK_NS sets the execution priority to 0x0 or 0x80, according to AIRCR.PRIS, to mask the Non-secure programmable priority exception only.

When BusFaults and fixed priority exceptions are Secure, FAULTMASK_S sets execution priority to -1 to inhibit everything up to and including HardFault.

When BusFaults and fixed priority exceptions are designated as Non-secure, FAULTMASK_NS boosts priority to -1 to inhibit everything up to Non-secure HardFault at priority -1, while FAULTMASK_S boosts priority to -3 to inhibit all faults and fixed priority exceptions including the Secure HardFault at priority -3.

Note

Only Reset can preempt the fixed priority Secure HardFault when SCB.AIRCR[13] BFHFNMINS is set to 1. A Secure HardFault when SCB.AIRCR[13] BFHFNMINS is set to 1 can preempt any exception other than Reset.

A Secure HardFault when SCB.AIRCR[13] BFHFNMINS is set to 0 can preempt any exception other than Reset, NMI, or another HardFault.

5.2.3 Fault Status Registers and Fault Address Registers

The fault status registers indicate the cause of a fault. For BusFaults, MemManage faults, and SecureFaults, the fault address register indicates the address that is accessed by the operation that caused the fault.

The processor has two physical fault address registers. One shared between the MMFAR_S (SCB.MMFAR), SAU.SFAR, and SCB.BFAR (only if SCB.AIRCR[13] BFHFNMINS is set to 0), and the other shared between the MMFAR_NS (SCB.MMFAR) and SCB.BFAR (only if SCB.AIRCR[13] BFHFNMINS is set to 1). These are targeted by Secure and Non-secure faults respectively.

For each physical fault address register, it is only possible to report the address of one fault at a time.

Each fault address register is updated when one of the *FARVALID bits is set for their respective faults in the associated *FSR register. BFARVALID is located in SCB.CFSR and SFARVALID is located in SAU.SFSR. Any

fault that targets a fault address register with one of its *FARVALID bits already set does not update the fault address. The *FARVALID bits must be cleared before another fault address can be reported.

5.2.4 Lockup

The processor enters a lockup state if a fault occurs when it cannot be serviced or escalated. When the processor is in lockup state, it does not execute any instructions.

The processor remains in lockup state until either:

- It is reset
- Preemption by a higher priority exception occurs
- It is halted by a debugger

Note

5.3 Security State Switches

Table 5-6 presents the possible security transitions, the instructions that can cause them, and any faults that may be generated.

Table 5-6. Security State Transitions

Current Security State	Security Attribute of the Branch Target Address	Security State Change
Secure	Non-secure	Change to Non-secure state if the branch was a BXNS or BLXNS instruction with the LSB of the target address set to 0. Otherwise, a SecureFault is generated.
Non-secure	Secure and Non-secure callable	Change to Secure state if the branch target address contains an SG instruction. If the target address does not contain an SG a SecureFault is generated.
Non-secure	Secure and not Non-secure callable	A SecureFault is generated.

Secure software can call a Non-secure function using the BLXNS instruction. When this happens, the LR is set to a special value called FNC_RETURN, and the return address and XPSR is saved onto the Secure stack. Return from Non-secure state to Secure state is triggered when one of the following instructions attempts to set the PC to an FNC_RETURN value:

- A POP or LDM instruction that loads the PC
- An LDR instruction that loads the PC
- A BX instruction using any register

When a return from Non-secure state to Secure state occurs the processor restores the program counter and XPSR from the Secure stack.

Any scenario not listed in the table triggers a SecureFault. For example:

- Sequential instructions that cross security attributes from Secure to Non-secure.
  - A 32-bit instruction fetch that crosses regions with different security attributes.

5.4 Event Manager

5.4.1 Introduction

The event manager is a combinational router between event publishers and event subscribers. The event publishers are routed to a central event manager IP where a subscriber can select the appropriate events.

The publisher signals can be driven from the peripherals, GPIOs, and different system resources. The subscribers are the Host MCU nVIC, Host MCU AON (ELP), and peripherals.

The publisher signals can be driven directly to the subscribers (direct events) or concentrated into a single common event to the subscriber (concentrated events). In addtion, the publisher signals can be driven as trigger events into the peripherals (HW events).

Direct events are connected directly from the publisher to the subscriber with no configurations in the event manager.

Concentrated events are several events concentrated together into a single event. Each of the individual events can be masked and have status read separately.

Hardware (HW) events are driven to the event manager via hardware, and a single event can be selected for each peripheral.

Figure 5-1 shows a simple illustration of the event manager concept

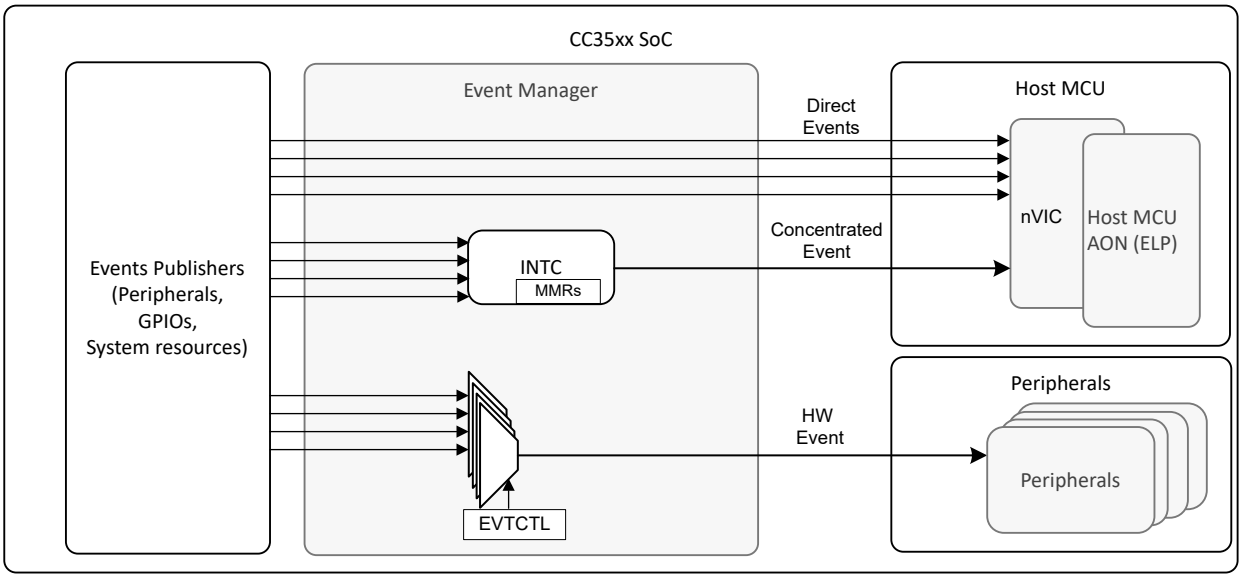

Figure 5-1. Event Manager Concept

The event manager is divided into AON and AAON power domains blocks. The AON registers are in the SOC AON aperture and the AAON registers are in the SOC AAON aperture. All event manager registers are in the AON domain except for DMA concentrator registers.

The SOC AON register values are kept when the device enters low power mode unlike the the SOC AAON registers which are reset.

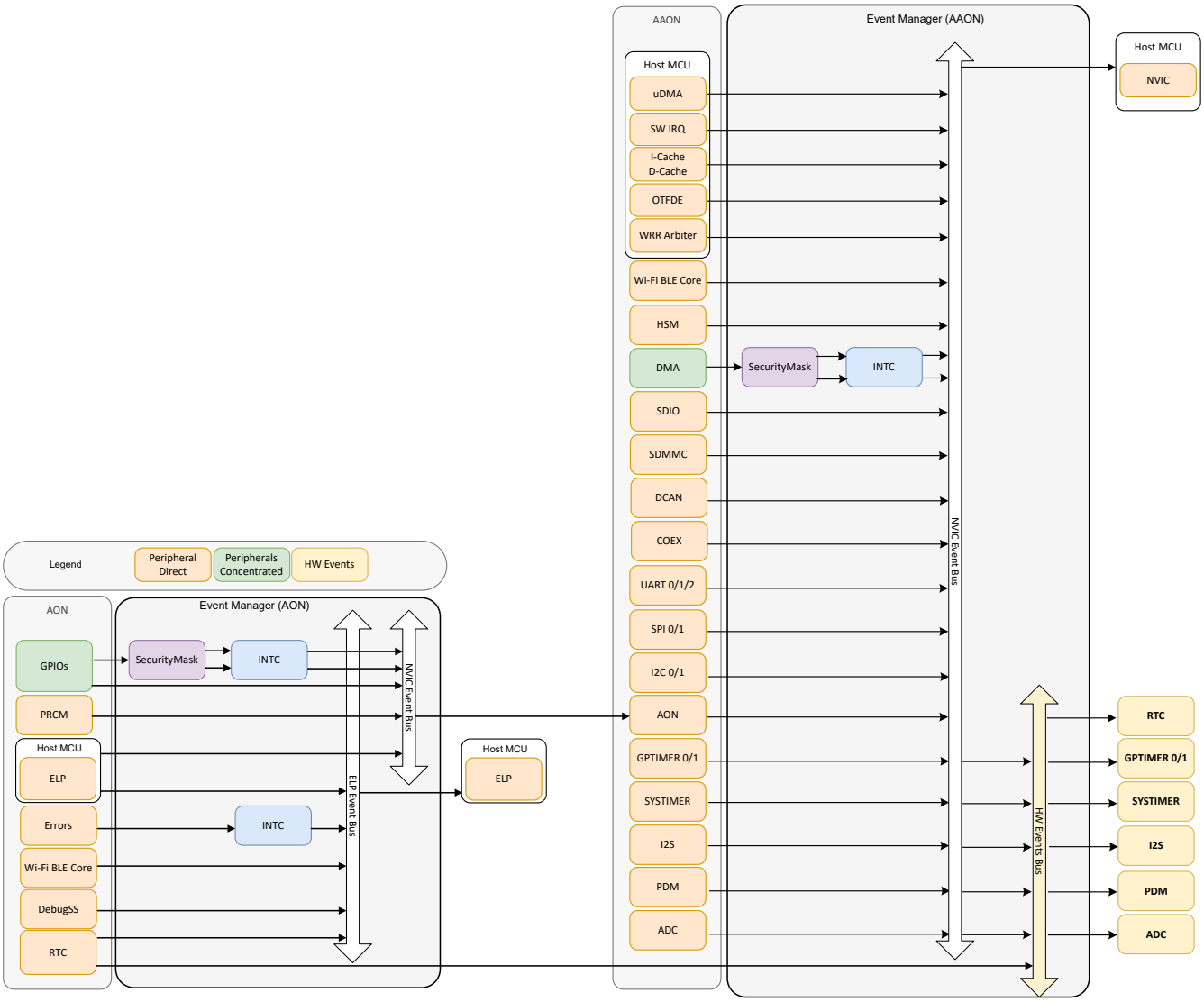

Figure 5-2. Event Manager Overview

Note

DMA and GPIOs are concentrated events and they generate secure and non-secure events.

5.4.2 Interrupts List

Table 5-7 lists the input events for the Event Manager.

Table 5-7. Interrupts List

IRQ Index	Name	Event Type	Power Domain	Subscribers
0	UART0_IRQ	Direct	AAON	NVIC
1	UART1_IRQ	Direct	AAON	NVIC
2	I2C0_IRQ	Direct	AAON	NVIC
3	I2C1_IRQ	Direct	AAON	NVIC
4	SPI0_IRQ	Direct	AAON	NVIC
5	SPI1_IRQ	Direct	AAON	NVIC
6	GPTIMER0_IRQ	Direct	AAON	HW, NVIC
7	GPTIMER1_IRQ	Direct	AAON	HW, NVIC

Table 5-7. Interrupts List (continued)

IRQ Index	Name	Event Type	Power Domain	Subscribers
8	UART2_IRQ	Direct	AAON	NVIC
9	I2S_IRQ	Direct	AAON	HW, NVIC
10	PDM_IRQ	Direct	AAON	HW, NVIC
11	DCAN_IRQ0	Direct	AAON	NVIC
12	DCAN_IRQ1	Direct	AAON	NVIC
13	SDMMC_IRQ0	Direct	AAON	NVIC
14	SDIO CARD_IRQ	Direct	AAON	NVIC
15	ADC_IRQ	Direct	AAON	HW, NVIC
16	GPIO Non Secured IRQ	Concentrated (1)	AON	NVIC
17	GPIO Secured IRQ	Concentrated (1)	AON	NVIC
18	HSM_Secured_IRQ	Direct	AAON	NVIC
19	HSM_0_IRQ	Direct	AAON	NVIC
20	HSM_1_IRQ	Direct	AAON	NVIC
21	SYS_TIMER_IRQ	Direct	AAON	HW, NVIC
22	SYS_TIMER_Heartbeat	Direct	AAON	HW, NVIC
23	SYS_TIMER_CH0_Event	Direct	AAON	HW, NVIC
24	SYS_TIMER_CH1_Event	Direct	AAON	HW, NVIC
25	Host DMA_NonSecured_IRQ	Concentrated (1)	AAON	NVIC
26	Host DMA_Secured_IRQ	Concentrated (1)	AAON	NVIC
27	Reserved	Reserved		
28	Reserved	Reserved		
29	I-Cache_IRQ	Direct	AAON	NVIC
30	xSPI_IRQ	Direct	AAON	NVIC
31	OTFDE_IRQ	Direct	AAON	NVIC
32	WRR Arbiter_IRQ	Direct	AAON	NVIC
33	uDMA_Secured_IRQ	Direct	AAON	NVIC
34	uDMA_NonSecured_IRQ	Direct	AAON	NVIC
35	SW_IRQ0	Direct	AAON	NVIC
36	SW_IRQ1	Direct	AAON	NVIC
37	SW_IRQ2	Direct	AAON	NVIC
38	SW_IRQ3	Direct	AAON	NVIC
39	SW_IRQ4	Direct	AAON	NVIC
40	SW_IRQ5	Direct	AAON	NVIC
41	SW_IRQ6	Direct	AAON	NVIC
42	SW_IRQ7	Direct	AAON	NVIC
43	Reserved	Reserved		
45	HIF_IRQ	Direct	AAON	NVIC
46	HOST ELP IRQ	Direct	AON	NVIC
47	Host WLAN IRQ	Direct	AAON	ELP, NVIC
48	Host BLE IRQ	Direct	AON	ELP, NVIC
49	RTC_IRQ	Direct	AON	HW, NVIC
50	DEBUG_HOST_PWR_UP_REQ	Direct	AON	ELP
51	DEBUG_HOST_FORCEACTIVE	Direct	AON	ELP

Table 5-7. Interrupts List (continued)

IRQ Index	Name	Event Type	Power Domain	Subscribers
52	SoC Errors IRQ	Direct	AON	ELP

(1) All concentrated events are configured in registers SOC_AON aperture, except for DMA events which are configured by registers in SOC_AAON aperture.

5.4.3 Wakeup Sources

The ELP subscriber has programmable events in AON event manager, which are ORed together to form a single wake-up event to PRCM configurable via the HOSTMCU_AON.CFGWICSNS register. This wake-up event is used to trigger the wakeup of the MCU power domain from Sleep mode. Any of the events listed in the HOSTMCU_AON.CFGWICSNS can be chosen as input by selecting the appropriate event publisher or publishers. By default, this register is set to 0, meaning that no publishers are selected to drive the wake-up event towards PRCM.

5.4.4 Shared Peripherals MUX Selector

The ADC, I2S, and PDM peripherals can be configured as subscribers for HW events from the Event Manager. These subscribers are different peripherals that must be configured differently according to the purpose of those specific peripherals.

HW events input to these peripherals can be configured in the SOC_AON.SPEVTCTL register.

5.4.4.1 ADC HW Event Selector Mux

The table below shows the possible HW events input to the ADC. This should be configured in the SOC_AON.SPEVTCTL[5:0] ADC field.

Table 5-8. ADC HW Event Selector Table

Select Config	Event Name
0	0 (Logic Low)
1	1 (Logic High)
2	GPTIMER0_ADC_Trigger
3	GPTIMER0_DMA_Trigger
4	GPTIMER1_ADC_Trigger
5	GPTIMER1_DMA_Trigger
6	GPIO0_IRQ
7	GPIO1_IRQ
8	GPIO2_IRQ
9	GPIO3_IRQ
10	GPIO4_IRQ
11	GPIO5_IRQ
12	GPIO6_IRQ
13	Reserved
14	Reserved
15	Reserved
16	GPIO10_IRQ
17	GPIO11_IRQ
18	GPIO12_IRQ
19	GPIO13_IRQ
20	GPIO14_IRQ
21	GPIO15_IRQ
22	GPIO16_IRQ
23	GPIO17_IRQ

Table 5-8. ADC HW Event Selector Table (continued)

Select Config	Event Name
24	GPIO18_IRQ
25	GPIO19_IRQ
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved
32	GPIO26_IRQ
33	GPIO27_IRQ
34	GPIO28_IRQ
35	GPIO29_IRQ
36	GPIO30_IRQ
37	GPIO31_IRQ
38	GPIO32_IRQ
39	GPIO33_IRQ
40	GPIO34_IRQ
41	GPIO35_IRQ
42	GPIO36_IRQ
43	GPIO37_IRQ
44	Reserved
45	Reserved
46	Reserved
47	Reserved
48	Reserved
49	Reserved
50	Reserved
51	SYS_TIMER_IRQ
52	SYS_TIMER_Heartbeat
53	SYS_TIMER_CH0_EVENT
54	SYS_TIMER_CH1_EVENT
55	SYS_TIMER_LFTICK_IRQ
56	Reserved
57	Reserved
58	RTC_IRQ
else	0

5.4.4.2 I2S HW Event Selector Mux

The table below shows the possible HW events input to the I2S. This should be configured in the SOC_AON.SPEVTCTL[14:8] I2S field.

Table 5-9. I2S HW Event Selector Table

Select Config	Event Name
0	0 (Logic Low)
1	1 (Logic High)
2	GPTIMER0_DMA_Trigger

Table 5-9. I2S HW Event Selector Table (continued)

Select Config	Event Name
3	GPTIMER0_EVENT0
4	GPTIMER0_EVENT1
5	GPTIMER0_EVENT2
6	GPTIMER0_EVENT3
7	GPTIMER1_DMA_Trigger
8	GPTIMER1_EVENT0
9	GPTIMER1_EVENT1
10	GPTIMER1_EVENT2
11	GPTIMER1_EVENT3
12	GPIO0_IRQ
13	GPIO1_IRQ
14	GPIO2_IRQ
15	GPIO3_IRQ
16	GPIO4_IRQ
17	GPIO5_IRQ
18	GPIO6_IRQ
19	Reserved
20	Reserved
21	Reserved
22	GPIO10_IRQ
23	GPIO11_IRQ
24	GPIO12_IRQ
25	GPIO13_IRQ
26	GPIO14_IRQ
27	GPIO15_IRQ
28	GPIO16_IRQ
29	GPIO17_IRQ
30	GPIO18_IRQ
31	GPIO19_IRQ
32	Reserved
33	Reserved
34	Reserved
35	Reserved
36	Reserved
37	Reserved
38	GPIO26_IRQ
39	GPIO27_IRQ
40	GPIO28_IRQ
41	GPIO29_IRQ
42	GPIO30_IRQ
43	GPIO31_IRQ
44	GPIO32_IRQ
45	GPIO33_IRQ
46	GPIO34_IRQ
47	GPIO35_IRQ

Table 5-9. I2S HW Event Selector Table (continued)

Select Config	Event Name
48	GPIO36_IRQ
49	GPIO37_IRQ
50	Reserved
51	Reserved
52	Reserved
53	Reserved
54	Reserved
55	Reserved
56	Reserved
57	SYS_TIMER_IRQ
58	SYS_TIMER_Heartbeat
59	SYS_TIMER_CH0_Event
60	SYS_TIMER_CH1_Event
61	SYS_TIMER_LFTICK_IRQ
62	Reserved
63	Reserved
64	RTC_IRQ
65	0

5.4.4.3 PDM HW Event Selector Mux

The table below shows the possible HW events input to the PDM. This should be configured in the SOC_AON.SPEVTCTL[22:16] PDM field.

Table 5-10. PDM HW Event Selector Table

Select Config	Event Name
0	0 (Logic Low)
1	1 (Logic High)
2	GPTIMER0_DMA_Trigger
3	GPTIMER0_EVENT0
4	GPTIMER0_EVENT1
5	GPTIMER0_EVENT2
6	GPTIMER0_EVENT3
7	GPTIMER1_DMA_Trigger
8	GPTIMER1_EVENT0
9	GPTIMER1_EVENT1
10	GPTIMER1_EVENT2
11	GPTIMER1_EVENT3
12	GPIO0_IRQ
13	GPIO1_IRQ
14	GPIO2_IRQ
15	GPIO3_IRQ
16	GPIO4_IRQ
17	GPIO5_IRQ
18	GPIO6_IRQ
19	Reserved
20	Reserved

Table 5-10. PDM HW Event Selector Table (continued)

Select Config	Event Name
21	Reserved
22	GPIO10_IRQ
23	GPIO11_IRQ
24	GPIO12_IRQ
25	GPIO13_IRQ
26	GPIO14_IRQ
27	GPIO15_IRQ
28	GPIO16_IRQ
29	GPIO17_IRQ
30	GPIO18_IRQ
31	GPIO19_IRQ
32	Reserved
33	Reserved
34	Reserved
35	Reserved
36	Reserved
37	Reserved
38	GPIO26_IRQ
39	GPIO27_IRQ
40	GPIO28_IRQ
41	GPIO29_IRQ
42	GPIO30_IRQ
43	GPIO31_IRQ
44	GPIO32_IRQ
45	GPIO33_IRQ
46	GPIO34_IRQ
47	GPIO35_IRQ
48	GPIO36_IRQ
49	GPIO37_IRQ
50	Reserved
51	Reserved
52	Reserved
53	Reserved
54	Reserved
55	Reserved
56	Reserved
57	SYS_TIMER_IRQ
58	SYS_TIMER_Heartbeat
59	SYS_TIMER_CH0_Event
60	SYS_TIMER_CH1_Event
61	SYS_TIMER_LFTICK_IRQ
62	Reserved
63	Reserved
64	RTC_IRQ

Table 5-10. PDM HW Event Selector Table (continued)

Select Config	Event Name
else	0

5.4.5 Timers MUX Selector Mux

The system timers (SysTimer and RTC) can be configured as subscribers for HW events from the Event Manager. These subscribers are different peripherals that must be configured differently according to the purpose of those specific peripherals. HW events input to these peripherals can be configured in the SOC_AON.TMEVTCTL register.

5.4.5.1 SysTimer0 HW Event Selector Mux

The table below shows the possible HW events input to SysTimer channel 0. This should be configured in the SOC_AON.TMEVTCTL[5:0] SYSTM0 field.

Table 5-11. SysTimer0 HW Event Selector Table

Select Config	Event Name
0	0 (Logic Low)
1	1 (Logic High)
2	GPTIMER0_DMA_Trigger
3	GPTIMER0_EVENT0
4	GPTIMER0_EVENT1
5	GPTIMER0_EVENT2
6	GPTIMER0_EVENT3
7	GPTIMER1_DMA_Trigger
8	GPTIMER1_EVENT0
9	GPTIMER1_EVENT1
10	GPTIMER1_EVENT2
11	GPTIMER1_EVENT3
12	ADC_Event
13	GPIO0_IRQ
14	GPIO1_IRQ
15	GPIO2_IRQ
16	GPIO3_IRQ
17	GPIO4_IRQ
18	GPIO5_IRQ
19	GPIO6_IRQ
20	Reserved
21	Reserved
22	Reserved
23	GPIO10_IRQ
24	GPIO11_IRQ
25	GPIO12_IRQ
26	GPIO13_IRQ
27	GPIO14_IRQ
28	GPIO15_IRQ
29	GPIO16_IRQ
30	GPIO17_IRQ
31	GPIO18_IRQ
32	GPIO19_IRQ

Table 5-11. SysTimer0 HW Event Selector Table (continued)

Select Config	Event Name
33	Reserved
34	Reserved
35	Reserved
36	Reserved
37	Reserved
38	Reserved
39	GPIO26_IRQ
40	GPIO27_IRQ
41	GPIO28_IRQ
42	GPIO29_IRQ
43	GPIO30_IRQ
44	GPIO31_IRQ
45	GPIO32_IRQ
46	GPIO33_IRQ
47	GPIO34_IRQ
48	GPIO35_IRQ
49	GPIO36_IRQ
50	GPIO37_IRQ
51	Reserved
52	Reserved
53	Reserved
54	Reserved
55	Reserved
56	Reserved
57	Reserved
58	Reserved
59	Reserved
else	0

5.4.5.2 SysTimer1 HW Event Selector Mux

The table below shows the possible HW events input to SysTimer channel 1. This should be configured in the SOC_AON.TMEVTCTL[13:8] SYSTM1 field.

Table 5-12. SysTimer1 HW Event Selector Table

Select Config	Event Name
0	0 (Logic Low)
1	1 (Logic High)
2	GPTIMER0_DMA_Trigger
3	GPTIMER0_EVENT0
4	GPTIMER0_EVENT1
5	GPTIMER0_EVENT2
6	GPTIMER0_EVENT3
7	GPTIMER1_DMA_Trigger
8	GPTIMER1_EVENT0
9	GPTIMER1_EVENT1
10	GPTIMER1_EVENT2

Table 5-12. SysTimer1 HW Event Selector Table (continued)

Select Config	Event Name
11	GPTIMER1_EVENT3
12	ADC_Event
13	GPIO0_IRQ
14	GPIO1_IRQ
15	GPIO2_IRQ
16	GPIO3_IRQ
17	GPIO4_IRQ
18	GPIO5_IRQ
19	GPIO6_IRQ
20	Reserved
21	Reserved
22	Reserved
23	GPIO10_IRQ
24	GPIO11_IRQ
25	GPIO12_IRQ
26	GPIO13_IRQ
27	GPIO14_IRQ
28	GPIO15_IRQ
29	GPIO16_IRQ
30	GPIO17_IRQ
31	GPIO18_IRQ
32	GPIO19_IRQ
33	Reserved
34	Reserved
35	Reserved
36	Reserved
37	Reserved
38	Reserved
39	GPIO26_IRQ
40	GPIO27_IRQ
41	GPIO28_IRQ
42	GPIO29_IRQ
43	GPIO30_IRQ
44	GPIO31_IRQ
45	GPIO32_IRQ
46	GPIO33_IRQ
47	GPIO34_IRQ
48	GPIO35_IRQ
49	GPIO36_IRQ
50	GPIO37_IRQ
51	Reserved
52	Reserved
53	Reserved
54	Reserved
55	Reserved

Table 5-12. SysTimer1 HW Event Selector Table (continued)

Select Config	Event Name
56	Reserved
57	Reserved
58	Reserved
59	Reserved
else	0

5.4.5.3 RTC HW Event Selector Mux

The table below shows the possible HW events input to RTC. This should be configured in the SOC_AON.TMEVTCTL[22:16] RTC field.

Table 5-13. RTC HW Event Selector Table

Select Config	Event Name
0	0 (Logic Low)
1	1 (Logic High)
2	GPTIMER0_DMA_Trigger
3	GPTIMER0_EVENT0
4	GPTIMER0_EVENT1
5	GPTIMER0_EVENT2
6	GPTIMER0_EVENT3
7	GPTIMER1_DMA_Trigger
8	GPTIMER1_EVENT0
9	GPTIMER1_EVENT1
10	GPTIMER1_EVENT2
11	GPTIMER1_EVENT3
12	ADC_Event
13	GPIO0_IRQ
14	GPIO1_IRQ
15	GPIO2_IRQ
16	GPIO3_IRQ
17	GPIO4_IRQ
18	GPIO5_IRQ
19	GPIO6_IRQ
20	Reserved
21	Reserved
22	Reserved
23	GPIO10_IRQ
24	GPIO11_IRQ
25	GPIO12_IRQ
26	GPIO13_IRQ
27	GPIO14_IRQ
28	GPIO15_IRQ
29	GPIO16_IRQ
30	GPIO17_IRQ
31	GPIO18_IRQ
32	GPIO19_IRQ
33	Reserved

Table 5-13. RTC HW Event Selector Table (continued)

Select Config	Event Name
34	Reserved
35	Reserved
36	Reserved
37	Reserved
38	Reserved
39	GPIO26_IRQ
40	GPIO27_IRQ
41	GPIO28_IRQ
42	GPIO29_IRQ
43	GPIO30_IRQ
44	GPIO31_IRQ
45	GPIO32_IRQ
46	GPIO33_IRQ
47	GPIO34_IRQ
48	GPIO35_IRQ
49	GPIO36_IRQ
50	GPIO37_IRQ
51	Reserved
52	Reserved
53	Reserved
54	Reserved
55	Reserved
56	Reserved
57	Reserved
58	SYS_TIMER_IRQ
59	SYS_TIMER_Heartbeat
60	SYS_TIMER_CH0_Event
61	SYS_TIMER_CH1_Event
62	SYS_TIMER_LFTICK_IRQ
63	Reserved
64	Reserved
else	0

5.4.6 GPTIMERs MUX Selector Mux

The GPTIMERs (GPTIMER0 and GPTIMER1) can be configured as subscribers for HW events from the Event Manager. These subscribers are different peripherals that must be configured differently according to the purpose of those specific peripherals.

5.4.6.1 GPTIMER0 HW Event Selector Mux

The table below shows the possible HW events input to GPTIMER0. This should be configured in the SOC_AON.GPT0EVTCTL0 register.

Table 5-14. GPTIMER0 HW Event Selector Table

Select Config	Event Name
0	1'b0
1	1'b1
2	UART0 IRQ

Table 5-14. GPTIMER0 HW Event Selector Table (continued)

Select Config	Event Name
3	UART1 IRQ
4	I2C0 IRQ
5	I2C1 IRQ
6	SPI0 IRQ
7	SPI1 IRQ
8	GPTIMER1 DMA Trigger
9	GPTIMER1 Event 0
10	GPTIMER1 Event 1
11	GPTIMER1 Event 2
12	GPTIMER1 Event 3
13	Reserved
14	I2S IRQ
15	PDM IRQ
16	DCAN IRQ 0
17	DCAN IRQ 1
18	ADC IRQ
19	ADC Event
20	GPIO0 IRQ
21	GPIO1 IRQ
22	GPIO2 IRQ
23	GPIO3 IRQ
24	GPIO4 IRQ
25	GPIO5 IRQ
26	GPIO6 IRQ
27	Reserved
28	Reserved
29	Reserved
30	GPIO10 IRQ
31	GPIO11 IRQ
32	GPIO12 IRQ
33	GPIO13 IRQ
34	GPIO14 IRQ
35	GPIO15 IRQ
36	GPIO16 IRQ
37	GPIO17 IRQ
38	GPIO18 IRQ
39	GPIO19 IRQ
40	Reserved
41	Reserved
42	Reserved
43	Reserved
44	Reserved
45	Reserved
46	GPIO26 IRQ
47	GPIO27 IRQ

Table 5-14. GPTIMER0 HW Event Selector Table (continued)

Select Config	Event Name
48	GPIO28 IRQ
49	GPIO29 IRQ
50	GPIO30 IRQ
51	GPIO31 IRQ
52	GPIO32 IRQ
53	GPIO33 IRQ
54	GPIO34 IRQ
55	GPIO35 IRQ
56	GPIO36 IRQ
57	GPIO37 IRQ
58	Reserved
59	Reserved
60	Reserved
61	Reserved
62	Reserved
63	Reserved
64	Reserved
65	Systimer IRQ
66	Systimer heartbeat
67	Systimer Ch0 Event
68	Systimer Ch1 Event
69	Systimer LFTICK IRQ
70	Reserved
71	Reserved
72	RTC IRQ
73	SoC Errors IRQ
else	1'b0

5.4.6.2 GPTIMER1 HW Event Selector Mux

The table below shows the possible HW events input to GPTIMER1. This should be configured in the SOC_AON.GPT1EVTCTL1 register.

Table 5-15. GPTIMER1 HW Event Selector Table

Select Config	Event Name
0	1'b0
1	1'b1
2	UART0 IRQ
3	UART1 IRQ
4	I2C0 IRQ
5	I2C1 IRQ
6	SPI0 IRQ
7	SPI1 IRQ
8	GPTIMER0 DMA Trigger
9	GPTIMER0 Event 0
10	GPTIMER0 Event 1
11	GPTIMER0 Event 2

Table 5-15. GPTIMER1 HW Event Selector Table (continued)

Select Config	Event Name
12	GPTIMER0 Event 3
13	Reserved
14	I2S IRQ
15	PDM IRQ
16	DCAN IRQ 0
17	DCAN IRQ 1
18	ADC IRQ
19	ADC Event
20	GPIO0 IRQ
21	GPIO1 IRQ
22	GPIO2 IRQ
23	GPIO3 IRQ
24	GPIO4 IRQ
25	GPIO5 IRQ
26	GPIO6 IRQ
27	Reserved
28	Reserved
29	Reserved
30	GPIO10 IRQ
31	GPIO11 IRQ
32	GPIO12 IRQ
33	GPIO13 IRQ
34	GPIO14 IRQ
35	GPIO15 IRQ
36	GPIO16 IRQ
37	GPIO17 IRQ
38	GPIO18 IRQ
39	GPIO19 IRQ
40	Reserved
41	Reserved
42	Reserved
43	Reserved
44	Reserved
45	Reserved
46	GPIO26 IRQ
47	GPIO27 IRQ
48	GPIO28 IRQ
49	GPIO29 IRQ
50	GPIO30 IRQ
51	GPIO31 IRQ
52	GPIO32 IRQ
53	GPIO33 IRQ
54	GPIO34 IRQ
55	GPIO35 IRQ
56	GPIO36 IRQ

Table 5-15. GPTIMER1 HW Event Selector Table (continued)

Select Config	Event Name
57	GPIO37 IRQ
58	Reserved
59	Reserved
60	Reserved
61	Reserved
62	Reserved
63	Reserved
64	Reserved
65	Systimer IRQ
66	Systimer heartbeat
67	Systimer Ch0 Event
68	Systimer Ch1 Event
69	Systimer LFTICK IRQ
70	Reserved
71	Reserved
72	RTC IRQ
73	SoC Errors IRQ
else	1'b0

5.5 SOC_IC Registers

Table 5-16 lists the memory-mapped registers for the SOC_IC registers. All register offset addresses not listed in Table 5-16 should be considered as reserved locations and the register contents should not be modified.

Table 5-16. SOC_IC Registers

Offset	Acronym	Register Name	Section
14h	ERRSTS1	Error Status Register	Section 5.5.1
18h	ERRSTS2	Error Status Register	Section 5.5.2
2Ch	AWSTAT1	Address Watch Status	Section 5.5.3
30h	AWSTAT2	Address Watch Status	Section 5.5.4

Complex bit access types are encoded to fit into small table cells. Table 5-17 shows the codes that are used for access types in this section.

Table 5-17. SOC_IC Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

5.5.1 ERRSTS1 Register (Offset = 14h) [Reset = 00000000h]

ERRSTS1 is shown in Table 5-18.

Return to the Summary Table.

OCP Peripheral Error and Timeout Status 1 Register. This register captures and maintains the status of Open Core Protocol (OCP) peripheral errors and timeout conditions. The register contains sticky status bits that record the first error occurrence when an OCP peripheral responds with a System Error (SERROR). Once an error is captured, the status bits remain set until explicitly cleared by writing to this register. This mechanism allows for error detection and diagnostic purposes by preserving the first error condition until acknowledged. Write any value to clear all status bits to zero.

Table 5-18. ERRSTS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MADDR	R/W	0h	Memory Error Status bits that indicate when the On-Chip Protocol (OCP) peripheral responded with a system error (SERROR). This 32-bit field [31:0] stores the memory address (maddr) where the error occurred. This register is sticky, meaning it captures and holds the first error until explicitly cleared. To clear this register, write 0x00000000 to it. Note that writing to any byte of this register will clear all 4 bytes. Read operation returns the memory address of the first error detected since the last clear operation.

5.5.2 ERRSTS2 Register (Offset = 18h) [Reset = 00000000h]

ERRSTS2 is shown in Table 5-19.

Return to the Summary Table.

OCP Slave Serious Error and Timeout Status Register 2. This register maintains the status of serious errors and timeout conditions for the OCP (Open Core Protocol) slave interface. It captures error conditions that require attention, providing visibility into communication faults between the system and slave devices. The register can be read to diagnose problems and written to clear specific status flags.

Table 5-19. ERRSTS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	ERRSTA2	R/W	0h	Status bits that report Open Core Protocol (OCP) peripheral response errors (SERROR) or timeouts. This field is sticky and captures the first error until the register is cleared by writing 0. The field contains the following information: Bits [9:6] - Error Cause: - 0: Controllers - 1: Core Always-On (AON) - 2: Hardware Security Module (HSM) - 3: Host Execute-In-Place (XIP) - 4: Host Direct Memory Access (DMA) - 5: Host Microcontroller Unit (MCU) - 6: Shared Peripherals - 7: App-to-NAB - 8: Core WSOCIC - 9: L3 Peripherals Bits [5:4] - Command Type (MCMD): - 1: Write operation - 2: Read operation Bits [3:0] - Controller ID: If cause is 'Controllers', the Controller ID is mapped according to TOMSTCFG.SEL. Otherwise, Controller ID mapping is as follows: - 0: M33NS (Non-secure M33) - 1: M33S (Secure M33) - 6: Core (WSOC_IC) - 8: I2S/HSM M33NS access - 9: I2S/HSM M33S access - 10: I2S/HSM Core access - 12: DMA M33NS access - 13: DMA M33S access - 14: DMA Core access Note: This field can only be cleared by writing all bits to 0. Writing to any byte will clear the entire 2-byte field.

5.5.3 AWSTAT1 Register (Offset = 2Ch) [Reset = 00000000h]

AWSTAT1 is shown in Table 5-20.

Return to the Summary Table.

Address Watch Status 1.

Table 5-20. AWSTAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	AWADDR	R/W	0h	keep when hit - Clear on Write [31:0] - maddr

5.5.4 AWSTAT2 Register (Offset = 30h) [Reset = 00000000h]

AWSTAT2 is shown in Table 5-21.

Return to the Summary Table.

Address Watch Status Register 2. This 32-bit read-write register displays the status information for the second address watch point. It reports when memory access matches configured watch conditions and provides status flags for debugging purposes. The register can be cleared by writing to it, allowing for the reset of status flags after processing a watch event.

Table 5-21. AWSTAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	AWCMD	R/W	0h	Address Watch Status 2 Write Options Field. This field provides information about the transaction that triggered the address watch. The information is preserved when a hit occurs and can be cleared by writing to this field. The field consists of: - Bit [4]: Command type indicator (0 = Read operation, 1 = Write operation) - Bits [3:0]: Master ID that identifies the source of the transaction with the following mapping: - 0: M33 Non-Secure mode - 1: M33 Secure mode - 6: Core (wsoc_ic) - 8: I2S/HSM in M33 Non-Secure access mode - 9: I2S/HSM in M33 Secure access mode - 10: I2S/HSM in Core access mode - 12: DMA in M33 Non-Secure access mode - 13: DMA in M33 Secure access mode - 14: DMA in Core access mode

5.6 SOC_AON Registers

Table 5-22 lists the memory-mapped registers for the SOC_AON registers. All register offset addresses not listed in Table 5-22 should be considered as reserved locations and the register contents should not be modified.

Table 5-22. SOC_AON Registers

Offset	Acronym	Register Name	Section
Ch	SPEVTCTL	Peripheral Interrupt Control	Section 5.6.1
10h	TMEVTCTL	Timers Interrupt Control	Section 5.6.2
14h	GPT0EVTCTL0	GPTIMER0 Interrupt Control 0	Section 5.6.3
18h	GPT1EVTCTL0	GPTIMER1 Interrupt Control	Section 5.6.4
54h	DMEMSTART	Data Ram Start Adress	Section 5.6.5
58h	DMEMEND	Data Ram End Adress	Section 5.6.6
64h	TCMSTART	TCM Data Ram Start Adress	Section 5.6.7
68h	TCMEND	TCM Data Ram End Adress	Section 5.6.8
7Ch	GPIOEVTS0	GPIO Event Status 0	Section 5.6.9
80h	GPIOEVTS1	GPIO Event Status 1	Section 5.6.10
84h	MEMSSCTL0	MEMSS Control 0	Section 5.6.11
88h	MEMSSCTL1	MEMSS Control 1	Section 5.6.12
9Ch	VTORS	VTOR Host Secure Address	Section 5.6.13
A0h	VTORNS	VTOR Host Non-Secure Address	Section 5.6.14
A8h	CPULOCKS	CPU Locks	Section 5.6.15
ACh	HOSTLOCKS	Host Locks	Section 5.6.16
B0h	HOSTBOOT	Host Boot Done	Section 5.6.17
B4h	SECCFG	Security Configurations	Section 5.6.18
D4h	ERRSIMASK	Error Host Secured Interrupt Mask	Section 5.6.19
D8h	ERRSISET	Error Host Secured Interrupt Set	Section 5.6.20
DCh	ERRSICLR	Error Host Secured Interrupt Clear	Section 5.6.21
E0h	ERRSIMSET	Error Host Secured Masked Interrupt Set	Section 5.6.22
E4h	ERRSIMCLR	Error Host Secured Masked Interrupt Clear	Section 5.6.23
E8h	ERRSRIS	Error Host Secured Raw Interrupt Status	Section 5.6.24
ECh	ERRSMIS	Doorbell Host Secured Masked Interrupt Status	Section 5.6.25
F0h	GPT0EVTCTL1	GPTIMER0 Interrupt Control 1	Section 5.6.26
F4h	GPT1EVTCTL1	GPTIMER1 Interrupt Control 1	Section 5.6.27
104h	ESMSTACST	ESM's Status	Section 5.6.28
10Ch	MEMSSCFG	MEMSS Configurations	Section 5.6.29
138h	GPIOMIS0S	GPIO's Masked Interrupt Status 0	Section 5.6.30
13Ch	GPIOMIS1S	GPIO's Masked Interrupt Status 1	Section 5.6.31
140h	GPIOFNC0S	GPIO's Interrupt Mask 0	Section 5.6.32
144h	GPIOFNC1S	GPIO's Interrupt Mask 1	Section 5.6.33
14Ch	ESM1VAL2ND	ESM1 Second Magic Value	Section 5.6.34
150h	ESM2VAL2ND	ESM2 Second Magic Value	Section 5.6.35
154h	ESM1STA2ND	ESM1 Second Magic Value Status	Section 5.6.36
158h	ESM2STA2ND	ESM2 Second Magic Value Status	Section 5.6.37
15Ch	FWCFGHOST	Host Firewall Bypass	Section 5.6.38
160h	FWCFGDMA	DMA Firewall Bypass	Section 5.6.39
164h	FWCFGFPRPH	Peripherals Firewall Bypass	Section 5.6.40
168h	FWCFGM33	Cortex Firewall Bypass	Section 5.6.41

Table 5-22. SOC_AON Registers (continued)

Offset	Acronym	Register Name	Section
16Ch	FWCFGMEMSS	MEMSS Firewall Bypass	Section 5.6.42
170h	FWIOGENSEL	IOMUX Common Firewall Configuration	Section 5.6.43
174h	FWPRCMHOST	PRCM HOST Firewall Configuration	Section 5.6.44
178h	FWPRCMSPAD	PRCM Scratchpad Firewall Configuration	Section 5.6.45
17Ch	FWPRCMCMN	PRCM Common Firewall Configuration	Section 5.6.46
180h	FWCKM	Clock Manager Firewall Configuration	Section 5.6.47
184h	FWSOCIC	Interconnect Firewall Configuration	Section 5.6.48
188h	FWAONM33S	SOC AON Host Secure Aperture Firewall Configuration	Section 5.6.49
18Ch	FWAONM33NS	SOC AON Host Non-Secure Aperture Firewall Configuration	Section 5.6.50
190h	FWAAONM33S	SOC AAON Host Secure Aperture Firewall Configuration	Section 5.6.51
194h	FWAAONM33NS	SOC AAON Host Non-Secure Aperture Firewall Configuration	Section 5.6.52
198h	FWCMNRTC	RTC Firewall Configuration	Section 5.6.53
19Ch	FWMEMSS0	MEMSS Region 0 Firewall Configuration	Section 5.6.54
1A0h	FWMEMSS1	MEMSS Region 1 Firewall Configuration	Section 5.6.55
1A4h	FWMEMSS2	MEMSS Region 2 Firewall Configuration	Section 5.6.56
1A8h	FWHOSTAON	HOST AON Target Firewall Configuration	Section 5.6.57
1B0h	FWHIF	HIF Firewall Configuration	Section 5.6.58
1B4h	FWHOST0	HOST Target Region 0 Firewall Configuration	Section 5.6.59
1B8h	FWHOST1	HOST Target Region 1 Firewall Configuration	Section 5.6.60
1BCh	FWHOST2	HOST Target Region 2 Firewall Configuration	Section 5.6.61
1C0h	FWHOST3	HOST Target Region 3 Firewall Configuration	Section 5.6.62
1C4h	FWHOST4	HOST Target Region 4 Firewall Configuration	Section 5.6.63
1C8h	FWHOST5	HOST Target Region 5 Firewall Configuration	Section 5.6.64
1CCh	FWHOST6	HOST Target Region 6 Firewall Configuration	Section 5.6.65
1D0h	FWHOST7	HOST Target Region 7 Firewall Configuration	Section 5.6.66
1D4h	FWHOST8	HOST Target Region 8 Firewall Configuration	Section 5.6.67
1D8h	FWHOST9	HOST Target Region 9 Firewall Configuration	Section 5.6.68
1DCh	FWHOST10	HOST Target Region 10 Firewall Configuration	Section 5.6.69
1E0h	FWHOST11	HOST Target Region 11 Firewall Configuration	Section 5.6.70
1E4h	FWXIPOSPI	xSPI Registers Firewall Configuration	Section 5.6.71
1E8h	FWXIPINDAC	xSPI Indac Firewall Configuration	Section 5.6.72
1ECh	FWXIPGEN	xSPI General Firewall Configuration	Section 5.6.73
1F0h	FWXIPUDMAS	xSPI uDMA Secured Firewall Configuration	Section 5.6.74
1F4h	FWXIPUDMANS	xSPI uDMA Non-Secured Firewall Configuration	Section 5.6.75
1F8h	FWOTFDE0	xSPI OTFDE 0 Firewall Configuration	Section 5.6.76
1FCh	FWOTFDE1	xSPI OTFDE 1 Firewall Configuration	Section 5.6.77
200h	FWOTFDE2	xSPI OTFDE 2 Firewall Configuration	Section 5.6.78
204h	FWOTFDE3	xSPI OTFDE 3 Firewall Configuration	Section 5.6.79
208h	FWDMAGEN	DMA Target Common Firewall Configuration	Section 5.6.80
20Ch	FWDMA0	DMA Target Region 0 Firewall Configuration	Section 5.6.81
210h	FWDMA1	DMA Target Region 1 Firewall Configuration	Section 5.6.82
214h	FWDMA2	DMA Target Region 2 Firewall Configuration	Section 5.6.83
218h	FWDMA3	DMA Target Region 3 Firewall Configuration	Section 5.6.84
21Ch	FWDMA4	DMA Target Region 4 Firewall Configuration	Section 5.6.85

Table 5-22. SOC_AON Registers (continued)

Offset	Acronym	Register Name	Section
220h	FWDMA5	DMA Target Region 5 Firewall Configuration	Section 5.6.86
224h	FWDMA6	DMA Target Region 6 Firewall Configuration	Section 5.6.87
228h	FWDMA7	DMA Target Region 7 Firewall Configuration	Section 5.6.88
22Ch	FWDMA8	DMA Target Region 8 Firewall Configuration	Section 5.6.89
230h	FWDMA9	DMA Target Region 9 Firewall Configuration	Section 5.6.90
234h	FWDMA10	DMA Target Region 10 Firewall Configuration	Section 5.6.91
238h	FWDMA11	DMA Target Region 11 Firewall Configuration	Section 5.6.92
23Ch	FWHSMEIPNS	HSM EIP Non-Secured Registers Firewall Configuration	Section 5.6.93
240h	FWHSMEIPS	HSM EIP Secured Registers Firewall Configuration	Section 5.6.94
244h	FWHSMWRAPNS	HSM Non-Secured Wrapper Firewall Configuration	Section 5.6.95
248h	FWHSMWRAPS	HSM Secured Wrapper Firewall Configuration	Section 5.6.96
24Ch	FWHSMDBG	HSM Debug Memory Firewall Configuration	Section 5.6.97
250h	FWI2C0	I2C 0 Firewall Configuration	Section 5.6.98
254h	FWI2C1	I2C 1 Firewall Configuration	Section 5.6.99
258h	FWSPSPI0	SPI 0 Firewall Configuration	Section 5.6.100
25Ch	FWSPSPI1	SPI 1 Firewall Configuration	Section 5.6.101
260h	FWSPUART0	UART 0 Firewall Configuration	Section 5.6.102
264h	FWSPUART1	UART 1 Firewall Configuration	Section 5.6.103
268h	FWSPGPT0	GPTIMER0 Firewall Configuration	Section 5.6.104
26Ch	FWSPGPT1	GPTIMER1 Firewall Configuration	Section 5.6.105
270h	FWSPI2S	I2S Firewall Configuration	Section 5.6.106
274h	FWPDM	PDM Firewall Configuration	Section 5.6.107
278h	FWSPCAN	DCAN Firewall Configuration	Section 5.6.108
27Ch	FWSPADC	ADC Firewall Configuration	Section 5.6.109
280h	FWSPSDMMC	SDMMC Firewall Configuration	Section 5.6.110
284h	FWSPSDIO	SDIO CARD Firewall Configuration	Section 5.6.111
288h	FWSPUART2	UART 2 Firewall Configuration	Section 5.6.112
28Ch	UDMANSCTL	uDMA Non-Secured Channel Control	Section 5.6.113
290h	FWIOPAD0	IOMUX PAD 0 Firewall Configuration	Section 5.6.114
294h	FWIOPAD1	IOMUX PAD 1 Firewall Configuration	Section 5.6.115
298h	FWIOPAD2	IOMUX PAD 2 Firewall Configuration	Section 5.6.116
29Ch	FWIOPAD3	IOMUX PAD 3 Firewall Configuration	Section 5.6.117
2A0h	FWIOPAD4	IOMUX PAD 4 Firewall Configuration	Section 5.6.118
2A4h	FWIOPAD5	IOMUX PAD 5 Firewall Configuration	Section 5.6.119
2A8h	FWIOPAD6	IOMUX PAD 6 Firewall Configuration	Section 5.6.120
2ACh	FWIOPAD7	IOMUX PAD 7 Firewall Configuration	Section 5.6.121
2B0h	FWIOPAD8	IOMUX PAD 8 Firewall Configuration	Section 5.6.122
2B4h	FWIOPAD9	IOMUX PAD 9 Firewall Configuration	Section 5.6.123
2B8h	FWIOPAD10	IOMUX PAD 10 Firewall Configuration	Section 5.6.124
2BCh	FWIOPAD11	IOMUX PAD 11 Firewall Configuration	Section 5.6.125
2C0h	FWIOPAD12	IOMUX PAD 12 Firewall Configuration	Section 5.6.126
2C4h	FWIOPAD13	IOMUX PAD 13 Firewall Configuration	Section 5.6.127
2C8h	FWIOPAD14	IOMUX PAD 14 Firewall Configuration	Section 5.6.128
2CCh	FWIOPAD15	IOMUX PAD 15 Firewall Configuration	Section 5.6.129
2D0h	FWIOPAD16	IOMUX PAD 16 Firewall Configuration	Section 5.6.130

Table 5-22. SOC_AON Registers (continued)

Offset	Acronym	Register Name	Section
2D4h	FWIOPAD17	IOMUX PAD 17 Firewall Configuration	Section 5.6.131
2D8h	FWIOPAD18	IOMUX PAD 18 Firewall Configuration	Section 5.6.132
2DCh	FWIOPAD19	IOMUX PAD 19 Firewall Configuration	Section 5.6.133
2E0h	FWIOPAD20	IOMUX PAD 20 Firewall Configuration	Section 5.6.134
2E4h	FWIOPAD21	IOMUX PAD 21 Firewall Configuration	Section 5.6.135
2E8h	FWIOPAD22	IOMUX PAD 22 Firewall Configuration	Section 5.6.136
2ECh	FWIOPAD23	IOMUX PAD 23 Firewall Configuration	Section 5.6.137
2F0h	FWIOPAD24	IOMUX PAD 24 Firewall Configuration	Section 5.6.138
2F4h	FWIOPAD25	IOMUX PAD 25 Firewall Configuration	Section 5.6.139
2F8h	FWIOPAD26	IOMUX PAD 26 Firewall Configuration	Section 5.6.140
2FCh	FWIOPAD27	IOMUX PAD 27 Firewall Configuration	Section 5.6.141
300h	FWIOPAD28	IOMUX PAD 28 Firewall Configuration	Section 5.6.142
304h	FWIOPAD29	IOMUX PAD 29 Firewall Configuration	Section 5.6.143
308h	FWIOPAD30	IOMUX PAD 30 Firewall Configuration	Section 5.6.144
30Ch	FWIOPAD31	IOMUX PAD 31 Firewall Configuration	Section 5.6.145
310h	FWIOPAD32	IOMUX PAD 32 Firewall Configuration	Section 5.6.146
314h	FWIOPAD33	IOMUX PAD 33 Firewall Configuration	Section 5.6.147
318h	FWIOPAD34	IOMUX PAD 34 Firewall Configuration	Section 5.6.148
31Ch	FWIOPAD35	IOMUX PAD 35 Firewall Configuration	Section 5.6.149
320h	FWIOPAD36	IOMUX PAD 36 Firewall Configuration	Section 5.6.150
324h	FWIOPAD37	IOMUX PAD 37 Firewall Configuration	Section 5.6.151
328h	FWIOPAD38	IOMUX PAD 38 Firewall Configuration	Section 5.6.152
32Ch	FWIOPAD39	IOMUX PAD 39 Firewall Configuration	Section 5.6.153
330h	FWIOPAD40	IOMUX PAD 40 Firewall Configuration	Section 5.6.154
334h	FWIOPAD41	IOMUX PAD 41 Firewall Configuration	Section 5.6.155
338h	FWIOPAD42	IOMUX PAD 42 Firewall Configuration	Section 5.6.156
33Ch	FWIOPAD43	IOMUX PAD 43 Firewall Configuration	Section 5.6.157
340h	FWIOPAD44	IOMUX PAD 44 Firewall Configuration	Section 5.6.158
344h	FWIOPAD45	IOMUX PAD 45 Firewall Configuration	Section 5.6.159
348h	FWIOPAD46	IOMUX PAD 46 Firewall Configuration	Section 5.6.160
34Ch	FWIOPAD47	IOMUX PAD 47 Firewall Configuration	Section 5.6.161
350h	FWIOPAD48	IOMUX PAD 48 Firewall Configuration	Section 5.6.162
354h	FWDMA12	DMA Target Region 12 Firewall Configuration	Section 5.6.163
358h	FWDMA13	DMA Target Region 13 Firewall Configuration	Section 5.6.164
1000h	USECSTB	Micro Second STB	Section 5.6.165
1044h	GPIOEVT0NS	GPIO Event Status 0	Section 5.6.166
1048h	GPIOEVT1NS	GPIO Event Status 1	Section 5.6.167
1054h	DBM33NS0	Doorbell Host Non-Secured Interrupt Mask	Section 5.6.168
1058h	DBNSISET	Doorbell Host Non-Secured Interrupt Set	Section 5.6.169
105Ch	DBNSICLR	Doorbell Host Non-Secured Interrupt Clear	Section 5.6.170
1060h	DBNSIMSET	Doorbell Host Non-Secured Masked Interrupt Set	Section 5.6.171
1064h	DBNSIMCLR	Doorbell Host Non-Secured Masked Interrupt Clear	Section 5.6.172
1068h	DBNSRIS	Doorbell Host Non-Secured Raw Interrupt Status	Section 5.6.173
106Ch	DBNSMIS	Doorbell Host Non-Secured Masked Interrupt Status	Section 5.6.174
1070h	GPIOMIS0NS	GPIO's Non-Secured Masked Interrupt Status 0	Section 5.6.175

Table 5-22. SOC_AON Registers (continued)

Offset	Acronym	Register Name	Section
1074h	GPIOMIS1NS	GPIO's Non-Secured Masked Interrupt Status 1	Section 5.6.176
1078h	GPIOFNC0NS	GPIO's Non-Secured Function 0	Section 5.6.177
107Ch	GPIOFNC1NS	GPIO's Non-Secured Function 1	Section 5.6.178

Complex bit access types are encoded to fit into small table cells. Table 5-23 shows the codes that are used for access types in this section.

Table 5-23. SOC_AON Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

5.6.1 SPEVTCTL Register (Offset = Ch) [Reset = 00000000h]

SPEVTCTL is shown in Table 5-24.

Return to the Summary Table.

Shared Peripherals Event MUXs Selectors. This register selects events to ADC, I2S and PDM.

Table 5-24. SPEVTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Reserved
22-16	PDM	R/W	0h	PDM Event Selector. This field selects event to PDM.
15	RESERVED	R	0h	Reserved
14-8	I2S	R/W	0h	I2S Event Selector. This field selects event to I2S.
7-6	RESERVED	R	0h	Reserved
5-0	ADC	R/W	0h	ADC Event Selector. This field selects event to ADC.

5.6.2 TMEVTCTL Register (Offset = 10h) [Reset = 00000000h]

TMEVTCTL is shown in Table 5-25.

Return to the Summary Table.

Timers Event MUXs Selectors. This register selects events to SYSTIMER and RTC. There are two MUXs of SYSTIMER and one for RTC.

Table 5-25. TMEVTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Reserved
22-16	RTC	R/W	0h	RTC Event Selector. This field selects event to RTC.
15-14	RESERVED	R	0h	Reserved
13-8	SYSTM1	R/W	0h	SYSTIMER Event 2nd Selector. This field selects event to SYSTIMER.
7-6	RESERVED	R	0h	Reserved
5-0	SYSTM0	R/W	0h	SYSTIMER Event 1st Selector. This field selects event to SYSTIMER.

5.6.3 GPT0EVTCTL0 Register (Offset = 14h) [Reset = 00000000h]

GPT0EVTCTL0 is shown in Table 5-26.

Return to the Summary Table.

GPTIMER0 Channels Event MUXs Selectors. This register selects events to GPTIMER0. There are 4 event MUXs for GPTIMER Channels.

Table 5-26. GPT0EVTCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-21	CH3SEL	R/W	0h	This field selects MUX output to CH3 of GPTIMER0 IRQ.
20-14	CH2SEL	R/W	0h	This field selects MUX output to CH2 of GPTIMER0 IRQ.
13-7	CH1SEL	R/W	0h	This field selects MUX output to CH1 of GPTIMER0 IRQ.
6-0	CH0SEL	R/W	0h	This field selects MUX output to CH0 of GPTIMER0 IRQ.

5.6.4 GPT1EVTCTL0 Register (Offset = 18h) [Reset = 00000000h]

GPT1EVTCTL0 is shown in Table 5-27.

Return to the Summary Table.

GPTIMER1 Event MUXs Selectors. This register selects events to GPTIMER1. There are 4 event MUXs for GPTIMER Channels.

Table 5-27. GPT1EVTCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-21	CH3SEL	R/W	0h	This field selects MUX output to CH3 of GPTIMER1 IRQ.
20-14	CH2SEL	R/W	0h	This field selects MUX output to CH2 of GPTIMER1 IRQ.
13-7	CH1SEL	R/W	0h	This field selects MUX output to CH1 of GPTIMER1 IRQ.
6-0	CH0SEL	R/W	0h	This field selects MUX output to CH0 of GPTIMER1 IRQ.

5.6.5 DMEMSTART Register (Offset = 54h) [Reset = 28000000h]

DMEMSTART is shown in Table 5-28.

Return to the Summary Table.

DATA Memory MEMSS Start Address. DMEM Start Address-also define S/NS region split

Table 5-28. DMEMSTART Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	ADDR	R/W	00028000h	DMEM Start Address-also define S/NS region split
11-0	RESERVED	R	0h	Reserved

5.6.6 DMEMEND Register (Offset = 58h) [Reset = 2FFFFFFFh]

DMEMEND is shown in Table 5-29.

Return to the Summary Table.

DATA Memory MEMSS End Address. DMEM end Address-also define S/NS region split

Table 5-29. DMEMEND Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	ADDR	R/W	0002FFFFh	DMEM end Address-also define S/NS region split
11-0	RESERVED	R	0h	Reserved

5.6.7 TCMSTART Register (Offset = 64h) [Reset = 20000000h]

TCMSTART is shown in Table 5-30.

Return to the Summary Table.

TCM DATA Memory MEMSS Start Address. TCM data Start Address-also define S/NS region split

Table 5-30. TCMSTART Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	ADDR	R/W	00080000h	TCM data Start Address-also define S/NS region split
9-0	RESERVED	R	0h	Reserved

5.6.8 TCMEND Register (Offset = 68h) [Reset = 27FFFFFFh]

TCMEND is shown in Table 5-31.

Return to the Summary Table.

TCM DATA Memory MEMSS End Address. TCM data end Address-also define S/NS region split

Table 5-31. TCMEND Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	ADDR	R/W	0009FFFFh	TCM data end Address-also define S/NS region split
9-0	RESERVED	R	0h	Reserved

5.6.9 GPIOEVTS0 Register (Offset = 7Ch) [Reset = 00000000h]

GPIOEVTS0 is shown in Table 5-32.

Return to the Summary Table.

Secured GPIO Event Status, 1st Register. 45 bits status over two registers.

Table 5-32. GPIOEVTS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STA31TO0	R	0h	Secured event status , first 32 bits. ([31:0])

5.6.10 GPIOEVTS1 Register (Offset = 80h) [Reset = 00000000h]

GPIOEVTS1 is shown in Table 5-33.

Return to the Summary Table.

Secured GPIO Event Status, 2nd Register. 45 bits status over two registers.

Table 5-33. GPIOEVTS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	STA44TO32	R	0h	Secured event status , 13 MSBs. ([44:32])

5.6.11 MEMSSCTL0 Register (Offset = 84h) [Reset = 00000000h]

MEMSSCTL0 is shown in Table 5-34.

Return to the Summary Table.

MEMSS General Control Register. This register controls starvation mechanism counter value and MEMSS bus fault mask.

Table 5-34. MEMSSCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6-4	BFLTMSTA	R	0h	Bus Fault Masked Status. Out of Memory Index: 0. No error 1. M33 Code 2. M33 Data #1 + #2 3. M3 Code 4. M3 Data 5. M3 PRAM 6. BLE Code 7. Global OCP
3	BFLTMASK	R/W	0h	MEMSS Bus Fault Mask 1. Mask 0. Do not mask
2-0	STRVCNTV	R/W	0h	Starvation Counter Value Configuration. That value reflect how long writing to mailbox can be delayed.

5.6.12 MEMSSCTL1 Register (Offset = 88h) [Reset = 00000000h]

MEMSSCTL1 is shown in Table 5-35.

Return to the Summary Table.

MEMSS General Control Register. This is a status register for bus fault raw status.

Table 5-35. MEMSSCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	BFLTRWSTA	R	0h	Bus Fault Raw Status. Error indication from memss. Out of Memory Index: 0. No error 1. M33 Code 2. M33 Data #1 + #2 3. M3 Code 4. M3 Data 5. M3 PRAM 6. BLE Code 7. Global OCP Type: Read-Clear

5.6.13 VTORS Register (Offset = 9Ch) [Reset = 00000000h]

VTORS is shown in Table 5-36.

Return to the Summary Table.

M33 Secure Vector Table Base Address.

Table 5-36. VTORS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	ADDR	R/W	0h	init VTOR Secured Address.
6-0	RESERVED	R	0h	Reserved

5.6.14 VTORNS Register (Offset = A0h) [Reset = 00000000h]

VTORNS is shown in Table 5-37.

Return to the Summary Table.

M33 Non-Secure Vector Table Base Address.

Table 5-37. VTORNS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	ADDR	R/W	0h	init VTOR non Secured address
6-0	RESERVED	R	0h	Reserved

5.6.15 CPULOCKS Register (Offset = A8h) [Reset = 00000000h]

CPULOCKS is shown in Table 5-38.

Return to the Summary Table.

CPU Locks. This register contain 5 locks. Issued to M33 Cortex and used to lock internal cortex registers. LOCKSVTAIRCR, LOCKNSVTOR, LOCKSMPU, LOCKNSMPU, LOCKSAU.

Table 5-38. CPULOCKS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	SAU	R/W	0h	Locking this Cortex internal configuration
3	NSPMU	R/W	0h	Locking this Cortex internal configuration
2	SMPU	R/W	0h	Locking this Cortex internal configuration
1	NSVTOR	R/W	0h	Locking this Cortex internal configuration
0	SVTAIRCR	R/W	0h	Locking this Cortex internal configuration

5.6.16 HOSTLOCKS Register (Offset = ACh) [Reset = 00000000h]

HOSTLOCKS is shown in Table 5-39.

Return to the Summary Table.

Host Lock Signals. lock once. Do Not lock until written. When written Locked immediately, cleared only at soc aon reset or por reset. These are host security lock configurations (some can be also locked by TI)

Table 5-39. HOSTLOCKS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	PERIPHEVT	R/W	0h	Locking the firewall configurations of: HIF, CORE, CORE AON, HSM, shared Periphs
5	M3EVT	R/W	0h	Locking the configurations of M3 Events
4	FLASH	R/W	0h	Locking the configurations of On The Fly Enc/Decryption Module Region Related Registers (four registers per region, four regions)
3	DMA	R/W	0h	Locking the configurations of System DMA
2	MEMSSANDFW	R/W	0h	Locking the configurations of Memory Sub System
1	M33	R/W	0h	Locking the configurations of Host MCU, both Secured and non Secured
0	CACHE	R/W	0h	Locking the configurations of ICACHE

5.6.17 HOSTBOOT Register (Offset = B0h) [Reset = 00000000h]

HOSTBOOT is shown in Table 5-40.

Return to the Summary Table.

Host Boot Done 1 lock. Write once. Asserted by FW by the end of soc boot done Or in elevated mode By either by TI of by the host and indicates device exit from secure boot mode. this signal also locks host security configurations , Locked immediately , cleared only at soc aon reset or por reset

Table 5-40. HOSTBOOT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	DONE	R/W	0h	Locking host security configurations

5.6.18 SECCFG Register (Offset = B4h) [Reset = 00000000h]

SECCFG is shown in Table 5-41.

Return to the Summary Table.

Security Configurations.

Table 5-41. SECCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	BLKSBSWR	R/W	0h	BLOCK SBUS WRITE LOCK Enable this field to block sbus write transactions
1	SELNSIRQ	R/W	0h	This field determine whether the 4 SW interrupts MSbits will be owned by secured/non secured. 0. Non-Secured 1. Secured
0	BLKDMA	R/W	0h	This Field blocks the uDMA transactions to CMEM. 0. un-Block 1. Block

5.6.19 ERRSIMASK Register (Offset = D4h) [Reset = 00000000h]

ERRSIMASK is shown in Table 5-42.

Return to the Summary Table.

M33 Secured Error IMASK. Mask Event. '0' - CLR - Clear Interrupt Mask '1' - SET - Set Interrupt Mask

Table 5-42. ERRSIMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8-0	IMASK	R/W	0h	Bits division to events: bit[8] - UDMA ERR IRQ bit[7] - CORE ELP WATCHDOG Timer bit[6] - SOC IC IRQs - Address Watch bit[5] - SOC IC IRQs - IC Timeout bit[4] - SOC IC IRQs - serror bit[3] - CORE to SDIO WATCHDOG bit[2] - PLL Unlock bit[1] - MEMss bus fault bit[0] - HSM fatal error

5.6.20 ERRSISET Register (Offset = D8h) [Reset = 00000000h]

ERRSISET is shown in Table 5-43.

Return to the Summary Table.

M33 Secured Error ISET. Sets event in RIS Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - SET - Sets interrupt

Table 5-43. ERRSISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8-0	ISET	W	0h	Bits division to events: bit[8] - UDMA ERR IRQ bit[7] - CORE ELP WATCHDOG Timer bit[6] - SOC IC IRQs - Address Watch bit[5] - SOC IC IRQs - IC Timeout bit[4] - SOC IC IRQs - serror bit[3] - CORE to SDIO WATCHDOG bit[2] - PLL Unlock bit[1] - MEMss bus fault bit[0] - HSM fatal error Type: Write-Clear

5.6.21 ERRSICLR Register (Offset = DCh) [Reset = 00000000h]

ERRSICLR is shown in Table 5-44.

Return to the Summary Table.

M33 Secured Error ICLR. Clears event in RIS Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - CLR - Clears the Event

Table 5-44. ERRSICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8-0	ICLR	W	0h	Bits division to events: bit[8] - UDMA ERR IRQ bit[7] - CORE ELP WATCHDOG Timer bit[6] - SOC IC IRQs - Address Watch bit[5] - SOC IC IRQs - IC Timeout bit[4] - SOC IC IRQs - serror bit[3] - CORE to SDIO WATCHDOG bit[2] - PLL Unlock bit[1] - MEMss bus fault bit[0] - HSM fatal error Type: Write-Clear

5.6.22 ERRSIMSET Register (Offset = E0h) [Reset = 00000000h]

ERRSIMSET is shown in Table 5-45.

Return to the Summary Table.

M33 Secured Error IMSET. Sets Event Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - SET - Set interrupt mask

Table 5-45. ERRSIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8-0	IMSET	W	0h	Bits division to events: bit[8] - UDMA ERR IRQ bit[7] - CORE ELP WATCHDOG Timer bit[6] - SOC IC IRQs - Address Watch bit[5] - SOC IC IRQs - IC Timeout bit[4] - SOC IC IRQs - serror bit[3] - CORE to SDIO WATCHDOG bit[2] - PLL Unlock bit[1] - MEMss bus fault bit[0] - HSM fatal error Type: Write-Clear

5.6.23 ERRSIMCLR Register (Offset = E4h) [Reset = 00000000h]

ERRSIMCLR is shown in Table 5-46.

Return to the Summary Table.

M33 Secured Error IMCLR. Clears Event Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - CLR - Clear interrupt mask

Table 5-46. ERRSIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8-0	IMCLR	W	0h	Bits division to events: bit[8] - UDMA ERR IRQ bit[7] - CORE ELP WATCHDOG Timer bit[6] - SOC IC IRQs - Address Watch bit[5] - SOC IC IRQs - IC Timeout bit[4] - SOC IC IRQs - serror bit[3] - CORE to SDIO WATCHDOG bit[2] - PLL Unlock bit[1] - MEMss bus fault bit[0] - HSM fatal error Type: Write-Clear

5.6.24 ERRSRIS Register (Offset = E8h) [Reset = 00000000h]

ERRSRIS is shown in Table 5-47.

Return to the Summary Table.

M33 Secured Error RIS. Raw interrupt status for event. This bit is set to 1 when an event is received. when the corresponding bit in ICLR is set to 1, this bit will be cleared. Read 0 - CLR - Interrupt did not occur Read 1 - SET - Interrupt occurred

Table 5-47. ERRSRIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8-0	RIS	R	0h	Bits division to events: bit[8] - UDMA ERR IRQ bit[7] - CORE ELP WATCHDOG Timer bit[6] - SOC IC IRQs - Address Watch bit[5] - SOC IC IRQs - IC Timeout bit[4] - SOC IC IRQs - serror bit[3] - CORE to SDIO WATCHDOG bit[2] - PLL Unlock bit[1] - MEMss bus fault bit[0] - HSM fatal error

5.6.25 ERRSMIS Register (Offset = ECh) [Reset = 00000000h]

ERRSMIS is shown in Table 5-48.

Return to the Summary Table.

M33 Secured Error MIS. Mask interrupt status for event Read 0 - CLR - Interrupt did not occur Read 1 - SET - Interrupt occurred

Table 5-48. ERRSMIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8-0	MIS	R	0h	Bits division to events: bit[8] - UDMA ERR IRQ bit[7] - CORE ELP WATCHDOG Timer bit[6] - SOC IC IRQs - Address Watch bit[5] - SOC IC IRQs - IC Timeout bit[4] - SOC IC IRQs - serror bit[3] - CORE to SDIO WATCHDOG bit[2] - PLL Unlock bit[1] - MEMss bus fault bit[0] - HSM fatal error

5.6.26 GPT0EVTCTL1 Register (Offset = F0h) [Reset = 00000000h]

GPT0EVTCTL1 is shown in Table 5-49.

Return to the Summary Table.

GPTIMER0 Sync, Tick Enable and Fault Event MUXs Selectors. This register selects events to GPTIMER0.

Table 5-49. GPT0EVTCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Reserved
22-16	FAULT	R/W	0h	Selects fault MUX output to GPTIMER0 IRQ
15	RESERVED	R	0h	Reserved
14-8	TICKEN	R/W	0h	Selects tick enable MUX output to GPTIMER0 IRQ
7	RESERVED	R	0h	Reserved
6-0	SYNC	R/W	0h	Selects sync MUX output to GPTIMER0 IRQ

5.6.27 GPT1EVTCTL1 Register (Offset = F4h) [Reset = 00000000h]

GPT1EVTCTL1 is shown in Table 5-50.

Return to the Summary Table.

GPTIMER1 Sync, Tick Enable and Fault Event MUXs Selectors. This register selects events to GPTIMER1.

Table 5-50. GPT1EVTCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Reserved
22-16	FAULT	R/W	0h	Selects fault MUX output to GPTIMER0 IRQ
15	RESERVED	R	0h	Reserved
14-8	TICKEN	R/W	0h	Selects tick enable MUX output to GPTIMER0 IRQ
7	RESERVED	R	0h	Reserved
6-0	SYNC	R/W	0h	Selects sync MUX output to GPTIMER0 IRQ

5.6.28 ESMSTACST Register (Offset = 104h) [Reset = 00000000h]

ESMSTACST is shown in Table 5-51.

Return to the Summary Table.

Customer ESMs Status. status register , for each of the ESM (enable sequence monitor) what is the status (Done, violated, or None) Final ESM status for the entire ESM - ESM machine + magic value comparators

Table 5-51. ESMSTACST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9	ESM2VIO	R	0h	This field indicates that ESM1 is violated.
8	ESM2DONE	R	0h	This field indicates that ESM2 is done.
7-2	RESERVED	R	0h	Reserved
1	ESM1VIO	R	0h	This field indicates that ESM1 is violated.
0	ESM1DONE	R	0h	This field indicates that ESM1 is done.

5.6.29 MEMSSCFG Register (Offset = 10Ch) [Reset = 00000000h]

MEMSSCFG is shown in Table 5-52.

Return to the Summary Table.

MEMSS Configurations. Supported Memory configurations: Functional Modes: 0x0. Baseline 0x1. Extended M3 0x2. Extended throughput 0x3. Extended throughput + WIFI features 0x4. Extended Host Execution 0x5. Extended M33 Data Debug Modes (OCLA Memory): 0x6. Core debug (<M33 Data) 0x7. Core debug Extended throughput (<M33 Data <M3 Exec) 0x8. Core debug PHY only (<M3,M33 Data) 0x9. Host debug (<M3 Exec) 0xA. Host debug extended Host Execution 0xB. Host debug extended M33 Data

Table 5-52. MEMSSCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	MODE	R/W	0h	MEMSS mode of bank ownership

5.6.30 GPIOMIS0S Register (Offset = 138h) [Reset = 00000000h]

GPIOMIS0S is shown in Table 5-53.

Return to the Summary Table.

Secured Gpio MIS.

Table 5-53. GPIOMIS0S Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	31TO0	R	0h	32 LSBs of MIS. (45 Total)

5.6.31 GPIOMIS1S Register (Offset = 13Ch) [Reset = 00000000h]

GPIOMIS1S is shown in Table 5-54.

Return to the Summary Table.

Secured Gpio MIS.

Table 5-54. GPIOMIS1S Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	44TO32	R	0h	13 MSBs of MIS. (45 Total)

5.6.32 GPIOFNC0S Register (Offset = 140h) [Reset = 00000000h]

GPIOFNC0S is shown in Table 5-55.

Return to the Summary Table.

Secured GPIO Functional Mask. 0. Mask 1. Un-Mask

Table 5-55. GPIOFNC0S Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MASK31TO0	R/W	0h	32 LSBs of MASK. (45 Total)

5.6.33 GPIOFNC1S Register (Offset = 144h) [Reset = 00000000h]

GPIOFNC1S is shown in Table 5-56.

Return to the Summary Table.

Secured GPIO Functional Mask. 0. Mask 1. Un-Mask

Table 5-56. GPIOFNC1S Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	MASK44TO32	R/W	0h	13 MSBs of MASK. (45 Total)

5.6.34 ESM1VAL2ND Register (Offset = 14Ch) [Reset = 00000000h]

ESM1VAL2ND is shown in Table 5-57.

Return to the Summary Table.

ESM1 2nd Magic Value. This value is compared to hard coded value and unmask ESM only when value is matched. This additional compare allow additional protection on ESM and also allow vendor to unmask ESM only at the end of vendor secure boot (SBL) is completed

Table 5-57. ESM1VAL2ND Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	MGCVAL	R/W	0h	ESM 2nd magic value

5.6.35 ESM2VAL2ND Register (Offset = 150h) [Reset = 00000000h]

ESM2VAL2ND is shown in Table 5-58.

Return to the Summary Table.

ESM2 2nd Magic Value. This value is compared to hard coded value and unmask ESM only when value is matched. This additional compare allow additional protection on ESM and also allow vendor to unmask ESM only at the end of vendor secure boot (SBL) is completed

Table 5-58. ESM2VAL2ND Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	MGCVAL	R/W	0h	ESM 2nd magic value

5.6.36 ESM1STA2ND Register (Offset = 154h) [Reset = 00000000h]

ESM1STA2ND is shown in Table 5-59.

Return to the Summary Table.

ESM1 2nd Magic Value Status. ESM magic value match indication.

Table 5-59. ESM1STA2ND Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	FAULT	R	0h	ESM 2nd magic val fault (note: indicates fault before a write to the magic val register)
0	DONE	R	0h	ESM 2nd magic val match

5.6.37 ESM2STA2ND Register (Offset = 158h) [Reset = 00000000h]

ESM2STA2ND is shown in Table 5-60.

Return to the Summary Table.

ESM2 2nd Magic Value. ESM magic value match indication.

Table 5-60. ESM2STA2ND Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	FAULT	R	0h	ESM 2nd magic val fault (note: indicates fault before a write to the magic val register)
0	DONE	R	0h	ESM 2nd magic val match

5.6.38 FWCFGHOST Register (Offset = 15Ch) [Reset = 00000000h]

FWCFGHOST is shown in Table 5-61.

Return to the Summary Table.

HOST FW Bypass.

Table 5-61. FWCFGHOST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	BYPASS	R/W	1h	bypass the following module's firewall configuration: IOMUX_COMMON_SEL PRCM_AON_HOST PRCM_AON_COMMON SCRATCHPAD PLLSHARING SOC_IC SOC_AON_M33_S SOC_AON_M33_NS SOC_AAON_M33_S SOC_AAON_M33_NS RTC XIP_OSPI XIP_OSPI_INDAC XIP_GENERAL XIP_UDMA_SEC XIP_UDMA_NON_SEC OTFDE_REGION0-3 HOST_DMA_GENERAL_CFG

5.6.39 FWCFGDMA Register (Offset = 160h) [Reset = 00000000h]

FWCFGDMA is shown in Table 5-62.

Return to the Summary Table.

DMA FW BYPASS

Table 5-62. FWCFGDMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	BYPASS	R/W	1h	Bypass the firewall configuration for HOST_DMA module

5.6.40 FWCFGFPRPH Register (Offset = 164h) [Reset = 00000000h]

FWCFGFPRPH is shown in Table 5-63.

Return to the Summary Table.

Peripheral Firewall Bypass.

Table 5-63. FWCFGFPRPH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	BYPASS	R/W	1h	bypass the following module's firewall configuration: HIF HSM CORE_AON I2C0/1 SPI0/1 UART0/1 GPTIMER0/1 I2S PDM CAN ADC SDMMC SDIO

5.6.41 FWCFGM33 Register (Offset = 168h) [Reset = 00000000h]

FWCFGM33 is shown in Table 5-64.

Return to the Summary Table.

HOST MCU Firewall Bypass

Table 5-64. FWCFGM33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	BYPASS	R/W	1h	bypass the firewall configuration for HOST MCU module.

5.6.42 FWCFGMEMSS Register (Offset = 16Ch) [Reset = 00000000h]

FWCFGMEMSS is shown in Table 5-65.

Return to the Summary Table.

MEMSS Firewall Bypass

Table 5-65. FWCFGMEMSS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	BYPASS	R/W	1h	bypass the Firewall configuration for MEMSS module.

5.6.43 FWIOGENSEL Register (Offset = 170h) [Reset = 00000000h]

FWIOGENSEL is shown in Table 5-66.

Return to the Summary Table.

IOMUX General firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-66. FWIOGENSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.44 FWPRCMHOST Register (Offset = 174h) [Reset = 00000000h]

FWPRCMHOST is shown in Table 5-67.

Return to the Summary Table.

PRCM_HOST firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-67. FWPRCMHOST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed
1	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
0	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed

5.6.45 FWPRCMSPAD Register (Offset = 178h) [Reset = 00000000h]

FWPRCMSPAD is shown in Table 5-68.

Return to the Summary Table.

M33 SCRATCHPAD firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-68. FWPRCMSPAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.46 FWPRCMCMN Register (Offset = 17Ch) [Reset = 00000000h]

FWPRCMCMN is shown in Table 5-69.

Return to the Summary Table.

PRCM_COMMON firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-69. FWPRCMCMN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	CORENSRD	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
4	CORENSWR	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
3	M33NSRD	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed
2	M33NSWR	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed
1	M33SRD	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33SWR	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed

5.6.47 FWCKM Register (Offset = 180h) [Reset = 00000000h]

FWCKM is shown in Table 5-70.

Return to the Summary Table.

CKM firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-70. FWCKM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.48 FWSOCIC Register (Offset = 184h) [Reset = 00000000h]

FWSOCIC is shown in Table 5-71.

Return to the Summary Table.

SOC_IC firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-71. FWSOCIC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	CORENSRD	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
4	CORENSWR	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
3	M33SRD	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
2	M33SWR	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
1	M33NSRD	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed
0	M33NSWR	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.49 FWAONM33S Register (Offset = 188h) [Reset = 00000000h]

FWAONM33S is shown in Table 5-72.

Return to the Summary Table.

AON_M33_S firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-72. FWAONM33S Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.50 FWAONM33NS Register (Offset = 18Ch) [Reset = 00000000h]

FWAONM33NS is shown in Table 5-73.

Return to the Summary Table.

AON_M33_NS firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-73. FWAONM33NS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.51 FWAAONM33S Register (Offset = 190h) [Reset = 00000000h]

FWAAONM33S is shown in Table 5-74.

Return to the Summary Table.

AAON_M33_S firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-74. FWAAONM33S Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.52 FWAAONM33NS Register (Offset = 194h) [Reset = 00000000h]

FWAAONM33NS is shown in Table 5-75.

Return to the Summary Table.

AAON_M33_NS firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-75. FWAAONM33NS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.53 FWCMNRTC Register (Offset = 198h) [Reset = 00000000h]

FWCMNRTC is shown in Table 5-76.

Return to the Summary Table.

RTC firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-76. FWCMNRTC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	CORENSRD	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
4	CORENSWR	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
3	M33SRD	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
2	M33SWR	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
1	M33NSRD	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed
0	M33NSWR	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.54 FWMEMSS0 Register (Offset = 19Ch) [Reset = 00000000h]

FWMEMSS0 is shown in Table 5-77.

Return to the Summary Table.

MEMSS region 0 firewall access permission for 3 controller id : 0 - M33 Non Secured (valid only in privilege mode) 1 - M33 Secured (valid only in privilege mode) 2 - Core (Non Secure) MEMSS address space: 0x41C00000 - 0x41CCFFFF for Memss the base address for security firewalls is 0x41c40000 (M33 Data Ram from global port access) max window size is 256Kb (M33D banks) + 10*32K (Flex) = 576Kb

Table 5-77. FWMEMSS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-16	LEN	R/W	0h	address base with 1K granularity : address base len for firewall is the offset from the region's base address indicated in the same region field describing the end of a firewall window that has a certain access rules (R/W Permission) for each controller-id MEMSS address space: 0x41C00000 - 0x41CCFFFF for Memss the base address for security firewalls is 0x41c40000 (M33 Data Ram from global port access) max window size is 576Kb example: worker base address: 0x41C40000 current address to access: 0x41C41514 region_base_address: 0x4 region_base_address_len: 0x2 --> (region_base_address + region_base_address_len) --> 0x4+0x2 -->0x6 0x41C41514 --> ((0x41C41514 - 0x41C40000) >> 10) -->0x5 0x4 <= 0x5 < 0x6 that address falls on the region window and therefor obeys to that region set of access rules
15-14	RESERVED	R	0h	Reserved
13-4	BASE	R/W	0h	address base with 1K granularity : address base for firewall is the the offset start address from a worker base address describing the beginning of a firewall window that has a certain access rules (R/W Permission) for each controller-id MEMSS address space: 0x41C00000 - 0x41CCFFFF for Memss the base address for security firewalls is 0x41c40000 (M33 Data Ram from global port access) max base value is 0x23F max window size is 576Kb example: worker base address: 0x41C40000 current address to access: 0x41C40504 region_base_address: 0x1 region_base_address_len: 0x1 0x41C40504 --> ((0x41C40504 - 0x41C40000) >> 10) --> 0x1 0x1(base) <= 0x1(current) < 0x1(base) +0x1(len) that address falls on the region window and therefor obeys to that region set of access rules
3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: (valid only in privilege mode) '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: (valid only in privilege mode) '0' - access not allowed '1' - access allowed

5.6.55 FWMEMSS1 Register (Offset = 1A0h) [Reset = 00000000h]

FWMEMSS1 is shown in Table 5-78.

Return to the Summary Table.

MEMSS region 1 firewall access permission for 3 controller id : 0 - M33 Non Secured (valid only in privilege mode) 1 - M33 Secured (valid only in privilege mode) 2 - Core (Non Secure) MEMSS address space: 0x41C00000 - 0x41CCFFFF for Memss the base address for security firewalls is 0x41c40000 (M33 Data Ram from global port access) max window size is 256Kb (M33D banks) + 10*32K (Flex) = 576Kb

Table 5-78. FWMEMSS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-16	LEN	R/W	0h	address base with 1K granularity : address base len for firewall is the offset from the region's base address indicated in the same region field describing the end of a firewall window that has a certain access rules (R/W Permission) for each controller-id MEMSS address space: 0x41C00000 - 0x41CCFFFF for Memss the base address for security firewalls is 0x41c40000 (M33 Data Ram from global port access) max window size is 576Kb example: worker base address: 0x41C40000 current address to access: 0x41C41514 region_base_address: 0x4 region_base_address_len: 0x2 --> (region_base_address + region_base_address_len) --> 0x4+0x2 -->0x6 0x41C41514 --> ((0x41C41514 - 0x41C40000) >> 10) -->0x5 0x4 <= 0x5 < 0x6 that address falls on the region window and therefor obeys to that region set of access rules
15-14	RESERVED	R	0h	Reserved
13-4	BASE	R/W	0h	address base with 1K granularity : address base for firewall is the the offset start address from a worker base address describing the beginning of a firewall window that has a certain access rules (R/W Permission) for each controller-id MEMSS address space: 0x41C00000 - 0x41DFFFFF for Memss the base address for security firewalls is 0x41c40000 (M33 Data Ram from global port access) max base value is 0x23F max window size is 576Kb example: worker base address: 0x41C40000 current address to access: 0x41C40504 region_base_address: 0x1 region_base_address_len: 0x1 0x41C40504 --> ((0x41C40504 - 0x41C40000) >> 10) --> 0x1 0x1(base) <= 0x1(current) < 0x1(base)+0x1(len) that address falls on the region window and therefor obeys to that region set of access rules
3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: (valid only in privilege mode) '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: (valid only in privilege mode) '0' - access not allowed '1' - access allowed

5.6.56 FWMEMSS2 Register (Offset = 1A4h) [Reset = 00000000h]

FWMEMSS2 is shown in Table 5-79.

Return to the Summary Table.

MEMSS region 2 firewall access permission for 3 controller id : 0 - M33 Non Secured (valid only in privilege mode) 1 - M33 Secured (valid only in privilege mode) 2 - Core (Non Secure) MEMSS address space: 0x41C00000 - 0x41CCFFFF for Memss the base address for security firewalls is 0x41c40000 (M33 Data Ram from global port access) max window size is 256Kb (M33D banks) + 10*32K (Flex) = 576Kb

Table 5-79. FWMEMSS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-16	LEN	R/W	0h	address base with 1K granularity : address base len for firewall is the offset from the region's base address indicated in the same region field describing the end of a firewall window that has a certain access rules (R/W Permission) for each controller-id MEMSS address space: 0x41C00000 - 0x41CCFFFF for Memss the base address for security firewalls is 0x41c40000 (M33 Data Ram from global port access) max window size is 576Kb example: worker base address: 0x41C40000 current address to access: 0x41C41514 region_base_address: 0x4 region_base_address_len: 0x2 --> (region_base_address + region_base_address_len) --> 0x4+0x2 -->0x6 0x41C41514 --> ((0x41C41514 - 0x41C40000) >> 10) -->0x5 0x4 <= 0x5 < 0x6 that address falls on the region window and therefor obeys to that region set of access rules
15-14	RESERVED	R	0h	Reserved
13-4	BASE	R/W	0h	address base with 1K granularity : address base for firewall is the the offset start address from a worker base address describing the beginning of a firewall window that has a certain access rules (R/W Permission) for each controller-id MEMSS address space: 0x41C00000 - 0x41DFFFFF for Memss the base address for security firewalls is 0x41c40000 (M33 Data Ram from global port access) max base value is 0x23F max window size is 576Kb example: worker base address: 0x41C40000 current address to access: 0x41C40504 region_base_address: 0x1 region_base_address_len: 0x1 0x41C40504 --> ((0x41C40504 - 0x41C40000) >> 10) --> 0x1 0x1(base) <= 0x1(current) < 0x1(base)+0x1(len) that address falls on the region window and therefor obeys to that region set of access rules
3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: (valid only in privilege mode) '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 non Secured: (valid only in privilege mode) '0' - access not allowed '1' - access allowed

5.6.57 FWHOSTAON Register (Offset = 1A8h) [Reset = 00000000h]

FWHOSTAON is shown in Table 5-80.

Return to the Summary Table.

HOST_AON_SLV firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-80. FWHOSTAON Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.58 FWHIF Register (Offset = 1B0h) [Reset = 00000000h]

FWHIF is shown in Table 5-81.

Return to the Summary Table.

HIF firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure) - Not in use , core always has access.

Table 5-81. FWHIF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.59 FWHOST0 Register (Offset = 1B4h) [Reset = 00000000h]

FWHOST0 is shown in Table 5-82.

Return to the Summary Table.

HOST MCU region 0 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-82. FWHOST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-16	LEN	R/W	0h	address base with 1K granularity : address base len for firewall is the offset from the region's base address indicated in the same region field describing the end of a firewall window that has a certain access rules (R/W Permission) for each controller-id HOST_MCU_REGION_0 address space: 0x20000000 - 0x2FFFFFFF HOST_MCU_REGION_0 base_len can range from: ##register base_len value## 0x0 - 0x7F for HOST_MCU_REGION_0 the base address for security firewalls is 0x23F80000 (HOST_MCU_REGION_0) max window size is 128Kb example: worker base address: 0x23F80000 current address to access: 0x23F81504 region_base_address: 0x4 region_base_address_len: 0x2 --> (region_base_address + region_base_address_len) --> 0x4+0x2 -->0x6 0x23F81504 --> ((0x23F81504 - 0x23F80000) >> 10) -->0x4 0x4 <= 0x5 < 0x6 that address falls on the region window and therefor obeys to that region set of access rules
15	RESERVED	R	0h	Reserved
14-4	BASE	R/W	0h	address base with 1K granularity : address base for firewall is the the offset start address from a worker base address describing the beginning of a firewall window that has a certain access rules (R/W Permission) for each controller-id HOST_MCU address space: 0x00000000 - 0x2FFFFFFF / 0x41900000 - 0x4190FFFF HOST_MCU_REGION_0 is assigned to TCM DATA RAM HOST_MCU_REGION_0 base address can range from: ##register base value## 0x0 - 0x27F ##absolute equivalent value## 0x23F800000 - 0x2401FC00 for HOST_MCU_REGION_0 the base address for security firewalls is 0x23F80000 (M33 TCM Data RAM) max window size is 128Kb example: worker base address: 0x23F80000 current address to access: 0x23F80504 region_base_address: 0x1 region_base_address_len: 0x1 0x23F80504 --> ((0x23F80504 - 0x23F800000) >> 10) --> 0x1 0x1(base) <= 0x1(current) < 0x1(base)+0x1(len) that address falls on the region window and therefor obeys to that region set of access rules
3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.60 FWHOST1 Register (Offset = 1B8h) [Reset = 00000000h]

FWHOST1 is shown in Table 5-83.

Return to the Summary Table.

HOST MCU region 1 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-83. FWHOST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-16	LEN	R/W	0h	address base with 1K granularity : address base len for firewall is the offset from the region's base address indicated in the same region field describing the end of a firewall window that has a certain access rules (R/W Permission) for each controller-id HOST_MCU_REGION_0 address space: 0x20000000 - 0x2FFFFFFF HOST_MCU_REGION_0 base_len can range from: ##register base_len value## 0x0 - 0x7F for HOST_MCU_REGION_0 the base address for security firewalls is 0x23F80000 (HOST_MCU_REGION_1) max window size is 128Kb example: worker base address: 0x23F80000 current address to access: 0x23F81504 region_base_address: 0x4 region_base_address_len: 0x2 --> (region_base_address + region_base_address_len) --> 0x4+0x2 -->0x6 0x23F81504 --> ((0x23F81504 - 0x23F80000) >> 10) -->0x4 0x4 <= 0x5 < 0x6 that address falls on the region window and therefor obeys to that region set of access rules
15	RESERVED	R	0h	Reserved
14-4	BASE	R/W	0h	address base with 1K granularity : address base for firewall is the the offset start address from a worker base address describing the beginning of a firewall window that has a certain access rules (R/W Permission) for each controller-id HOST_MCU address space: 0x00000000 - 0x2FFFFFFF / 0x41900000 - 0x4190FFFF HOST_MCU_REGION_1 is assigned to TCM DATA RAM HOST_MCU_REGION_1 base address can range from: ##register base value## 0x0 - 0x27F ##absolute equivalent value## 0x23F800000 - 0x2401FC00 for HOST_MCU_REGION_0 the base address for security firewalls is 0x23F80000 (M33 TCM Data RAM) max window size is 128Kb example: worker base address: 0x23F80000 current address to access: 0x23F80504 region_base_address: 0x1 region_base_address_len: 0x1 0x23F80504 --> ((0x23F80504 - 0x23F800000) >> 10) --> 0x1 0x1(base) <= 0x1(current) < 0x1(base)+0x1(len) that address falls on the region window and therefor obeys to that region set of access rules
3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.61 FWHOST2 Register (Offset = 1BCh) [Reset = 00000000h]

FWHOST2 is shown in Table 5-84.

Return to the Summary Table.

HOST MCU region 2 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-84. FWHOST2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-16	LEN	R/W	0h	address base with 1K granularity : address base len for firewall is the offset from the region's base address indicated in the same region field describing the end of a firewall window that has a certain access rules (R/W Permission) for each controller-id HOST_MCU_REGION_2 address space: 0x20000000 - 0x2FFFFFFF HOST_MCU_REGION_2 base_len can range from: ##register base_len value## 0x0 - 0x240 for HOST_MCU_REGION_0 the base address for security firewalls is 0x2BF00000 (HOST_MCU_REGION_2) max window size is 576Kb example: worker base address: 0x2BF00000 current address to access: 0x2BF01504 region_base_address: 0x4 region_base_address_len: 0x2 --> (region_base_address + region_base_address_len) --> 0x4+0x2 -->0x6 0x2BF01504 --> ((0x2BF01504 - 0x2BF00000) >> 10) -->0x4 0x4 <= 0x5 < 0x6 that address falls on the region window and therefor obeys to that region set of access rules
15	RESERVED	R	0h	Reserved
14-4	BASE	R/W	0h	address base with 1K granularity : address base for firewall is the the offset start address from a worker base address describing the beginning of a firewall window that has a certain access rules (R/W Permission) for each controller-id HOST_MCU address space: 0x00000000 - 0x2FFFFFFF / 0x41900000 - 0x4190FFFF HOST_MCU_REGION_2 is assigned to M33 DATA RAM HOST_MCU_REGION_2 base address can range from: ##register base value## 0x0 - 0x63F ##absolute equivalent value## 0x2BF00000 - 0x2C08FC00 for HOST_MCU_REGION_2 the base address for security firewalls is 0x2BF00000 (M33 Data RAM) max window size is 576Kb (depending on the MEMSS mode) example: worker base address: 0x2BF000000 current address to access: 0x2BF00504 region_base_address: 0x1 region_base_address_len: 0x1 0x2BF00504 --> ((0x2BF00504 - 0x2BF000000) >> 10) --> 0x1 0x1(base) <= 0x1(current) < 0x1(base)+0x1(len) that address falls on the region window and therefor obeys to that region set of access rules
3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.62 FWHOST3 Register (Offset = 1C0h) [Reset = 00000000h]

FWHOST3 is shown in Table 5-85.

Return to the Summary Table.

HOST MCU region 3 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-85. FWHOST3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-16	LEN	R/W	0h	address base with 1K granularity : address base len for firewall is the offset from the region's base address indicated in the same region field describing the end of a firewall window that has a certain access rules (R/W Permission) for each controller-id HOST_MCU_REGION_2 address space: 0x20000000 - 0x2FFFFFFF HOST_MCU_REGION_2 base_len can range from: ##register base_len value## 0x0 - 0x240 for HOST_MCU_REGION_0 the base address for security firewalls is 0x2BF00000 (HOST_MCU_REGION_2) max window size is 576Kb example: worker base address: 0x2BF00000 current address to access: 0x2BF01504 region_base_address: 0x4 region_base_address_len: 0x2 --> (region_base_address + region_base_address_len) --> 0x4+0x2 -->0x6 0x2BF01504 --> ((0x2BF01504 - 0x2BF00000) >> 10) -->0x4 0x4 <= 0x5 < 0x6 that address falls on the region window and therefor obeys to that region set of access rules
15	RESERVED	R	0h	Reserved
14-4	BASE	R/W	0h	address base with 1K granularity : address base for firewall is the the offset start address from a worker base address describing the beginning of a firewall window that has a certain access rules (R/W Permission) for each controller-id HOST_MCU address space: 0x00000000 - 0x2FFFFFFF / 0x41900000 - 0x4190FFFF HOST_MCU_REGION_3 is assigned to M33 DATA RAM HOST_MCU_REGION_3 base address can range from: ##register base value## 0x0 - 0x63F ##absolute equivalent value## 0x2BF00000 - 0x2C08FC00 for HOST_MCU_REGION_2 the base address for security firewalls is 0x2BF00000 (M33 Data RAM) max window size is 576Kb (depending on the MEMSS mode) example: worker base address: 0x2BF000000 current address to access: 0x2BF00504 region_base_address: 0x1 region_base_address_len: 0x1 0x2BF00504 --> ((0x2BF00504 - 0x2BF000000) >> 10) --> 0x1 0x1(base) <= 0x1(current) < 0x1(base)+0x1(len) that address falls on the region window and therefor obeys to that region set of access rules
3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.63 FWHOST4 Register (Offset = 1C4h) [Reset = 00000000h]

FWHOST4 is shown in Table 5-86.

Return to the Summary Table.

access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-86. FWHOST4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26	BASESEL	R/W	0h	Base select for Reserved region defaulted to M33 TCM Data RAM (base_sel = 0): this select bit will assign this region to either TCM Data (base_sel = 0) ##register base value## 0x0 - 0x80 ##absolute equivalent value## 0x200000000 - 0x20001FFFF or Data RAM (base_sel = 1) ##register base value## 0x0 - 0x63F ##absolute equivalent value## 0x2BF00000 - 0x2C08FC00 for HOST_MCU_REGION_4 with base_sel = 0 the base address for security firewalls is 0x23F80000 (M33 TCM Data RAM) max window size is 128Kb (depending on the MEMSS mode) for HOST_MCU_REGION_4 with base_sel = 1 the base address for security firewalls is 0x2BF00000 (M33 Data RAM) max window size is 576Kb (depending on the MEMSS mode) example: worker base address: 0x2BF00000 current address to access: 0x2BF00504 region_base_address: 0x1 region_base_address_len: 0x1 0x2BF00504 --> ((0x2BF00504 - 0x2BF00000) >> 10) --> 0x1 0x1(base) <= 0x1(current) < 0x1(base)+0x1(len) that address falls on the region window and therefor obeys to that region set of access rules
25-16	LEN	R/W	0h	address base len for firewall is the offset from the region's base address indicated in the same region field describing the end of a firewall window that has a certain access rules (R/W Permission) for each controller-id HOST_MCU_REGION_4 address space: 0x20000000 - 0x2FFFFFFF HOST_MCU_REGION_4 base_len can range from: base_sel = 0 ##register base_len value## 0x0 - 0x7F base_sel = 0 --> HOST_MCU_REGION_4 the base address for security firewalls is 0x23F80000 (TCM M33 Data RAM) max window size is 128Kb ################## base_sel = 1 ##register base_len value## 0x0 - 0x240 base_sel = 1 --> HOST_MCU_REGION_4 the base address for security firewalls is 0x2BF00000 (M33 Data RAM) max window size is 576Kb ################## example: worker base address: 0x23F80000 current address to access: 0x23F81504 region_base_address: 0x4 region_base_address_len: 0x2 --> (region_base_address + region_base_address_len) --> 0x4+0x2 -->0x6 0x23F81504 --> ((0x23F81504 - 0x23F80000) >> 10) -->0x4 0x4 <= 0x5 < 0x6 that address falls on the region window and therefor obeys to that region set of access rules
15	RESERVED	R	0h	Reserved

Table 5-86. FWHOST4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-4	BASE	R/W	0h	address base with 1K granularity : address base for firewall is the the offset start address from a worker base address describing the beginning of a firewall window that has a certain access rules (R/W Permission) for each controller-id HOST_MCU address space: 0x00000000 - 0x2FFFFFFF / 0x41900000 - 0x4190FFFF HOST_MCU_REGION_4 is assigned to TCM DATA RAM (base_sel = 0) or M33 Data Ram (base_sel = 1) HOST_MCU_REGION_4 base address can range from: (base_sel = 0) ##register base value## 0x0 - 0x27F ##absolute equivalent value## 0x23F80000 - 0x2401FC00 for HOST_MCU_REGION_4 the base address for security firewalls is 0x23F80000 (TCM Data RAM) max window size is 128Kb ################## (base_sel = 1) ##register base value## 0x0 - 0x63F ##absolute equivalent value## 0x2BF000000 - 0x2C08FC00 for HOST_MCU_REGION_4 the base address for security firewalls is 0x2BF00000 (M33 Data RAM) max window size is 576Kb (depending on the MEMSS mode) example: worker base address: 0x2BF000000 current address to access: 0x2BF00504 region_base_address: 0x1 region_base_address_len: 0x1 0x2BF00504 --> ((0x2BF00504 - 0x2BF00000) >> 10) --> 0x1 0x1(base) <= 0x1(current) < 0x1(base)+0x1(len) that address falls on the region window and therefor obeys to that region set of access rules
3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.64 FWHOST5 Register (Offset = 1C8h) [Reset = 00000000h]

FWHOST5 is shown in Table 5-87.

Return to the Summary Table.

HOST MCU region 5 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-87. FWHOST5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26	BASESEL	R/W	0h	Base select for Reserved region defaulted to M33 TCM Data RAM (base_sel = 0): this select bit will assign this region to either TCM Data (base_sel = 0) ##register base value## 0x0 - 0x80 ##absolute equivalent value## 0x200000000 - 0x20001FFFF or Data RAM (base_sel = 1) ##register base value## 0x0 - 0x63F ##absolute equivalent value## 0x2BF00000 - 0x2C08FC00 for HOST_MCU_REGION_4 with base_sel = 0 the base address for security firewalls is 0x23F80000 (M33 TCM Data RAM) max window size is 128Kb (depending on the MEMSS mode) for HOST_MCU_REGION_4 with base_sel = 1 the base address for security firewalls is 0x2BF00000 (M33 Data RAM) max window size is 576Kb (depending on the MEMSS mode) example: worker base address: 0x2BF00000 current address to access: 0x2BF00504 region_base_address: 0x1 region_base_address_len: 0x1 0x2BF00504 --> ((0x2BF00504 - 0x2BF00000) >> 10) --> 0x1 0x1(base) <= 0x1(current) < 0x1(base)+0x1(len) that address falls on the region window and therefor obeys to that region set of access rules
25-16	LEN	R/W	0h	address base len for firewall is the offset from the region's base address indicated in the same region field describing the end of a firewall window that has a certain access rules (R/W Permission) for each controller-id HOST_MCU_REGION_4 address space: 0x20000000 - 0x2FFFFFFF HOST_MCU_REGION_4 base_len can range from: base_sel = 0 ##register base_len value## 0x0 - 0x7F base_sel = 0 --> HOST_MCU_REGION_4 the base address for security firewalls is 0x23F80000 (TCM M33 Data RAM) max window size is 128Kb ################## base_sel = 1 ##register base_len value## 0x0 - 0x240 base_sel = 1 --> HOST_MCU_REGION_4 the base address for security firewalls is 0x2BF00000 (M33 Data RAM) max window size is 576Kb ################## example: worker base address: 0x23F80000 current address to access: 0x23F81504 region_base_address: 0x4 region_base_address_len: 0x2 --> (region_base_address + region_base_address_len) --> 0x4+0x2 -->0x6 0x23F81504 --> ((0x23F81504 - 0x23F80000) >> 10) -->0x4 0x4 <= 0x5 < 0x6 that address falls on the region window and therefor obeys to that region set of access rules
15	RESERVED	R	0h	Reserved

Table 5-87. FWHOST5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-4	BASE	R/W	0h	address base with 1K granularity : address base for firewall is the the offset start address from a worker base address describing the beginning of a firewall window that has a certain access rules (R/W Permission) for each controller-id HOST_MCU address space: 0x00000000 - 0x2FFFFFFF / 0x41900000 - 0x4190FFFF HOST_MCU_REGION_4 is assigned to TCM DATA RAM (base_sel = 0) or M33 Data Ram (base_sel = 1) HOST_MCU_REGION_4 base address can range from: (base_sel = 0) ##register base value## 0x0 - 0x27F ##absolute equivalent value## 0x23F80000 - 0x2401FC00 for HOST_MCU_REGION_4 the base address for security firewalls is 0x23F80000 (TCM Data RAM) max window size is 128Kb ################## (base_sel = 1) ##register base value## 0x0 - 0x63F ##absolute equivalent value## 0x2BF000000 - 0x2C08FC00 for HOST_MCU_REGION_4 the base address for security firewalls is 0x2BF00000 (M33 Data RAM) max window size is 576Kb (depending on the MEMSS mode) example: worker base address: 0x2BF000000 current address to access: 0x2BF00504 region_base_address: 0x1 region_base_address_len: 0x1 0x2BF00504 --> ((0x2BF00504 - 0x2BF00000) >> 10) --> 0x1 0x1(base) <= 0x1(current) < 0x1(base)+0x1(len) that address falls on the region window and therefor obeys to that region set of access rules
3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.65 FWHOST6 Register (Offset = 1CCh) [Reset = 00000000h]

FWHOST6 is shown in Table 5-88.

Return to the Summary Table.

HOST MCU region 6 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-88. FWHOST6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26	BASESEL	R/W	1h	Base select for Reserved region defaulted to M33 TCM Data RAM (base_sel = 0): this select bit will assign this region to either TCM Data (base_sel = 0) ##register base value## 0x0 - 0x80 ##absolute equivalent value## 0x200000000 - 0x20001FFFF or Data RAM (base_sel = 1) ##register base value## 0x0 - 0x63F ##absolute equivalent value## 0x2BF00000 - 0x2C08FC00 for HOST_MCU_REGION_4 with base_sel = 0 the base address for security firewalls is 0x23F80000 (M33 TCM Data RAM) max window size is 128Kb (depending on the MEMSS mode) for HOST_MCU_REGION_4 with base_sel = 1 the base address for security firewalls is 0x2BF00000 (M33 Data RAM) max window size is 576Kb (depending on the MEMSS mode) example: worker base address: 0x2BF00000 current address to access: 0x2BF00504 region_base_address: 0x1 region_base_address_len: 0x1 0x2BF00504 --> ((0x2BF00504 - 0x2BF00000) >> 10) --> 0x1 0x1(base) <= 0x1(current) < 0x1(base)+0x1(len) that address falls on the region window and therefor obeys to that region set of access rules
25-16	LEN	R/W	0h	address base len for firewall is the offset from the region's base address indicated in the same region field describing the end of a firewall window that has a certain access rules (R/W Permission) for each controller-id HOST_MCU_REGION_4 address space: 0x20000000 - 0x2FFFFFFF HOST_MCU_REGION_4 base_len can range from: base_sel = 0 ##register base_len value## 0x0 - 0x7F base_sel = 0 --> HOST_MCU_REGION_4 the base address for security firewalls is 0x23F80000 (TCM M33 Data RAM) max window size is 128Kb ################## base_sel = 1 ##register base_len value## 0x0 - 0x240 base_sel = 1 --> HOST_MCU_REGION_4 the base address for security firewalls is 0x2BF00000 (M33 Data RAM) max window size is 576Kb ################## example: worker base address: 0x23F80000 current address to access: 0x23F81504 region_base_address: 0x4 region_base_address_len: 0x2 --> (region_base_address + region_base_address_len) --> 0x4+0x2 -->0x6 0x23F81504 --> ((0x23F81504 - 0x23F80000) >> 10) -->0x4 0x4 <= 0x5 < 0x6 that address falls on the region window and therefor obeys to that region set of access rules
15	RESERVED	R	0h	Reserved

Table 5-88. FWHOST6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-4	BASE	R/W	0h	address base with 1K granularity : address base for firewall is the the offset start address from a worker base address describing the beginning of a firewall window that has a certain access rules (R/W Permission) for each controller-id HOST_MCU address space: 0x00000000 - 0x2FFFFFFF / 0x41900000 - 0x4190FFFF HOST_MCU_REGION_4 is assigned to TCM DATA RAM (base_sel = 0) or M33 Data Ram (base_sel = 1) HOST_MCU_REGION_4 base address can range from: (base_sel = 0) ##register base value## 0x0 - 0x27F ##absolute equivalent value## 0x23F80000 - 0x2401FC00 for HOST_MCU_REGION_4 the base address for security firewalls is 0x23F80000 (TCM Data RAM) max window size is 128Kb ################### (base_sel = 1) ##register base value## 0x0 - 0x63F ##absolute equivalent value## 0x2BF000000 - 0x2C08FC00 for HOST_MCU_REGION_4 the base address for security firewalls is 0x2BF00000 (M33 Data RAM) max window size is 576Kb (depending on the MEMSS mode) example: worker base address: 0x2BF000000 current address to access: 0x2BF00504 region_base_address: 0x1 region_base_address_len: 0x1 0x2BF00504 --> ((0x2BF00504 - 0x2BF00000) >> 10) --> 0x1 0x1(base) <= 0x1(current) < 0x1(base)+0x1(len) that address falls on the region window and therefor obeys to that region set of access rules
3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.66 FWHOST7 Register (Offset = 1D0h) [Reset = 00000000h]

FWHOST7 is shown in Table 5-89.

Return to the Summary Table.

HOST MCU region 7 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-89. FWHOST7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26	BASESEL	R/W	01h	Base select for Reserved region defaulted to M33 TCM Data RAM (base_sel = 0): this select bit will assign this region to either TCM Data (base_sel = 0) ##register base value## 0x0 - 0x80 ##absolute equivalent value## 0x200000000 - 0x20001FFFF or Data RAM (base_sel = 1) ##register base value## 0x0 - 0x63F ##absolute equivalent value## 0x2BF00000 - 0x2C08FC00 for HOST_MCU_REGION_4 with base_sel = 0 the base address for security firewalls is 0x23F80000 (M33 TCM Data RAM) max window size is 128Kb (depending on the MEMSS mode) for HOST_MCU_REGION_4 with base_sel = 1 the base address for security firewalls is 0x2BF00000 (M33 Data RAM) max window size is 576Kb (depending on the MEMSS mode) example: worker base address: 0x2BF00000 current address to access: 0x2BF00504 region_base_address: 0x1 region_base_address_len: 0x1 0x2BF00504 --> ((0x2BF00504 - 0x2BF00000) >> 10) --> 0x1 0x1(base) <= 0x1(current) < 0x1(base)+0x1(len) that address falls on the region window and therefor obeys to that region set of access rules
25-16	LEN	R/W	0h	address base len for firewall is the offset from the region's base address indicated in the same region field describing the end of a firewall window that has a certain access rules (R/W Permission) for each controller-id HOST_MCU_REGION_4 address space: 0x20000000 - 0x2FFFFFFF HOST_MCU_REGION_4 base_len can range from: base_sel = 0 ##register base_len value## 0x0 - 0x7F base_sel = 0 --> HOST_MCU_REGION_4 the base address for security firewalls is 0x23F80000 (TCM M33 Data RAM) max window size is 128Kb ################## base_sel = 1 ##register base_len value## 0x0 - 0x240 base_sel = 1 --> HOST_MCU_REGION_4 the base address for security firewalls is 0x2BF00000 (M33 Data RAM) max window size is 576Kb ################## example: worker base address: 0x23F80000 current address to access: 0x23F81504 region_base_address: 0x4 region_base_address_len: 0x2 --> (region_base_address + region_base_address_len) --> 0x4+0x2 -->0x6 0x23F81504 --> ((0x23F81504 - 0x23F80000) >> 10) -->0x4 0x4 <= 0x5 < 0x6 that address falls on the region window and therefor obeys to that region set of access rules
15	RESERVED	R	0h	Reserved

Table 5-89. FWHOST7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-4	BASE	R/W	0h	address base with 1K granularity : address base for firewall is the the offset start address from a worker base address describing the beginning of a firewall window that has a certain access rules (R/W Permission) for each controller-id HOST_MCU address space: 0x00000000 - 0x2FFFFFFF / 0x41900000 - 0x4190FFFF HOST_MCU_REGION_4 is assigned to TCM DATA RAM (base_sel = 0) or M33 Data Ram (base_sel = 1) HOST_MCU_REGION_4 base address can range from: (base_sel = 0) ##register base value## 0x0 - 0x27F ##absolute equivalent value## 0x23F80000 - 0x2401FC00 for HOST_MCU_REGION_4 the base address for security firewalls is 0x23F80000 (TCM Data RAM) max window size is 128Kb ################## (base_sel = 1) ##register base value## 0x0 - 0x63F ##absolute equivalent value## 0x2BF000000 - 0x2C08FC00 for HOST_MCU_REGION_4 the base address for security firewalls is 0x2BF00000 (M33 Data RAM) max window size is 576Kb (depending on the MEMSS mode) example: worker base address: 0x2BF000000 current address to access: 0x2BF00504 region_base_address: 0x1 region_base_address_len: 0x1 0x2BF00504 --> ((0x2BF00504 - 0x2BF00000) >> 10) --> 0x1 0x1(base) <= 0x1(current) < 0x1(base)+0x1(len) that address falls on the region window and therefor obeys to that region set of access rules
3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.67 FWHOST8 Register (Offset = 1D4h) [Reset = 00000000h]

FWHOST8 is shown in Table 5-90.

Return to the Summary Table.

HOST MCU region 8 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-90. FWHOST8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.68 FWHOST9 Register (Offset = 1D8h) [Reset = 00000000h]

FWHOST9 is shown in Table 5-91.

Return to the Summary Table.

HOST MCU region 9 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-91. FWHOST9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.69 FWHOST10 Register (Offset = 1DCh) [Reset = 00000000h]

FWHOST10 is shown in Table 5-92.

Return to the Summary Table.

HOST MCU region 10 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-92. FWHOST10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.70 FWHOST11 Register (Offset = 1E0h) [Reset = 00000000h]

FWHOST11 is shown in Table 5-93.

Return to the Summary Table.

HOST MCU region 11 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-93. FWHOST11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.71 FWXIPOSPI Register (Offset = 1E4h) [Reset = 00000000h]

FWXIPOSPI is shown in Table 5-94.

Return to the Summary Table.

XIP_OSPI firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-94. FWXIPOSPI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.72 FWXIPINDAC Register (Offset = 1E8h) [Reset = 00000000h]

FWXIPINDAC is shown in Table 5-95.

Return to the Summary Table.

OSPI_INDAC firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-95. FWXIPINDAC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.73 FWXIPGEN Register (Offset = 1ECh) [Reset = 00000000h]

FWXIPGEN is shown in Table 5-96.

Return to the Summary Table.

XIP_GEN firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-96. FWXIPGEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.74 FWXIPUDMAS Register (Offset = 1F0h) [Reset = 00000000h]

FWXIPUDMAS is shown in Table 5-97.

Return to the Summary Table.

XIP_UDMA_SEC firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-97. FWXIPUDMAS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.75 FWXIPUDMANS Register (Offset = 1F4h) [Reset = 00000000h]

FWXIPUDMANS is shown in Table 5-98.

Return to the Summary Table.

UDMA_NONSEC firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-98. FWXIPUDMANS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.76 FWOTFDE0 Register (Offset = 1F8h) [Reset = 00000000h]

FWOTFDE0 is shown in Table 5-99.

Return to the Summary Table.

OTFDE_REGION0 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-99. FWOTFDE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.77 FWOTFDE1 Register (Offset = 1FCh) [Reset = 00000000h]

FWOTFDE1 is shown in Table 5-100.

Return to the Summary Table.

OTFDE_REGION1 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-100. FWOTFDE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.78 FWOTFDE2 Register (Offset = 200h) [Reset = 00000000h]

FWOTFDE2 is shown in Table 5-101.

Return to the Summary Table.

OTFDE_REGION2 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-101. FWOTFDE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.79 FWOTFDE3 Register (Offset = 204h) [Reset = 00000000h]

FWOTFDE3 is shown in Table 5-102.

Return to the Summary Table.

OTFDE_REGION3 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-102. FWOTFDE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.80 FWDMAGEN Register (Offset = 208h) [Reset = 00000000h]

FWDMAGEN is shown in Table 5-103.

Return to the Summary Table.

DMA_GEN firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-103. FWDMAGEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.81 FWDMA0 Register (Offset = 20Ch) [Reset = 00000000h]

FWDMA0 is shown in Table 5-104.

Return to the Summary Table.

DMA_CH_0 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-104. FWDMA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.82 FWDMA1 Register (Offset = 210h) [Reset = 00000000h]

FWDMA1 is shown in Table 5-105.

Return to the Summary Table.

DMA_CH_1 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-105. FWDMA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.83 FWDMA2 Register (Offset = 214h) [Reset = 00000000h]

FWDMA2 is shown in Table 5-106.

Return to the Summary Table.

DMA_CH_2 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-106. FWDMA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.84 FWDMA3 Register (Offset = 218h) [Reset = 00000000h]

FWDMA3 is shown in Table 5-107.

Return to the Summary Table.

DMA_CH_3 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-107. FWDMA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.85 FWDMA4 Register (Offset = 21Ch) [Reset = 00000000h]

FWDMA4 is shown in Table 5-108.

Return to the Summary Table.

DMA_CH_4 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-108. FWDMA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.86 FWDMA5 Register (Offset = 220h) [Reset = 00000000h]

FWDMA5 is shown in Table 5-109.

Return to the Summary Table.

DMA_CH_5 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-109. FWDMA5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.87 FWDMA6 Register (Offset = 224h) [Reset = 00000000h]

FWDMA6 is shown in Table 5-110.

Return to the Summary Table.

DMA_CH_6 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-110. FWDMA6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.88 FWDMA7 Register (Offset = 228h) [Reset = 00000000h]

FWDMA7 is shown in Table 5-111.

Return to the Summary Table.

DMA_CH_7 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-111. FWDMA7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.89 FWDMA8 Register (Offset = 22Ch) [Reset = 00000000h]

FWDMA8 is shown in Table 5-112.

Return to the Summary Table.

DMA_CH_8 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-112. FWDMA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.90 FWDMA9 Register (Offset = 230h) [Reset = 00000000h]

FWDMA9 is shown in Table 5-113.

Return to the Summary Table.

DMA_CH_9 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-113. FWDMA9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.91 FWDMA10 Register (Offset = 234h) [Reset = 00000000h]

FWDMA10 is shown in Table 5-114.

Return to the Summary Table.

DMA_CH_10 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-114. FWDMA10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.92 FWDMA11 Register (Offset = 238h) [Reset = 00000000h]

FWDMA11 is shown in Table 5-115.

Return to the Summary Table.

DMA_CH_11 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-115. FWDMA11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.93 FWHSMEIPNS Register (Offset = 23Ch) [Reset = 00000000h]

FWHSMEIPNS is shown in Table 5-116.

Return to the Summary Table.

HSM EIP NONSEC firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-116. FWHSMEIPNS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20-16	LEN	R/W	0h	address base with 1K granularity : address base len for firewall is the offset from the region's base address indicated in the same region field describing the end of a firewall window that has a certain access rules (R/W Permission) for each controller-id HSM address space: 0x41B00000 - 0x41B3FFFF HSM_EIP_REGS base_len can range from: ##register base_len value## 0x0 - 0xF for HSM the base address for security firewalls is 0x41B00000 (HSM_EIP_REGS) max window size is 16Kb example: worker base address: 0x41B00000 current address to access: 0x41B01504 region_base_address: 0x4 region_base_address_len: 0x2 --> (region_base_address + region_base_address_len) --> 0x4+0x2 -->0x6 0x41B01504 --> ((0x41B01504 - 0x41B00000) >> 10) -->0x4 0x4 <= 0x5 < 0x6 that address falls on the region window and therefor obeys to that region set of access rules
15-9	RESERVED	R	0h	Reserved
8-4	BASE	R/W	0h	address base with 1K granularity : address base for firewall is the the offset start address from a worker base address describing the beginning of a firewall window that has a certain access rules (R/W Permission) for each controller-id HSM address space: 0x41B00000 - 0x41B3FFFF HSM_EIP_REGS base address can range from: ##register base value## 0x0 - 0xF ##absolute equivalent value## 0x41B00000 - 0x41B03FFF for HSM the base address for security firewalls is 0x41B00000 (HSM_EIP_REGS) max window size is 16Kb example: worker base address: 0x41B00000 current address to access: 0x41B00504 region_base_address: 0x1 region_base_address_len: 0x1 0x41B00504 --> ((0x41B00504 - 0x41B00000) >> 10) --> 0x1 0x1(base) <= 0x1(current) < 0x1(base) +0x1(len) that address falls on the region window and therefor obeys to that region set of access rules
3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.94 FWHSMEIPS Register (Offset = 240h) [Reset = 00000000h]

FWHSMEIPS is shown in Table 5-117.

Return to the Summary Table.

HSM EIP SEC firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-117. FWHSMEIPS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20-16	LEN	R/W	0h	address base with 1K granularity : address base len for firewall is the offset from the region's base address indicated in the same region field describing the end of a firewall window that has a certain access rules (R/W Permission) for each controller-id HSM address space: 0x41B00000 - 0x41B3FFFF HSM_EIP_REGS base_len can range from: ##register base_len value## 0x0 - 0xF for HSM the base address for security firewalls is 0x41B00000 (HSM_EIP_REGS) max window size is 16Kb example: worker base address: 0x41B00000 current address to access: 0x41B01504 region_base_address: 0x4 region_base_address_len: 0x2 --> (region_base_address + region_base_address_len) --> 0x4+0x2 -->0x6 0x41B01504 --> ((0x41B01504 - 0x41B00000) >> 10) -->0x4 0x4 <= 0x5 < 0x6 that address falls on the region window and therefor obeys to that region set of access rules
15-9	RESERVED	R	0h	Reserved
8-4	BASE	R/W	0h	address base with 1K granularity : address base for firewall is the the offset start address from a worker base address describing the beginning of a firewall window that has a certain access rules (R/W Permission) for each controller-id HSM address space: 0x41B00000 - 0x41B3FFFF HSM_EIP_REGS base address can range from: ##register base value## 0x0 - ##absolute equivalent value## 0x41B00000 - 0x41B03FFF for HSM the base address for security firewalls is 0x41B00000 (HSM_EIP_REGS) max window size is 16Kb example: worker base address: 0x41B00000 current address to access: 0x41B00504 region_base_address: 0x1 region_base_address_len: 0x1 0x41B00504 --> ((0x41B00504 - 0x41B00000) >> 10) --> 0x1 0x1(base) <= 0x1(current) < 0x1(base) +0x1(len) that address falls on the region window and therefor obeys to that region set of access rules
3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.95 FWHSMWRAPNS Register (Offset = 244h) [Reset = 00000000h]

FWHSMWRAPNS is shown in Table 5-118.

Return to the Summary Table.

HSM Wrapper NONSEC firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-118. FWHSMWRAPNS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.96 FWHSMWRAPS Register (Offset = 248h) [Reset = 00000000h]

FWHSMWRAPS is shown in Table 5-119.

Return to the Summary Table.

HSM Wrapper SEC firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-119. FWHSMWRAPS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.97 FWHSMDBG Register (Offset = 24Ch) [Reset = 00000000h]

FWHSMDBG is shown in Table 5-120.

Return to the Summary Table.

HSM DEBUG firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-120. FWHSMDBG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.98 FWI2C0 Register (Offset = 250h) [Reset = 00000000h]

FWI2C0 is shown in Table 5-121.

Return to the Summary Table.

I2C0 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-121. FWI2C0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.99 FWI2C1 Register (Offset = 254h) [Reset = 00000000h]

FWI2C1 is shown in Table 5-122.

Return to the Summary Table.

I2C1 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-122. FWI2C1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.100 FWSPSPI0 Register (Offset = 258h) [Reset = 00000000h]

FWSPSPI0 is shown in Table 5-123.

Return to the Summary Table.

SPI0 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-123. FWSPSPI0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.101 FWSPSPI1 Register (Offset = 25Ch) [Reset = 00000000h]

FWSPSPI1 is shown in Table 5-124.

Return to the Summary Table.

SPI1 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-124. FWSPSPI1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.102 FWSPUART0 Register (Offset = 260h) [Reset = 00000000h]

FWSPUART0 is shown in Table 5-125.

Return to the Summary Table.

UART0 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-125. FWSPUART0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.103 FWSPUART1 Register (Offset = 264h) [Reset = 00000000h]

FWSPUART1 is shown in Table 5-126.

Return to the Summary Table.

UART1 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-126. FWSPUART1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.104 FWSPGPT0 Register (Offset = 268h) [Reset = 00000000h]

FWSPGPT0 is shown in Table 5-127.

Return to the Summary Table.

GPTIMER0 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-127. FWSPGPT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.105 FWSPGPT1 Register (Offset = 26Ch) [Reset = 00000000h]

FWSPGPT1 is shown in Table 5-128.

Return to the Summary Table.

GPTIMER1 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-128. FWSPGPT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.106 FWSPI2S Register (Offset = 270h) [Reset = 00000000h]

FWSPI2S is shown in Table 5-129.

Return to the Summary Table.

I2S firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-129. FWSPI2S Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.107 FWPDM Register (Offset = 274h) [Reset = 00000000h]

FWPDM is shown in Table 5-130.

Return to the Summary Table.

PDM firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-130. FWPDM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.108 FWSPCAN Register (Offset = 278h) [Reset = 00000000h]

FWSPCAN is shown in Table 5-131.

Return to the Summary Table.

CAN firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-131. FWSPCAN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.109 FWSPADC Register (Offset = 27Ch) [Reset = 00000000h]

FWSPADC is shown in Table 5-132.

Return to the Summary Table.

ADC firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-132. FWSPADC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.110 FWSPSDMMC Register (Offset = 280h) [Reset = 00000000h]

FWSPSDMMC is shown in Table 5-133.

Return to the Summary Table.

SDMMC firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-133. FWSPSDMMC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.111 FWSPSDIO Register (Offset = 284h) [Reset = 00000000h]

FWSPSDIO is shown in Table 5-134.

Return to the Summary Table.

SDIO firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-134. FWSPSDIO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.112 FWSPUART2 Register (Offset = 288h) [Reset = 00000000h]

FWSPUART2 is shown in Table 5-135.

Return to the Summary Table.

UART2 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-135. FWSPUART2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.113 UDMANSCTL Register (Offset = 28Ch) [Reset = 00000000h]

UDMANSCTL is shown in Table 5-136.

Return to the Summary Table.

uDMA Non-secured Channel Control.

Table 5-136. UDMANSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	ACCPER	R/W	0h	Access Permission. Define uDMA non-sec channel access permission to secured flash address: '0' - access not allowed '1' - access allowed

5.6.114 FWIOPAD0 Register (Offset = 290h) [Reset = 00000000h]

FWIOPAD0 is shown in Table 5-137.

Return to the Summary Table.

IOMUX_PAD_0 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-137. FWIOPAD0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.115 FWIOPAD1 Register (Offset = 294h) [Reset = 00000000h]

FWIOPAD1 is shown in Table 5-138.

Return to the Summary Table.

IOMUX_PAD_1 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-138. FWIOPAD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.116 FWIOPAD2 Register (Offset = 298h) [Reset = 00000000h]

FWIOPAD2 is shown in Table 5-139.

Return to the Summary Table.

IOMUX_PAD_2 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-139. FWIOPAD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.117 FWIOPAD3 Register (Offset = 29Ch) [Reset = 00000000h]

FWIOPAD3 is shown in Table 5-140.

Return to the Summary Table.

IOMUX_PAD_3 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-140. FWIOPAD3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.118 FWIOPAD4 Register (Offset = 2A0h) [Reset = 00000000h]

FWIOPAD4 is shown in Table 5-141.

Return to the Summary Table.

IOMUX_PAD_4 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-141. FWIOPAD4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.119 FWIOPAD5 Register (Offset = 2A4h) [Reset = 00000000h]

FWIOPAD5 is shown in Table 5-142.

Return to the Summary Table.

IOMUX_PAD_5 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-142. FWIOPAD5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.120 FWIOPAD6 Register (Offset = 2A8h) [Reset = 00000000h]

FWIOPAD6 is shown in Table 5-143.

Return to the Summary Table.

IOMUX_PAD_6 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-143. FWIOPAD6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.121 FWIOPAD7 Register (Offset = 2ACh) [Reset = 00000000h]

FWIOPAD7 is shown in Table 5-144.

Return to the Summary Table.

IOMUX_PAD_7 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-144. FWIOPAD7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.122 FWIOPAD8 Register (Offset = 2B0h) [Reset = 00000000h]

FWIOPAD8 is shown in Table 5-145.

Return to the Summary Table.

IOMUX_PAD_8 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-145. FWIOPAD8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.123 FWIOPAD9 Register (Offset = 2B4h) [Reset = 00000000h]

FWIOPAD9 is shown in Table 5-146.

Return to the Summary Table.

IOMUX_PAD_9 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-146. FWIOPAD9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.124 FWIOPAD10 Register (Offset = 2B8h) [Reset = 00000000h]

FWIOPAD10 is shown in Table 5-147.

Return to the Summary Table.

IOMUX_PAD_10 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-147. FWIOPAD10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.125 FWIOPAD11 Register (Offset = 2BCh) [Reset = 00000000h]

FWIOPAD11 is shown in Table 5-148.

Return to the Summary Table.

IOMUX_PAD_11 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-148. FWIOPAD11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.126 FWIOPAD12 Register (Offset = 2C0h) [Reset = 00000000h]

FWIOPAD12 is shown in Table 5-149.

Return to the Summary Table.

IOMUX_PAD_12 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-149. FWIOPAD12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.127 FWIOPAD13 Register (Offset = 2C4h) [Reset = 00000000h]

FWIOPAD13 is shown in Table 5-150.

Return to the Summary Table.

IOMUX_PAD_13 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-150. FWIOPAD13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.128 FWIOPAD14 Register (Offset = 2C8h) [Reset = 00000000h]

FWIOPAD14 is shown in Table 5-151.

Return to the Summary Table.

IOMUX_PAD_14 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-151. FWIOPAD14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.129 FWIOPAD15 Register (Offset = 2CCh) [Reset = 00000000h]

FWIOPAD15 is shown in Table 5-152.

Return to the Summary Table.

IOMUX_PAD_15 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-152. FWIOPAD15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.130 FWIOPAD16 Register (Offset = 2D0h) [Reset = 00000000h]

FWIOPAD16 is shown in Table 5-153.

Return to the Summary Table.

IOMUX_PAD_16 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-153. FWIOPAD16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.131 FWIOPAD17 Register (Offset = 2D4h) [Reset = 00000000h]

FWIOPAD17 is shown in Table 5-154.

Return to the Summary Table.

IOMUX_PAD_17 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-154. FWIOPAD17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.132 FWIOPAD18 Register (Offset = 2D8h) [Reset = 00000000h]

FWIOPAD18 is shown in Table 5-155.

Return to the Summary Table.

IOMUX_PAD_18 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-155. FWIOPAD18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.133 FWIOPAD19 Register (Offset = 2DCh) [Reset = 00000000h]

FWIOPAD19 is shown in Table 5-156.

Return to the Summary Table.

IOMUX_PAD_19 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-156. FWIOPAD19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.134 FWIOPAD20 Register (Offset = 2E0h) [Reset = 00000000h]

FWIOPAD20 is shown in Table 5-157.

Return to the Summary Table.

IOMUX_PAD_20 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-157. FWIOPAD20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.135 FWIOPAD21 Register (Offset = 2E4h) [Reset = 00000000h]

FWIOPAD21 is shown in Table 5-158.

Return to the Summary Table.

IOMUX_PAD_21 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-158. FWIOPAD21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.136 FWIOPAD22 Register (Offset = 2E8h) [Reset = 00000000h]

FWIOPAD22 is shown in Table 5-159.

Return to the Summary Table.

IOMUX_PAD_22 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-159. FWIOPAD22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.137 FWIOPAD23 Register (Offset = 2ECh) [Reset = 00000000h]

FWIOPAD23 is shown in Table 5-160.

Return to the Summary Table.

IOMUX_PAD_23 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-160. FWIOPAD23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.138 FWIOPAD24 Register (Offset = 2F0h) [Reset = 00000000h]

FWIOPAD24 is shown in Table 5-161.

Return to the Summary Table.

IOMUX_PAD_24 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-161. FWIOPAD24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.139 FWIOPAD25 Register (Offset = 2F4h) [Reset = 00000000h]

FWIOPAD25 is shown in Table 5-162.

Return to the Summary Table.

IOMUX_PAD_25 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-162. FWIOPAD25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.140 FWIOPAD26 Register (Offset = 2F8h) [Reset = 00000000h]

FWIOPAD26 is shown in Table 5-163.

Return to the Summary Table.

IOMUX_PAD_26 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-163. FWIOPAD26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.141 FWIOPAD27 Register (Offset = 2FCh) [Reset = 00000000h]

FWIOPAD27 is shown in Table 5-164.

Return to the Summary Table.

IOMUX_PAD_27 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-164. FWIOPAD27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.142 FWIOPAD28 Register (Offset = 300h) [Reset = 00000000h]

FWIOPAD28 is shown in Table 5-165.

Return to the Summary Table.

IOMUX_PAD_28 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-165. FWIOPAD28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.143 FWIOPAD29 Register (Offset = 304h) [Reset = 00000000h]

FWIOPAD29 is shown in Table 5-166.

Return to the Summary Table.

IOMUX_PAD_29 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-166. FWIOPAD29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.144 FWIOPAD30 Register (Offset = 308h) [Reset = 00000000h]

FWIOPAD30 is shown in Table 5-167.

Return to the Summary Table.

IOMUX_PAD_30 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-167. FWIOPAD30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.145 FWIOPAD31 Register (Offset = 30Ch) [Reset = 00000000h]

FWIOPAD31 is shown in Table 5-168.

Return to the Summary Table.

IOMUX_PAD_31 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-168. FWIOPAD31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.146 FWIOPAD32 Register (Offset = 310h) [Reset = 00000000h]

FWIOPAD32 is shown in Table 5-169.

Return to the Summary Table.

IOMUX_PAD_32 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-169. FWIOPAD32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.147 FWIOPAD33 Register (Offset = 314h) [Reset = 00000000h]

FWIOPAD33 is shown in Table 5-170.

Return to the Summary Table.

IOMUX_PAD_33 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-170. FWIOPAD33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.148 FWIOPAD34 Register (Offset = 318h) [Reset = 00000000h]

FWIOPAD34 is shown in Table 5-171.

Return to the Summary Table.

IOMUX_PAD_34 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-171. FWIOPAD34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.149 FWIOPAD35 Register (Offset = 31Ch) [Reset = 00000000h]

FWIOPAD35 is shown in Table 5-172.

Return to the Summary Table.

IOMUX_PAD_35 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-172. FWIOPAD35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.150 FWIOPAD36 Register (Offset = 320h) [Reset = 00000000h]

FWIOPAD36 is shown in Table 5-173.

Return to the Summary Table.

IOMUX_PAD_36 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-173. FWIOPAD36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.151 FWIOPAD37 Register (Offset = 324h) [Reset = 00000000h]

FWIOPAD37 is shown in Table 5-174.

Return to the Summary Table.

IOMUX_PAD_37 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-174. FWIOPAD37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.152 FWIOPAD38 Register (Offset = 328h) [Reset = 00000000h]

FWIOPAD38 is shown in Table 5-175.

Return to the Summary Table.

IOMUX_PAD_38 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-175. FWIOPAD38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.153 FWIOPAD39 Register (Offset = 32Ch) [Reset = 00000000h]

FWIOPAD39 is shown in Table 5-176.

Return to the Summary Table.

IOMUX_PAD_39 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-176. FWIOPAD39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.154 FWIOPAD40 Register (Offset = 330h) [Reset = 00000000h]

FWIOPAD40 is shown in Table 5-177.

Return to the Summary Table.

IOMUX_PAD_40 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-177. FWIOPAD40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.155 FWIOPAD41 Register (Offset = 334h) [Reset = 00000000h]

FWIOPAD41 is shown in Table 5-178.

Return to the Summary Table.

IOMUX_PAD_41 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-178. FWIOPAD41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.156 FWIOPAD42 Register (Offset = 338h) [Reset = 00000000h]

FWIOPAD42 is shown in Table 5-179.

Return to the Summary Table.

IOMUX_PAD_42 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-179. FWIOPAD42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.157 FWIOPAD43 Register (Offset = 33Ch) [Reset = 00000000h]

FWIOPAD43 is shown in Table 5-180.

Return to the Summary Table.

IOMUX_PAD_43 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-180. FWIOPAD43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.158 FWIOPAD44 Register (Offset = 340h) [Reset = 00000000h]

FWIOPAD44 is shown in Table 5-181.

Return to the Summary Table.

IOMUX_PAD_44 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-181. FWIOPAD44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.159 FWIOPAD45 Register (Offset = 344h) [Reset = 00000000h]

FWIOPAD45 is shown in Table 5-182.

Return to the Summary Table.

IOMUX_PAD_45 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-182. FWIOPAD45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.160 FWIOPAD46 Register (Offset = 348h) [Reset = 00000000h]

FWIOPAD46 is shown in Table 5-183.

Return to the Summary Table.

IOMUX_PAD_46 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-183. FWIOPAD46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.161 FWIOPAD47 Register (Offset = 34Ch) [Reset = 00000000h]

FWIOPAD47 is shown in Table 5-184.

Return to the Summary Table.

IOMUX_PAD_47 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-184. FWIOPAD47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.162 FWIOPAD48 Register (Offset = 350h) [Reset = 00000000h]

FWIOPAD48 is shown in Table 5-185.

Return to the Summary Table.

IOMUX_PAD_48 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-185. FWIOPAD48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.163 FWDMA12 Register (Offset = 354h) [Reset = 00000000h]

FWDMA12 is shown in Table 5-186.

Return to the Summary Table.

DMA_CH_12 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-186. FWDMA12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.164 FWDMA13 Register (Offset = 358h) [Reset = 00000000h]

FWDMA13 is shown in Table 5-187.

Return to the Summary Table.

DMA_CH_13 firewall access permission for 3 controller id : 0 - M33 Non Secured 1 - M33 Secured 2 - Core (Non Secure)

Table 5-187. FWDMA13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	CORENS	R/W	0h	Controller Core Non Secured: '0' - access not allowed '1' - access allowed
1	M33S	R/W	0h	Controller M33 Secured: '0' - access not allowed '1' - access allowed
0	M33NS	R/W	0h	Controller M33 None Secured: '0' - access not allowed '1' - access allowed

5.6.165 USECSTB Register (Offset = 1000h) [Reset = 00000000h]

USECSTB is shown in Table 5-188.

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Table 5-188. USECSTB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-8	16US	R/W	Fh	Set how many micro second strobes are in 16 micro seconds, minus 1. Default: 16-1 =15.
7-0	US	R/W	4Fh	Set how many soc clk are in one micro second, minus 1. for 40mhz : should be 39. for 80mhz : should be 79. (Soc clock default is 80MHz)

5.6.166 GPIOEVT0NS Register (Offset = 1044h) [Reset = 00000000h]

GPIOEVT0NS is shown in Table 5-189.

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Non-Secured GPIO Event Status, 1st Register. 45 bits status over two registers.

Table 5-189. GPIOEVT0NS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STA31TO0	R	0h	Non-Secured event status , first 32 bits. ([31:0])

5.6.167 GPIOEVT1NS Register (Offset = 1048h) [Reset = 00000000h]

GPIOEVT1NS is shown in Table 5-190.

Return to the Summary Table.

Non-Secured GPIO Event Status, 2nd Register. 45 bits status over two registers.

Table 5-190. GPIOEVT1NS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	STA44TO32	R	0h	Non-Secured event status , 13 MSBs. ([44:32])

5.6.168 DBM33NS0 Register (Offset = 1054h) [Reset = 00000000h]

DBM33NS0 is shown in Table 5-191.

Return to the Summary Table.

M33 Non-Secured Doorbell IMASK. Mask Event. '0' - CLR - Clear Interrupt Mask '1' - SET - Set Interrupt Mask

Table 5-191. DBM33NS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	IMASK	R/W	0h	bit3 - doorbell 7 M3 IRQ bit2 - doorbell 6 M3 IRQ bit1 - doorbell 3 M3 IRQ bit0 - doorbell 2 M3 IRQ

5.6.169 DBNSISET Register (Offset = 1058h) [Reset = 00000000h]

DBNSISET is shown in Table 5-192.

Return to the Summary Table.

M33 Non-Secured Doorbells ISET. Sets event in RIS Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - SET - Sets interrupt

Table 5-192. DBNSISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	ISET	W	0h	bit3 - doorbell 7 M3 IRQ bit2 - doorbell 6 M3 IRQ bit1 - doorbell 3 M3 IRQ bit0 - doorbell 2 M3 IRQ Type: Write-Clear

5.6.170 DBNSICLR Register (Offset = 105Ch) [Reset = 00000000h]

DBNSICLR is shown in Table 5-193.

Return to the Summary Table.

M33 Non-Secured Doorbell ICLR. Clears event in RIS Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - CLR - Clears the Event

Table 5-193. DBNSICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	ICLR	W	0h	bit3 - doorbell 7 M3 IRQ bit2 - doorbell 6 M3 IRQ bit1 - doorbell 3 M3 IRQ bit0 - doorbell 2 M3 IRQ Type: Write-Clear

5.6.171 DBNSIMSET Register (Offset = 1060h) [Reset = 00000000h]

DBNSIMSET is shown in Table 5-194.

Return to the Summary Table.

M33 Non-Secured Doorbell IMSET. Sets Event Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - SET - Set interrupt mask

Table 5-194. DBNSIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	IMSET	W	0h	bit3 - doorbell 7 M3 IRQ bit2 - doorbell 6 M3 IRQ bit1 - doorbell 3 M3 IRQ bit0 - doorbell 2 M3 IRQ Type: Write-Clear

5.6.172 DBNSIMCLR Register (Offset = 1064h) [Reset = 00000000h]

DBNSIMCLR is shown in Table 5-195.

Return to the Summary Table.

M33 Non-Secured Doorbell IMCLR, Clears Event Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - CLR - Clear interrupt mask

Table 5-195. DBNSIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	IMCLR	W	0h	bit3 - doorbell 7 M3 IRQ bit2 - doorbell 6 M3 IRQ bit1 - doorbell 3 M3 IRQ bit0 - doorbell 2 M3 IRQ Type: Write-Clear

5.6.173 DBNSRIS Register (Offset = 1068h) [Reset = 00000000h]

DBNSRIS is shown in Table 5-196.

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M33 Non-Secured Doorbell RIS. Raw interrupt status for event. This bit is set to 1 when an event is received. when the corresponding bit in ICLR is set to 1, this bit will be cleared. Read 0 - CLR - Interrupt did not occur Read 1 - SET - Interrupt occurred

Table 5-196. DBNSRIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	RIS	R	0h	bit3 - doorbell 7 M3 IRQ bit2 - doorbell 6 M3 IRQ bit1 - doorbell 3 M3 IRQ bit0 - doorbell 2 M3 IRQ

5.6.174 DBNSMIS Register (Offset = 106Ch) [Reset = 00000000h]

DBNSMIS is shown in Table 5-197.

Return to the Summary Table.

M33 Non-Secured Doorbell MIS. Mask interrupt status for event Read 0 - CLR - Interrupt did not occur Read 1 - SET - Interrupt occurred

Table 5-197. DBNSMIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	MIS	R	0h	bit3 - doorbell 7 M3 IRQ bit2 - doorbell 6 M3 IRQ bit1 - doorbell 3 M3 IRQ bit0 - doorbell 2 M3 IRQ

5.6.175 GPIOMIS0NS Register (Offset = 1070h) [Reset = 00000000h]

GPIOMIS0NS is shown in Table 5-198.

Return to the Summary Table.

Non Secured GPIO MIS. 31-0

Table 5-198. GPIOMIS0NS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	31TO0	R	0h	32 LSBs of GPIO MIS

5.6.176 GPIOMIS1NS Register (Offset = 1074h) [Reset = 00000000h]

GPIOMIS1NS is shown in Table 5-199.

Return to the Summary Table.

Non Secure GPIO MIS. 44-32

Table 5-199. GPIOMIS1NS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	44TO32	R	0h	13 MSBs of GPIO MIS. 44-32

5.6.177 GPIOFNC0NS Register (Offset = 1078h) [Reset = 00000000h]

GPIOFNC0NS is shown in Table 5-200.

Return to the Summary Table.

Non Secured GPIO Functional Mask. 31-0 0. Mask 1. Un-Mask

Table 5-200. GPIOFNC0NS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MASK31TO0	R/W	0h	32 LSBs of non-secured functional mask for GPIO.

5.6.178 GPIOFNC1NS Register (Offset = 107Ch) [Reset = 00000000h]

GPIOFNC1NS is shown in Table 5-201.

Return to the Summary Table.

non secured gpio functional mask

Table 5-201. GPIOFNC1NS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	MASK44TO32	R/W	0h	13 MSBs of non-secured functional mask for GPIO. 44-32

5.7 SOC_AAON Registers

Table 5-202 lists the memory-mapped registers for the SOC_AAON registers. All register offset addresses not listed in Table 5-202 should be considered as reserved locations and the register contents should not be modified.

Table 5-202. SOC_AAON Registers

Offset	Acronym	Register Name	Section
0h	DMASIMASK	Secure Interrupt Mask	Section 5.7.1
4h	DMASISET	Secure Interrupt Set	Section 5.7.2
8h	DMASICLR	Secure Interrupt Clear	Section 5.7.3
Ch	DMASIMSET	Interrupt Mask Set	Section 5.7.4
10h	DMASIMCLR	Interrupt Mask Clear	Section 5.7.5
14h	DMASRIS	Secure Event Status	Section 5.7.6
18h	DMASMIS	Masked Interrupt Status	Section 5.7.7
1000h	DMANSIMASK	DMA Non-Secure Interrupt Mask	Section 5.7.8
1004h	DMANSISET	DMA Non-Secure Interrupt Set	Section 5.7.9
1008h	DMANSICLR	DMA Non-Secure Interrupt Clear Register	Section 5.7.10
100Ch	DMANSIMSET	DMA Non-Secure Interrupt Mask Set	Section 5.7.11
1010h	DMANSIMCLR	DMA Interrupt Mask Clear	Section 5.7.12
1014h	DMANSRIS	DMA Non -Secure Raw interrupt Status	Section 5.7.13
1018h	DMANSMIS	DMA Non-Secure Mask Interrupt Status	Section 5.7.14

Complex bit access types are encoded to fit into small table cells. Table 5-203 shows the codes that are used for access types in this section.

Table 5-203. SOC_AAON Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

5.7.1 DMASIMASK Register (Offset = 0h) [Reset = 00000000h]

DMASIMASK is shown in Table 5-204.

Return to the Summary Table.

DMA M33 Secure Event IMASK. Mask Event. '0' - CLR - Clear Interrupt Mask '1' - SET - Set Interrupt Mask

Table 5-204. DMASIMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	IMASK	R/W	0h	'0' - CLR - Clear Interrupt Mask '1' - SET - Set Interrupt Mask

5.7.2 DMASISET Register (Offset = 4h) [Reset = 00000000h]

DMASISET is shown in Table 5-205.

Return to the Summary Table.

DMA M33 Secure Event ISET. Sets event in RIS Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - SET - Sets interrupt

Table 5-205. DMASISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	ISET	W	0h	Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - SET - Sets interrupt Type: Write-Clear.

5.7.3 DMASICLR Register (Offset = 8h) [Reset = 00000000h]

DMASICLR is shown in Table 5-206.

Return to the Summary Table.

DMA M33 Secure Event ICLR. Clears event in RIS Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - CLR - Clears the Event

Table 5-206. DMASICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	ICLR	W	0h	Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - CLR - Clears the Event Type: Write-Clear.

5.7.4 DMASIMSET Register (Offset = Ch) [Reset = 00000000h]

DMASIMSET is shown in Table 5-207.

Return to the Summary Table.

DMA M33 Secure Event IMSET. Sets Event Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - SET - Set interrupt mask

Table 5-207. DMASIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	IMSET	W	0h	Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - SET - Set interrupt mask Type: Write-Clear

5.7.5 DMASIMCLR Register (Offset = 10h) [Reset = 00000000h]

DMASIMCLR is shown in Table 5-208.

Return to the Summary Table.

DMA M33 Secure Event IMCLR. Clears Event Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - CLR - Clear interrupt mask

Table 5-208. DMASIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	IMCLR	W	0h	Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - CLR - Clear interrupt mask Type: Write-Clear.

5.7.6 DMASRIS Register (Offset = 14h) [Reset = 00000000h]

DMASRIS is shown in Table 5-209.

Return to the Summary Table.

DMA M33 Secure Event RIS. Raw interrupt status for event. This bit is set to 1 when an event is received. when the corresponding bit in ICLR is set to 1, this bit will be cleared. Read 0 - CLR - Interrupt did not occur Read 1 - SET - Interrupt occurred

Table 5-209. DMASRIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	RIS	R	0h	Read 0 - CLR - Interrupt did not occur Read 1 - SET - Interrupt occurred

5.7.7 DMASMIS Register (Offset = 18h) [Reset = 00000000h]

DMASMIS is shown in Table 5-210.

Return to the Summary Table.

DMA M33 Secure Event MIS. Mask interrupt status for event Read 0 - CLR - Interrupt did not occur Read 1 - SET - Interrupt occurred

Table 5-210. DMASMIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	MIS	R	0h	Read 0 - CLR - Interrupt did not occur Read 1 - SET - Interrupt occurred

5.7.8 DMANSIMASK Register (Offset = 1000h) [Reset = 00000000h]

DMANSIMASK is shown in Table 5-211.

Return to the Summary Table.

DMA M33 Non-Secured IMASK. Mask Event. '0' - CLR - Clear Interrupt Mask '1' - SET - Set Interrupt Mask

Table 5-211. DMANSIMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	IMASK	R/W	0h	'0' - CLR - Clear Interrupt Mask '1' - SET - Set Interrupt Mask

5.7.9 DMANSISET Register (Offset = 1004h) [Reset = 00000000h]

DMANSISET is shown in Table 5-212.

Return to the Summary Table.

DMA M33 Non-Secured ISET. Sets event in RIS Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - SET - Sets interrupt

Table 5-212. DMANSISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	ISET	W	0h	Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - SET - Sets interrupt Type: Write-Clear.

5.7.10 DMANSICLR Register (Offset = 1008h) [Reset = 00000000h]

DMANSICLR is shown in Table 5-213.

Return to the Summary Table.

DMA M33 Non-Secured ICLR. Clears event in RIS Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - CLR - Clears the Event

Table 5-213. DMANSICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	ICLR	W	0h	Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - CLR - Clears the Event Type: Write-Clear.

5.7.11 DMANSIMSET Register (Offset = 100Ch) [Reset = 00000000h]

DMANSIMSET is shown in Table 5-214.

Return to the Summary Table.

DMA M33 Non-Secured IMSET. Sets Event Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - SET - Set interrupt mask

Table 5-214. DMANSIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	IMSET	W	0h	Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - SET - Set interrupt mask Type: Write-Clear

5.7.12 DMANSIMCLR Register (Offset = 1010h) [Reset = 00000000h]

DMANSIMCLR is shown in Table 5-215.

Return to the Summary Table.

DMA M33 Non-Secured IMCLR. Clears Event Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - CLR - Clear interrupt mask

Table 5-215. DMANSIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	IMCLR	W	0h	Write 0 - NO_EFFECT - Writing 0 has no effect Write 1 - CLR - Clear interrupt mask Type: Write-Clear.

5.7.13 DMANSRIS Register (Offset = 1014h) [Reset = 00000000h]

DMANSRIS is shown in Table 5-216.

Return to the Summary Table.

DMA M33 Non-Secured RIS. Raw interrupt status for event. This bit is set to 1 when an event is received. when the corresponding bit in ICLR is set to 1, this bit will be cleared. Read 0 - CLR - Interrupt did not occur Read 1 - SET - Interrupt occurred

Table 5-216. DMANSRIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	RIS	R	0h	Read 0 - CLR - Interrupt did not occur Read 1 - SET - Interrupt occurred

5.7.14 DMANSMIS Register (Offset = 1018h) [Reset = 00000000h]

DMANSMIS is shown in Table 5-217.

Return to the Summary Table.

DMA M33 Non-Secured MIS. Mask interrupt status for event Read 0 - CLR - Interrupt did not occur Read 1 - SET - Interrupt occurred

Table 5-217. DMANSMIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	MIS	R	0h	Read 0 - CLR - Interrupt did not occur Read 1 - SET - Interrupt occurred

Chapter 6

Debug Subsystem (DEBUGSS)

This chapter discussions the features of the debug subsystem (DEBUGSS).

6.1 Introduction

The debug subsystem (DEBUGSS) interfaces the serial wire debug (SWD) two-wire physical interface to multiple debug functions within the device. Debugging of processor execution and the device state are supported. The DEBUGSS also provides a mailbox system for communicating with software through SWD.

Key features provided by the debug subsystem include:

- Two-wire(SWDIO, SWCLK) debug interface, compatible with both TI and 3rd party debug probes
  - On-chip pull-up/pull-down resistors for SWDIO and SWCLK, respectively, enabled by default
  - Support for disabling SWD functions to use SWD pins as general purpose input/output pins
  - Capability of waking the device from SHUTDOWN mode upon valid SWD activity
- Debug of the processor
  - Run, halt, and step debug support
  - 8 hardware breakpoints (BPU)
- Software
  - configurable peripheral behavior during processor debug
  - Ability to free run select peripherals through debug halt
  - Ability to halt select peripherals on a debug halt
  - Ability to obtain status and override the power, reset and execution state of debug targets in dynamically controlled sub-domains (Sub-Domain PREC Register that can be configured by debug tooling)
- Debug subsystem mailbox (DSSM) for passing data and control signals over SWD interface to and from boot coprocessor
- Cold start reset
- Boot
  - Device Activation
  - Programming
- Support for various security features, including software authenticated request.

6.2 Block Diagram

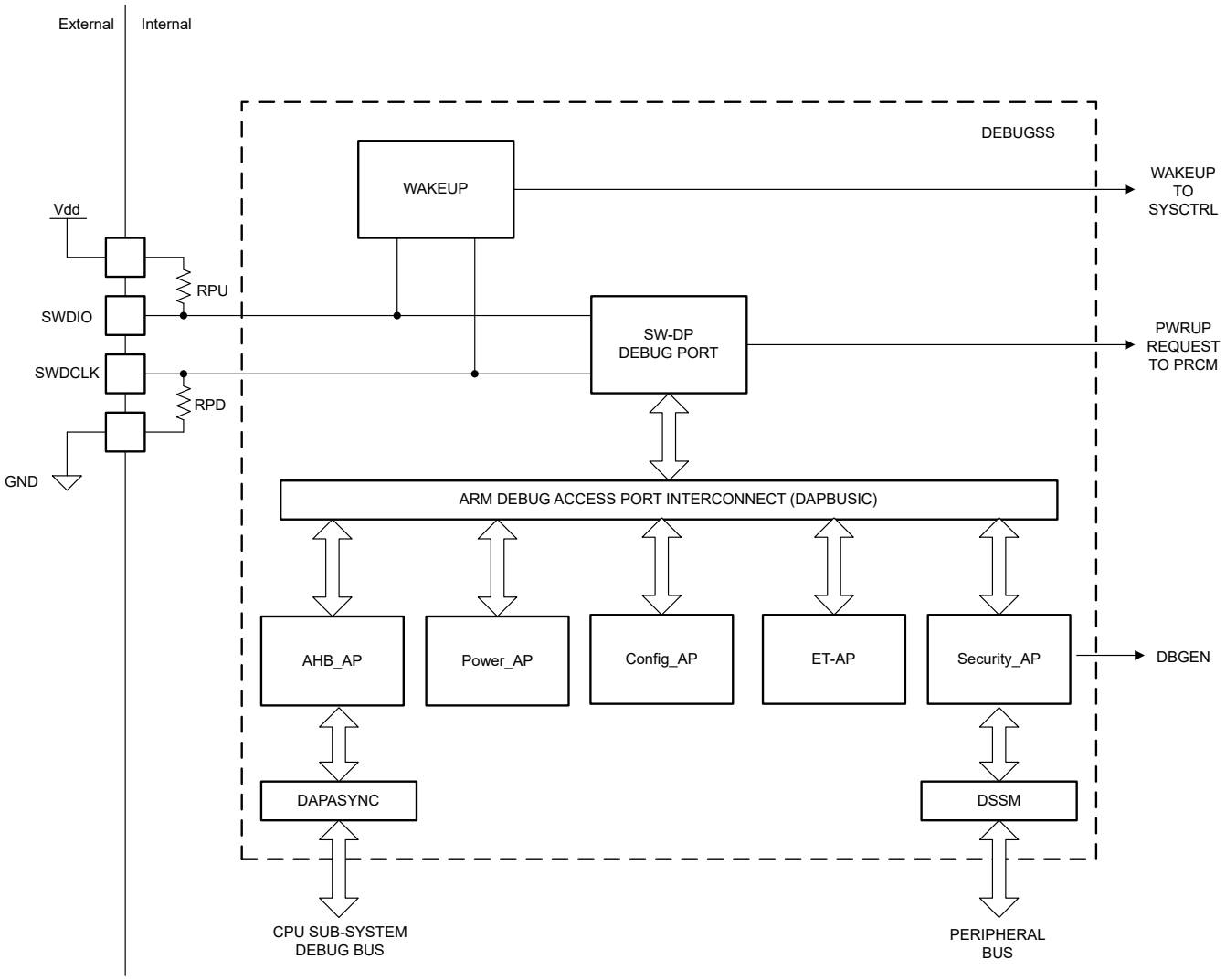

Figure 6-1. DEBUGSS Block Diagram

6.3 Overview

The SWD physical interface interacts with the Arm serial wire debug port (SW-DP) to gain access to the debug access port bus interconnect (DAPBUSIC) when the SW-DP is enabled. From TI, devices ship with the SW-DP enabled to allow SWD access to the device for development and production programming. The DAPBUSIC enables a debug probe to access one or more debug access ports. The available access ports are given in Section 6.5.

6.4 Physical Interface

Debug connections to the device are supported through an Arm serial wire debug (SWD) compliant interface.

The SWD interface requires two connections:

- A bidirectional data line (SWDIO) used to send data to, and receive data from the device
- A unidirectional clock line (SWCLK) driven by the debug probe connecting to the device

The SWD interface uses the standard logic levels of the device for SWD communication. See the device-specific data sheet for input and output logic levels for a given supply voltage (VIO). A SWCLK frequency of up to 20MHz is supported by the DEBUGSS.

During SWD operation, the SWDIO line can be driven high or driven low by either the target device or the debug probe. As either device can drive the line, when ownership of the shared SWDIO line is switched between the device and the debug probe, undriven time slots are inserted as a part of the SWD protocol. The primary purpose of the pull-up resistor on the SWDIO line, and the pull-down resistor on the SWCLK line, is to place the SWD pins into a known state when no debug probe is attached. A minimum resistance of 100 kΩ is recommended by Arm. The internal pull-up/pull-down resistors fulfill this requirement and external resistors are not required for correct operation of the SWD interface.

Upon physical connection of a debug probe, a configuration sequence must be sent from the debug probe to the target device to initiate a valid SWD connection with the SW-DP. Once the sequence is transmitted and the SWD connection is established, communication with enabled debug access points is possible and the bootcode is alerted through assertion of DBGSS.DBGCTL[1] SWDSEL bit which is continuously monitored in bootcode. The debug probe must be disconnected by sending disconnection sequence from the debug probe to target device.

6.5 Debug Access Ports

The debug access ports in the DEBUGSS are given in Table 6-1

Table 6-1. DEBUGSS Access Port Listing

APSEL	AP	Port Description	Purpose
0x0	Config-AP	Configuration access port	Access device type information
0x1	Power-AP	PRCM access port	Access power, reset, and clock status
0x2	Security-AP	Security access port	Access the debug mailbox
0x3	ET-AP	Energy Trace access port	Access status of internal IP's
0x7	AHB-AP	CPUSS debug access port	Debug of the processor and peripherals

Debug of the processor and peripherals

The Config-AP provides device information to the debug probe so that the debug probe can identify device characteristics, including the device part number and the device revision.

The Power-AP provides the option to query and control the subdomain power, clock reset and execution states.

The Security-AP provides access to the mailbox for communicating with software running on the device through SWD.

The ET-AP provides access to the activity status of every IP (reset, enabled, active).

The AHB-AP provides the complete device debug functionality (processor debug, peripheral and memory bus access and processor state). See Section 6.6 for more information.

6.6 Debug Features

The DEBUGSS supports processor debug and peripheral debug.

6.6.1 Processor Debug

The Arm Cortex-M33 processor supports a wide range of features to simplify debugging of application software during development. Key features supported by CC35xx wireless MCUs include:

- Ability to halt the processor through an assertion of a halt signal, such as a configured debug event (such as a hard fault entry or reset)
- Ability to step through instructions (with or without peripheral interrupts enabled)
- Ability to run through instructions (with or without peripheral interrupts enabled)

- Ability to read and write CPU registers when halted
- Ability to read exception information through the system control space (SCS)
- Support for 8 hardware breakpoints
- Support for accessing the device memory map and seperate into secure/non-secure partitions

6.6.2 Breakpoint Unit (BPU)

The breakpoint unit (BPU) provides 8 comparators which can be used to generate a debug event when the address of an instruction fetch matches the address programmed into the one of the BPU comparators.

The BPU comparators match instruction fetches from the code memory region, meaning the comparators only operate on instruction read accesses.

The comparators do not match data read or data write accesses. Address matching is possible for half-word (16-bit) instructions and word (32-bit) instructions fetched from the CODE region (0x00000000 to 0x1FFFFFFF).

6.6.3 Peripheral Debug

In addition to processor debug, the DEBUGSS can be used to access the device memory map from the perspective of the processor. Thus, a connected debug probe can be used to read and write memory-mapped peripheral registers, the system SRAM, and the flash memory.

Certain peripherals support advanced debug configuration options. These options are configured by application software (or optionally, the debug probe) by setting/clearing various debug control bits in the memory map of a given peripheral. In general, the debug behavior of a particular peripheral is specified in the EMU register of each peripheral. Many peripherals offer the option of halting the functional clock to the peripheral when the processor is halted for debug, thus pausing the peripheral together with the processor (default configuration), or letting the peripheral run even when the processor is halted for debug.

For example, the SYSTIM peripheral supports the RUN/STOP bits in the EMU register. Setting the RUN bit in EMU for a SYSTIM causes the SYSTIM to run even if the processor is halted for debug.

6.7 Behavior in Low Power Modes

The DEBUGSS supports maintaining a debug connection through SWD in all operating modes except SHUTDOWN.

Access to device memory and peripherals is possible in ACTIVE mode and IDLE mode, in which a debug probe can be actively connected to the AHB-AP access port to interface with the processor. In SLEEP mode, a debug connection can be established and/or maintained with the DEBUGSS, but not with the CPU debug access port.

The DEBUGSS functionality by operating mode is given in Table 6-2.

Table 6-2. DEBUGSS Functionality by Operating Mode

Capability	ACTIVE	IDLE	SLEEP
Processor debug	Y	Y	N
Memory Map access	Y	Y	N
Debug status through SWDP	Y	Y	Y
Cold Start Reset	Y	Y	Y
Debug state maintained	Y	Y	Y

6.8 Debug Access Control

The debug subsystem supports several methods for controlling JTAG debug access to the device through the SWD interface through fuses.

- Open (default) – the debug authentication is bypassed when the device is passed to the vendor for its SW development to allow simple debug. Recommended not to deploy the device with this method.

- Authenticated Debug – only based on signed and authenticated debug request (different per device). Accessed via Vendor ROT public key – debug request is signed using the private key associated with the public key vendor ROT.

For more information on Root-of-Trust (ROT), see Chapter 12.

6.9 SOC_DEBUGSS Registers

Table 6-3 lists the memory-mapped registers for the SOC_DEBUGSS registers. All register offset addresses not listed in Table 6-3 should be considered as reserved locations and the register contents should not be modified.

Table 6-3. SOC_DEBUGSS Registers

Offset	Acronym	Register Name	Section
0h	CFGAPDEVID	Device Identification	Section 6.9.1
4h	CFGAPDEVUC	Device User Identifier	Section 6.9.2
8h	DBGSSVER	Debug Subsystem Version	Section 6.9.3
10h	CFGAPBOOT	Boot Diagnostics	Section 6.9.4
14h	CFGAPLCST	Lifecycle State	Section 6.9.5
1Ch	RSTREQ	Reset Request	Section 6.9.6
28h	CFGAPUDID0	Device Identifier Low	Section 6.9.7
2Ch	CFGAPUDID1	Device ID Upper	Section 6.9.8
FCh	CFGAPIDR	AP identification register	Section 6.9.9
100h	PWRAPDP0	Domain Power Reset Execution Control Register0	Section 6.9.10
104h	PWRAPDP1	Power Reset Control	Section 6.9.11
108h	PWRAPDP2	Debug Power Control	Section 6.9.12
10Ch	PWRAPDP3	Power Reset Control	Section 6.9.13
1FCh	PWRAPIDR	Identification Register	Section 6.9.14
200h	SECAPTXD	Security Transmit Data	Section 6.9.15
204h	SECAPTXCTL	Transmit Control	Section 6.9.16
208h	SECAPRXD	Receive data register	Section 6.9.17
20Ch	RXCTL	Receive Control	Section 6.9.18
2FCh	SECAPIDR	Access Port Identification	Section 6.9.19

Complex bit access types are encoded to fit into small table cells. Table 6-4 shows the codes that are used for access types in this section.

Table 6-4. SOC_DEBUGSS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

6.9.1 CFGAPDEVID Register (Offset = 0h) [Reset = 0000002Fh]

CFGAPDEVID is shown in Table 6-5.

Return to the Summary Table.

CFGAP Device ID. The device identification register allows the manufacturer, part number, and version of a component to be determined. This is the same 32-bit value obtained via the IDCODE instruction in the optional ICEPickM Scan module and is determined by tie-offs at DebugSS boundary.

Table 6-5. CFGAPDEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	VER	R	0h	Revision of the device. This field should change each time that the logic or mask set of the device is revised.
27-12	PARTNUM	R	0h	Identifies the part
11-1	MAN	R	17h	TI's JEDEC bank and company code, which is 00000010111b
0	ALWAYSONE	R	1h	The value 1 in bit 0 of a JTAG IDCODE means that a 32-bit scan register exists. This is replicated here for completeness.

6.9.2 CFGAPDEVUC Register (Offset = 4h) [Reset = 00000000h]

CFGAPDEVUC is shown in Table 6-6.

Return to the Summary Table.

CFGAP Device User Code. The Device Usercode register is used in conjunction with the Device Identification Register to provide extended device information. This is the same 32-bit value obtained via the USERCODE instruction in the optional ICEPickM Scan module and is determined by tie-offs at DebugSS boundary.

Table 6-6. CFGAPDEVUC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	USERCODE	R	0h	The Device Usercode register is used in conjunction with the Device Identification Register to provide extended device information. This is the same 32-bit value obtained via the USERCODE instruction in the optional ICEPickM Scan module and is determined by tie-offs at DebugSS boundary.

6.9.3 DBGSSVER Register (Offset = 8h) [Reset = 40000098h]

DBGSSVER is shown in Table 6-7.

Return to the Summary Table.

CFGAP DEBUGSS Version. The DebugSS Configuration Register provides information on the configuration of this particular instance of the subsystem.

Table 6-7. DBGSSVER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	REVMAJ	R	4h	Indicates the major revision of this Subsystem instance.
27-24	REVMIN	R	0h	Indicates the minor revision of this Subsystem instance. Currently 0000b
23-8	RESERVED	R	0h	Reserved space write will be ignored and read will result in zeroes
7	PWRAP	R	1h	A value of '1' indicates this subsystem instance contains a Power-AP module
6	SYSTEMAP	R	0h	A value of '1' indicates this subsystem instance contains an AHB-AP module for system bus controllering
5	APBAP	R	0h	A value of '1' indicates this subsystem instance contains an ABP-AP for accessing system level debug components
4	SECAP	R	1h	A value of '1' indicates this subsystem instance contains a Secure AP
3	ETAP	R	1h	A value of '1' indicates this subsystem instance contains an EnergyTrace AP
2	ICEPICKM	R	0h	A value of '1' indicates this subsystem instance contains an ICEPickM Scan module for extended scan support
1	TRIG	R	0h	A value of '1' indicates this subsystem instance contains Cross Trigger submodule
0	TRACE	R	0h	A value of '1' indicates this subsystem instance contains a Trace submodule

6.9.4 CFGAPBOOT Register (Offset = 10h) [Reset = 00000000h]

CFGAPBOOT is shown in Table 6-8.

Return to the Summary Table.

CFGAP Boot Diag. This register provides feedback on the boot process

Table 6-8. CFGAPBOOT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DIAGVAL	R	0h	This register provides feedback on the boot process [3:0] PG_Version [5:3] Metal_Version [8:6] Memory Stacking [11:9] Package type [13:12] Temperature [17:14] Device PartNumber [18] Disable 5GHz [19] Disable 6GHz [20] Disable BLE [21] Disable BLE M0+ [22] Disable CAN FD [25:23] Boot ROM Version (FMU) [26] Launch pad Mode [28:27] SDIO Product ID [31:29] TI Fuse ROM Structure Version

6.9.5 CFGAPLCST Register (Offset = 14h) [Reset = 00000000h]

CFGAPLCST is shown in Table 6-9.

Return to the Summary Table.

CFGAP Life-cycle. Indicates the current device lifecycle state

Table 6-9. CFGAPLCST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LCSVAL	R	0h	Life cycle state [3:0] PG_Version [5:3] Metal_Version [8:6] Memory Stacking [11:9] Package type [13:12] Temperature [17:14] Device PartNumber [18] Disable 5GHz [19] Disable 6GHz [20] Disable BLE [21] Disable BLE M0+ [22] Disable CAN FD [25:23] Boot ROM Version (FMU) [26] Launch pad Mode [28:27] SDIO Product ID [31:29] TI Fuse ROM Structure Version

6.9.6 RSTREQ Register (Offset = 1Ch) [Reset = 00000000h]

RSTREQ is shown in Table 6-10.

Return to the Summary Table.

Reset Request. This bit can be configured to request reset.

Table 6-10. RSTREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	REQ	W	0h	This bit can be configured to request device reset

6.9.7 CFGAPUDID0 Register (Offset = 28h) [Reset = 00000000h]

CFGAPUDID0 is shown in Table 6-11.

Return to the Summary Table.

CFGAP Unique Device 0. Used to provide a unique device ID/token for security authentication of tester and tools. Unique device ID is 64bit value and this register reads lower 32 bits.

Table 6-11. CFGAPUDID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Used to provide a unique divide ID/token for security authentication of tester and tools

6.9.8 CFGAPUDID1 Register (Offset = 2Ch) [Reset = 00000000h]

CFGAPUDID1 is shown in Table 6-12.

Return to the Summary Table.

CFGAP Unique Device 1. Used to provide a unique device ID/token for security authentication of tester and tools. Unique device ID is 64bit value and this register reads upper 32 bits.

Table 6-12. CFGAPUDID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Used to provide a unique devide ID/token for security authentication of tester and tools

6.9.9 CFGAPIDR Register (Offset = FCh) [Reset = 102E0001h]

CFGAPIDR is shown in Table 6-13.

Return to the Summary Table.

CFGAP Identification Register. AP Identification Register. The AP identification register allows tools to determine the manufacturer and the type of AP.

Table 6-13. CFGAPIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	REV	R	1h	Component Revision. Indicates the revision of this AP instance. Currently 0001b
27-17	JEPIDS	R	17h	Manufacturer JEP106 ID. The concatenated JEP106 ID and continuation ID for TI. This is 00000010111b.
16	APCLASS	R	0h	AP Class. 0 indicates that this AP is not a bridge to a memory interconnect (not a Memory Access Port).
15-8	RESERVED	R	0h	reserved.
7-4	APVAR	R	0h	AP Variant. There is only one variant for this AP Type and it is 0.
3-0	APTYPE	RC	1h	The AP Type Register. TI Subsystem Config APs have a type of 0001b

6.9.10 PWRAPDP0 Register (Offset = 100h) [Reset = 00000000h]

PWRAPDP0 is shown in Table 6-14.

Return to the Summary Table.

Sub-Domain PREC Register This register provides an interface for debug tooling to obtain status and override the power, reset and execution state of debug targets in dynamically controlled sub-domains.

Table 6-14. PWRAPDP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	RESERVED	R	0h	Reserved
29	RESERVED	R	0h	Reserved
28	RESERVED	R	0h	Reserved
27	RESERVED	R	0h	Reserved
26	RESERVED	R	0h	Reserved
25	RESERVED	R	0h	Reserved
24	RESERVED	R	0h	Reserved
23	RESERVED	R	0h	Reserved
22	RSTOCC	RH/W	0h	Input from CPU-SS. Used by debug tools. A sticky bit Indicate that a reset to WSOC MCU has happened since last time tools checked. Cleared on write by the tool.
21	PWRLOSS	RH/W	0h	Input from PRCM. Used by debug tools. A sticky bit Indicate that a power loss to CORE has happened since last time tools checked. Cleared on write by the tool.
20	RESERVED	R	0h	Reserved
19	DBGPWR	RH	0h	Used to indicate power state of debug logic in the associated domain. 0 -> Debug logic is off. 1 -> Debug logic is powered.
18	UNNATRST	RH	0h	input from PRCM. "1" indicate that WSOC MCU (SYSRSTn) reset is extended.
17	IRSTRELWIR	RH/W	0h	Input from PRCM. "1" indicates WSOC MCU is in reset. Setting this bit shall release the extended SYSRSTn to WSOc MCU.
16-14	RSTCTL	RH/W	0h	Following are the field values with their description. 000 -> Normal Operation; 001 -> Wait in Reset (Reset Ext); 010 -> Block Reset; 100- > Reset Req.
13	DBGEN	RH/W	0h	Defines operating mode of debug logic in Cortex. Not used in MX.
12-11	DBGMOD	RH/W	0h	Used to define debug properties. Not used in MX.
10	DBGATT	RH	0h	Input from CPU-SS. "1" indicate that WSOC MCU is halted and in debug mode.
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	PWRDWNDES	RH	0h	Input from ELP. Indicates that CORE domain can be shutdown.
6	RESERVED	R	0h	Reserved
5	PWR	RH	0h	Input from PRCM. "1" indicates CORE domain is powered.
4	CLKDWNDES	RH	0h	"1" indicated that WSOC MCU is clocked artificially.
3	FORCEACT	RH/W	0h	Provides debug override of the default state of the CORE P.D power and clock.
2	CLKSTATE	RH	0h	Input from CPU-SS. "1" indicated that WSOC MCU is clocked by it's functional clock.
1	CORESACC	RH	0h	Input from DSSM. Indicate that WSOC MCU Power-AP overrides are writable.
0	COREPRES	RH	0h	1 indicates that WSOC MCU is present in this device.

6.9.11 PWRAPDP1 Register (Offset = 104h) [Reset = 00000000h]

PWRAPDP1 is shown in Table 6-15.

Return to the Summary Table.

Sub-Domain PREC Register This register provides an interface for debug tooling to obtain status and override the power, reset and execution state of debug targets in dynamically controlled sub-domains.

Table 6-15. PWRAPDP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	RESERVED	R	0h	Reserved
29	RESERVED	R	0h	Reserved
28	RESERVED	R	0h	Reserved
27	RESERVED	R	0h	Reserved
26	RESERVED	R	0h	Reserved
25	RESERVED	R	0h	Reserved
24	RESERVED	R	0h	Reserved
23	RESERVED	R	0h	Reserved
22	RSTOCC	RH/W	0h	Input from CPU-SS. Used by debug tools. A sticky bit Indicate that a reset to WPHY MCU has happened since last time tools checked. Cleared on write by the tool.
21	PWRLOSS	RH/W	0h	Input from PRCM. Used by debug tools. A sticky bit Indicate that a power loss to CORE has happened since last time tools checked. Cleared on write by the tool.
20	RESERVED	R	0h	Reserved
19	DBGPWR	RH	0h	Used to indicate power state of debug logic in the associated domain. 0 -> Debug logic is off. 1 -> Debug logic is powered.
18	RESERVED	R	0h	Reserved
17	INRST	RH	0h	Input from PRCM. "1" indicates WPHY MCU is in reset.
16-14	RSTCTL	RH/W	0h	Following are the field values with their description. 000 -> Normal Operation; 001 -> Wait in Reset (Reset Ext); 010 -> Block Reset; 100- > Reset Req.
13	DBGEN	RH/W	0h	Defines operating mode of debug logic in Cortex. Not used in MX.
12-11	DBGMOD	RH/W	0h	Used to define debug properties. Not used in MX.
10	DBGATT	RH	0h	Input from CPU-SS. "1" indicate that WPHY MCU is halted and in debug mode.
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	PWRDWNDES	RH	0h	Input from ELP. Indicates that CORE domain can be shutdown.
6	RESERVED	R	0h	Reserved
5	PWR	RH	0h	Input from PRCM. "1" indicates CORE domain is powered.
4	CLKDWNDES	RH	0h	Input from ?. "1" indicated that WPHY MCU is clocked artificially.
3	FORCEACT	RH/W	0h	Provides debug override of the default state of the CORE P.D power and clock.
2	CLKSTATE	RH	0h	Input from CPU-SS. "1" indicated that WPHY MCU is clocked by it's functional clock.
1	CORESACC	RH	0h	Input from DSSM. Indicate that WSOC MCU, WPHY and LRF MCU (CORE domain cores) Power-AP overrides are writable.
0	COREPRES	RH	0h	1 indicates that WPHY MCU is present in this device.

6.9.12 PWRAPDP2 Register (Offset = 108h) [Reset = 00000000h]

PWRAPDP2 is shown in Table 6-16.

Return to the Summary Table.

Sub-Domain PREC Register This register provides an interface for debug tooling to obtain status and override the power, reset and execution state of debug targets in dynamically controlled sub-domains.

Table 6-16. PWRAPDP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	RESERVED	R	0h	Reserved
29	RESERVED	R	0h	Reserved
28	RESERVED	R	0h	Reserved
27	RESERVED	R	0h	Reserved
26	RESERVED	R	0h	Reserved
25	RESERVED	R	0h	Reserved
24	RESERVED	R	0h	Reserved
23	RESERVED	R	0h	Reserved
22	RSTOCC	RH/W	0h	Input from CPU-SS. Used by debug tools. A sticky bit Indicate that a reset to LRF MCU has happened since last time tools checked. Cleared on write by the tool.
21	PWRLOSS	RH/W	0h	Input from PRCM. Used by debug tools. A sticky bit Indicate that a power loss to CORE has happened since last time tools checked. Cleared on write by the tool.
20	RESERVED	R	0h	Reserved
19	DBGPWR	RH	0h	Used to indicate power state of debug logic in the associated domain. 0 -> Debug logic is off. 1 -> Debug logic is powered.
18	RESERVED	R	0h	Reserved
17	INRST	RH	0h	Input from PRCM. "1" indicates LRF MCU is in reset.
16-14	RSTCTL	RH/W	0h	Following are the field values with their description. 000 -> Normal Operation; 001 -> Wait in Reset (Reset Ext); 010 -> Block Reset; 100- > Reset Req.
13	DBGEN	RH/W	0h	Defines operating mode of debug logic in Cortex. Not used in MX.
12-11	DBGMOD	RH/W	0h	Used to define debug properties. Not used in MX.
10	DBGATT	RH	0h	Input from CPU-SS. "1" indicate that LRF MCU is halted and in debug mode.
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	PWRDWNDES	RH	0h	Input from ELP. Indicates that CORE domain can be shutdown.
6	RESERVED	R	0h	Reserved
5	PWR	RH	0h	Input from PRCM. "1" indicates CORE domain is powered.
4	CLKDWNDES	RH	0h	Input from ?. "1" indicated that LRF MCU is clocked artificially.
3	FORCEACT	RH/W	0h	Provides debug override of the default state of the CORE P.D power and clock.
2	CLKSTATE	RH	0h	Input from CPU-SS. "1" indicated that LRF MCU is clocked by it's functional clock.
1	CORESACC	RH	0h	Input from DSSM. Indicate that WSOC MCU, WPHY and LRF MCU (CORE domain cores) Power-AP overrides are writable.
0	COREPRES	RH	0h	1 indicates that LRF MCU is present in this device.

6.9.13 PWRAPDP3 Register (Offset = 10Ch) [Reset = 00000000h]

PWRAPDP3 is shown in Table 6-17.

Return to the Summary Table.

Sub-Domain PREC Register This register provides an interface for debug tooling to obtain status and override the power, reset and execution state of debug targets in dynamically controlled sub-domains.

Table 6-17. PWRAPDP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	RESERVED	R	0h	Reserved
29	RESERVED	R	0h	Reserved
28	RESERVED	R	0h	Reserved
27	RESERVED	R	0h	Reserved
26	RESERVED	R	0h	Reserved
25	RESERVED	R	0h	Reserved
24	RESERVED	R	0h	Reserved
23	RESERVED	R	0h	Reserved
22	RSTOCC	RH/W	0h	Input from CPU-SS. Used by debug tools. A sticky bit Indicate that a reset to APP MCU has happened since last time tools checked. Cleared on write by the tool.
21	PWRLOSS	RH/W	0h	Input from PRCM. Used by debug tools. A sticky bit Indicate that a power loss to HOST has happened since last time tools checked. Cleared on write by the tool.
20	RESERVED	R	0h	Reserved
19	DBGPWR	RH	0h	Used to indicate power state of debug logic in the associated domain. 0 -> Debug logic is off. 1 -> Debug logic is powered.
18	UNNATRST	RH	0h	input from PRCM. "1" indicate that APPCPU (SYSRSTn) reset is extended.
17	IRSTRELWIR	RH	0h	Input from PRCM. "1" indicates APP MCU is in reset.
16-14	RSTCTL	RH/W	0h	Following are the field values with their description. 000 -> Normal Operation; 001 -> Wait in Reset (Reset Ext); 010 -> Block Reset; 100- > Reset Req.
13	DBGEN	RH/W	0h	Defines operating mode of debug logic in Cortex. Not used in MX.
12-11	DBGMOD	RH/W	0h	Used to define debug properties. Not used in MX.
10	DBGATT	RH	0h	Input from CPU-SS. "1" indicate that APP MCU is halted and in debug mode.
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	PWRDWNDES	RH	0h	Input from ?. Indicates that HOST domain can be shutdown.
6	RESERVED	R	0h	Reserved
5	PWR	RH	0h	Input from PRCM. "1" indicates HOST domain is powered.
4	CLKDWNDES	RH	0h	Input from ?. "1" indicated that APP MCU is clocked artificially.
3	FORCEACT	RH/W	0h	Provides debug override of the default state of the HOST P.D power and clock.
2	CLKSTATE	RH	0h	Input from CPU-SS. "1" indicated that APP MCU is clocked by it's functional clock.
1	CORESACC	RH	0h	Input from DSSM. Indicate that HOST Power-AP overrides are writable.
0	COREPRES	RH	0h	1 indicates that APP MCU is present in this device.

6.9.14 PWRAPIDR Register (Offset = 1FCh) [Reset = 002E0002h]

PWRAPIDR is shown in Table 6-18.

Return to the Summary Table.

PWEAP Identification Register. The AP identification register allows tools to determine the manufacturer and the type of AP.

Table 6-18. PWRAPIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	REV	R	0h	Component Revision. Indicates the revision of this AP instance. Currently 0000b
27-17	JEPIDS	R	17h	Manufacturer JEP106 ID. The concatenated JEP106 ID and continuation ID for TI. This is 00000010111b.
16	APCLASS	R	0h	AP Class. 0 indicates that this is AP is not a bridge to a memory interconnect (not a Memory Access Port).
15-8	RESERVED	R	0h	Reserved.
7-4	APVAR	R	0h	AP Variant. There is only one variant for this AP Type and it is 0.
3-0	APTYPE	RC	2h	The AP Type Register. TI Subsystem Config APs have a type of 0001b

6.9.15 SECAPTXD Register (Offset = 200h) [Reset = 00000000h]

SECAPTXD is shown in Table 6-19.

Return to the Summary Table.

Transmit Data Register. This register is used to pass data to the system security logic.

Table 6-19. SECAPTXD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Transmit Data Register. This register is used to pass data to the system security logic.

6.9.16 SECAPTXCTL Register (Offset = 204h) [Reset = 00000000h]

SECAPTXCTL is shown in Table 6-20.

Return to the Summary Table.

Transmit Control Register. This register provides the handshake for the TX Data Register and can also be used to pass control data to the system security logic.

Table 6-20. SECAPTXCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	TXCTL	R/W	0h	Device specific control information from the system security logic
0	DATAVAIL	R	0h	Transmit Data Available. Set automatically when the TX data Register is written Cleared automatically when the system debug logic indicates it has accepted the TX data

6.9.17 SECAPRXD Register (Offset = 208h) [Reset = 00000000h]

SECAPRXD is shown in Table 6-21.

Return to the Summary Table.

Receive Data Register. This register is used to pass data from the system security logic.

Table 6-21. SECAPRXD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Receive Data Register. This register is used to pass data from the system security logic.

6.9.18 RXCTL Register (Offset = 20Ch) [Reset = 00000000h]

RXCTL is shown in Table 6-22.

Return to the Summary Table.

Receive Control Register. This register provides the handshake for the RX Data Register and can also be used to pass control data from the system security logic.

Table 6-22. RXCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RXCTL	R/W	0h	Device specific control information from the system security logic
0	DATAVAIL	R	0h	Set automatically when the system security logic indicates that RX Data Register is valid. Cleared automatically when the RX data Register is read.

6.9.19 SECAPIDR Register (Offset = 2FCh) [Reset = 002E0000h]

SECAPIDR is shown in Table 6-23.

Return to the Summary Table.

AP Identification Register. The AP identification register allows tools to determine the manufacturer and the type of AP.

Table 6-23. SECAPIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	REVISION	R	0h	Component Revision. Indicates the revision of this AP instance.
27-17	JEPIDS	R	17h	Manufacturer JEP106 ID. The concatenated JEP106 ID and continuation ID for TI. This is 00000010111b.
16	APCLASS	R	0h	AP Class. 0 indicates that this AP is not a bridge to a memory interconnect (not a Memory Access Port).
15-8	RESERVED	R	0h	reserved.
7-4	APVAR	R	0h	AP Variant. There is only one variant for this AP Type and it is 0.
3-0	APTYPE	RC	0h	The AP Type Register.

Chapter 7

Power, Reset, Clock Management

This chapter describes the systems related to power, resets, and clocking management (PRCM).

7.1 Power Management

Power and clock management is flexible to facilitate low-power applications. The following sections describe details for clock and power control. The features in this chapter are embedded and optimized in TI's Power Manager. Please see the SDK documentation for more details.

Low-power consumption and cycling time for a power saving mode has an inverse relationship. The power-saving mode with the lowest power consumption requires the longest time from initiation until that power-saving models enabled, as well as wake-up time back to active mode. Table 7-1 table summarizes the power saving features (VD = Voltage Domain, PD = Power Domain).

The Host M33 can control the device modes to optimize the power consumption. The Host M33 can be either be clock gated (idle) or enter sleep where the Host domain is disabled. The WiFi-BLE domain can be enabled or disabled by Host M33, however WiFi-BLE enter low power mode is managed by the WiFi-BLE and transparent to the host. The following table describes the device power modes:

Table 7-1. Device Power Modes

Mode	Host MCU M33 Domain	Wireless Subsystem Domain	Description
Shutdown	OFF	OFF	Supplies are connected to the device but device is in reset
Host M33 Sleep	Sleep	OFF	Device is in low power mode (RTC+ Memory Retention) Digital & SRAM KA internal supplies are ON. Memories are in retention. All switchable power domains are OFF (Core/AAOD) WiFi-BLE domain is OFF with no memory retention.
	Sleep	Sleep	Device is in low power mode (RTC+ Memory Retention) Digital & SRAM KA internal supplies are ON. Memories are in retention. All switchable power domains are OFF (Core/AAOD) WiFi-BLE domain is sleep with memory retention.
	Sleep	Active	The system is in idle mode - all supplies and clocks are enabled. In this mode the CPU clock is gated while the peripherals or BLE-WiFi Core could be active
Host M33 Idle	Idle	OFF	The system is in active mode - all supplies and clocks are enabled. In this mode the host domain is enabled and initialized including the peripherals however the Host M33 clock is gated. The WiFi-BLE core is OFF.
	Idle	Sleep	The system is in active mode - all supplies and clocks are enabled. In this mode the Host MCU domain is enabled and initialized including the peripherals however the Host M33 clock is gated. The WiFi-BLE is in sleep mode.
	Idle	Active	The system is in active mode - all supplies and clocks are enabled. In this mode the Host MCU domain is enabled and initialized including the peripherals however the Host M33 clock is gated. The WiFi-BLE is active.
Host M33 Active	Active	OFF	The system is in active mode - all supplies and clocks are enabled. In this mode the Host M33 is active while the Wi-Fi BLE is OFF
	Active	Sleep	The system is in active mode - all supplies and clocks are enabled. In this mode the Host M33 is active while the Wi-Fi BLE is in sleep
	Active	Active	The system is in active mode - all supplies and clocks are enabled. In this mode both the Host M33 and WiFi-BLE are active.

7.1.1 Power Supply System

There are multiple voltage levels in use on the device to effectively optimize the power consumption of various modules operating in different power modes. Figure 7-1 shows an overview of the supply system.

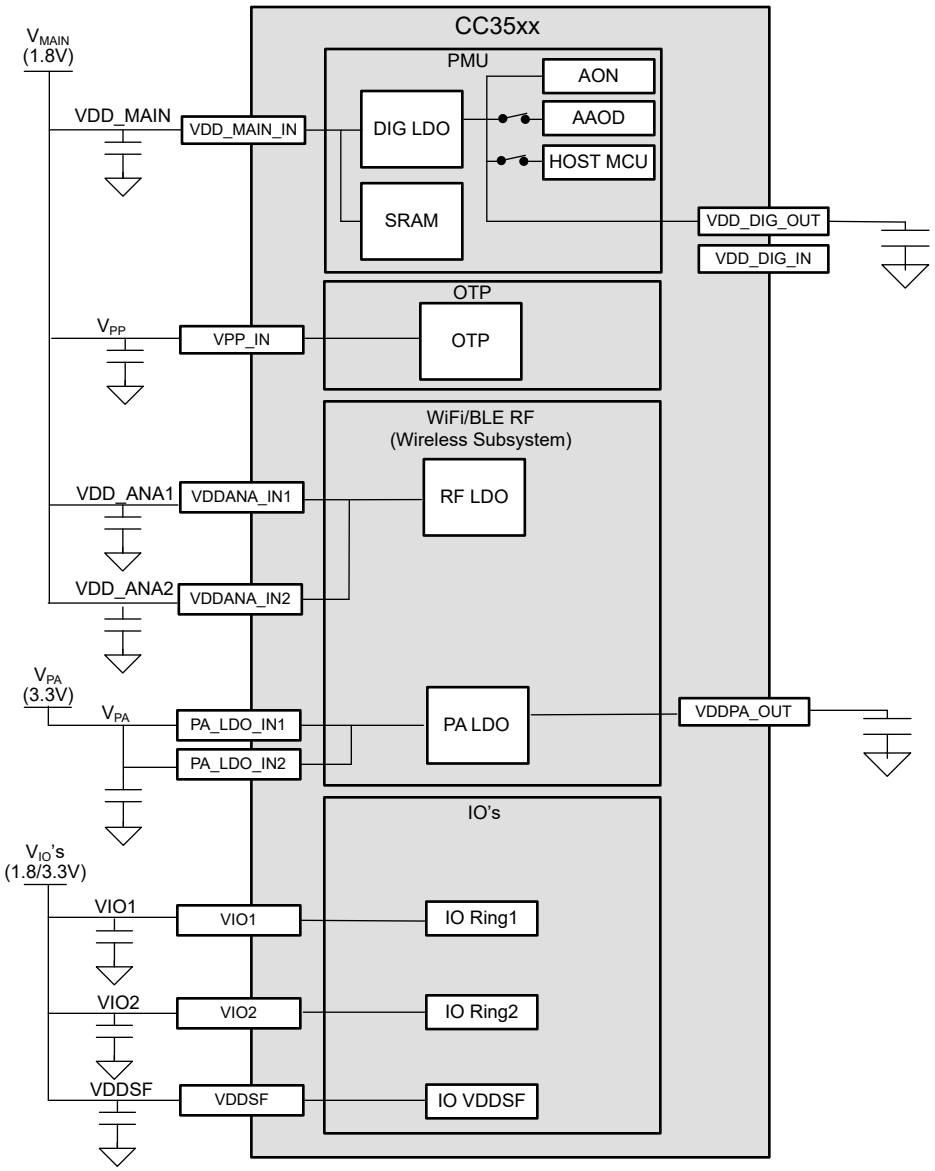

Figure 7-1. Power Supply Subsystem

7.1.1.1 VDD_MAIN

The main supply of the device generating the digital and memories supplies.

7.1.1.2 VIO

This VDDIO supply powers for the split rails IO supply for device GPIOs (VIO1, VIO2). VDDIO split rail I/O supply enables using a different I/O supply rail compared to the main VDDMAIN supply rail. This enables applications to interface with other system components at a different voltage level compared to the main VDDMAIN power supply level.

7.1.1.3 VDDSF

This VDDSF supply powers for the split rails IO supply for external Flash GPIOs only.VDDSF split rail I/O supply enables using a different I/O supply rail compared to the main VDDMAIN supply rail.This enables applications to interface with external Flash at a different voltage level compared tothe main VDDMAIN power supply level.

7.1.1.4 V_{PA}

The input supply to the Power Amplifier of the device.

7.1.2 Power States

The following power states and power state transitions are used in the device:

SHUTDOWN

The lowest power state of the device, SHUTDOWN is entered unconditionally when the reset pin is held low or the supply is below the minimum required. In this state no fast clocks are running, all voltage regulators are disabled and I/Os are in their default state. There is no internal mechanism to allow software to enter SHUTDOWN, nor any software mechanism to allow exit from SHUTDOWN.

SLEEP

SLEEP is the low power state of the device where slow clock is running and RTC and Watchdog timer can be active. The MCU domain is powered off, but all logic in the AON power domain remains on and clocked by slow clock. There are wake-up sources for SLEEP to ACTIVE as described in Section 5.4.3. On SLEEP exit, AAON is powered up again. MCU modules with retention will restore the state they had before SLEEP entry. See Figure 6-3 to see which modules have retention. Modules without retention are reset and need to be reconfigured when exiting SLEEP

IDLE

In IDLE the CPU is in sleep but selected peripherals and subsystems (such as the BLE-WiFi) can be active. In Idle mode, all modules are available and power consumption is highly application dependent.

ACTIVE

Once the reset pin is de-asserted and the minimum supply voltage is supplied, the device enters the ACTIVE power state. The fast clocks and internal LDOs are enabled. Once the digital supply and the internal slow clock (LFOSC) are stable, the cold boot sequence is performed, applying trims to analog circuitry (including oscillators and voltage regulators), memories and turn ON the fast clock of the device. The device boots, MCU is released from reset and start execution. The user application can configure and enable the LFXT or external slow clock. For more information on the boot process see Chapter 10. In the ACTIVE power state, both MCU and AON power domains are powered. Clock gating is used to minimize power consumption. Clock gating to peripherals/subsystems is controlled manually by the CPU.

7.1.3 Power Domains

The device has multiple power domains. The always on (AON) domain, the almost always on (AAOD) domain, the switchable Host MCU domain, and the BLE-WiFi Core domain. The power domains state is determined according to the device power state. See Figure 7-2 below for an overview of the voltage and power partitioning

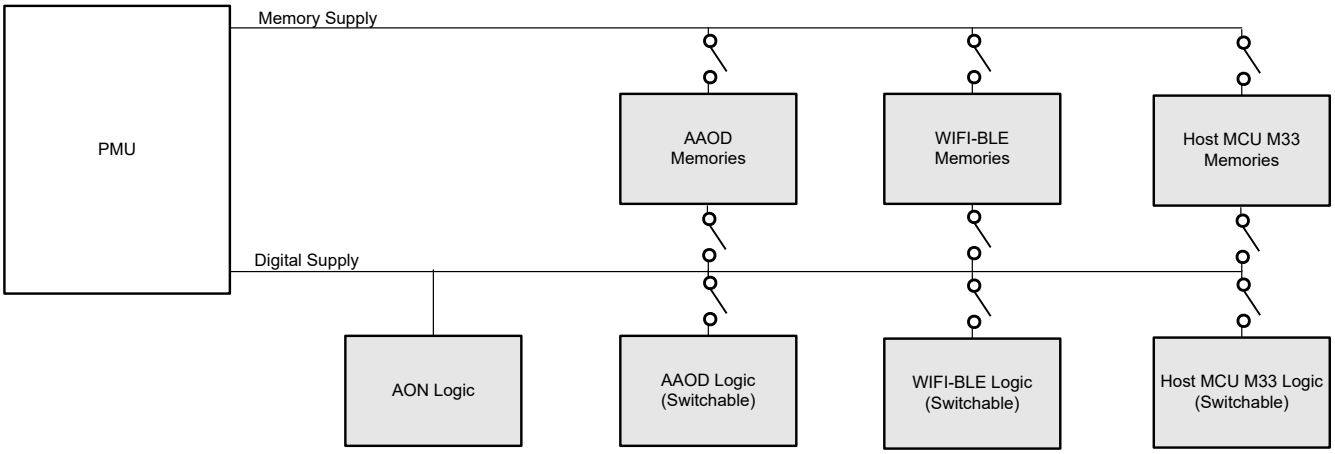

Figure 7-2. CC35xx Power Domains

Table 7-2. CC35xx Power Partitioning

Module	Power Domain	Module Retention During Sleep
ELP (Host MCU)	AON	Retained
PRCM	AON	Retained
IOMUX	AON	Retained
Wireless Subsystem	AON	Retained
DEBUGSS	AON	Retained
RTC	AON	Retained
I-Cache (Host MCU)	AAOD	Retained
D-Cache (Host MCU)	AAOD	Retained
OTFDE (Host MCU)	AAOD	Retained
WRR Arbiter (Host MCU)	AAOD	Retained
µDMA (Host MCU)	AAOD	Not retained
Host DMA	AAOD	Partial retention (only channel allocation)
HSM	AAOD	Not retained
SDIO	AAOD	Not retained
SDMMC	AAOD	Not retained
DCAN	AAOD	Not retained
COEX	AAOD	Not retained
UART	AAOD	Not retained
SPI	AAOD	Not retained
I2C	AAOD	Not retained
GPTIMER	AAOD	Not retained
SYSTIMER	AAOD	Not retained
I2S	AAOD	Not retained
PDM	AAOD	Not retained
ADC	AAOD	Not retained

7.1.4 Brownout (BOR)

The device supports monitoring VDDMAIN to reset the device when supply is below threshold and to boot the device when supply is above threshold.

This feature is mainly for battery powered applications where there is no external entity managing the reset of device and power supply.

The device initiates:

- Reset the Device: VDDMAIN supply < **1.71V** Threshold
- Power up Device: VDDMAIN supply > **1.71V** Threshold

7.1.5 Boot Sequence

The boot process of the Host M33 MCU includes multiple phases including the HW init, FW Init, application code authentication and the last is application code execution. For more information on the CC35xx boot process see Chapter 10. The following diagram describes the boot sequence of the device:

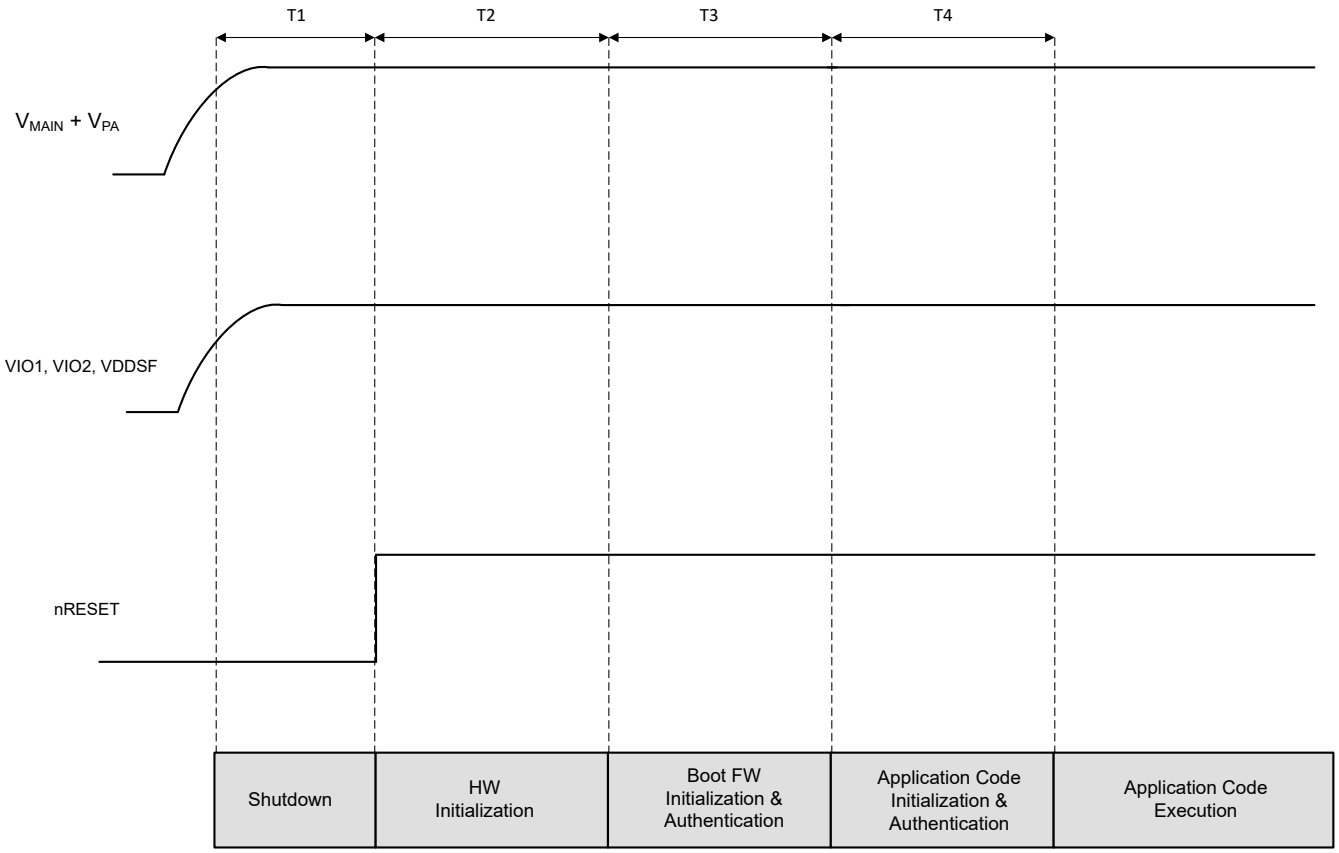

Figure 7-3. CC35xx Boot Sequence

Table 7-3. Boot Sequence Timing

Time	Name	Description	Typ	Units
T1	Supply Settling Time	This depends on the application board power management scheme		
T2	Hardware Wakeup Time	Enabling of the power supply and clocks of the device	20	ms
T3	Boot FW Initialization and authentication(TI's 1st Stage boot (BL))	Boot FW load and execution.This period depends on the boot FW code size.	380	ms
T4	Application Code Authentication(TI's 1st Stage boot (BL2))	The application code authentication.This period depended on the code size.	500	ms

Power Supply Sequencing

The device supports power up due to de-assert of the reset pin or supply voltage VDD_MAIN above threshold.

Power up by reset pin

The device is released from reset by de-asserting the reset pin. For proper operation of the device, perform the recommended power-up sequencing as follows:

1. All supplies (VDD_MAIN_IN, VDD_ANA, VIO_1, VIO_2, VDDSF, V_{PA}) must be available before nReset is released.
2. For an external slow clock, ensure that the clock is stable before nReset is deasserted (high).
3. The nReset pin should be held low for at least 10 us after stabilization of the external power supplies.

Power up when supply above threshold

In this configuration the reset pin needs to be shorted to the VDD_MAIN_IN pin. The VDDSF needs to be shorted to either VDD_MAIN or VIO_1 or VIO_2. The device is released from reset when the VDD_MAIN, VIO_1, VIO_2 and VDDSF supply voltages are above threshold.

It is important to note:

- When either VIO1, VDDSF or VIO2 is 3.3V while the VDDMAIN/VIOs supplies are 1.8V it should be ensured that the 3.3V is available <15ms after VDDMAIN reaches 1.8V. It is expected this will be the normal case in systems where the 1.8V supply is derived from the 3.3V supply.
- When reset is driven from an external source, it can be driven from 1.8V or 3.3V IO independently of VIO1 level.
- When VIO ramps up slowly, the IO will be in undefined state until VIO reaches ~0.7V typical. During this period the IO leakage can be tens of uA.
- IO state is undefined and leakage can be tens of uA when VIO <0.7V.

7.2 Reset

Only a global asynchronous reset is available; no partial or subsystem reset is supported.

Reset can be triggered by:

- RSTN pin
- Power on Reset (POR)
- Rail Voltage Monitor (RVM)
- VDDMAIN Brown-out detector reset
- Debug Subsystem Mailbox (DSSM) Request Reset
- Watchdog reset
- Software reset request
- Debug reset request

The hierarchy of reset signals is as follows:

- RSTN_POR: Everything is reset, everything is disabled
- RSTN Asserted until all reset sources are released, and all regulated and unregulated voltage supplies are above the minimum required levels

Any reset higher in the hierarchy propagates to everything below. Resets are released at least one clock cycle before any clock starts running or synchronously to the clock edge if that is not possible.

7.2.1 Reset Cause

CC35xx HW keeps information on the reset cause. This information is used by the boot code to identify the required boot flow: boot after reset, boot on WiFi enable or due to error/fault event. The reset cause information is also transferred to application FW. The reset cause sources are listed on the table below:

Table 7-4. Reset Cause Sources

Reset Cause	Reset Drive	Reset Level
Reset Line OR POR	Reset Pin OR Power Crossed ~1.3V Threshold	Power On Reset (Cold Reset)
RVML / RVMH	Reset was caused by Low/High side RVM comparator tripping	
Brownout Detection	Power Crossed ~1.6V Threshold	
M33 WD	Watchdog Timer - TH2	Power On Reset
Device Self Reset - Requested by M33	Reset requested by Host CPU - M33	Device AON Reset

7.2.2 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is used to regain control when the system has failed due to a software error or due to the failure of an external device to respond in the expected way during sleep. The WDT supports 2 thresholds: the first (31b) generates an event (this is reserved for TI SW) and the second (23b with 8 bit resolution) generates a reset when a time-out value is reached. The WDT relies on a working LFCLK.

The WDT can be configured using the following sequence of writes and reads in the HOSTMCU_AON.ELPTMREN register: Halt (ELPTMRRST=1) □ Verify halted (Read VAL=0) □ Unhalt (ELPTMRRST=0) □ Reset counter value (ELPTMRLD=1) □ Start (ELPTMRSET) □ Verify started (VAL=1).

The reset bit (ELPTMREN[3] ELPTMRRST) takes precedence over start bit (ELPTMREN[2] ELPTMRSET), if both are set, the timer is halted.

1. WDT Reset Sequence + Un Halt :
   a. Write '1' in HOSTMCU_AON.ELPTMREN[3] ELPTMRRST to stop counting.
   b. Verify ELP is disabled by reading '0' in HOSTMCU_AON.ELPTMREN[0] VAL.
2. Set Timer threshold (threshold 2 only):
   a. HOSTMCU_AON.CFGWDT[31] EN to enable WDT
   b. HOSTMCU_AON.CFGWDT[30:8] THR to set threshold value
3. Un Halt + Start Timer Un halt (Release from stop)
   a. Release the counter from stop counting by writing '0' to HOSTMCU_AON.ELPTMREN[3] ELPTMRRST
   b. Restart counter to value '2' by writing '1' to HOSTMCU_AON.ELPTMREN[16] ELPTMRLD
   c. Start timer by writing '1' to HOSTMCU_AON.ELPTMREN[2] ELPTMRSET. Verify timer is on by reading '1' HOSTMCU_AON.ELPTMREN[0] VAL.

7.3 Clocks

The CC35xx uses two clock domains, fast clock and slow clock.

7.3.1 Fast Clock

The CC35xx uses the fast clock for active MCU functions and peripherals, as well as for WiFi/BLE functions. This clock is generated from an external XTAL running at 52MHz (HFXT).

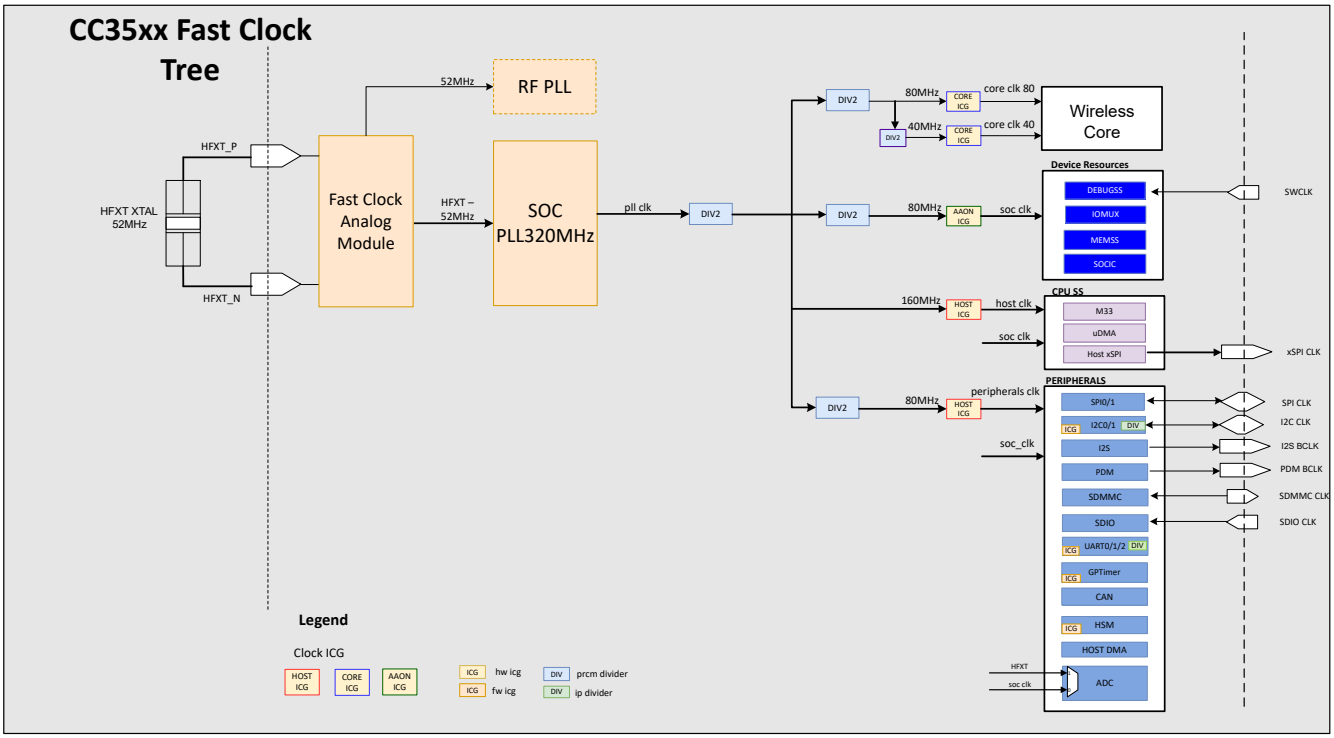

Figure 7-4. Fast Clock Tree

The clock signals shown in the diagram above are described in the table below.

Table 7-5. CC35xx Clock Signals

Clock Name	Frequency	Destination	Clock Gating (HW/SW)	Power State			
				Active	Host Sleep, Wireless Core Active	Host Active, Wireless Core Sleep	Sleep
Device Clocks							
HFXT_P, HFXT_N	52MHz	Fast Clock Analog Module	NA	ON	ON	ON	ON/OFF
PLL_CLK	320MHz	PRCM dividers	HW	ON	ON	ON	OFF
HOST_CLK	160MHz	CPUSS: M33, xSPI, OTFDE, µDMA	HW	ON	OFF	ON	OFF
SOC_CLK	80MHz	Internal resources and peripherals MMR	HW	ON	OFF	ON	OFF
Peripherals Clock	80MHz	Host Peripherals Clock	HW	ON	OFF	ON	OFF
Core CLK 80	80MHz	Wireless Core	HW (at core)	ON	ON	OFF	OFF
Core CLK 40	40MHz	Wireless Core	HW (at core)	ON	ON	OFF	OFF
ADC Conversion CLK	80MHz/52MHz	ADC	SW	ON/OFF	ON/OFF	OFF	OFF
Peripherals Clocks							
SWCLK	20MHz	DEBUGSS	none	NA	NA	NA	NA
SPI CLK	26MHz (peripheral) 40MHz (controller)	SPI (input/output)	none (peripheral) SW (controller)	NA	NA	NA	NA
xSPI CLK	80MHz	xSPI flash/PSRAM (output)	SW	ON/OFF	ON/OFF	OFF	OFF
I2C CLK	100kHz / 400kHz / 1MHz	I2C (input/output)	none	ON/OFF	ON/OFF	OFF	OFF

Table 7-5. CC35xx Clock Signals (continued)

Clock Name	Frequency	Destination	Clock Gating (HW/SW)	Power State			
				Active	Host Sleep, Wireless Core Active	Host Active, Wireless Core Sleep	Sleep
I2S CLK	11kHz - 96kHz	I2S (output)	SW	ON/OFF	ON/OFF	OFF	OFF
PDM BCLK	6MHz	PDM (output)	SW	ON/OFF	ON/OFF	OFF	OFF
SDMMC CLK	40MHz	SD card (output)	SW	ON/OFF	ON/OFF	OFF	OFF
SDIO CLK	40MHz	SDIO (input)	SW	ON/OFF	ON/OFF	OFF	OFF

7.3.2 Slow Clock

The CC35xx uses the slow clock for Sleep functions and certain peripherals. It can be generated externally with an xtal or one-pin oscillator, or generated internally.

7.3.2.1 Slow Clock Overview

The Slow Clock is the initiator clock of the SoC system, and the only active clock in the sleep modes for power saving optimization. The Slow Clock supports several options (modes) of clock sources for different solutions according to relevant use cases and cost wishes.

To enable those modes Slow Clock uses the two Analog IPs: LFXT for the external clock options, and LFOSC for the internal clock option. The default Slow Clock mode is the Internal Slow Clock (generated by LFOSC IP), and in the boot sequence one of the modes is selected for the continuation operation.

The 4 slow clock modes (sources):

1. **Internal Slow Clock Mode (LFOSC)**

   Generates 256kHz clock by dedicated analog IP.
2. **Internal PLL-32kHz Mode**

   32kHz clock generated by SOC PLL (320MHz) from fast clock (see Section 7.3.1). Used for accuracy improvement during active power mode.
3. **External Crystal Mode (LFXT)**

   LFXT analog IP generated 32kHz clock using an external crystal (XTAL) connected to LFXT_P and LFXT_N pins.
4. **External Clock Mode**

   An external device or dedicated one-pin oscilator generates a 32kHz clock, connected to LFXT_P pin.

7.3.2.2 Slow Clock Tree

The slow clock tree in Figure 7-5 shows the configurable connections between the clock sources available for the slow clock.

It contains four main MUXs: M0, M1, M2, M3 (shown below) which are used to configure the clock tree propogation according to the selected mode described in Section 7.3.2.1.

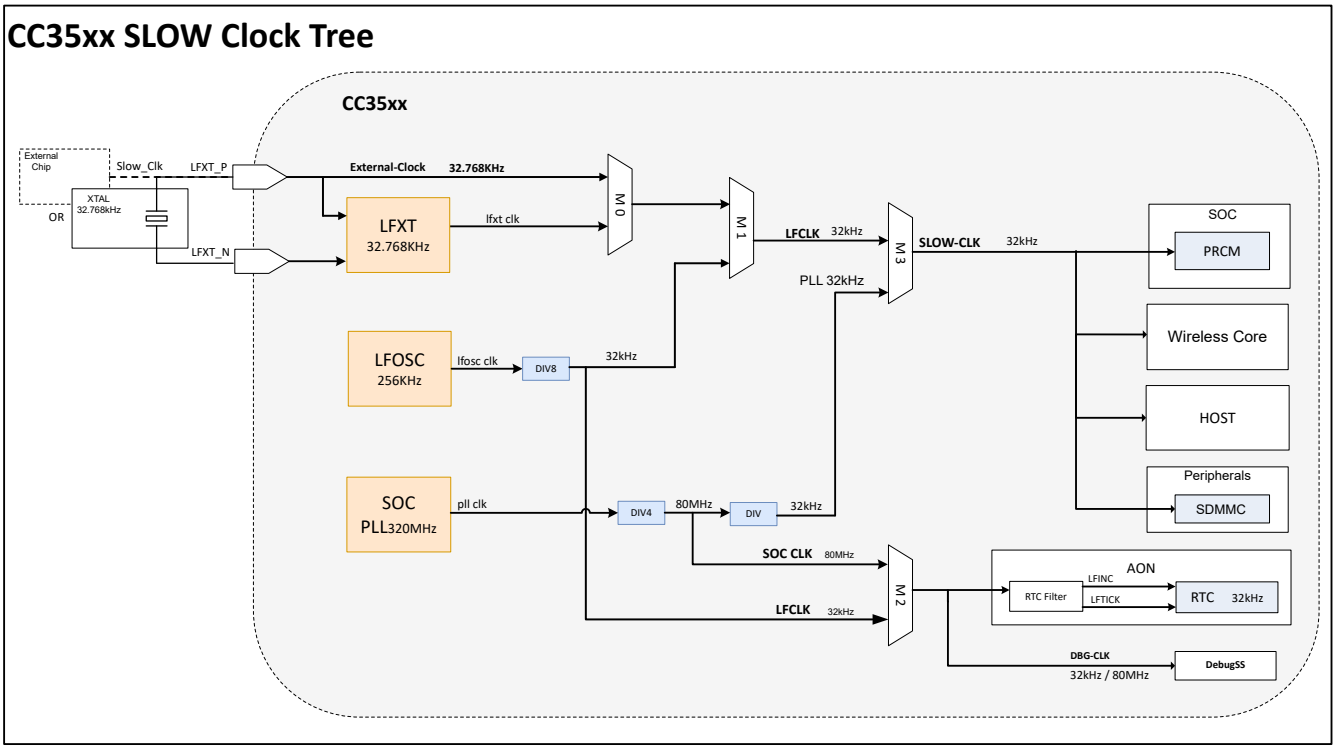

Figure 7-5. Slow Clock Tree

7.3.2.3 Slow Clock Boot Process

There are 4 stages from RESET (Shutdown) to stable Slow Clock.

High level description:

1. RESET - Device is in RESET (Shutdown), Slow Clock is inactive.
2. HW Boot - Upon exit from RESET (device is enabled), the default setting initiated by the HW Boot sets the slow clock to LFOSC mode, used for PRCM functionality.
3. SW Boot - After completion of the HW Boot, the HOST MCU performs a SW sequence to set one of the Slow-Clock functional modes:
   a. The SW sets M0/M1/M2/M3 Muxs in the correct order and timing for smooth transition (i.e. no glitches or RTC accuracy penalty) according to the slow clock mode chosen (see Section 7.3.2.1).
4. Operational: Active / Sleep states - After applying the SW Boot settings, the selected Functional-Mode is remains stable, as long as device is not reset.

7.4 PRCM_AON Registers

Table 7-6 lists the memory-mapped registers for the PRCM_AON registers. All register offset addresses not listed in Table 7-6 should be considered as reserved locations and the register contents should not be modified.

Table 7-6. PRCM_AON Registers

Offset	Acronym	Register Name	Section
1034h	HFLXGRP	Memory Power Control	Section 7.4.1
1038h	HFLXGRPIND	Memory Sharing Status	Section 7.4.2
1054h	HSTATICGRP	Memory Groups Control	Section 7.4.3
1058h	HSTATICGRPIND	Memory Sharing Status	Section 7.4.4
105Ch	LOGHMEMSTA	Memory Status	Section 7.4.5
1060h	CONNSTP	Connectivity Control	Section 7.4.6
2008h	LFXTCTL	Low-Frequency Oscillator Control	Section 7.4.7
2010h	LFOSCEN	Low-Frequency Oscillator Enable	Section 7.4.8
2068h	FCLKDET	Clock Detection Status	Section 7.4.9
2074h	RTCCTL	Real-Time Clock Control	Section 7.4.10
2078h	LFINCCTL	Low Frequency Increment	Section 7.4.11
207Ch	LFCLKSTA	Low-Frequency Clock Status	Section 7.4.12
2080h	LFINCOVR	Time Increment Override	Section 7.4.13
2084h	LFQUALCTL	Frequency Qualification Control	Section 7.4.14
2088h	LFINCCTLI	Time Increment Value	Section 7.4.15
208Ch	SCLKCNT	Slow Clock Counter	Section 7.4.16
2090h	SCLKCNTCTL	Slow Clock Control	Section 7.4.17
2094h	SCLKCNTSTRT	Slow Clock Counter	Section 7.4.18
2098h	SCLKCTL	Slow Clock Control	Section 7.4.19
209Ch	STA	Power Reset Status	Section 7.4.20
20A0h	INTERUPT	Clock Status Flags	Section 7.4.21
20A8h	CRSLPIND	Sleep Status	Section 7.4.22
20ACh	HSLPIND	Controller Sleep Status	Section 7.4.23
20B0h	FNCLKMUXCTL	Clock Selection Control	Section 7.4.24
20B4h	RSTCTL	Reset Control	Section 7.4.25
20B8h	LFOSC	Low Frequency Oscillator	Section 7.4.26
70F4h	PUSHPULEN	PUSH PULL ENABLE cfg option for the clock to the host	Section 7.4.27
7108h	FCLK	Clock Selector Override	Section 7.4.28
710Ch	FCLKDURDLY	Clock Duration Settings	Section 7.4.29
7110h	FREFDET	Frequency Reference Detection	Section 7.4.30
71A8h	MEMGCTLCRSTAT1	Memory Group Control	Section 7.4.31

Complex bit access types are encoded to fit into small table cells. Table 7-7 shows the codes that are used for access types in this section.

Table 7-7. PRCM_AON Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		

Table 7-7. PRCM_AON Access Type Codes (continued)

Access Type	Code	Description
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.4.1 HFLXGRP Register (Offset = 1034h) [Reset = 000FFFFFh]

HFLXGRP is shown in Table 7-8.

Return to the Summary Table.

PSCON Memory Groups Control Host Flex. Applicable only if MODE selected flex as HOST memory. Bank power State When owner IP Active/Sleep (power domain is ON/OFF) 0 - OFF/OFF 1 - Reserved 2 - ON/OFF 3 - ON/RET

Table 7-8. HFLXGRP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-18	PWRSTATE10	R/W	3h	POWER STATE 10 Group 10
17-16	PWRSTATE9	R/W	3h	POWER STATE 9 Group 9
15-14	PWRSTATE8	R/W	3h	POWER STATE 8 Group 8
13-12	PWRSTATE7	R/W	3h	POWER STATE 7 Group 7
11-10	PWRSTATE6	R/W	3h	POWER STATE 6 Group 6
9-8	PWRSTATE5	R/W	3h	POWER STATE 5 Group 5
7-6	PWRSTATE4	R/W	3h	POWER STATE 4 Group 4
5-4	PWRSTATE3	R/W	3h	POWER STATE 3 Group 3
3-2	PWRSTATE2	R/W	3h	POWER STATE 2 Group 2
1-0	PWRSTATE1	R/W	3h	POWER STATE 1 Group 1

7.4.2 HFLXGRPIND Register (Offset = 1038h) [Reset = 00000000h]

HFLXGRPIND is shown in Table 7-9.

Return to the Summary Table.

PSCON Memory Groups Indication Host Flex Applicable only if MODE selected flex as HOST memory. Memory bank from this group is shared 1 - Shared 0 - Not Shared

Table 7-9. HFLXGRPIND Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9	ISSHARED10	R/W	0h	IS SHARED 10 Group 10
8	ISSHARED9	R/W	0h	IS SHARED 9 Group 9
7	ISSHARED8	R/W	0h	IS SHARED 8 Group 8
6	ISSHARED7	R/W	0h	IS SHARED 7 Group 7
5	ISSHARED6	R/W	0h	IS SHARED 6 Group 6
4	ISSHARED5	R/W	0h	IS SHARED 5 Group 5
3	ISSHARED4	R/W	0h	IS SHARED 4 Group 4
2	ISSHARED3	R/W	0h	IS SHARED 3 Group 3
1	ISSHARED2	R/W	0h	IS SHARED 2 Group 2
0	ISSHARED1	R/W	0h	IS SHARED 1 Group 1

7.4.3 HSTATICGRP Register (Offset = 1054h) [Reset = 0BEEFFFFh]

HSTATICGRP is shown in Table 7-10.

Return to the Summary Table.

PSCON Memory Groups Control Host Static. Bank power State When owner IP Active/Sleep (power domain is ON/OFF) 0 - OFF/OFF 1 - Reserved 2 - ON/OFF 3 - ON/RET

Table 7-10. HSTATICGRP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-26	PWRSTAT14	R/W	2h	POWER STATE 14 Group 36
25-24	PWRSTAT13	R/W	3h	POWER STATE 13 Group 35
23-22	PWRSTAT12	R/W	3h	POWER STATE 12 HIF Group 34 - being used as shared memory
21-20	PWRSTAT11	R/W	2h	POWER STATE 11 Group 33
19-18	PWRSTAT10	R/W	3h	POWER STATE 10 Group 32
17-16	PWRSTAT9	R/W	2h	POWER STATE 9 Group 31
15-14	PWRSTAT8	R/W	3h	POWER STATE 8 Group 30
13-12	PWRSTAT7	R/W	3h	POWER STATE 7 Group 29
11-10	PWRSTAT6	R/W	3h	POWER STATE 6 Group 28
9-8	PWRSTAT5	R/W	3h	POWER STATE 5 Group 27
7-6	PWRSTAT4	R/W	3h	POWER STATE 4 Group 26
5-4	PWRSTAT3	R/W	3h	POWER STATE 3 Group 25
3-2	PWRSTAT2	R/W	3h	POWER STATE 2 Group 24
1-0	PWRSTAT1	R/W	3h	POWER STATE 1 Group 23

7.4.4 HSTATICGRPIND Register (Offset = 1058h) [Reset = 00000000h]

HSTATICGRPIND is shown in Table 7-11.

Return to the Summary Table.

Memory bank from this group is shared 1 - Shared 0 - Not Shared

Table 7-11. HSTATICGRPIND Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	ISSHARED4	R/W	0h	IS SHARED 4 Group 26
2	ISSHARED3	R/W	0h	IS SHARED 3 Group 25
1	ISSHARED2	R/W	0h	IS SHARED 2 Group 24
0	ISSHARED1	R/W	0h	IS SHARED 1 Group 23

7.4.5 LOGHMEMSTA Register (Offset = 105Ch) [Reset = 00000000h]

LOGHMEMSTA is shown in Table 7-12.

Return to the Summary Table.

Logic Host Memory Status

Table 7-12. LOGHMEMSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-0	AONIN	R	0h	Host Memory AONIN indication

7.4.6 CONNSTP Register (Offset = 1060h) [Reset = 00000001h]

CONNSTP is shown in Table 7-13.

Return to the Summary Table.

Connectivity Stop

Table 7-13. CONNSTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	SET	R/W	1h	'1' - Connectivity Stop '0' - Connectivity Start

7.4.7 LFXTCTL Register (Offset = 2008h) [Reset = 00000000h]

LFXTCTL is shown in Table 7-14.

Return to the Summary Table.

LFXT CONTROL

Table 7-14. LFXTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-22	AMPREGITRIM	R/W	0h	AMPLITUDE REGULATION CURRENT TRIM Amplitude regulation current trim
21-17	IBIASRTRIM	R/W	0h	IBIAS RTRIM Constant gm bias resistor ladder trim
16-12	AMPREGRTRIM	R/W	0h	AMPLITUDE REGULATION RESISTOR TRIM Amplitude regulation resistor ladder trim
11-7	IBIASITRIM	R/W	0h	IBIAS ITRIM Constant gm bias current trim
6	AMPREGEN	R/W	0h	AMPLITUDE REGULATION ENABLE Enable amplitude regulation
5	BOOSTMODE	R/W	0h	BOOST MODE Start-up pulse for bias current generation
4	BYPASS	R/W	0h	Bypass LFXT
3	CPEN	R/W	0h	Comparator (slicer) enable
2	CPHPMODEN	R/W	0h	COMP HP MODE EN Comparator high current mode
1	IBIASEN	R/W	0h	Enable constant-gm bias
0	OSCEN	R/W	0h	Oscillator core enable

7.4.8 LFOSCEN Register (Offset = 2010h) [Reset = 00000000h]

LFOSCEN is shown in Table 7-15.

Return to the Summary Table.

LFOSC ENABLE

Table 7-15. LFOSCEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	GOOD	R	0h	CLK GOOD LFOSC clock good indication based on clock qualification logic

7.4.9 FCLKDET Register (Offset = 2068h) [Reset = 00000000h]

FCLKDET is shown in Table 7-16.

Return to the Summary Table.

FAST CLK DETECTION primary clock detection result

Table 7-16. FCLKDET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	OVERLAP	R	0h	Not in use. '1' - if FREF value is overlapping at 40/48MHz or 48/52MHz
4	FAILED	R	0h	fast clock detection FSM failed counter was no in any FREQ boundaries '1' - failed '0' - OK
3	RESERVED	R	0h	Reserved
2-0	FREQVAL	R	0h	FAST CLK FREQUENCY DETECTION VALUE fast clock detection value : 0: 10MHz 1: 26MHz 2: 40MHz 3: 52MHz

7.4.10 RTCCTL Register (Offset = 2074h) [Reset = 00000002h]

RTCCTL is shown in Table 7-17.

Return to the Summary Table.

RTC CONTROL

Table 7-17. RTCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	LFTICKSTA	R	0h	LFTICK STATE '1101' - Real LFTICK '1100' - Gate RTC CLK '1110' - Force LFTICK high '1010' - Switch RTC CLK low '0010' - Standby '0000' - Force LFTICK low '0100' - switch RTC CLK high '0101' - Ungate RTC CLK
7-2	RESERVED	R	0h	Reserved
1	DISIMMINENT	R/W	1h	NOT USED - DO NOT CHANGE VALUE '1' - disables imminent option towards SYSTIMER '0' - enables imminent
0	LFTICKSEL	R/W	0h	LFTICK SELECT '1' - use real LFTICK '0' - use fake LFTICK

7.4.11 LFINCCTL Register (Offset = 2078h) [Reset = 00000000h]

LFINCCTL is shown in Table 7-18.

Return to the Summary Table.

LFINC CONTROL Low frequency time increment control

Table 7-18. LFINCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PREVSTBY	R/W	1h	PREVENT STANDBY Controls if the LFINC filter prevents STANDBY entry until settled. 0h = Disable. Do not prevent STANDBY entry. 1h = Enable. Prevent STANDBY entry.
30-10	RESERVED	R	0h	Reserved
9-8	FKLFTICKSEL	R/W	0h	FAKE LFTICK SELECTOR '00' - default - LOKI + corner case scenario '01' - first integration '10' - LOKI '11' - always enable 0h = Restart gearing on large error. Fewer false restarts, slower response on small frequency shifts. 1h = Middle value towards LARGE. 2h = Middle value towards SMALL. 3h = Restart gearing on small error. Potentially more false restarts, faster response on small frequency shifts.
7	STOPGEAR	R/W	0h	STOP GEAR Controls the final gear of the LFINC filter. 0h = Lowest final gear. Best settling, but less dynamic frequency tracking. 1h = Highest final gear. Best dynamic frequency tracking, but higher variation in filter value.
6-5	ERRTHR	R/W	0h	ERROR THRESHOLD Controls the threshold for gearing restart of the LFINC filter. Only effective if [GEARRSTRT] is not ONETHR or TWOTHR. 0h = Restart gearing on large error. Fewer false restarts, slower response on small frequency shifts. 1h = Middle value towards LARGE. 2h = Middle value towards SMALL. 3h = Restart gearing on small error. Potentially more false restarts, faster response on small frequency shifts.
4-3	GEARRSTRT	R/W	2h	GEAR RESTART Controls gearing restart of the LFINC filter. 0h = Never restart gearing. Very stable filter value, but very slow response on frequency changes. 1h = Restart gearing when the error accumulator crosses the threshold once. 2h = Restart gearing when the error accumulator crosses the threshold twice in a row.
2	SOFTRSTRT	R/W	1h	SOFT RESTART Use a higher gear after re-enabling / wake-up. The filter will require 16-24 LFCLK periods to settle (depending on [STOPGEAR]), but may respond faster to frequency changes during STANDBY. 0h = Don't use soft gearing restarts 1h = Use soft gearing restarts
1-0	RESERVED	R	0h	Reserved

7.4.12 LFCLKSTA Register (Offset = 207Ch) [Reset = 00000000h]

LFCLKSTA is shown in Table 7-19.

Return to the Summary Table.

LFCLK STATUS Low-frequency clock status

Table 7-19. LFCLKSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GOOD	R	0h	Low frequency clock good Note: This is only a coarse frequency check based on [LFQUALCTL.*]. The clock may not be accurate enough for timing purposes.
30-26	RESERVED	R	0h	Reserved
25	FLTSETLED	R	0h	FILTER SETTLED LFINC filter is running and settled.
24	LFTICKSRC	R	0h	Source of LFTICK. 0h = LFTICK generated from the selected LFCLK 1h = LFTICK generated from CLKULL (LFCLK not available)
23-22	LFINCSRC	R	0h	Source of LFINC used by the RTC. This value depends on LFINCOVR.OVERRIDE, LF clock availability, HF tracking loop status and the device state (ACTIVE/STANDBY). 0h = Using measured value. This value is updated by hardware and can be read from [LFINC]. 1h = Using filtered / average value. This value is updated by hardware and can be read and updated in LFINCCTLI. 2h = Using override value from LFINCOVR.LFINC 3h = Using FAKE LFTICKs with corresponding LFINC value.
21-0	LFINC	R	0h	Measured value of LFCLKSTAT_LFINC. Given in microseconds with 16 fractional bits. This value is calculated by Hardware. It is the LFCLK period according to CLKULL cycles.

7.4.13 LFINCOVR Register (Offset = 2080h) [Reset = 00000000h]

LFINCOVR is shown in Table 7-20.

Return to the Summary Table.

LFINC OVERRIDE Low frequency time increment override control

Table 7-20. LFINCOVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OV	R/W	0h	Override LF increment Use the value provided in [LFINC] instead of the value calculated by Hardware.
30-22	RESERVED	R	0h	Reserved
21-0	LFINC	R/W	0h	LF increment value This value is used when [OVERRIDE] is set to 1. Otherwise the value is calculated automatically.

7.4.14 LFQUALCTL Register (Offset = 2084h) [Reset = 00000000h]

LFQUALCTL is shown in Table 7-21.

Return to the Summary Table.

Low frequency clock qualification control

Table 7-21. LFQUALCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-8	MAXERR	R/W	20h	Maximum LFCLK period error. Value given in microseconds, 3 integer bits + 3 fractional bits.
7-0	CONSEC	R/W	64h	Number of consecutive times the LFCLK period error has to be smaller than [MAXERR] to be considered 'good'. Setting this value to 0 will bypass clock qualification, and the 'good' indicator will always be 1.

7.4.15 LFINCCTLI Register (Offset = 2088h) [Reset = 00000000h]

LFINCCTLI is shown in Table 7-22.

Return to the Summary Table.

Low frequency time increment value

Table 7-22. LFINCCTLI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0h	Reserved
21-0	INT	RH/W	001E8480h	Increment override value write opt SW and HW can write this value Integral part of the LFINC filter. This value is updated by Hardware to reflect the current state of the filter. It can also be written to change the current state.

7.4.16 SCLKCNT Register (Offset = 208Ch) [Reset = 00000000h]

SCLKCNT is shown in Table 7-23.

Return to the Summary Table.

SLOW CLK COUNT

Table 7-23. SCLKCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Reserved
22-16	PERVAL	R	0h	PERIOD VALUE slow CLK current value. bounds are 0 to slow_clk_counter_period
15	RESERVED	R	0h	Reserved
14-0	DET	R	0h	FAST CLK DETECTION COUNTER VALUE Counter results for 4 slow clock freq lower upper (MHz) (dec) (dec) 10 1190 1503 26 3094 3908 40 4760 6012 52 6188 7815

7.4.17 SCLKCNTCTL Register (Offset = 2090h) [Reset = 0000000Ch]

SCLKCNTCTL is shown in Table 7-24.

Return to the Summary Table.

SLOW CLOCK COUNTER CONTROL

Table 7-24. SCLKCNTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	RESULTVAL	R	0h	RESULT VALID read clear pulse Determine whether the measurement is in progress or done: 0x0 - In progress (Relevant in one shot only) 0x1 - Done (when finish measurement and result ready)
23-9	RESULT	R	0h	RESULT Slow Clock counter result
8-2	PER	R/W	3h	PERIOD Determine the Slow clock counter period (Slow Clock cycles), 1 - 128. '0' - 1 CLK cycle '1' - 2 CLK cycles '2' - 3 CLK cycles ... '127' - 128 CLK cycles
1-0	MODE	R/W	0h	MODE Determine the Slow clock counter mode- 0x3 - Reserved 0x2 - Periodic 0x1 - One Shot 0x0 - Disable

7.4.18 SCLKCNTSTRT Register (Offset = 2094h) [Reset = 00000000h]

SCLKCNTSTRT is shown in Table 7-25.

Return to the Summary Table.

SLOW CLK COUNT START KICK

Table 7-25. SCLKCNTSTRT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EN	W	0h	ENABLE write clear start the FREQUENCY DETECTION. MEM_SLOW_CLK_COUNTER_MODE should be set prior to the start indication

7.4.19 SCLKCTL Register (Offset = 2098h) [Reset = 00000000h]

SCLKCTL is shown in Table 7-26.

Return to the Summary Table.

SLOW CLK CONTROL

Table 7-26. SCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	DETGOOD	R	0h	DETECTION GOOD '1' - means 5 edges detected of LFXT/EXT/XTAL
3	GOOD	R/W	0h	'1' - set LFXT CLK good
2	P32CLKSEL	R/W	0h	PLL CLOCK SELECTOR '0' - LFCLK (real tick should be selected) '1' - PLL32 CLK (fake tick should be selected)
1	SDIVCLKSEL	R/W	0h	SLOW CLOCK DIVISION SELECTOR 1 - select LFXT/EXT/XTAL CLK DIV 8 0 - select LFXT/EXT/XTAL CLK
0	LFOSCSEL	R/W	0h	LFOSC SELECTOR 0 - select RCOSC 1 - select LFXT/EXT/XTAL

7.4.20 STA Register (Offset = 209Ch) [Reset = 00000000h]

STA is shown in Table 7-27.

Return to the Summary Table.

PRCM STATUS

Table 7-27. STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	XTALMOD	R	0h	XTAL MODE '1' - XTAL mode '0' - TCXO External mode
0	FCLKDETFAIL	R	0h	FAST CLK DETECTIOn FAILED '1' - FREF detection failed

7.4.21 INTERUPT Register (Offset = 20A0h) [Reset = 00000000h]

INTERUPT is shown in Table 7-28.

Return to the Summary Table.

[0]- indication at slow CLK calibration for one shot mode. [1] - lfinc_updated [2] - lfinc_gearing_restart [3] - lfclk_oor [4] - lfclk_loss [5] - NU [6] - NU [7] - NU

Table 7-28. INTERUPT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	IRQSTABM	R	0h	IRQs indication after Mask
15-8	IRQBM	R/W	0h	PRCM IRQ mask option
7-0	IRQSTARAW	R	0h	PRCM IRQ Clear indication and raw status read clear

7.4.22 CRSLPIND Register (Offset = 20A8h) [Reset = 00000000h]

CRSLPIND is shown in Table 7-29.

Return to the Summary Table.

CORE SLEEP INDICATION

Table 7-29. CRSLPIND Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CTLSTAT	R	0h	CONTROL STATE '1' - CORE is SLEEP '0' - CORE is in ACTIVE or gets into ACTIVE

7.4.23 HSLPIND Register (Offset = 20ACh) [Reset = 00000000h]

HSLPIND is shown in Table 7-30.

Return to the Summary Table.

HOST SLEEP INDICATION

Table 7-30. HSLPIND Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CTLSTAT	R	0h	CONTROL STATE '1' - HOST is SLEEP '0' - HOST is in ACTIVE or gets into ACTIVE

7.4.24 FNCLKMUXCTL Register (Offset = 20B0h) [Reset = 00000000h]

FNCLKMUXCTL is shown in Table 7-31.

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PRCM functional selection towards FAST CLK DETECTION '00000' - prcm_fast_clock 'xxx01' - ospr_hsm_tst_fro_clk_out 'xxx10' - clk_gpadc_clk 'xxx11' - fref_2m_socpll_1p8v 'xx100' - rf_pll_divided_clk '01000' - src_clk_40 '10000' - lfxt / xtal / ext '11000' - rcosc

Table 7-31. FNCLKMUXCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-3	SEL	R/W	0h	Fast CLK detection selector MEM_DBG_CLK_SEL should be set 3'b0 for this reg to take place '00' - prcm_fast_clock. '01' - src_clk_40 '10' - lfxt / xtal / ext '11' - rcosc
2-0	DBGCLKSEL	R	0h	Debug and Fast CLK detection selector 'x00' - prcm_fast_clock. 'x01' - ospr_hsm_tst_fro_clk_out 'x10' - clk_gpadc_clk 'x11' - fref_2m_socpll_1p8v '100' - rf_pll_divided_clk

7.4.25 RSTCTL Register (Offset = 20B4h) [Reset = 00000000h]

RSTCTL is shown in Table 7-32.

Return to the Summary Table.

RESET CONTROL

Table 7-32. RSTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	SOCAON	W	0h	SOC AON write clear '1' - set reset

7.4.26 LFOSC Register (Offset = 20B8h) [Reset = 00000000h]

LFOSC is shown in Table 7-33.

Return to the Summary Table.

LFOSC OVERRIDE STATUS

Table 7-33. LFOSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Reserved
22	OVOSCSTOPEN	R/W	0h	OVERRIDE OSC STOP EN LFOSC STOP enable override value
21	OVOSCEN	R/W	0h	OVERRIDE OSC EN LFOSC enable override value
20	SELOVOSCEN	R/W	0h	SELECTOR OVERRIDE OSC ENABLE LFOSC enable override select
19-13	OVRESTRIMVAL	R/W	0h	OVERRIDE RESISTOR SELECTOR VALUE LFOSC RES trim override value
12	SELOVRESTRIM	R/W	0h	SELECTOR OVERRIDE RESISTOR TRIM LFOSC RES trim override select
11-5	FSRESTRIM	R	0h	FUSE RESISTOR TRIM Analog band gap rtrimfuse value for LFOSC rtrim
4-3	OVFSELVAL	R/W	0h	OVERRIDE FSEL SELECTOR VALUE LFOSC frequency trim override value
2	SELOVFSEL	R/W	0h	SELECT OVERRIDE FSEL LFOSC frequency trim override select
1-0	FSFSEL	R	0h	LFOSC frequency trim value

7.4.27 PUSHPULEN Register (Offset = 70F4h) [Reset = 00000000h]

PUSHPULEN is shown in Table 7-34.

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PUSH PULL ENABLE cfg option for the clock to the host

Table 7-34. PUSHPULEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	VAL	R/W	0h	'1' - enables push pull

7.4.28 FCLK Register (Offset = 7108h) [Reset = 00000840h]

FCLK is shown in Table 7-35.

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fast CLK control over selectors and overrides

Table 7-35. FCLK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	FSMREQIN	R	1h	primary clock request indication to FSM
10	OVREQGZ	R/W	0h	fast CLK request gz override Override CLK req to pad (GZ)
9	SELOVREQGZ	R/W	0h	fast CLK request gz select Override CLK req to pad (GZ)
8	OVREQOUT	R/W	0h	fast CLK request out override Override CLK req to pad (A)
7	SELOVREQOUT	R/W	0h	fast CLK request out select Override CLK req to pad (A)
6	VAL	R	1h	primary clock valid indication status
5	OVVAL	R/W	0h	OVERRIDE VALUE fast CLK valid override Override fref valid
4	SELOVVAL	R/W	0h	SELECT OVERRIDE VALUE fast CLK valid select Override fref valid
3-0	RESERVED	R	0h	Reserved

7.4.29 FCLKDURDLY Register (Offset = 710Ch) [Reset = 00000001h]

FCLKDURDLY is shown in Table 7-36.

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Primary TMUX CFG

Table 7-36. FCLKDURDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	STOP	R/W	1h	time (sclk) from end of CLK_STOP state elapse to CLK_OFF '0' - bypass '1' - 1 + 8 sclks delay ~250us '2' - 1 + 16 sclks delay ~500us '3' - 1 + 32 sclks delay ~1ms

7.4.30 FREFDET Register (Offset = 7110h) [Reset = 00000002h]

FREFDET is shown in Table 7-37.

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FREF DETECTION

Table 7-37. FREFDET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-1	OV	R/W	1h	0: 10MHz 1: 26MHz 2: 40MHz 3: 52MHz
0	SELOV	R/W	0h	'1' - fref detection value to pll sharing will be override '0' - fast CLK fsm (fref) value is selected

7.4.31 MEMGCTLCRSTAT1 Register (Offset = 71A8h) [Reset = FFFFFFFFh]

MEMGCTLCRSTAT1 is shown in Table 7-38.

Return to the Summary Table.

MEMORY GROUP CONTROL CORE STATIC 1 Bank power State When owner IP Active/Sleep (power domain is ON/OFF) 0 - OFF/OFF 1 - Reserved 2 - ON/OFF 3 - ON/RET

Table 7-38. MEMGCTLCRSTAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-22	PWRSTA12	R/W	3h	POWER STATE 12 Group 22
21-20	PWRSTA11	R/W	3h	POWER STATE 11 Group 21
19-18	PWRSTA10	R/W	3h	POWER STATE 10 Group 20
17-16	PWRSTA9	R/W	3h	POWER STATE 9 Group 19
15-14	PWRSTA8	R/W	3h	POWER STATE 8 Group 18
13-12	PWRSTA7	R/W	3h	POWER STATE 7 Group 17
11-10	PWRSTA6	R/W	3h	POWER STATE 6 Group 16
9-8	PWRSTA5	R/W	3h	POWER STATE 5 Group 15
7-6	PWRSTA4	R/W	3h	POWER STATE 4 Group 14
5-4	PWRSTA3	R/W	3h	POWER STATE 3 Group 13
3-2	PWRSTA2	R/W	3h	POWER STATE 2 Group 12
1-0	PWRSTA1	R/W	3h	POWER STATE 1 Group 11

7.5 PRCM_SCRATCHPAD Registers

Table 7-39 lists the memory-mapped registers for the PRCM_SCRATCHPAD registers. All register offset addresses not listed in Table 7-39 should be considered as reserved locations and the register contents should not be modified.

Table 7-39. PRCM_SCRATCHPAD Registers

Offset	Acronym	Register Name	Section
1000h	LINE2	Scratch Register 2	Section 7.5.1

Complex bit access types are encoded to fit into small table cells. Table 7-40 shows the codes that are used for access types in this section.

Table 7-40. PRCM_SCRATCHPAD Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.5.1 LINE2 Register (Offset = 1000h) [Reset = 00000000h]

LINE2 is shown in Table 7-41.

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PRCM SCRATCHPAD 2 m33 messages which should survive AON Reset: OTA info -number of bits? Critical error types + indication if reset applied for this error- number of bits?

Table 7-41. LINE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	VALUE LINE 2 Scratch pad line 2

Chapter 8

Memory Subsystem (MEMSS)

This chapter describes the Memory Subsystem (MEMSS), which includes the internal memories and external memory interface.

8.1 Introduction

The CC35xx device supports on-chip and off-chip memories. Memories are used for execution, data and non-volatile memory. The on-chip memory includes SRAM, and the off-chip memories supported are serial Flash (external or stacked) and serial PSRAM (stacked only).

SRAM is used for execution and data. It is divided into instruction and data partitions, as well as secure and non-secure. The instruction memory partition is split into Instruction Tightly Coupled Memory (ITCM) and Instruction Cache memory (I-Cache). I-Cache allows for execution from Flash and the PSRAM (Refer to current sofwate development kit (SDK) for support). Data memory is divided into Data Tightly Coupled Memory (DTCM) and non-TCM (DMEM), as well as Data Cache Memory (D-Cache). The D-Cache is designed to access the PSRAM.

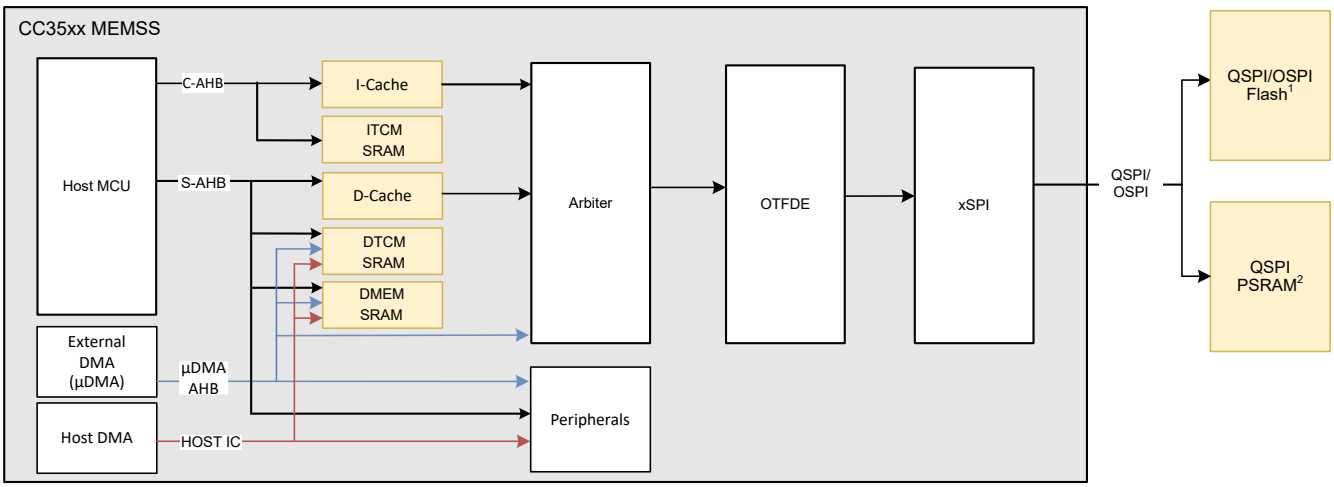
Flash is non-volatile memory used for execution and for data storage. The PSRAM is used predominantly as data storage.

Each of the memories can be accessed by the M33 MCU, µDMA and the Host DMA. The µDMA is used for data transfer between the external Flash/PSRAM and on-chip SRAM. The host DMA is used for data transfer between peripherals and the device's on-chip SRAM.

Note

In this document the flash and PSRAM is considered "external" because it is external memory from the host MCU. The flash can be stacked inside the physical package or connected external to the IC via the xSPI pins. The PSRAM is only available stacked.

The following diagram describes the device memories and which can access it:



1. Off chip/stacked depends on device version
2. Optional stacked PSRAM depends on device version

Figure 8-1. CC35xx Memory Subsystem

The properties of the available memories are listed in the table below:

Memory	Description	Size (1)	CLK	Secure/Non-Secure partition
Internal Memories				
I-Cache	Instruction Cache Memory	32kB / 64kB configurable	160MHz	Not required. Supported by M33 trust-zone (accessed by M33 only)
ITCM	Instruction Tightly Coupled Memory	32kB / 0 configurable	160MHz	Supported

Memory	Description	Size [1]	CLK	Secure/Non-Secure partition
D-Cache	Data Cache Memory	0 / 32kB / 64kB configurable	160MHz	Not required. Supported by M33 trust-zone (accessed by M33 only)
DTCM	Data Tightly Coupled Memory	128kB / 96kB / 64kB configurable	160MHz	Supported
DMEM	Data Memory	256kB configurable	80MHz	Supported
External Memories				
Flash	External Flash	Up to 64MB (8MB executable)	xSPI I/F	Supported
PSRAM	Stacked PSRAM	Up to 64MB	xSPI I/F	Supported

(1) The different options of the memory size (signalled by the '/') correspond to the different memory mode options in Table 8-1.

8.2 SRAM

The system static RAM (SRAM) is split into DTCM (Data Tightly Coupled Memory) and DMEM (Data Non-Tightly Coupled Memory) for data and ITCM (Instruction Tightly Coupled Memory) for execution.

The device has up to 1024 KB of on-chip SRAM with retention in all power modes except Shutdown. Data can be transferred to and from the SRAM using the host DMA and µDMA controllers.

Different memory modes with different allocations of memory can be defined at boot. The following table describes the memory assignment on each memory mode supported by the device:

Table 8-1. Memory Modes

Mode	Memory Mode	I-Cache	ITCM	D-Cache	DTCM	DMEM
0	Baseline (Full Feature Set)	32/64 kB	32/0 kB	0 / 32 / 64kB	128 / 96 / 64kB	512kB
5	No BLE, Extend M33 Data	32/64 kB	32/0 kB	0 / 32 / 64kB	128 / 96 / 64kB	576kB
1-4	TI Internal Modes	-	-	-	-	-

Note

I-Cache + ITCM and D-Cache + DTCM szie options can be configured independently of the memory mode described in the table above.

The user can decide if to use all or part of the 64kB I-Cache memory as ITCM, in the following configurations:

1. 32kB I-Cache + 32kB ITCM
2. 64kB I-Cache + 0kB ITCM

The user can decide if to use all or part of the 128kB DTCM memory as D-Cache, in the following configurations:

1. 128kB DTCM + 0kB D-Cache
2. 96kB DTCM + 32kB D-Cache
3. 64kB DTCM + 64kB D-Cache

8.3 D-Cache

The Data Cache (D-Cache) supports accessing the PSRAM, which is partitioned into cacheable and non-cacheable regions.

The D-Cache memory size allocation can be determined at boot and is locked by internal security. For the relevant memory allocations see Table 8-2.

Table 8-2. D-Cache Modes

Mode	D-Cache	DTCM
All Non-Cacheable	0kB	128kB
Baseline D-Cache	32kB	96kB
Enhanced D-Cache	64kB	64kB

The data access to cache can be either 1/2/4 Bytes either aligned/unaligned, for both cacheable and non-cacheable regions.

PSRAM Cacheable Regions

The D-cache supports defining the cacheable and non cacheable regions in the PSRAM with the following parameters:

- Maximum cacheable region is 8MB
- The resolution for cacheable vs non-cacheable is 4KB.

Access to both cacheable and non-cacheable regions will be through the D-cache.

- Access to non-cacheable regions (Read and Write) can be byte/word aligned/unaligned. The memory access will translate to the external memory directly with no allocation in D-Cache.
- Access to cacheable regions:
  - Read Hit behavior - Read from cache (Read Cache only)
  - Read Miss behavior - Read Allocate (Read line from PSRAM and allocate line)
  - Write Hit Policy - Write Back (WB) (Updated Cache line only + Dirty bit) Dirty bit is set, and the updated line will be stored in PSRAM only on block replacement
  - Write Miss policy - Write Allocate (WA) (Read line from PSRAM and allocate line with the new data, mark as Dirty)

Flush and Invalidate

The D-Cache supports Flush and Invalidate requests to when updating the D-Cache data. Flush is used when the D-cache needs to update the PSRAM with all Dirty bits. Invalidate is used when the D-Cache needs to be cleared and restarted without updating the PSRAM.

8.4 Flash

The flash block provides programmable, nonvolatile program memory for the device. Up to 64MB of flash memory is supported.

The flash can be external to the CC35xx or stacked, depending on device variant. In addition to holding program code, constants and OTA, the nonvolatile memory allows the application to save data that must be preserved so that the data is available after restarting the device. Using this feature lets the user use saved network-specific data and avoids the need for a full start-up and network find-and-join process.

8.5 PSRAM

The PSRAM block provides an extended RAM memory for the device. Up to 64MB of flash memory is supported. The PSRAM is available in stacked device variants. This memory is not preserved so the data is not available after restarting the device.

8.6 XiP Memory Access

The device supports Flash/PSRAM interface (XIP) and supports the following features:

- Encrypt/Decrypt external memory data (flash only)
- Logical to physical address translator
- Secured/non-secured partitioning

8.6.1 OTFDE

The On-the-Fly Decryption Encryption (OTFDE) IP is primarily intended to support on-the-fly decryption of a code fetched from external serial Flash via Execute-In-Place (XIP) mode. The OTFDE is designed to provide system memory directly based on the fly encrypt/decrypt services. In addition, support for the bypass is provided.

At the Host-MCU level, the OTFDE IP is part of the access chain, along with the cache controller and xSPI controller IPs, for storing/fetching code and data to/from external memory devices; Flash and optionally PSRAM. The external memories are split into logical memory regions based on the device type, managed content (code/data) and the required security level (encrypted/plaintext). System consumers of the OTFDE services include the Instruction cache for fetching code hosted on the external serial flash and Data (SW) and µDMA for storing and retrieving data on an external serial flash and PSRAM.

OTFDE supports the following features:

- On the On-the-fly AES-128 encryption with external memory
  - Decryption of memory-mapped code execution from external serial flash
  - Decryption/Encryption of memory-mapped NV data from external serial flash
  - Encryption bypass support
  - Address based memory region mapping
- Minimum four independent memory-mapped regions
  - Non overlapped regions
  - Minimum 4kB region granularity
  - Per region unique KEY+IV management
  - Write access privilege enforcement
- Security
  - AES-CTR-based encryption with 128-bit keystream buffers support (pipeline rate alignment with instruction/data xSPI operation)
  - Encryption confidentiality management with access enforcement (trust zone) support
  - "Zeroisation" support
  - Write Lock Region Configuration
  - Read/Write access policing
  - IV policy management of Code/NVS/ Data regions

8.6.2 xSPI

The xSPI Controller is a serial interface that allows communication on four or eight data lines between the CC35xx host MCU (M33) and an external Serial NOR flash device memory. The xSPI supports the traditional SPI (serial peripheral interface) as well as the QSPI mode which allows communication on 4 lines, and the OSPI mode which allowed communication on 8 lines.

The xSPI supports the following features:

- XIP Mode selection and configuration
- Errors/events/status reports
- Data interface
  - Single/Burst incremental
  - Single outstanding transaction
  - Bus Master
  - Direct memory-mapped access only

- External Flash/PSRAM Interface:
  - SDR/DDR
  - 40/80MHz
  - Quad/Octal Data Lines
  - DQS

8.6.3 Topology

The device supports the external/stacked Flash and/or PSRAM.

The external memory signals are multiplexed on the following IO rings:

- VDDSF:
  - Flash CS
  - Clock
  - Data (3:0)

When stacked PSRAM is used then the VIO2 and VDDSF need to be driven by the same supply.

The following table describes the external memory topology and the VDDSF/VIO2 voltage level implications.

#	Topology [1]	Description	Flash	PSRAM	XiP Mode Common for both Flash + PSRAM [4]	VDDSF	VIO2 [2]
1	External Flash QSPI	External Flash only QSPI	External QSPI	None	**Flash:** QSPI, 40/80MHz, SDR/DDR	1.8V or 3.3V	Independent 1.8 or 3.3V
2	External Flash Octal SPI	External Flash only Octal SPI	External Octal SPI	None	**Flash:** OSPI, 40/80MHz, SDR/DDR	1.8V or 3.3V	Same as VDDSF (D[7:4] on VIO2)
3	Stacked Flash QSPI	Stacked Flash, No PSRAM support	Stacked QSPI	Not Supported	**Flash:** QSPI, 40/80MHz, SDR/DDR	1.8V only (Stacked Flash is 1.8V only)	Independent 1.8 or 3.3V
4	External Flash QSPI + Stacked PSRAM QSPI	Stacked PSRAM + External Flash (Stacked PSRAM only is not supported)	External QSPI	Stacked QSPI	**Flash:** QSPI, 80MHz, SDR/DDR **PSRAM:** QSPI, 80MHz, DDR	1.8V only (Stacked PSRAM is 1.8V only)	1.8V [3] (PSRAM CS on VIO2)
5	External Flash Octal SPI +Stacked PSRAM QSPI	Stacked PSRAM + External Flash (Stacked PSRAM only is not supported)	External Octal SPI	Stacked QSPI	**Flash:** OSPI, 40/80MHz, SDR/DDR **PSRAM:** QSPI, 80MHz, DDR	1.8V only (Stacked PSRAM is 1.8V only)	1.8V [3] (PSRAM CS on VIO2)

(1) In stacked Flash versions, XiP pads are connected internally only and due to that the XiP pins are free and used for extra functionality.
(2) VIO2 must be identical to VDDSF when working with both external Flash and stacked PSRAM
(3) Stacked Flash/PSRAM are 1.8V only
(4) Consult SDK documentation for supported external memory topologies

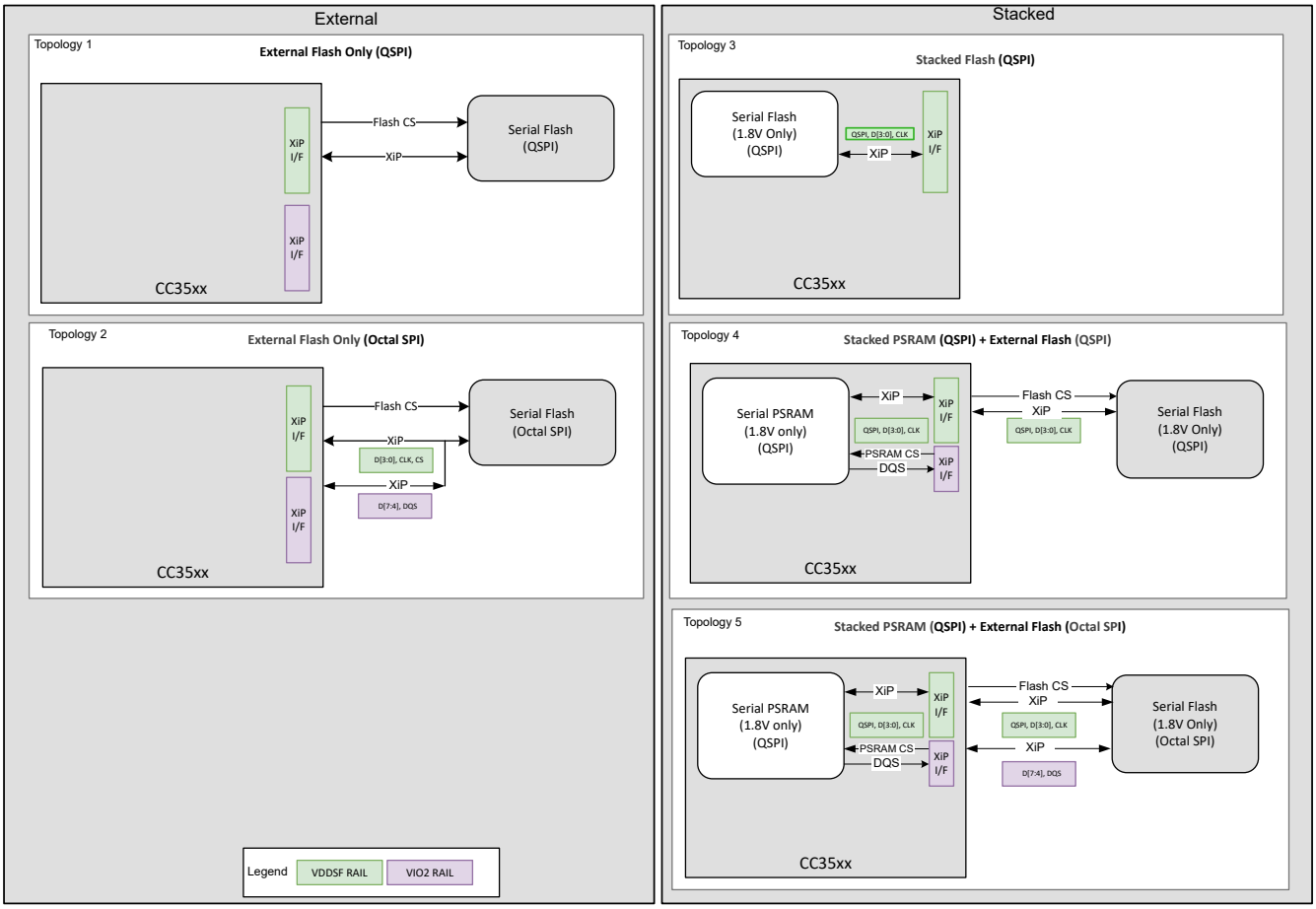


Figure 8-2. CC35xx Memory Topologies

8.6.4 µDMA

The µDMA (also called external DMA) is an auxiliary module dedicated to performing data movement between external and internal memory without CPU intervention. The µDMA is a basic DMA (single task execution) with two AHB masters interfacing OTFDE and MEMSS/SOC interconnect. The µDMA also has interface capabilites to peripherals, consult SDK documentation for support.

External DMA supports the following features:

- 2 Channels
- Secured/Non Secured or both Secured
- Separate IRQs for secure and non-secure
- Continuation of service: the second channel starts when the first finishes
- Data copy to/from Flash/PSRAM
- 32bits only
- FIFO 128B

The two channels can be defined as secured and non-secured, or both secured. The secured channel should be used to access secured memory regions and the non-secured to access non-secured memory regions. Access control based on the initiating context (secured / non-secured).

8.6.5 Arbiter

The External Memory Arbiter (EMA) module is an auxiliary module that controls the arbitration policy of direct access to external memory (OTFDE slave port arbitration). The EMA master multiplexer has three slave ports to which three masters can connect.

The EMA serves the following three Host MCU subsystem agents requiring access to external memory:

- Port 0 - External DMA (µDMA) - lowest prioirty
- Port 1 - D-Cache - middle priority
- Port 2 - I-Cache - highest priority

8.7 ICACHE Registers

Table 8-3 lists the memory-mapped registers for the ICACHE registers. All register offset addresses not listed in Table 8-3 should be considered as reserved locations and the register contents should not be modified.

Table 8-3. ICACHE Registers

Offset	Acronym	Register Name	Section
0h	MOD_VERSION	Module Identifier	Section 8.7.1
4h	CTRL	Cache Control	Section 8.7.2
8h	STATUS	Cache Status	Section 8.7.3
10h	Cache_Address_Low	Cache Start Address	Section 8.7.4
18h	Cache_Address_High	Cache Address Limit	Section 8.7.5
20h	Register_Address	RAM Address Register	Section 8.7.6
40h	HIT_COUNTER	Cache Hit Counter	Section 8.7.7
44h	MISS_COUNTER	Cache Miss Counter	Section 8.7.8
80h	IRQ_STATUS_RAW	Interrupt Raw Status	Section 8.7.9
84h	IRQ_STATUS_MASK	Interrupt Mask Status	Section 8.7.10
88h	IRQ_ENABLE_SET	Interrupt Set Register	Section 8.7.11
8Ch	IRQ_ENABLE_CLR	Interrupt Clear Register	Section 8.7.12

Complex bit access types are encoded to fit into small table cells. Table 8-4 shows the codes that are used for access types in this section.

Table 8-4. ICACHE Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.7.1 MOD_VERSION Register (Offset = 0h) [Reset = 00000000h]

MOD_VERSION is shown in Table 8-5.

Return to the Summary Table.

The Module and Version Register identifies the module identifier and revision of the icache module.

Table 8-5. MOD_VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Module Scheme
29-28	BU	R	2h	Module Business Unit
27-16	MODULE_ID	R	880h	Module ID
15-11	RTL_VERSION	R	1h	RTL version
10-8	MAJOR_REVISION	R	0h	Major Revision
7-6	CUSTOM_REVISION	R	0h	Custom Revision
5-0	MINOR_REVISION	R	0h	Minor revision

8.7.2 CTRL Register (Offset = 4h) [Reset = 00000000h]

CTRL is shown in Table 8-6.

Return to the Summary Table.

The control register defines the size of the remote cache data storage memory to use and whether the icache controller is enabled.

Table 8-6. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	mem_CENABLE	R/W	0h	.
30	mem_RENABLE	R/W	0h	.
29-0	RESERVED	R	0h	Reserved

8.7.3 STATUS Register (Offset = 8h) [Reset = 00000000h]

STATUS is shown in Table 8-7.

Return to the Summary Table.

The Status register displays the state of the icache controller.

Table 8-7. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OK_TO_GO	R	0h	The ok_to_go status bit indicates the Tag/LRU Ram has been initialized and the cache is in an operable state.
30-0	RESERVED	R	0h	Reserved

8.7.4 Cache_Address_Low Register (Offset = 10h) [Reset = 00000000h]

Cache_Address_Low is shown in Table 8-8.

Return to the Summary Table.

The Cache Address Low Register defines start of the cacheable space. The icache controller can cache up to a range of 8MB of of the target Flash as defined by CAL gt= CachedRange lt= CAH. This register is write protected when cenable is set.

Table 8-8. Cache_Address_Low Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	mem_addr_low	R/W	0h	The addr_lo defines the cache low address[31:12] for the icache controller to cache. The remaining bits 10:0 are assumed to be zero
11-0	RESERVED	R	0h	Reserved

8.7.5 Cache_Address_High Register (Offset = 18h) [Reset = 00000000h]

Cache_Address_High is shown in Table 8-9.

Return to the Summary Table.

The L1 Cache Address High Register defines end of the L1 cacheable space. The L1 cache can cache up to a range of 8MB of of the target Flash as defined by CAL >= CachedRange <= CAH. This register is write protected when cenable is set.

Table 8-9. Cache_Address_High Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	mem_addr_high	R/W	0h	The addr_hi defines the L1 high address[31:12] for the L1 to cache. The remaining bits 10:0 are assumed to be ones.
11-0	RESERVED	R	0h	Reserved

8.7.6 Register_Address (Offset = 20h) [Reset = 00000000h]

Register_Address is shown in Table 8-10.

Return to the Summary Table.

The RAM Address register defines the upper 17 bits of address for the RAM when renable is set. This register is write protected when renable is set

Table 8-10. Register_Address Field Descriptions

Bit	Field	Type	Reset	Description
31-15	mem_seg_addr	R/W	0h	The seg_addr defines RAM address[31:15] value for RAM access .
14-0	RESERVED	R	0h	Reserved

8.7.7 HIT_COUNTER Register (Offset = 40h) [Reset = 00000000h]

HIT_COUNTER is shown in Table 8-11.

Return to the Summary Table.

The HIT Counter register holds the number of cache Hits to the internal cache

Table 8-11. HIT_COUNTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	mem_hit_counter	R/W	0h	The hit Counts the number of hits to the L1 cache. Writing zero to this register will clear its contents.

8.7.8 MISS_COUNTER Register (Offset = 44h) [Reset = 00000000h]

MISS_COUNTER is shown in Table 8-12.

Return to the Summary Table.

The MISS Counter register holds the number of cache misses to the internal cache .

Table 8-12. MISS_COUNTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	mem_miss_counter	R/W	0h	The miss Counts the number of misses to the L1 cache. Writing zero to this register will clear its contents.

8.7.9 IRQ_STATUS_RAW Register (Offset = 80h) [Reset = 00000000h]

IRQ_STATUS_RAW is shown in Table 8-13.

Return to the Summary Table.

The Interrupt Raw Status Register holds the raw status of the icache error interrupts .

Table 8-13. IRQ_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	WR_HIT	R/W	0h	The wr_hit bit indicates a write to the cacheable range has occured potentially causing a coherency issue and the L1 is logically disabled while this bit is a '1'. Write 1 to set the wr_hit status for diagnostic purposes. Writing a 0 has no effect.
0	WR_ERR	R/W	0h	The wr_err bit indicates a write error has occured to the remote cache data storage memory and the L1 is logically disabled while this bit is a '1'. Write 1 to set the wr_err status for diagnostic purposes. Writing a 0 has no effect.

8.7.10 IRQ_STATUS_MASK Register (Offset = 84h) [Reset = 00000000h]

IRQ_STATUS_MASK is shown in Table 8-14.

Return to the Summary Table.

The Interrupt Masked Status Register holds the masked status for the icache error interrupts. Writing to this register will EOI the interrupt, that is if another interrupt is pending, a new pulse interrupt will be generated .

Table 8-14. IRQ_STATUS_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	mem_HIT	R/W	0h	The wr_hit bit indicates a write to the cacheable range has occured potentially causing a coherency issue and the L1 is logically disabled while this bit is a '1'. Write 1 to clear the wr_hit status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect to this field.
0	mem_ERR	R/W	0h	The wr_err bit indicates a write error has occured to the remote cache data storage memory and the L1 is logically disabled while this bit is a '1'. Write 1 to clear the wr_err status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect to this field.

8.7.11 IRQ_ENABLE_SET Register (Offset = 88h) [Reset = 00000000h]

IRQ_ENABLE_SET is shown in Table 8-15.

Return to the Summary Table.

The Interrupt Enable Set Register holds the interrupt enable status of the icache error interrupts .

Table 8-15. IRQ_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	EN_WR_HIT	R/W	0h	Interrupt Enable Set for wr_hit error bit. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
0	EN_WR_ERR	R/W	0h	Interrupt Enable Set for wr_err error bit. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.

8.7.12 IRQ_ENABLE_CLR Register (Offset = 8Ch) [Reset = 00000000h]

IRQ_ENABLE_CLR is shown in Table 8-16.

Return to the Summary Table.

The Interrupt Enable Clear Register holds the interrupt enable status of the icache error interrupts.

Table 8-16. IRQ_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	EN_WR_HIT	R/W	0h	Interrupt Enable Clear for wr_hit error bit. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect
0	EN_WR_ERR	R/W	0h	Interrupt Enable Clear for wr_err error bit. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.

8.8 DCACHE Registers

Table 8-17 lists the memory-mapped registers for the DCACHE registers. All register offset addresses not listed in Table 8-17 should be considered as reserved locations and the register contents should not be modified.

Table 8-17. DCACHE Registers

Offset	Acronym	Register Name	Section
0h	MOD_VER	Module Identification	Section 8.8.1
4h	CTRL	Cache Configuration	Section 8.8.2
8h	STS	Module Status	Section 8.8.3
10h	CAL	Cache Address Low	Section 8.8.4
18h	CAH	Cache Range End	Section 8.8.5
40h	READ_COUNTER	Cache Hit Counter	Section 8.8.6
44h	WRITE_COUNTER	Cache Miss Counter	Section 8.8.7
48h	ADDRESS_LATCH	Error Address Storage	Section 8.8.8
4Ch	CACHE_FSM_STATE	Cache Status Register	Section 8.8.9
80h	IRQSTATUS_RAW	Error Interrupt Status	Section 8.8.10
84h	IRQSTATUS_MSK	Masked Interrupt Status	Section 8.8.11
88h	IRQENABLE_SET	Interrupt Enable Set	Section 8.8.12
8Ch	IRQENABLE_CLR	Interrupt Enable Clear	Section 8.8.13
C0h	CTRL1	Cache Control	Section 8.8.14
C4h	STATUS1	Cache Operation Status	Section 8.8.15

Complex bit access types are encoded to fit into small table cells. Table 8-18 shows the codes that are used for access types in this section.

Table 8-18. DCACHE Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
W1S	W 1S	Write 1 to set
Reset or Default Value		
-n		Value after reset or the default value

8.8.1 MOD_VER Register (Offset = 0h) [Reset = 68800800h]

MOD_VER is shown in Table 8-19.

Return to the Summary Table.

The Module and Version Register identifies the module identifier and revision of the L1 module.

Table 8-19. MOD_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	RH	1h	Module Scheme
29-28	BU	RH	2h	Module Business Unit
27-16	MODULE_ID	RH	880h	L1 module ID.
15-11	RTL_VERSION	RH	1h	RTL Version.
10-8	MAJOR_REVISION	RH	0h	Major Revision.
7-6	CUSTOM_REVISION	RH	0h	Custom Revision.
5-0	MINOR_REVISION	RH	0h	Minor Revision.

8.8.2 CTRL Register (Offset = 4h) [Reset = XXXXXXXXh]

CTRL is shown in Table 8-20.

Return to the Summary Table.

The control register defines the size of the remote cache data storage memory to use and whether the L1 is enabled.

Table 8-20. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CENABLE	RH/W	0h	The ~icenable field determines whether the L1 configuration is enabled or not. 0: Disabled 1: Enabled This field is write protected when the t_cfg_lock_ipcfg input is high.
30	RENABLE	RH/W	1h	The ~irenable field determines if half the cache space is RAM or cache. 0: No RAM 64K of cache 1: RAM 32K of cache, 32K of RAM. This field is write protected when ~icenable is set or the t_cfg_lock_ipcfg input is high.
29-0	RESERVED	RH	0h	

8.8.3 STS Register (Offset = 8h) [Reset = XXXXXXXXh]

STS is shown in Table 8-21.

Return to the Summary Table.

The Status register displays the state of the L1 module

Table 8-21. STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OK_TO_GO	RH	0h	The ~iok_to_go status bit indicates the Tag/LRU Ram has been initialized and the cache is in an operable state.
30-0	RESERVED	R	0h	

8.8.4 CAL Register (Offset = 10h) [Reset = 00000XXXh]

CAL is shown in Table 8-22.

Return to the Summary Table.

The L1 Cache Address Low Register defines start of the L1 cacheable space. The L1 cache can cache up to a range of 8MB of of the target Flash as defined by CAL>=CachedRange<=CAH. This register is write protected when ~icenable is set or the t_cfg_lock_ipcfg input is high.

Table 8-22. CAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	ADDR_LO	RH/W	0h	The ~iaddr_lo defines the L1 low address[31:12] for the L1 to cache. The remaining bits 10:0 are assumed to be zero.
11-0	RESERVED	RH	0h	

8.8.5 CAH Register (Offset = 18h) [Reset = 00000XXXh]

CAH is shown in Table 8-23.

Return to the Summary Table.

The L1 Cache Address High Register defines end of the L1 cacheable space. The L1 cache can cache up to a range of 8MB of of the target Flash as defined by CAL>=CachedRange<=CAH. This register is write protected when ~icenable is set or the t_cfg_lock_ipcfg input is high.

Table 8-23. CAH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	ADDR_HI	RH/W	0h	The ~iaddr_hi defines the L1 high address[31:12] for the L1 to cache. The remaining bits 10:0 are assumed to be ones.
11-0	RESERVED	RH	0h	

8.8.6 READ_COUNTER Register (Offset = 40h) [Reset = 00000000h]

READ_COUNTER is shown in Table 8-24.

Return to the Summary Table.

The L1 HIT Counter register holds the number of L1 Hits to the internal cache.

Table 8-24. READ_COUNTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	READ_HIT_COUNTER	RH/W	0h	The hit Counts the number of hits to the L1 cache. Writing zero to this register will clear its contents When one reach the max, the rest of the counters are halted too.
11-0	READ_MISS_COUNTER	RH/W	0h	The miss Counts the number of misses to the L1 cache. Writing zero to this register will clear its contents. When one reach the max, the rest of the counters are halted too.

8.8.7 WRITE_COUNTER Register (Offset = 44h) [Reset = 00000000h]

WRITE_COUNTER is shown in Table 8-25.

Return to the Summary Table.

The L1 MISS Counter register holds the number of L1 Misses to the internal cache.

Table 8-25. WRITE_COUNTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	WRITE_HIT_COUNTER	RH/W	0h	The hit Counts the number of hits to the L1 cache. Writing zero to this register will clear its contents. When one reach the max, the rest of the counters are halted too.
11-0	WRITE_MISS_COUNTER	RH/W	0h	The miss Counts the number of misses to the L1 cache. Writing zero to this register will clear its contents. When one reach the max, the rest of the counters are halted too

8.8.8 ADDRESS_LATCH Register (Offset = 48h) [Reset = 00000000h]

ADDRESS_LATCH is shown in Table 8-26.

Return to the Summary Table.

When having OTFDE AHB error, Latch the address accessed by D-cache

Table 8-26. ADDRESS_LATCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS_LATCH	RH/W	0h	When D-cache receive AHB error from the OTFDE it should latch the address accessed by D-cache. (OTFDE generates an error for write only) Writing zero to this register will clear its contents.

8.8.9 CACHE_FSM_STATE Register (Offset = 4Ch) [Reset = 00000000h]

CACHE_FSM_STATE is shown in Table 8-27.

Return to the Summary Table.

Table 8-27. CACHE_FSM_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Dcache current FSM state
4-0	FSM_STATE	R	0h	Dcache current FSM state WIDLE = 5'd0; - No access to D-cache WRAMWR = 5'd1; - Data RAM Write WRAMRD = 5'd2; - Data RAM Read WCREADT = 5'd4; - Read Hit WCREADC = 5'd5; - Read Miss WCWRITET = 5'd6; - Write Hit EVICT = 5'd7; -Write back to PSRAM WR_ALLOC = 5'd8; - Write Allocate in write miss RD_WA = 5'd9; - Word aligned read for a byte aligned read WD = 5'd10; - Writing data to PSRAM RDATA_CACHE = 5'd3; Reading data RAM for eviction DEC_DIR = 5'd11; - Deciding direction RDATA_CACHE_FLUSH = 5'd12; Reading data from data RAM for flush RD_SET = 5'd13; Reading TAG & MRU DET_GRANT = 5'd14; Detecting the granted way to evict EVICT_FLUSH = 5'd15; Eviction during Flush WD_DEBUG = 5'd16; Writing data to PSRAM during a debugger access

8.8.10 IRQSTATUS_RAW Register (Offset = 80h) [Reset = 00000000h]

IRQSTATUS_RAW is shown in Table 8-28.

Return to the Summary Table.

The Interrupt Raw Status Register holds the raw status of the L1 error interrupts. Note: Read to the field of this register gives raw status of corresponding interrupt. S/W can set corresponding interrupt field for diagnostic purposes.

Table 8-28. IRQSTATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1	LOCK_CFG_WR	R/W	0h	The ~ilock_cfg_wr bit indicates a write to a locked configuration register has occured. Write 1 to set the ~ilock_cfg_wr status for diagnostic purposes. Writing a 0 has no effect.
0	RESERVED	RH/W1S	0h	reserved

8.8.11 IRQSTATUS_MSK Register (Offset = 84h) [Reset = 00000000h]

IRQSTATUS_MSK is shown in Table 8-29.

Return to the Summary Table.

The Interrupt Masked Status Register holds the masked status for the L1 error interrupts. Writing to this register will EOI the interrupt, that is if another interrupt is pending, a new pulse interrupt will be generated. Note: Read to the field of this register gives masked status of corresponding interrupt. Writing 1 to the field of this register clears corresponding interrupt.

Table 8-29. IRQSTATUS_MSK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1	LOCK_CFG_WR	R/W	0h	The ~ilock_cfg_wr bit indicates a write to a locked configuration register has occured. Write 1 to clear the ~ilock_cfg_wr status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect to this field.
0	RESERVED	RH/W1C	0h	reserved

8.8.12 IRQENABLE_SET Register (Offset = 88h) [Reset = 00000000h]

IRQENABLE_SET is shown in Table 8-30.

Return to the Summary Table.

The Interrupt Enable Set Register holds the interrupt enable status of the L1 error interrupts. Note:Writing 1 to field of this register will not mask the corresponding interrupt. IRQSTATUS_RAW and IRQSTATUS_MSK status field gives the same status.

Table 8-30. IRQENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1	EN_LOCK_CFG_WR	R/W	0h	Interrupt Enable Set for ~ilock_cfg_wr error bit. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
0	RESERVED	RH/W1S	0h	reserved

8.8.13 IRQENABLE_CLR Register (Offset = 8Ch) [Reset = 00000000h]

IRQENABLE_CLR is shown in Table 8-31.

Return to the Summary Table.

The Interrupt Enable Clear Register holds the interrupt enable status of the L1 error interrupts. Note:Writing 1 to field of this register masks the corresponding interrupt. IRQSTATUS_RAW and IRQSTATUS_MSK status field gives the raw status and masked status respectively

Table 8-31. IRQENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1	EN_LOCK_CFG_WR	R/W	0h	Interrupt Enable Clear for ~ilock_cfg_wr error bit. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.
0	RESERVED	RH/W1C	0h	reserved

8.8.14 CTRL1 Register (Offset = C0h) [Reset = XXXXXXXXh]

CTRL1 is shown in Table 8-32.

Return to the Summary Table.

Flush and invalidates requests

Table 8-32. CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FLUSH	RH/W	0h	0x0 - Do nothing 0x1 - Flush The bit is self cleared when flush completed
30	INVALIDATE	RH/W	0h	0x0 - Do nothing 0x1 - Invalidate This bit is self cleared when invalidate completed
29-0	RESERVED	R	0h	

8.8.15 STATUS1 Register (Offset = C4h) [Reset = XXXXXXXXh]

STATUS1 is shown in Table 8-33.

Return to the Summary Table.

Flush and invalidates status

Table 8-33. STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FLUSH_STATUS	R	0h	This bit indicates that Flush as been completed (Bit is cleared when Flush request bit is asserted)
30	INVALIDATE_STATUS	RH	0h	This bit indicates that invalidate has been completed (Bit is cleared when flush request bit is asserted)
29	FLUSH_FAIL	RH	0h	This bit indicates that Flush has failed (Bit is cleared when Flush request bit is asserted)
28-0	RESERVED	R	0h	

8.9 OSPI Registers

Table 8-34 lists the memory-mapped registers for the OSPI registers. All register offset addresses not listed in Table 8-34 should be considered as reserved locations and the register contents should not be modified.

Table 8-34. OSPI Registers

Offset	Acronym	Register Name	Section
0h	CONFIG	Configuration Register	Section 8.9.1
4h	DEV_INSTR_RD_CONFIG	Read Instruction Configuration	Section 8.9.2
8h	DEV_INSTR_WR_CONFIG	Device Write Instruction Configuration Register	Section 8.9.3
Ch	DEV_DELAY	Device Delay Control	Section 8.9.4
10h	RD_DATA_CAPTURE	Data Capture	Section 8.9.5
14h	DEV_SIZE_CONFIG	Memory Size Configuration	Section 8.9.6
18h	SRAM_PARTITION_CFG	Memory Partition Control	Section 8.9.7
1Ch	IND_AHB_ADDR_TRIGGER	Indirect Address Trigger	Section 8.9.8
20h	DMA_PERIPH_CONFIG	Peripheral Configuration	Section 8.9.9
24h	REMAP_ADDR	Address Remapping	Section 8.9.10
28h	MODE_BIT_CONFIG	Mode Configuration	Section 8.9.11
2Ch	SRAM_FILL	Memory Fill Status	Section 8.9.12
30h	TX_THRESH	Transmit Threshold	Section 8.9.13
34h	RX_THRESH	Receive Threshold	Section 8.9.14
38h	WRITE_COMPLETION_CTRL	Write Polling Control	Section 8.9.15
3Ch	NO_OF_POLLS_BEF_EXP	Polling Expiration Register	Section 8.9.16
40h	IRQ_STATUS	Interrupt Status	Section 8.9.17
44h	IRQ_MASK	Interrupt Enable Control	Section 8.9.18
50h	LOWER_WR_PROT	Write Protection	Section 8.9.19
54h	UPPER_WR_PROT	Write Protection Control	Section 8.9.20
58h	WR_PROT_CTRL	Write Protection Control	Section 8.9.21
60h	INDIRECT_READ_XFER_CTRL	Transfer Control	Section 8.9.22
64h	INDIRECT_READ_XFER_WATERMARK	Indirect Read Transfer Watermark Register	Section 8.9.23
68h	INDIRECT_READ_XFER_START	Indirect Read Transfer Start Address Register	Section 8.9.24
6Ch	INDIRECT_READ_XFER_NUM_BYTES	Transfer Size	Section 8.9.25
70h	INDIRECT_WRITE_XFER_CTRL	Transfer Control	Section 8.9.26
74h	INDIRECT_WRITE_XFER_WATERMARK	Transfer Watermark	Section 8.9.27
78h	INDIRECT_WRITE_XFER_START	Transfer Start Address	Section 8.9.28
7Ch	INDIRECT_WRITE_XFER_NUM_BYTES	Transfer Byte Count	Section 8.9.29
80h	INDIRECT_TRIGGER_ADDR_RANGE	Address Range Control	Section 8.9.30
8Ch	FLASH_COMMAND_CTRL_MEM	Command Control	Section 8.9.31
90h	FLASH_CMD_CTRL	Command Control	Section 8.9.32
94h	FLASH_CMD_ADDR	Command Address	Section 8.9.33
A0h	FLASH_RD_DATA_LOWER	Flash Read Data	Section 8.9.34
A4h	FLASH_RD_DATA_UPPER	Flash Command Read Data Register (Upper)	Section 8.9.35
A8h	FLASH_WR_DATA_LOWER	Lower Write Data	Section 8.9.36
ACh	FLASH_WR_DATA_UPPER	Flash Command Write Data Register (Upper)	Section 8.9.37
B0h	POLLING_FLASH_STATUS	Polling Flash Status Register	Section 8.9.38
B4h	PHY_CONFIGURATION	PHY Configuration	Section 8.9.39
B8h	PHY_MASTER_CONTROL	PHY DLL controller Control Register	Section 8.9.40
BCh	DLL_OBSERVABLE_LOWER	Clock Observable Values	Section 8.9.41

Table 8-34. OSPI Registers (continued)

Offset	Acronym	Register Name	Section
C0h	DLL_OBSERVABLE_UPPER	Upper Observable Values	Section 8.9.42
E0h	OPCODE_EXT_LOWER	Lower Extension Control	Section 8.9.43
E4h	OPCODE_EXT_UPPER	Extended Instruction Upper	Section 8.9.44
FCh	MODULE_ID	Module Identifier	Section 8.9.45

Complex bit access types are encoded to fit into small table cells. Table 8-35 shows the codes that are used for access types in this section.

Table 8-35. OSPI Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

8.9.1 CONFIG Register (Offset = 0h) [Reset = 82080081h]

CONFIG is shown in Table 8-36.

Return to the Summary Table.

Octal-SPI Configuration Register

Table 8-36. CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	Serial interface and low level SPI pipeline is IDLE: This is a STATUS read-only bit. Note this is a retimed signal, so there will be some inherent delay on the generation of this status signal. 0h = Disable 1h = Enable
30	DUAL_BYTE_OPCODE_EN	R/W	0h	Dual-byte Opcode Mode enable bit This bit is to be set in case the target Flash Device supports dual byte opcode (i.e. Macronix MX25). It is applicable for Octal I/O Mode or Protocol only so should be set back to low if the device is configured to work in another SPI Mode. If enabled, the supplementing bytes are taken from Opcode Extension Register (Lower) and from Opcode Extension Register (Upper). 0h = Disable 1h = Enable
29	CRC_ENABLE	R/W	0h	CRC enable bit This bit is to be set in case the target Flash Device supports CRC (Macronix MX25). It is applicable for Octal DDR Protocol only so should be set back to low if the device is configured to work in another SPI Mode. 0h = Disable 1h = Enable
28-26	RESERVED	R	0h	
25	PIPELINE_PHY	R/W	1h	Pipeline PHY Mode enable: This bit is relevant only for configuration with PHY Module. It should be asserted to '1' between consecutive PHY pipeline reads transfers and de-asserted to '0' otherwise. 0h = Disable 1h = Enable
24	ENABLE_DTR_PROTOCOL	R/W	0h	Enable DTR Protocol: This bit should be set if device is configured to work in DTR protocol. 0h = Disable 1h = Enable
23	ENABLE_AHB_DECODER	R/W	0h	Enable AHB Decoder: Value=0 : Active peripheral is selected based on Peripheral Chip Select Lines (bits [13:10]). Value=1 Active peripheral is selected based on actual AHB address (the partition for each device is calculated with respect to bits [28:21] of Device Size Configuration Register) 0h = Disable 1h = Enable
22-19	MSTR_BAUD_DIV	R/W	1h	controller Mode Baud Rate Divisor: SPI baud rate = (controller reference clock) baud_rate_divisor. The baud rate is the clock rate divided by 2 multiplied by (Divisor + 1). Meaning, when Divisor Value is set to 0,1,2,..15 it sets the baud rate is the clock rate divided by 2, 4, 6,..32 respectively 0h = Smallest value Fh = Highest possible value

Table 8-36. CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	ENTER_XIP_MODE_IMM	R/W	0h	Enter XIP Mode immediately: Value=0 : If XIP is enabled, then setting to 0 will cause the controller to exit XIP mode on the next READ instruction. Value=1 : Operate the device in XIP mode immediately Use this register when the external device wakes up in XIP mode (as per the contents of its non- volatile configuration register). The controller will assume the next READ instruction will be passed to the device as an XIP instruction, and therefore will not require the READ opcode to be transferred. Note: To exit XIP mode, this bit should be set to 0. This will take effect in the attached device only after the next READ instruction is executed. Software therefore should ensure that at least one READ instruction is requested after resetting this bit in order to be sure that XIP mode is exited. 0h = Disable 1h = Enable
17	ENTER_XIP_MODE	R/W	0h	Enter XIP Mode on next READ: Value=0 : If XIP is enabled, then setting to 0 will cause the controller to exit XIP mode on the next READ instruction. Value=1 : If XIP is disabled, then setting to ?1? will inform the controller that the device is ready to enter XIP on the next READ instruction. The controller will therefore send the appropriate command sequence, including mode bits to cause the device to enter XIP mode. Use this register after the controller has ensured the FLASH device has been configured to be ready to enter XIP mode. Note : To exit XIP mode, this bit should be set to 0. This will take effect in the attached device only AFTER the next READ instruction is executed. Software should therefore ensure that at least one READ instruction is requested after resetting this bit before it can be sure XIP mode in the device is exited. 0h = Disable 1h = Enable
16	ENB_AHB_ADDR_REMAP	R/W	0h	Enable AHB Address Re-mapping: (Direct Access Mode Only) When set to 1, the incoming AHB address will be adapted and sent to the FLASH device as (address + N), where N is the value stored in the remap address register. 0h = Disable 1h = Enable
15	ENB_DMA_IF	R/W	0h	Enable DMA Peripheral Interface: Set to 1 to enable the DMA handshaking logic. When enabled the controller will trigger DMA transfer requests via the DMA peripheral interface. Set to 0 to disable 0h = Disable 1h = Enable
14	WR_PROT_FLASH	R/W	0h	Write Protect Flash Pin: Set to drive the Write Protect pin of the FLASH device. This is resynchronized to the generated memory clock as necessary. 0h = Disable 1h = Enable
13-10	PERIPH_CS_LINES	R/W	0h	Peripheral Chip Select Lines: Peripheral chip select lines If pdec = 0, ss[3:0] are output thus: ss[3:0] n_ss_out[3:0] xxx0 1110 xx01 1101 x011 1011 0111 0111 1111 1111 (no peripheral selected) else ss[3:0] directly drives n_ss_out[3:0] 0h = Smallest value Fh = Highest possible value
9	PERIPH_SEL_DEC	R/W	0h	Peripheral select decode: 0h = only 1 of 4 selects n_ss_out[3:0] is active 1 : allow external 4-to-16 decode (n_ss_out = ss) 1h = allow external 4-to-16 decode (n_ss_out = ss)

Table 8-36. CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	ENB_LEGACY_IP_MODE	R/W	0h	Legacy IP Mode Enable: 0h = Use Direct Access Controller/Indirect Access Controller 1 : legacy Mode is enabled. In this mode, any write to the controller via the AHB interface is serialized and sent to the FLASH device. Any valid AHB read will pop the internal RX-FIFO, retrieving data that was forwarded by the external FLASH device on the SPI lines,4,2 or 1 byte transfers are permitted and controlled via the HSIZE input. 1h = legacy Mode is enabled. In this mode, any write to the controller via the AHB interface is serialized and sent to the FLASH device. Any valid AHB read will pop the internal RX-FIFO, retrieving data that was forwarded by the external FLASH device on the SPI lines,4,2 or 1 byte transfers are permitted and controlled via the HSIZE input.
7	ENB_DIR_ACC_CTLR	R/W	1h	Enable Direct Access Controller: 0h = disable the Direct Access Controller once current transfer of the data word (FF_W) is complete. 1 : enable the Direct Access Controller When the Direct Access Controller and Indirect Access Controller are both disabled, all AHB requested are completed with an error response. 1h = enable the Direct Access Controller When the Direct Access Controller and Indirect Access Controller are both disabled, all AHB requested are completed with an error response.
6	RESET_CFG	R/W	0h	RESET pin configuration: 0 = RESET feature on DQ3 pin of the device 1 = RESET feature on dedicated pin of the device (controlling of 5th bit influences on reset_out output) 0h = Disable 1h = Enable
5	RESET_PIN	R/W	0h	Set to drive the RESET pin of the FLASH device and reset for de-activation of the RESET pin feature 0h = Disable 1h = Enable
4	HOLD_PIN	R/W	0h	Set to drive the HOLD pin of the FLASH device and reset for de-activation of the HOLD pin feature 0h = Disable 1h = Enable
3	PHY_MODE_ENABLE	R/W	0h	PHY mode enable: When enabled, the controller is informed that PHY Module is to be used for handling SPI transfers. This bit is relevant only for configuration with PHY Module. 0h = Disable 1h = Enable
2	SEL_CLK_PHASE	R/W	0h	Select Clock Phase: Selects whether the clock is in an active or inactive phase outside the SPI word. 0h = the SPI clock is active outside the word 1 : the SPI clock is inactive outside the word 1h = the SPI clock is inactive outside the word
1	SEL_CLK_POL	R/W	0h	Clock polarity outside SPI word: 0h = the SPI clock is quiescent low 1 : the SPI clock is quiescent high 1h = the SPI clock is quiescent high
0	ENB_SPI	R/W	1h	Octal-SPI Enable: 0h = disable the Octal-SPI, once current transfer of the data word (FF_W) is complete. 1 : enable the Octal-SPI, when spi_enable = 0, all output enables are inactive and all pins are set to input mode. 1h = enable the Octal-SPI, when spi_enable = 0, all output enables are inactive and all pins are set to input mode.

8.9.2 DEV_INSTR_RD_CONFIG Register (Offset = 4h) [Reset = 00000003h]

DEV_INSTR_RD_CONFIG is shown in Table 8-37.

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Device Read Instruction Configuration Register

Table 8-37. DEV_INSTR_RD_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	
28-24	DUMMY_RD_CLK_CYCLES	R/W	0h	Dummy Read Clock Cycles: Number of dummy clock cycles required by device for read instruction. 0h = Smallest value 1Fh = Highest possible value
23-21	RESERVED	R	0h	
20	MODE_BIT_ENABLE	R/W	0h	Mode Bit Enable: Set this field to 1 to ensure that the mode bits as defined in the Mode Bit Configuration register are sent following the address bytes. 0h = Disable 1h = Enable
19-18	RESERVED	R	0h	
17-16	DATA_XFER_TYPE_EXT_MODE	R/W	0h	Data Transfer Type for Standard SPI modes: 0 : SIO mode data is shifted to the device on DQ0 only and from the device on DQ1 only 1 : Used for Dual Input/Output instructions. For data transfers, DQ0 and DQ1 are used as both inputs and outputs. 2 : Used for Quad Input/Output instructions. For data transfers, DQ0,DQ1,DQ2 and DQ3 are used as both inputs and outputs. 3 : Used for Quad Input/Output instructions. For data transfers, DQ[7:0] are used as both inputs and outputs. 0h = Smallest value 3h = Highest possible value
15-14	RESERVED	R	0h	
13-12	ADDR_XFER_TYPE_STD_MODE	R/W	0h	Address Transfer Type for Standard SPI modes: 0 : Addresses can be shifted to the device on DQ0 only 1 : Addresses can be shifted to the device on DQ0 and DQ1 only 2 : Addresses can be shifted to the device on DQ0, DQ1, DQ2 and DQ3 3 : Addresses can be shifted to the device on DQ[7:0] 0h = Smallest value 3h = Highest possible value
11	PRED_DIS	R/W	0h	Predicted Read Disable Bit: Disable generation of predicted read when doing read accesses using Direct Mode 0h = Disable 1h = Enable
10	DDR_EN	R/W	0h	DDR Enable: This is to inform that opcode from rd_opcode_non_xip_fld is compliant with one of the DDR READ Commands 0h = Disable 1h = Enable
9-8	INSTR_TYPE	R/W	0h	Instruction Type: 0 : Use Standard SPI mode (instruction always shifted into the device on DQ0 only) 1 : Use DIO-SPI mode (Instructions always sent on DQ0 and DQ1) 2 : Use QIO-SPI mode (Instructions always sent on DQ0, DQ1, DQ2 and DQ3) 3 : Use Octal-IO-SPI mode (Instructions always sent on DQ[7:0]) 0h = Smallest value 3h = Highest possible value
7-0	RD_OPCODE_NON_XIP	R/W	3h	Read Opcode in non-XIP mode: Read Opcode to use when not in XIP mode 0h = Smallest value FFh = Highest possible value

8.9.3 DEV_INSTR_WR_CONFIG Register (Offset = 8h) [Reset = 00000002h]

DEV_INSTR_WR_CONFIG is shown in Table 8-38.

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Device Write Instruction Configuration Register

Table 8-38. DEV_INSTR_WR_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	
28-24	DUMMY_WR_CLK_CYCLES	R/W	0h	Dummy Write Clock Cycles: Number of dummy clock cycles required by device for write instruction. 0h = Smallest value 1Fh = Highest possible value
23-18	RESERVED	R	0h	
17-16	DATA_XFER_TYPE_EXT_MODE	R/W	0h	Data Transfer Type for Standard SPI modes: 0 : SIO mode data is shifted to the device on DQ0 only and from the device on DQ1 only 1 : Used for Dual Input/Output instructions. For data transfers, DQ0 and DQ1 are used as both inputs and outputs. 2 : Used for Quad Input/Output instructions. For data transfers, DQ0,DQ1,DQ2 and DQ3 are used as both inputs and outputs. 3 : Used for Quad Input/Output instructions. For data transfers, DQ[7:0] are used as both inputs and outputs. 0h = Smallest value 3h = Highest possible value
15-14	RESERVED	R	0h	
13-12	ADDR_XFER_TYPE_STD_MODE	R/W	0h	Address Transfer Type for Standard SPI modes: 0 : Addresses can be shifted to the device on DQ0 only 1 : Addresses can be shifted to the device on DQ0 and DQ1 only 2 : Addresses can be shifted to the device on DQ0, DQ1, DQ2 and DQ3 3 : Addresses can be shifted to the device on DQ[7:0] 0h = Smallest value 3h = Highest possible value
11-9	RESERVED	R	0h	
8	WEL_DIS	R/W	0h	WEL Disable: This is to turn off automatic issuing of WEL Command before write operation for DAC or INDAC 0h = Disable 1h = Enable
7-0	WR_OPCODE	R/W	2h	Write Opcode 0h = Smallest value FFh = Highest possible value

8.9.4 DEV_DELAY Register (Offset = Ch) [Reset = 00000000h]

DEV_DELAY is shown in Table 8-39.

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Octal-SPI Device Delay Register: This register is used to introduce relative delays into the generation of the controller output signals. All timings are defined in cycles of the SPI REFERENCE CLOCK/ext_clk, defined in this table as SPI controller ref clock.

Table 8-39. DEV_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	D_NSS	R/W	0h	Clock Delay for Chip Select Deassert: Delay in controller reference clocks for the length that the controller mode chip select outputs are de-asserted between transactions. The minimum delay is always SCLK period to ensure the chip select is never re-asserted within an SCLK period. 0h = Smallest value FFh = Highest possible value
23-16	D_BTWN	R/W	0h	Clock Delay for Chip Select Deactivation: Delay in controller reference clocks between one chip select being de-activated and the activation of another. This is used to ensure a quiet period between the selection of two different peripherals and requires the transmit FIFO to be empty. 0h = Smallest value FFh = Highest possible value
15-8	D_AFTER	R/W	0h	Clock Delay for Last Transaction Bit: Delay in controller reference clocks between last bit of current transaction and deasserting the device chip select (n_ss_out). By default, the chip select will be deasserted on the cycle following the completion of the current transaction. 0h = Smallest value FFh = Highest possible value
7-0	D_INIT	R/W	0h	Clock Delay with n_ss_out: Delay in controller reference clocks between setting n_ss_out low and first bit transfer. 0h = Smallest value FFh = Highest possible value

8.9.5 RD_DATA_CAPTURE Register (Offset = 10h) [Reset = 00000001h]

RD_DATA_CAPTURE is shown in Table 8-40.

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Read Data Capture Register

Table 8-40. RD_DATA_CAPTURE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	
19-16	DDR_READ_DELAY	R/W	0h	DDR read delay: Delay the transmitted data by the programmed number of ref_clk cycles.This field is only relevant when DDR Read Command is executed. Otherwise can be ignored. 0h = Smallest value Fh = Highest possible value
15-9	RESERVED	R	0h	
8	DQS_ENABLE	R/W	0h	DQS enable bit: If enabled, signal from DQS input is driven into RX DLL and is used for data capturing in PHY Mode rather than internally generated gated ref_clk.. 0h = Disable 1h = Enable
7-6	RESERVED	R	0h	
5	SAMPLE_EDGE_SEL	R/W	0h	Sample edge selection: Choose edge on which data outputs from flash memory will be sampled 0h = Disable 1h = Enable
4-1	DELAY	R/W	0h	Read Delay: Delay the read data capturing logic by the programmed number of ref_clk cycles 0h = Smallest value Fh = Highest possible value
0	BYPASS	R/W	1h	Bypass the adapted loopback clock circuit 0h = Disable 1h = Enable

8.9.6 DEV_SIZE_CONFIG Register (Offset = 14h) [Reset = 00101002h]

DEV_SIZE_CONFIG is shown in Table 8-41.

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Device Size Configuration Register

Table 8-41. DEV_SIZE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	
28-27	MEM_SIZE_ON_CS3	R/W	0h	Size of Flash Device connected to CS[3] pin: Value=00 : size of 512Mb. Value=01 : size of 1Gb. Value=10 : size of 2Gb. Value=11 : size of 4Gb. 0h = Smallest value 3h = Highest possible value
26-25	MEM_SIZE_ON_CS2	R/W	0h	Size of Flash Device connected to CS[2] pin: Value=00 : size of 512Mb. Value=01 : size of 1Gb. Value=10 : size of 2Gb. Value=11 : size of 4Gb. 0h = Smallest value 3h = Highest possible value
24-23	MEM_SIZE_ON_CS1	R/W	0h	Size of Flash Device connected to CS[1] pin: Value=00 : size of 512Mb. Value=01 : size of 1Gb. Value=10 : size of 2Gb. Value=11 : size of 4Gb. 0h = Smallest value 3h = Highest possible value
22-21	MEM_SIZE_ON_CS0	R/W	0h	Size of Flash Device connected to CS[0] pin: Value=00 : size of 512Mb. Value=01 : size of 1Gb. Value=10 : size of 2Gb. Value=11 : size of 4Gb. 0h = Smallest value 3h = Highest possible value
20-16	BYTES_PER_SUBSECTOR	R/W	10h	Number of bytes per Block. This is required by the controller for performing the write protection logic. The number of bytes per block must be a power of 2 number. 0h = Smallest value 1Fh = Highest possible value
15-4	BYTES_PER_DEVICE_PAGE	R/W	100h	Number of bytes per device page. This is required by the controller for performing FLASH writes up to and across page boundaries. 0h = Smallest value FFFh = Highest possible value
3-0	NUM_ADDR_BYTES	R/W	2h	Number of address bytes. A value of 0 indicates 1 byte. 0h = Smallest value Fh = Highest possible value

8.9.7 SRAM_PARTITION_CFG Register (Offset = 18h) [Reset = 00000080h]

SRAM_PARTITION_CFG is shown in Table 8-42.

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SRAM Partition Configuration Register

Table 8-42. SRAM_PARTITION_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	THRESHOLD	R/W	80h	Defines the size of the indirect read partition in the SRAM, in units of SRAM locations. By default, half of the SRAM is reserved for indirect read operation, and half for indirect write. The size of this register will scale with the depth of the SRAM.

8.9.8 IND_AHB_ADDR_TRIGGER Register (Offset = 1Ch) [Reset = 00000000h]

IND_AHB_ADDR_TRIGGER is shown in Table 8-43.

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Indirect AHB Address Trigger Register

Table 8-43. IND_AHB_ADDR_TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR	R/W	0h	This is the base address that will be used by the AHB controller. When the incoming AHB read access address matches a range of addresses from this trigger address to the trigger address + 15, then the AHB request will be completed by fetching data from the Indirect Controllers SRAM. 0h = Smallest value FFFFFFFFh = Highest possible value

8.9.9 DMA_PERIPH_CONFIG Register (Offset = 20h) [Reset = 00000000h]

DMA_PERIPH_CONFIG is shown in Table 8-44.

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DMA Peripheral Configuration Register

Table 8-44. DMA_PERIPH_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	
11-8	NUM_BURST_REQ_BYTES	R/W	0h	Number of Burst Bytes: Number of bytes in a burst type request on the DMA peripheral request. A programmed value of 0 represents a single byte. This should be setup before starting the indirect read or write operation. The actual number of bytes used is 2**(value in this register) which will simplify implementation. 0h = Smallest value Fh = Highest possible value
7-4	RESERVED	R	0h	
3-0	NUM_SINGLE_REQ_BYTES	R/W	0h	Number of Single Bytes: Number of bytes in a single type request on the DMA peripheral request. A programmed value of 0 represents a single byte. This should be setup before starting the indirect read or write operation. The actual number of bytes used is 2**(value in this register) which will simplify implementation. 0h = Smallest value Fh = Highest possible value

8.9.10 REMAP_ADDR Register (Offset = 24h) [Reset = 00000000h]

REMAP_ADDR is shown in Table 8-45.

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Remap Address Register

Table 8-45. REMAP_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALUE	R/W	0h	This register is used to remap an incoming AHB address to a different address used by the FLASH device. 0h = Smallest value FFFFFFFFh = Highest possible value

8.9.11 MODE_BIT_CONFIG Register (Offset = 28h) [Reset = 00000200h]

MODE_BIT_CONFIG is shown in Table 8-46.

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Mode Bit Configuration Register

Table 8-46. MODE_BIT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RX_CRC_DATA_LOW	R	0h	RX CRC data (lower) The first CRC byte returned after RX data chunk. 0h = Smallest value FFh = Highest possible value
23-16	RX_CRC_DATA_UP	R	0h	RX CRC data (upper) The second CRC byte returned after RX data chunk. 0h = Smallest value FFh = Highest possible value
15	CRC_OUT_ENABLE	R/W	0h	CRC# output enable bit When enabled, the controller expects the Flash Device to toggle CRC data on both SPI clock edges in CRC->CRC# sequence and calculates CRC compliance accordingly. 0h = Disable 1h = Enable
14-11	RESERVED	R	0h	
10-8	CHUNK_SIZE	R/W	2h	It defines size of chunk after which CRC data is expected to show up on the SPI interface for write and read data transfers. 0h = Smallest value 7h = Highest possible value
7-0	MODE	R/W	0h	These are the 8 mode bits that are sent to the device following the address bytes if mode bit transmission has been enabled. 0h = Smallest value FFh = Highest possible value

8.9.12 SRAM_FILL Register (Offset = 2Ch) [Reset = 00000000h]

SRAM_FILL is shown in Table 8-47.

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SRAM Fill Register

Table 8-47. SRAM_FILL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SRAM_FILL_INDAC_WRITE	R	0h	SRAM Fill Level (Indirect Write Partition): Identifies the current fill level of the SRAM Indirect Write partition 0h = Smallest value FFFFh = Highest possible value
15-0	SRAM_FILL_INDAC_READ	R	0h	SRAM Fill Level (Indirect Read Partition): Identifies the current fill level of the SRAM Indirect Read partition 0h = Smallest value FFFFh = Highest possible value

8.9.13 TX_THRESH Register (Offset = 30h) [Reset = 00000001h]

TX_THRESH is shown in Table 8-48.

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TX Threshold Register

Table 8-48. TX_THRESH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	
4-0	LEVEL	R/W	1h	Defines the level at which the small TX FIFO not full interrupt is generated 0h = Smallest value 1Fh = Highest possible value

8.9.14 RX_THRESH Register (Offset = 34h) [Reset = 00000001h]

RX_THRESH is shown in Table 8-49.

Return to the Summary Table.

RX Threshold Register

Table 8-49. RX_THRESH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	
4-0	LEVEL	R/W	1h	Defines the level at which the small RX FIFO not empty interrupt is generated 0h = Smallest value 1Fh = Highest possible value

8.9.15 WRITE_COMPLETION_CTRL Register (Offset = 38h) [Reset = 00040005h]

WRITE_COMPLETION_CTRL is shown in Table 8-50.

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Write Completion Control Register: This register defines how the controller will poll the device following a write transfer

Table 8-50. WRITE_COMPLETION_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	POLL_REP_DELAY	R/W	0h	Defines additional delay for maintain Chip Select de-asserted during auto-polling phase 0h = Smallest value FFh = Highest possible value
23-16	POLL_COUNT	R/W	4h	Defines the number of times the controller should expect to see a true result from the polling in successive reads of the device register. 0h = Smallest value FFh = Highest possible value
15	ENABLE_POLLING_EXP	R/W	0h	Set to '1' for enabling auto-polling expiration. 0h = Disable 1h = Enable
14	DISABLE_POLLING	R/W	0h	This switches off the automatic polling function 0h = Disable 1h = Enable
13	POLLING_POLARITY	R/W	0h	Defines the polling polarity. If '1', then the write transfer to the device will be complete if the polled bit is equal to '1'. If '0', then the write transfer to the device will be complete if the polled bit is equal to '0'. 0h = Disable 1h = Enable
12	RESERVED	R	0h	
11	POLLING_ADDR_EN	R/W	0h	Enables address phase of auto-polling (Read Status) command. 0h = Disable 1h = Enable
10-8	POLLING_BIT_INDEX	R/W	0h	Defines the bit index that should be polled. A value of 010 means that bit 2 of the returned data will be polled for.A value of 111 means that bit 7 of the returned data will be polled for. 0h = Smallest value 7h = Highest possible value
7-0	OPCODE	R/W	5h	Defines the opcode that should be issued by the controller when it is automatically polling for device program completion. This command is issued followed all device write operations. By default, this will poll the standard device STATUS register using opcode 0x05 0h = Smallest value FFh = Highest possible value

8.9.16 NO_OF_POLLS_BEF_EXP Register (Offset = 3Ch) [Reset = FFFFFFFFh]

NO_OF_POLLS_BEF_EXP is shown in Table 8-51.

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Polling Expiration Register

Table 8-51. NO_OF_POLLS_BEF_EXP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NO_OF_POLLS_BEF_EXP	R/W	FFFFFFFFh	Number of polls cycles before expiration 0h = Smallest value FFFFFFFFh = Highest possible value

8.9.17 IRQ_STATUS Register (Offset = 40h) [Reset = 00000000h]

IRQ_STATUS is shown in Table 8-52.

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Interrupt Status Register: The status fields in this register are set when the described event occurs and the interrupt is enabled in the mask register. When any of these bit fields are set, the interrupt output is asserted high. The fields are each cleared by writing a 1 to the field. Note that bit fields 6 thru 10 are only valid when legacy SPI mode is active.

Table 8-52. IRQ_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	
19	ECC_FAIL	R/W1C	0h	ECC failure This interrupt informs the system that Flash Device reported ECC error. 0h = Disable 1h = Enable
18	TX_CRC_CHUNK_BRK	R/W1C	0h	TX CRC chunk was broken This interrupt informs the system that program page SPI transfer was discontinued somewhere inside the chunk. 0h = Disable 1h = Enable
17	RX_CRC_DATA_VAL	R/W1C	0h	RX CRC data valid New RX CRC data was captured from Flash Device 0h = Disable 1h = Enable
16	RX_CRC_DATA_ERR	R/W1C	0h	RX CRC data error CRC data from Flash Device does not correspond to the one dynamically calculated by the controller. 0h = Disable 1h = Enable
15	RESERVED	R	0h	
14	STIG_REQ_INT	R/W1C	0h	The controller is ready for getting another STIG request. 0h = Disable 1h = Enable
13	POLL_EXP_INT	R/W1C	0h	The maximum number of programmed polls cycles is expired 0h = Disable 1h = Enable
12	INDRD_SRAM_FULL	R/W1C	0h	Indirect Read Partition overflow: Indirect Read Partition of SRAM is full and unable to immediately complete indirect operation 0h = Disable 1h = Enable
11	RX_FIFO_FULL	R/W1C	0h	Small RX FIFO full: Current FIFO status can be ignored in non-SPI legacy mode 0h = FIFO is not full 1 : FIFO is full 1h = FIFO is full
10	RX_FIFO_NOT_EMPTY	R/W1C	0h	Small RX FIFO not empty: Current FIFO status can be ignored in non-SPI legacy mode 0h = FIFO has less than RX THRESHOLD entries, 1 : FIFO has >= THRESHOLD entries 1h = FIFO has >= THRESHOLD entries
9	TX_FIFO_FULL	R/W1C	0h	Small TX FIFO full: Current FIFO status can be ignored in non-SPI legacy mode 0h = FIFO is not full, 1 : FIFO is full 1h = FIFO is full
8	TX_FIFO_NOT_FULL	R/W1C	0h	Small TX FIFO not full: Current FIFO status can be ignored in non-SPI legacy mode 0h = FIFO has >= THRESHOLD entries, 1 : FIFO has less than THRESHOLD entries 1h = FIFO has less than THRESHOLD entries

Table 8-52. IRQ_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RECV_OVERFLOW	R/W1C	0h	Receive Overflow: This should only occur in Legacy SPI mode. Set if an attempt is made to push the RX FIFO when it is full. This bit is reset only by a system reset and cleared only when this register is read. If a new push to the RX FIFO occurs coincident with a register read this flag will remain set. 0h = no overflow has been detected. 1 : an overflow has occurred. 1h = an overflow has occurred.
6	INDIRECT_XFER_LEVEL_BREACH	R/W1C	0h	Indirect Transfer Watermark Level Breached 0h = Disable 1h = Enable
5	ILLEGAL_ACCESS_DET	R/W1C	0h	Illegal AHB access has been detected. AHB wrapping bursts and the use of SPLIT/RETRY accesses will cause this error interrupt to trigger. 0h = Disable 1h = Enable
4	PROT_WR_ATTEMPT	R/W1C	0h	Write to protected area was attempted and rejected. 0h = Disable 1h = Enable
3	INDIRECT_TRANSFER_REJECT	R/W1C	0h	Indirect operation was requested but could not be accepted. Two indirect operations already in storage. 0h = Disable 1h = Enable
2	INDIRECT_OP_DONE	R/W1C	0h	Indirect Operation Complete: Controller has completed last triggered indirect operation 0h = Disable 1h = Enable
1	UNDERFLOW_DET	R/W1C	0h	Underflow Detected: 0h = no underflow has been detected 1 : underflow is detected and an attempt to transfer data is made when the small TX FIFO is empty. This may occur when AHB write data is being supplied too slowly to keep up with the requested write operation This bit is reset only by a system reset and cleared only when the register is read. 1h = underflow is detected and an attempt to transfer data is made when the small TX FIFO is empty. This may occur when AHB write data is being supplied too slowly to keep up with the requested write operation This bit is reset only by a system reset and cleared only when the register is read.
0	MODE_M_FAIL	R/W1C	0h	Mode M Failure: Mode M failure indicates the voltage on pin n_ss_in is inconsistent with the SPI mode. Set =1 if n_ss_in is low in controller mode (multi-controller contention). These conditions will clear the spi_enable bit and disable the SPI. This bit is reset only by a system reset and cleared only when this register is read. 0h = no mode fault has been detected 1 : a mode fault has occurred 1h = a mode fault has occurred

8.9.18 IRQ_MASK Register (Offset = 44h) [Reset = 00000000h]

IRQ_MASK is shown in Table 8-53.

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Interrupt Mask: 0 : the interrupt for the corresponding interrupt status register bit is disabled. 1 : the interrupt for the corresponding interrupt status register bit is enabled.

Table 8-53. IRQ_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	
19	ECC_FAIL_MASK	R/W	0h	ECC failure Mask 0h = Disable 1h = Enable
18	TX_CRC_CHUNK_BRK_MASK	R/W	0h	TX CRC chunk was broken Mask 0h = Disable 1h = Enable
17	RX_CRC_DATA_VAL_MASK	R/W	0h	RX CRC data valid Mask 0h = Disable 1h = Enable
16	RX_CRC_DATA_ERR_MASK	R/W	0h	RX CRC data error Mask 0h = Disable 1h = Enable
15	RESERVED	R	0h	
14	STIG_REQ_MASK	R/W	0h	STIG request completion Mask 0h = Disable 1h = Enable
13	POLL_EXP_INT_MASK	R/W	0h	Polling expiration detected Mask 0h = Disable 1h = Enable
12	INDRD_SRAM_FULL_MASK	R/W	0h	Indirect Read Partition overflow mask 0h = Disable 1h = Enable
11	RX_FIFO_FULL_MASK	R/W	0h	Small RX FIFO full Mask 0h = Disable 1h = Enable
10	RX_FIFO_NOT_EMPTY_MASK	R/W	0h	Small RX FIFO not empty Mask 0h = Disable 1h = Enable
9	TX_FIFO_FULL_MASK	R/W	0h	Small TX FIFO full Mask 0h = Disable 1h = Enable
8	TX_FIFO_NOT_FULL_MASK	R/W	0h	Small TX FIFO not full Mask 0h = Disable 1h = Enable
7	RECV_OVERFLOW_MASK	R/W	0h	Receive Overflow Mask 0h = Disable 1h = Enable
6	INDIRECT_XFER_LEVEL_BREACH_MASK	R/W	0h	Transfer Watermark Breach Mask 0h = Disable 1h = Enable
5	ILLEGAL_ACCESS_DET_MASK	R/W	0h	Illegal Access Detected Mask 0h = Disable 1h = Enable
4	PROT_WR_ATTEMPT_MASK	R/W	0h	Protected Area Write Attempt Mask 0h = Disable 1h = Enable

Table 8-53. IRQ_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	INDIRECT_TRANSFER_REJECT_MASK	R/W	0h	Indirect Read Reject Mask 0h = Disable 1h = Enable
2	INDIRECT_OP_DONE_MASK	R/W	0h	Indirect Complete Mask 0h = Disable 1h = Enable
1	UNDERFLOW_DET_MASK	R/W	0h	Underflow Detected Mask 0h = Disable 1h = Enable
0	MODE_M_FAIL_MASK	R/W	0h	Mode M Failure Mask 0h = Disable 1h = Enable

8.9.19 LOWER_WR_PROT Register (Offset = 50h) [Reset = 00000000h]

LOWER_WR_PROT is shown in Table 8-54.

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Lower Write Protection Register

Table 8-54. LOWER_WR_PROT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SUBSECTOR	R/W	0h	The block number that defines the lower block in the range of blocks that is to be locked from writing. The definition of a block in terms of number of bytes is programmable via the Device Size Configuration register. 0h = Smallest value FFFFFFFFh = Highest possible value

8.9.20 UPPER_WR_PROT Register (Offset = 54h) [Reset = 00000000h]

UPPER_WR_PROT is shown in Table 8-55.

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Upper Write Protection Register

Table 8-55. UPPER_WR_PROT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SUBSECTOR	R/W	0h	The block number that defines the upper block in the range of blocks that is to be locked from writing. The definition of a block in terms of number of bytes is programmable via the Device Size Configuration register. 0h = Smallest value FFFFFFFFh = Highest possible value

8.9.21 WR_PROT_CTRL Register (Offset = 58h) [Reset = 00000000h]

WR_PROT_CTRL is shown in Table 8-56.

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Write Protection Control Register

Table 8-56. WR_PROT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	
1	ENB	R/W	0h	Write Protection Enable Bit: When set to 1, any AHB write access with an address within the protection region defined in the lower and upper write protection registers is rejected. An AHB error response is generated and an interrupt source triggered. When set to 0, the protection region is disabled. 0h = Disable 1h = Enable
0	INV	R/W	0h	Write Protection Inversion Bit: When set to 1, the protection region defined in the lower and upper write protection registers is inverted meaning it is the region that the system is permitted to write to. When set to 0, the protection region defined in the lower and upper write protection registers is the region that the system is not permitted to write to. 0h = Disable 1h = Enable

8.9.22 INDIRECT_READ_XFER_CTRL Register (Offset = 60h) [Reset = 00000000h]

INDIRECT_READ_XFER_CTRL is shown in Table 8-57.

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Indirect Read Transfer Control Register

Table 8-57. INDIRECT_READ_XFER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-6	NUM_IND_OPS_DONE	R	0h	This field contains the number of indirect operations which have been completed. This is used in conjunction with the indirect completion status field (bit 5). It is incremented by hardware when an indirect operation has completed. Write a 1 to bit 5 of this register to decrement it. 0h = Smallest value 3h = Highest possible value
5	IND_OPS_DONE_STATUS	R/W1C	0h	Indirect Completion Status: This field is set to 1 when an indirect operation has completed. Write a 1 to this field to clear it. 0h = Disable 1h = Enable
4	RD_QUEUED	R	0h	Two indirect read operations have been queued 0h = Disable 1h = Enable
3	SRAM_FULL	R/W1C	0h	SRAM Full: SRAM full and unable to immediately complete an indirect operation. Write a 1 to this field to clear it.\"; indirect operation (status) 0h = Disable 1h = Enable
2	RD_STATUS	R	0h	Indirect Read Status: Indirect read operation in progress (status) 0h = Disable 1h = Enable
1	CANCEL	W	0h	Cancel Indirect Read: Writing a 1 to this bit will cancel all ongoing indirect read operations. 0h = Disable 1h = Enable
0	START	W	0h	Start Indirect Read: Writing a 1 to this bit will trigger an indirect read operation. The assumption is that the indirect start address and the indirect number of bytes register is setup before triggering the indirect read operation. 0h = Disable 1h = Enable

8.9.23 INDIRECT_READ_XFER_WATERMARK Register (Offset = 64h) [Reset = 00000000h]

INDIRECT_READ_XFER_WATERMARK is shown in Table 8-58.

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Indirect Read Transfer Watermark Register

Table 8-58. INDIRECT_READ_XFER_WATERMARK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LEVEL	R/W	0h	Watermark Value: This represents the minimum fill level of the SRAM before a DMA peripheral access is permitted. When the SRAM fill level passes the watermark, an interrupt is also generated. This field can be disabled by writing a value of all zeroes. 0h = Smallest value FFFFFFFFh = Highest possible value

8.9.24 INDIRECT_READ_XFER_START Register (Offset = 68h) [Reset = 00000000h]

INDIRECT_READ_XFER_START is shown in Table 8-59.

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Indirect Read Transfer Start Address Register

Table 8-59. INDIRECT_READ_XFER_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR	R/W	0h	This is the start address from which the indirect access will commence its READ operation. 0h = Smallest value FFFFFFFFh = Highest possible value

8.9.25 INDIRECT_READ_XFER_NUM_BYTES Register (Offset = 6Ch) [Reset = 00000000h]

INDIRECT_READ_XFER_NUM_BYTES is shown in Table 8-60.

Return to the Summary Table.

Indirect Read Transfer Number Bytes Register

Table 8-60. INDIRECT_READ_XFER_NUM_BYTES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALUE	R/W	0h	This is the number of bytes that the indirect access will consume. This can be bigger than the configured size of SRAM. 0h = Smallest value FFFFFFFFh = Highest possible value

8.9.26 INDIRECT_WRITE_XFER_CTRL Register (Offset = 70h) [Reset = 00000000h]

INDIRECT_WRITE_XFER_CTRL is shown in Table 8-61.

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Indirect Write Transfer Control Register

Table 8-61. INDIRECT_WRITE_XFER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-6	NUM_IND_OPS_DONE	R	0h	This field contains the number of indirect operations which have been completed. This is used in conjunction with the indirect completion status field (bit 5). It is incremented by hardware when an indirect operation has completed. Write a 1 to bit 5 of this register to decrement it. 0h = Smallest value 3h = Highest possible value
5	IND_OPS_DONE_STATUS	R/W1C	0h	Indirect Completion Status: This field is set to 1 when an indirect operation has completed. Write a 1 to this field to clear it. 0h = Disable 1h = Enable
4	WR_QUEUED	R	0h	Two indirect write operations have been queued 0h = Disable 1h = Enable
3	RESERVED	R	0h	
2	WR_STATUS	R	0h	Indirect Write Status: Indirect write operation in progress (status) 0h = Disable 1h = Enable
1	CANCEL	W	0h	Cancel Indirect Write: Writing a 1 to this bit will cancel all ongoing indirect write operations. 0h = Disable 1h = Enable
0	START	W	0h	Start Indirect Write: Writing a 1 to this bit will trigger an indirect write operation. The assumption is that the indirect start address and the indirect number of bytes register is setup before triggering the indirect write operation. 0h = Disable 1h = Enable

8.9.27 INDIRECT_WRITE_XFER_WATERMARK Register (Offset = 74h) [Reset = FFFFFFFFh]

INDIRECT_WRITE_XFER_WATERMARK is shown in Table 8-62.

Return to the Summary Table.

Indirect Write Transfer Watermark Register

Table 8-62. INDIRECT_WRITE_XFER_WATERMARK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LEVEL	R/W	FFFFFFFFh	Watermark Value: This represents the maximum fill level of the SRAM before a DMA peripheral access is permitted. When the SRAM fill level falls below the watermark, an interrupt is also generated. This field can be disabled by writing a value of all ones. 0h = Smallest value FFFFFFFFh = Highest possible value

8.9.28 INDIRECT_WRITE_XFER_START Register (Offset = 78h) [Reset = 00000000h]

INDIRECT_WRITE_XFER_START is shown in Table 8-63.

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Indirect Write Transfer Start Address Register

Table 8-63. INDIRECT_WRITE_XFER_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR	R/W	0h	Start of Indirect Access: This is the start address from which the indirect access will commence its READ operation. 0h = Smallest value FFFFFFFFh = Highest possible value

8.9.29 INDIRECT_WRITE_XFER_NUM_BYTES Register (Offset = 7Ch) [Reset = 00000000h]

INDIRECT_WRITE_XFER_NUM_BYTES is shown in Table 8-64.

Return to the Summary Table.

Indirect Write Transfer Number Bytes Register

Table 8-64. INDIRECT_WRITE_XFER_NUM_BYTES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALUE	R/W	0h	Indirect Number of Bytes: This is the number of bytes that the indirect access will consume. This can be bigger than the configured size of SRAM. 0h = Smallest value FFFFFFFFh = Highest possible value

8.9.30 INDIRECT_TRIGGER_ADDR_RANGE Register (Offset = 80h) [Reset = 00000004h]

INDIRECT_TRIGGER_ADDR_RANGE is shown in Table 8-65.

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Indirect Trigger Address Range Register

Table 8-65. INDIRECT_TRIGGER_ADDR_RANGE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3-0	IND_RANGE_WIDTH	R/W	4h	This is the address offset of Indirect Trigger Address Register. 0h = Smallest value Fh = Highest possible value

8.9.31 FLASH_COMMAND_CTRL_MEM Register (Offset = 8Ch) [Reset = 00000000h]

FLASH_COMMAND_CTRL_MEM is shown in Table 8-66.

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Flash Command Control Memory Register

Table 8-66. FLASH_COMMAND_CTRL_MEM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	
28-20	MEM_BANK_ADDR	R/W	0h	The address of the Memory Bank which data will be read from. 0h = Smallest value 1FFh = Highest possible value
19	RESERVED	R	0h	
18-16	NB_OF_STIG_READ_BYTES	R/W	0h	It defines the number of read bytes for the extended STIG. 0h = Smallest value 7h = Highest possible value
15-8	MEM_BANK_READ_DATA	R	0h	Last requested data from the STIG Memory Bank. 0h = Smallest value FFh = Highest possible value
7-2	RESERVED	R	0h	
1	MEM_BANK_REQ_IN_PROGRESS	R	0h	Memory Bank data request in progress. 0h = Disable 1h = Enable
0	TRIGGER_MEM_BANK_REQ	W	0h	Trigger the Memory Bank data request. 0h = Disable 1h = Enable

8.9.32 FLASH_CMD_CTRL Register (Offset = 90h) [Reset = 00000000h]

FLASH_CMD_CTRL is shown in Table 8-67.

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Flash Command Control Register

Table 8-67. FLASH_CMD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CMD_OPCODE	R/W	0h	Command Opcode: The command opcode field should be setup before triggering the command. For example, 0x20 maps to SubSector Erase. Writing to the execute field (bit 0) of this register launches the command. NOTE : Using this approach to issue commands to the device will make use of the instruction type of the device instruction configuration register. If this field is set to 2'b00, then the command opcode, command address, command dummy bytes and command data will all be transferred in a serial fashion. If this field is set to 2'b01, then the command opcode, command address, command dummy bytes and command data will all be transferred in parallel using DQ0 and DQ1 pins. If this field is set to 2'b10, then the command opcode, command address, command dummy bytes and command data will all be transferred in parallel using DQ0, DQ1, DQ2 and DQ3 pins. 0h = Smallest value FFh = Highest possible value
23	ENB_READ_DATA	R/W	0h	Read Data Enable: Set to 1 if the command specified in the command opcode field (bits 31:24) requires read data bytes to be received from the device. 0h = Disable 1h = Enable
22-20	NUM_RD_DATA_BYTES	R/W	0h	Number of Read Data Bytes: Up to 8 data bytes may be read using this command. Set to 0 for 1 byte and 7 for 8 bytes. 0h = Smallest value 7h = Highest possible value
19	ENB_COMD_ADDR	R/W	0h	Command Address Enable: Set to 1 if the command specified in bits 31:24 requires an address. This should be setup before triggering the command via writing a 1 to the execute field. 0h = Disable 1h = Enable
18	ENB_MODE_BIT	R/W	0h	Mode Bit Enable: Set to 1 to ensure the mode bits as defined in the Mode Bit Configuration register are sent following the address bytes. 0h = Disable 1h = Enable
17-16	NUM_ADDR_BYTES	R/W	0h	Number of Address Bytes: Set to the number of address bytes required (the address itself is programmed in the FLASH COMMAND ADDRESS REGISTERS). This should be setup before triggering the command via bit 0 of this register. 2'b00 : 1 address byte 2'b01 : 2 address bytes 2'b10 : 3 address bytes 2'b11 : 4 address bytes 0h = Smallest value 3h = Highest possible value
15	ENB_WRITE_DATA	R/W	0h	Write Data Enable: Set to 1 if the command specified in the command opcode field requires write data bytes to be sent to the device. 0h = Disable 1h = Enable
14-12	NUM_WR_DATA_BYTES	R/W	0h	Number of Write Data Bytes: Up to 8 Data bytes may be written using this command Set to 0 for 1 byte, 7 for 8 bytes. 0h = Smallest value 7h = Highest possible value

Table 8-67. FLASH_CMD_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-7	NUM_DUMMY_CYCLES	R/W	0h	Number of Dummy cycles: Set to the number of dummy cycles required. This should be setup before triggering the command via the execute field of this register. 0h = Smallest value 1Fh = Highest possible value
6-3	CMD_GEN_FSM_STATE	R	0h	CMD_GEN_FSM_STATE is used to define the "Polling flag": If (CMD_GEN_FSM_STATE[6:3] = 0x7 or 0x8 or 0xa or 0xb) then "Polling_flag"=1 Usage: In order to make sure a write to external device was done and ended successfully, following condition should be met: "Command execution in progress" (FLASH_CMD_CTRL.CMD_EXEC_STATUS) = 0 AND "Polling flag" is '0'. Design NOTE: Command gen FSM polling states are: CMD_GEN_FSM_STATE == POLL_STATUS_AFTER_WRITE (0x7) CMD_GEN_FSM_STATE == POLL_STATUS_AFTER_WRITE2 (0x8) CMD_GEN_FSM_STATE == POLL_STATUS_WAIT (0xb) CMD_GEN_FSM_STATE == LET_TXFIFO_EMPTY (0xa) 0h = 0x0 1h = 0x1 2h = 0x2 3h = 0x3 4h = 0x4 5h = 0x5 6h = 0x6 7h = 0x7 8h = 0x8 Ah = 0xa Bh = 0xb Ch = 0xc
2	STIG_MEM_BANK_EN	R/W	0h	STIG Memory Bank enable bit. 0h = Disable 1h = Enable
1	CMD_EXEC_STATUS	R	0h	Command execution in progress. 0h = Disable 1h = Enable
0	CMD_EXEC	W	0h	Execute the command. 0h = Disable 1h = Enable

8.9.33 FLASH_CMD_ADDR Register (Offset = 94h) [Reset = 00000000h]

FLASH_CMD_ADDR is shown in Table 8-68.

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Flash Command Address Register

Table 8-68. FLASH_CMD_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR	R/W	0h	Command Address: This should be setup before triggering the command with execute field (bit 0) of the Flash Command Control register. It is the address used by the command specified in the opcode field (bits 31:24) of the Flash Command Control register. 0h = Smallest value FFFFFFFFh = Highest possible value

8.9.34 FLASH_RD_DATA_LOWER Register (Offset = A0h) [Reset = 00000000h]

FLASH_RD_DATA_LOWER is shown in Table 8-69.

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Flash Command Read Data Register (Lower)

Table 8-69. FLASH_RD_DATA_LOWER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R	0h	This is the data that is returned by the flash device for any status or configuration read operation carried out by triggering the event in the control register. The register will be valid when the polling bit in the control register is low. 0h = Smallest value FFFFFFFFh = Highest possible value

8.9.35 FLASH_RD_DATA_UPPER Register (Offset = A4h) [Reset = 00000000h]

FLASH_RD_DATA_UPPER is shown in Table 8-70.

Return to the Summary Table.

Flash Command Read Data Register (Upper)

Table 8-70. FLASH_RD_DATA_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R	0h	This is the data that is returned by the FLASH device for any status or configuration read operation carried out by triggering the event in the control register. The register will be valid when the polling bit in the control register is low. 0h = Smallest value FFFFFFFFh = Highest possible value

8.9.36 FLASH_WR_DATA_LOWER Register (Offset = A8h) [Reset = 00000000h]

FLASH_WR_DATA_LOWER is shown in Table 8-71.

Return to the Summary Table.

Flash Command Write Data Register (Lower)

Table 8-71. FLASH_WR_DATA_LOWER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Command Write Data Lower Byte: This is the command write data lower byte. This should be setup before triggering the command with execute field (bit 0) of the Flash Command Control register. It is the data that is to be written to the flash for any status or configuration write operation carried out by triggering the event in the Flash Command Control register. 0h = Smallest value FFFFFFFFh = Highest possible value

8.9.37 FLASH_WR_DATA_UPPER Register (Offset = ACh) [Reset = 00000000h]

FLASH_WR_DATA_UPPER is shown in Table 8-72.

Return to the Summary Table.

Flash Command Write Data Register (Upper)

Table 8-72. FLASH_WR_DATA_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Command Write Data Upper Byte: This is the command write data upper byte. This should be setup before triggering the command with execute field (bit 0) of the Flash Command Control register. It is the data that is to be written to the flash for any status or configuration write operation carried out by triggering the event in the Flash Command Control register. 0h = Smallest value FFFFFFFFh = Highest possible value

8.9.38 POLLING_FLASH_STATUS Register (Offset = B0h) [Reset = 00000000h]

POLLING_FLASH_STATUS is shown in Table 8-73.

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Polling Flash Status Register

Table 8-73. POLLING_FLASH_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	
20-16	DEVICE_STATUS_NB_DUMMY	R/W	0h	Number of dummy cycles for auto-polling 0h = Smallest value 1Fh = Highest possible value
15-9	RESERVED	R	0h	
8	DEVICE_STATUS_VALID	R	0h	Device Status Valid: This should be set when value in bits from 7 to 0 is valid. 0h = Disable 1h = Enable
7-0	DEVICE_STATUS	R	0h	Defines actual Status Register of Device 0h = Smallest value FFh = Highest possible value

8.9.39 PHY_CONFIGURATION Register (Offset = B4h) [Reset = 40000000h]

PHY_CONFIGURATION is shown in Table 8-74.

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PHY Configuration Register

Table 8-74. PHY_CONFIGURATION Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_CONFIG_RESYNC	W	0h	This bit is used for re-synchronisation delay lines to update them with values from TX DLL Delay and RX DLL Delay fields. 0h = Disable 1h = Enable
30	PHY_CONFIG_RESET	W	1h	DLL Reset bit: This bit is used for reset of Delay Lines by software. 0h = Disable 1h = Enable
29	PHY_CONFIG_RX_DLL_BYPASS	R/W	0h	RX DLL Bypass: This field determines id RX DLL is bypassed. 0h = Disable 1h = Enable
28-23	RESERVED	R	0h	
22-16	PHY_CONFIG_TX_DLL_DELAY	R/W	0h	TX DLL Delay: This field determines the number of delay elements to insert on data path between ref_clk and spi_clk. 0h = Smallest value 7Fh = Highest possible value
15-7	RESERVED	R	0h	
6-0	PHY_CONFIG_RX_DLL_DELAY	R/W	0h	RX DLL Delay: This field determines the number of delay elements to insert on data path between ref_clk and rx_dll_clk. 0h = Smallest value 7Fh = Highest possible value

8.9.40 PHY_MASTER_CONTROL Register (Offset = B8h) [Reset = 00800000h]

PHY_MASTER_CONTROL is shown in Table 8-75.

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PHY DLL controller Control Register

Table 8-75. PHY_MASTER_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	
24	PHY_MASTER_LOCK_MODE	R/W	0h	Determines if the controller delay line locks on a full cycle or half cycle of delay. 0h = Disable 1h = Enable
23	PHY_MASTER_BYPASS_MODE	R/W	1h	Controls the bypass mode of the controller and peripheral DLLs. 0h = Disable 1h = Enable
22-20	PHY_MASTER_PHASE_DETECT_SELECTOR	R/W	0h	Selects the number of delay elements to be inserted between the phase detect flip-flops. 0h = Smallest value 7h = Highest possible value
19	RESERVED	R	0h	
18-16	PHY_MASTER_NB_INDICATIONS	R/W	0h	Holds the number of consecutive increment or decrement indications. 0h = Smallest value 7h = Highest possible value
15-7	RESERVED	R	0h	
6-0	PHY_MASTER_INITIAL_DELAY	R/W	0h	This value is the initial delay value for the DLL. 0h = Smallest value 7Fh = Highest possible value

8.9.41 DLL_OBSERVABLE_LOWER Register (Offset = BCh) [Reset = 00000000h]

DLL_OBSERVABLE_LOWER is shown in Table 8-76.

Return to the Summary Table.

DLL Observable Register Lower

Table 8-76. DLL_OBSERVABLE_LOWER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	DLL_OBSERVABLE_LOWER_DLL_LOCK_INC	R	0h	Holds the state of the cumulative dll_lock_inc register. 0h = Smallest value FFh = Highest possible value
23-16	DLL_OBSERVABLE_LOWER_DLL_LOCK_DEC	R	0h	Holds the state of the cumulative dll_lock_dec register. 0h = Smallest value FFh = Highest possible value
15	DLL_OBSERVABLE_LOWER_LOOPBACK_LOCK	R	0h	This bit indicates that lock of loopback is done. 0h = Disable 1h = Enable
14-8	DLL_OBSERVABLE_LOWER_LOCK_VALUE	R	0h	Reports the DLL encoder value from the controller DLL to the peripheral DLLs. 0h = Smallest value 7Fh = Highest possible value
7-3	DLL_OBSERVABLE_LOWER_UNLOCK_COUNTER	R	0h	Reports the number of increments or decrements required for the controller DLL to complete the locking process. 0h = Smallest value 1Fh = Highest possible value
2-1	DLL_OBSERVABLE_LOWER_LOCK_MODE	R	0h	Defines the mode in which the DLL has achieved the lock. 0h = Smallest value 3h = Highest possible value
0	DLL_OBSERVABLE_LOWER_DLL_LOCK	R	0h	Indicates status of DLL. 0h = Disable 1h = Enable

8.9.42 DLL_OBSERVABLE_UPPER Register (Offset = C0h) [Reset = 00000000h]

DLL_OBSERVABLE_UPPER is shown in Table 8-77.

Return to the Summary Table.

DLL Observable Register Upper

Table 8-77. DLL_OBSERVABLE_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	
22-16	DLL_OBSERVABLE_UPPER_TX_DECODER_OUTPUT	R	0h	Holds the encoded value for the TX delay line for this slice. 0h = Smallest value 7Fh = Highest possible value
15-7	RESERVED	R	0h	
6-0	DLL_OBSERVABLE__UPPER_RX_DECODER_OUTPUT	R	0h	Holds the encoded value for the RX delay line for this slice. 0h = Smallest value 7Fh = Highest possible value

8.9.43 OPCODE_EXT_LOWER Register (Offset = E0h) [Reset = 13EDFA00h]

OPCODE_EXT_LOWER is shown in Table 8-78.

Return to the Summary Table.

Opcode Extension Register (Lower)

Table 8-78. OPCODE_EXT_LOWER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	EXT_READ_OPCODE	R/W	13h	Supplement byte of any Read Opcode 0h = Smallest value FFh = Highest possible value
23-16	EXT_WRITE_OPCODE	R/W	EDh	Supplement byte of any Write Opcode 0h = Smallest value FFh = Highest possible value
15-8	EXT_POLL_OPCODE	R/W	FAh	Supplement byte of any Polling Opcode 0h = Smallest value FFh = Highest possible value
7-0	EXT_STIG_OPCODE	R/W	0h	Supplement byte of any STIG Opcode 0h = Smallest value FFh = Highest possible value

8.9.44 OPCODE_EXT_UPPER Register (Offset = E4h) [Reset = 06F90000h]

OPCODE_EXT_UPPER is shown in Table 8-79.

Return to the Summary Table.

Opcode Extension Register (Upper)

Table 8-79. OPCODE_EXT_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	WEL_OPCODE	R/W	6h	First byte of any WEL Opcode 0h = Smallest value FFh = Highest possible value
23-16	EXT_WEL_OPCODE	R/W	F9h	Supplement byte of any WEL Opcode 0h = Smallest value FFh = Highest possible value
15-0	RESERVED	R	0h	

8.9.45 MODULE_ID Register (Offset = FCh) [Reset = 04000300h]

MODULE_ID is shown in Table 8-80.

Return to the Summary Table.

Module ID Register

Table 8-80. MODULE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	FIX_PATCH	R	4h	Fix/path number related to revision described by 3 LSBs of this register 0h = Smallest value FFh = Highest possible value
23-8	MODULE_ID	R	3h	Module/Revision ID number 0h = Smallest value FFFFh = Highest possible value
7-2	RESERVED	R	0h	
1-0	CONF	R	0h	Configuration ID number: 0 : OCTAL + PHY Configuration 1 : OCTAL Configuration 2 : QUAD + PHY Configuration 3 : QUAD Configuration 0h = Smallest value 3h = Highest possible value

8.10 HOST_XIP Registers

Table 8-81 lists the memory-mapped registers for the HOST_XIP registers. All register offset addresses not listed in Table 8-81 should be considered as reserved locations and the register contents should not be modified.

Table 8-81. HOST_XIP Registers

Offset	Acronym	Register Name	Section
14h	SWCHDLY	Register to configure the extra delay added before the device switch	Section 8.10.1
28h	RCMCLKSTA	Clock Status	Section 8.10.2
1000h	UDSCFG0	Secure Source Address	Section 8.10.3
1004h	UDSCFG1	Secure Destination Address	Section 8.10.4
1008h	UDSCFG2	Secured Length Configuration	Section 8.10.5
100Ch	UDSCFG3	Security Mode Configuration	Section 8.10.6
1010h	UDSCTL0	Secure Transfer Start	Section 8.10.7
1014h	UDSCTL1	Secure Operation Cancellation Control	Section 8.10.8
1020h	UDSSTA	Secure Status Flags	Section 8.10.9
1024h	UDSIRQ	Secured Interrupt Status	Section 8.10.10
102Ch	UDSSTA1	uDMA secured Status bits in addition to [UDMSSTA] register	Section 8.10.11
1040h	UDSPERCFG	Peripheral Security Configuration	Section 8.10.12
1060h	UDSPERSEL	Register to select the peripheral to be served on secured channel	Section 8.10.13
1064h	UDNSPERSEL	Register to select the peripheral to be served on non secured channel	Section 8.10.14
2000h	UDNSCFG0	Nonsecure Source Address	Section 8.10.15
2004h	UDNSCFG1	Non-Secure Destination Address	Section 8.10.16
2008h	UDNSCFG2	uDMA non-secured job Length	Section 8.10.17
200Ch	UDNSCFG3	DMA Security Mode	Section 8.10.18
2010h	UDNSCTL0	uDMA non-secured job kick	Section 8.10.19
2014h	UDNSCTL1	Non-Secure Job Termination	Section 8.10.20
2020h	UDNSSTA	Non-Secure Status	Section 8.10.21
2024h	UDNSIRQ	Non-Secure Interrupt Status	Section 8.10.22
2028h	UTHRCNF	Threshold Configuration	Section 8.10.23
202Ch	UDNSSTA1	Non-Secure Status Extension	Section 8.10.24
2040h	UDNSPERCFG	Non secure peirpheral job configuration	Section 8.10.25
3000h	OTOSMEM	OSPI Configuration	Section 8.10.26

Complex bit access types are encoded to fit into small table cells. Table 8-82 shows the codes that are used for access types in this section.

Table 8-82. HOST_XIP Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.10.1 SWCHDLY Register (Offset = 14h) [Reset = 00000001h]

SWCHDLY is shown in Table 8-83.

Return to the Summary Table.

Register to configure the extra delay added before the device switch

Table 8-83. SWCHDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	
1-0	DEVSWCHDLY	R/W	1h	This field configures the extra delay added before the device switch 0h = No extra delay 1h = Extra delay of 16 cycles 2h = Extra delay of 32 cycles 3h = Extra delay of 64 cycles

8.10.2 RCMCLKSTA Register (Offset = 28h) [Reset = 00000000h]

RCMCLKSTA is shown in Table 8-84.

Return to the Summary Table.

(ICG) Clock Status from HOST_XIP_RCM Module

Table 8-84. RCMCLKSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	OSPIREF	R	0h	1 - Force clk (even if sw_disable_clk is 1 or clk_req is 0) 0 - Clock is not forced, but gated with clk_req input port
1	SOC	R	0h	1 - Force clk (even if sw_disable_clk is 1 or clk_req is 0) 0 - Clock is not forced, but gated with clk_req input port
0	HOSTXIP	R	0h	1 - Force clk (even if sw_disable_clk is 1 or clk_req is 0) 0 - Clock is not forced, but gated with clk_req input port

8.10.3 UDSCFG0 Register (Offset = 1000h) [Reset = 00000000h]

UDSCFG0 is shown in Table 8-85.

Return to the Summary Table.

uDMA source address for secured read controller. Must be Word aligned.

Table 8-85. UDSCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	JSRCADDR	R/W	0h	DMA SEC JOB SRC ADDR: Specifies source address for secured read controller. Source address must comply with bit.26 to enable Sec/Non-Sec accesses, otherwise transactions will be blocked.

8.10.4 UDSCFG1 Register (Offset = 1004h) [Reset = 00000000h]

UDSCFG1 is shown in Table 8-86.

Return to the Summary Table.

uDMA destination address for secured write controller. Must be Word aligned.

Table 8-86. UDSCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	JDESTADDR	R/W	0h	DMA SEC JOB DST ADDR: Specifies destination address for secured write controller. Destination address must comply with bit.26 to enable Sec/Non-Sec accesses, otherwise transactions will be blocked.

8.10.5 UDSCFG2 Register (Offset = 1008h) [Reset = 00000000h]

UDSCFG2 is shown in Table 8-87.

Return to the Summary Table.

uDMA secured job Length

Table 8-87. UDSCFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17-0	JLEN	R/W	0h	DMA SEC JOB LENGTH: Resolution - 32 bits/4 bytes Maximum configurable job size - 1 Mega byte (256K Words). (Maximum available size in MEMSS is 1MB).

8.10.6 UDSCFG3 Register (Offset = 100Ch) [Reset = 00000000h]

UDSCFG3 is shown in Table 8-88.

Return to the Summary Table.

uDMA Direction

Table 8-88. UDSCFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	SMODE	R/W	0h	Secure channel mode 0: Memory Mode 1: Peripheral Mode
0	JDIR	R/W	0h	DMA SEC JOB MODE: 0 - Data movement from External memory to Internal memory/Peripheral 1 - Data movement from Internal memory/Peripheral to External memory.

8.10.7 UDSCTL0 Register (Offset = 1010h) [Reset = 00000000h]

UDSCTL0 is shown in Table 8-89.

Return to the Summary Table.

uDMA secured job kick

Table 8-89. UDSCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	JSTART	W	0h	DMA SEC JOB START WRCL: Start command for uDMA to start working on secured configured job.

8.10.8 UDSCTL1 Register (Offset = 1014h) [Reset = 00000000h]

UDSCTL1 is shown in Table 8-90.

Return to the Summary Table.

uDMA secured job abort

Table 8-90. UDSCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	JCLR	W	0h	DMA SEC JOB CLEAR WRCL: Clear command for uDMA to stop working and clear configuration.

8.10.9 UDSSTA Register (Offset = 1020h) [Reset = 00000000h]

UDSSTA is shown in Table 8-91.

Return to the Summary Table.

uDMA secured Status bits

Table 8-91. UDSSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	
27-8	RDWRDSLFT	R	0h	DMA SEC JOB READ WORDS LEFT: number of read words left in sec job. Note: This value would be updated on a read to this register. [UDSSTA1.WRWRDSLFT] is updated on a read to this register This register value shows number of words in 32 bit when field [UDSCFG3.JDIR] is configured '0' else shows number of words in 8/16/32 bit based on the configuration of [UDSCFG3.SMODE] and [UDPERCFG.SWORDSZ] fields
7-5	RESERVED	R	0h	Reserved
4	JINPROG	R	0h	DMA SEC JOB IN PROGRESS: 1- sec job is currently in progress and being executed by uDMA
3-1	RESERVED	R	0h	Reserved
0	JSTA	R	0h	DMA SEC JOB ACTIVE: Status bit to indicate that DMA is processing a secured job. When this bit is set, SW has written all the job parameters and also provided a start_pulse to HW, and cannot change job parameters without clear_pulse. Job will wait to be executed (indicated by job_in_progress)

8.10.10 UDSIRQ Register (Offset = 1024h) [Reset = 00000000h]

UDSIRQ is shown in Table 8-92.

Return to the Summary Table.

uDMA secured IRQ Status bits

Table 8-92. UDSIRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	JIRQBEDIR	R	0h	Bus Error direction 0: Source bus 1: Destination bus Note: Source and destination is determined based on JDIR configuration
1-0	JIRQSTA	R	0h	Status vector for IRQ indication for secured DMA IRQ: 2'd0 - DMA done. 2'd1 - DMA Internal bus error occurred. check SEC_STATUS in order to recovers

8.10.11 UDSSTA1 Register (Offset = 102Ch) [Reset = 00000000h]

UDSSTA1 is shown in Table 8-93.

Return to the Summary Table.

uDMA secured Status bits in addition to [UDMSSTA] register

Table 8-93. UDSSTA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	
27-8	WRWRDSLFT	R	0h	DMA SEC JOB WRITE WORDS LEFT: Number of write words left in sec job. Note: This value would be updated only on a read to [UDSSTA] register. This register value shows number of words in 32 bit when field [UDSCFG3.JDIR] is configured '1' else shows number of words in 8/16/32 bit based on the configuration of [UDSCFG3.SMODE] and [UDPERCFG.SWORDSZ] fields
7-0	WRDOFST	R	0h	DMA SEC PERIPH WORD OFFSET: Number of words left in a peripheral block. Note: This value would be updated only on a read to [UDSSTA] register. This register value shows number of words in 8/16/32 bit based on the configuration of [UDSCFG3.SMODE] and [UDPERCFG.SWORDSZ] fields

8.10.12 UDSPERCFG Register (Offset = 1040h) [Reset = 00000000h]

UDSPERCFG is shown in Table 8-94.

Return to the Summary Table.

uDMA Secure channel peripheral config register

Table 8-94. UDSPERCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8	SENCLRSRT	R/W	0h	Enable uDMA to set a rd/wr clear pulse at the beginning of a job
7-2	SPERBLKSZ	R/W	0h	Secure channel peripheral block size(in 32bits/4bytes) Multiplication of Word size Upto 64 words based on the word size selected Block = block_size * word_size
1-0	SPERWDSZ	R/W	0h	Secure channel peripheral job word size 8/16/32 (Word Size of 1/2/4 bytes) Sel_0 - 32 bit Sel_1 - 16 bit Sel_2 - 8 bit

8.10.13 UDSPERSEL Register (Offset = 1060h) [Reset = 00000000h]

UDSPERSEL is shown in Table 8-95.

Return to the Summary Table.

Register to select the peripheral to be served on secured channel

Table 8-95. UDSPERSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3-0	SPERSEL	R/W	0h	Select the peripheral to serve job. This field along with [UDMA_SEC_MODE.MEM_SEC_MODE] selects the peripheral to the channel 0x0 UART0 0x1 UART1 0x2 SPI0 0x3 SPI1 0x4 I2C0 0x5 I2C1 0x6 SDMMC 0x7 SDIO 0x8 MCAN 0x9 ADC 0xA PDM 0xB HIF

8.10.14 UDNSPERSEL Register (Offset = 1064h) [Reset = 00000000h]

UDNSPERSEL is shown in Table 8-96.

Return to the Summary Table.

Register to select the peripheral to be served on non secured channel

Table 8-96. UDNSPERSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3-0	NSPERSEL	R/W	0h	Select the peripheral to serve job. This field along with [UDMA_NONSEC_MODE.MEM_NON_SEC_MODE] selects the peripheral to the channel 0x0 UART0 0x1 UART1 0x2 SPI0 0x3 SPI1 0x4 I2C0 0x5 I2C1 0x6 SDMMC 0x7 SDIO 0x8 MCAN 0x9 ADC 0xA PDM 0xB HIF

8.10.15 UDNSCFG0 Register (Offset = 2000h) [Reset = 00000000h]

UDNSCFG0 is shown in Table 8-97.

Return to the Summary Table.

uDMA source address for non-secured read controller. Must be Word aligned.

Table 8-97. UDNSCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	JSRCADDR	R/W	0h	DMA NONSEC JOB SRC ADDR: Specifies source address for non-secured read controller. Source address must comply with bit.26 to enable Sec/Non-Sec accesses, otherwise transactions will be blocked. In case using SAU to define secured memory region 'inside' the non-secured, this channel will allow this.

8.10.16 UDNSCFG1 Register (Offset = 2004h) [Reset = 00000000h]

UDNSCFG1 is shown in Table 8-98.

Return to the Summary Table.

uDMA destination address for non-secured write controller. Must be Word aligned.

Table 8-98. UDNSCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	JDESTADDR	R/W	0h	DMA NONSEC JOB DST ADDR: Specifies destination address for non-secured write controller. Destination address must comply with bit.26 to enable Sec/Non-Sec accesses, otherwise transactions will be blocked. In case using SAU to define secured memory region 'inside' the non-secured, this channel will allow this.

8.10.17 UDNSCFG2 Register (Offset = 2008h) [Reset = 00000000h]

UDNSCFG2 is shown in Table 8-99.

Return to the Summary Table.

uDMA non-secured job Length

Table 8-99. UDNSCFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17-0	JLEN	R/W	0h	DMA NONSEC JOB LENGTH: Resolution - 32 bits/4bytes Maximum configurable job size - 1 Mega byte (256K Words). (Maximum available size in MEMSS is 1MB).

8.10.18 UDNSCFG3 Register (Offset = 200Ch) [Reset = 00000000h]

UDNSCFG3 is shown in Table 8-100.

Return to the Summary Table.

uDMA Direction

Table 8-100. UDNSCFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	NSMODE	R/W	0h	Non secure channel mode 0: Memory Mode 1: Peripheral Mode
0	JDIR	R/W	0h	DMA NONSEC JOB MODE: 0 - Data movement from External memory to Internal memory. 1 - Data movement from Internal memory to External memory.

8.10.19 UDNSCTL0 Register (Offset = 2010h) [Reset = 00000000h]

UDNSCTL0 is shown in Table 8-101.

Return to the Summary Table.

uDMA non-secured job kick

Table 8-101. UDNSCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	JSTART	W	0h	DMA NONSEC JOB START WRCL: Start command for uDMA to start working on non-secured configured job.

8.10.20 UDNSCTL1 Register (Offset = 2014h) [Reset = 00000000h]

UDNSCTL1 is shown in Table 8-102.

Return to the Summary Table.

uDMA non-secured job abort

Table 8-102. UDNSCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	JCLR	W	0h	DMA NONSEC JOB CLEAR WRCL: Clear command for uDMA to stop working and clear configuration.

8.10.21 UDNSSTA Register (Offset = 2020h) [Reset = 00000000h]

UDNSSTA is shown in Table 8-103.

Return to the Summary Table.

uDMA non-secured Status bits

Table 8-103. UDNSSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	
27-8	RDWRDSLFT	R	0h	DMA NONSEC JOB READ WORDS LEFT: Number of read words left in nonsec job Note: This value would be updated on a read to this register. [UDNSSTA1.WRWRDSLFT] is updated on a read to this register This register value shows number of words in 32 bit when field [UDNSCFG3.JDIR] is configured '0' else shows number of words in 8/16/32 bit based on the configuration of [UDNSCFG3.NSMODE] and [UDPERCFG.NSWORDSZ] fields
7-5	RESERVED	R	0h	Reserved
4	JINPROG	R	0h	DMA NONSEC JOB IN PROGRESS: 1- nonsec job is currently in progress and being executed by uDMA
3-1	RESERVED	R	0h	Reserved
0	JSTA	R	0h	DMA NONSEC JOB ACTIVE: Status bit to indicate that DMA is processing a non-secured job. When this bit is set, SW has written all the job parameters and also provided a start_pulse to HW, and cannot change job parameters without clear_pulse. Job will wait to be executed (indicated by job_in_progress)

8.10.22 UDNSIRQ Register (Offset = 2024h) [Reset = 00000000h]

UDNSIRQ is shown in Table 8-104.

Return to the Summary Table.

uDMA non-secured IRQ Status bits

Table 8-104. UDNSIRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	JIRQBEDIR	R	0h	Bus Error direction 0: Source bus 1: Destination bus Note: Source and destination is determined based on JDIR configuration
1-0	JIRQSTA	R	0h	Status vector for IRQ indication for non-secured DMA IRQ: 2'd0 - DMA done. 2'd1 - DMA bus error occurred. check NONSEC_STATUS in order to recovers

8.10.23 UTHRCNF Register (Offset = 2028h) [Reset = 00000090h]

UTHRCNF is shown in Table 8-105.

Return to the Summary Table.

uDMA threshold configuration

Table 8-105. UTHRCNF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6-5	BURSTVAL	R/W	0h	FIFO WRITE BURST LEN: After uDMA will reached the threshold, uDMA will sent the data in blocks. 0x0 : block size = 4 word 0x1 : block size = 8 word 0x2 : block size = 16 word 0x3 : block size = 32 word
4-0	THRVAL	R/W	10h	FIFO WRITE THRESHOLD: In case of write to ext mem, uDMA will reach the threshold and after that will send the data to the ext mem Note: 0(Zero) is not allowed

8.10.24 UDNSSTA1 Register (Offset = 202Ch) [Reset = 00000000h]

UDNSSTA1 is shown in Table 8-106.

Return to the Summary Table.

uDMA non-secured Status bits in addition to [UDNSSTA] register

Table 8-106. UDNSSTA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	
27-8	WRDOFST	R	0h	DMA NONSEC JOB WRITE WORDS LEFT: Number of write words left in nonsec job. Note: This value would be updated only on a read to [UDNSSTA] register. This register value shows number of words in 32 bit when field [UDNSCFG3.JDIR] is configured '1' else shows number of words in 8/16/32 bit based on the configuration of [UDNSCFG3.NSMODE] and [UDPERCFG.NSWORDSZ] fields
7-0	WRWRDSLFT	R	0h	DMA NONSEC PERIPH WORD OFFSET: Number of words left in a peripheral block. Note: This value would be updated only on a read to [UDNSSTA] register. This register value shows number of words in 8/16/32 bit based on the configuration of [UDNSCFG3.NSMODE] and [UDPERCFG.NSWORDSZ] fields

8.10.25 UDNSPERCFG Register (Offset = 2040h) [Reset = 00000000h]

UDNSPERCFG is shown in Table 8-107.

Return to the Summary Table.

Non secure peirpheral job configuration

Table 8-107. UDNSPERCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8	NSENCLRSRT	R/W	0h	Enable uDMA to set a rd/wr clear pulse at the beginning of a job
7-2	NSPERBLSZ	R/W	0h	Non-secure channel peripheral job block size(in 32bits/4bytes) Multiplication of Word size. Upto 64 words based on Word size Block = block_size * word_size
1-0	NSPERWDSZ	R/W	0h	Non-secure channel peripheral job word size 8/16/32 (Word Size of 1/2/4 bytes) Sel_0 - 32 bit Sel_1 - 16 bit Sel_2 - 8 bit

8.10.26 OTOSMEM Register (Offset = 3000h) [Reset = 00000000h]

OTOSMEM is shown in Table 8-108.

Return to the Summary Table.

For Load/Read xSPI config job in OTFDE memory

Table 8-108. OTOSMEM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	WDATACFG	R/W	0h	OTFDE CFG OSPI 81FC WR MEM xSPI config Memory wr/rd access (under OTFDE module)

Chapter 9

Hardware Security Module (HSM)

This section describes the Hardware Security Module (HSM).

9.1 Introduction

The CC35xx devices have an integrated hardware security module (HSM) supporting an isolated environment for cryptographic, key management, secure counters, and random number generation operations. Selected algorithms are protected from differential power analysis (DPA) side channel attacks. Together with a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), the system supports secure and future proof IoT applications to be easily built on the platform

9.2 Overview

The following cryptographic functions using energy efficient accelerators and RNG functions are accelerated by the HSM:

- Key Agreement Schemes
  - Elliptic Curve Diffie-Hellman with static or ephemeral keys (ECDH and ECDHE)
  - Elliptic Curve Password Authenticated Key Exchange by Juggling (ECJ-PAKE)
  - Diffie Hellman with static or ephemeral keys (DH, and DHE)
- Key Derivation Methods:
  - Random (from DRBG)
  - SHA2 HMAC PRF (Pseudorandom Function)
  - AES CMAC PRF
- Signature Processing
  - Elliptic Curve Diffie-Hellman Digital Signature Algorithm (ECDSA)
  - Edwards-curve Digital Signature Algorithm (EdDSA)
  - RSA PKCS #1 v1.5
  - RSA PSS
- Message Authentication Codes
  - AES CBC-MAC
  - AES CMAC
  - HMAC with SHA2-224, SHA2-256, SHA2-384, and SHA2-512
  - HMAC with SHA3-224, SHA2-256, SHA2-384, and SHA2-512
- Block Cipher Modes of Operation
  - AES CCM and AES CCM* (CCM-Star)
  - AES GCM
  - AES ECB
  - AES CBC
  - AES CTR
- Hash Algorithms
  - SHA3-224
  - SHA3-256
  - SHA3-384
  - SHA3-512
  - SHA2-224
  - SHA2-256
  - SHA2-384
  - SHA2-512
- Random Number Generation:
  - NIST SP800-90B compliant TRNG (True Random Number Generator)
  - AES-CTR DRBG (Deterministic Random Bit Generator)

Cryptographic key sizes and types include:

- Advanced Encryption Standard (AES) key sizes of 128, 192, and 256bits
- RSA key sizes up to 3072-bits (Sign and Verify supported), and up to 4096-bits (Verify only)
- Diffie-Hellman key sizes of 2048-bits and 3072-bits
- Elliptic Curve Support

  - Short Weierstrass
    - NIST-P224 (secp224r1), NIST-P256 (secp256r1), NIST-P384 (secp384r1), NIST-P521 (secp521r1)
    - Brainpool-256R1, Brainpool-384R1, Brainpool-512R1
  - Montgomery
    - Curve25519
  - Twisted Edwards form, such as:
    - Ed25519

DPA countermeasures are implemented for:

- AES operations
- ECDH operations involving private key material
- ECDSA and EdDSA sign operations
- RSA sign operations on 2048-bit and smaller keys

The HSM also has its own data RAM region that is not accessible to the rest of the system (system CPU, DMA, debug access, etc.). The data RAM region is retained in low power modes, supporting quick power up of the HSM and retention of key material. In addition to the storage of key material in data RAM, the HSM supports importing and exporting wrapped key material (NIST SP800-38F) with a key unique to the device, known as a HW Unique Key (HUK). This allows the wrapped keys to be securely stored anywhere in the system's nonvolatile (Flash) memory.

The HSM is accessible to the application running on the system CPU in a controlled manner via the HSM mailbox interface. The HSM is a bus controller in the device and can access the system memory directly enabling better efficiency for moving data in and out during cryptographic operations.

The HSM supports master DMA with AHB I/F to device memory mapping. The DMA access to memory is controlled by firewall that classify access according to mailbox task type and operation policy

9.3 Mailbox and Register Access Firewall

The HSM MMR address space is divided into 3 sub-section.

- Mailbox 1
- Mailbox 2
- Control Registers

Each of these sub-sections have individual security access controls configured by the user.

9.4 DMA Firewall

The DMA firewall is a concatenation of two back-to-back firewalls. The first stage is explained below and the second stage is same as master TrustZone in the system and controlled by the user.

- DMA performing secure transaction for secure mailbox task:
  - All addresses are accessible
- DMA performing non-secure transaction for non-secure mailbox task:
  - Non-secure accesses are allowed
  - Secure accesses are blocked

Blocked transactions will internally cause DMA transaction error. This firewall can be enabled/disabled via CTL.DMAFWDIS.

9.5 HSM Key Storage

The HSM supports 2 types of assets: static and dynamic assets.

Static Assets

Key material that is available immediately after power-on and instantiated on HSM OTP memory. The static assets are intialized to OTP memory by device secure boot on power up. The OTP size is 1kB.

The following assets are initialized by secure boot:

- COID - Crypto Officer ID - 32bit - Madatory for FIPS140-3, required for certain operations - login, dynamic asset reset
- HUK - Hardware unique device key - 256bit - Device Root Key that can be used to derive other keys TKDK and TKEK
- TRNG/CRNG setup configurations

Dynamic Assets

Key material of any other sensitive assets that can be initialized by application in one of the following methods:

- Derive from another asset
- Load plaintext
- Import of assets key blob (wrapped using KEK) - allow keeping wrapped key outside the device (external flash)
- Import symmetric wrapped key blob - based AES/SM4
- Generate build in random data (using TRNG) - for symmetric and a-symmetric keys

The dynamic assets are instantiated on HSM data RAM - The HSM data RAM size is 16kB, 4.5 kB are used for HSM FW data and the rest is available for HSM assets.

9.6 HSM Registers

Table 9-1 lists the memory-mapped registers for the HSM registers. All register offset addresses not listed in Table 9-1 should be considered as reserved locations and the register contents should not be modified.

Table 9-1. HSM Registers

Offset	Acronym	Register Name	Section
3E00h	AICPOLCTL	Polarity Control Register	Section 9.6.1
3E04h	AICTYPCTL	AIC Type Control	Section 9.6.2
3E08h	AICENCTL	Audio Interface Control	Section 9.6.3
3E0Ch	AICRAWCTL	Interrupt Raw Status	Section 9.6.4
3E10h	AICENSTA	Accelerator Status	Section 9.6.5
3E14h	AICENCLR	Interrupt Enable Clear	Section 9.6.6
3E18h	AICOPTS	Audio Configuration Options	Section 9.6.7
3E1Ch	AICVER	Version Identifier	Section 9.6.8
3F00h	MBXSTA	Mailbox Status	Section 9.6.9
3F04h	MBXRAWSTA	Mailbox Raw Status	Section 9.6.10
3F08h	MBXLINKID	Controller Link Status	Section 9.6.11
3F0Ch	MBXOUTID	Output Controller Identifiers	Section 9.6.12
3F10h	MBXLCKOUT	Mailbox Lockout Control	Section 9.6.13
3FE0h	MODULESTA	Module Status	Section 9.6.14
3FF4h	EIPOPTS2	Module Configuration Options	Section 9.6.15
3FF8h	EIPOPTS1	Hardware Configuration Options	Section 9.6.16
3FFCh	EIPVER	EIP Version	Section 9.6.17

Complex bit access types are encoded to fit into small table cells. Table 9-2 shows the codes that are used for access types in this section.

Table 9-2. HSM Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

9.6.1 AICPOLCTL Register (Offset = 3E00h) [Reset = 00000000h]

AICPOLCTL is shown in Table 9-3.

Return to the Summary Table.

AIC Polarity Control Register

Table 9-3. AICPOLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
4	CTL4	R/W	0h	Individual polarity (high level/rising edge or low level/falling edge) control bits per interrupt input: 0b = Low level/falling edge 1b = High level/rising edge.
3	CTL3	R/W	0h	Individual polarity (high level/rising edge or low level/falling edge) control bits per interrupt input: 0b = Low level/falling edge 1b = High level/rising edge.
2	CTL2	R/W	0h	Individual polarity (high level/rising edge or low level/falling edge) control bits per interrupt input: 0b = Low level/falling edge 1b = High level/rising edge.
1	CTL1	R/W	0h	Individual polarity (high level/rising edge or low level/falling edge) control bits per interrupt input: 0b = Low level/falling edge 1b = High level/rising edge.
0	CTL0	R/W	0h	Individual polarity (high level/rising edge or low level/falling edge) control bits per interrupt input: 0b = Low level/falling edge 1b = High level/rising edge.

9.6.2 AICTYPCTL Register (Offset = 3E04h) [Reset = 00000000h]

AICTYPCTL is shown in Table 9-4.

Return to the Summary Table.

AIC Type Control Register

Table 9-4. AICTYPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
4	CTL4	R/W	0h	Signal type (level or edge) control bits for each interrupt input: 0b = level (the interrupt source level determines the raw status). 1b = edge (the interrupt source is connected to an edge detector and the edge detector output determines the raw status).
3	CTL3	R/W	0h	Signal type (level or edge) control bits for each interrupt input: 0b = level (the interrupt source level determines the raw status). 1b = edge (the interrupt source is connected to an edge detector and the edge detector output determines the raw status).
2	CTL2	R/W	0h	Signal type (level or edge) control bits for each interrupt input: 0b = level (the interrupt source level determines the raw status). 1b = edge (the interrupt source is connected to an edge detector and the edge detector output determines the raw status).
1	CTL1	R/W	0h	Signal type (level or edge) control bits for each interrupt input: 0b = level (the interrupt source level determines the raw status). 1b = edge (the interrupt source is connected to an edge detector and the edge detector output determines the raw status).
0	CTL0	R/W	0h	Signal type (level or edge) control bits for each interrupt input: 0b = level (the interrupt source level determines the raw status). 1b = edge (the interrupt source is connected to an edge detector and the edge detector output determines the raw status).

9.6.3 AICENCTL Register (Offset = 3E08h) [Reset = 00000000h]

AICENCTL is shown in Table 9-5.

Return to the Summary Table.

AIC Enable Control Register

Table 9-5. AICENCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
4-0	CTL	R/W	0h	Individual enable control bits per interrupt input: 0b = Disabled. 1b = Enabled

9.6.4 AICRAWCTL Register (Offset = 3E0Ch) [Reset = 0000000Fh]

AICRAWCTL is shown in Table 9-6.

Return to the Summary Table.

AIC Raw Source Status Register

Table 9-6. AICRAWCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
4	STA4	RH	0h	Individual interrupt status bit before masking with enable_ctrl_r[4] (programmable, reset to 'low level' mode): 0b = Inactive, 1b = Pending.
3	STA3	RH	1h	Individual interrupt status bit before masking with enable_ctrl_r[3] (programmable, reset to 'low level' mode): 0b = Inactive, 1b = Pending.
2	STA2	RH	1h	Individual interrupt status bit before masking with enable_ctrl_r[2] (programmable, reset to 'low level' mode): 0b = Inactive, 1b = Pending.
1	STA1	RH	1h	Individual interrupt status bit before masking with enable_ctrl_r[1] (programmable, reset to 'low level' mode): 0b = Inactive, 1b = Pending.
0	STA0	RH	1h	Individual interrupt status bit before masking with enable_ctrl_r[0] (programmable, reset to 'low level' mode): 0b = Inactive, 1b = Pending.

9.6.5 AICENSTA Register (Offset = 3E10h) [Reset = 00000000h]

AICENSTA is shown in Table 9-7.

Return to the Summary Table.

AIC Enabled Status Register

Table 9-7. AICENSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
4-0	STA	RH	0h	These bits reflect the status of the interrupts after polarity control and optional edge detection, gated with bits in AIC_ENABLE_CTRL register: 0b = Inactive. 1b = Pending.

9.6.6 AICENCLR Register (Offset = 3E14h) [Reset = X0000000h]

AICENCLR is shown in Table 9-8.

Return to the Summary Table.

AIC Enable Clear Register

Table 9-8. AICENCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	W	0h	Reserved field. Write with zero
4-0	CLR	W	Xh	Individual interrupt disable bits per interrupt input: 0b = No effect. 1b = Clear the corresponding bit in the AIC_ENABLE_CTRL register, disabling the interrupt. After writing a 1b, there is no need to write a 0b.

9.6.7 AICOPTS Register (Offset = 3E18h) [Reset = 000000X5h]

AICOPTS is shown in Table 9-9.

Return to the Summary Table.

AIC Options Register

Table 9-9. AICOPTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
8	MINIMAP	R	0h	Mini register map.
7	EXTMAP	R	0h	Extended register map.
6	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
5-0	NUMOFIN	R	5h	The number of interrupt request inputs.

9.6.8 AICVER Register (Offset = 3E1Ch) [Reset = 014036C9h]

AICVER is shown in Table 9-10.

Return to the Summary Table.

AIC Version Register

Table 9-10. AICVER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
27-24	MAJORVER	R	1h	These bits encode the major version number for the EIP-201 module.
23-20	MINORVER	R	4h	These bits encode the minor version number for the EIP-201 module.
19-16	PATCHLVL	R	0h	These bits encode the hardware patch level for the EIP-201 module, starting at value 0 on the first release.
15-8	EIPNUMCOMP	R	36h	These bits simply contain the complement of bits [7:0], used by a driver to ascertain that this version register is indeed read.
7-0	EIPNUM	R	C9h	These bits encode the Rambus EIP number.

9.6.9 MBXSTA Register (Offset = 3F00h) [Reset = 00000088h]

MBXSTA is shown in Table 9-11.

Return to the Summary Table.

Mailbox Status Register

Table 9-11. MBXSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
7	AVAIL2	R	1h	(set)-Input Mailbox is linked to a Host or is filled, (Clear)- Input Mailbox is available for linking by this Host
6	LINKED2	R	0h	(set)-This Host is linked to Mailbox, (Clear)-This Host is not linked to Mailbox
5	OUTFULL2	R	0h	(set)-Output Mailbox contains an output token, (Clear)-Output Mailbox is empty
4	INFULL2	R	0h	(set)-Input Mailbox contains a token that is handed over to Internal Controller, (Clear)-Input Mailbox is ready to rceive new token
3	AVAIL1	R	1h	(set)-Input Mailbox is linked to a Host or is filled, (Clear)- Input Mailbox is available for linking by this Host
2	LINKED1	R	0h	(set)-This Host is linked to Mailbox, (Clear)-This Host is not linked to Mailbox
1	OUTFULL1	R	0h	(set)-Output Mailbox contains an output token, (Clear)-Output Mailbox is empty
0	INFULL1	R	0h	(set)-Input Mailbox contains a token that is handed over to Internal Controller, (Clear)-Input Mailbox is ready to rceive new token

9.6.10 MBXRAWSTA Register (Offset = 3F04h) [Reset = 0000000Xh]

MBXRAWSTA is shown in Table 9-12.

Return to the Summary Table.

Raw (unmasked) Mailbox Status Register

Table 9-12. MBXRAWSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
6	LINKED2	R	0h	(set)-This Host is linked to Mailbox mbx%d , (Clear)-This Host is not linked to Mailbox mbx%d
5	OUTFULL2	R	0h	(set)-Output Mailbox contains an output token, (Clear)-Output Mailbox mbx%d is empty
4	INFULL2	R	0h	(set)-Input Mailbox contains a token that is handed over to Internal Controller, (Clear)-Input Mailbox mbx%d is ready to rceive new token
3	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
2	LINKED1	R	0h	(set)-This Host is linked to Mailbox mbx%d , (Clear)-This Host is not linked to Mailbox mbx%d
1	OUTFULL1	R	0h	(set)-Output Mailbox contains an output token, (Clear)-Output Mailbox mbx%d is empty
0	INFULL1	R	0h	(set)-Input Mailbox contains a token that is handed over to Internal Controller, (Clear)-Input Mailbox mbx%d is ready to rceive new token

9.6.11 MBXLINKID Register (Offset = 3F08h) [Reset = 00000000h]

MBXLINKID is shown in Table 9-13.

Return to the Summary Table.

Mailbox Status - linked Host IDs Register

Table 9-13. MBXLINKID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
7	PORTACC2	R	0h	0: Mailbox 2 can be accessed by the Host using protected or non-protected access. 1: Mailbox 2 is only accessible if the Host uses protected access.
6-4	LINKID2	R	0h	Bits[1:0]Host cpu_id of the Host linked to the Mailbox, bit[2] Set - Mailbox is only accessible if Host uses protected access, Clear - Mailbox accessed with protected of non-protected access
3	PROTACC1	R	0h	0: Mailbox 1 can be accessed by the Host using protected or non-protected access. 1: Mailbox 1 is only accessible if the Host uses protected access.
2-0	LINKID1	R	0h	Bits[1:0]Host cpu_id of the Host linked to the Mailbox, bit[2] Set - Mailbox is only accessible if Host uses protected access, Clear - Mailbox accessed with protected of non-protected access

9.6.12 MBXOUTID Register (Offset = 3F0Ch) [Reset = 00000000h]

MBXOUTID is shown in Table 9-14.

Return to the Summary Table.

Mailbox Status - output Host IDs Register

Table 9-14. MBXOUTID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
7	PORTACC2	R	0h	0: Output mailbox 2 can be accessed by the Host using protected or non-protected access. 1: Output mailbox 2 is only accessible if the Host uses protected access.
6-4	OUTID2	R	0h	Bit[1,0] Host cpu_id of the Host allowed to read a result from the Mailbox, bit[2] Set - Out Mailbox is only accessible if Host uses protected access, Clear - Output Mailbox accessed with protected of non-protected access
3	PROTACC1	R	0h	0: Output mailbox 1 can be accessed by the Host using protected or non-protected access. 1: Output mailbox 1 is only accessible if the Host uses protected access.
2-0	OUTID1	R	0h	Bit[1,0] Host cpu_id of the Host allowed to read a result from the Mailbox, bit[2] Set - Out Mailbox is only accessible if Host uses protected access, Clear - Output Mailbox accessed with protected of non-protected access

9.6.13 MBXLCKOUT Register (Offset = 3F10h) [Reset = 00000E0Eh]

MBXLCKOUT is shown in Table 9-15.

Return to the Summary Table.

Host/Mailbox1-4 lockout control Register

Table 9-15. MBXLCKOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
15-8	LOCKOUT2	R/W	Eh	Bit map indicates which Hosts are blocked from accessing mailbox
7-0	LOCKOUT1	R/W	Eh	Bit map indicates which Hosts are blocked from accessing mailbox

9.6.14 MODULESTA Register (Offset = 3FE0h) [Reset = XXXXXXXXh]

MODULESTA is shown in Table 9-16.

Return to the Summary Table.

Module Status Register

Table 9-16. MODULESTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FATALERR	R	0h	Read-Only. Set if fatal error occured
30-11	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
10	CRCERR	R	0h	Read-Only. Set if CRC on ProgramROM is fails
9	CRCOK	RH	Xh	Read-Only. Set if CRC on ProgramROM is passes
8	CRCBUSY	RH	Xh	Read-Only. Set if CRC on ProgramROM is busy
7-2	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
1	NFIPSMOD	R	0h	Read-Only. Set if VaultIP is in non-FIPS mode
0	FIPSMOD	R	0h	Read-Only. Set if VaultIP is in FIPS mode

9.6.15 EIPOPTS2 Register (Offset = 3FF4h) [Reset = 0020XXXXh]

EIPOPTS2 is shown in Table 9-17.

Return to the Summary Table.

VaultIP configured options(2)

Table 9-17. EIPOPTS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
25	ADDCE10	R	0h	Set - an additional crypto engine is available in hardware as custom engine10
24	ADDCE9	R	0h	Set - an additional crypto engine is available in hardware as custom engine9
23	ADDCE8	R	0h	Set - an additional crypto engine is available in hardware as custom engine8
22	ADDCE7	R	0h	Set - an additional crypto engine is available in hardware as custom engine7
21	ADDCE6	R	1h	Set - an additional crypto engine is available in hardware as custom engine6
20	ADDCE5	R	0h	Set - an additional crypto engine is available in hardware as custom engine5
19	ADDCE4	R	0h	Set - an additional crypto engine is available in hardware as custom engine4
18	ADDCE3	R	0h	Set - an additional crypto engine is available in hardware as custom engine3
17	ADDCE2	R	0h	Set - an additional crypto engine is available in hardware as custom engine2
16	ADDCE1	R	0h	Set - an additional crypto engine is available in hardware as custom engine1
15-13	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
12	BUSIF	R	0h	Bus interface type, for both Master and Slave: 0b = 32-bit AHB, 1b = 32-bit AXI
11-10	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
9	PRAM	R	0h	1b = downloadable RAM based firmware program memory. 0b = ROM only firmware program memory.
8	CCPU	R	0h	C capable local cpu available
7-6	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
5	PKCP	R	1h	PKCP Engine available
4	CRC	R	1h	CRC calculation available
3	TRNG	R	1h	Set - TRNG engine available
2	SHA	R	1h	Set - SHA1/SHA2 combination core available
1	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
0	DESAES	R	0h	Set - (3)DES/AES combination crypto core available

9.6.16 EIPOPTS1 Register (Offset = 3FF8h) [Reset = 018X0FX2h]

EIPOPTS1 is shown in Table 9-18.

Return to the Summary Table.

VaultIP configured options(1)

Table 9-18. EIPOPTS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	HOSTIDSEC	R	1h	Bits to indicate which of the 8 possible cpu_id codes on the bus interface are active Hosts with secure access
23	MYIDSEC	R	1h	Indicates the current protection bit values of the Host actually reading the register
22-20	MYID	R	0h	Slave & Master interface support protection bit (secure/non-secure) accesses
19	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
18-16	MASID	R	0h	Value of the cpu_id that designates the Master Host
15-8	HOSTID	R	Fh	Bits to indicate which of the 8 possible cpu_id codes on the bus interface are active
7-6	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
5-4	MBXSIZE	R	1h	Implemented size of Mailbox pairs - 00b-128bytes, 01b-256bytes, 10b-512bytes, 11b-1Kbyte
3-0	NUMOFMBX	R	2h	Number of Input/Output Mailbox pairs

9.6.17 EIPVER Register (Offset = 3FFCh) [Reset = 04007D82h]

EIPVER is shown in Table 9-19.

Return to the Summary Table.

Standard EIP version register

Table 9-19. EIPVER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved field. Write with zero and ignore on read
27-24	MAJORVER	R	4h	Major Version release number for this module
23-20	MINORVER	R	0h	Minor Version release number for this module
19-16	PATCHLVL	R	0h	Hardware Patch Level for this module
15-8	EIPNUMCOMP	R	7Dh	Bit by Bit compliment of EIP Number
7-0	EIPNUM	R	82h	RAMBUS EIP number - EIP130

9.7 HSM_NON_SEC Registers

Table 9-20 lists the memory-mapped registers for the HSM_NON_SEC registers. All register offset addresses not listed in Table 9-20 should be considered as reserved locations and the register contents should not be modified.

Table 9-20. HSM_NON_SEC Registers

Offset	Acronym	Register Name	Section
0h	CLK_MEM_CTRL	Memory Clock Control	Section 9.7.1
4h	PKA_ABORT_CTRL	This register is used for aborting PKA operation.	Section 9.7.2
8h	HSM_STA_REG	Hardware Security Status	Section 9.7.3
Ch	RAM_CLR_STA	Memory Clear Status	Section 9.7.4

Complex bit access types are encoded to fit into small table cells. Table 9-21 shows the codes that are used for access types in this section.

Table 9-21. HSM_NON_SEC Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

9.7.1 CLK_MEM_CTRL Register (Offset = 0h) [Reset = 00000000h]

CLK_MEM_CTRL is shown in Table 9-22.

Return to the Summary Table.

This register is used for enabling clock to the module

Table 9-22. CLK_MEM_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CTR_CLK_BUSY	R	0h	When 1b, indicates that the counter clock domain is active. This signal is always asserted (set to '1'), except when the counter module is in reset (ctr_reset_n set to '0').
7	SLV_CLK_BUSY	R	0h	When 1b indicates the Host interface is active and busy with Host bus transfers.
6	CLK_BUSY	R	0h	when 1b, indicates that the module is active and busy with processing data and tokens.
5	MEM_CTR_CLK_GO_M3	R/W	0h	Write this bit to enable counter clock 0h = Write 0b to disable clock 1h = Write 1b to enable clock
4	MEM_SLV_CLK_GO_M3	R/W	0h	Write this bit to enable host interface clock 0h = Write 0b to disable clock 1h = Write 1b to enable clock
3	MEM_CLK_GO_M3	R/W	0h	M3 writes this bit to enable clock to the module 0h = Write 0b to disable clock 1h = Write 1b to enable clock
2	MEM_CTR_CLK_GO	R/W	0h	Write this bit to enable counter clock 0h = Write 0b to disable clock 1h = Write 1b to enable clock
1	MEM_SLV_CLK_GO	R/W	0h	Write this bit to enable host interface clock 0h = Write 0b to disable clock 1h = Write 1b to enable clock
0	MEM_CLK_GO	R/W	0h	Write this bit to enable clock to the module 0h = Write 0b to disable clock 1h = Write 1b to enable clock

9.7.2 PKA_ABORT_CTRL Register (Offset = 4h) [Reset = 00000000h]

PKA_ABORT_CTRL is shown in Table 9-23.

Return to the Summary Table.

This register is used for aborting PKA operation.

Table 9-23. PKA_ABORT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	MEM_PKA_ABORT_NS	R/W	0h	Write 1 to this bit to abort PKA operation 1h = Set to 1, to abort PKA operation

9.7.3 HSM_STA_REG Register (Offset = 8h) [Reset = 00000000h]

HSM_STA_REG is shown in Table 9-24.

Return to the Summary Table.

This register provides EIP130 status
This register must be accessed using a minimum write width of 32.

Table 9-24. HSM_STA_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	POWER_MODE	R	0h	Power mode value 1'b1 indicates hsm is in sleep and value 1'b0 indicates hsm is out of sleep.
2	FATAL_ERROR	R	0h	If active (set to 1b), EIP130 detected a fatal error and stops operation. fatal error can happen when CRC on firmware ROM fails or selftest fails.
1	NON_FIPS_MODE	R	0h	If active (set to 1b), EIP130 is in NON-FIPS mode
0	FIPS_MODE	R	0h	If active (set to 1b), EIP130 is in FIPS mode

9.7.4 RAM_CLR_STA Register (Offset = Ch) [Reset = 00000000h]

RAM_CLR_STA is shown in Table 9-25.

Return to the Summary Table.

This register stores status of asset clear indication.
This register must be accessed using a minimum write width of 32.

Table 9-25. RAM_CLR_STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	DATARAM_CLR_DONE	R	0h	If active (set to 1b), it indicates that auto clear of Dataram on reset release has been completed.
0	OTP_CLR_DONE	R	0h	If active (set to 1b), it indicates that auto clear of OTP on reset release has been completed.

9.8 HSM_SEC Registers

Table 9-26 lists the memory-mapped registers for the HSM_SEC registers. All register offset addresses not listed in Table 9-26 should be considered as reserved locations and the register contents should not be modified.

Table 9-26. HSM_SEC Registers

Offset	Acronym	Register Name	Section
0h	CLKCTL	Secure Clock Control	Section 9.8.1
4h	SRSTCTL	Reset Control	Section 9.8.2
8h	PKACTL	Cancel Operation Control	Section 9.8.3
18h	SLPCTL	Sleep Control	Section 9.8.4

Complex bit access types are encoded to fit into small table cells. Table 9-27 shows the codes that are used for access types in this section.

Table 9-27. HSM_SEC Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

9.8.1 CLKCTL Register (Offset = 0h) [Reset = 00000000h]

CLKCTL is shown in Table 9-28.

Return to the Summary Table.

Clock Control Secured Register. This register is used for enabling clock to the module.

Table 9-28. CLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	CTLCLKBUSY	R	0h	When 1b, indicates that the counter clock domain is active. This signal is always asserted (set to '1'), except when the counter module is in reset (ctr_reset_n set to '0').
5	HIFCLKBUSY	R	0h	When 1b indicates the Host interface is active and busy with Host bus transfers.
4	CLKBUSY	R	0h	when 1b, indicates that the module is active and busy with processing data and tokens.
3	CLKDISREQ	R/W	0h	This bit is set to disable all clock sources. 1h = Write 1 to disable clock
2	CNTCLKGO	R/W	0h	Write this bit to enable counter clock 0h = Write 0 to disable clock 1h = Write 1 to enable clock
1	HIFCLKGO	R/W	0h	Write this bit to enable host interface clock 0h = Write 0 to disable clock 1h = Write 1 to enable clock
0	CLKGO	R/W	0h	Write this bit to enable clock to the module 0h = Write 0 to disable clock 1h = Write 1 to enable clock

9.8.2 SRSTCTL Register (Offset = 4h) [Reset = 00000000h]

SRSTCTL is shown in Table 9-29.

Return to the Summary Table.

Soft Reset Control. This register is used for controlling soft reset mechanism.

Table 9-29. SRSTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6-4	STATE	R	0h	It indicates state of soft reset assertion. 0h = soft reset is not requested 1h = Soft reset is requested 2h = Soft reset is acknowledged. 3h = Soft reset can be asserted 4h = soft reset is set
3	STA	R	0h	When 1b, soft reset is asserted to the module
2	FRCACK	W	0h	Write 1b, to forcely assert soft reset without waiting for abort acknowledge from EIP. 1h = To force soft reset
1	ABORTACK	R	0h	when 1b, indicates abort request is acknowledged by EIP and soft reset is asserted
0	ABORTREQ	W	0h	Write this bit to request soft reset. It is a write-clear or auto clear register. 1h = To enable Abort request

9.8.3 PKACTL Register (Offset = 8h) [Reset = 00000000h]

PKACTL is shown in Table 9-30.

Return to the Summary Table.

PKA Abort Control Secured Register. This register is used for aborting PKA operation.

Table 9-30. PKACTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	NSMASKREQ	R/W	0h	This bit is used to mask PKA abort request generated by non-secure controller. 1h = Mask request
0	ABORT	R/W	0h	Write 1 to Abort. 1h = Write 1 to this bit to abort PKA operation

9.8.4 SLPCTL Register (Offset = 18h) [Reset = 00000000h]

SLPCTL is shown in Table 9-31.

Return to the Summary Table.

Sleep Control.

Table 9-31. SLPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reads to this field return zero, writes to this field are ignored.
1	SRCVAL	R/W	0h	power_mode_in source select MMR 0-power_mode_in comes from logic 1-power_mode_in comes from mem_slp_ovr_val
0	OVRVAL	R/W	0h	power_mode_in override value by FW. FW can set to 1 after cold boot

Chapter 10

Device Boot and Bootloader

This chapter describes the CC35xx Boot concept and two stage bootloader.

10.1 CC35xx Boot Concept

CC35xx boot is designed to support processes and flows throughout the entire supply chain and life cycle – starting at TI FAB as the Silicon manufacturer, followed by shipping to the vendor OEM/ODM where the IC purchased by TI is assembled on a board and where the vendor application is developed by the vendors' R&D and terminating at the end-equipment deployment where the end-users are using the end-product with the vendor's board integrated as part of the connected device solution as shown in the following figure.

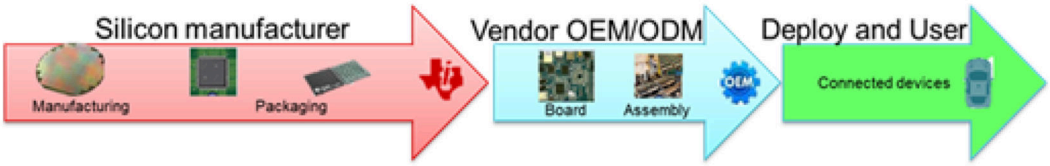

Figure 10-1. CC35xx Boot Concept

The underlying concept of the CC35xx device boot is to provide vendors with a secured, flexible and simple bootloader scheme executed on a coprocessor (M3) and isolated from the end-equipment application code execution environment.

This ensures that the first interaction of the system with the vendor's code entry point on the main processor (M33) is after its code has been authenticated and its system level secured configurations and initial system state working point were safely set by TI's bootloader on its behalf.

TI bootloader ensures secured vendor configurations by enforcing them only after they are authenticated (i.e. cryptographically signed by the vendor) either permanently at production line or as part of the vendor deployment images.

This method was devised to provide a secured yet simple and controllable IP protection capabilities and initial system state configurations by the customer.

10.2 Features

- TI's 1st stage boot (BL1) – immutable ROM by TI:
  - Authentication of BL2 using TI credentials
  - Authentication of connectivity radio testing tool
- TI's 2nd stage boot (BL2) – updatable TI bootloader:
  - Secured vendor code execution environment (for deployed end-devices or at vendor's R&D where the vendor application is being deployed):
    - Authenticates Vendor's image (signed MCUboot images using ECC)
    - Enforcement of initial system working point through authenticated vendor configurations (part of the signed MCUboot image)
  - Provide device level secured management utilities:
    - Device activation a one-time process in which the vendor changes the device ownership from TI to the vendor. Until activation is done, the device is locked for programming.
    - Device initial programming required for 1st time programming of the device fuses and flash (for production line).
    - Device re-programming for updating images on devices that already underwent initial programming (for vendor applications development purpose)
    - Device debug control to enable/disable debug capabilities

10.3 Vendor Images Format and Processing

10.3.1 External Flash Arrangement

The external flash is arranged as follows:

- Boot sector – beginning of flash in a fixed location which contains the information required for setting up the specific external flash configurations used by the vendor and points to the other images.

- TI Bootloader (BL2) image – BL2 that the ROM loads in normal execution.
- Wireless Connectivity Image – connectivity image containing FW that the vendor's main core needs to push to the connectivity core when it requires availability of the wireless interfaces (BLE and WiFi).
- Vendor Image – containing the vendor application and initial system state configurations.

10.3.2 Vendor Images Format

Format and processing of vendor images comply with standard MCUBoot formats and methods of operation (see MCUboot)).

10.4 Boot Flows

10.4.1 Application Execution Boot Flow

The purpose of the application execution boot flow is to run only trusted vendor application code on the device main processor (with or without M33 debug capability). The CC35xx device executes the boot sequence for vendor trusted application execution in multiple stages through a Chain of Trust.

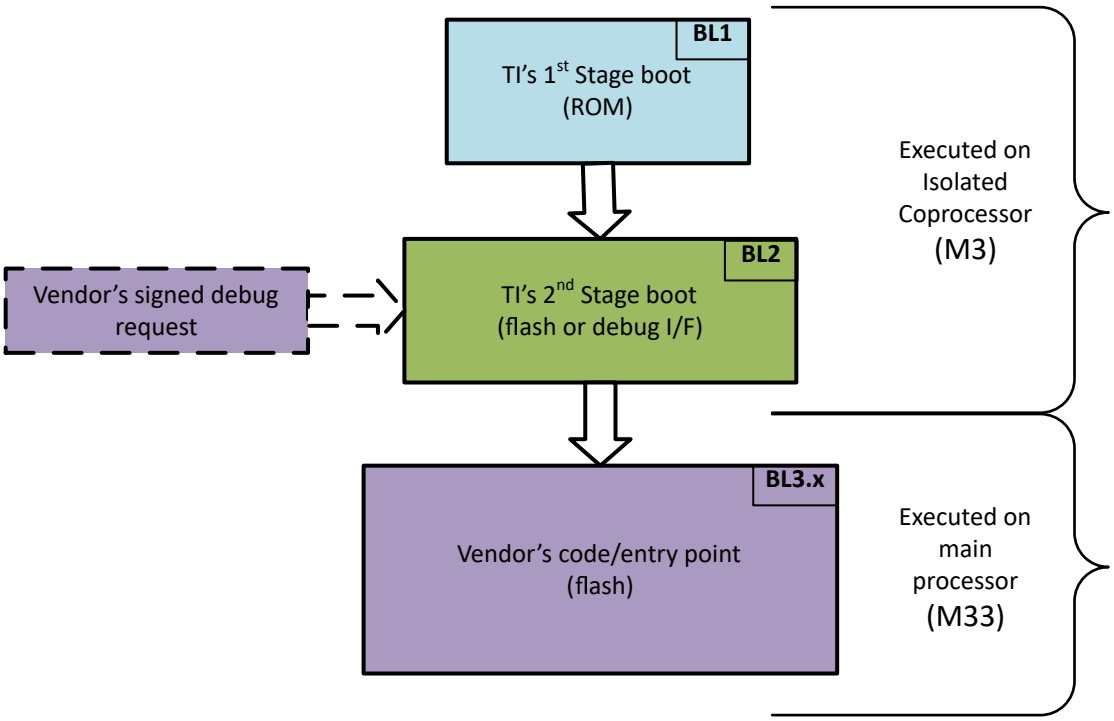

Figure 10-2. Application Execution Boot Flow

A detailed description of the flow is as follows:

- This is the default flow that runs upon any power on reset.
- BL1 loads, authenticates and invokes BL2 into the co-processor either from the flash or if requested over the debug I/F for supporting more advanced debug capabilities.
- BL2 performs the following actions:
  - Authenticates the vendor's code, namely BL3.x which runs from flash (XIP mode).
  - Enforces the initial system state configurations based on the vendor's settings and configurations delivered as part of its image.
  - If an signed debug request was issued through the debug interface – BL2 authenticates it and enforces requested debug settings.
- BL3.x is the trusted vendor's code entry point based on the vendor credentials. Vendor code can be for example:
  - Custom bare metal M33 based application (non-TFM based).

- SPE-TFM/NSPE partitioning
- Additional vendor bootloader (a future extension that TI bootloader will provide)

Note

An uploaded application version needs to pass both authentication and version rollback checks.

10.4.2 Activation Flow

The purpose of the activation flow is to perform a one-time action per device by the vendor to switch the device ownership from TI to the vendor to secure its IP. This means that from this point on, any vendor IP stored on the device cannot be accessed by anyone without vendor privileges and credentials.

The CC35xx device executes the boot sequence for device activation in two stages through a Chain of Trust that terminates at TI level.

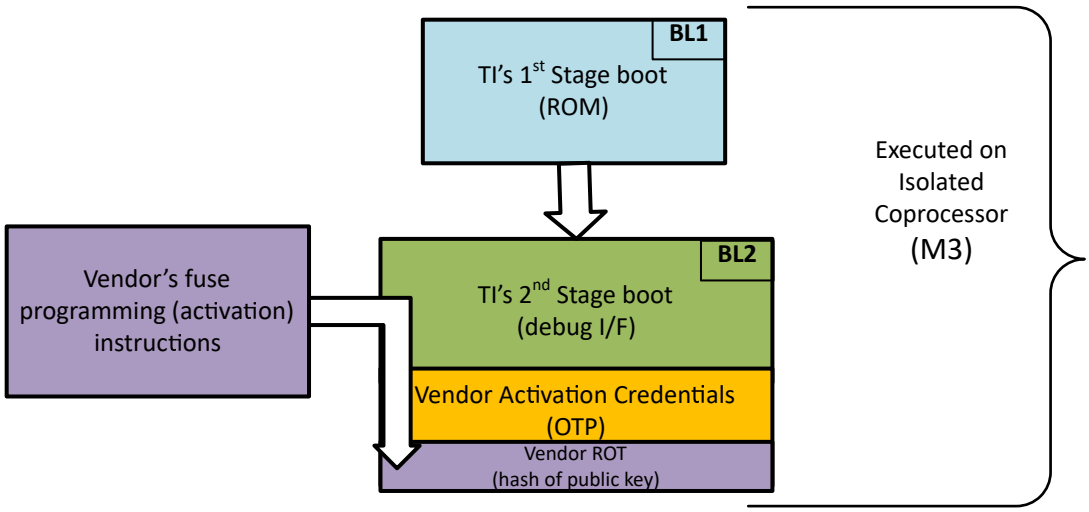

Figure 10-3. Activation Flow

A detailed description of the flow is as follows:

- Flow execution upon special reset triggered through the debug I/F.
- BL1, authenticates and invokes BL2 into the co-processor from the debug I/F.
- BL2 performs the following actions:
  - Identifies that the device is not yet activated.
  - Authenticates the vendor's programming instructions and verifies its format.
  - Performs the vendor credentials installation on the OTP by programming the vendor ROT fuses as indicated in the fuse instructions.
- BL2 issues a report to indicate success or failure of the process

If successful, from this point on – the device is associated with the vendor who owns the private key whose hash of public key is installed on the device.

This ROT installation and identification method is a common industry good security practice and part of the MCUboot infrastructure.

10.4.3 Initial Programming Flow

The purpose of the initial programming flow is to setup a blank device in order to be able to run a trusted vendor application upon reset.

- May be done as needed at the vendor R&D to "reformat" the flash or add capabilities by programming additional fuse based capabilities (e.g. authentication bypass disable/authentication enable - which is highly recommended for deployed devices).
- Suitable for production lines to pre-program deployed devices.

The CC35xx device executes the boot sequence for initial programming in multiple stages through the full Chain of Trust.

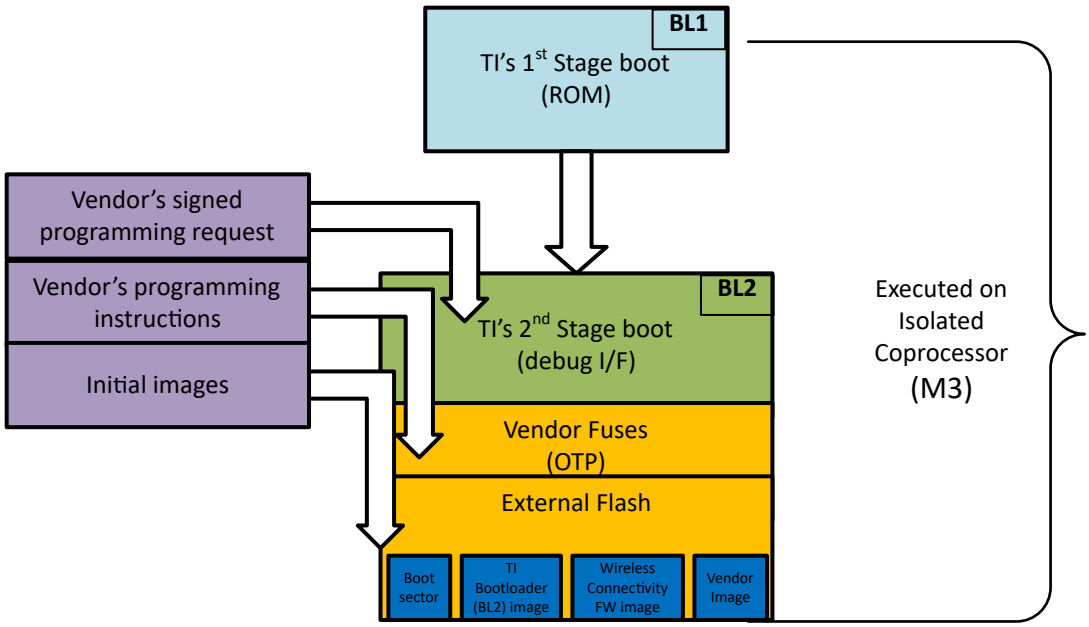

Figure 10-4. Initial Programming Flow

A detailed description of the flow is as follows:

- Flow execution upon special reset triggered through the debug I/F.
- BL1 loads, authenticates and invokes BL2 into the co-processor from the debug I/F.
- BL2 Identifies that the device was activated already
- BL2 Identifies the request as a signed programming request
- BL2 Authenticates the signed programming request (unique per device) using the public key whose hash matches the one installed during the one-time activation.
- Once authenticated, BL2 performs the programming instructions for programming fuses and configuring the external flash for programming of images based on the vendor programming instructions provided over the debug I/F.
- Then BL2 programs to the flash the images that the vendor issues over the debug I/F. For successful initial programming the flash must contain the following:
  - Boot sector
  - TI bootloader (BL2) image (signed by TI)
  - Wireless Connectivity FW image (signed by TI)
  - Vendor image (signed by the vendor)
- BL2 issues a report to indicate success or failure of the process

After successful initial programming, upon reset, the device executes the programmed vendor image in a trusted manner after running the Application Execution Boot Flow.

10.4.4 Reprogramming Flow

The purpose of the reprogramming flow is to update vendor images during development which is expected to be the most common operation the vendor will perform while developing its application.

The CC35xx device executes the boot sequence for reprogramming in multiple stages through the full Chain of Trust.

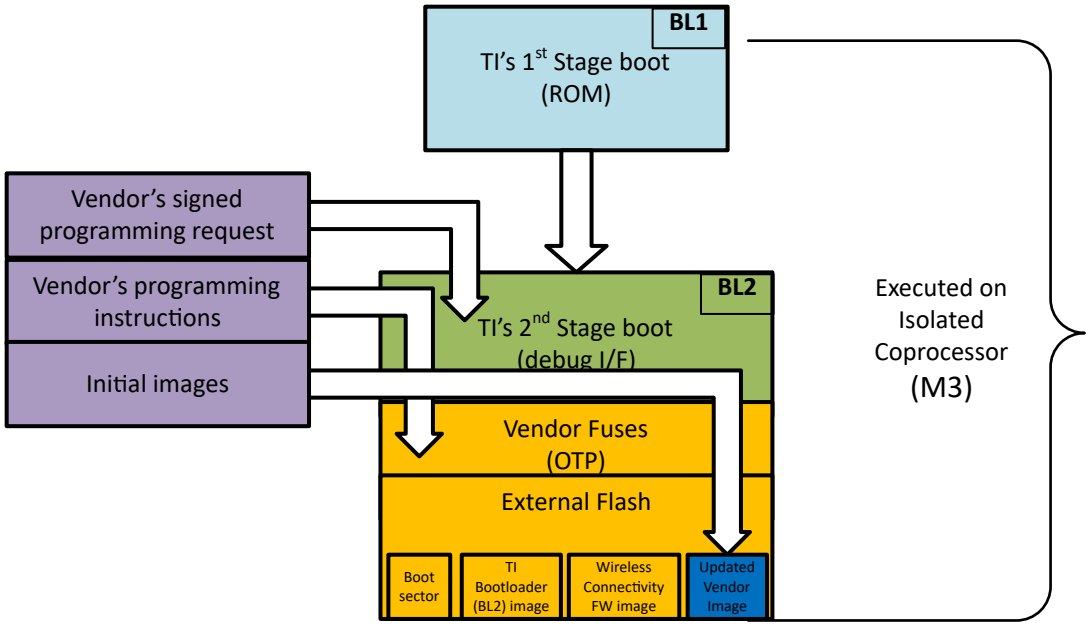

Figure 10-5. Reprogramming Flow

- Flow execution upon special reset triggered through the debug I/F.
- BL1 loads, authenticates and invokes BL2 into the co-processor from the debug I/F.
- BL2 identifies that the device was activated already
- BL2 Identifies the request as a signed programming request
- BL2 authenticates the signed programming request (unique per device) using the public key whose hash matches the one installed during the one-time activation.
- Once authenticated, BL2 performs the programming instructions for configuring the external flash for programming of the updated vendor image based on the vendor programming instructions provided over the debug I/F.
- Then BL2 programs to the flash the updated and newly signed vendor image the vendor issues over the debug I/F (to replace the already programmed vendor image).
- BL2 issues a report to indicate success or failure of the process

After successful reprogramming, the device will be able to successfully run the updated vendor image in a trusted manner.

10.4.5 Wireless Connectivity Testing Tool Flow

The purpose of the wireless connectivity testing tool flow is to test the connectivity performances of the device e.g. during development or production line.

The CC35xx device executes the boot sequence for wireless connectivity testing tool in multiple stages through the full Chain of Trust.

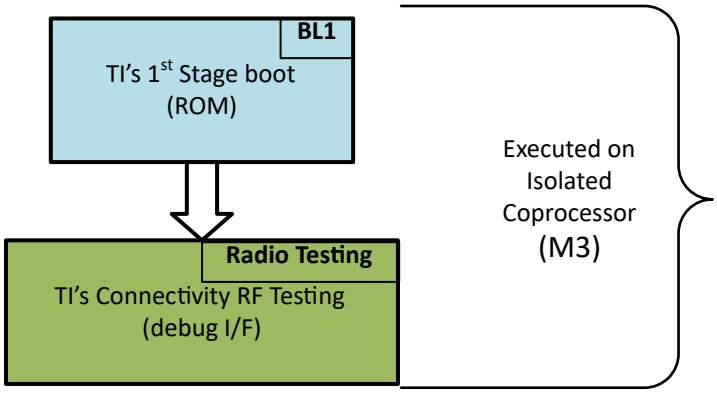

Figure 10-6. Wireless Connectivity Testing Tool Flow

- Flow execution upon special reset triggered through the debug I/F.
- BL1 loads, authenticates and invokes the wireless connectivity testing FW into the co-processor from the debug I/F.
- No BL2 or vendor main processor vendor images are involved.

10.5 Chain of Trust

The Chain of Trust of CC35xx to enable trusted bootloader vendor activities (setup the system for trusted application execution, vendor IP programming and system initial secured working point setup) is established as follows:

- TI's 1st stage boot (BL1) – immutable ROM by TI contains public keys to authenticate:
  - TI's 2nd stage Bootloader – signed by TI and authenticated by dedicated TI immutable public key o TI's Connectivity Radio Testing public key – signed by TI and authenticated by dedicated TI immutable public key
- TI's 2nd stage boot (BL2) – updatable boot validates vendor public keys against a production line installed ROT and uses them to authenticate:
  - Vendor image: BL2 matches OTP containing the hash of the vendor public key (as the vendor ROT installed during production line activation) with the hash of the public key provided with the vendor image on flash.
  - Unique per-device authenticated debug actions (optional): For secured debug purposes, the vendor needs to provide BL2 with a signed debug request (unique per device) through the Debug I/F. BL2 matches OTP containing the hash of the vendor public key installed during activation with the hash of the public key provided with an authenticated debug request provided by the vendor over the debug I/F. If this validation matches and signature authentication of the request passes successfully, TI bootloader will ensure the debug interface of the device will be open for the vendor. Alternatively, BL2 also supports a separate debug public key, such that BL2 matches OTP containing the hash of the vendor debug public key with the hash of the public key provided with an authenticated debug request provided by the vendor over a debug I/F.

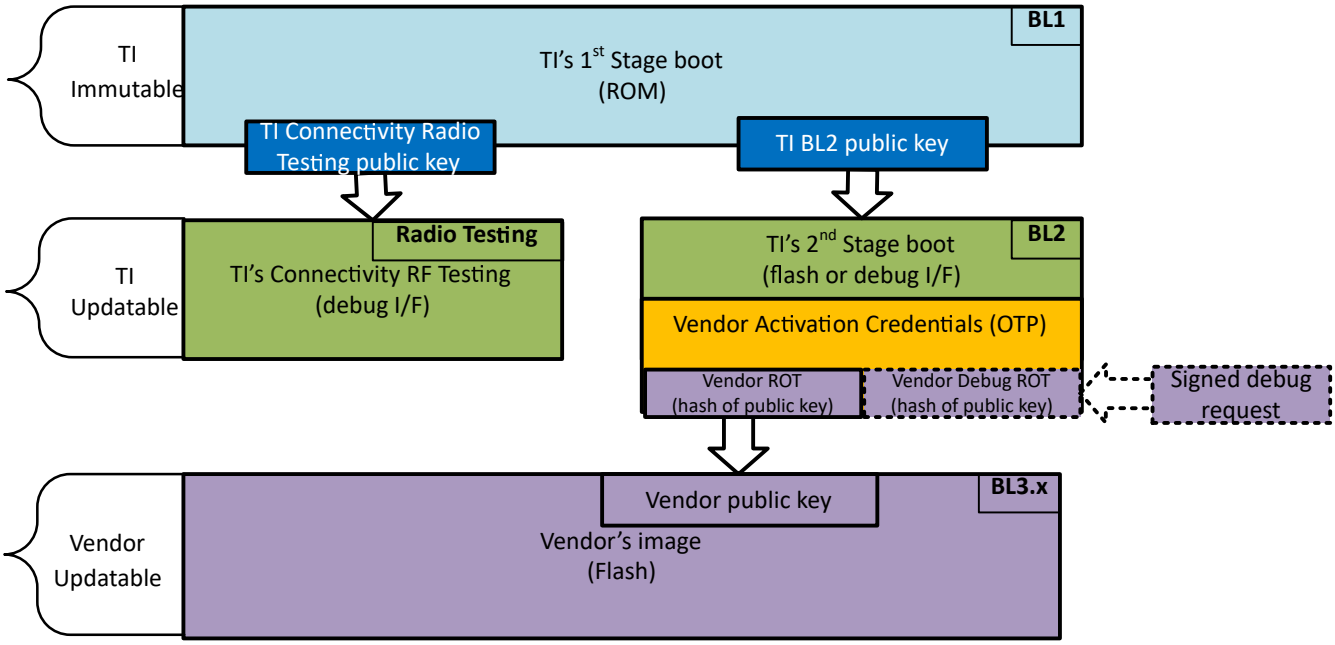

Figure 10-7. Chain of Trust

Note

For development purposes, signature authentication can be bypassed through special OTP programming. **It is not recommended to deploy such devices**.

Chapter 11

Direct Memory Access (DMA)

This chapter describes the direct memory access (DMA) controller, known as Host DMA.

11.1 Overview

The CC35xx device includes a direct memory access (DMA) controller, known as Host DMA. The Host DMA controller provides a way to offload data transfer tasks from the Arm® Cortex®-M33 processor, allowing for more efficient use of the processor and the available bus bandwidth. The Host DMA controller can perform transfers between memory and peripherals. The Host DMA includes multiple channels and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data.

The DMA controller transfers data from a source address to a destination address without CPU intervention. For example, the DMA controller can be used to move data from SPI peripheral to SRAM. Using the DMA controller can increase the throughput of peripheral modules.

DMA controller features include:

- 14 independent transfer channels
- Support for memory-to-memory, memory-to-peripheral, and peripheral-to-memory in multiple transfer modes (Support HW flow control with peripherals)
- Highly flexible and configurable channel operation:
  - Independently configured and operated channels
  - Flexible channel assignments
  - Each channel can be used for peripheral receive and/or transmit paths
  - Configurable DMA channel priorities
  - Payload transformation (byte swap,endianness)
- Job Size up to 16384Bytes
- Single or block transfer modes up to 64 words. Word size can be configured to 8,16, or 32 bits.
- FIFO mode (fixed address) or incremental address are supported
- Alignment - Every combination of start address, word size and job size is valid
- Up to two channels can be defined and high priority
- Interrupt on transfer completion with a separate interrupt per channel

11.2 Block Diagram

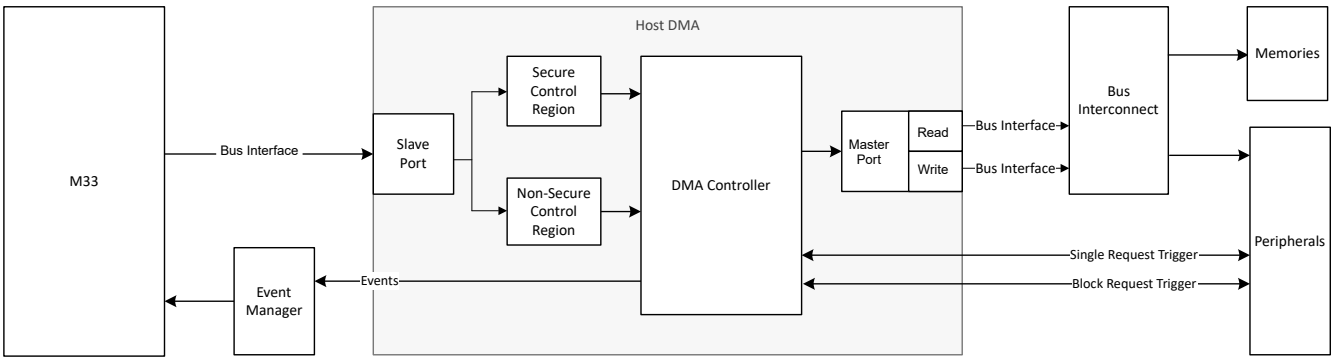

Figure 11-1. DMA Block Diagram

11.3 Functional Description

The DMA controller is a flexible and highly configurable DMA controller designed to work efficiently with the Arm Cortex-M33 processor core of the microcontroller. The controller supports multiple data sizes and address increment schemes, multiple levels of priority among DMA channels, and several transfer modes to allow for sophisticated programmed data transfers. Each DMA channel can support all peripheral function, this can be configured independently.

Each channel also has a configurable block transfer size. The arbitration between channels is done at the end of block transfer and according to the priority scheme. Using the block size, it is possible to control exactly how many items are transferred to or from a peripheral every time a DMA service request is made.

Each DMA channel can be assigned as secured or non-secured at device cold boot. The secure or non-secure definition of a DMA channel is defined by the owner (the module which configured the DMA channel) amd the peripheral by the firewall assigned to it.

11.3.1 Channels Assignment

The following table describes the list of peripherals and their index supported by each DMA channel.For example, data transfer from UART RX to memory can be done by assigning the DMA channel to use peripheral index 0.

The channel assignment to the secured/non secured peripherals and/or memory need to verify that both DMA and/or peripheral/memory have the same security level (e.g. assigned secured peripherals/memory to secured DMA channel only).

Index #	Peripheral	Trigger
0	UART0 RX	Any
1	UART0 TX	Any
2	UART1 RX	Any
3	UART1 TX	Any
4	SPI0 RX	Any
5	SPI0 TX	Any
6	SPI1 RX	Any
7	SPI1 TX	Any
8	I2C0 RX	Any
9	I2C0 TX	Any
10	I2C1 RX	Any
11	I2C1 TX	Any
12	SDMMC RX	Any
13	SDMMC TX	Any
14	SDIO RX	Any
15	SDIO TX	Any
16	DCAN RX	Any
17	DCAN TX	Any
18	ADC Read	Any
19	Not Used	Any
20	PDM Read	Any
21	Not Used	Any
22	Wi-Fi/BLE Host Interface (HIF)	Any
23	Wi-Fi/BLE Host Interface (HIF)	Any
24	UART2 RX	Any
25	UART2 TX	Any

11.3.2 Transfer Types

The DMA controller support multiple transfer types. The transfer type for each DMA channel is independently configurable. For example, channel 0 may transfer memory to memory while channel 1 transfers between memory and peripherals. The DMA controller supports the following transfer types:

- Internal Memory to Internal Memory
- Internal Memory to Peripheral
- Peripheral to Internal Memory

11.3.3 Addressing Modes

The DMA controller has 4 addressing modes. The addressing mode for each DMA channel is independently configurable. For example, channel 0 may transfer between two fixed addresses, while channel 1 transfers between two blocks of addresses.

The addressing modes supported are:

1. Fixed address to fixed address (FIFO to FIFO)
2. Fixed address to incremental address (FIFO to Memory)
3. Incremental address to fixed address (Memory to FIFO)
4. Incremental address to Incremental address (Memory to Memory)

11.3.4 Transfer Modes

The DMA controller supports block transfer mode. The block size can be defined for each DMA job and it is individually configured per channel. The supported block sizes are 1-63 words, each word can be either 8/16/32 bits. The job size can be any number of bytes independent of the block size. For single transfer per trigger the block size need to be configured to 1. Therefore, the block size must be the same as the number of data items that the peripheral can accommodate when making a block request. For example, the UART and SPI, which use a mix of single or burst requests, could generate a burst request based on the FIFO trigger level.

The DMA controller responds to two types of requests from a peripheral: single request or block request. Each peripheral can support either or both types of requests. A single request means that the peripheral is ready to transfer one item, while a block request means that the peripheral is ready to transfer multiple items.

When a block request is detected, the DMA controller transfers the number of items that is the lesser of the block size or the number of items remaining in the transfer. Therefore, the block size must be the same as the number of data items that the peripheral can accommodate when making a block request. For example, the UART and SPI, which use a mix of single or block requests, could generate a block request based on the FIFO trigger level.

Each DMA request signal remains asserted until the relevant DMA clear signal is asserted. After the DMA clear signal is deasserted, a request signal can become active again, if conditions are setup correctly. The DMA clear signal must be connected to the DMA active signal from the DMA module. This signal is asserted when DMA is granted access and is active. The DMA active signal is deasserted when the DMA transfer completes. Connecting the DMA active signal from DMA to the DMA request clear input of the peripheral ensures that no requests are generated by the peripheral while the DMA is active.

The burst transfer and single transfer request signals are not mutually exclusive, and both can be asserted at the same time. For example, when there is more data than the watermark level in the receive FIFO, the burst transfer request and the single transfer request are asserted.

The FIFO trigger level at the source/destination memory must fit the block size of the transfer.

For example:

- DMA block size of 4 words (each 1 byte) and transfer to UART (FIFO size 8 bytes)
  - FIFO level trigger in UART should be defined at half empty or half full
- DMA block size of 6 words (each 1 byte) and transfer to UART (FIFO size 8 bytes)
  - RX FIFO level trigger in UART should be ¾ full, signaling to DMA that it has a block to transfer.
  - TX FIFO level trigger in UART should be ¼ full, signaling to DMA that it has space to receive a block.

Each DMA trigger a block is transferred by the DMA until the job is completed. In case the remaining bytes in the last transfer are smaller than the block size the DMA will transfer a single word per single trigger (if enabled).

For example, DMA word size 8 bits:

- UART reads 30 bytes (30 words)
- Block size configured to 4 words
- DMA will perform 9 transactions:
  - 7 block transactions (each 4 words, 4 bytes)
  - 2 single transactions (each 1 word, 1byte)

Another example, DMA word size 16 bits:

- SPI reads 40 bytes (20 words)
- Block size is 8 words
- DMA will perform 6 transactions:
  - 2 block transactions (each 8 words, 16 bytes)
  - 4 single transactions (each 1 word, 2 bytes)

11.3.5 DMA Aligner Support

The DMA supports unaligned address access and unaligned job size (not multiplication of word size) when 32 bits word is used.

The following table describes the supported un-align transactions:

Job Start Address	Job Size	Transactions
Aligned	Aligned	All DMA transactions are address and word aligned.
Aligned	Unaligned	All DMA transactions will be address and word aligned however the last transfer will be < word.
Unaligned	Aligned	The first DMA transactions will be address un-aligned and < word. The last DMA transactions will be address aligned and < word. All other DMA transactions will be address and word aligned.
Unaligned	Unaligned	The first DMA transactions will be address un-aligned and < word. The last DMA transactions might be address aligned and < word. All other DMA transactions will be address and word aligned.

For example: Address aligned, Job Size Aligned

Start address 0x0, Job size 16 bytes

DMA Transaction	Job Address	Byte 0	Byte 1	Byte 2	Byte 3
1	0x0	First byte			
2	0x4				
3	0x8				
4	0xC				Last byte (16)

In this example the job size and address are all aligned.

For example: Address aligned, Job Size Un-Aligned

Start address 0x0, Job size 13 bytes

DMA Transaction	Job Address	Byte 0	Byte 1	Byte 2	Byte 3
1	0x0	First byte			
2	0x4				

DMA Transaction	Job Address	Byte 0	Byte 1	Byte 2	Byte 3
3	0x8				
4	0xC	Last byte (13)			

In this example the job size and address are all aligned.

For example: Address un-aligned, Job Size Un-Aligned

Start address 0x1, Job size 14 bytes

DMA Transaction	Job Address	Byte 0	Byte 1	Byte 2	Byte 3
1	0x0		First byte		
2	0x4				
3	0x8				
4	0xC			Last byte (14)	

In this example the job size and address are un aligned. Both first and last transaction are unaligned (<word)

For example: Address un-aligned, Job Size Un-Aligned

Start address 0x1, Job size 15 bytes

DMA Transaction	Job Address	Byte 0	Byte 1	Byte 2	Byte 3
1	0x0		First byte		
2	0x4				
3	0x8				
4	0xC				Last byte (15)

In this example the job size and address are un aligned. However last transaction is aligned.

11.3.6 Initiating DMA Transfers

Each DMA channel is independently configured. The job and the start transaction are configured and initiated by the SW. The correct sequence involves defining the memory or peripheral which is linked to the specific channel.

11.3.7 Stopping DMA Transfers

A DMA job may be stopped/aborted by the SW. The DMA will stop after the completion of the ongoing block transfer cycle and all the channel registers will stay in the current state. This transfer can be continued and a new job need to be initiated.

11.3.8 Channel Priorities

The DMA controller supports round robin arbitration and up to 2 channels can be assigned as high priority. The round robin arbitration is done according to the channel numbering starting from 0 and up. High priority can be assigned to each channels, up to 2 channel. The high priority channels will be assigned as first and second high priority while the other channels will be served in round robin and the third priority.

The high priority channel is served first. However to prevent starvation of other channels, the max number of consecutive high priory transactions can be limited.

For example:

- Channel 1 is high priority 1 (highest priority) - requests 3 consecutive times
- Channel 4 is high priority 2 - request 1
- Max number of consecutive high priory transaction is set to 4
- The DMA arbitration will be: **1**, **1**, **1**, **4**, 2, 3, 5, **1**, **1**, **1**, **4**, 6, 7, 8, **1**, **1**, **1**, **4**, 9,10,11

For example:

- Channel 1 is high priority 1 (highest priority) - requests 3 consecutive times
- Channel 4 is high priority 2 - request 1
- Max number of consecutive high priory transaction is set to **3**
- The DMA arbitration will be: **1**, **1**, **1**, 2, **4**, 3, 5, **1**, **1**, **1**, 6, **4**, 7, 8, **1**, **1**, **1**, 9, **4**, 10,11

11.3.9 DMA Interrupts

The DMA controller generates a completion interrupt on the interrupt vector of the peripheral when a DMA transfer completes. The DMA channels interrupt are concentrates in the event manager into secured and non secured DMA events driven to the CPU nVIC. All DMA secured channels interrupts are driven to the DMA secured event and the non secured DMA channels interrupts are driven to the to the DMA non-secured event. When DMA event is asserted the CPU can access the event manager and read which DMA channels interrupt has been asserted.

11.4 HOST_DMA Registers

Table 11-1 lists the memory-mapped registers for the HOST_DMA registers. All register offset addresses not listed in Table 11-1 should be considered as reserved locations and the register contents should not be modified.

Table 11-1. HOST_DMA Registers

Offset	Acronym	Register Name	Section
0h	CHCTL0	Channel Assignment Control	Section 11.4.1
4h	CHCTL1	Channel Assignment Map	Section 11.4.2
18h	PRIOCFG	Priority Channel Configuration	Section 11.4.3
1000h	CH0STA	Channel Status	Section 11.4.4
1004h	CH0TIPTR	Input Pointer Address	Section 11.4.5
1008h	CH0OPTR	Output Address Pointer	Section 11.4.6
100Ch	CH0TCTL	Transaction Control	Section 11.4.7
1010h	CH0TCTL2	Transfer Control Configuration	Section 11.4.8
1014h	CH0TSTA	Transaction Status	Section 11.4.9
101Ch	CH0JCTL	Channel Job Control	Section 11.4.10
2000h	CH1STA	Channel Status	Section 11.4.11
2004h	CH1TIPTR	Input Pointer Address	Section 11.4.12
2008h	CH1TOPTR	Output Pointer Address	Section 11.4.13
200Ch	CH1TCTL	Transaction Control	Section 11.4.14
2010h	CH1TCTRL2	Transaction Control	Section 11.4.15
2014h	CH1TSTA	Transaction Status	Section 11.4.16
201Ch	CH1JCTL	Channel Job Control	Section 11.4.17
3000h	CH2STA	Channel Status	Section 11.4.18
3004h	CH2TIPTR	Input Address Pointer	Section 11.4.19
3008h	CH2TOPTR	Output Address Pointer	Section 11.4.20
300Ch	CH2TCTL	Transaction Control	Section 11.4.21
3010h	CH2TCTL2	DMA Command Interface	Section 11.4.22
3014h	CH2TSTA	Transaction Status	Section 11.4.23
301Ch	CH2JCTL	Channel 2 Control	Section 11.4.24
4000h	CH3STA	Channel Status	Section 11.4.25
4004h	CH3TIPTR	Input Address Pointer	Section 11.4.26
4008h	CH3TOPTR	Output Address Pointer	Section 11.4.27
400Ch	CH3TCTL	Transaction Control	Section 11.4.28
4010h	CH3TCTL2	Channel 3 Control	Section 11.4.29
4014h	CH3TSTA	Channel 3 Status	Section 11.4.30
401Ch	CH3JCTL	Channel 3 Control	Section 11.4.31
5000h	CH4STA	Channel Status Information	Section 11.4.32
5004h	CH4TIPTR	Input Address Pointer	Section 11.4.33
5008h	CH4TOPTR	Output Address Pointer	Section 11.4.34
500Ch	CH4TCTL	Transaction Control	Section 11.4.35
5010h	CH4TCTL2	Channel 4 Transfer Control	Section 11.4.36
5014h	CH4TSTA	Transfer Status Channel 4	Section 11.4.37
501Ch	CH4JCTL	Channel 4 Control	Section 11.4.38
6000h	CH5STA	Channel Status	Section 11.4.39
6004h	CH5TIPTR	Input Address Pointer	Section 11.4.40
6008h	CH5TOPTR	Output Address Pointer	Section 11.4.41

Table 11-1. HOST_DMA Registers (continued)

Offset	Acronym	Register Name	Section
600Ch	CH5TCTL	Channel 5 Control	Section 11.4.42
6010h	CH5TCTL2	Transfer Control	Section 11.4.43
6014h	CH5TSTA	Transaction Status	Section 11.4.44
601Ch	CH5JCTL	Channel 5 Control	Section 11.4.45
7000h	CH6STA	Channel Status	Section 11.4.46
7004h	CH6TIPTR	Input Address Pointer	Section 11.4.47
7008h	CH6TOPTR	Output Address Pointer	Section 11.4.48
700Ch	CH6TCTL	Transaction Control	Section 11.4.49
7010h	CH6TCTL2	Channel 6 Control	Section 11.4.50
7014h	CH6TSTA	Transaction Status	Section 11.4.51
701Ch	CH6JCTL	Channel 6 Control	Section 11.4.52
8000h	CH7STA	Channel Status	Section 11.4.53
8004h	CH7TIPTR	Input Address Pointer	Section 11.4.54
8008h	CH7TOPTR	Output Address Pointer	Section 11.4.55
800Ch	CH7TCTL	Transaction Control	Section 11.4.56
8010h	CH7TCTL2	Channel 7 Control	Section 11.4.57
8014h	CH7TSTA	Channel 7 Status	Section 11.4.58
801Ch	CH7JCTL	Channel 7 Control	Section 11.4.59
9000h	CH8STA	Channel Status	Section 11.4.60
9004h	CH8TIPTR	Input Address Pointer	Section 11.4.61
9008h	CH8TOPTR	Output Address Pointer	Section 11.4.62
900Ch	CH8TCTL	Channel 8 Control	Section 11.4.63
9010h	CH8TCTL2	Channel 8 Control	Section 11.4.64
9014h	CH8TSTA	Channel 8 Status	Section 11.4.65
901Ch	CH8JCTL	Channel 8 Control	Section 11.4.66
A000h	CH9STA	Channel Status	Section 11.4.67
A004h	CH9TIPTR	Output Address Pointer	Section 11.4.68
A008h	CH9TOPTR	Output Address Pointer	Section 11.4.69
A00Ch	CH9TCTL	Transaction Control	Section 11.4.70
A010h	CH9TCTL2	Channel 9 Control	Section 11.4.71
A014h	CH9TSTA	Transaction Status	Section 11.4.72
A01Ch	CH9JCTL	Channel 9 Control	Section 11.4.73
B000h	CH10STA	Channel Status	Section 11.4.74
B004h	CH10TIPTR	Input Address Pointer	Section 11.4.75
B008h	CH10TOPTR	Output Address Pointer	Section 11.4.76
B00Ch	CH10TCTL	Channel 10 Control	Section 11.4.77
B010h	CH10TCTL2	Channel 10 Control	Section 11.4.78
B014h	CH10TSTA	Transfer Status	Section 11.4.79
B01Ch	CH10JCTL	Channel 10 Control	Section 11.4.80
C000h	CH11STA	Channel Status Information	Section 11.4.81
C004h	CH11TIPTR	Input Address Pointer	Section 11.4.82
C008h	CH11TOPTR	Output Address Pointer	Section 11.4.83
C00Ch	CH11TCTL	Channel Transaction Control	Section 11.4.84
C010h	CH11TCTL2	Channel 11 Transfer Control	Section 11.4.85
C014h	CH11TSTA	Channel Transaction Status	Section 11.4.86

Table 11-1. HOST_DMA Registers (continued)

Offset	Acronym	Register Name	Section
C01Ch	CH11JCTL	Channel 11 Control	Section 11.4.87
D000h	CH12STA	Channel Status	Section 11.4.88
D004h	CH12TIPTR	Input Pointer	Section 11.4.89
D008h	CH12TOPTR	Output Address Pointer	Section 11.4.90
D00Ch	CH12TCTL	Transaction Control	Section 11.4.91
D010h	CH12TCTL2	Channel 12 Transfer	Section 11.4.92
D014h	CH12TSTA	Transaction Status	Section 11.4.93
D01Ch	CH12JCTL	Job Control	Section 11.4.94
E000h	CH13STA	Channel Status Register	Section 11.4.95
E004h	CH13TIPTR	Input Address Pointer	Section 11.4.96
E008h	CH13TOPTR	Output Address Pointer	Section 11.4.97
E00Ch	CH13TCTL	Channel Transaction Control	Section 11.4.98
E010h	CH13TCTL2	Channel 13 Transfer	Section 11.4.99
E014h	CH13TSTA	Transfer Status	Section 11.4.100
E01Ch	CH13JCTL	Channel 13 Control	Section 11.4.101

Complex bit access types are encoded to fit into small table cells. Table 11-2 shows the codes that are used for access types in this section.

Table 11-2. HOST_DMA Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

11.4.1 CHCTL0 Register (Offset = 0h) [Reset = 00000000h]

CHCTL0 is shown in Table 11-3.

Return to the Summary Table.

Host DMA Channel Controlled by Defined Peripheral. The value of each fields concats with [HOST_DMA:JOBCTLCHx.SRCDSTCFG] (when x is channel num) if [CHCTL0.CHx] = 4 and [JOBCTLCHx.SRCDSTCFG] = 1 (value = 0100_1 = 9) then flow control signals of channel x are connected to periph number 9 flow control signals Note: [CHCTL0.CHx] = 0xF is forbidden. This configuration should be only used for Dynamic Switch

Table 11-3. CHCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	CH7	R/W	0h	Channel 7 Control. The following Enums represent the configuration values to bind the DMA channel to each peripheral: 0h = UART0 peripheral 1h = UART1 peripheral 2h = SPI0 peripheral 3h = SPI1 peripheral 4h = I2C0 peripheral 5h = I2C1 peripheral 6h = SDMMC peripheral 7h = SDIO peripheral 8h = DCAN peripheral 9h = ADC peripheral Ah = PDM peripheral Bh = HIF peripheral Ch = UART2 peripheral
27-24	CH6	R/W	0h	Channel 6 Control. The following Enums represent the configuration values to bind the DMA channel to each peripheral: 0h = UART0 peripheral 1h = UART1 peripheral 2h = SPI0 peripheral 3h = SPI1 peripheral 4h = I2C0 peripheral 5h = I2C1 peripheral 6h = SDMMC peripheral 7h = SDIO peripheral 8h = DCAN peripheral 9h = ADC peripheral Ah = PDM peripheral Bh = HIF peripheral Ch = UART2 peripheral
23-20	CH5	R/W	0h	Channel 5 Control. The following Enums represent the configuration values to bind the DMA channel to each peripheral: 0h = UART0 peripheral 1h = UART1 peripheral 2h = SPI0 peripheral 3h = SPI1 peripheral 4h = I2C0 peripheral 5h = I2C1 peripheral 6h = SDMMC peripheral 7h = SDIO peripheral 8h = DCAN peripheral 9h = ADC peripheral Ah = PDM peripheral Bh = HIF peripheral Ch = UART2 peripheral

Table 11-3. CHCTL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-16	CH4	R/W	0h	Channel 4 Control. The following Enums represent the configuration values to bind the DMA channel to each peripheral: 0h = UART0 peripheral 1h = UART1 peripheral 2h = SPI0 peripheral 3h = SPI1 peripheral 4h = I2C0 peripheral 5h = I2C1 peripheral 6h = SDMMC peripheral 7h = SDIO peripheral 8h = DCAN peripheral 9h = ADC peripheral Ah = PDM peripheral Bh = HIF peripheral Ch = UART2 peripheral
15-12	CH3	R/W	0h	Channel 3 Control. The following Enums represent the configuration values to bind the DMA channel to each peripheral: 0h = UART0 peripheral 1h = UART1 peripheral 2h = SPI0 peripheral 3h = SPI1 peripheral 4h = I2C0 peripheral 5h = I2C1 peripheral 6h = SDMMC peripheral 7h = SDIO peripheral 8h = DCAN peripheral 9h = ADC peripheral Ah = PDM peripheral Bh = HIF peripheral Ch = UART2 peripheral
11-8	CH2	R/W	0h	Channel 2 Control. The following Enums represent the configuration values to bind the DMA channel to each peripheral: 0h = UART0 peripheral 1h = UART1 peripheral 2h = SPI0 peripheral 3h = SPI1 peripheral 4h = I2C0 peripheral 5h = I2C1 peripheral 6h = SDMMC peripheral 7h = SDIO peripheral 8h = DCAN peripheral 9h = ADC peripheral Ah = PDM peripheral Bh = HIF peripheral Ch = UART2 peripheral
7-4	CH1	R/W	0h	Channel 1 Control. The following Enums represent the configuration values to bind the DMA channel to each peripheral: 0h = UART0 peripheral 1h = UART1 peripheral 2h = SPI0 peripheral 3h = SPI1 peripheral 4h = I2C0 peripheral 5h = I2C1 peripheral 6h = SDMMC peripheral 7h = SDIO peripheral 8h = DCAN peripheral 9h = ADC peripheral Ah = PDM peripheral Bh = HIF peripheral Ch = UART2 peripheral

Table 11-3. CHCTL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CH0	R/W	0h	Channel 0 Control. The following Enums represent the configuration values to bind the DMA channel to each peripheral: 0h = UART0 peripheral 1h = UART1 peripheral 2h = SPI0 peripheral 3h = SPI1 peripheral 4h = I2C0 peripheral 5h = I2C1 peripheral 6h = SDMMC peripheral 7h = SDIO peripheral 8h = DCAN peripheral 9h = ADC peripheral Ah = PDM peripheral Bh = HIF peripheral Ch = UART2 peripheral

11.4.2 CHCTL1 Register (Offset = 4h) [Reset = 00000000h]

CHCTL1 is shown in Table 11-4.

Return to the Summary Table.

Host DMA Channel Controlled by Defined Peripheral. The value of each fields concats with [HOST_DMA:JOBCTLCHx.SRCDSTCFG] (when x is channel num) if [CHCTL1.CHx] = 4 and [JOBCTLCHx.SRCDSTCFG] = 1 (value = 0100_1 = 9) then flow control signals of channel x are connected to periph number 9 flow control signals Note: [CHCTL0.CHx] = 0xF is forbidden. This configuration should be only used for Dynamic Switch

Table 11-4. CHCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-20	CH13	R/W	0h	Channel 13 Control. The following Enums represent the configuration values to bind the DMA channel to each peripheral: 0h = UART0 peripheral 1h = UART1 peripheral 2h = SPI0 peripheral 3h = SPI1 peripheral 4h = I2C0 peripheral 5h = I2C1 peripheral 6h = SDMMC peripheral 7h = SDIO peripheral 8h = DCAN peripheral 9h = ADC peripheral Ah = PDM peripheral Bh = HIF peripheral Ch = UART2 peripheral
19-16	CH12	R/W	0h	Channel 12 Control. The following Enums represent the configuration values to bind the DMA channel to each peripheral: 0h = UART0 peripheral 1h = UART1 peripheral 2h = SPI0 peripheral 3h = SPI1 peripheral 4h = I2C0 peripheral 5h = I2C1 peripheral 6h = SDMMC peripheral 7h = SDIO peripheral 8h = DCAN peripheral 9h = ADC peripheral Ah = PDM peripheral Bh = HIF peripheral Ch = UART2 peripheral
15-12	CH11	R/W	0h	Channel 11 Control. The following Enums represent the configuration values to bind the DMA channel to each peripheral: 0h = UART0 peripheral 1h = UART1 peripheral 2h = SPI0 peripheral 3h = SPI1 peripheral 4h = I2C0 peripheral 5h = I2C1 peripheral 6h = SDMMC peripheral 7h = SDIO peripheral 8h = DCAN peripheral 9h = ADC peripheral Ah = PDM peripheral Bh = HIF peripheral Ch = UART2 peripheral

Table 11-4. CHCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-8	CH10	R/W	0h	Channel 10 Control. The following Enums represent the configuration values to bind the DMA channel to each peripheral: 0h = UART0 peripheral 1h = UART1 peripheral 2h = SPI0 peripheral 3h = SPI1 peripheral 4h = I2C0 peripheral 5h = I2C1 peripheral 6h = SDMMC peripheral 7h = SDIO peripheral 8h = DCAN peripheral 9h = ADC peripheral Ah = PDM peripheral Bh = HIF peripheral Ch = UART2 peripheral
7-4	CH9	R/W	0h	Channel 9 Control. The following Enums represent the configuration values to bind the DMA channel to each peripheral: 0h = UART0 peripheral 1h = UART1 peripheral 2h = SPI0 peripheral 3h = SPI1 peripheral 4h = I2C0 peripheral 5h = I2C1 peripheral 6h = SDMMC peripheral 7h = SDIO peripheral 8h = DCAN peripheral 9h = ADC peripheral Ah = PDM peripheral Bh = HIF peripheral Ch = UART2 peripheral
3-0	CH8	R/W	0h	Channel 8 Control. The following Enums represent the configuration values to bind the DMA channel to each peripheral: 0h = UART0 peripheral 1h = UART1 peripheral 2h = SPI0 peripheral 3h = SPI1 peripheral 4h = I2C0 peripheral 5h = I2C1 peripheral 6h = SDMMC peripheral 7h = SDIO peripheral 8h = DCAN peripheral 9h = ADC peripheral Ah = PDM peripheral Bh = HIF peripheral Ch = UART2 peripheral

11.4.3 PRIOCFG Register (Offset = 18h) [Reset = 1F0F0F00h]

PRIOCFG is shown in Table 11-5.

Return to the Summary Table.

Priority Channel Configuration.

Table 11-5. PRIOCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28-24	MAXBLOCKS	R/W	1Fh	Maximum consecutive priority blocks. Maximum consecutive block transactions of 'priority channels' . After this number of consecutive blocks one of 'roubd robin' channels will win arbitration. 31 means there is no limitation on number of consecutive priority blocks
23-20	RESERVED	R	0h	Reserved
19-16	CH2ND	R/W	Fh	Second priority channel. channel with second highest prioriry
15-12	RESERVED	R	0h	Reserved
11-8	CH1ST	R/W	Fh	First priority channel. channel with highest prioriry
7-1	RESERVED	R	0h	Reserved
0	PRIOEN	R/W	0h	Enable priority channel. Enable one channel to be prioritize - no round rubin would be done

11.4.4 CH0STA Register (Offset = 1000h) [Reset = 00000000h]

CH0STA is shown in Table 11-6.

Return to the Summary Table.

Channel Status FSM state and run indication.

Table 11-6. CH0STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	RUN	R	0h	Indication that channel is currently transfering data and is not idle. Channels that are waiting on arbitration are considered running.
15-12	RESERVED	R	0h	Reserved
11-8	FSMSTATE	R	0h	FSM state: 0x0. IDLE 0x2. EXCEPTION 0x3. DRAIN 0x4. ABORT 0x8. PENDING ARB 0x9. COPY 0xA. COPY LAST 0xC. DONE 0xD. SAVE CTX 0xE. WAIT NEXT TRANS 0xF. LAST
7-3	RESERVED	R	0h	Reserved
2-0	HWEVENT	R	0h	HW event status. Channel status is a bit mask. Multiple bits can be set at the same time 0. PROCESSING 1. TRANS DONE 2. ABORT 4. EXCEPTION

11.4.5 CH0TIPTR Register (Offset = 1004h) [Reset = 00000000h]

CH0TIPTR is shown in Table 11-7.

Return to the Summary Table.

Input Pointer Channel Transaction. 32 bit address pointer of channel current input.

Table 11-7. CH0TIPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IPTR	R/W	0h	Transaction input pointer. 32 bit address pointer of channel current input.

11.4.6 CH0OPTR Register (Offset = 1008h) [Reset = 00000000h]

CH0OPTR is shown in Table 11-8.

Return to the Summary Table.

Output Pointer Channel Transaction. 32 bit address pointer of channel current output.

Table 11-8. CH0OPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	OPTR	R/W	0h	Transaction output pointer. 32 bit address pointer of channel current output.

11.4.7 CH0TCTL Register (Offset = 100Ch) [Reset = 00000000h]

CH0TCTL is shown in Table 11-9.

Return to the Summary Table.

Transaction control

Table 11-9. CH0TCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-24	ENDIANESS	R/W	0h	0 -no endianess, 1 - byte endianess, 2 - bit endianess
23-18	RESERVED	R	0h	Reserved
17	SPARE	R/W	0h	spare
16	BURSTREQ	R/W	0h	Use burst request. In case number of words to tranfer smaller than block size, DMA would use signle request and work with block size of 1 word. In case we know request would be set on altough number of words to tranfer is smaller than block size, we can set this field on and DMA will wait for block_request and transact all remaining words in one block.
15-14	RESERVED	R	0h	Reserved
13-0	TRANSB	R/W	0h	Transaction bytes number. Number of bytes of the transaction to move from source to destination.

11.4.8 CH0TCTL2 Register (Offset = 1010h) [Reset = 00000000h]

CH0TCTL2 is shown in Table 11-10.

Return to the Summary Table.

DMA command interface

Table 11-10. CH0TCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CMD	W	0h	1 - run command. Start a transaction. 2- abort command - stop reansaction. 4- init command - init new transaction afet abort/error. Type:Write-Clear.

11.4.9 CH0TSTA Register (Offset = 1014h) [Reset = 00000000h]

CH0TSTA is shown in Table 11-11.

Return to the Summary Table.

Transaction Status. Job completion reason - either last transaction or exception

Table 11-11. CH0TSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	REMAINB	R	0h	Remain bytes number. Number of bytes remaining to complete the transaction.
15-8	OFFSET	R	0h	Word offset. Offset in words from block boundary. Actually number of word have been transferred in this block
7-1	RESERVED	R	0h	Reserved
0	STA	R	0h	channel OCP rstatus recieved at one of the primary ports. Once an error is encountered the channel will enter an Exception state and stay the until an init command is recieved. ICLR does not affect this status.

11.4.10 CH0JCTL Register (Offset = 101Ch) [Reset = 00000000h]

CH0JCTL is shown in Table 11-12.

Return to the Summary Table.

Job control register

Table 11-12. CH0JCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	ENCLR	R/W	0h	Enable DMA to set a rd/wr clear pulse at the beginning of a job (one cycle after run cmd)
29	SRCDSTCFG	R/W	0h	0 - Sorce is periph: transaction from periph to memory. 1 - Destination is periph :transaction from Memory to periph
28	FIFOMODD	R/W	0h	Destination pointer fifo mode
27	FIFOMODS	R/W	0h	Source pointer fifo mode
26	DMASIGBPS	R/W	0h	Tie high channel DMA req signal. This is useful for memory to memort transaction
25	BLKMODEDST	R/W	0h	Destination pointer wrap around mode 0: no wrap around(non block mode) 1: with wrap around(block mode)
24	BLKMODESRC	R/W	0h	source pointer wrap around mode 0: no wrap around(non block mode) 1: with wrap around(block mode)
23-22	RESERVED	R	0h	Reserved
21-16	BLKSIZE	R/W	0h	size of the block in words. If block mode is enabled, defines the address wrap around. Since channel arbitration decisions are made every block, this also effect how much bandwidth is given to a specific channel.
15-2	RESERVED	R	0h	Reserved
1-0	WORDSIZE	R/W	0h	00 -word size is 32 bits 01 -word size is 16 bits 10 -word size is 8 bits

11.4.11 CH1STA Register (Offset = 2000h) [Reset = 00000000h]

CH1STA is shown in Table 11-13.

Return to the Summary Table.

Channel Status FSM state and run indication.

Table 11-13. CH1STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	RUN	R	0h	Indication that channel is currently transfering data and is not idle. Channels that are waiting on arbitration are considered running.
15-12	RESERVED	R	0h	Reserved
11-8	FSMSTATE	R	0h	FSM state: 0x0. IDLE 0x2. EXCEPTION 0x3. DRAIN 0x4. ABORT 0x8. PENDING ARB 0x9. COPY 0xA. COPY LAST 0xC. DONE 0xD. SAVE CTX 0xE. WAIT NEXT TRANS 0xF. LAST
7-3	RESERVED	R	0h	Reserved
2-0	HWEVENT	R	0h	HW event status. Channel status is a bit mask. Multiple bits can be set at the same time 0. PROCESSING 1. TRANS DONE 2. ABORT 4. EXCEPTION

11.4.12 CH1TIPTR Register (Offset = 2004h) [Reset = 00000000h]

CH1TIPTR is shown in Table 11-14.

Return to the Summary Table.

32 bit address pointer of channel current input.

Table 11-14. CH1TIPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IPTR	R/W	0h	32 bit address pointer of channel current input.

11.4.13 CH1TOPTR Register (Offset = 2008h) [Reset = 00000000h]

CH1TOPTR is shown in Table 11-15.

Return to the Summary Table.

32 bit address pointer of channel current output.

Table 11-15. CH1TOPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	OPTR	R/W	0h	32 bit address pointer of channel current output.

11.4.14 CH1TCTL Register (Offset = 200Ch) [Reset = 00000000h]

CH1TCTL is shown in Table 11-16.

Return to the Summary Table.

Transaction control

Table 11-16. CH1TCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-24	ENDIANESS	R/W	0h	0 -no endianess, 1 - byte endianess, 2 - bit endianess
23-18	RESERVED	R	0h	Reserved
17	SPARE	R/W	0h	spare
16	BURSTREQ	R/W	0h	In case number of words to tranfer smaller than block size, DMA would use signle request and work with block size of 1 word. In case we know request would be set on altough number of words to tranfer is smaller than block size, we can set this field on and DMA will wait for block_request and transact all remaining words in one block.
15-14	RESERVED	R	0h	Reserved
13-0	TRANSB	R/W	0h	Number of bytes of the transaction to move from source to destination.

11.4.15 CH1TCTRL2 Register (Offset = 2010h) [Reset = 00000000h]

CH1TCTRL2 is shown in Table 11-17.

Return to the Summary Table.

DMA command interface

Table 11-17. CH1TCTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CMD	W	0h	1 - run command. Start a transaction. 2- abort command - stop reansaction. 4- init command - init new transaction afet abort/error.

11.4.16 CH1TSTA Register (Offset = 2014h) [Reset = 00000000h]

CH1TSTA is shown in Table 11-18.

Return to the Summary Table.

Job completion reason - either last transaction or exception

Table 11-18. CH1TSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	REMAINB	R	0h	Number of bytes remaining to complete the transaction.
15-8	OFFSET	R	0h	Offset in words from block boundary. Actually number of word have been transferred in this block
7-1	RESERVED	R	0h	Reserved
0	STA	R	0h	channel OCP rstatus recieved at one of the primary ports. Once an error is encountered the channel will enter an Exception state and stay the until an init command is recieved. ICLR does not affect this status.

11.4.17 CH1JCTL Register (Offset = 201Ch) [Reset = 00000000h]

CH1JCTL is shown in Table 11-19.

Return to the Summary Table.

Job control register

Table 11-19. CH1JCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	ENCLR	R/W	0h	Enable DMA to set a rd/wr clear pulse at the beginning of a job (one cycle after run cmd)
29	SRCDSTCFG	R/W	0h	0 - Sorce is periph: transaction from periph to memory. 1 - Destination is periph :transaction from Memory to periph
28	FIFOMODD	R/W	0h	Destination pointer fifo mode
27	FIFOMODS	R/W	0h	Source pointer fifo mode
26	DMASIGBPS	R/W	0h	Tie high channel DMA req signal. This is useful for memory to memort transaction
25	BLKMODEDST	R/W	0h	Destination pointer wrap around mode 0: no wrap around(non block mode) 1: with wrap around(block mode)
24	BLKMODESRC	R/W	0h	source pointer wrap around mode 0: no wrap around(non block mode) 1: with wrap around(block mode)
23-22	RESERVED	R	0h	Reserved
21-16	BLKSIZE	R/W	0h	size of the block in words. If block mode is enabled, defines the address wrap around. Since channel arbitration decisions are made every block, this also effect how much bandwidth is given to a specific channel.
15-2	RESERVED	R	0h	Reserved
1-0	WORDSIZE	R/W	0h	00 -word size is 32 bits 01 -word size is 16 bits 10 -word size is 8 bits

11.4.18 CH2STA Register (Offset = 3000h) [Reset = 00000000h]

CH2STA is shown in Table 11-20.

Return to the Summary Table.

Channel Status FSM state and run indication.

Table 11-20. CH2STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	RUN	R	0h	Indication that channel is currently transfering data and is not idle. Channels that are waiting on arbitration are considered running.
15-12	RESERVED	R	0h	Reserved
11-8	FSMSTATE	R	0h	FSM state: 0x0. IDLE 0x2. EXCEPTION 0x3. DRAIN 0x4. ABORT 0x8. PENDING ARB 0x9. COPY 0xA. COPY LAST 0xC. DONE 0xD. SAVE CTX 0xE. WAIT NEXT TRANS 0xF. LAST
7-3	RESERVED	R	0h	Reserved
2-0	HWEVENT	R	0h	HW event status. Channel status is a bit mask. Multiple bits can be set at the same time 0. PROCESSING 1. TRANS DONE 2. ABORT 4. EXCEPTION

11.4.19 CH2TIPTR Register (Offset = 3004h) [Reset = 00000000h]

CH2TIPTR is shown in Table 11-21.

Return to the Summary Table.

32 bit address pointer of channel current input.

Table 11-21. CH2TIPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IPTR	R/W	0h	32 bit address pointer of channel current input.

11.4.20 CH2TOPTR Register (Offset = 3008h) [Reset = 00000000h]

CH2TOPTR is shown in Table 11-22.

Return to the Summary Table.

32 bit address pointer of channel current output.

Table 11-22. CH2TOPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	OPTR	R/W	0h	32 bit address pointer of channel current output.

11.4.21 CH2TCTL Register (Offset = 300Ch) [Reset = 00000000h]

CH2TCTL is shown in Table 11-23.

Return to the Summary Table.

Transaction control

Table 11-23. CH2TCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-24	ENDIANESS	R/W	0h	0 -no endianess, 1 - byte endianess, 2 - bit endianess
23-18	RESERVED	R	0h	Reserved
17	SPARE	R/W	0h	spare
16	BURSTREQ	R/W	0h	In case number of words to tranfer smaller than block size, DMA would use signle request and work with block size of 1 word. In case we know request would be set on altough number of words to tranfer is smaller than block size, we can set this field on and DMA will wait for block_request and transact all remaining words in one block.
15-14	RESERVED	R	0h	Reserved
13-0	TRANSB	R/W	0h	Number of bytes of the transaction to move from source to destination.

11.4.22 CH2TCTL2 Register (Offset = 3010h) [Reset = 00000000h]

CH2TCTL2 is shown in Table 11-24.

Return to the Summary Table.

DMA command interface

Table 11-24. CH2TCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CMD	W	0h	1 - run command. Start a transaction. 2- abort command - stop reansaction. 4- init command - init new transaction afet abort/error.

11.4.23 CH2TSTA Register (Offset = 3014h) [Reset = 00000000h]

CH2TSTA is shown in Table 11-25.

Return to the Summary Table.

Job completion reason - either last transaction or exception

Table 11-25. CH2TSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	REMAINB	R	0h	Number of bytes remaining to complete the transaction.
15-8	OFFSET	R	0h	Offset in words from block boundary. Actually number of word have been transferred in this block
7-1	RESERVED	R	0h	Reserved
0	STA	R	0h	channel OCP rstatus recieved at one of the primary ports. Once an error is encountered the channel will enter an Exception state and stay the until an init command is recieved. ICLR does not affect this status.

11.4.24 CH2JCTL Register (Offset = 301Ch) [Reset = 00000000h]

CH2JCTL is shown in Table 11-26.

Return to the Summary Table.

Job control register

Table 11-26. CH2JCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	ENCLR	R/W	0h	Enable DMA to set a rd/wr clear pulse at the beginning of a job (one cycle after run cmd)
29	SRCDSTCFG	R/W	0h	0 - Sorce is periph: transaction from periph to memory. 1 - Destination is periph :transaction from Memory to periph
28	FIFOMODD	R/W	0h	Destination pointer fifo mode
27	FIFOMODS	R/W	0h	Source pointer fifo mode
26	DMASIGBPS	R/W	0h	Tie high channel DMA req signal. This is useful for memory to memort transaction
25-22	RESERVED	R	0h	Reserved
21-16	BLKSIZE	R/W	0h	size of the block in words. If block mode is enabled, defines the address wrap around. Since channel arbitration decisions are made every block, this also effect how much bandwidth is given to a specific channel.
15-2	RESERVED	R	0h	Reserved
1-0	WORDSIZE	R/W	0h	00 -word size is 32 bits 01 -word size is 16 bits 10 -word size is 8 bits

11.4.25 CH3STA Register (Offset = 4000h) [Reset = 00000000h]

CH3STA is shown in Table 11-27.

Return to the Summary Table.

Channel Status FSM state and run indication.

Table 11-27. CH3STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	RUN	R	0h	Indication that channel is currently transfering data and is not idle. Channels that are waiting on arbitration are considered running.
15-12	RESERVED	R	0h	Reserved
11-8	FSMSTATE	R	0h	FSM state: 0x0. IDLE 0x2. EXCEPTION 0x3. DRAIN 0x4. ABORT 0x8. PENDING ARB 0x9. COPY 0xA. COPY LAST 0xC. DONE 0xD. SAVE CTX 0xE. WAIT NEXT TRANS 0xF. LAST
7-3	RESERVED	R	0h	Reserved
2-0	HWEVENT	R	0h	HW event status. Channel status is a bit mask. Multiple bits can be set at the same time 0. PROCESSING 1. TRANS DONE 2. ABORT 4. EXCEPTION

11.4.26 CH3TIPTR Register (Offset = 4004h) [Reset = 00000000h]

CH3TIPTR is shown in Table 11-28.

Return to the Summary Table.

32 bit address pointer of channel current input.

Table 11-28. CH3TIPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IPTR	R/W	0h	32 bit address pointer of channel current input.

11.4.27 CH3TOPTR Register (Offset = 4008h) [Reset = 00000000h]

CH3TOPTR is shown in Table 11-29.

Return to the Summary Table.

32 bit address pointer of channel current output.

Table 11-29. CH3TOPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	OPTR	R/W	0h	32 bit address pointer of channel current output.

11.4.28 CH3TCTL Register (Offset = 400Ch) [Reset = 00000000h]

CH3TCTL is shown in Table 11-30.

Return to the Summary Table.

Transaction control

Table 11-30. CH3TCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-24	ENDIANESS	R/W	0h	0 -no endianess, 1 - byte endianess, 2 - bit endianess
23-18	RESERVED	R	0h	Reserved
17	SPARE	R/W	0h	spare
16	BURSTREQ	R/W	0h	In case number of words to tranfer smaller than block size, DMA would use signle request and work with block size of 1 word. In case we know request would be set on altough number of words to tranfer is smaller than block size, we can set this field on and DMA will wait for block_request and transact all remaining words in one block.
15-14	RESERVED	R	0h	Reserved
13-0	TRANSB	R/W	0h	Number of bytes of the transaction to move from source to destination.

11.4.29 CH3TCTL2 Register (Offset = 4010h) [Reset = 00000000h]

CH3TCTL2 is shown in Table 11-31.

Return to the Summary Table.

DMA command interface

Table 11-31. CH3TCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CMD	W	0h	1 - run command. Start a transaction. 2- abort command - stop reansaction. 4- init command - init new transaction afet abort/error.

11.4.30 CH3TSTA Register (Offset = 4014h) [Reset = 00000000h]

CH3TSTA is shown in Table 11-32.

Return to the Summary Table.

Job completion reason - either last transaction or exception

Table 11-32. CH3TSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	REMAINB	R	0h	Number of bytes remaining to complete the transaction.
15-8	OFFSET	R	0h	Offset in words from block boundary. Actually number of word have been transferred in this block
7-1	RESERVED	R	0h	Reserved
0	STA	R	0h	channel OCP rstatus recieved at one of the primary ports. Once an error is encountered the channel will enter an Exception state and stay the until an init command is recieved. ICLR does not affect this status.

11.4.31 CH3JCTL Register (Offset = 401Ch) [Reset = 00000000h]

CH3JCTL is shown in Table 11-33.

Return to the Summary Table.

Job control register

Table 11-33. CH3JCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	ENCLR	R/W	0h	Enable DMA to set a rd/wr clear pulse at the beginning of a job (one cycle after run cmd)
29	SRCDSTCFG	R/W	0h	0 - Sorce is periph: transaction from periph to memory. 1 - Destination is periph :transaction from Memory to periph
28	FIFOMODD	R/W	0h	Destination pointer fifo mode
27	FIFOMODS	R/W	0h	Source pointer fifo mode
26	DMASIGBPS	R/W	0h	Tie high channel DMA req signal. This is useful for memory to memort transaction
25-22	RESERVED	R	0h	Reserved
21-16	BLKSIZE	R/W	0h	size of the block in words. If block mode is enabled, defines the address wrap around. Since channel arbitration decisions are made every block, this also effect how much bandwidth is given to a specific channel.
15-2	RESERVED	R	0h	Reserved
1-0	WORDSIZE	R/W	0h	00 -word size is 32 bits 01 -word size is 16 bits 10 -word size is 8 bits

11.4.32 CH4STA Register (Offset = 5000h) [Reset = 00000000h]

CH4STA is shown in Table 11-34.

Return to the Summary Table.

Channel Status FSM state and run indication.

Table 11-34. CH4STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	RUN	R	0h	Indication that channel is currently transfering data and is not idle. Channels that are waiting on arbitration are considered running.
15-12	RESERVED	R	0h	Reserved
11-8	FSMSTATE	R	0h	FSM state: 0x0. IDLE 0x2. EXCEPTION 0x3. DRAIN 0x4. ABORT 0x8. PENDING ARB 0x9. COPY 0xA. COPY LAST 0xC. DONE 0xD. SAVE CTX 0xE. WAIT NEXT TRANS 0xF. LAST
7-3	RESERVED	R	0h	Reserved
2-0	HWEVENT	R	0h	HW event status. Channel status is a bit mask. Multiple bits can be set at the same time 0. PROCESSING 1. TRANS DONE 2. ABORT 4. EXCEPTION

11.4.33 CH4TIPTR Register (Offset = 5004h) [Reset = 00000000h]

CH4TIPTR is shown in Table 11-35.

Return to the Summary Table.

32 bit address pointer of channel current input.

Table 11-35. CH4TIPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	INPTR	R/W	0h	32 bit address pointer of channel current input.

11.4.34 CH4TOPTR Register (Offset = 5008h) [Reset = 00000000h]

CH4TOPTR is shown in Table 11-36.

Return to the Summary Table.

32 bit address pointer of channel current output.

Table 11-36. CH4TOPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	OPTR	R/W	0h	32 bit address pointer of channel current output.

11.4.35 CH4TCTL Register (Offset = 500Ch) [Reset = 00000000h]

CH4TCTL is shown in Table 11-37.

Return to the Summary Table.

Transaction control

Table 11-37. CH4TCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-24	ENDIANESS	R/W	0h	0 -no endianess, 1 - byte endianess, 2 - bit endianess
23-18	RESERVED	R	0h	Reserved
17	SPARE	R/W	0h	spare
16	BURSTREQ	R/W	0h	In case number of words to tranfer smaller than block size, DMA would use signle request and work with block size of 1 word. In case we know request would be set on altough number of words to tranfer is smaller than block size, we can set this field on and DMA will wait for block_request and transact all remaining words in one block.
15-14	RESERVED	R	0h	Reserved
13-0	TRANSB	R/W	0h	Number of bytes of the transaction to move from source to destination.

11.4.36 CH4TCTL2 Register (Offset = 5010h) [Reset = 00000000h]

CH4TCTL2 is shown in Table 11-38.

Return to the Summary Table.

DMA command interface

Table 11-38. CH4TCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CMD	W	0h	1 - run command. Start a transaction. 2- abort command - stop reansaction. 4- init command - init new transaction afet abort/error.

11.4.37 CH4TSTA Register (Offset = 5014h) [Reset = 00000000h]

CH4TSTA is shown in Table 11-39.

Return to the Summary Table.

Job completion reason - either last transaction or exception

Table 11-39. CH4TSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	REMAINB	R	0h	Number of bytes remaining to complete the transaction.
15-8	OFFSET	R	0h	Offset in words from block boundary. Actually number of word have been transferred in this block
7-1	RESERVED	R	0h	Reserved
0	STA	R	0h	channel OCP rstatus recieved at one of the primary ports. Once an error is encountered the channel will enter an Exception state and stay the until an init command is recieved. ICLR does not affect this status.

11.4.38 CH4JCTL Register (Offset = 501Ch) [Reset = 00000000h]

CH4JCTL is shown in Table 11-40.

Return to the Summary Table.

Job control register

Table 11-40. CH4JCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	ENCLR	R/W	0h	Enable DMA to set a rd/wr clear pulse at the beginning of a job (one cycle after run cmd)
29	SRCDSTCFG	R/W	0h	0 - Sorce is periph: transaction from periph to memory. 1 - Destination is periph :transaction from Memory to periph
28	FIFOMODD	R/W	0h	Destination pointer fifo mode
27	FIFOMODS	R/W	0h	Source pointer fifo mode
26	DMASIGBPS	R/W	0h	Tie high channel DMA req signal. This is useful for memory to memort transaction
25-22	RESERVED	R	0h	Reserved
21-16	BLKSIZE	R/W	0h	size of the block in words. If block mode is enabled, defines the address wrap around. Since channel arbitration decisions are made every block, this also effect how much bandwidth is given to a specific channel.
15-2	RESERVED	R	0h	Reserved
1-0	WORDSIZE	R/W	0h	00 -word size is 32 bits 01 -word size is 16 bits 10 -word size is 8 bits

11.4.39 CH5STA Register (Offset = 6000h) [Reset = 00000000h]

CH5STA is shown in Table 11-41.

Return to the Summary Table.

Channel Status FSM state and run indication.

Table 11-41. CH5STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	RUN	R	0h	Indication that channel is currently transfering data and is not idle. Channels that are waiting on arbitration are considered running.
15-12	RESERVED	R	0h	Reserved
11-8	FSMSTATE	R	0h	FSM state: 0x0. IDLE 0x2. EXCEPTION 0x3. DRAIN 0x4. ABORT 0x8. PENDING ARB 0x9. COPY 0xA. COPY LAST 0xC. DONE 0xD. SAVE CTX 0xE. WAIT NEXT TRANS 0xF. LAST
7-3	RESERVED	R	0h	Reserved
2-0	HWEVENT	R	0h	HW event status. Channel status is a bit mask. Multiple bits can be set at the same time 0. PROCESSING 1. TRANS DONE 2. ABORT 4. EXCEPTION

11.4.40 CH5TIPTR Register (Offset = 6004h) [Reset = 00000000h]

CH5TIPTR is shown in Table 11-42.

Return to the Summary Table.

32 bit address pointer of channel current input.

Table 11-42. CH5TIPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IPTR	R/W	0h	32 bit address pointer of channel current input.

11.4.41 CH5TOPTR Register (Offset = 6008h) [Reset = 00000000h]

CH5TOPTR is shown in Table 11-43.

Return to the Summary Table.

32 bit address pointer of channel current output.

Table 11-43. CH5TOPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	OPTR	R/W	0h	32 bit address pointer of channel current output.

11.4.42 CH5TCTL Register (Offset = 600Ch) [Reset = 00000000h]

CH5TCTL is shown in Table 11-44.

Return to the Summary Table.

Transaction control

Table 11-44. CH5TCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-24	ENDIANESS	R/W	0h	0 -no endianess, 1 - byte endianess, 2 - bit endianess
23-18	RESERVED	R	0h	Reserved
17	SPARE	R/W	0h	spare
16	BURSTREQ	R/W	0h	In case number of words to tranfer smaller than block size, DMA would use signle request and work with block size of 1 word. In case we know request would be set on altough number of words to tranfer is smaller than block size, we can set this field on and DMA will wait for block_request and transact all remaining words in one block.
15-14	RESERVED	R	0h	Reserved
13-0	TRANSB	R/W	0h	Number of bytes of the transaction to move from source to destination.

11.4.43 CH5TCTL2 Register (Offset = 6010h) [Reset = 00000000h]

CH5TCTL2 is shown in Table 11-45.

Return to the Summary Table.

DMA command interface

Table 11-45. CH5TCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CMD	W	0h	1 - run command. Start a transaction. 2- abort command - stop reansaction. 4- init command - init new transaction afet abort/error.

11.4.44 CH5TSTA Register (Offset = 6014h) [Reset = 00000000h]

CH5TSTA is shown in Table 11-46.

Return to the Summary Table.

Job completion reason - either last transaction or exception

Table 11-46. CH5TSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	REMAINB	R	0h	Number of bytes remaining to complete the transaction.
15-8	OFFSET	R	0h	Offset in words from block boundary. Actually number of word have been transferred in this block
7-1	RESERVED	R	0h	Reserved
0	STA	R	0h	channel OCP rstatus recieved at one of the primary ports. Once an error is encountered the channel will enter an Exception state and stay the until an init command is recieved. ICLR does not affect this status.

11.4.45 CH5JCTL Register (Offset = 601Ch) [Reset = 00000000h]

CH5JCTL is shown in Table 11-47.

Return to the Summary Table.

Job control register

Table 11-47. CH5JCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	ENCLR	R/W	0h	Enable DMA to set a rd/wr clear pulse at the beginning of a job (one cycle after run cmd)
29	SRCDSTCFG	R/W	0h	0 - Sorce is periph: transaction from periph to memory. 1 - Destination is periph :transaction from Memory to periph
28	FIFOMODD	R/W	0h	Destination pointer fifo mode
27	FIFOMODS	R/W	0h	Source pointer fifo mode
26	DMASIGBPS	R/W	0h	Tie high channel DMA req signal. This is useful for memory to memort transaction
25-22	RESERVED	R	0h	Reserved
21-16	BLKSIZE	R/W	0h	size of the block in words. If block mode is enabled, defines the address wrap around. Since channel arbitration decisions are made every block, this also effect how much bandwidth is given to a specific channel.
15-2	RESERVED	R	0h	Reserved
1-0	WORDSIZE	R/W	0h	00 -word size is 32 bits 01 -word size is 16 bits 10 -word size is 8 bits

11.4.46 CH6STA Register (Offset = 7000h) [Reset = 00000000h]

CH6STA is shown in Table 11-48.

Return to the Summary Table.

Channel Status FSM state and run indication.

Table 11-48. CH6STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	RUN	R	0h	Indication that channel is currently transfering data and is not idle. Channels that are waiting on arbitration are considered running.
15-12	RESERVED	R	0h	Reserved
11-8	FSMSTATE	R	0h	FSM state: 0x0. IDLE 0x2. EXCEPTION 0x3. DRAIN 0x4. ABORT 0x8. PENDING ARB 0x9. COPY 0xA. COPY LAST 0xC. DONE 0xD. SAVE CTX 0xE. WAIT NEXT TRANS 0xF. LAST
7-3	RESERVED	R	0h	Reserved
2-0	HWEVENT	R	0h	HW event status. Channel status is a bit mask. Multiple bits can be set at the same time 0. PROCESSING 1. TRANS DONE 2. ABORT 4. EXCEPTION

11.4.47 CH6TIPTR Register (Offset = 7004h) [Reset = 00000000h]

CH6TIPTR is shown in Table 11-49.

Return to the Summary Table.

32 bit address pointer of channel current input.

Table 11-49. CH6TIPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IPTR	R/W	0h	32 bit address pointer of channel current input.

11.4.48 CH6TOPTR Register (Offset = 7008h) [Reset = 00000000h]

CH6TOPTR is shown in Table 11-50.

Return to the Summary Table.

32 bit address pointer of channel current output.

Table 11-50. CH6TOPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	OPTR	R/W	0h	32 bit address pointer of channel current output.

11.4.49 CH6TCTL Register (Offset = 700Ch) [Reset = 00000000h]

CH6TCTL is shown in Table 11-51.

Return to the Summary Table.

Transaction control

Table 11-51. CH6TCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-24	ENDIANESS	R/W	0h	0 -no endianess, 1 - byte endianess, 2 - bit endianess
23-18	RESERVED	R	0h	Reserved
17	SPARE	R/W	0h	spare
16	BURSTREQ	R/W	0h	In case number of words to tranfer smaller than block size, DMA would use signle request and work with block size of 1 word. In case we know request would be set on altough number of words to tranfer is smaller than block size, we can set this field on and DMA will wait for block_request and transact all remaining words in one block.
15-14	RESERVED	R	0h	Reserved
13-0	TRANSB	R/W	0h	Number of bytes of the transaction to move from source to destination.

11.4.50 CH6TCTL2 Register (Offset = 7010h) [Reset = 00000000h]

CH6TCTL2 is shown in Table 11-52.

Return to the Summary Table.

DMA command interface

Table 11-52. CH6TCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CMD	W	0h	1 - run command. Start a transaction. 2- abort command - stop reansaction. 4- init command - init new transaction afet abort/error.

11.4.51 CH6TSTA Register (Offset = 7014h) [Reset = 00000000h]

CH6TSTA is shown in Table 11-53.

Return to the Summary Table.

Job completion reason - either last transaction or exception

Table 11-53. CH6TSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	REMAINB	R	0h	Number of bytes remaining to complete the transaction.
15-8	WORDOFFSET	R	0h	Offset in words from block boundary. Actually number of word have been transferred in this block
7-1	RESERVED	R	0h	Reserved
0	STA	R	0h	channel OCP rstatus recieved at one of the primary ports. Once an error is encountered the channel will enter an Exception state and stay the until an init command is recieved. ICLR does not affect this status.

11.4.52 CH6JCTL Register (Offset = 701Ch) [Reset = 00000000h]

CH6JCTL is shown in Table 11-54.

Return to the Summary Table.

Job control register

Table 11-54. CH6JCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	ENCLR	R/W	0h	Enable DMA to set a rd/wr clear pulse at the beginning of a job (one cycle after run cmd)
29	SRCDSTCFG	R/W	0h	0 - Sorce is periph: transaction from periph to memory. 1 - Destination is periph :transaction from Memory to periph
28	FIFOMODD	R/W	0h	Destination pointer fifo mode
27	FIFOMODS	R/W	0h	Source pointer fifo mode
26	DMASIGBPS	R/W	0h	Tie high channel DMA req signal. This is useful for memory to memort transaction
25-22	RESERVED	R	0h	Reserved
21-16	BLKSIZE	R/W	0h	size of the block in words. If block mode is enabled, defines the address wrap around. Since channel arbitration decisions are made every block, this also effect how much bandwidth is given to a specific channel.
15-2	RESERVED	R	0h	Reserved
1-0	WORDSIZE	R/W	0h	00 -word size is 32 bits 01 -word size is 16 bits 10 -word size is 8 bits

11.4.53 CH7STA Register (Offset = 8000h) [Reset = 00000000h]

CH7STA is shown in Table 11-55.

Return to the Summary Table.

Channel Status FSM state and run indication.

Table 11-55. CH7STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	RUN	R	0h	Indication that channel is currently transfering data and is not idle. Channels that are waiting on arbitration are considered running.
15-12	RESERVED	R	0h	Reserved
11-8	FSMSTATE	R	0h	FSM state: 0x0. IDLE 0x2. EXCEPTION 0x3. DRAIN 0x4. ABORT 0x8. PENDING ARB 0x9. COPY 0xA. COPY LAST 0xC. DONE 0xD. SAVE CTX 0xE. WAIT NEXT TRANS 0xF. LAST
7-3	RESERVED	R	0h	Reserved
2-0	HWEVENT	R	0h	HW event status. Channel status is a bit mask. Multiple bits can be set at the same time 0. PROCESSING 1. TRANS DONE 2. ABORT 4. EXCEPTION

11.4.54 CH7TIPTR Register (Offset = 8004h) [Reset = 00000000h]

CH7TIPTR is shown in Table 11-56.

Return to the Summary Table.

32 bit address pointer of channel current input.

Table 11-56. CH7TIPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IPTR	R/W	0h	32 bit address pointer of channel current input.

11.4.55 CH7TOPTR Register (Offset = 8008h) [Reset = 00000000h]

CH7TOPTR is shown in Table 11-57.

Return to the Summary Table.

32 bit address pointer of channel current output.

Table 11-57. CH7TOPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	OPTR	R/W	0h	32 bit address pointer of channel current output.

11.4.56 CH7TCTL Register (Offset = 800Ch) [Reset = 00000000h]

CH7TCTL is shown in Table 11-58.

Return to the Summary Table.

Transaction control

Table 11-58. CH7TCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-24	ENDIANESS	R/W	0h	0 -no endianess, 1 - byte endianess, 2 - bit endianess
23-18	RESERVED	R	0h	Reserved
17	SPARE	R/W	0h	spare
16	BURSTREQ	R/W	0h	In case number of words to tranfer smaller than block size, DMA would use signle request and work with block size of 1 word. In case we know request would be set on altough number of words to tranfer is smaller than block size, we can set this field on and DMA will wait for block_request and transact all remaining words in one block.
15-14	RESERVED	R	0h	Reserved
13-0	TRANSB	R/W	0h	Number of bytes of the transaction to move from source to destination.

11.4.57 CH7TCTL2 Register (Offset = 8010h) [Reset = 00000000h]

CH7TCTL2 is shown in Table 11-59.

Return to the Summary Table.

DMA command interface

Table 11-59. CH7TCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CMD	W	0h	1 - run command. Start a transaction. 2- abort command - stop reansaction. 4- init command - init new transaction afet abort/error.

11.4.58 CH7TSTA Register (Offset = 8014h) [Reset = 00000000h]

CH7TSTA is shown in Table 11-60.

Return to the Summary Table.

Job completion reason - either last transaction or exception

Table 11-60. CH7TSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	REMAINB	R	0h	Number of bytes remaining to complete the transaction.
15-8	OFFSET	R	0h	Offset in words from block boundary. Actually number of word have been transferred in this block
7-1	RESERVED	R	0h	Reserved
0	STA	R	0h	channel OCP rstatus recieved at one of the primary ports. Once an error is encountered the channel will enter an Exception state and stay the until an init command is recieved. ICLR does not affect this status.

11.4.59 CH7JCTL Register (Offset = 801Ch) [Reset = 00000000h]

CH7JCTL is shown in Table 11-61.

Return to the Summary Table.

Job control register

Table 11-61. CH7JCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	ENCLR	R/W	0h	Enable DMA to set a rd/wr clear pulse at the beginning of a job (one cycle after run cmd)
29	SRCDSTCFG	R/W	0h	0 - Sorce is periph: transaction from periph to memory. 1 - Destination is periph :transaction from Memory to periph
28	FIFOMODD	R/W	0h	Destination pointer fifo mode
27	FIFOMODS	R/W	0h	Source pointer fifo mode
26	DMASIGBPS	R/W	0h	Tie high channel DMA req signal. This is useful for memory to memort transaction
25-22	RESERVED	R	0h	Reserved
21-16	BLKSIZE	R/W	0h	size of the block in words. If block mode is enabled, defines the address wrap around. Since channel arbitration decisions are made every block, this also effect how much bandwidth is given to a specific channel.
15-2	RESERVED	R	0h	Reserved
1-0	WORDSIZE	R/W	0h	00 -word size is 32 bits 01 -word size is 16 bits 10 -word size is 8 bits

11.4.60 CH8STA Register (Offset = 9000h) [Reset = 00000000h]

CH8STA is shown in Table 11-62.

Return to the Summary Table.

Channel Status FSM state and run indication.

Table 11-62. CH8STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	RUN	R	0h	Indication that channel is currently transfering data and is not idle. Channels that are waiting on arbitration are considered running.
15-12	RESERVED	R	0h	Reserved
11-8	FSMSTATE	R	0h	FSM state: 0x0. IDLE 0x2. EXCEPTION 0x3. DRAIN 0x4. ABORT 0x8. PENDING ARB 0x9. COPY 0xA. COPY LAST 0xC. DONE 0xD. SAVE CTX 0xE. WAIT NEXT TRANS 0xF. LAST
7-3	RESERVED	R	0h	Reserved
2-0	HWEVENT	R	0h	HW event status. Channel status is a bit mask. Multiple bits can be set at the same time 0. PROCESSING 1. TRANS DONE 2. ABORT 4. EXCEPTION

11.4.61 CH8TIPTR Register (Offset = 9004h) [Reset = 00000000h]

CH8TIPTR is shown in Table 11-63.

Return to the Summary Table.

32 bit address pointer of channel current input.

Table 11-63. CH8TIPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IPTR	R/W	0h	32 bit address pointer of channel current input.

11.4.62 CH8TOPTR Register (Offset = 9008h) [Reset = 00000000h]

CH8TOPTR is shown in Table 11-64.

Return to the Summary Table.

32 bit address pointer of channel current output.

Table 11-64. CH8TOPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	OPTR	R/W	0h	32 bit address pointer of channel current output.

11.4.63 CH8TCTL Register (Offset = 900Ch) [Reset = 00000000h]

CH8TCTL is shown in Table 11-65.

Return to the Summary Table.

Transaction control

Table 11-65. CH8TCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-24	ENDIANESS	R/W	0h	0 -no endianess, 1 - byte endianess, 2 - bit endianess
23-18	RESERVED	R	0h	Reserved
17	SPARE	R/W	0h	spare
16	BURSTREQ	R/W	0h	In case number of words to tranfer smaller than block size, DMA would use signle request and work with block size of 1 word. In case we know request would be set on altough number of words to tranfer is smaller than block size, we can set this field on and DMA will wait for block_request and transact all remaining words in one block.
15-14	RESERVED	R	0h	Reserved
13-0	TRANSB	R/W	0h	Number of bytes of the transaction to move from source to destination.

11.4.64 CH8TCTL2 Register (Offset = 9010h) [Reset = 00000000h]

CH8TCTL2 is shown in Table 11-66.

Return to the Summary Table.

DMA command interface

Table 11-66. CH8TCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CMD	W	0h	1 - run command. Start a transaction. 2- abort command - stop reansaction. 4- init command - init new transaction afet abort/error.

11.4.65 CH8TSTA Register (Offset = 9014h) [Reset = 00000000h]

CH8TSTA is shown in Table 11-67.

Return to the Summary Table.

Job completion reason - either last transaction or exception

Table 11-67. CH8TSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	REMAINB	R	0h	Number of bytes remaining to complete the transaction.
15-8	OFFSET	R	0h	Offset in words from block boundary. Actually number of word have been transferred in this block
7-1	RESERVED	R	0h	Reserved
0	STA	R	0h	channel OCP rstatus recieved at one of the primary ports. Once an error is encountered the channel will enter an Exception state and stay the until an init command is recieved. ICLR does not affect this status.

11.4.66 CH8JCTL Register (Offset = 901Ch) [Reset = 00000000h]

CH8JCTL is shown in Table 11-68.

Return to the Summary Table.

Job control register

Table 11-68. CH8JCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	ENCLR	R/W	0h	Enable DMA to set a rd/wr clear pulse at the beginning of a job (one cycle after run cmd)
29	SRCDSTCFG	R/W	0h	0 - Sorce is periph: transaction from periph to memory. 1 - Destination is periph :transaction from Memory to periph
28	FIFOMODD	R/W	0h	Destination pointer fifo mode
27	FIFOMODS	R/W	0h	Source pointer fifo mode
26	DMASIGBPS	R/W	0h	Tie high channel DMA req signal. This is useful for memory to memort transaction
25-22	RESERVED	R	0h	Reserved
21-16	BLKSIZE	R/W	0h	size of the block in words. If block mode is enabled, defines the address wrap around. Since channel arbitration decisions are made every block, this also effect how much bandwidth is given to a specific channel.
15-2	RESERVED	R	0h	Reserved
1-0	WORDSIZE	R/W	0h	00 -word size is 32 bits 01 -word size is 16 bits 10 -word size is 8 bits

11.4.67 CH9STA Register (Offset = A000h) [Reset = 00000000h]

CH9STA is shown in Table 11-69.

Return to the Summary Table.

Channel Status FSM state and run indication.

Table 11-69. CH9STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	RUN	R	0h	Indication that channel is currently transfering data and is not idle. Channels that are waiting on arbitration are considered running.
15-12	RESERVED	R	0h	Reserved
11-8	FSMSTATE	R	0h	FSM state: 0x0. IDLE 0x2. EXCEPTION 0x3. DRAIN 0x4. ABORT 0x8. PENDING ARB 0x9. COPY 0xA. COPY LAST 0xC. DONE 0xD. SAVE CTX 0xE. WAIT NEXT TRANS 0xF. LAST
7-3	RESERVED	R	0h	Reserved
2-0	HWEVENT	R	0h	HW event status. Channel status is a bit mask. Multiple bits can be set at the same time 0. PROCESSING 1. TRANS DONE 2. ABORT 4. EXCEPTION

11.4.68 CH9TIPTR Register (Offset = A004h) [Reset = 00000000h]

CH9TIPTR is shown in Table 11-70.

Return to the Summary Table.

32 bit address pointer of channel current input.

Table 11-70. CH9TIPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IPTR	R/W	0h	32 bit address pointer of channel current input.

11.4.69 CH9TOPTR Register (Offset = A008h) [Reset = 00000000h]

CH9TOPTR is shown in Table 11-71.

Return to the Summary Table.

32 bit address pointer of channel current output.

Table 11-71. CH9TOPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	OPTR	R/W	0h	32 bit address pointer of channel current output.

11.4.70 CH9TCTL Register (Offset = A00Ch) [Reset = 00000000h]

CH9TCTL is shown in Table 11-72.

Return to the Summary Table.

Transaction control

Table 11-72. CH9TCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-24	ENDIANESS	R/W	0h	0 -no endianess, 1 - byte endianess, 2 - bit endianess
23-18	RESERVED	R	0h	Reserved
17	SPARE	R/W	0h	spare
16	BURSTREQ	R/W	0h	In case number of words to tranfer smaller than block size, DMA would use signle request and work with block size of 1 word. In case we know request would be set on altough number of words to tranfer is smaller than block size, we can set this field on and DMA will wait for block_request and transact all remaining words in one block.
15-14	RESERVED	R	0h	Reserved
13-0	TRANSB	R/W	0h	Number of bytes of the transaction to move from source to destination.

11.4.71 CH9TCTL2 Register (Offset = A010h) [Reset = 00000000h]

CH9TCTL2 is shown in Table 11-73.

Return to the Summary Table.

DMA command interface

Table 11-73. CH9TCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CMD	W	0h	1 - run command. Start a transaction. 2- abort command - stop reansaction. 4- init command - init new transaction afet abort/error.

11.4.72 CH9TSTA Register (Offset = A014h) [Reset = 00000000h]

CH9TSTA is shown in Table 11-74.

Return to the Summary Table.

Job completion reason - either last transaction or exception

Table 11-74. CH9TSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	REMAINB	R	0h	Number of bytes remaining to complete the transaction.
15-8	OFFSET	R	0h	Offset in words from block boundary. Actually number of word have been transferred in this block
7-1	RESERVED	R	0h	Reserved
0	STA	R	0h	channel OCP rstatus recieved at one of the primary ports. Once an error is encountered the channel will enter an Exception state and stay the until an init command is recieved. ICLR does not affect this status.

11.4.73 CH9JCTL Register (Offset = A01Ch) [Reset = 00000000h]

CH9JCTL is shown in Table 11-75.

Return to the Summary Table.

Job control register

Table 11-75. CH9JCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	ENCLR	R/W	0h	Enable DMA to set a rd/wr clear pulse at the beginning of a job (one cycle after run cmd)
29	SRCDSTCFG	R/W	0h	0 - Sorce is periph: transaction from periph to memory. 1 - Destination is periph :transaction from Memory to periph
28	FIFOMODD	R/W	0h	Destination pointer fifo mode
27	FIFOMODS	R/W	0h	Source pointer fifo mode
26	DMASIGBPS	R/W	0h	Tie high channel DMA req signal. This is useful for memory to memort transaction
25-22	RESERVED	R	0h	Reserved
21-16	BLKSIZE	R/W	0h	size of the block in words. If block mode is enabled, defines the address wrap around. Since channel arbitration decisions are made every block, this also effect how much bandwidth is given to a specific channel.
15-2	RESERVED	R	0h	Reserved
1-0	WORDSIZE	R/W	0h	00 -word size is 32 bits 01 -word size is 16 bits 10 -word size is 8 bits

11.4.74 CH10STA Register (Offset = B000h) [Reset = 00000000h]

CH10STA is shown in Table 11-76.

Return to the Summary Table.

Channel Status FSM state and run indication.

Table 11-76. CH10STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	RUN	R	0h	Indication that channel is currently transfering data and is not idle. Channels that are waiting on arbitration are considered running.
15-12	RESERVED	R	0h	Reserved
11-8	FSMSTATE	R	0h	FSM state: 0x0. IDLE 0x2. EXCEPTION 0x3. DRAIN 0x4. ABORT 0x8. PENDING ARB 0x9. COPY 0xA. COPY LAST 0xC. DONE 0xD. SAVE CTX 0xE. WAIT NEXT TRANS 0xF. LAST
7-3	RESERVED	R	0h	Reserved
2-0	HWEVENT	R	0h	HW event status. Channel status is a bit mask. Multiple bits can be set at the same time 0. PROCESSING 1. TRANS DONE 2. ABORT 4. EXCEPTION

11.4.75 CH10TIPTR Register (Offset = B004h) [Reset = 00000000h]

CH10TIPTR is shown in Table 11-77.

Return to the Summary Table.

32 bit address pointer of channel current input.

Table 11-77. CH10TIPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IPTR	R/W	0h	32 bit address pointer of channel current input.

11.4.76 CH10TOPTR Register (Offset = B008h) [Reset = 00000000h]

CH10TOPTR is shown in Table 11-78.

Return to the Summary Table.

32 bit address pointer of channel current output.

Table 11-78. CH10TOPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	OPTR	R/W	0h	32 bit address pointer of channel current output.

11.4.77 CH10TCTL Register (Offset = B00Ch) [Reset = 00000000h]

CH10TCTL is shown in Table 11-79.

Return to the Summary Table.

Transaction control

Table 11-79. CH10TCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-24	ENDIANESS	R/W	0h	0 -no endianess, 1 - byte endianess, 2 - bit endianess
23-18	RESERVED	R	0h	Reserved
17	SPARE	R/W	0h	spare
16	BURSTREQ	R/W	0h	In case number of words to tranfer smaller than block size, DMA would use signle request and work with block size of 1 word. In case we know request would be set on altough number of words to tranfer is smaller than block size, we can set this field on and DMA will wait for block_request and transact all remaining words in one block.
15-14	RESERVED	R	0h	Reserved
13-0	TRANSB	R/W	0h	Number of bytes of the transaction to move from source to destination.

11.4.78 CH10TCTL2 Register (Offset = B010h) [Reset = 00000000h]

CH10TCTL2 is shown in Table 11-80.

Return to the Summary Table.

DMA command interface

Table 11-80. CH10TCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CMD	W	0h	1 - run command. Start a transaction. 2- abort command - stop reansaction. 4- init command - init new transaction afet abort/error.

11.4.79 CH10TSTA Register (Offset = B014h) [Reset = 00000000h]

CH10TSTA is shown in Table 11-81.

Return to the Summary Table.

Job completion reason - either last transaction or exception

Table 11-81. CH10TSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	REMAINB	R	0h	Number of bytes remaining to complete the transaction.
15-8	OFFSET	R	0h	Offset in words from block boundary. Actually number of word have been transferred in this block
7-1	RESERVED	R	0h	Reserved
0	STA	R	0h	channel OCP rstatus recieved at one of the primary ports. Once an error is encountered the channel will enter an Exception state and stay the until an init command is recieved. ICLR does not affect this status.

11.4.80 CH10JCTL Register (Offset = B01Ch) [Reset = 00000000h]

CH10JCTL is shown in Table 11-82.

Return to the Summary Table.

Job control register

Table 11-82. CH10JCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	ENCLR	R/W	0h	Enable DMA to set a rd/wr clear pulse at the beginning of a job (one cycle after run cmd)
29	SRCDSTCFG	R/W	0h	0 - Sorce is periph: transaction from periph to memory. 1 - Destination is periph :transaction from Memory to periph
28	FIFOMODD	R/W	0h	Destination pointer fifo mode
27	FIFOMODS	R/W	0h	Source pointer fifo mode
26	DMASIGBPS	R/W	0h	Tie high channel DMA req signal. This is useful for memory to memort transaction
25-24	RESERVED	R	0h	Reserved
23-16	BLKSIZE	R/W	0h	size of the block in words. If block mode is enabled, defines the address wrap around. Since channel arbitration decisions are made every block, this also effect how much bandwidth is given to a specific channel.
15-2	RESERVED	R	0h	Reserved
1-0	WORDSIZE	R/W	0h	00 -word size is 32 bits 01 -word size is 16 bits 10 -word size is 8 bits

11.4.81 CH11STA Register (Offset = C000h) [Reset = 00000000h]

CH11STA is shown in Table 11-83.

Return to the Summary Table.

Channel Status FSM state and run indication.

Table 11-83. CH11STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	RUN	R	0h	Indication that channel is currently transfering data and is not idle. Channels that are waiting on arbitration are considered running.
15-12	RESERVED	R	0h	Reserved
11-8	FSMSTATE	R	0h	FSM state: 0x0. IDLE 0x2. EXCEPTION 0x3. DRAIN 0x4. ABORT 0x8. PENDING ARB 0x9. COPY 0xA. COPY LAST 0xC. DONE 0xD. SAVE CTX 0xE. WAIT NEXT TRANS 0xF. LAST
7-3	RESERVED	R	0h	Reserved
2-0	HWEVENT	R	0h	HW event status. Channel status is a bit mask. Multiple bits can be set at the same time 0. PROCESSING 1. TRANS DONE 2. ABORT 4. EXCEPTION

11.4.82 CH11TIPTR Register (Offset = C004h) [Reset = 00000000h]

CH11TIPTR is shown in Table 11-84.

Return to the Summary Table.

32 bit address pointer of channel current input.

Table 11-84. CH11TIPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IPTR	R/W	0h	32 bit address pointer of channel current input.

11.4.83 CH11TOPTR Register (Offset = C008h) [Reset = 00000000h]

CH11TOPTR is shown in Table 11-85.

Return to the Summary Table.

32 bit address pointer of channel current output.

Table 11-85. CH11TOPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	OPTR	R/W	0h	32 bit address pointer of channel current output.

11.4.84 CH11TCTL Register (Offset = C00Ch) [Reset = 00000000h]

CH11TCTL is shown in Table 11-86.

Return to the Summary Table.

Transaction control

Table 11-86. CH11TCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-24	ENDIANESS	R/W	0h	0 -no endianess, 1 - byte endianess, 2 - bit endianess
23-18	RESERVED	R	0h	Reserved
17	SPARE	R/W	0h	spare
16	BURSTREQ	R/W	0h	In case number of words to tranfer smaller than block size, DMA would use signle request and work with block size of 1 word. In case we know request would be set on altough number of words to tranfer is smaller than block size, we can set this field on and DMA will wait for block_request and transact all remaining words in one block.
15-14	RESERVED	R	0h	Reserved
13-0	TRANSB	R/W	0h	Number of bytes of the transaction to move from source to destination.

11.4.85 CH11TCTL2 Register (Offset = C010h) [Reset = 00000000h]

CH11TCTL2 is shown in Table 11-87.

Return to the Summary Table.

DMA command interface

Table 11-87. CH11TCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CMD	W	0h	1 - run command. Start a transaction. 2- abort command - stop reansaction. 4- init command - init new transaction afet abort/error.

11.4.86 CH11TSTA Register (Offset = C014h) [Reset = 00000000h]

CH11TSTA is shown in Table 11-88.

Return to the Summary Table.

Job completion reason - either last transaction or exception

Table 11-88. CH11TSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	REMAINB	R	0h	Number of bytes remaining to complete the transaction.
15-8	OFFSET	R	0h	Offset in words from block boundary. Actually number of word have been transferred in this block
7-1	RESERVED	R	0h	Reserved
0	STA	R	0h	channel OCP rstatus recieved at one of the primary ports. Once an error is encountered the channel will enter an Exception state and stay the until an init command is recieved. ICLR does not affect this status.

11.4.87 CH11JCTL Register (Offset = C01Ch) [Reset = 00000000h]

CH11JCTL is shown in Table 11-89.

Return to the Summary Table.

Job control register

Table 11-89. CH11JCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	ENCLR	R/W	0h	Enable DMA to set a rd/wr clear pulse at the beginning of a job (one cycle after run cmd)
29	SRCDSTCFG	R/W	0h	0 - Sorce is periph: transaction from periph to memory. 1 - Destination is periph :transaction from Memory to periph
28	FIFOMODD	R/W	0h	Destination pointer fifo mode
27	FIFOMODS	R/W	0h	Source pointer fifo mode
26	DMASIGBPS	R/W	0h	Tie high channel DMA req signal. This is useful for memory to memort transaction
25-22	RESERVED	R	0h	Reserved
21-16	BLKSIZE	R/W	0h	size of the block in words. If block mode is enabled, defines the address wrap around. Since channel arbitration decisions are made every block, this also effect how much bandwidth is given to a specific channel.
15-2	RESERVED	R	0h	Reserved
1-0	WORDSIZE	R/W	0h	00 -word size is 32 bits 01 -word size is 16 bits 10 -word size is 8 bits

11.4.88 CH12STA Register (Offset = D000h) [Reset = 00000000h]

CH12STA is shown in Table 11-90.

Return to the Summary Table.

Channel Status FSM state and run indication.

Table 11-90. CH12STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	RUN	R	0h	Indication that channel is currently transfering data and is not idle. Channels that are waiting on arbitration are considered running.
15-12	RESERVED	R	0h	Reserved
11-8	FSMSTATE	R	0h	FSM state: 0x0. IDLE 0x2. EXCEPTION 0x3. DRAIN 0x4. ABORT 0x8. PENDING ARB 0x9. COPY 0xA. COPY LAST 0xC. DONE 0xD. SAVE CTX 0xE. WAIT NEXT TRANS 0xF. LAST
7-3	RESERVED	R	0h	Reserved
2-0	HWEVENT	R	0h	HW event status. Channel status is a bit mask. Multiple bits can be set at the same time 0. PROCESSING 1. TRANS DONE 2. ABORT 4. EXCEPTION

11.4.89 CH12TIPTR Register (Offset = D004h) [Reset = 00000000h]

CH12TIPTR is shown in Table 11-91.

Return to the Summary Table.

32 bit address pointer of channel current input.

Table 11-91. CH12TIPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IPTR	R/W	0h	32 bit address pointer of channel current input.

11.4.90 CH12TOPTR Register (Offset = D008h) [Reset = 00000000h]

CH12TOPTR is shown in Table 11-92.

Return to the Summary Table.

32 bit address pointer of channel current output.

Table 11-92. CH12TOPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	OPTR	R/W	0h	32 bit address pointer of channel current output.

11.4.91 CH12TCTL Register (Offset = D00Ch) [Reset = 00000000h]

CH12TCTL is shown in Table 11-93.

Return to the Summary Table.

Transaction control

Table 11-93. CH12TCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-24	ENDIANESS	R/W	0h	0 -no endianess, 1 - byte endianess, 2 - bit endianess
23-18	RESERVED	R	0h	Reserved
17	SPARE	R/W	0h	spare
16	BURSTREQ	R/W	0h	In case number of words to tranfer smaller than block size, DMA would use signle request and work with block size of 1 word. In case we know request would be set on altough number of words to tranfer is smaller than block size, we can set this field on and DMA will wait for block_request and transact all remaining words in one block.
15-14	RESERVED	R	0h	Reserved
13-0	TRANSB	R/W	0h	Number of bytes of the transaction to move from source to destination.

11.4.92 CH12TCTL2 Register (Offset = D010h) [Reset = 00000000h]

CH12TCTL2 is shown in Table 11-94.

Return to the Summary Table.

DMA command interface

Table 11-94. CH12TCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CMD	W	0h	1 - run command. Start a transaction. 2- abort command - stop reansaction. 4- init command - init new transaction afet abort/error.

11.4.93 CH12TSTA Register (Offset = D014h) [Reset = 00000000h]

CH12TSTA is shown in Table 11-95.

Return to the Summary Table.

Job completion reason - either last transaction or exception

Table 11-95. CH12TSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	REMAINB	R	0h	Number of bytes remaining to complete the transaction.
15-8	OFFSET	R	0h	Offset in words from block boundary. Actually number of word have been transferred in this block
7-1	RESERVED	R	0h	Reserved
0	STA	R	0h	channel OCP rstatus recieved at one of the primary ports. Once an error is encountered the channel will enter an Exception state and stay the until an init command is recieved. ICLR does not affect this status.

11.4.94 CH12JCTL Register (Offset = D01Ch) [Reset = 00000000h]

CH12JCTL is shown in Table 11-96.

Return to the Summary Table.

Job control register

Table 11-96. CH12JCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	ENCLR	R/W	0h	Enable DMA to set a rd/wr clear pulse at the beginning of a job (one cycle after run cmd)
29	SRCDSTCFG	R/W	0h	0 - Sorce is periph: transaction from periph to memory. 1 - Destination is periph :transaction from Memory to periph
28	FIFOMODD	R/W	0h	Destination pointer fifo mode
27	FIFOMODS	R/W	0h	Source pointer fifo mode
26	DMASIGBPS	R/W	0h	Tie high channel DMA req signal. This is useful for memory to memort transaction
25-22	RESERVED	R	0h	Reserved
21-16	BLKSIZE	R/W	0h	size of the block in words. If block mode is enabled, defines the address wrap around. Since channel arbitration decisions are made every block, this also effect how much bandwidth is given to a specific channel.
15-2	RESERVED	R	0h	Reserved
1-0	WORDSIZE	R/W	0h	00 -word size is 32 bits 01 -word size is 16 bits 10 -word size is 8 bits

11.4.95 CH13STA Register (Offset = E000h) [Reset = 00000000h]

CH13STA is shown in Table 11-97.

Return to the Summary Table.

Channel Status FSM state and run indication.

Table 11-97. CH13STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	RUN	R	0h	Indication that channel is currently transfering data and is not idle. Channels that are waiting on arbitration are considered running.
15-12	RESERVED	R	0h	Reserved
11-8	FSMSTATE	R	0h	FSM state: 0x0. IDLE 0x2. EXCEPTION 0x3. DRAIN 0x4. ABORT 0x8. PENDING ARB 0x9. COPY 0xA. COPY LAST 0xC. DONE 0xD. SAVE CTX 0xE. WAIT NEXT TRANS 0xF. LAST
7-3	RESERVED	R	0h	Reserved
2-0	HWEVENT	R	0h	HW event status. Channel status is a bit mask. Multiple bits can be set at the same time 0. PROCESSING 1. TRANS DONE 2. ABORT 4. EXCEPTION

11.4.96 CH13TIPTR Register (Offset = E004h) [Reset = 00000000h]

CH13TIPTR is shown in Table 11-98.

Return to the Summary Table.

32 bit address pointer of channel current input.

Table 11-98. CH13TIPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IPTR	R/W	0h	32 bit address pointer of channel current input.

11.4.97 CH13TOPTR Register (Offset = E008h) [Reset = 00000000h]

CH13TOPTR is shown in Table 11-99.

Return to the Summary Table.

32 bit address pointer of channel current output.

Table 11-99. CH13TOPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	OPTR	R/W	0h	32 bit address pointer of channel current output.

11.4.98 CH13TCTL Register (Offset = E00Ch) [Reset = 00000000h]

CH13TCTL is shown in Table 11-100.

Return to the Summary Table.

Transaction control

Table 11-100. CH13TCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-24	ENDIANESS	R/W	0h	0 -no endianess, 1 - byte endianess, 2 - bit endianess
23-18	RESERVED	R	0h	Reserved
17	SPARE	R/W	0h	spare
16	BURSTREQ	R/W	0h	In case number of words to tranfer smaller than block size, DMA would use signle request and work with block size of 1 word. In case we know request would be set on altough number of words to tranfer is smaller than block size, we can set this field on and DMA will wait for block_request and transact all remaining words in one block.
15-14	RESERVED	R	0h	Reserved
13-0	TRANSB	R/W	0h	Number of bytes of the transaction to move from source to destination.

11.4.99 CH13TCTL2 Register (Offset = E010h) [Reset = 00000000h]

CH13TCTL2 is shown in Table 11-101.

Return to the Summary Table.

DMA command interface

Table 11-101. CH13TCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CMD	W	0h	1 - run command. Start a transaction. 2- abort command - stop reansaction. 4- init command - init new transaction afet abort/error.

11.4.100 CH13TSTA Register (Offset = E014h) [Reset = 00000000h]

CH13TSTA is shown in Table 11-102.

Return to the Summary Table.

Job completion reason - either last transaction or exception

Table 11-102. CH13TSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	REMAINB	R	0h	Number of bytes remaining to complete the transaction.
15-8	OFFSET	R	0h	Offset in words from block boundary. Actually number of word have been transferred in this block
7-1	RESERVED	R	0h	Reserved
0	STA	R	0h	channel OCP rstatus recieved at one of the primary ports. Once an error is encountered the channel will enter an Exception state and stay the until an init command is recieved. ICLR does not affect this status.

11.4.101 CH13JCTL Register (Offset = E01Ch) [Reset = 00000000h]

CH13JCTL is shown in Table 11-103.

Return to the Summary Table.

Job control register

Table 11-103. CH13JCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	ENCLR	R/W	0h	Enable DMA to set a rd/wr clear pulse at the beginning of a job (one cycle after run cmd)
29	SRCDSTCFG	R/W	0h	0 - Sorce is periph: transaction from periph to memory. 1 - Destination is periph :transaction from Memory to periph
28	FIFOMODD	R/W	0h	Destination pointer fifo mode
27	FIFOMODS	R/W	0h	Source pointer fifo mode
26	DMASIGBPS	R/W	0h	Tie high channel DMA req signal. This is useful for memory to memort transaction
25-22	RESERVED	R	0h	Reserved
21-16	BLKSIZE	R/W	0h	size of the block in words. If block mode is enabled, defines the address wrap around. Since channel arbitration decisions are made every block, this also effect how much bandwidth is given to a specific channel.
15-2	RESERVED	R	0h	Reserved
1-0	WORDSIZE	R/W	0h	00 -word size is 32 bits 01 -word size is 16 bits 10 -word size is 8 bits

Chapter 12

One Time Programming (OTP)

The CC35xx device includes 3136 fuse bits, 1056 bits for one-time-programming (OTP) which are available for customer use. The programming of OTP data is handled by TI secure bootloader in a secure manner, customer programming requests are authenticated using customer root-of-trust (ROT) Key. For more information on activation please see Chapter 10.

Vendor OTP programming can be done on customer production line only including initial rollback protection versions. In addition the next rollback version protection can still be updated in field.

The following features are supported by the OTP:

- WiFi 6 disable
- MAC address override
- Vendor ROT (256 bits) - hash of vendor public key used for authenticating images and requests by the vendor
- APPLICATION OTP (256 bits) - Can be used for application data
- Authentication bypass disable - default is enabled to support development for vendor R&D
- Anti-Rollback protection bits - anti rollback protection bits for each of the device components (Rollback bits are reserved exclusively for security fixes).
  - TI:
    - Connectivity FW
    - Bootloader/Programmer FW
  - Vendor application FW

Note

To improve security the OTP bits become write protected once they've been programmed - excluding the rollback bits.

Chapter 13

General Purpose Timers (GPT)

This section describes the General Purpose Timer (GPT) module and provides example use case scenarios.

13.1 Overview

The General Purpose Timer (GPT) is used to count or time external or internal events, generate Pulse-Width Modulation (PWM) signals, and generate IR modulated codes. There are two general purpose timers available, each with 4 channels. See the device specific data sheet for available timers and features.

Features

- General timing features, capture and compare
  - 4 Capture/Compare channels per timer
  - 32-bit counter width
- 8-bit prescaler
  - Configurable counter rate
  - Count from external event
- Different counter modes
  - Count up once
  - Count up repeatedly
  - Count up and down repeatedly
  - Start counting on configurable event
  - Quadrature decoding (QDEC)
- 15 different channel Capture/Compare actions
  - Period and pulse width measurement
  - 2 capture actions
  - 8 compare actions
- Filtering on capture inputs
- Generate PWM
  - Complementary PWM outputs
  - Programmable dead-band insertion
  - Park Mode on fault, sets the GPIO to a predetermined state upon fault
- IR signal generation
- Generate interrupts, DMA requests and ADC triggers
- Possible to chain the timers together and synchronize them.

13.2 Block Diagram

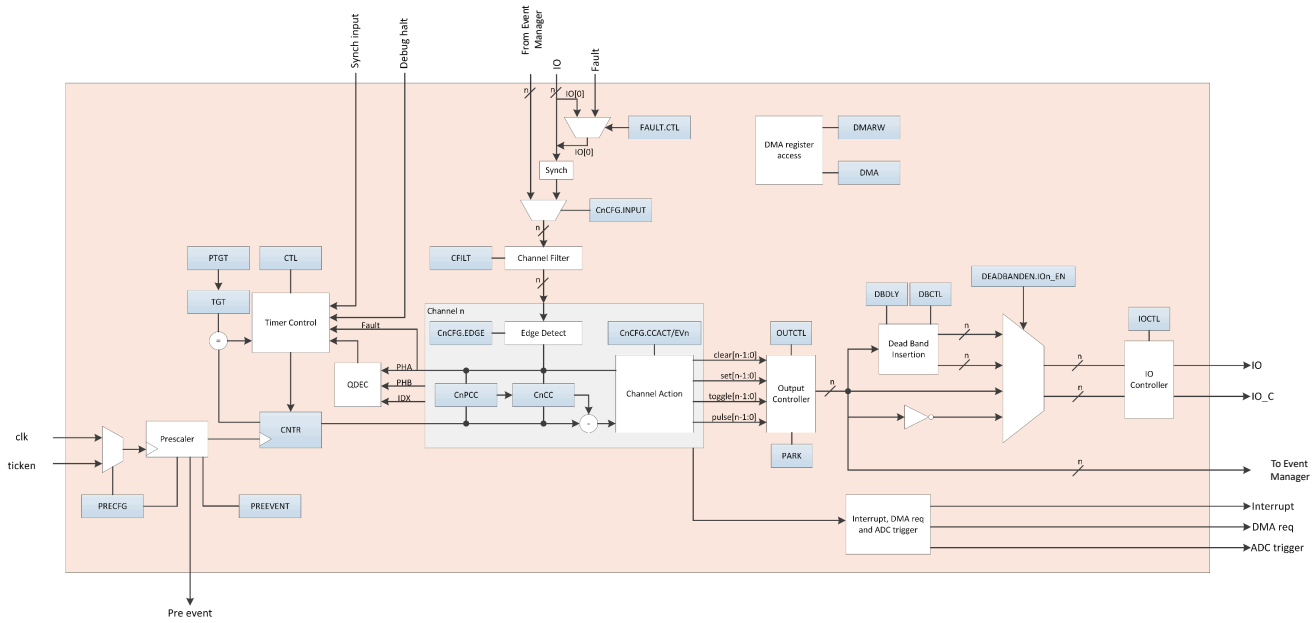

Figure 13-1. Single Timer Block Diagram

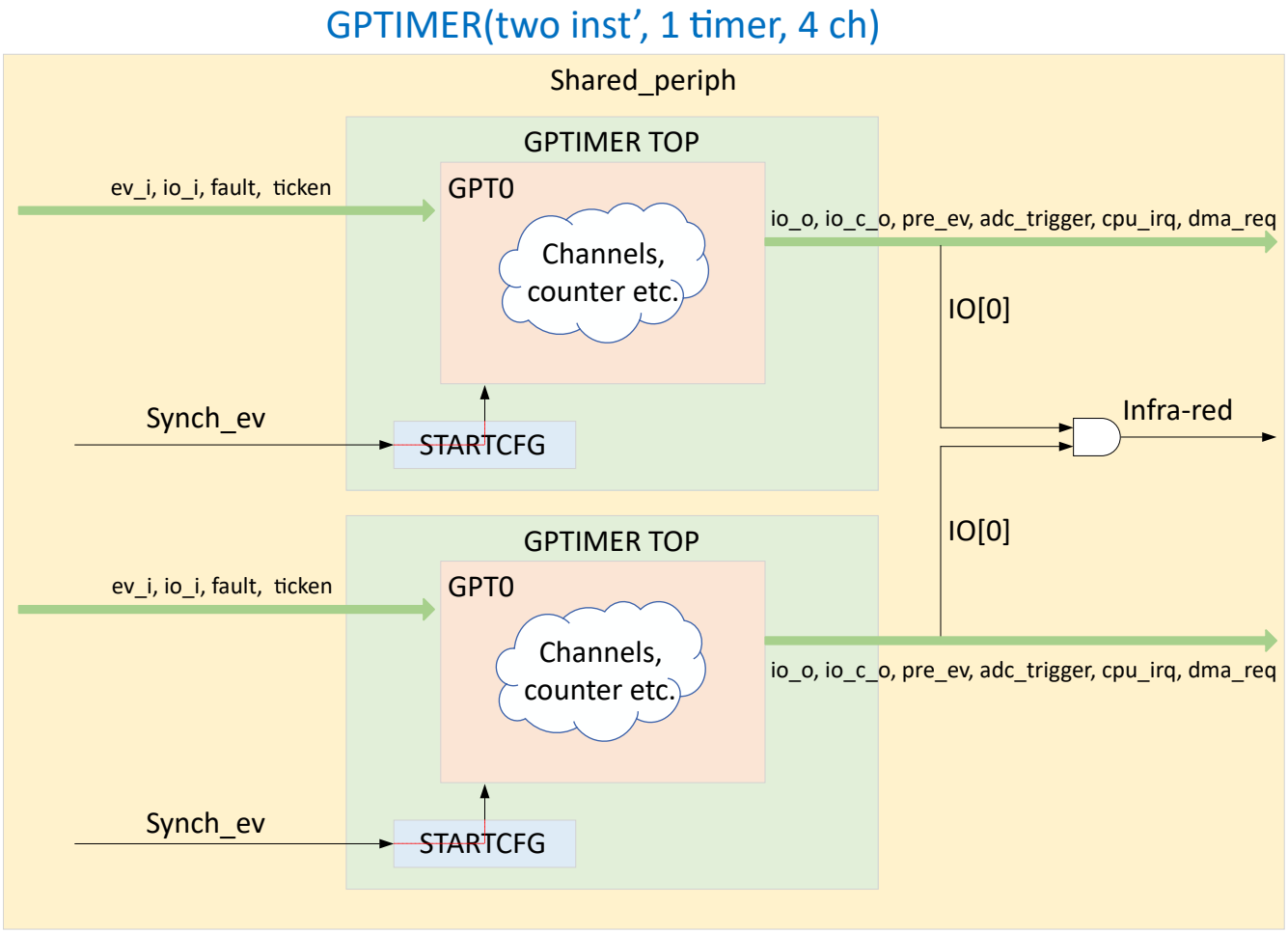

Figure 13-2. Multiple Timer Block Diagram

13.3 Functional Description

13.3.1 Prescaler

The prescaler is an 8-bit counter which counts down from the value PRECFG.TICKDIV to zero repeatedly. The rate of the down count is referred to as the prescaler clock. When the prescaler counter reaches zero, CNTR is updated. The rate of the CNTR update is referred to as the timer clock.

The prescaler can optionally run on the system clock (80MHz) or the TICKEN signal from the Event Manager. This can be configured in the PRECFG.TICKSRC register field.

If the prescaler clock is configured to be the TICKEN event signal from the Event Manager, the source of the event must be subscribed by the GPTxEVTCTL1.TICKEN register.

The timer clock and prescaler clock determine the following:

- **Prescaler clock**
  - Timer clock
  - Prescaler event output update
  - Sampling of channel filter (optionally)
- **Timer clock**
  - CNTR rate
  - Channels update event outputs on this clock
  - Sampling of channel filter (optionally)

– QDEC sampling

13.3.2 Counter

The value written to CTL.MODE[0:2] determines the counter mode as follows:

- UP_ONCE: The timer counts from 0 to the selected target. The timer then becomes disabled.
- UP_PER: The timer counts from 0 to the selected target, repeatedly.
- UPDWN_PER: The timer counts from 0 to the selected target and decrements back to 0, repeatedly.
- QDEC: The timer functions as a quadrature decoder. IOC input 0, IOC input 1 and IOC input 2 are used respectively as PHA, PHB and IDX inputs. IDX can be turned off by setting C2CFG.EDGE = NONE.
- SYNC_UP_ONCE: Same as UP_ONCE but the timer synchronizes to another timer.
- SYNC_UP_PER: Same as UP_PER but the timer synchronizes to another timer.
- SYNC_UPDWN_PER: Same as SYNC_UPDWN_PER but the timer synchronizes to another timer.

Note

While the counter can be written, the intent is only to support the setting of an initial position in QDEC mode. The ability to write the counter in other modes while the timer is running is possible, but the resulting behavior is unpredictable.

13.3.3 Target

The Target TGT register sets the target value for the counter.

The Pipline Target PTGT register, if written to, is loaded into TGT on counter zero crossing.

The QDEC mode and the SYNC modes are further described in Section 13.4.1 and Section 13.3.9.

13.3.4 Channel Input Logic

Every channel has an input which is used when the channel is configured in a capture action. The channel input can come from different sources, can be filtered and goes through an edge detection logic before triggering the channel capture. See Figure 13-3detailing the input logic.

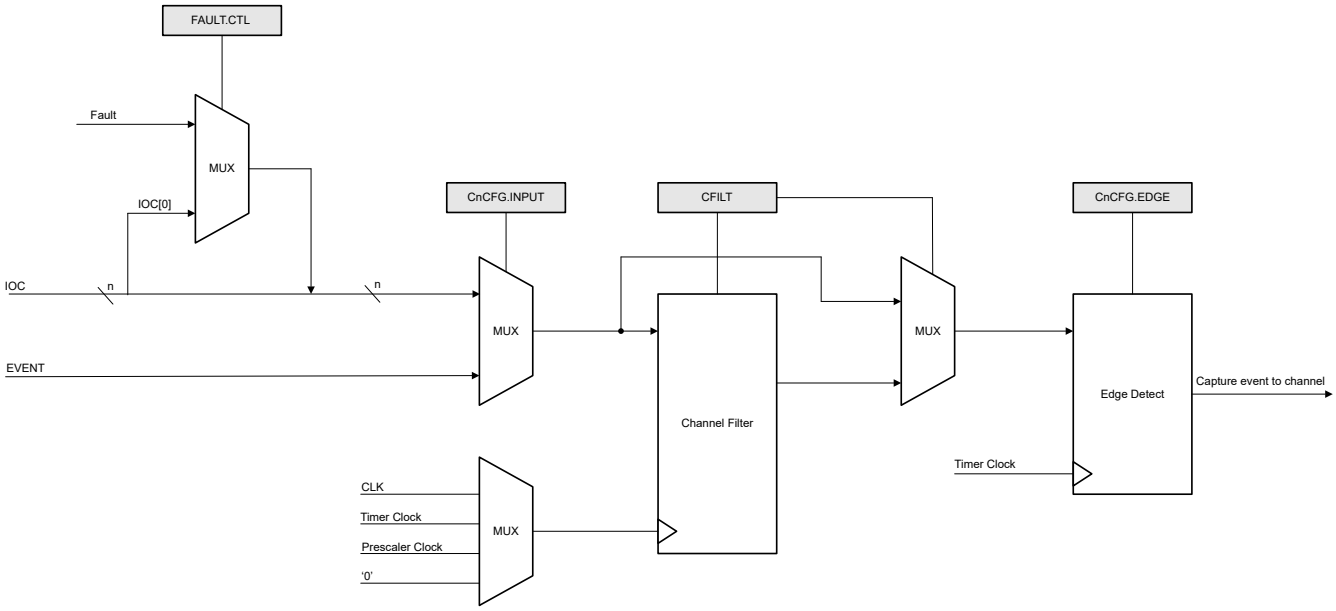

Figure 13-3. Channel Input Logic

If the FAULT register is present then enabling the FAULT logic uses channel 0 as fault input. The CnCFG.INPUT field configures if the input comes from the IOC or Event logic. The channel filter can be configured to require up to CHFILT.LOAD +1 consecutive input samples before the input is propagated to the edge detection logic. This

can typically be used to avoid capturing on glitches. After the channel filter the input goes into the edge detection logic. This is configured in the CnCFG.EDGE field.

The different components of the capture data path are clocked as follow:

- The channel filter, if used, is either clocked at the system clock, timer clock or the prescaler clock.
- The edge detect logic is always clocked at the timer clock.

13.3.5 Channel Output Logic

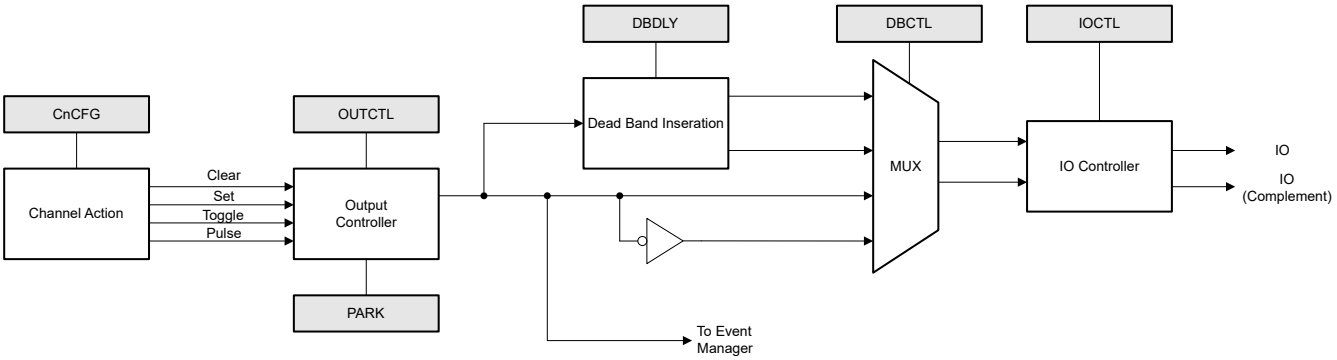

Figure 13-4. Channel Output Logic

Each GPTIMER has the same number of outputs as channels, but each channel does not control a dedicated output. Instead every channel can control every output. Which output each channel controls is configured in the CnCFG.OUTn fields.

The user can set and clear timer outputs manually by writing OUTCTL. Manual update of an output takes priority over automatic channel updates of the same output. Listed in decreasing order of priority, each output can:

1. Clear
2. Set
3. Toggle
4. Pulse (The output remains high for two counter clock periods, then goes low.)

An output can receive update requests from several channels at the same time. In this case, the output is updated according to the priority list. The output updated from an channel is decided by the channel action, CnCFG.CCACT.

13.3.6 Channel Actions

Each channel implements 15 different channel actions. Configured in CnCFG.CCACT, actions are categorized as one-shot and continuous:

- A one-shot channel action performs a function only once before the timer disables the channel.
- A continuous channel action performs a function until the user disables the channel.

Table 13-1 lists the 15 channel actions

Table 13-1. Channel Actions

GPT.CnCFG[3:0] CCACT bit field	Action	One-shot or Continuous
0	Disable channel	One-shot
1	Set on capture, and then disable channel	One-shot
2	Clear on zero, toggle on compare, and then disable channel	One-shot
3	Set on zero, toggle on compare, and then disable channel	One-shot
4	Clear on compare, and then disable channel	One-shot
5	Set on compare, and then disable channel	One-shot
6	Toggle on compare, and then disable channel	One-shot

Table 13-1. Channel Actions (continued)

GPT.CnCFG[3:0] CCACT bit field	Action	One-shot or Continuous
7	Pulse on compare, and then disable channel	One-shot
8	Period and pulse width measurement	Continuous
9	Set on capture repeatedly	Continuous
10	Clear on zero, toggle on compare repeatedly	Continuous
11	Set on zero, toggle on compare repeatedly	Continuous
12	Clear on compare repeatedly	Continuous
13	Set on compare repeatedly	Continuous
14	Toggle on compare repeatedly	Continuous
15	Pulse on compare repeatedly	Continuous

After configuration, the channel requests updates of enabled event outputs (set by CnCFG.OUT fields) according to the channel action description in the table above. There are three channel actions that require further description.

13.3.6.1 Period and Pulse Width Measurement

This channel action continuously captures period and pulse width of the channel's input signal relative to the signal edge given by CnCFG.EDGE. The channel requests to set enabled events when CnCC.VALUE contains signal period and PCnCC.VALUE contains signal pulse width. The channel function synchronizes the timer counter to the selected signal edge of the incoming signal. Hence:

- The counter restarts regularly, so other channel actions must be chosen with this in mind.
- The channels configured for this channel action cannot perform measurements simultaneously. The measurements are done in a time-interleaved manner.

Example: Two channels in Timer Period and Pulse Width Capture

The timer measures signal period and pulse width of two different signals A (From IO Mux or Event Manager) and B (From IO Mux or Event Manager). See Chapter 16 and Section 5.4 for more information on configuring the I/O Mux and Event Manager.

In this example, both signals have periods less than the counter range. Hence, time-out detection as described in the register documentation is not required. Configure as follows:

- Channel 0:
  - C0CFG. CCACT = PER_PULSE_WIDTH_MEAS
  - C0CFG. OUT0 = 1
  - C0CFG.INPUT = EVT/IO (Signal A)
  - C0CFG.EDGE = RISING
- Channel 1:
  - C1CFG. CCACT = PER_PULSE_WIDTH_MEAS
  - C1CFG. OUT1 = 1
  - C1CFG.INPUT = EVT/IO (Signal B)
  - C1CFG.EDGE = FALLING
- Timer: – CTL.MODE = UP_PER

Figure 13-5 shows how the timer counter first synchronizes to signal A. Channel 0 then captures the high phase of signal A into PC0CC at time t_0.The period of signal A is captured in C0CC at time t_1. At the same time, Channel 0 sets the event output 0 high, and the timer counter starts to synchronize to signal B. Channel 1 then captures the low phase of signal B into PC1CC at time t_2. Finally, the period of signal B is captured in C1CC at time t_3. At the same time, channel 1 sets the event output 1 high, and the timer counter starts to synchronize to signal A. The sequence then repeats itself until stopped by the user.

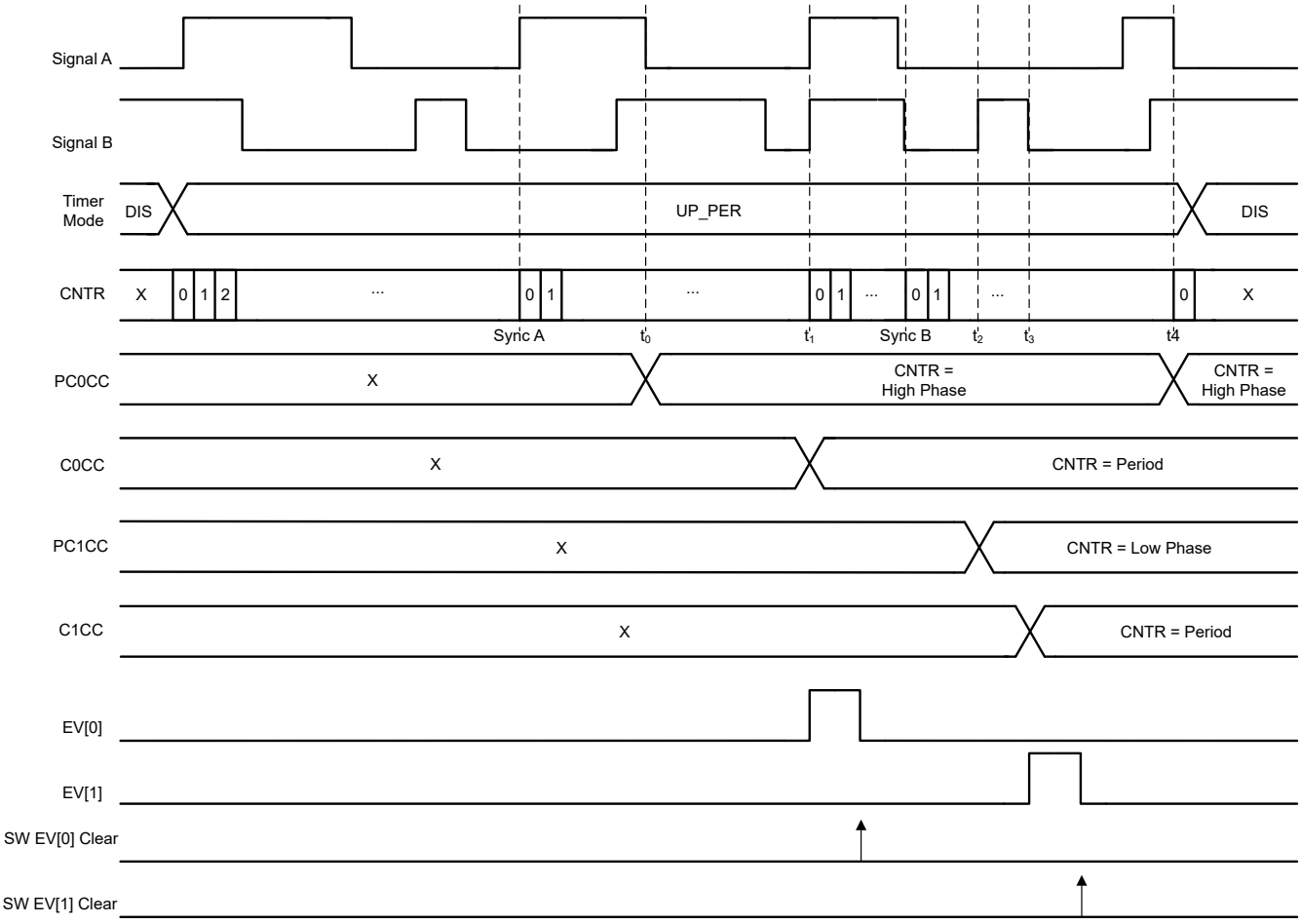

Figure 13-5. Period Pulse Width Measurement

13.3.6.2 Clear on Zero, Toggle on Compare Repeatedly

This channel action continuously:

- Clears the enabled output events when CNTR = 0
- Toggles the enabled output events when CNTR = CnCC

The channel generates center-aligned PWM waveform when CTL.MODE = UPDWN_PER. The channel copies a new value written in PCnCC to CnCC when CNTR becomes 0. This action prevents jitter on the edges of the generated PWM signal. Similarly, the timer copies a new value written in PTGT to TGT when CNTR becomes 0. This action avoids period-jitter in PWM applications with time-varying periods.

Example: Center-Aligned PWM Generation by Channel 0

This example illustrates center-aligned PWM generation by channel 0. The waveform is synthesized on output 0. The timer period is kept static, and the target value is set to half the period. Configure as follows:

- Channel 0:
  - C0CFG.CCACT = CLR_ON_0_TGL_ON_CMP
  - C0CFG.OUT0 = 1
  - C0CC = C0
- Timer:
  - TARGET = PERIOD / 2
  - CTL.MODE = UPDWN_PER

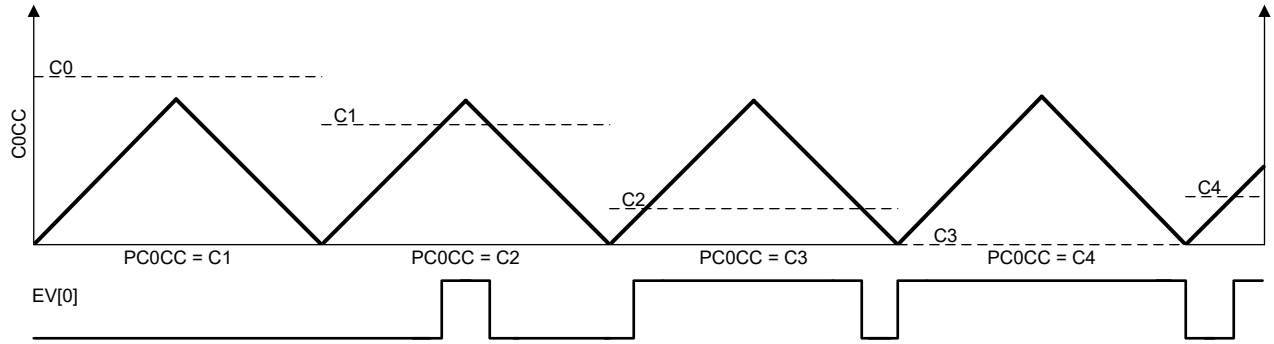

Figure 13-6. Center-Aligned PWM

The duty-cycle of the generated PWM waveform is controlled by PC0CC updates. Waveform generation on event output 0 continues until aborted by the user.

If the user wants to stop/pause the PWM generation in a controlled manner, the following procedure is recommended:

- Set FAULT.CTL = ZEROCOND
- Then set ISET.FAULT. The counter then halts at CNTR = 0.
- Counter can then either be started again by clearing RIS.FAULT, or turned completely off by setting CTL.MODE = DIS.

13.3.6.3 Set on Zero, Toggle on Compare Repeatedly

This channel action continuously does the following:

- Sets the enabled output events when CNTR = 0.
- Toggles the enabled output events when CNTR = CnCC

The channel generates an edge-aligned PWM waveform when CTL.MODE = UP_PER. The channel copies a new value written in PCnCC to CnCC when CNTR becomes 0. This prevents jitter on the edges of the generated PWM signal. Similarly, the timer copies a new value written in PTGT to TGT when CNTR becomes 0. This avoids period-jitter in PWM applications with time-varying period.

Example: Edge-Aligned PWM Generation by Channel 0

This example illustrates edge-aligned PWM generation by channel 0 (see below). The waveform is synthesized on event output 0. The timer period is kept static, and the target value is set to period minus 1. Configure as follows:

- Channel 0:
  - C0CFG.CCACT = SET_ON_0_TGL_ON_CMP
  - C0CFG. OUT0 = 1
  - C0CC = C0
- Timer:
  - TGT = PERIOD - 1
  - CTL.MODE = UP_PER

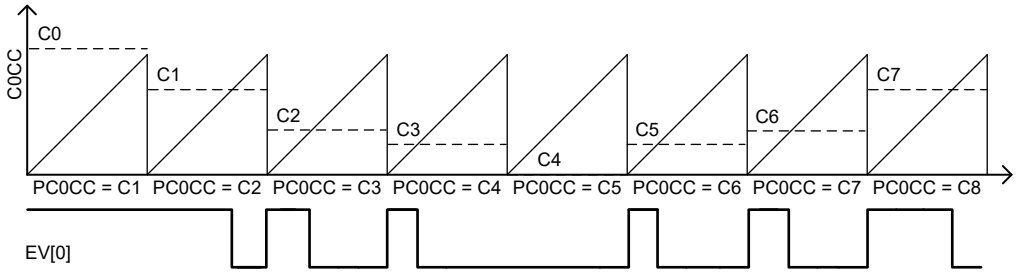

Figure 13-7. Edge-Aligned PWM

The duty-cycle of the generated PWM waveform is controlled by PC0CC updates. Waveform generation on event output 0 continues until aborted by the user.

13.3.7 Channel Capture Configuration

The channel's capture source can be set by the GPT.CnCFG[6] INPUT bit field. Here the bit field INPUT sets either the synchronous event from event manager, or the asynchronous IO Mux inputs as capture source. See Chapter 16 and Section 5.4 for more information on configuring the I/O Mux and Event Manager.

13.3.8 Channel Filters

The channel filter sets a window within which the input must remain stable, otherwise the transition is not passed to the edge detection logic.

The channel filter counts down from CHFILT.LOAD[15:8] while two consecutive input samples are equal. If two consecutive input samples are unequal the filter counter is re-loaded with LOAD. If the channel filter reaches zero the input is passed to the edge detection logic. The filter delays the input signal by at least LOAD + 1 filter clock cycles.

When writing CTL.MODE to any other value than disabled (0x0) the internal channel filter counter is loaded with the LOAD value. Do not change the CHFILT register while the timer is running and CTL.MODE[2:0] is not disabled (0x0).

13.3.8.1 Setting up the Channel Filters

To setup the channel filters in GPT follow these steps:

- Set the channel filter sample period by setting CHFILT.MODE:
  - CHFILT.MODE = BYPASS: No filter is used
  - CHFILT.MODE = CLK: 80MHz sample rate (Peripherals clock)
  - CHFILT.MODE = TICKCLK: Sample same as PRECFG.TICKSRC
  - CHFILT.MODE = TIMERCLK: Samples rate is same as counter rate
- Set CHFILT.LOAD value
- Start GPT

When configuring the channel filter make sure the channel filter period is not shorter than the timer clock period. That is,

(Channel filter clock period) x (CHFILT.LOAD) > timer clock period.

If this is not satisfied capture events can be missed.

13.3.9 Synchronize Multiple GPTimers

The GPTIMERs are configured in the following manner to sync to GPT0:

- Configure GPTIMER1.CTL.MODE in one of the SYNC modes.

Table 13-2. Sync Modes

GPTIMERx.CTL[2:0] MODE bit field	SYNC MODE
0	Disable
1	Not Synchronous
2	Not Synchronous
3	Not Synchronous
4	Not Synchronous
5	Count Up Once - Synchronous to another GPT
6	Count Up Periodically - Synchronous to another GPT
7	Count Up and Down Periodically - Synchronous to another GPT

The event which triggers the GPTIMER should be defined in Event Manager with the GPTxEVTCTL1.SYNC register. Once the sync event arrives, the timer starts. If both timers are configured with the same sync event, both will begin counting at the same time.

13.3.10 Interrupts, ADC Trigger, and DMA Request

Each GPTIMER can generate an Interrupt request, ADC trigger and DMA request output event. These output events can be triggered on different internal GPTIMER events. The different internal events can be viewed in the RIS register.

If one or more of the fields in the IMASK register are set high, the timer sends out an interrupt event when the internal GPTIMER event corresponding to the fields set in IMASK occur.

These internal GPTIMER events can also set the ADC trigger or DMA request depending on the configuration of the ADCTRG.SRC and DMA.REQ field. That is, the ADC trigger and DMA request output events are generated when the corresponding interrupt is set in the RIS register.

Below are some important side effects regarding the Interrupts, ADC trigger and DMA request.

- Reading/writing to the CnCC or PCnCC register shall clear the corresponding channel interrupt.
- Reading/writing to NC (No Clear) registers does not have any side effects on interrupts.
- Reading/writing to PTGT or TGT clears both RIS.ZERO and RIS.TGT.
- The TGT interrupts are updated on the timer clock. These interrupts trigger at the same time as an CMP event.
- The ZERO and TGT interrupts trigger after one system clock cycle when CNTR = ZERO/TARGET.
- The field CTL.INTP gets set when the ZERO and TGT interrupts are set. This field decides if the interrupts are set on the beginning of the timer period or on the end of the timer period.
- The RIS.ZERO interrupt is not set when starting the timer.
- Note that if you have a short timer period, and you have configured the GPT to set the interrupt output on both ZERO and TGT, you can accidentally clear both ZERO and TGT when reading/writing to PTGT/TGT. This depends on the CPU's response time. If you want to make sure both the ZERO and TGT interrupts are received, use PTGTNC/TGTNC and clear the corresponding interrupt by writing to RIS.TGT.CLR and RIS.ZERO.CLR.
- If the Host DMA request is used in addition to the interrupt make sure that a write/read does not clear unhandled interrupt requests. As an example, if the Host DMA updates PTGT on ZERO interrupt and the CPU does some external handling on TGT interrupt, then if the timer period is short, the Host DMA write to PTGT can clear the unhandled TGT interrupt. This can be avoided by letting the Host DMA write to PTGTNC and letting the CPU clear both TGT and ZERO

13.4 Timer Modes

13.4.1 Quadrature Decoder

The Phase A (PHA), Phase B (PHB) and IDX signals are input events of channel 0, channel 1 and channel 2 respectively. PHA and PHB are required and IDX is optional. The signals are typically provided from an incremental encoder. An incremental encoder can provide two outputs which indicate a linear or a rotary motion. The output of the incremental encoder is typically a 90º shifted square wave and is provided as an input to the GPT. When enabled in QDEC mode, the GPT is used to decode the quadrature encoded data to provide information on the relative positioning and movement of a linear or rotary motion. The accumulation of the counter value in GPT with respect to PHA/PHB follows the following table:

Table 13-3. Counter Accumulation Based on QDEC Inputs

Previous Pin Event	Current Pin Event	Counter (+ or -)	Direction
PHA Falling	PHB Rising	-	Down
PHA Falling	PHB Falling	+	Up
PHA Falling	PHA Rising	+ if new dir is up, - if new dir is down	Toggle
PHA Rising	PHB Rising	+	Up
PHA Rising	PHB Falling	-	Down
PHA Rising	PHA Falling	+ if new dir is up, - if new dir is down	Toggle
PHB Falling	PHA Rising	+	Up
PHB Falling	PHA Falling	-	Down
PHB Falling	PHB Rising	+ if new dir is up, - if new dir is down	Toggle
PHB Rising	PHA Rising	-	Down
PHB Rising	PHA Falling	+	Up
PHB Rising	PHB Falling	+ if new dir is up, - if new dir is down	Toggle

To setup GPT in QDEC mode follow these steps:

- Configure where the input is from, IOC or event manager. Normally this is IOC:
  - PHA: C0CFG.INPUT = 1 (IOC)
  - PHB: C1CFG.INPUT = 1 (IOC)
- (Optional) IDX: C2CFG.INPUT = 1 (IOC)
- (Optional) If IDX is used set C2CFG.EDGE != 0.
- Set the sample rate. Use PRECFG.TICKDIV/TICKSRC to set the sample rate. The sample rate is:
  - TICKSRC = 0: 80 MHz / (PRECFG.TICKDIV + 1)
  - TICKSRC !=0: (ticken freq) / (PREVFG.TICKDIV + 1)
- Configure TGT and PTGT.
- (Optional) Enable channel filters. See Section 13.3.8
- (Optional) Enable QDEC interrupts:
  - (Optional) Set IMASK.DBLTRANS to get interrupt when a double transition occurs. This indicates that the sampling rate is too low.
  - (Optional) Set IMASK.CNTRCHNG to get interrupt when the counter changes. This indicates a movement of the measuring device.
  - (Optional) Set IMASK.DIRCHNG to get interrupt when the direction of the counter changes.
- (Optional) Configure PREEVENT if you want a high output signal just before the sampling, e.g. turn on a LED.
- Start timer in QDEC by writing CTL.MODE= QDEC_MODE.

Figure 13-8 shows the QDEC related signals with PREEVENT.

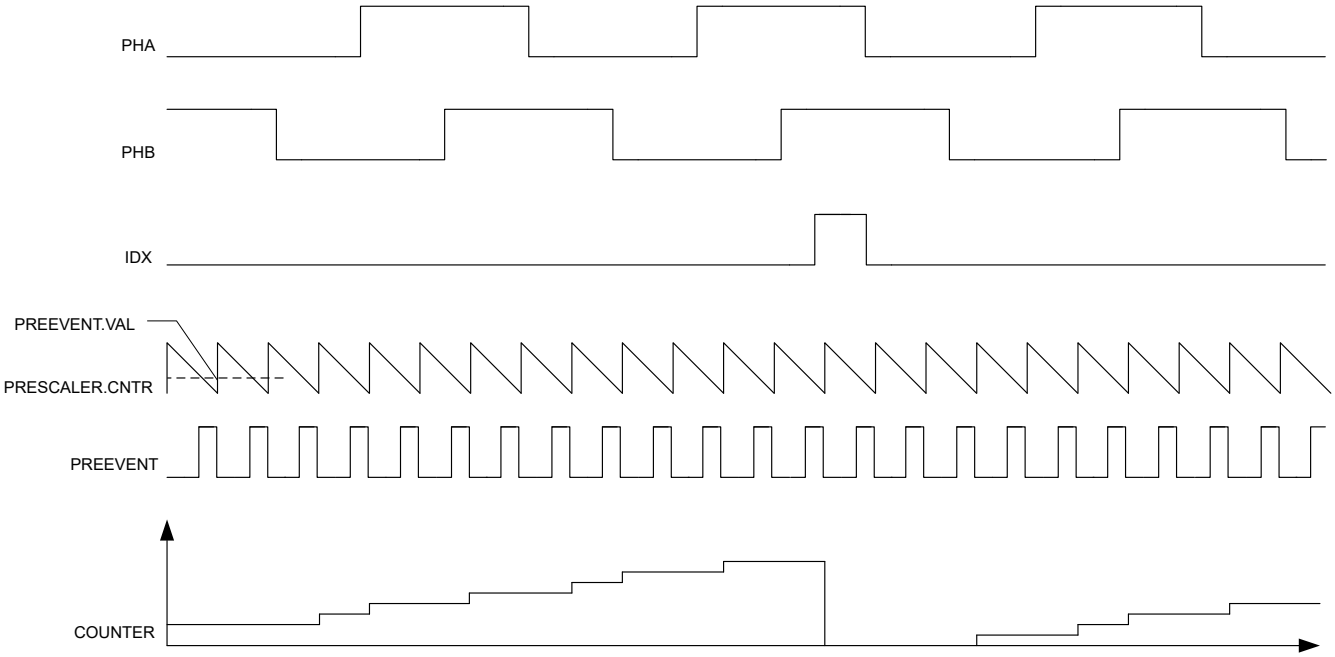

Figure 13-8. QDEC Example with PREEVENT

13.4.2 DMA

The register DMA is used to enable DMA requests. The DMA.REQ field sets which interrupt event generates a DMA request. The request is a pulse (one system clock period) which is generated when the corresponding interrupt is set in the RIS register. Upon a DMA request defined by REQ an internal address pointer is set to RWADDR*4. Every access to DMARW increments the internal pointer by 4 such that the next DMA access is to the next register.

The internal pointer stops after RWCNTR increments. Further access is ignored.

Below is an example of how to setup DMA and DMARW for updating PTGT, PC0CC, PC1CC when the counter hits zero.

- Set DMA.REQ = 2
- Set DMA.RWADDR = 63 (The PTGT address is 63*4=0xFC)
- Set DMA.RWCNTR = 2 (The PC1CC address is 63*4 + 2*4 = 0x104)
- Start timer in required mode.
- Upon receiving the DMA request the DMA should make at least 3 writes to DMARW which will be as if writing to PTGT, PC0CC then PC1CC. Any other read/writes to DMARW will be ignored.

13.4.3 IR Generation

By using GPT0 and GPT1 the timers can generate IR codes with minimal software interaction. An AND gate is set between GPT0 Channel 0 and GPT1 Channel 0, the output of this AND gate replaces GPT0 Channel 0. In IR generation mode GPT0 generates the carrier wave, while GPT1 works as the modulator.

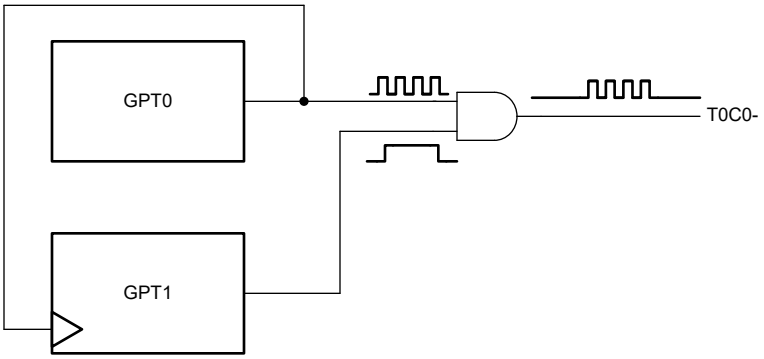

Figure 13-9. GPT IR Generation

Below is an example on how to setup the timers for IR with a 38kHz carrier wave.

GPT0 (Carrier wave generation):

- Set the PRECFG.TICKDIV and TGT to fulfill the following equation:

$$(PRECFG.TICKDIV + 1)*TGT*2 = 80MHz / 38kHz \quad (1)$$

  E.g. PRECFG.TICKDIV = 3 and TGT 263. This gives a carrier wave of approximately 38kHz (Theoretically 38.022kHz).

- Set C0CC = 210 to give roughly 50% duty cycle.
- Set C0CFG.CCACT = TGL_ON_CMP, and C0CFG.OUT0 = 1.
- Set IRGEN.CTL = 1.
- Start timer in up-periodic. CTL.MODE = 2

Configure SOC AON

- Set SOC_AON.GPT1EVTCTL1.TICKEN = GPT0OUT0

GPT1 (Modulator, example for the NEC protocol)

- Set PRECFG.TICKSRC = FALL_TICK
- Set C0CFG.CCACT = SET_ON_0_TGL_ON_CMP, C0CFG.OUT0 = 1
- Set TGT to the length of the symbol.
- Set C0CC to number of 38 kHz pulses in the symbol.
- Update PTGT on RIS.ZERO interrupt to send a new symbol.

13.4.4 Fault and Park

If GPTn.DESCEX[18] HBDF (Has Dead-Band, Fault, and Park logic) bit is set to one, the GPT implements the FAULT and PARK registers. The FAULT register is used to stop the timer upon an active fault input signal from the IOC. The PARK register can be used to set the IOC outputs of the GPT to a given state when the timer has stopped as a result of fault.

The fault input overrides channel 0 IOC input when FAULT.CTL != DIS. See Figure 13-3.

This means that channel 0 receives fault as input signal when C0CFG.INPUT = IO and FAULT.CTL != DIS. CHFILT can be used to avoid glitching on the fault input. Fault is level triggered, the polarity is set by the C0CFG.EDGE field. Here C0CFG.EDGE = RISE gives active high and C0CFG.EDGE = FALL gives active low polarity.

Set the Fault mode by setting FAULT.CTL. There are four different modes:

- **DIS**: The counter ignores the fault input.
- **IMMEDIATE**: In this mode the counter stops immediately on an active fault input (2 system clock cycles of synch delay is expected). This is done by hardware by setting CTL.MODE = DIS. To start the counter

software must set CTL.MODE != DIS. The RIS.FAULT interrupt is also set immediately on active fault input. If the RIS.FAULT input is cleared, it will not be set again while CTL.MODE == DIS even though the fault input is active. This is because the 2 stage synchronizers and the channel filter is not active while CTL.MODE == DIS. If the counter is started by setting CTL.MODE != DIS when the fault input is active it will immediately stop the counter and set RIS.FAULT.

- **ZEROCOND**: In this mode the counter stops when CNTR = 0 after an active fault input. If the RIS.FAULT flag has been cleared by software before CNTR= 0, and the fault input is inactive, the counter will continue as normal. When the counter stops on zero, it can be started again by clearing the RIS.FAULT flag. If you want to change the counter mode you should set CTL.MODE = DIS, clear the RIS.FAULT interrupt, then start timer in required mode. The channel filter will keep running while the CNTR is halted at zero. This ensures an up-to-date fault input.
- **IRQ**: In this mode only the RIS.FAULT interrupt is set on active fault.

General notes on Fault:

- When the channel filter is used together with Fault, and and the timer is restarted, the fault input will not be evaluated before CHFILT.LOAD number of consecutive equal samples. This means that an active fault could have been present when the timer started (by setting CTL.MODE != DIS), but the timer will not stop before CHFILT.LOAD samples.
- In IMMEDIATE mode clear RIS.FAULT to start the timer again. Not doing so will immediately stop the timer upon start.

Example setup of Fault and Park.

- Set FAULT.CTL to wanted mode.
- Set C0CFG.EDGE = RISE/FALL. Here RISE = active high, and FALL = active low.
- Set C0CFG.INPUT = IO.
- (Optional) Config CHFILT
- (Optional) Config IMASK to set CPU interrupt on fault. Typically required.
- (Optional) Config PARK.
- Start timer in wanted mode.

Figure 13-10 and Figure 13-11 illustrate the consequences of some of the possible Fault and Park configurations.

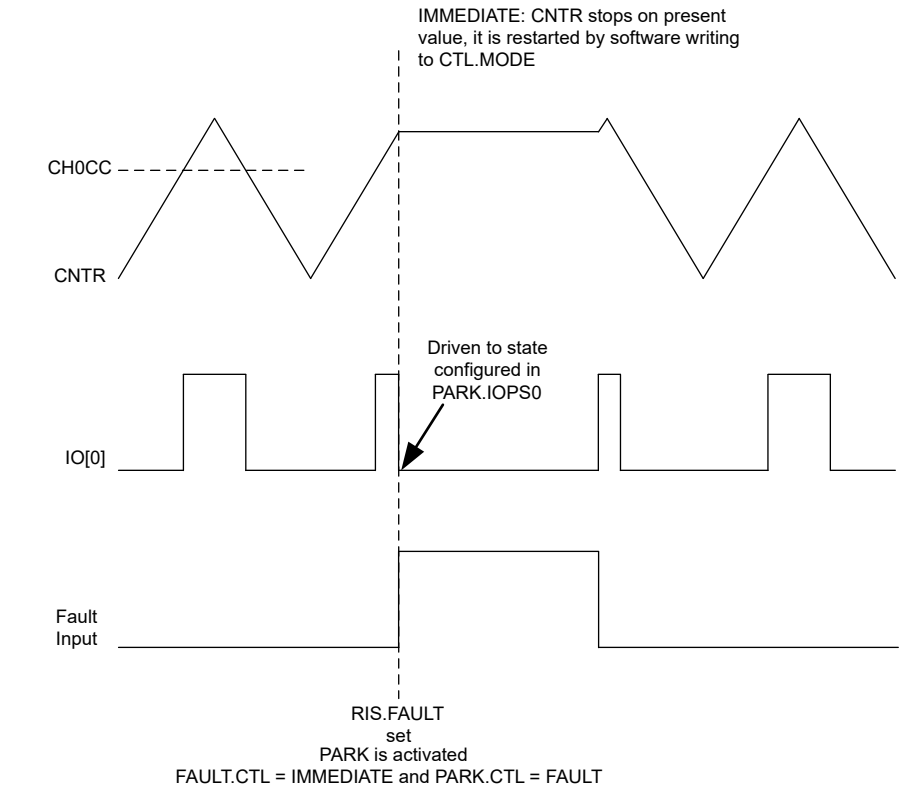

Figure 13-10. Fault and Park - Immediate Mode

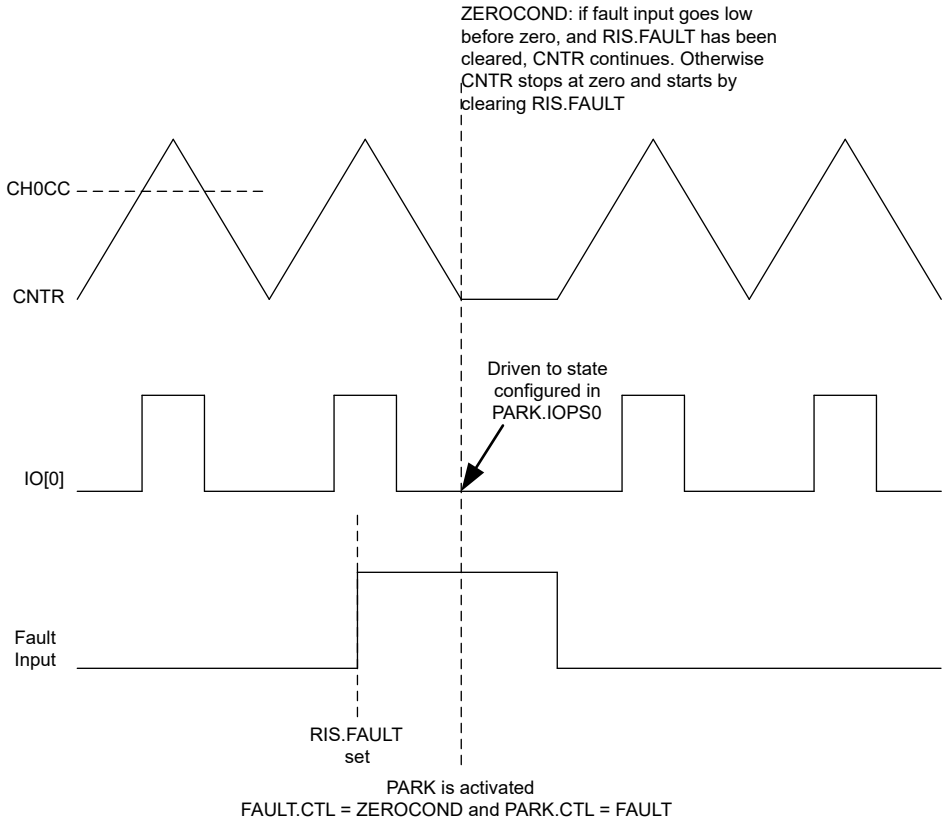

Figure 13-11. Fault and Park - Zero Condition

13.4.5 Dead-Band

If the SYS_HDBF=1 the GPT can optionally insert a dead-band transition in a reference PWM signal. Dead band insertion is accomplished by taking a reference pulse width modulated signal and generating two pulse width modulated signals (IOn and IO_Cn) of the same frequency but with a dead band period inserted between the signals. This is shown in Figure 13-12 .

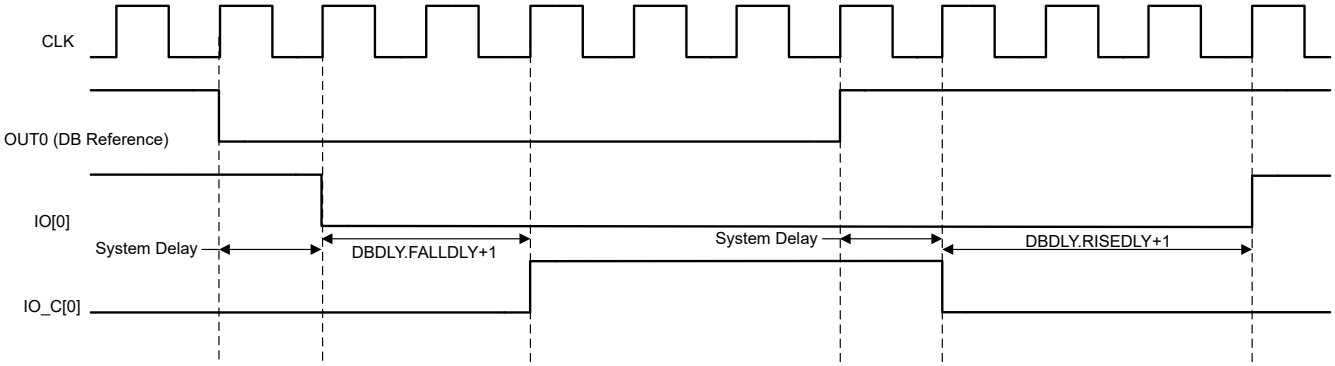

Figure 13-12. Dead-band Insertion

As shown in Figure 13-12 RISEDLY and FALLDLY fields from the DBDLY register are added with a value of 1 during Dead-Band insertion. Both IO and IO_C signals are also one system clock cycled delayed due to the Dead-band insertion logic.

Note

- Configuring RISEDLY longer than or equal to the pulse width of the reference signal results in a constant low IO output.
- Configuring FALLDLY longer than or equal to the low pulse width of the reference signal results in a constant low IO_C output.

Example setup of Dead-Band on IO0 and IO_C0

- Configure PWM output as required on channel 0. See Section 13.3.6.2
- Set PWM output to be generated on output 0 by setting C0CFG.OUT0 = 1
- Set wanted fall/rise delay by setting DBDLY.RISEDLY and DBDLY.FALLDLY.
- Set DBCTL to generate dead band on IO0 and IO_C0 by setting DBCTL.IO0 = 1.
- Start timer by writing to CTL.

13.4.6 Dead-Band, Fault and Park

An important feature to maintain when dead-band is used together with Fault and Park is to never make a switch on the IO outputs without dead band insertion. When the park values for IO and IO_C are opposite this switch is trivial, as this corresponds to a switch done under normal PWM dead band operation. See Figure 13-13.

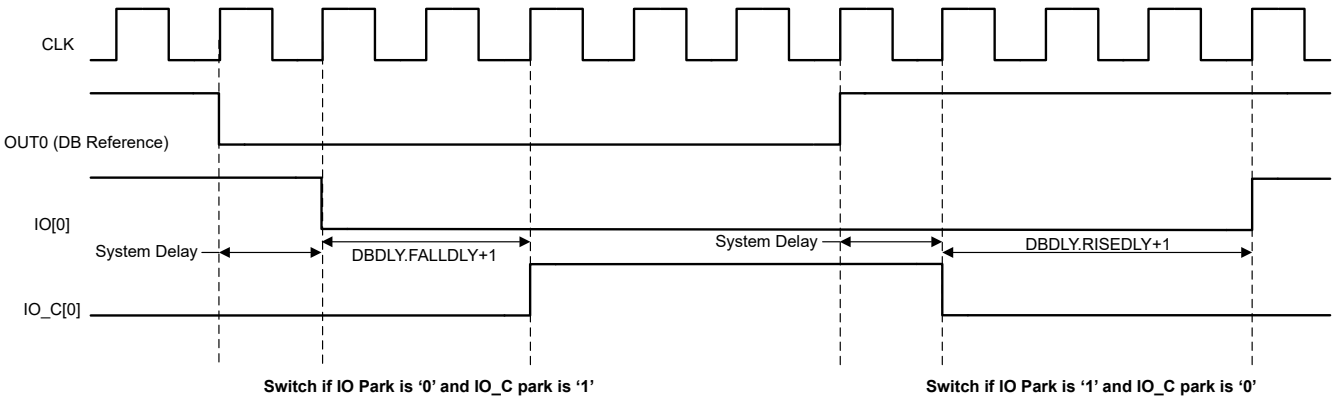

Figure 13-13. Dead-band Switch to Opposite Park States

If the IO and IO_C park values are equal the switch is not trivial. To maintain a dead-band insertion between switches, the implementation principle is as follows:

- When park is activated (either from fault or debug) the dead band reference input is set to IO park state immediately. • This will ensure that the IO output gets set to park state after a fall/rise delay.
- When the delay is finished, meaning that IO output is in park state, this output is "locked" to the park state. The dead-band logic does not control this output anymore.
- At the same time as the IO output is locked, the dead-band reference signal is switched to the inverse of IO_C park state. This then sets IO_C to the IO_C park state after a fall/rise delay.
- As the IO output is locked, the output does not change as the dead-band reference signal changes.

When using this method, the IO and IO_C outputs can use (FALLDLY+RISEDLY+2) cycles before settling in the park state when the IO and IO_C outputs are equal. The IO and IO_C outputs use FALLDLY+1 or RISEDLY+1 to settle when the IO and IO_C outputs are opposite.

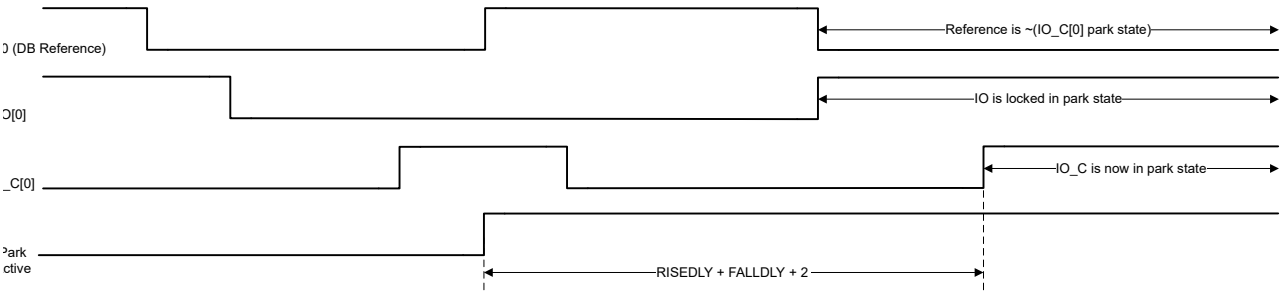

Figure 13-14. Dead-band Switch to Equal Park States

In Figure 13-14 Park active is an internal signal set by either Fault or Debug depending on the configuration. Park active is set one clock cycle after Fault or Debug is registered.

13.4.7 Example Application: Brushless DC (BLDC) Motor

The GPT can be used to drive a BLDC motor. Consider a BLDC motor with 3 half bridges, this requires three or more channels. In this scenario the 3 IOC and the 3 IOC complementary outputs of one GPT are connected to a motor driver or directly to the half bridges. See Figure 13-15.

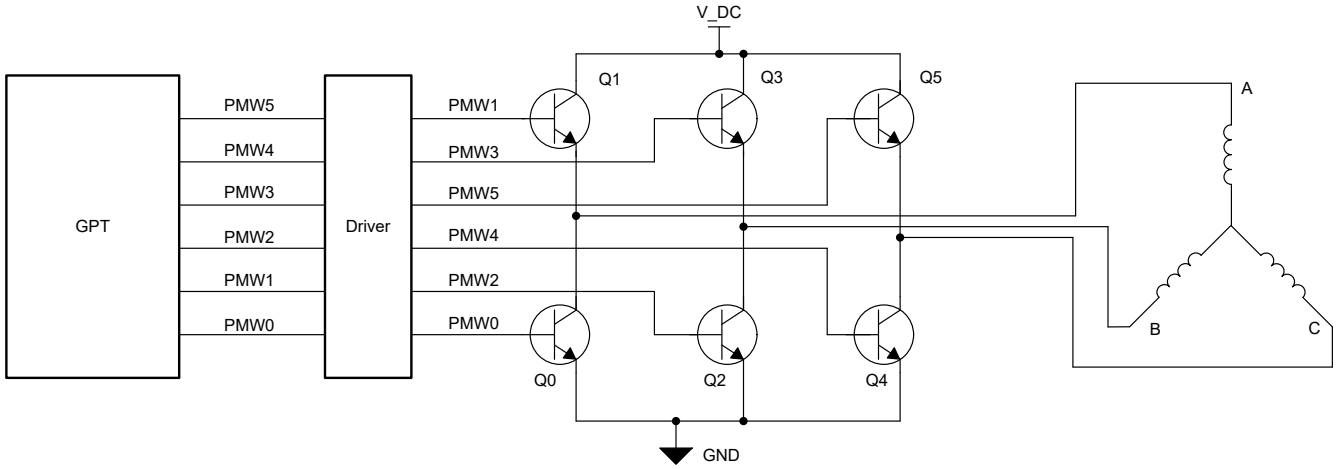

Figure 13-15. BLDC Application Example

Here each half bridge is controlled by an IOC and IOC complementary pair, that is, PWM0 and PWM1 corresponds to IOC[0] and IOC_C[0], PWM2 and PWM3 to IOC[1] and IOC_C[1] and so on. To operate the motor in a basic fashion current is driven through two of the inductors at a time in a sequential pattern. This is done by switching the transistors in a distinct pattern, see Figure 13-16.

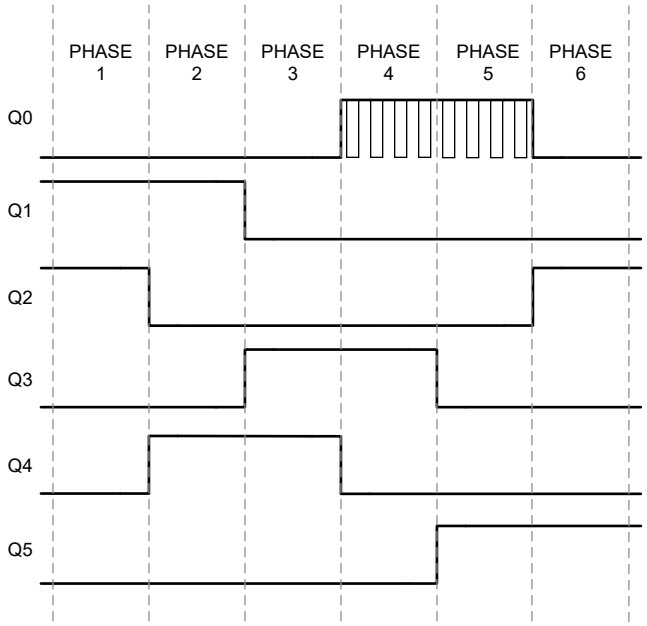

Figure 13-16. Example of Transition Phases to Drive a BLDC Motor

Notice that the high time of each transistor consists of a PWM signal (as illustrated in Q0). The duty cycle of the PWM signal corresponds to the current that is driven through the inductors and consequently the motor speed/load. The PWM can be generated as mentioned in Section 13.3.6.2. The software interactions needed to operate the motor (We assume Q0 is connected to IOC[0] and Q1 connected to IOC_C[0] etc.) are as follows:

SW operations:

- Phase 1: Configure IOCTL to invert IOC_C[0] (Q1) and let IOC[1] (Q2) out. All other outputs are configured low.
- Phase 2: Configure IOCTL to invert IOC_C[0] (Q1) and let IOC[2] (Q4) out. All other outputs are configured low.

- Phase 3: Configure IOCTL to invert IOC_C[1] (Q3) and let IOC[2] (Q4) out. All other outputs are configured low.
- Phase 4: Configure IOCTL to invert IOC_C[1] (Q3) and let IOC[0] (Q0) out. All other outputs are configured low.
- Phase 5: Configure IOCTL to invert IOC_C[2] (Q5) and let IOC[0] (Q0) out. All other outputs are configured low.
- Phase 6: Configure IOCTL to invert IOC_C[2] (Q5) and let IOC[1] (Q2) out. All other outputs are configured low.

Software needs a signal to determine when to change between the different phases, this can for example be done by an ADC measuring the back (EMF) Electromotive Force at the inactive inductor. Software can also change phases only on a ZERO interrupt from GPT to ensure complete PWM pulses during phase changes.

13.5 GPTIMER Registers

Table 13-4 lists the memory-mapped registers for the GPTIMER registers. All register offset addresses not listed in Table 13-4 should be considered as reserved locations and the register contents should not be modified.

Table 13-4. GPTIMER Registers

Offset	Acronym	Register Name	Section
0h	DESC	Description	Section 13.5.1
4h	DESCEX	Description Extended	Section 13.5.2
8h	STARTCFG	Start Configuration	Section 13.5.3
Ch	CTL	Timer Control	Section 13.5.4
10h	OUTCTL	Output Control	Section 13.5.5
14h	CNTR	Counter	Section 13.5.6
18h	PRECFG	Clock Prescaler Configuration	Section 13.5.7
1Ch	PREEVENT	Prescaler Event	Section 13.5.8
3Ch	DMA	Direct Memory Accsess	Section 13.5.9
40h	DMARW	Direct Memory Accsess	Section 13.5.10
44h	ADCTRG	Direct Memory Accsess	Section 13.5.11
48h	IOCTL	IO Control Register	Section 13.5.12
68h	IMASK	Interrupt Mask	Section 13.5.13
6Ch	RIS	Raw Interrupt Status	Section 13.5.14
70h	MIS	Masked Interrupt Status	Section 13.5.15
74h	ISET	Interrupt Set	Section 13.5.16
78h	ICLR	Interrupt Clear	Section 13.5.17
7Ch	IMSET	Interrupt Clear	Section 13.5.18
80h	IMCLR	Interrupt Clear	Section 13.5.19
84h	EMU	Interrupt Clear	Section 13.5.20
C0h	C0CFG	Channel 0 Configuration	Section 13.5.21
C4h	C1CFG	Channel 1 Configuration	Section 13.5.22
C8h	C2CFG	Channel 2 Configuration	Section 13.5.23
FCh	PTGT	Target	Section 13.5.24
100h	PC0CC	Pipeline Channel 0 Capture Compare	Section 13.5.25
104h	PC1CC	Pipeline Channel 1 Capture Compare	Section 13.5.26
108h	PC2CC	Pipeline Channel 2 Capture Compare	Section 13.5.27
13Ch	TGT	Target	Section 13.5.28
140h	C0CC	Channel Capture Compare	Section 13.5.29
144h	C1CC	Channel Capture Compare	Section 13.5.30
148h	C2CC	Channel Capture Compare	Section 13.5.31
17Ch	PTGTNC	Shadow Target	Section 13.5.32
180h	PC0CCNC	Pipeline Channel 0 Capture Compare No Clear	Section 13.5.33
184h	PC1CCNC	Pipeline Channel 1 Capture Compare No Clear	Section 13.5.34
188h	PC2CCNC	Pipeline Channel 2 Capture Compare No Clear	Section 13.5.35
1BCh	TGTNC	Shadow Target No Clear	Section 13.5.36
1C0h	C0CCNC	Channel 0 Capture Compare No Clear	Section 13.5.37
1C4h	C1CCNC	Channel 1 Capture Compare No Clear	Section 13.5.38
1C8h	C2CCNC	Channel 2 Capture Compare No Clear	Section 13.5.39
1000h	CLKCFG	Clock Enable Register	Section 13.5.40

Complex bit access types are encoded to fit into small table cells. Table 13-5 shows the codes that are used for access types in this section.

Table 13-5. GPTIMER Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

13.5.1 DESC Register (Offset = 0h) [Reset = DE491000h]

DESC is shown in Table 13-6.

Return to the Summary Table.

Description Register. This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 13-6. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	DE49h	Module identifier used to uniquely identify this IP.
15-12	STDIPOFF	R	1h	Standard IP MMR block offset. Standard IP MMRs are the set of from aggregated IRQ registers till DTB. 0: Standard IP MMRs do not exist 0x1-0xF: Standard IP MMRs begin at offset of (64*STDIPOFF from the base IP address)
11-8	INSTIDX	R	0h	IP Instance ID number. If multiple instances of IP exist in the device, this field can identify the instance number.
7-4	MAJREV	R	1h	Major revision of IP.
3-0	MINREV	R	0h	Minor revision of IP.

13.5.2 DESCEX Register (Offset = 4h) [Reset = 00000000h]

DESCEX is shown in Table 13-7.

Return to the Summary Table.

Description Extended This register describes the parameters of the LGPT.

Table 13-7. DESCEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	HIR	R	1h	Has IR logic.
18	HDBF	R	1h	Has Dead-Band, Fault, and Park logic.
17-14	PREW	R	8h	Prescaler width. The prescaler can maximum be configured to 2^PREW-1.
13	HQDEC	R	1h	Has Quadrature Decoder.
12	HCIF	R	1h	Has channel input filter.
11-8	CIFS	R	8h	Channel input filter size. The prevailing state filter can maximum be configured to 2^CIFS-1.
7	HDMA	R	1h	Has uDMA output and logic.
6	HINT	R	1h	Has interrupt output and logic.
5-4	CNTRW	R	0h	Counter bit-width. The maximum counter value is equal to 2^CNTRW-1. 0h = 16-bit counter. 1h = 24-bit counter. 2h = 32-bit counter. 3h = RESERVED
3-0	NCH	R	4h	Number of channels.

13.5.3 STARTCFG Register (Offset = 8h) [Reset = 00000000h]

STARTCFG is shown in Table 13-8.

Return to the Summary Table.

Start Configuration This register is only for when MODE is configured to one of the SYNC modes. This register defines when this LGPT starts.

Table 13-8. STARTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LGPT0	R/W	0h	LGPT start

13.5.4 CTL Register (Offset = Ch) [Reset = 00000000h]

CTL is shown in Table 13-9.

Return to the Summary Table.

Timer Control

Table 13-9. CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	C2RST	W	0h	Channel 2 reset. 0h = No effect. 1h = Reset [C2CC.*], [PC2CC.*], and [C2CFG.*].
9	C1RST	W	0h	Channel 1 reset. 0h = No effect. 1h = Reset [C1CC.*], [PC1CC.*], and [C1CFG.*].
8	C0RST	W	0h	Channel 0 reset. 0h = No effect. 1h = Reset [C0CC], PC0CC, and C0CFG.
7-6	RESERVED	R	0h	Reserved
5	INTP	R/W	0h	Interrupt Phase. This bit field controls when the TGT and ZERO interrupts are set. 0h = TGT and ZERO are set one system clock cycle after [CNTR.*] = TARGET/ZERO. 1h = TGT and ZERO are set one timer clock cycle after [CNTR.*] = TARGET/ZERO.
4-3	CMPDIR	R/W	0h	Compare direction. This bit field controls the direction the counter must have in order to set the [RIS.*] compare interrupts. 0h = Compare [RIS.*] fields are set on up count and down count. 1h = Compare [RIS.*] fields are only set on up count. 2h = Compare [RIS.*] fields are only set on down count. 3h = RESERVED

Table 13-9. CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	MODE	R/W	0h	Timer mode control The [CNTR.*] restarts from 0 when MODE is written to UP_ONCE, UP_PER, UPDWN_PER, QDEC, SYNC_UP_ONCE, SYNC_UP_PER or SYNC_UPDWN_PER. When writing MODE all internally queued updates to the channels and [TGT.*] is cleared. When configuring the timer, MODE should be the last thing to configure. If changing timer configuration after MODE has been set is necessary, instructions, if any, given in the configuration registers should be followed. See for example [C0CFG.*]. 0h = Disable timer. Updates to counter, channels, and events stop. 1h = Count up once. The timer increments from 0 to target value, then stops and sets MODE to DIS. 2h = Count up periodically. The timer increments from 0 to target value, repeatedly. Period = (target value + 1) * timer clock period 3h = Count up and down periodically. The timer counts from 0 to target value and back to 0, repeatedly. Period = (target value * 2) * timer clock period 4h = The timer functions as a quadrature decoder. IOC input 0, IOC input 1 and IOC input 2 are used respectively as PHA, PHB and IDX inputs. IDX can be turned off by setting EDGE = NONE. The timer clock frequency sets the sample rate of the QDEC logic. This frequency can be configured in [PRECFG.*]. 5h = Start counting up once synchronous to another LGPT, selected within [STARTCFG.*]. The timer is started by setting MODE = UP_ONCE automatically. It then functions as a normal timer in MODE = UP_ONCE, incrementing from 0 to target value, then stops and sets MODE to DIS. 6h = Start counting up periodically synchronous to another LGPT, selected within [STARTCFG.*]. The timer is started by setting MODE = UP_PER automatically. It then operates as a normal timer in MODE = UP_PER, incrementing from 0 to target value, repeatedly. Period = (target value * 2) * timer clock period 7h = Start counting up and down periodically synchronous to another LGPT, selected within [STARTCFG.*]. The timer is started by setting MODE = UPDWN_PER automatically. It then operates as a normal timer in MODE = UPDWN_PER, counting from 0 to target value and back to 0, repeatedly. Period = (target value * 2) * timer clock period

13.5.5 OUTCTL Register (Offset = 10h) [Reset = 00000000h]

OUTCTL is shown in Table 13-10.

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Output Control Set and clear individual outputs manually. Manual update of an output takes priority over automatic channel updates to the same output. It is not possible to set and clear an output at the same time, such requests will be neglected. An output can be automatically cleared, set, toggled, or pulsed by each channel, listed in decreasing order of priority. The action with highest priority happens when multiple channels want to update an output at the same time. All outputs are connected to the event fabric and the IO controller. The outputs going to the IO controller have an additional complementary output, this output is the inverted IO output. Both the IO and the IO complementary outputs are passed through an IO Controller, see [IOCTL.*].

Table 13-10. OUTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	SETOUT2	W	0h	Set output 2. Write 1 to set output 2.
4	CLROUT2	W	0h	Clear output 2. Write 1 to clear output 2.
3	SETOUT1	W	0h	Set output 1. Write 1 to set output 1.
2	CLROUT1	W	0h	Clear output 1. Write 1 to clear output 1.
1	SETOUT0	W	0h	Set output 0. Write 1 to set output 0.
0	CLROUT0	W	0h	Clear output 0. Write 1 to clear output 0.

13.5.6 CNTR Register (Offset = 14h) [Reset = 00000000h]

CNTR is shown in Table 13-11.

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Counter The counter of this timer. After MODE is set the counter updates at the rate specified in [PRECFG.*].

Table 13-11. CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Current counter value. If MODE = QDEC this can be used to set the initial counter value during QDEC.

13.5.7 PRECFG Register (Offset = 18h) [Reset = 00000000h]

PRECFG is shown in Table 13-12.

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Clock Prescaler Configuration This register is used to set the timer clock period. The prescaler is a counter which counts down from the value TICKDIV. When the prescaler counter reaches zero, [CNTR.*] is updated. The field TICKDIV effectively divides the prescaler tick source. The timer clock frequency can be calculated as TICKSRC/(TICKDIV+1).

Table 13-12. PRECFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	TICKDIV	R/W	0h	Tick division. TICKDIV determines the timer clock frequency for the counter, and timer output updates. The timer clock frequency is the clock selected by TICKSRC divided by (TICKDIV + 1). This inverse is the timer clock period. 0x00: Divide by 1. 0x01: Divide by 2. ... 0xFF: Divide by 256.
7-2	RESERVED	R	0h	Reserved
1-0	TICKSRC	R/W	0h	Prescaler tick source. TICKSRC determines the source which decrements the prescaler. 0h = Prescaler is updated at the system clock. 1h = Prescaler is updated at the rising edge of TICKEN. 2h = Prescaler is updated at the falling edge of TICKEN. 3h = Prescaler is updated at both edges of TICKEN.

13.5.8 PREEVENT Register (Offset = 1Ch) [Reset = 00000000h]

PREEVENT is shown in Table 13-13.

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Prescaler Event This register is used to output a logic high signal before the zero crossing of the prescaler counter. The output is routed to the IOC.

Table 13-13. PREEVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VAL	R/W	0h	Sets the HIGH time of the prescaler event output. Event goes high when the prescaler counter equals [VAL]. Event goes low when prescaler counter is 0. Note: - Can be used to precharge or turn an external component on for a short time before sampling, like in QDEC. - If there is a requirement to create such events that have very short periods compared to timer clock period, use two timers. One timer acts as prescaler and event generator for another timer.

13.5.9 DMA Register (Offset = 3Ch) [Reset = 00000000h]

DMA is shown in Table 13-14.

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Direct Memory Access This register is used to enable DMA requests from the timer and set the register addresses which the DMA will access (read/write). Choose DMA request source by setting the REQ field. The setting of the corresponding interrupt in the [RIS.*] registers also sets the DMA request. Upon a DMA request defined by REQ an internal address pointer is set to Address*4. Every access to [DMARW.*] will increment the internal pointer by 4 such that the next DMA access will be to the next register. The internal pointer will stop after RWC increments. Further access will be ignored.

Table 13-14. DMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	RWC	R/W	0h	The read/write counter. RWCNTR+1 is the number of times the DMA can access (read/write) the DMARW register. For each DMA access to DMARW an internal counter is incremented, writing to the next address field. Address + 4*RWC is the final register address which can be accessed by the DMA.
15	RESERVED	R	0h	Reserved
14-8	Address	R/W	0h	The base address which the DMA access when reading/writing DMARW. The base address is set by taking the 9 LSB of the physical address and divide by 4. For example, if you wanted the Address to point to the PTGT register you should set Address = 0x0FC/4.
7-3	RESERVED	R	0h	Reserved
2-0	REQ	R/W	0h	DMA request trigger 0h = Disabled 1h = Setting of TGT generates a DMA request. 2h = Setting of ZERO generates a DMA request. 3h = Setting of FAULT generates a DMA request. 4h = Setting of C0CC generates a DMA request. 5h = Setting of C1CC generates a DMA request. 6h = Setting of C2CC generates a DMA request. 7h = Setting of C3CC generates a DMA request.

13.5.10 DMARW Register (Offset = 40h) [Reset = 00000000h]

DMARW is shown in Table 13-15.

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Direct Memory Access This register is used by the DMA to access (read/write) register inside this LGPT module. Each access to this register will increment the internal DMA address counter. See [DMA.*] for description.

Table 13-15. DMARW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	DMA read write value. The value that is read/written from/to the registers.

13.5.11 ADCTRG Register (Offset = 44h) [Reset = 00000000h]

ADCTRG is shown in Table 13-16.

Return to the Summary Table.

ADC Trigger This register is used to enable ADC trigger from the timer. Choose ADC trigger source by setting the SRC field. The setting of the corresponding interrupt in the [RIS.*] registers also sets the ADC trigger.

Table 13-16. ADCTRG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	SRC	R/W	0h	ADC request trigger 0h = Disabled 1h = Setting of TGT generates an ADC trigger. 2h = Setting of ZERO generates an ADC trigger. 3h = Setting of FAULT generates an ADC trigger. 4h = Setting of C0CC generates an ADC trigger. 5h = Setting of C1CC generates an ADC trigger. 6h = Setting of C2CC generates an ADC trigger. 7h = Setting of C3CC generates an ADC trigger.

13.5.12 IOCTL Register (Offset = 48h) [Reset = 00000000h]

IOCTL is shown in Table 13-17.

Return to the Summary Table.

IO Controller This register controls the IO outputs.

Table 13-17. IOCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-14	RESERVED	R	0h	Reserved
13-12	RESERVED	R	0h	Reserved
11-10	COUT2	R/W	0h	IO complementary output 2 control This bit field controls IO complementary output 2. 0h = Normal output. The IO complementary output is not changed. 1h = Driven low. The IO complementary output is driven low. 2h = Driven high. The IO complementary output is driven high. 3h = Inverted value. The IO complementary output is inverted.
9-8	OUT2	R/W	0h	IO output 2 control This bit field controls IO output 2. 0h = Normal output. The IO output is not changed. 1h = Driven low. The IO output is driven low. 2h = Driven high. The IO output is driven high. 3h = Inverted value. The IO output is inverted.
7-6	COUT1	R/W	0h	IO complementary output 1 control This bit field controls IO complementary output 1. 0h = Normal output. The IO complementary output is not changed. 1h = Driven low. The IO complementary output is driven low. 2h = Driven high. The IO complementary output is driven high. 3h = Inverted value. The IO complementary output is inverted.
5-4	OUT1	R/W	0h	IO output 1 control This bit field controls IO output 1. 0h = Normal output. The IO output is not changed. 1h = Driven low. The IO output is driven low. 2h = Driven high. The IO output is driven high. 3h = Inverted value. The IO output is inverted.
3-2	COUT0	R/W	0h	IO complementary output 0 control This bit field controls IO complementary output 0. 0h = Normal output. The IO complementary output is not changed. 1h = Driven low. The IO complementary output is driven low. 2h = Driven high. The IO complementary output is driven high. 3h = Inverted value. The IO complementary output is inverted.
1-0	OUT0	R/W	0h	IO output 0 control This bit field controls IO output 0. 0h = Normal output. The IO output is not changed. 1h = Driven low. The IO output is driven low. 2h = Driven high. The IO output is driven high. 3h = Inverted value. The IO output is inverted.

13.5.13 IMASK Register (Offset = 68h) [Reset = 00000000h]

IMASK is shown in Table 13-18.

Return to the Summary Table.

Interrupt mask. This register selects interrupt sources which are allowed to pass from [RIS.*] to [MIS.*] when the corresponding bit-fields are set to 1.

Table 13-18. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	C2CC	R/W	0h	Enable C2CC interrupt. 0h = Disable 1h = Enable
9	C1CC	R/W	0h	Enable C1CC interrupt. 0h = Disable 1h = Enable
8	C0CC	R/W	0h	Enable C0CC interrupt. 0h = Disable 1h = Enable
7	RESERVED	R	0h	Reserved
6	FAULT	R/W	0h	Enable FAULT interrupt. 0h = Disable 1h = Enable
5	IDX	R/W	0h	Enable IDX interrupt. 0h = Disable 1h = Enable
4	DIRCHNG	R/W	0h	Enable DIRCHNG interrupt. 0h = Disable 1h = Enable
3	CNTRCHNG	R/W	0h	Enable CNTRCHNG interrupt. 0h = Disable 1h = Enable
2	DBLTRANS	R/W	0h	Enable DBLTRANS interrupt. 0h = Disable 1h = Enable
1	ZERO	R/W	0h	Enable ZERO interrupt. 0h = Disable 1h = Enable
0	TGT	R/W	0h	Enable TGT interrupt. 0h = Disable 1h = Enable

13.5.14 RIS Register (Offset = 6Ch) [Reset = 00000000h]

RIS is shown in Table 13-19.

Return to the Summary Table.

Raw interrupt status. This register reflects the state of all pending interrupts, regardless of masking. This register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the corresponding [ICLR.*] register bit.

Table 13-19. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	C2CC	R	0h	Status of the [C2CC] interrupt. The interrupt is set when [C2CC] has capture or compare event. 0h = Cleared 1h = Set
9	C1CC	R	0h	Status of the [C1CC] interrupt. The interrupt is set when [C1CC] has capture or compare event. 0h = Cleared 1h = Set
8	C0CC	R	0h	Status of the [C0CC] interrupt. The interrupt is set when [C0CC] has capture or compare event. 0h = Cleared 1h = Set
7	RESERVED	R	0h	Reserved
6	FAULT	R	0h	Status of the [FAULT] interrupt. The interrupt is set immediately on active fault input. 0h = Cleared 1h = Set
5	IDX	R	0h	Status of the [IDX] interrupt. The interrupt is set when [IDX] is active. 0h = Cleared 1h = Set
4	DIRCHNG	R	0h	Status of the [DIRCHNG] interrupt. The interrupt is set when the direction of the counter changes. 0h = Cleared 1h = Set
3	CNTRCHNG	R	0h	Status of the [CNTRCHNG] interrupt. The interrupt is set when the counter increments or decrements. 0h = Cleared 1h = Set
2	DBLTRANS	R	0h	Status of the [DBLTRANS] interrupt. The interrupt is set when a double transition has happened during QDEC mode. 0h = Cleared 1h = Set
1	ZERO	R	0h	Status of the [ZERO] interrupt. The interrupt is set when [CNTR.*] = 0. 0h = Cleared 1h = Set
0	TGT	R	0h	Status of the [TGT] interrupt. The interrupt is set when [CNTR.*] = [TGT.*]. 0h = Cleared 1h = Set

13.5.15 MIS Register (Offset = 70h) [Reset = 00000000h]

MIS is shown in Table 13-20.

Return to the Summary Table.

Masked interrupt status. This register is simply a bit-wise AND of the contents of [IMASK.*] and RIS.*] registers. A flag set in this register can be cleared by writing 1 to the corresponding [ICLR.*] register bit.

Table 13-20. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	C2CC	R	0h	Masked status of the C2CC interrupt. 0h = Cleared 1h = Set
9	C1CC	R	0h	Masked status of the C1CC interrupt. 0h = Cleared 1h = Set
8	C0CC	R	0h	Masked status of the C0CC interrupt. 0h = Cleared 1h = Set
7	RESERVED	R	0h	Reserved
6	FAULT	R	0h	Masked status of the FAULT interrupt. 0h = Cleared 1h = Set
5	IDX	R	0h	Masked status of the IDX interrupt. 0h = Cleared 1h = Set
4	DIRCHNG	R	0h	Masked status of the DIRCHNG interrupt. 0h = Cleared 1h = Set
3	CNTRCHNG	R	0h	Masked status of the CNTRCHNG interrupt. 0h = Cleared 1h = Set
2	DBLTRANS	R	0h	Masked status of the DBLTRANS interrupt. 0h = Cleared 1h = Set
1	ZERO	R	0h	Masked status of the ZERO interrupt. 0h = Cleared 1h = Set
0	TGT	R	0h	Masked status of the TGT interrupt. 0h = Cleared 1h = Set

13.5.16 ISET Register (Offset = 74h) [Reset = 00000000h]

ISET is shown in Table 13-21.

Return to the Summary Table.

Interrupt set register. This register can used by software for diagnostics and safety checking purposes. Writing a 1 to a bit in this register will set the event and the corresponding [RIS.*] bit also gets set. If the corresponding [IMASK.*] bit is set, then the corresponding [MIS.*] register bit also gets set.

Table 13-21. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	C2CC	W	0h	Set the C2CC interrupt. 0h = No effect 1h = Set
9	C1CC	W	0h	Set the C1CC interrupt. 0h = No effect 1h = Set
8	C0CC	W	0h	Set the C0CC interrupt. 0h = No effect 1h = Set
7	RESERVED	R	0h	Reserved
6	FAULT	W	0h	Set the FAULT interrupt. 0h = No effect 1h = Set
5	IDX	W	0h	Set the IDX interrupt. 0h = No effect 1h = Set
4	DIRCHNG	W	0h	Set the DIRCHNG interrupt. 0h = No effect 1h = Set
3	CNTRCHNG	W	0h	Set the CNTRCHNG interrupt. 0h = No effect 1h = Set
2	DBLTRANS	W	0h	Set the DBLTRANS interrupt. 0h = No effect 1h = Set
1	ZERO	W	0h	Set the ZERO interrupt. 0h = No effect 1h = Set
0	TGT	W	0h	Set the TGT interrupt. 0h = No effect 1h = Set

13.5.17 ICLR Register (Offset = 78h) [Reset = 00000000h]

ICLR is shown in Table 13-22.

Return to the Summary Table.

Interrupt clear register. This register allows software to clear interrupts. Writing a 1 to a bit in this register will clear the event and the corresponding [RIS.*] bit also gets cleared. If the corresponding [IMASK.*] bit is set, then the corresponding [MIS.*] register bit also gets cleared.

Table 13-22. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	C2CC	W	0h	Clear the C2CC interrupt. 0h = No effect 1h = Clear
9	C1CC	W	0h	Clear the C1CC interrupt. 0h = No effect 1h = Clear
8	C0CC	W	0h	Clear the C0CC interrupt. 0h = No effect 1h = Clear
7	RESERVED	R	0h	Reserved
6	FAULT	W	0h	Clear the FAULT interrupt. 0h = No effect 1h = Clear
5	IDX	W	0h	Clear the IDX interrupt. 0h = No effect 1h = Clear
4	DIRCHNG	W	0h	Clear the DIRCHNG interrupt. 0h = No effect 1h = Clear
3	CNTRCHNG	W	0h	Clear the CNTRCHNG interrupt. 0h = No effect 1h = Clear
2	DBLTRANS	W	0h	Clear the DBLTRANS interrupt. 0h = No effect 1h = Clear
1	ZERO	W	0h	Clear the ZERO interrupt. 0h = No effect 1h = Clear
0	TGT	W	0h	Clear the TGT interrupt. 0h = No effect 1h = Clear

13.5.18 IMSET Register (Offset = 7Ch) [Reset = 00000000h]

IMSET is shown in Table 13-23.

Return to the Summary Table.

Interrupt mask set register. Writing a 1 to a bit in this register will set the corresponding [IMASK.*] bit.

Table 13-23. IMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	C2CC	W	0h	Set the C2CC mask. 0h = No effect 1h = Set
9	C1CC	W	0h	Set the C1CC mask. 0h = No effect 1h = Set
8	C0CC	W	0h	Set the C0CC mask. 0h = No effect 1h = Set
7	RESERVED	R	0h	Reserved
6	FAULT	W	0h	Set the FAULT mask. 0h = No effect 1h = Set
5	IDX	W	0h	Set the IDX mask. 0h = No effect 1h = Set
4	DIRCHNG	W	0h	Set the DIRCHNG mask. 0h = No effect 1h = Set
3	CNTRCHNG	W	0h	Set the CNTRCHNG mask. 0h = No effect 1h = Set
2	DBLTRANS	W	0h	Set the DBLTRANS mask. 0h = No effect 1h = Set
1	ZERO	W	0h	Set the ZERO mask. 0h = No effect 1h = Set
0	TGT	W	0h	Set the TGT mask. 0h = No effect 1h = Set

13.5.19 IMCLR Register (Offset = 80h) [Reset = 00000000h]

IMCLR is shown in Table 13-24.

Return to the Summary Table.

Interrupt mask clear register. Writing a 1 to a bit in this register will clear the corresponding [IMASK.*] bit.

Table 13-24. IMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	C2CC	W	0h	Clear the C2CC mask. 0h = No effect 1h = Clear
9	C1CC	W	0h	Clear the C1CC mask. 0h = No effect 1h = Clear
8	C0CC	W	0h	Clear the C0CC mask. 0h = No effect 1h = Clear
7	RESERVED	R	0h	Reserved
6	FAULT	W	0h	Clear the FAULT mask. 0h = No effect 1h = Clear
5	IDX	W	0h	Clear the IDX mask. 0h = No effect 1h = Clear
4	DIRCHNG	W	0h	Clear the DIRCHNG mask. 0h = No effect 1h = Clear
3	CNTRCHNG	W	0h	Clear the CNTRCHNG mask. 0h = No effect 1h = Clear
2	DBLTRANS	W	0h	Clear the DBLTRANS mask. 0h = No effect 1h = Clear
1	ZERO	W	0h	Clear the ZERO mask. 0h = No effect 1h = Clear
0	TGT	W	0h	Clear the TGT mask. 0h = No effect 1h = Clear

13.5.20 EMU Register (Offset = 84h) [Reset = 00000000h]

EMU is shown in Table 13-25.

Return to the Summary Table.

Debug control This register can be used to freeze the timer when CPU halts when HALT is set to 1. When HALT is set to 0, or when the CPU releases debug halt, the filters and edge detection logic is flushed and the timer starts. For setting a predefined output value during a CPU debug halt, [PARK.*], if the timer has this register, should be configured additionally. If this timer does not have the [PARK.*] register a predefined output value during CPU halt is not possible.

Table 13-25. EMU Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	CTL	R/W	0h	Halt control. Configure when the counter shall stop upon CPU halt. This bitfield only applies if HALT = 1. 0h = Immediate reaction. The counter stops immediately on debug halt. 1h = Zero condition. The counter stops when [CNTR.*] = 0.
0	HALT	R/W	0h	Halt LGPT when CPU is halted in debug. 0h = Disable. 1h = Enable.

13.5.21 C0CFG Register (Offset = C0h) [Reset = 00000000h]

C0CFG is shown in Table 13-26.

Return to the Summary Table.

Channel 0 Configuration This register configures channel function and enables outputs. Each channel has an edge-detection circuit. The the edge-detection circuit is: - enabled while [CCACT] selects a capture function and MODE is different from DIS. - flushed while [CCACT] selects a capture function and MODE is changed from DIS to another mode. The flush action uses two system clock periods. It prevents capture events caused by expired signal values stored in the edge-detection circuit. The channel input signal enters the edge-detection circuit. False capture events can occur when: - the edge-detection circuit contains expired signal samples and the circuit is enabled without flush as described above. - the [CCACT] field is reconfigured while CTL.MODE is different from DIS. Primary use scenario is to select [CCACT] before starting the timer. Follow these steps to configure [CCACT] to a capture action while MODE is different from DIS: - Set [EDGE] to NONE. - Configure [CCACT]. - Wait for three system clock periods before setting [EDGE] different from NONE. These steps prevent capture events caused by expired signal values in edge-detection circuit.

Table 13-26. C0CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	OUT2	R/W	0h	Output 2 enable. When 0 < [CCACT] < 8, OUT2 becomes zero after a capture or compare event. 0h = Channel 0 does not control output 2. 1h = Channel 0 controls output 2.
9	OUT1	R/W	0h	Output 1 enable. When 0 < [CCACT] < 8, OUT1 becomes zero after a capture or compare event. 0h = Channel 0 does not control output 1. 1h = Channel 0 controls output 1.
8	OUT0	R/W	0h	Output 0 enable. When 0 < [CCACT] < 8, OUT0 becomes zero after a capture or compare event. 0h = Channel 0 does not control output 0. 1h = Channel 0 controls output 0.
7	RESERVED	R	0h	Reserved
6	INPUT	R/W	0h	Select channel input. 0h = Event fabric 1h = IO controller
5-4	EDGE	R/W	0h	Determines the edge that triggers the channel input event. This happens post filter. 0h = Input is turned off. 1h = Input event is triggered at rising edge. 2h = Input event is triggered at falling edge. 3h = Input event is triggered at both edges.

Table 13-26. C0CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CCACT	R/W	0h	Capture-Compare action. Capture-Compare action defines 15 different channel functions that utilize capture, compare, and zero events. In every compare event the timer looks at the current value of [CNTR.*]. The corresponding output event will be set 1 timer period after [CNTR.*] = [C0CC.*]. 0h = Disable channel. 1h = Set on capture, and then disable channel. Channel function sequence: - Set enabled outputs on capture event and copy VAL to VAL. - Disable channel. Primary use scenario is to select this function before starting the timer. Follow these steps to select this function while MODE is different from DIS: - Set CCACT to SET_ON_CAPT with no output enable. - Configure [INPUT] (optional). - Wait for three timer clock periods as defined in [PRECFG.*] before setting CCACT to SET_ON_CAPT_DIS. Output enable is optional. These steps prevent capture events caused by expired signal values in edge-detection circuit. 2h = Clear on zero, toggle on compare, and then disable channel. Channel function sequence: - Clear enabled outputs when VAL = 0. - Toggle enabled outputs when VAL = VAL. - Disable channel. Enabled outputs are set when VAL = 0 and VAL = 0. 3h = Set on zero, toggle on compare, and then disable channel. Channel function sequence: - Set enabled outputs when VAL = 0. - Toggle enabled outputs when VAL = VAL. - Disable channel. Enabled outputs are cleared when VAL = 0 and VAL = 0. 4h = Clear on compare, and then disable channel. Channel function sequence: - Clear enabled outputs when VAL = VAL. - Disable channel. 5h = Set on compare, and then disable channel. Channel function sequence: - Set enabled outputs when VAL = VAL. - Disable channel. 6h = Toggle on compare, and then disable channel. Channel function sequence: - Toggle enabled outputs when VAL = VAL. - Disable channel. 7h = Pulse on compare, and then disable channel. Channel function sequence: - Pulse enabled outputs when VAL = VAL. - Disable channel. The output is high for two timer clock periods. 8h = Period and pulse width measurement. Continuously capture period and pulse width of the signal selected by [INPUT] relative to the signal edge given by [EDGE]. Set enabled outputs and C0CC when VAL contains signal period and VAL contains signal pulse width. Notes: - Make sure to configure [INPUT] and CCACT when MODE equals DIS, then set MODE to UP_ONCE or UP_PER. - The counter restarts in the selected timer mode when VAL contains the signal period. - If more than one channel uses this function, the channels will perform this function one at a time. The channel with lowest number has priority and performs the function first. Next measurement starts when current measurement completes successfully or times out. A timeout occurs when counter equals target. - To observe a timeout event the TGT interrupt can be used, or another channel can be configured to SET_ON_CMP with compare value equal [TGT]. Signal property requirements: - Signal Period >= 2 * (1 + TICKDIV) * timer clock period. - Signal Period <= MAX([CNTR.*]) * (1 + TICKDIV) * timer clock period. - Signal low and high phase >= (1 + TICKDIV) * timer clock period. 9h = Set on capture repeatedly. Channel function sequence: - Set enabled outputs on capture event and copy VAL to VAL. Ah = Clear on zero, toggle on compare repeatedly. Channel function sequence: - Clear enabled outputs when VAL = 0. - Toggle enabled outputs when VAL = VAL. Set MODE to UPDWN_PER for center-aligned PWM generation. Duty cycle is given by: When VAL <= VAL: Duty cycle = 1 - (VAL / VAL). When VAL > VAL: Duty cycle = 0. Enabled outputs are set when VAL = 0 and VAL = 0. Bh = Set on zero, toggle on compare repeatedly. Channel function sequence: - Set enabled outputs when VAL = 0. - Toggle enabled outputs when VAL = VAL. Set MODE to UP_PER for edge-aligned

Table 13-26. C0CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				PWM generation. Duty cycle is given by: When VAL <= VAL: Duty cycle = VAL / (VAL + 1). When VAL > VAL: Duty cycle = 1. Enabled outputs are cleared when VAL = 0 and VAL = 0. Ch = Clear on compare repeatedly. Channel function sequence: - Clear enabled outputs when VAL = VAL. Dh = Set on compare repeatedly. Channel function sequence: - Set enabled outputs when VAL = VAL. Eh = Toggle on compare repeatedly. Channel function sequence: - Toggle enabled outputs when VAL = VAL. Fh = Pulse on compare repeatedly. Channel function sequence: - Pulse enabled outputs when VAL = VAL. The output is high for two timer clock periods.

13.5.22 C1CFG Register (Offset = C4h) [Reset = 00000000h]

C1CFG is shown in Table 13-27.

Return to the Summary Table.

Channel 1 Configuration This register configures channel function and enables outputs. Each channel has an edge-detection circuit. The the edge-detection circuit is: - enabled while [CCACT] selects a capture function and MODE is different from DIS. - flushed while [CCACT] selects a capture function and MODE is changed from DIS to another mode. The flush action uses two system clock periods. It prevents capture events caused by expired signal values stored in the edge-detection circuit. The channel input signal enters the edge-detection circuit. False capture events can occur when: - the edge-detection circuit contains expired signal samples and the circuit is enabled without flush as described above. - the [CCACT] field is reconfigured while CTL.MODE is different from DIS. Primary use scenario is to select [CCACT] before starting the timer. Follow these steps to configure [CCACT] to a capture action while MODE is different from DIS: - Set [EDGE] to NONE. - Configure [CCACT]. - Wait for three system clock periods before setting [EDGE] different from NONE. These steps prevent capture events caused by expired signal values in edge-detection circuit.

Table 13-27. C1CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	OUT2	R/W	0h	Output 2 enable. When 0 < [CCACT] < 8, OUT2 becomes zero after a capture or compare event. 0h = Channel 1 does not control output 2. 1h = Channel 1 controls output 2.
9	OUT1	R/W	0h	Output 1 enable. When 0 < [CCACT] < 8, OUT1 becomes zero after a capture or compare event. 0h = Channel 1 does not control output 1. 1h = Channel 1 controls output 1.
8	OUT0	R/W	0h	Output 0 enable. When 0 < [CCACT] < 8, OUT0 becomes zero after a capture or compare event. 0h = Channel 1 does not control output 0. 1h = Channel 1 controls output 0.
7	RESERVED	R	0h	Reserved
6	INPUT	R/W	0h	Select channel input. 0h = Event fabric 1h = IO controller
5-4	EDGE	R/W	0h	Determines the edge that triggers the channel input event. This happens post filter. 0h = Input is turned off. 1h = Input event is triggered at rising edge. 2h = Input event is triggered at falling edge. 3h = Input event is triggered at both edges.

Table 13-27. C1CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CCACT	R/W	0h	Capture-Compare action. Capture-Compare action defines 15 different channel functions that utilize capture, compare, and zero events. In every compare event the timer looks at the current value of [CNTR.*]. The corresponding output event will be set 1 timer period after [CNTR.*] = [C1CC.*]. 0h = Disable channel. 1h = Set on capture, and then disable channel. Channel function sequence: - Set enabled outputs on capture event and copy VAL to VAL. - Disable channel. Primary use scenario is to select this function before starting the timer. Follow these steps to select this function while MODE is different from DIS: - Set CCACT to SET_ON_CAPT with no output enable. - Configure [INPUT] (optional). - Wait for three timer clock periods as defined in [PRECFG.*] before setting CCACT to SET_ON_CAPT_DIS. Output enable is optional. These steps prevent capture events caused by expired signal values in edge-detection circuit. 2h = Clear on zero, toggle on compare, and then disable channel. Channel function sequence: - Clear enabled outputs when VAL = 0. - Toggle enabled outputs when VAL = VAL. - Disable channel. Enabled outputs are set when VAL = 0 and VAL = 0. 3h = Set on zero, toggle on compare, and then disable channel. Channel function sequence: - Set enabled outputs when VAL = 0. - Toggle enabled outputs when VAL = VAL. - Disable channel. Enabled outputs are cleared when VAL = 0 and VAL = 0. 4h = Clear on compare, and then disable channel. Channel function sequence: - Clear enabled outputs when VAL = VAL. - Disable channel. 5h = Set on compare, and then disable channel. Channel function sequence: - Set enabled outputs when VAL = VAL. - Disable channel. 6h = Toggle on compare, and then disable channel. Channel function sequence: - Toggle enabled outputs when VAL = VAL. - Disable channel. 7h = Pulse on compare, and then disable channel. Channel function sequence: - Pulse enabled outputs when VAL = VAL. - Disable channel. The output is high for two timer clock periods. 8h = Period and pulse width measurement. Continuously capture period and pulse width of the signal selected by [INPUT] relative to the signal edge given by [EDGE]. Set enabled outputs and C1CC when VAL contains signal period and VAL contains signal pulse width. Notes: - Make sure to configure [INPUT] and CCACT when MODE equals DIS, then set MODE to UP_ONCE or UP_PER. - The counter restarts in the selected timer mode when VAL contains the signal period. - If more than one channel uses this function, the channels will perform this function one at a time. The channel with lowest number has priority and performs the function first. Next measurement starts when current measurement completes successfully or times out. A timeout occurs when counter equals target. - To observe a timeout event the TGT interrupt can be used, or another channel can be configured to SET_ON_CMP with compare value equal [TGT]. Signal property requirements: - Signal Period >= 2 * (1 + TICKDIV) * timer clock period. - Signal Period <= MAX([CNTR.*]) * (1 + TICKDIV) * timer clock period. - Signal low and high phase >= (1 + TICKDIV) * timer clock period. 9h = Set on capture repeatedly. Channel function sequence: - Set enabled outputs on capture event and copy VAL to VAL. Ah = Clear on zero, toggle on compare repeatedly. Channel function sequence: - Clear enabled outputs when VAL = 0. - Toggle enabled outputs when VAL = VAL. Set MODE to UPDWN_PER for center-aligned PWM generation. Duty cycle is given by: When VAL <= VAL: Duty cycle = 1 - (VAL / VAL). When VAL > VAL: Duty cycle = 0. Enabled outputs are set when VAL = 0 and VAL = 0. Bh = Set on zero, toggle on compare repeatedly. Channel function sequence: - Set enabled outputs when VAL = 0. - Toggle enabled outputs when VAL = VAL. Set MODE to UP_PER for edge-aligned

Table 13-27. C1CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				PWM generation. Duty cycle is given by: When VAL <= VAL: Duty cycle = VAL / (VAL + 1). When VAL > VAL: Duty cycle = 1. Enabled outputs are cleared when VAL = 0 and VAL = 0. Ch = Clear on compare repeatedly. Channel function sequence: - Clear enabled outputs when VAL = VAL. Dh = Set on compare repeatedly. Channel function sequence: - Set enabled outputs when VAL = VAL. Eh = Toggle on compare repeatedly. Channel function sequence: - Toggle enabled outputs when VAL = VAL. Fh = Pulse on compare repeatedly. Channel function sequence: - Pulse enabled outputs when VAL = VAL. The output is high for two timer clock periods.

13.5.23 C2CFG Register (Offset = C8h) [Reset = 00000000h]

C2CFG is shown in Table 13-28.

Return to the Summary Table.

Channel 2 Configuration This register configures channel function and enables outputs. Each channel has an edge-detection circuit. The the edge-detection circuit is: - enabled while [CCACT] selects a capture function and MODE is different from DIS. - flushed while [CCACT] selects a capture function and MODE is changed from DIS to another mode. The flush action uses two system clock periods. It prevents capture events caused by expired signal values stored in the edge-detection circuit. The channel input signal enters the edge-detection circuit. False capture events can occur when: - the edge-detection circuit contains expired signal samples and the circuit is enabled without flush as described above. - the [CCACT] field is reconfigured while CTL.MODE is different from DIS. Primary use scenario is to select [CCACT] before starting the timer. Follow these steps to configure [CCACT] to a capture action while MODE is different from DIS: - Set [EDGE] to NONE. - Configure [CCACT]. - Wait for three system clock periods before setting [EDGE] different from NONE. These steps prevent capture events caused by expired signal values in edge-detection circuit.

Table 13-28. C2CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	OUT2	R/W	0h	Output 2 enable. When 0 < [CCACT] < 8, OUT2 becomes zero after a capture or compare event. 0h = Channel 2 does not control output 2. 1h = Channel 2 controls output 2.
9	OUT1	R/W	0h	Output 1 enable. When 0 < [CCACT] < 8, OUT1 becomes zero after a capture or compare event. 0h = Channel 2 does not control output 1. 1h = Channel 2 controls output 1.
8	OUT0	R/W	0h	Output 0 enable. When 0 < [CCACT] < 8, OUT0 becomes zero after a capture or compare event. 0h = Channel 2 does not control output 0. 1h = Channel 2 controls output 0.
7	RESERVED	R	0h	Reserved
6	INPUT	R/W	0h	Select channel input. 0h = Event fabric 1h = IO controller
5-4	EDGE	R/W	0h	Determines the edge that triggers the channel input event. This happens post filter. 0h = Input is turned off. 1h = Input event is triggered at rising edge. 2h = Input event is triggered at falling edge. 3h = Input event is triggered at both edges.

Table 13-28. C2CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CCACT	R/W	0h	Capture-Compare action. Capture-Compare action defines 15 different channel functions that utilize capture, compare, and zero events. In every compare event the timer looks at the current value of [CNTR.*]. The corresponding output event will be set 1 timer period after [CNTR.*] = [C2CC.*]. 0h = Disable channel. 1h = Set on capture, and then disable channel. Channel function sequence: - Set enabled outputs on capture event and copy VAL to VAL. - Disable channel. Primary use scenario is to select this function before starting the timer. Follow these steps to select this function while MODE is different from DIS: - Set CCACT to SET_ON_CAPT with no output enable. - Configure [INPUT] (optional). - Wait for three timer clock periods as defined in [PRECFG.*] before setting CCACT to SET_ON_CAPT_DIS. Output enable is optional. These steps prevent capture events caused by expired signal values in edge-detection circuit. 2h = Clear on zero, toggle on compare, and then disable channel. Channel function sequence: - Clear enabled outputs when VAL = 0. - Toggle enabled outputs when VAL = VAL. - Disable channel. Enabled outputs are set when VAL = 0 and VAL = 0. 3h = Set on zero, toggle on compare, and then disable channel. Channel function sequence: - Set enabled outputs when VAL = 0. - Toggle enabled outputs when VAL = VAL. - Disable channel. Enabled outputs are cleared when VAL = 0 and VAL = 0. 4h = Clear on compare, and then disable channel. Channel function sequence: - Clear enabled outputs when VAL = VAL. - Disable channel. 5h = Set on compare, and then disable channel. Channel function sequence: - Set enabled outputs when VAL = VAL. - Disable channel. 6h = Toggle on compare, and then disable channel. Channel function sequence: - Toggle enabled outputs when VAL = VAL. - Disable channel. 7h = Pulse on compare, and then disable channel. Channel function sequence: - Pulse enabled outputs when VAL = VAL. - Disable channel. The output is high for two timer clock periods. 8h = Period and pulse width measurement. Continuously capture period and pulse width of the signal selected by [INPUT] relative to the signal edge given by [EDGE]. Set enabled outputs and C2CC when VAL contains signal period and VAL contains signal pulse width. Notes: - Make sure to configure [INPUT] and CCACT when MODE equals DIS, then set MODE to UP_ONCE or UP_PER. - The counter restarts in the selected timer mode when VAL contains the signal period. - If more than one channel uses this function, the channels will perform this function one at a time. The channel with lowest number has priority and performs the function first. Next measurement starts when current measurement completes successfully or times out. A timeout occurs when counter equals target. - To observe a timeout event the TGT interrupt can be used, or another channel can be configured to SET_ON_CMP with compare value equal [TGT]. Signal property requirements: - Signal Period >= 2 * (1 + TICKDIV) * timer clock period. - Signal Period <= MAX([CNTR.*]) * (1 + TICKDIV) * timer clock period. - Signal low and high phase >= (1 + TICKDIV) * timer clock period. 9h = Set on capture repeatedly. Channel function sequence: - Set enabled outputs on capture event and copy VAL to VAL. Ah = Clear on zero, toggle on compare repeatedly. Channel function sequence: - Clear enabled outputs when VAL = 0. - Toggle enabled outputs when VAL = VAL. Set MODE to UPDWN_PER for center-aligned PWM generation. Duty cycle is given by: When VAL <= VAL: Duty cycle = 1 - (VAL / VAL). When VAL > VAL: Duty cycle = 0. Enabled outputs are set when VAL = 0 and VAL = 0. Bh = Set on zero, toggle on compare repeatedly. Channel function sequence: - Set enabled outputs when VAL = 0. - Toggle enabled outputs when VAL = VAL. Set MODE to UP_PER for edge-aligned

Table 13-28. C2CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				PWM generation. Duty cycle is given by: When VAL <= VAL: Duty cycle = VAL / (VAL + 1). When VAL > VAL: Duty cycle = 1. Enabled outputs are cleared when VAL = 0 and VAL = 0. Ch = Clear on compare repeatedly. Channel function sequence: - Clear enabled outputs when VAL = VAL. Dh = Set on compare repeatedly. Channel function sequence: - Set enabled outputs when VAL = VAL. Eh = Toggle on compare repeatedly. Channel function sequence: - Toggle enabled outputs when VAL = VAL. Fh = Pulse on compare repeatedly. Channel function sequence: - Pulse enabled outputs when VAL = VAL. The output is high for two timer clock periods.

13.5.24 PTGT Register (Offset = FCh) [Reset = 00000000h]

PTGT is shown in Table 13-29.

Return to the Summary Table.

Pipeline Target A read or write to this register will clear the ZERO and TGT interrupt. If MODE != QDEC. Target value for next counter period. The timer will copy VAL to VAL on the upcoming [CNTR.*] zero crossing only if VAL has been written. The copy does not happen when restarting the timer. This is useful to avoid period jitter in PWM applications with time-varying period, sometimes referenced as phase corrected PWM. If MODE = QDEC The [CNTR.*] value is updated with VALUE on IDX if the counter is counting down. If the counter is counting up, [CNTR.*] is loaded with zero on IDX. In this mode the VALUE is not loaded into [TGT] on zero crossing.

Table 13-29. PTGT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	The pipleline target value.

13.5.25 PC0CC Register (Offset = 100h) [Reset = 00000000h]

PC0CC is shown in Table 13-30.

Return to the Summary Table.

Pipeline Channel 0 Capture Compare

Table 13-30. PC0CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Pipeline Capture Compare value. User defined pipeline compare value or channel-updated capture value. A read or write to this register will clear the C0CC interrupt. Compare mode: An update of VAL will be transferred to VAL when the next VAL is zero and MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal. Capture mode: When CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by EDGE.

13.5.26 PC1CC Register (Offset = 104h) [Reset = 00000000h]

PC1CC is shown in Table 13-31.

Return to the Summary Table.

Pipeline Channel 1 Capture Compare

Table 13-31. PC1CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Pipeline Capture Compare value. User defined pipeline compare value or channel-updated capture value. A read or write to this register will clear the C1CC interrupt. Compare mode: An update of VAL will be transferred to VAL when the next VAL is zero and MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal. Capture mode: When CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by EDGE.

13.5.27 PC2CC Register (Offset = 108h) [Reset = 00000000h]

PC2CC is shown in Table 13-32.

Return to the Summary Table.

Pipeline Channel 2 Capture Compare

Table 13-32. PC2CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Pipeline Capture Compare value. User defined pipeline compare value or channel-updated capture value. A read or write to this register will clear the C2CC interrupt. Compare mode: An update of VAL will be transferred to VAL when the next VAL is zero and MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal. Capture mode: When CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by EDGE.

13.5.28 TGT Register (Offset = 13Ch) [Reset = 00000000h]

TGT is shown in Table 13-33.

Return to the Summary Table.

Target User defined counter target. A read or write to this register will clear the ZERO and TGT interrupt.

Table 13-33. TGT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	User defined counter target value.

13.5.29 C0CC Register (Offset = 140h) [Reset = 00000000h]

C0CC is shown in Table 13-34.

Return to the Summary Table.

Channel 0 Capture Compare

Table 13-34. C0CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture Compare value. User defined compare value or channel-updated capture value. A read or write to this register will clear the C0CC interrupt. Compare mode: VAL is compared against VAL and an event is generated as specified by CCACT when these are equal. Capture mode: The current counter value is stored in VAL when a capture event occurs. CCACT determines if VAL is a signal period or a regular capture value.

13.5.30 C1CC Register (Offset = 144h) [Reset = 00000000h]

C1CC is shown in Table 13-35.

Return to the Summary Table.

Channel 1 Capture Compare

Table 13-35. C1CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture Compare value. User defined compare value or channel-updated capture value. A read or write to this register will clear the C1CC interrupt. Compare mode: VAL is compared against VAL and an event is generated as specified by CCACT when these are equal. Capture mode: The current counter value is stored in VAL when a capture event occurs. CCACT determines if VAL is a signal period or a regular capture value.

13.5.31 C2CC Register (Offset = 148h) [Reset = 00000000h]

C2CC is shown in Table 13-36.

Return to the Summary Table.

Channel 2 Capture Compare

Table 13-36. C2CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture Compare value. User defined compare value or channel-updated capture value. A read or write to this register will clear the C2CC interrupt. Compare mode: VAL is compared against VAL and an event is generated as specified by CCACT when these are equal. Capture mode: The current counter value is stored in VAL when a capture event occurs. CCACT determines if VAL is a signal period or a regular capture value.

13.5.32 PTGTNC Register (Offset = 17Ch) [Reset = 00000000h]

PTGTNC is shown in Table 13-37.

Return to the Summary Table.

Pipeline Target No Clear Use this register to read or write to [PTGT.*] without clearing the ZERO and TGT interrupt.

Table 13-37. PTGTNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	A read or write to this register will not clear the TGT interrupt. If MODE != QDEC. Target value for next counter period. The timer copies VAL to VAL when VAL becomes 0. The copy does not happen when restarting the timer. This is useful to avoid period jitter in **PWM** applications with time-varying period, sometimes referenced as phase corrected PWM. If MODE = QDEC. The VAL is updated with VAL on IDX. VAL is not loaded into VAL when VAL becomes 0.

13.5.33 PC0CCNC Register (Offset = 180h) [Reset = 00000000h]

PC0CCNC is shown in Table 13-38.

Return to the Summary Table.

Pipeline Channel 0 Capture Compare No Clear

Table 13-38. PC0CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Pipeline Capture Compare value. User defined pipeline compare value or channel-updated capture value. A read or write to this register will not clear the C0CC interrupt. Compare mode: An update of VAL will be transferred to VAL when the next VAL is zero and MODE is different from DIS. This is useful for **PWM** generation and prevents jitter on the edges of the generated signal. Capture mode: When CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by EDGE.

13.5.34 PC1CCNC Register (Offset = 184h) [Reset = 00000000h]

PC1CCNC is shown in Table 13-39.

Return to the Summary Table.

Pipeline Channel 1 Capture Compare No Clear

Table 13-39. PC1CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Pipeline Capture Compare value. User defined pipeline compare value or channel-updated capture value. A read or write to this register will not clear the C1CC interrupt. Compare mode: An update of VAL will be transferred to VAL when the next VAL is zero and MODE is different from DIS. This is useful for **PWM** generation and prevents jitter on the edges of the generated signal. Capture mode: When CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by EDGE.

13.5.35 PC2CCNC Register (Offset = 188h) [Reset = 00000000h]

PC2CCNC is shown in Table 13-40.

Return to the Summary Table.

Pipeline Channel 2 Capture Compare No Clear

Table 13-40. PC2CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Pipeline Capture Compare value. User defined pipeline compare value or channel-updated capture value. A read or write to this register will not clear the C2CC interrupt. Compare mode: An update of VAL will be transferred to VAL when the next VAL is zero and MODE is different from DIS. This is useful for **PWM** generation and prevents jitter on the edges of the generated signal. Capture mode: When CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by EDGE.

13.5.36 TGTNC Register (Offset = 1BCh) [Reset = 00000000h]

TGTNC is shown in Table 13-41.

Return to the Summary Table.

Target No Clear Use this register to read or write to [TGT.*] without clearing the ZERO and TGT interrupt.

Table 13-41. TGTNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	User defined counter target value.

13.5.37 C0CCNC Register (Offset = 1C0h) [Reset = 00000000h]

C0CCNC is shown in Table 13-42.

Return to the Summary Table.

Channel 0 Capture Compare No Clear

Table 13-42. C0CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture Compare value. User defined compare value or channel-updated capture value. A read or write to this register will not clear the C0CC interrupt. Compare mode: VAL is compared against VAL and an event is generated as specified by CCACT when these are equal. Capture mode: The current counter value is stored in VAL when a capture event occurs. CCACT determines if VAL is a signal period or a regular capture value.

13.5.38 C1CCNC Register (Offset = 1C4h) [Reset = 00000000h]

C1CCNC is shown in Table 13-43.

Return to the Summary Table.

Channel 1 Capture Compare No Clear

Table 13-43. C1CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture Compare value. User defined compare value or channel-updated capture value. A read or write to this register will not clear the C1CC interrupt. Compare mode: VAL is compared against VAL and an event is generated as specified by CCACT when these are equal. Capture mode: The current counter value is stored in VAL when a capture event occurs. CCACT determines if VAL is a signal period or a regular capture value.

13.5.39 C2CCNC Register (Offset = 1C8h) [Reset = 00000000h]

C2CCNC is shown in Table 13-44.

Return to the Summary Table.

Channel 2 Capture Compare No Clear

Table 13-44. C2CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture Compare value. User defined compare value or channel-updated capture value. A read or write to this register will not clear the C2CC interrupt. Compare mode: VAL is compared against VAL and an event is generated as specified by CCACT when these are equal. Capture mode: The current counter value is stored in VAL when a capture event occurs. CCACT determines if VAL is a signal period or a regular capture value.

13.5.40 CLKCFG Register (Offset = 1000h) [Reset = 00000000h]

CLKCFG is shown in Table 13-45.

Return to the Summary Table.

Clock Enable Register

Table 13-45. CLKCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	ENABLE	R/W	0h	GPTimer main clock Enable

Chapter 14

System Timer (SysTimer)

This chapter discusses the features and configurations of the System Timer (SYSTIM) module.

14.1 Overview

SYSTIM is a 34-bit timer running at a resolution of 250 ns with a low range (about 1.2 hr) but high precision (of 250 ns) that can be used by both the Wi-Fi & BLE core and the system CPU. SYSTIM follows the RTC (Chapter 15) and can only be used in device ACTIVE state. The SYSTIM synchronizes with the RTC. This is done during start-up and continuously during ACTIVE state. When the device goes from SLEEP/SHUTDOWN to ACTIVE the value of the RTC time is loaded to SYSTIM with a resolution of 250 ns.

SYSTIM has two channels:

- Channel 0
  - Capture and compare options
  - Configurable for 1 µs or 250 ns resolution
  - Available for custom use-cases
- Channel 1
  - Reserved for TI software
  - Capture and compare options
  - Configurable for 1 µs resolution

14.2 Block Diagram

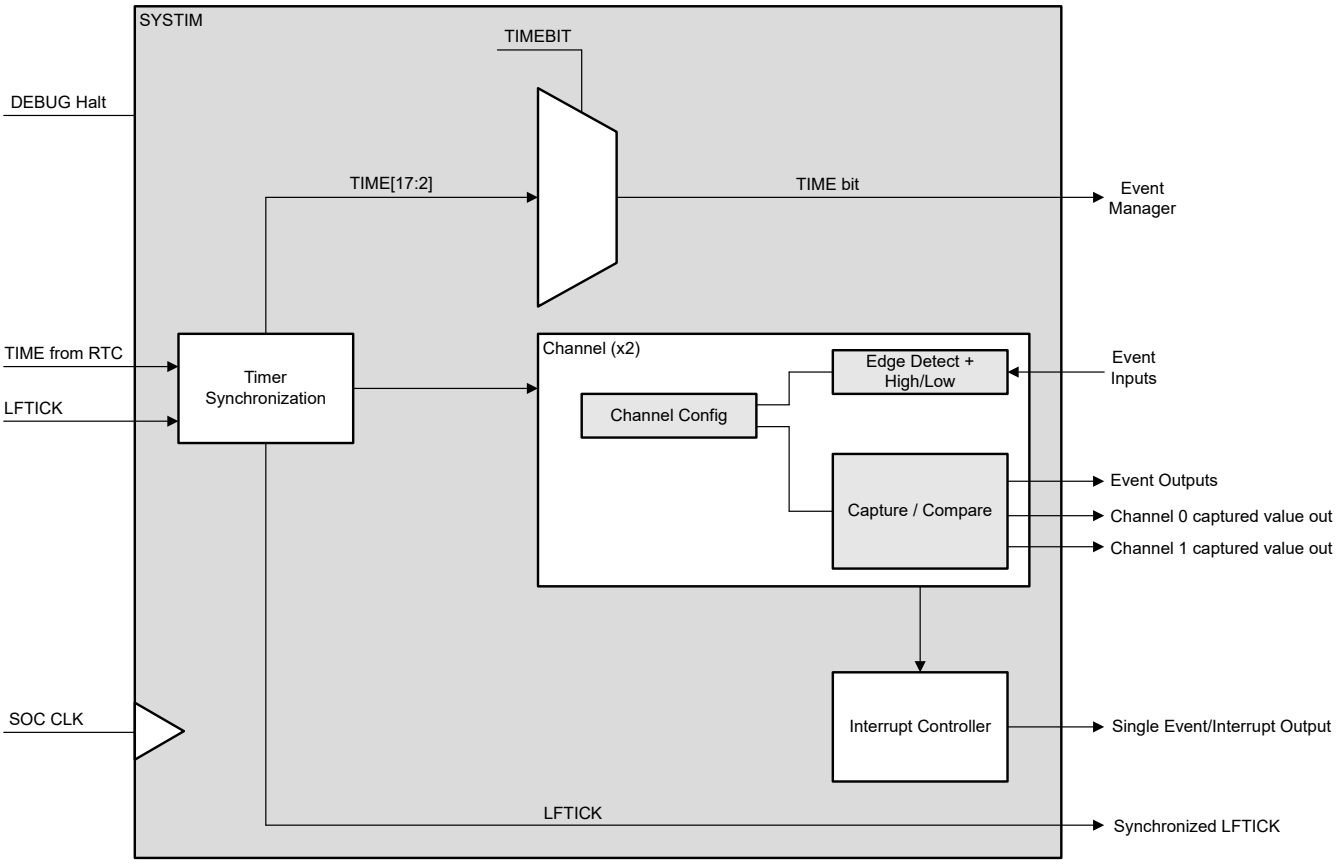

Figure 14-1. SYSTIM Block Diagram

14.3 Functional Description

14.3.1 Common Channel Features

14.3.1.1 Compare Mode

A channel is automatically armed in compare mode by writing any value to SYSTIM.CHnCC[31:0] DATA bit field.

Once programmed in compare mode the channel generates an event when SYSTIM time reaches the programmed value.

The SYSTIM channel generates an event immediately if the value programmed is within a certain limit in the past. This limit is 4 seconds in the past for 1 µs resolution channels. And the limit is 1 second in the past for 250 ns resolution channel.

14.3.1.2 Capture Mode

A channel can be armed in Capture mode by setting the SYSTIM.CHnCFG[0] MODE bit to 1.

In capture mode the channel captures the 32 bits of SYSTIM time based on the event which the channel receives. The resolution of these 32 bits is based on the type of channel which is being used. The capture can be configured on different edges of the input event . For more details refer to the SYSTIM.CHnCFG register.

By default a channel is disarmed after capture happens. The SYSTIM.CHnCFG[0] MODE bit is cleared to 0.

14.3.1.3 Additional Channel Arming Methods

In addition to the previously mentioned methods for arming a channel, a channel can be armed via programming the ARMSET register. When the SYSTIM.CHnCFG[0] MODE bit is 0 and SYSTIM.ARMSET[n] CHn bit is set for that channel, the channel is armed in compare mode and starts comparison based on the current CHnCC register value.

When SYSTIM.CHnCFG[3] REARM is set to 1, rearm is enabled. The channel remains in continuous capture mode. Otherwise the channel is in one-shot capture mode. Rearm is only valid for capture mode.

A channel can be disarmed by setting the SYSTIM.ARMCLR[n] CHn bit to 1. ARMCLR disarms the channel and resets the SYSTIM.CHnCFG[0] MODE bit to 0.

The CHnCCSR register can be written to load the channel with a value without triggering the channel to enter compare mode. Then ARMSET can be used to arm the channel in Compare mode by setting the ARMSET[n], provided the CHnCFG[0] MODE is zero.

14.3.2 Interrupts and Events

SYSTIM capture/compare events:

- SYSTIM event output:
  - One event output per channel + one combined event output for all the channels routed to the Event Manager.
  - Total of 2 event outputs. Only the combined event has a standard complement of MIS/RIS/IMASK/ ISET/ICLR/IMCLR/IMSET registers. RIS is automatically cleared when reading capture value or writing compare value.
    - The combined event also includes a timer overflow event. This event is asserted when time overflows and remain asserted till 4sec.
  - The event set within RIS can be cleared via ICLR, and also when any of the following occurs:
    - Reading from the capture register (this only occurs if the channel is in capture mode or disarmed).
    - Writing to the compare register.
    - Arming the channel in capture mode via writing CH n CFG.MODE bit to 1.
    - Arming the channel in capture mode via writing ARMSET n bit to 1, provided CH n CFG.MODE bit as 0.
  - Trigger past event
    - A compare event triggers immediately if 0 <= TIME-CMP < 2^22, in other words if the compare time is now or up to 1.048576s in the past for channel 0 (configured to 250 ns resolution), and up to 4.294s in the past for channel 1 (configured to 1 µs).
- SYSTIM event inputs:

- One event input per channel.
- Can be configured to capture on a configurable condition (rising edge, falling edge and both edges). This also generates a capture event output on the same channel, setting the RIS interrupt flag.
- Event input needs to be defined in the Event Manager by writing to SOC_AON.TMEVTCTL[5:0] SYSTIM0 bit field for SYSTIM channel 0 or SOC_AON.TMEVTCTL[13:8] SYSTIM1 bit field for SYSTIM channel 1.
- The SYSTIM.CHnCFG[2:1] INP bit field can be used to configure the capture condition.
  - If SYSTIM.CHnCFG[2:1] INP bit field = 0 then capture on the rising edge.
  - If SYSTIM.CHnCFG[2:1] INP bit field = 1 then capture on the falling edge.
  - If SYSTIM.CHnCFG[2:1] INP bit field = 2 then capture on both rising and falling edges.
- Software must arm a channel for capture, and a capture event automatically disarms the channel.

14.4 SYSRESOURCES Registers

Table 14-1 lists the memory-mapped registers for the SYSRESOURCES registers. All register offset addresses not listed in Table 14-1 should be considered as reserved locations and the register contents should not be modified.

Table 14-1. SYSRESOURCES Registers

Offset	Acronym	Register Name	Section
8h	SYSTIM_CTRL	System Timer Control	Section 14.4.1
400h	MEMSS_GENERAL	General Configuration	Section 14.4.2
404h	MEMSS_BUS_FAULT_RAW_STATUS	Bus Fault Status	Section 14.4.3

Complex bit access types are encoded to fit into small table cells. Table 14-2 shows the codes that are used for access types in this section.

Table 14-2. SYSRESOURCES Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

14.4.1 SYSTIM_CTRL Register (Offset = 8h) [Reset = 00000000h]

SYSTIM_CTRL is shown in Table 14-3.

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Table 14-3. SYSTIM_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	MEM_SYSTIM_ENCLK	R/W	0h	'1' - enable the reqeusets for the systim clk

14.4.2 MEMSS_GENERAL Register (Offset = 400h) [Reset = 00000000h]

MEMSS_GENERAL is shown in Table 14-4.

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Table 14-4. MEMSS_GENERAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6-4	MEMSS_BUS_FAULT_STATUS_MASKED	R	0h	'1' - Mask '0' - Do not mask
3	MEM_MEMSS_BUS_FAULT_MASK	R/W	0h	'1' - Mask '0' - Do not mask
2-0	RESERVED	R	0h	Reserved

14.4.3 MEMSS_BUS_FAULT_RAW_STATUS Register (Offset = 404h) [Reset = 00000000h]

MEMSS_BUS_FAULT_RAW_STATUS is shown in Table 14-5.

Return to the Summary Table.

Table 14-5. MEMSS_BUS_FAULT_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	MEMSS_BUS_FAULT_STATUS_RAW_RDCL	R	0h	HOST to config how long writing to mailbox can be delayed

14.5 SYSTIM Registers

Table 14-6 lists the memory-mapped registers for the SYSTIM registers. All register offset addresses not listed in Table 14-6 should be considered as reserved locations and the register contents should not be modified.

Table 14-6. SYSTIM Registers

Offset	Acronym	Register Name	Section
0h	DESC	Module Identification	Section 14.5.1
44h	IBM	Interrupt Mask	Section 14.5.2
48h	RIS	Interrupt Status Flags	Section 14.5.3
4Ch	MIS	Masked interrupt status	Section 14.5.4
50h	ISET	Interrupt Set	Section 14.5.5
54h	ICLR	Interrupt Clear	Section 14.5.6
58h	IMSET	Interrupt Mask Set	Section 14.5.7
5Ch	IMCLR	Interrupt Mask Clear	Section 14.5.8
60h	EMU	Emulation Control	Section 14.5.9
100h	TIME250N	Counter Low Value	Section 14.5.10
104h	TIME1U	System Timer Count	Section 14.5.11
108h	OUT	Output Values	Section 14.5.12
10Ch	CH0CFG	Channel Configuration	Section 14.5.13
110h	CH1CFG	Channel Configuration	Section 14.5.14
120h	CH0CC	Compare Value	Section 14.5.15
124h	CH1CC	Channel1 reg Value	Section 14.5.16
134h	TIMEBIT	System Timer Bit	Section 14.5.17
138h	KP	Proportional Gain	Section 14.5.18
13Ch	KI	Integral Gain Coefficient	Section 14.5.19
140h	STA	Timer Status	Section 14.5.20
144h	ARMSET	Arm Status Set	Section 14.5.21
148h	ARMCLR	Arm Clear Status	Section 14.5.22
14Ch	CH0CCSR	Channel Value Alias	Section 14.5.23
150h	CH1CCSR	Channel 1 Value	Section 14.5.24
1000h	CLKCFG	Clock Enable	Section 14.5.25

Complex bit access types are encoded to fit into small table cells. Table 14-7 shows the codes that are used for access types in this section.

Table 14-7. SYSTIM Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Rmodify	R modify	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

14.5.1 DESC Register (Offset = 0h) [Reset = 94431010h]

DESC is shown in Table 14-8.

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This register identifies the peripheral and its exact version.

Table 14-8. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	9443h	Module identifier MODID[15:0]. Used to uniquely identify this IP. See comment about derivation below 0h = Smallest value FFFFh = Highest possible value
15-12	STDIPOFF	R	1h	64 B standard IP MMR block (beginning with aggregated IRQ registers) 0: STDIP MMRs do not exist 1:15: These MMRs begin at offset 64*STDIPOFF from IP base address 0h = Smallest value Fh = Highest possible value
11-8	INSTIDX	R	0h	If multiple instances of IP exists in SOC, this field can identify the instance number 0-15 0h = Smallest value Fh = Highest possible value
7-4	MAJREV	R	1h	Major revision of IP 0-15 0h = Smallest value Fh = Highest possible value
3-0	MINREV	R	0h	Minor revision of IP 0-15. 0h = Smallest value Fh = Highest possible value

14.5.2 IBM Register (Offset = 44h) [Reset = 00000000h]

IBM is shown in Table 14-9.

Return to the Summary Table.

INTERRUPT BIT MASK Interrupt Mask. If a bit is cleared, then corresponding interrupt is masked.

Table 14-9. IBM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	OVFL	R/W	0h	Mask Timer Overflow Event in MIS register. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
5-2	RESERVED	R	0h	Reserved
1	EVT1	R/W	0h	Mask EVENT1 in MIS register. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
0	EVT0	R/W	0h	Mask EVENT0 in MIS register. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask

14.5.3 RIS Register (Offset = 48h) [Reset = 00000000h]

RIS is shown in Table 14-10.

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Raw interrupt status reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Table 14-10. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	OVFL	R	0h	Raw interrupt status for Timer Overflow EVENT. This bit is set to 1 when an event is received on Timer Ovreflow EVENT channel. 0h = Interrupt did not occur 1h = Interrupt occured
5-2	RESERVED	R	0h	Reserved
1	EVT1	R	0h	Raw interrupt status for EVENT1. This bit is set to 1 when an event is received on EVENT1 channel. 0h = Interrupt did not occur 1h = Interrupt occured
0	EVT0	R	0h	Raw interrupt status for EVENT0. This bit is set to 1 when an event is received on EVENT0 channel. 0h = Interrupt did not occur 1h = Interrupt occured

14.5.4 MIS Register (Offset = 4Ch) [Reset = 00000000h]

MIS is shown in Table 14-11.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Table 14-11. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	OVFL	R	0h	Mask Interrupt Status Timer Overflow Event in MIS register. 0h = Interrupt did not occur 1h = Interrupt occured
5-2	RESERVED	R	0h	Reserved
1	EVT1	R	0h	Mask interrupt status for EVENT1 0h = Interrupt did not occur 1h = Interrupt occured
0	EVT0	R	0h	Mask interrupt status for EVENT0 0h = Interrupt did not occur 1h = Interrupt occured

14.5.5 ISET Register (Offset = 50h) [Reset = 00000000h]

ISET is shown in Table 14-12.

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Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Table 14-12. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	OVFL	W	0h	Sets Timer Overflow EVENT in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
5-2	RESERVED	R	0h	Reserved
1	EVT1	W	0h	Sets channel1 EVENT in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
0	EVT0	W	0h	Sets channel0 EVENT in RIS 0h = Writing 0 has no effect 1h = Set Interrupt

14.5.6 ICLR Register (Offset = 54h) [Reset = 00000000h]

ICLR is shown in Table 14-13.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Table 14-13. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	OVFL	W	0h	Overflow 0h = Writing 0 has no effect 1h = Clear Interrupt
5-2	RESERVED	R	0h	Reserved
1	EVT1	W	0h	Clears EVENT1 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
0	EVT0	W	0h	Clears EVENT0 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt

14.5.7 IMSET Register (Offset = 58h) [Reset = 00000000h]

IMSET is shown in Table 14-14.

Return to the Summary Table.

Interrupt mask set. Writing a 1 to a bit in IMSET will set the related IMASK bit.

Table 14-14. IMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	OVFL	W	0h	Sets Timer Overflow Event. 0h = Writing 0 has no effect 1h = Set interrupt mask
5-2	RESERVED	R	0h	Reserved
1	EVT1	W	0h	Sets channel1 Event 0h = Writing 0 has no effect 1h = Set interrupt mask
0	EVT0	W	0h	Sets channel0 Event 0h = Writing 0 has no effect 1h = Set interrupt mask

14.5.8 IMCLR Register (Offset = 5Ch) [Reset = 00000000h]

IMCLR is shown in Table 14-15.

Return to the Summary Table.

Interrupt mask clear. Writing a 1 to a bit in IMCLR will clear the related IMASK bit.

Table 14-15. IMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	OVFL	W	0h	Clears Timer Overflow Event. 0h = Writing 0 has no effect 1h = Clear interrupt mask
5-2	RESERVED	R	0h	Reserved
1	EVT1	W	0h	Clears channel1 Event. 0h = Writing 0 has no effect 1h = Clear interrupt mask
0	EVT0	W	0h	Clears channel0 Event. 0h = Writing 0 has no effect 1h = Clear interrupt mask

14.5.9 EMU Register (Offset = 60h) [Reset = 00000000h]

EMU is shown in Table 14-16.

Return to the Summary Table.

This register can be used by the software developer to control the behavior of the peripheral relative to the CPU Halted input.

Table 14-16. EMU Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	HALT	R/W	0h	This bit controls peripheral behavior at CPU halt condition. 0h = Peripheral ignores the state of the CPU Halted input 1h = Peripheral freezes functionality immediately or at appropriate time when the CPU Halted input is asserted and resumes when it is deasserted

14.5.10 TIME250N Register (Offset = 100h) [Reset = 00000000h]

TIME250N is shown in Table 14-17.

Return to the Summary Table.

Systimer Counter Value[31:0]. Time with 250ns resolution from systimer

Table 14-17. TIME250N Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Counter Value. This is not writable while the systimer counter is enabled 0h = Smallest value FFFFFFFFh = Highest possible value

14.5.11 TIME1U Register (Offset = 104h) [Reset = 00000000h]

TIME1U is shown in Table 14-18.

Return to the Summary Table.

Systimer Counter Value[33:2]. Time with 1us resolution from systimer

Table 14-18. TIME1U Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Counter Value. This is not writable while the systimer counter is enabled 0h = Smallest value FFFFFFFFh = Highest possible value

14.5.12 OUT Register (Offset = 108h) [Reset = 00000000h]

OUT is shown in Table 14-19.

Return to the Summary Table.

SYSTIMER'S Channel Output Event Values

Table 14-19. OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	OUT1	R	0h	Output Value of channel 1. 0h = Event did not occur. 1h = Event occured
0	OUT0	R	0h	Output Value of channel 0. 0h = Event did not occur. 1h = Event occured

14.5.13 CH0CFG Register (Offset = 10Ch) [Reset = 00000000h]

CH0CFG is shown in Table 14-20.

Return to the Summary Table.

SYSTIMER channel 0 configuration

Table 14-20. CH0CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	RES	R/W	0h	This bit decides the RESOLUTION of the channel that will be used. 0h = Channel Works in Timer's 1us Resolution. 1h = Channel Works in Timer's 250ns resolution
3	REARM	R/W	0h	When Rearm is enabled the channel remains in continuous capture mode. Otherwise it'll be in One shot capture mode. Rearm is only valid for capture mode. 0h = Re Arm is disabled 1h = Re arm is enabled
2-1	INP	R/W	0h	Decides the channel input signal's mode. Setting the Value as 2'b11 selects the Rise Function. 0h = Capture on rising edge 1h = Capture on Falling Edge 2h = Capture on both Edge
0	MODE	R/W	0h	Decides the channel mode. 0h = Channel is disabled 1h = Channel is in capture mode

14.5.14 CH1CFG Register (Offset = 110h) [Reset = 00000000h]

CH1CFG is shown in Table 14-21.

Return to the Summary Table.

SYSTIMER channel 1 configuration

Table 14-21. CH1CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	REARM	R/W	0h	When Rearm is enabled the channel remains in continous capture mode. Otherwise it'll be in One shot capture mode. Rearm is only valid for capture mode. 0h = Re Arm is disabled 1h = Re arm is enabled
2-1	INP	R/W	0h	Decides the channel input signal's mode. Setting the Value as 2'b11 selects the Rise Function 0h = Capture on rising edge 1h = Capture on Falling Edge 2h = Capture on both Edge
0	MODE	R/W	0h	Decides the channel mode. 0h = Channel is disabled 1h = Channel is in capture mode

14.5.15 CH0CC Register (Offset = 120h) [Reset = 00000000h]

CH0CC is shown in Table 14-22.

Return to the Summary Table.

System Timer Channel 0 Capture/Compare Register. This Register when written with any compare value will arm the channel to work in compare mode.

Table 14-22. CH0CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture/compare value 0h = Smallest value FFFFFFFFh = Highest possible value

14.5.16 CH1CC Register (Offset = 124h) [Reset = 00000000h]

CH1CC is shown in Table 14-23.

Return to the Summary Table.

System Timer Channel 1 Capture/Compare Register. This Register when written with any compare value will arm the channel to work in compare mode.

Table 14-23. CH1CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture/compare value 0h = Smallest value FFFFFFFFh = Highest possible value

14.5.17 TIMEBIT Register (Offset = 134h) [Reset = 00000000h]

TIMEBIT is shown in Table 14-24.

Return to the Summary Table.

This Register will be used to specify which TIME bit is required by LGPT to be forwarded from SYSTIMER.

Table 14-24. TIMEBIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	The corresponding bit will have value '1' rest should be '0'. If more than one bit is asserted, output is "or" of all the bits. 0h = No bit is forwarded to the event fabric. 1h = Bit2 is forwarded to the event fabric. 2h = Bit3 is forwarded to the event fabric. 4h = Bit4 is forwarded to the event fabric. 8h = Bit5 is forwarded to the event fabric. 10h = Bit6 is forwarded to the event fabric. 20h = Bit7 is forwarded to the event fabric. 40h = Bit8 is forwarded to the event fabric. 80h = Bit9 is forwarded to the event fabric. 100h = Bit10 is forwarded to the event fabric. 200h = Bit11 is forwarded to the event fabric. 400h = Bit12 is forwarded to the event fabric. 800h = Bit13 is forwarded to the event fabric. 1000h = Bit14 is forwarded to the event fabric. 2000h = Bit15 is forwarded to the event fabric. 4000h = Bit16 is forwarded to the event fabric. 8000h = Bit17 is forwarded to the event fabric.

14.5.18 KP Register (Offset = 138h) [Reset = 00000004h]

KP is shown in Table 14-25.

Return to the Summary Table.

PI filter's Proportional Gain Value

Table 14-25. KP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	VAL	R/W	4h	Proportional Error is left shifted by this value. 0h = Smallest value Fh = Highest possible value

14.5.19 KI Register (Offset = 13Ch) [Reset = 00000001h]

KI is shown in Table 14-26.

Return to the Summary Table.

PI filter's Accumulator's Gain Value

Table 14-26. KI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	VAL	R/W	1h	Accumulated Error is left shifted by this value. 0h = Smallest value Fh = Highest possible value

14.5.20 STA Register (Offset = 140h) [Reset = 00000010h]

STA is shown in Table 14-27.

Return to the Summary Table.

STATUS This is the system timer status register.

Table 14-27. STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	SYNCUP	R	1h	This bit indicates the status of resyncup of systimer with RTC. The bitfield has a reset value of '1' , as out of reset the systimer syncs up with RTC, after the first_synced_lftick occurs the SYNCUP bit goes to zero. 0h = SYNC UP with RTC is not happening 1h = Any write to STATUS register, triggers the SYNCUP with RTC and this bit is set.
3-1	RESERVED	R	0h	Reserved
0	VAL	R	0h	This bit indicates if the system time is initialized and running. 0h = system timer is not running. 1h = system timer is running

14.5.21 ARMSET Register (Offset = 144h) [Reset = 00000000h]

ARMSET is shown in Table 14-28.

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ARMSET on read gives out the status of the 2 channels 1. Channel state UNARMED returns 0 2. Channel state CAPTURE or COMPARE returns 1 A write to ARMSET has for each channel the following effect: 1. If ARMSTA[x]==0 -> no effect 2. If ARMSTA[x]==1 and channel x is in CAPTURE state then no effect on the channel 3. Else Set channel in COMPARE mode using existing CHxVAL value

Table 14-28. ARMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	CH1	R/W	0h	Arming Channel 1 for either compare or capture operation. 0h = No effect on the channel 1h = if channel 1 is in CAPTURE state then no effect on the channel Else ; Set channel in COMPARE mode using existing CH1VAL value
0	CH0	R/W	0h	Arming Channel 0 for either compare or capture operation. 0h = No effect on the channel 1h = if channel 0 is in CAPTURE state then no effect on the channel 3. Else ; Set channel in COMPARE mode using existing CH0VAL value

14.5.22 ARMCLR Register (Offset = 148h) [Reset = 00000000h]

ARMCLR is shown in Table 14-29.

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ARMCLR on read gives out the status of the 2 channels 1. Channel state UNARMED returns 0 2. Channel state CAPTURE or COMPARE returns 1 A write to ARMCLR has for each channel the following effect: 1. If ARMCLR[x]==0 no effect 2. Else Set channel in UNARMED state without triggering event unless a compare/capture event happens in the same cycle

Table 14-29. ARMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	CH1	R/W	0h	Disarming Channel 1 0h = No effect on the channel 1h = Set channel in UNARMED state without triggering event unless a compare/capture event happens in the same cycle
0	CH0	R/W	0h	Disarming Channel 0 0h = No effect on the channel 1h = Set channel in UNARMED state without triggering event unless a compare/capture event happens in the same cycle

14.5.23 CH0CCSR Register (Offset = 14Ch) [Reset = 00000000h]

CH0CCSR is shown in Table 14-30.

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Save/restore alias registers Channel 0. i. A read to CH0SR behaves exactly as a read to CH0VAL. A write to CH0SR sets CH0VAL value of register without affecting channel state or configuration

Table 14-30. CH0CCSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture/compare value 0h = Smallest value FFFFFFFFh = Highest possible value

14.5.24 CH1CCSR Register (Offset = 150h) [Reset = 00000000h]

CH1CCSR is shown in Table 14-31.

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Save/restore alias registers Channel 1. i. A read to CH1SR behaves exactly as a read to CH1VAL. A write to CH1SR sets CH1VAL value of register without affecting channel state or configuration.

Table 14-31. CH1CCSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture/compare value 0h = Smallest value FFFFFFFFh = Highest possible value

14.5.25 CLKCFG Register (Offset = 1000h) [Reset = 00000000h]

CLKCFG is shown in Table 14-32.

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Table 14-32. CLKCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EN	Rmodify/W	0h	ENABLE '1' - enable systimer clk '0' - disable systimer clk 0h = Smallest value FFFFFFFFh = Highest possible value

Chapter 15

Real-Time Clock (RTC)

This chapter describes the functionality of the Real Time Clock (RTC) module.

15.1 Introduction

The RTC is a 67-bit, 2-channel timer running on the LFCLK system clock (see Section 7.3.2.2). The RTC is active in SLEEP and ACTIVE power states. When the device enters SHUTDOWN state the RTC is reset.

RTC is reset when device resets (reset pin, WDT, debug request reset). The RTC is not reset when Host MCU is executing SOC AON reset.

The RTC accumulates time elapsed since reset on each LFCLK. For better accuracy the source LFCLK is averaged by the RTC filter, generating clock signals LFTICK and LFINC. The RTC counter is incremented by LFINC at a rate of 32.768 kHz. LFINC indicates the period of LFCLK in µs, with an additional granularity of 16 fractional bits.

The counter can be read from two 32-bit registers. RTC.TIME8U has a range of approximately 9.5 hours with an LSB representing 8 microseconds. RTC.TIME524M has a range of approximately 71.4 years with an LSB representing 524 milliseconds.

There is hardware synchronization between the system timer (SYSTIM) and the RTC so that the multi-channel and higher resolution SYSTIM remain in synchronization with the RTC's time base.

The RTC has two channels: one compare channel and one capture channel and is capable of waking the device out of the sleep power state. The RTC compare channel is typically used only by system software and only during the sleep power state.

15.2 Block Diagram

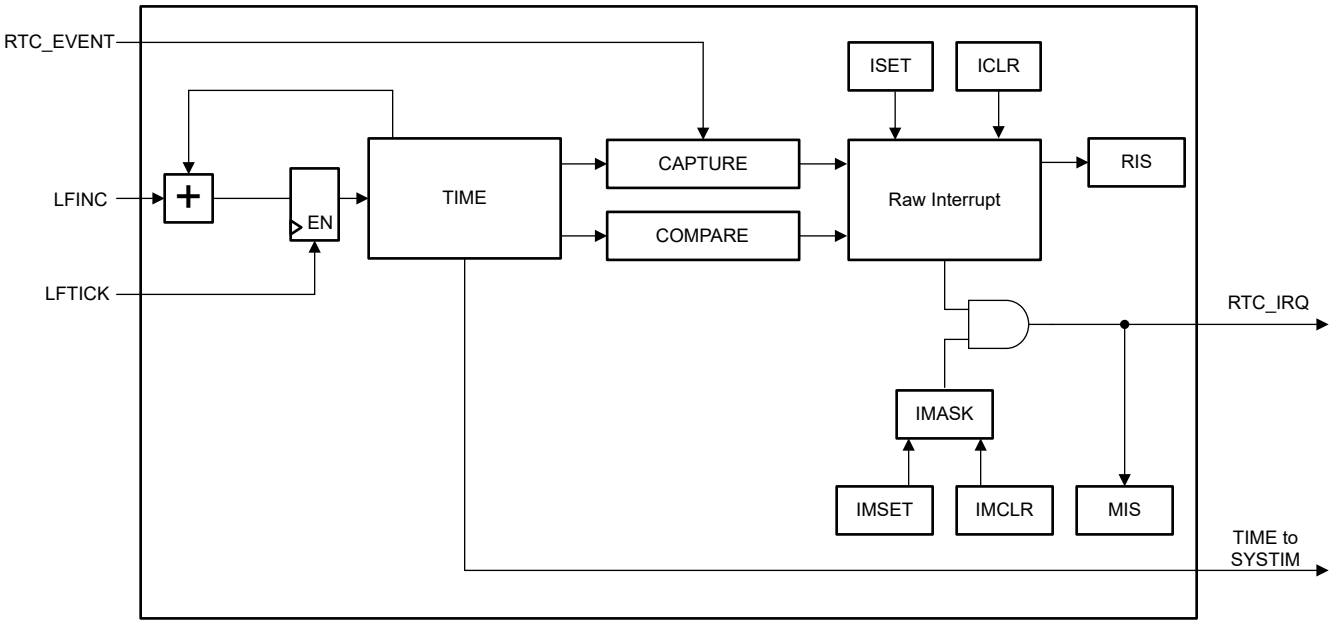

Figure 15-1. RTC Block Diagram

15.3 Interrupts and Events

15.3.1 Input Event

RTC has one capture input event from the AON/AAON Event Manager (see Section 5.4). The capture event is selected by writing SOC_AON.TMEVTCTL[22:16] RTC bit field. The capture can be on a rising or falling edge. This is configured by writing or clearing the RTC.CH1CFG[0] EDGE bit.

- RTC.CH1CFG[0] EDGE = 0 is rising edge configuration. This is the reset value for this bit.
- RTC.CH1CFG[0] EDGE = 1 is falling edge configuration.

15.3.2 Output Event

The RTC has one combined interrupt request event output. See Section 5.4 for more information on interrupt and event handling.

Interrupt flags for the combined interrupt can be read from the RTC.MIS register. Interrupts can be cleared by writing to the RTC.ICLR register. Interrupt status for the capture channel is cleared by reading the RTC.CH1CC8U[20:0] VAL bit field. Interrupt status for the compare channel is cleared by writing to the RTC.CH0CC8U[31:0] VAL bit field.

15.3.3 Arming and Disarming Channels

RTC.ARMSET and RTC.ARMCLR are provided as additional methods of arming and disarming channels. A read of either the RTC.ARMCLR or RTC.ARMSET register returns the armed status of each channel. If the capture or compare channel is armed, setting the corresponding bit in the RTC.ARMCLR register to 1 sets the channel in the unarmed state without triggering an event (unless a compare or capture event happens in the same cycle).

If the channel is not armed, writing the RTC.ARMSET[1] CH1 bit arms the capture channel. Writing to RTC.ARMSET[0] CH0 has no effect on the compare channel. The compare channel is automatically armed when a value is written to the RTC.CH0CCxx register(s).

15.4 CAPTURE and COMPARE Configurations

RTC has two channels.

15.4.1 CHANNEL 0 - COMPARE CHANNEL

The compare channel has the option to get armed via 3 different resolutions of time - 250ns, 1us and 8us.

The compare channel:

- Is armed in 250ns resolution when a compare value is written to the RTC.CH0CC250N register.
- Is armed in 1us resolution when a compare value is written to the RTC.CH0CC1U register.
- Is armed in 8us resolution when a compare value is written to the RTC.CH0CC8U register.

The compare channel is disarmed when a compare event occurs. Although the CH0CC250N/CH0CC1U registers are arming the channel in compare mode, the comparison still occurs w.r.t the TIME8U register register, Hence the events are generated every 32Khz based on the TIME8U register.

- RTC generates an immediate event if the compare value is between now and 1 second in the past
- Otherwise, RTC generates a compare event when the difference between the compare value and RTC value is within 32 µs.

15.4.2 CHANNEL 1 - CAPTURE CHANNEL

The capture event is selected by writing SOC_AON.TMEVTCTL[22:16] RTC bit field. Event capture can occur on either the rising or falling edge of the event by setting or clearing the RTC.CH1CFG[0] EDGE bit. Capture is armed by setting the RTC.ARMSET[1] CH1 bit. Once capture is armed the RTC.CH1CC8U[20:0] bit field is updated with the value from the RTC.TIME8U[31:0] VAL bit field at the time the capture event occurs.

15.5 RTC Registers

Table 15-1 lists the memory-mapped registers for the RTC registers. All register offset addresses not listed in Table 15-1 should be considered as reserved locations and the register contents should not be modified.

Table 15-1. RTC Registers

Offset	Acronym	Register Name	Section
0h	DESC	Module Description	Section 15.5.1
4h	CTL	RTC control Register	Section 15.5.2
8h	ARMSET	Interrupt mask	Section 15.5.3
Ch	ARMCLR	Interrupt mask	Section 15.5.4
10h	TIME250N	RTC Lower Time Slice	Section 15.5.5
14h	TIME1U	RTC Lower Time Slice	Section 15.5.6
18h	TIME8U	RTC Lower Time Slice	Section 15.5.7
1Ch	TIME524M	RTC Upper Time Slice	Section 15.5.8
20h	CH0CC250N	Channel0 compare value	Section 15.5.9
24h	CH0CC1U	Channel0 compare value	Section 15.5.10
28h	CH0CC8U	Channel0 compare value	Section 15.5.11
38h	CH1CC8U	channel1 capture Value	Section 15.5.12
3Ch	CH1CFG	channel1 Input Configuration	Section 15.5.13
44h	IMASK	Interrupt mask	Section 15.5.14
48h	RIS	Raw interrupt status	Section 15.5.15
4Ch	MIS	Masked interrupt status	Section 15.5.16
50h	ISET	Interrupt set	Section 15.5.17
54h	ICLR	Interrupt clear	Section 15.5.18
58h	IMSET	Interrupt mask set	Section 15.5.19
5Ch	IMCLR	Interrupt clear	Section 15.5.20
60h	EMU	Emulation	Section 15.5.21
68h	DTIME	RTC Upper Time Slice	Section 15.5.22

Complex bit access types are encoded to fit into small table cells. Table 15-2 shows the codes that are used for access types in this section.

Table 15-2. RTC Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

15.5.1 DESC Register (Offset = 0h) [Reset = 64421010h]

DESC is shown in Table 15-3.

Return to the Summary Table.

Description Register. This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 15-3. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	6442h	Module identifier used to uniquely identify this IP.
15-12	STDIPOFF	R	1h	Standard IP MMR block offset. Standard IP MMRs are the set of from aggregated IRQ registers till DTB. 0: Standard IP MMRs do not exist 0x1-0xF: Standard IP MMRs begin at offset of (64*STDIPOFF from the base IP address)
11-8	INSTIDX	R	0h	IP Instance ID number. If multiple instances of IP exist in the device, this field can identify the instance number (0-15).
7-4	MAJREV	R	1h	Major revision of IP (0-15).
3-0	MINREV	R	0h	Minor revision of IP (0-15).

15.5.2 CTL Register (Offset = 4h) [Reset = 00000000h]

CTL is shown in Table 15-4.

Return to the Summary Table.

RTC Control register. This register controls resetting the of RTC counter

Table 15-4. CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RST	W1C	0h	RTC counter reset. Writing 1 to this bit will reset the RTC counter, and cause it to resume counting from 0x0 0h = No effect 1h = Reset the timer.

15.5.3 ARMSET Register (Offset = 8h) [Reset = 00000000h]

ARMSET is shown in Table 15-5.

Return to the Summary Table.

RTC channel mode set register. Read to each bit field of this register provides the current channel mode. - Read of 1'b0 indicates the channel is unarmed. - Read of 1'b1 indicates the channel is either in capture or compare mode. A write to each bitfield of this register the following effect: - Write of 1'b0 has no effect on channel mode. - Write of 1'b1 has no effect on the compare channel. While write of 1'b1 for capture channel will arm it in capture mode if it is disabled.

Table 15-5. ARMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	CH1	R/W	0h	Arming Channel 1 for capture operation. 0h = No effect on the channel 1h = Enable the Channel 1 for capture operation
0	CH0	R/W	0h	No effect on arming the channel. Read will give the status of the Channel 0. 0h = No effect on the channel 1h = No effect on the compare channel

15.5.4 ARMCLR Register (Offset = Ch) [Reset = 00000000h]

ARMCLR is shown in Table 15-6.

Return to the Summary Table.

RTC channel mode clear register. Read to each bit field of this register provides the current channel mode. - Read of 1'b0 indicates the channel is unarmed. - Read of 1'b1 indicates the channel is either in capture or compare mode. A write to each bitfield of this register the following effect: - Write of 1'b0 has no effect on channel mode. - Write of 1'b1 for capture/compare channel will disarm it without triggering event unless a compare/capture event happens in the same cycle.

Table 15-6. ARMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	CH1	R/W	0h	Disarming Channel 1 0h = No effect on the channel 1h = Set channel in UNARMED state without triggering event unless a capture event happens in the same cycle
0	CH0	R/W	0h	Disarming Channel 0 0h = No effect on the channel 1h = Set channel in UNARMED state without triggering event unless a compare event happens in the same cycle

15.5.5 TIME250N Register (Offset = 10h) [Reset = 00000000h]

TIME250N is shown in Table 15-7.

Return to the Summary Table.

RTC Time value register. 32-bit unsigned integer representing [29:-2] time slice of the real time clock counter. The counter runs on **LFCLK**. This field has a resolution of 250ns, and range of about 17.8 minutes.

Table 15-7. TIME250N Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Unsigned integer representing [34:3]slice of real time counter.

15.5.6 TIME1U Register (Offset = 14h) [Reset = 00000000h]

TIME1U is shown in Table 15-8.

Return to the Summary Table.

RTC Time value register. 32-bit unsigned integer representing [31:0] time slice of the real time clock counter. The counter runs on **LFCLK**. This field has a resolution of 1us, and range of about 1.19 hours.

Table 15-8. TIME1U Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Unsigned integer representing [34:3]slice of real time counter.

15.5.7 TIME8U Register (Offset = 18h) [Reset = 00000000h]

TIME8U is shown in Table 15-9.

Return to the Summary Table.

RTC Time value register. 32-bit unsigned integer representing [34:3] time slice of the real time clock counter. The counter runs on **LFCLK**. This field has a resolution of 8us, and range of about 9.5 hours.

Table 15-9. TIME8U Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Unsigned integer representing [34:3]slice of real time counter.

15.5.8 TIME524M Register (Offset = 1Ch) [Reset = 00000000h]

TIME524M is shown in Table 15-10.

Return to the Summary Table.

RTC time value register. 32-bit unsigned integer representing [50:19] time slice of the real time clock counter. This field has a resolution of about 0.5s and a range of about 71.4 years.

Table 15-10. TIME524M Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Unsigned integer representing. [50:19]slice of real time counter.

15.5.9 CH0CC250N Register (Offset = 20h) [Reset = 00000000h]

CH0CC250N is shown in Table 15-11.

Return to the Summary Table.

Channel 0 compare value with 250ns resolution. A read to this register returns the value {CH0CC8U[29:3], 5b'0} A write to this register arms the channel in compare mode. Event would occur at the same time +/ Tlfclk/2 on the RTC as if it was written to SYSTIM.

Table 15-11. CH0CC250N Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	RTC Channel 0 compare value. This value is compared against VAL. A Channel 0 event is generated when VAL value reaches or exceeds this compare value.

15.5.10 CH0CC1U Register (Offset = 24h) [Reset = 00000000h]

CH0CC1U is shown in Table 15-12.

Return to the Summary Table.

Channel 0 compare value with 1us resolution. A read to this register returns the value {CH0CC8U[31:3], 3b'0} A write to this register arms the channel in compare mode. Event would occur at the same time +/ Tlfclk/2 on the RTC as if it was written to SYSTIM.

Table 15-12. CH0CC1U Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	RTC Channel 0 compare value. This value is compared against VAL. A Channel 0 event is generated when VAL value reaches or exceeds this compare value.

15.5.11 CH0CC8U Register (Offset = 28h) [Reset = 00000000h]

CH0CC8U is shown in Table 15-13.

Return to the Summary Table.

Channel 0 compare value. A write to this register automatically enables the channel to trigger an event when RTC timer reaches the programmed value or if the programmed value is 1 sec in the past.

Table 15-13. CH0CC8U Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	RTC Channel 0 compare value. This value is compared against VAL. A Channel 0 event is generated when VAL value reaches or exceeds this compare value.

15.5.12 CH1CC8U Register (Offset = 38h) [Reset = 00000000h]

CH1CC8U is shown in Table 15-14.

Return to the Summary Table.

Channel 1 capture value. This register captures the RTC time slice [34:3] on each selected edge of the capture event when the CH1 = 1.

Table 15-14. CH1CC8U Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20-0	VAL	R	0h	VAL captured value at the last selected edge of capture event.

15.5.13 CH1CFG Register (Offset = 3Ch) [Reset = 00000000h]

CH1CFG is shown in Table 15-15.

Return to the Summary Table.

Channel 1 configuration register. This register can be used to select the capture edge for generating the capture event.

Table 15-15. CH1CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EDGE	R/W	0h	Edge detect configuration for capture source 0h = Rising Edge. 1h = Falling Edge.

15.5.14 IMASK Register (Offset = 44h) [Reset = 00000000h]

IMASK is shown in Table 15-16.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Table 15-16. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	EV1	R/W	0h	Channel 1 Event Interrupt Mask. 0h = Clear Interrupt Mask 1h = Enable Interrrupt Mask
0	EV0	R/W	0h	Channel 0 Event Interrupt Mask. 0h = Disable Interrupt Mask 1h = Enable Interrupt Mask

15.5.15 RIS Register (Offset = 48h) [Reset = 00000000h]

RIS is shown in Table 15-17.

Return to the Summary Table.

Interrupt mask. This register selects interrupt sources which are allowed to pass from [RIS.*] to [MIS.*] when the corresponding bit-fields are set to 1.

Table 15-17. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	EV1	R	0h	Raw interrupt status for Channel 1 event. This bit is set to 1 when a capture event is received on Channel 1. This bit will be cleared when the bit in EV1 is set to 1 or when the captured time value is read from the [CH1CC8U.*] register. 0h = Interrupt did not occur 1h = Interrupt occured
0	EV0	R	0h	Raw interrupt status for Channel 0 event. This bit is set to 1 when a compare event occurs on Channel 0. This bit will be cleared. When the corresponding bit in EV0 is set to 1. Or when a new compare value is written in [CH0CC8U.*] register 0h = Interrupt did not occur 1h = Interrupt occured

15.5.16 MIS Register (Offset = 4Ch) [Reset = 00000000h]

MIS is shown in Table 15-18.

Return to the Summary Table.

Masked interrupt status. This register is simply a bitwise AND of the contents of [IMASK.*] and RIS.*] registers. A flag set in this register can be cleared by writing 1 to the corresponding [ICLR.*] register bit.

Table 15-18. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	EV1	R	0h	Masked interrupt status for channel 1 event. 0h = Interrupt did not occur 1h = Interrupt occured
0	EV0	R	0h	Masked interrupt status for channel 0 event. 0h = Interrupt did not occur 1h = Interrupt occured

15.5.17 ISET Register (Offset = 50h) [Reset = 00000000h]

ISET is shown in Table 15-19.

Return to the Summary Table.

Interrupt set register. This register can used by software for diagnostics and safety checking purposes. Writing a 1 to a bit in this register will set the event and the corresponding [RIS.*] bit also gets set. If the corresponding [IMASK.*] bit is set, then the corresponding [MIS.*] register bit also gets set.

Table 15-19. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	EV1	W	0h	Set Channel 1 event Interrupt. 0h = Writing 0 has no effect 1h = Set interrupt
0	EV0	W	0h	Set Channel 0 event Interrupt. 0h = Writing 0 has no effect 1h = Set interrupt

15.5.18 ICLR Register (Offset = 54h) [Reset = 00000000h]

ICLR is shown in Table 15-20.

Return to the Summary Table.

Interrupt clear register. This register allows software to clear interrupts. Writing a 1 to a bit in this register will clear the event and the corresponding [RIS.*] bit also gets cleared. If the corresponding [IMASK.*] bit is set, then the corresponding [MIS.*] register bit also gets cleared.

Table 15-20. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	EV1	W	0h	Clears channel 1 event interrupt. 0h = Writing 0 has no effect 1h = Clear Interrupt
0	EV0	W	0h	Clears channel 0 event interrupt. 0h = Writing 0 has no effect 1h = Clear Interrupt.

15.5.19 IMSET Register (Offset = 58h) [Reset = 00000000h]

IMSET is shown in Table 15-21.

Return to the Summary Table.

Interrupt mask set register. Writing a 1 to a bit in this register will set the corresponding [IMASK.*] bit.

Table 15-21. IMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	EV1	W	0h	Set channel 1 event interrupt mask. 0h = Writing 0 has no effect 1h = Set interrupt mask
0	EV0	W	0h	Set channel 0 event interrupt mask. 0h = Writing 0 has no effect 1h = Set interrupt mask

15.5.20 IMCLR Register (Offset = 5Ch) [Reset = 00000000h]

IMCLR is shown in Table 15-22.

Return to the Summary Table.

Interrupt mask clear register. Writing a 1 to a bit in this register will clear the corresponding [IMASK.*] bit.

Table 15-22. IMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	EV1	W	0h	Clears Channel 1 event interrupt mask. 0h = Writing 0 has no effect 1h = Clear Interrupt Mask
0	EV0	W	0h	Clears Channel 0 event interrupt mask. 0h = Writing 0 has no effect 1h = Clear Interrupt Mask

15.5.21 EMU Register (Offset = 60h) [Reset = 00000000h]

EMU is shown in Table 15-23.

Return to the Summary Table.

Emulation control register. This register controls the behavior of the IP related to core halted input.

Table 15-23. EMU Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	HALT	R/W	0h	Halt control. 0h = Free run option. The IP ignores the state of the core halted input. 1h = Freeze option. The IP freezes functionality when the core halted input is asserted, and resumes when it is deasserted. The freeze can either be immediate or after the IP has reached a boundary from where it can resume without corruption.

15.5.22 DTIME Register (Offset = 68h) [Reset = 00000000h]

DTIME is shown in Table 15-24.

Return to the Summary Table.

A delta time mechanism is implemented for RTC that allows the TIME value to be adjusted under software control. This is used by boot code to perform the compensation for reset duration (accomplished by adding MMR write to FCFG.generalTrims copylist to avoid ROM changes) DTIME format is: [31]: E (exponent) [30:0] M (mantissa) TIME[50:-2] is adjusted by TIME += sxt(M[30:0], 53) * 2^{22*E}. In other words: (E==0): TIME is adjusted by M * 250 ns (range +/-134 s) (E==1): TIME is adjusted by M * 1.049 s (range +/- 35.7 yr)

Table 15-24. DTIME Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved

Chapter 16

General Purpose Input/Output (GPIOs)

This chapter describes the input/output multiplexer (IO Mux) and the general-purpose inputs and outputs (GPIOs).

16.1 Introduction

The I/O Mux configures I/O pins and maps peripheral signals to physical pins (GPIOx). This chapter explains the I/O Mux functions and gives examples on how to map peripheral functions to the pins chosen by the user.

- Each pin can be mapped to a specific set of peripherals using IOMUX.GPIOn.PCFG register
- GPIOn (GPIO0 to GPIO44) are the logical names of the different I/O pins on the specific package, see the device specific data sheet for more information on package pin designation
- 8 of these GPIOs also have analog capabilities
- Pins can also be mapped to the digital test bus (DTB) to bring out clocks or physical signals like interrupts
- The device-specific data sheet provides:
  - Mapping between GPIOn and pins for the different packages
  - Peripheral pin mapping

16.2 Block Diagram

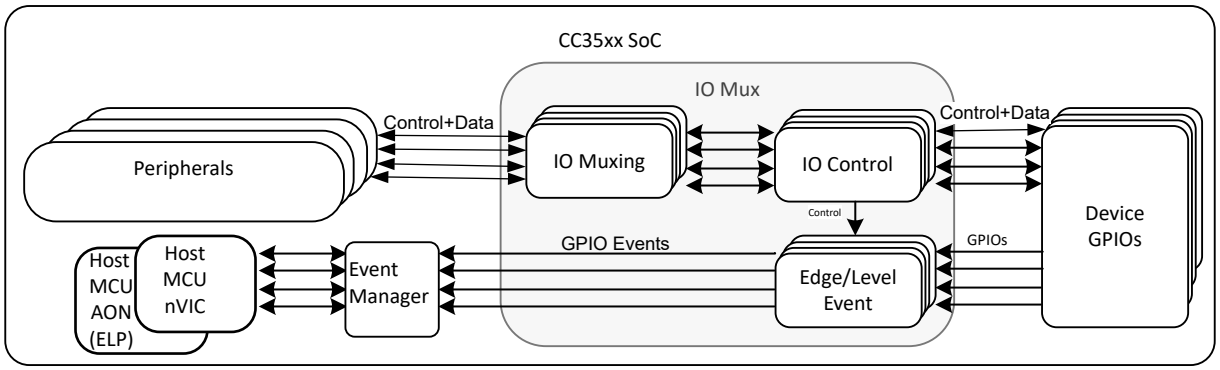

Figure 16-1. IO Mux Simplified Block Diagram

16.3 I/O Mapping and Configuration

Each peripheral with pin functions can be mapped to a specific set of pins. Refer to the device specific data sheet for the possible mappings.

16.3.1 Basic I/O Mapping

To map a peripheral function to a GPIOn, where n can range from 0 to 44, set IOMUX.GPIOn.PCFG to the value that represents the target function. For example, to set GPIO0 to the base function (GPIO) set IOMUX.GPIOn.PCFG = 0x2.

16.3.2 Pin Mapping

See the device specific data sheet for peripheral and I/O mapping and capability.

16.4 Edge Detection

The IO Mux supports detection of rising, falling, or both rising and falling edges.

When an edge is detected on a GPIO, the IO Mux publishes an event to the AON event manager if IOMUX.ECTL[1:0] EVTDETCFG bit field is configured to publish the event. Only one GPIOn can be selected to generate an event on the AON event manager. The event flag is cleared by the user by clearing IOMUX.GPIOnECTL[3] CLR.

The IO Mux can also generate a wake-up from standby signal to PRCM on edge detection by setting in the PRCM registers. Any or all GPIOn can be selected to generate a wake-up from standby on edge detection.

Note

Care must be taken to ensure that spurious edges are not generated while configuring edge detection feature. The recommended sequence is

1. Write all the IOMUX.GPIOn bit fields for a GPIO except for IOMUX.GPIOn[1:0] EVTDETCFG and IOMUX.GPIOnCFG[11] IE. These fields are left cleared to 0.
2. Then, write the IE bit field
3. Finally, write the EVTDETCFG bit field

16.5 GPIO

The GPIO is a general-purpose input/output module that allows software to write to and read from the GPIOs. GPIO supports up to 37 programmable I/O pins. These pins are configured by the IO Mux module. To modify a single GPIO output value, use the IOMUX.GPIOnCTL and IOMUX.GPIOnCFG registers. The following describes the necessary steps to set up GPIO1 as a GPIO output and toggle the bit.

TI recommends using the GPIO driver in the SimpleLink™ CC35xx Software Development Kit (SDK) when managing general purpose I/Os.

1. Map GPIO1 as a GPIO output by setting the IOMUX.GPIO1PCFG to 2 (Base function - GPIO).
2. Set GPIO1 as output by clearing the IOMUX.GPIO1CFG[11] IE bit. More port configurations can also be set in the IOMUX.GPIO1CTL, IOMUX.GPIO1CFG, IOMUX.GPIO1ECTL, IOMUX.GPIO1PCTL, and IOMUX.GPIO1PCFG registers (for more details, see Section 16.6).
3. Set the data output enable for GPIO1 by setting IOMUX.GPIO1CFG[1] OUTDIS = 0 and IOMUX.GPIO1CFG[13] ODISOVEN = 1, and output overide with IOMUX.GPIO1CTL[9] OUTOVREN = 1.
4. Toggle the GPIO1 output by writing a 1 to the IOMUX.GPIO1CTL[8] OUT bit.

16.6 I/O Pins

The IO Mux allows software to configure the pins based on the requirements of the application. The software can configure different characteristic settings for any or all of the I/O pins. All of the following features, are controlled in the IOMUX.GPIOn registers:

- **Drive Strength**(GPIOnCFG.IOSTR)
  - Configures the output drive strength of an I/O pin.
- **Pull Control**(GPIOnPCTL.CTL)
  - Configures a weak pull on an I/O pin. The following can be set: pull-up, pull-down, no pull, or IP pull control. See the data sheet for specific pull-up and pull-down current.
- **Edge Detection** (GPIOnECTL.EVTDETCFG)
  - Enables edge detection on I/O pin. The following modes are supported:
    - Rising edge
    - Falling edge
    - Level detection
    - No edge detection
  - Edge detection can be used for event generation on the AON event manager and/or a wake from standby signal to PRCM
- **Input Driver** (GPIOnCFG.IE)
  - Enables or disables the I/O input driver.
- **Pin Configuration** (GPIOnPCFG)
  - Selects the function of the pin. See the device specific data sheet for available functionality per I/O pin.

16.7 Unused Pins

By default, the I/O driver (output) and input buffer (input) are disabled (tri-state mode) at power on or reset, and thus the I/O pin can safely be left unconnected (floating). If the I/O pin is in a tri-state condition and connected to a node with a different voltage potential, a small leakage current can go through the pin. The same applies to

an I/O pin configured as input, where the pin is connected to a voltage source (for example VDD/2). The input is then an undefined value of either 0 or 1.

16.8 IOMUX Registers

Table 16-1 lists the memory-mapped registers for the IOMUX registers. All register offset addresses not listed in Table 16-1 should be considered as reserved locations and the register contents should not be modified.

Table 16-1. IOMUX Registers

Offset	Acronym	Register Name	Section
0h	SCLKICFG	Slow Clock Configuration	Section 16.8.1
4h	SCLKIPCTL	Slow Clock Pull Control	Section 16.8.2
8h	SCLKICTL	Slow Clock Input	Section 16.8.3
Ch	SCLKIECTL	Slow Clock Event Configuration	Section 16.8.4
1000h	LFXTNCFG	Low-Frequency Crystal Negative Config	Section 16.8.5
1004h	LFXTNPCTL	Low-Frequency Crystal Negative Control	Section 16.8.6
1008h	LFXTNCTL	Low-Frequency Crystal Control	Section 16.8.7
100Ch	LFXTNECTL	Low-Frequency Crystal Input	Section 16.8.8
2000h	GPIO2CFG	GPIO2 Configuration	Section 16.8.9
2004h	GPIO2PCTL	Pull Control	Section 16.8.10
2008h	GPIO2CTL	GPIO2 Control	Section 16.8.11
200Ch	GPIO2ECTL	GPIO2 Event Control	Section 16.8.12
3000h	GPIO3CFG	GPIO3 Configuration	Section 16.8.13
3004h	GPIO3PCTL	Pull Control	Section 16.8.14
3008h	GPIO3CTL	GPIO3 Control	Section 16.8.15
300Ch	GPIO3ECTL	GPIO3 Event Control	Section 16.8.16
4000h	GPIO4CFG	GPIO4 Configuration	Section 16.8.17
4004h	GPIO4PCTL	Pull Control	Section 16.8.18
4008h	GPIO4CTL	GPIO4 Control	Section 16.8.19
400Ch	GPIO4ECTL	GPIO4 Event Control	Section 16.8.20
5000h	GPIO5CFG	GPIO5 Configuration	Section 16.8.21
5004h	GPIO5PCTL	Pull Control	Section 16.8.22
5008h	GPIO5CTL	GPIO5 Control	Section 16.8.23
500Ch	GPIO5ECTL	GPIO5 Event Control	Section 16.8.24
6000h	GPIO6CFG	GPIO6 Configuration	Section 16.8.25
6004h	GPIO6PCTL	Pull Control	Section 16.8.26
6008h	GPIO6CTL	GPIO6 Control	Section 16.8.27
600Ch	GPIO6ECTL	GPIO6 Event Control	Section 16.8.28
7000h	SWDIOCFG	SWDIO Configuration	Section 16.8.29
7004h	SWDIOPCTL	SWDIO Pull Control	Section 16.8.30
7008h	SWDIOCTL	SWDIO Control	Section 16.8.31
700Ch	SWDIOECTL	SWDIO Event Control	Section 16.8.32
8000h	SWCLKCFG	JTAG Clock Configuration	Section 16.8.33
8004h	SWCLKPCTL	SWCLK Pull Control	Section 16.8.34
8008h	SWCLKCTL	SWCLK Control	Section 16.8.35
800Ch	SWCLKECTL	SWCLK Event Control	Section 16.8.36
9000h	LOGGERCFG	IO Logger Configuration	Section 16.8.37
9004h	LOGGERPCTL	Pull Control Configuration	Section 16.8.38
9008h	LOGGERCTL	Input/Output Logger Control	Section 16.8.39
900Ch	LOGGERECTL	Logger Event Control	Section 16.8.40
A000h	GPIO10CFG	GPIO10 Configuration	Section 16.8.41

Table 16-1. IOMUX Registers (continued)

Offset	Acronym	Register Name	Section
A004h	GPIO10PCTL	Pull Control	Section 16.8.42
A008h	GPIO10CTL	GPIO10 Control	Section 16.8.43
A00Ch	GPIO10ECTL	GPIO10 Event Control	Section 16.8.44
B000h	GPIO11CFG	GPIO11 Configuration	Section 16.8.45
B004h	GPIO11PCTL	Pull Control	Section 16.8.46
B008h	GPIO11CTL	GPIO11 Control	Section 16.8.47
B00Ch	GPIO11ECTL	GPIO11 Event Control	Section 16.8.48
C000h	GPIO12CFG	GPIO12 Configuration	Section 16.8.49
C004h	GPIO12PCTL	Pull Control	Section 16.8.50
C008h	GPIO12CTL	GPIO12 Control	Section 16.8.51
C00Ch	GPIO12ECTL	GPIO12 Event Control	Section 16.8.52
D000h	GPIO13CFG	GPIO13 Configuration	Section 16.8.53
D004h	GPIO13PCTL	Pull Control	Section 16.8.54
D008h	GPIO13CTL	GPIO13 Control	Section 16.8.55
D00Ch	GPIO13ECTL	GPIO13 Event Control	Section 16.8.56
E000h	GPIO14CFG	GPIO14 Configuration	Section 16.8.57
E004h	GPIO14PCTL	Pull Control Configuration	Section 16.8.58
E008h	GPIO14CTL	GPIO14 Control	Section 16.8.59
E00Ch	GPIO14ECTL	GPIO14 Event Control	Section 16.8.60
F000h	GPIO15CFG	GPIO15 Configuration	Section 16.8.61
F004h	GPIO15PCTL	Pull Control Configuration	Section 16.8.62
F008h	GPIO15CTL	GPIO15 Control	Section 16.8.63
F00Ch	GPIO15ECTL	GPIO15 Event Control	Section 16.8.64
00010000h	GPIO16CFG	GPIO16 Configuration	Section 16.8.65
00010004h	GPIO16PCTL	Pull Control	Section 16.8.66
00010008h	GPIO16CTL	GPIO16 Control	Section 16.8.67
0001000Ch	GPIO16ECTL	GPIO16 Event Control	Section 16.8.68
00011000h	GPIO17CFG	GPIO17 Configuration	Section 16.8.69
00011004h	GPIO17PCTL	Pull Control	Section 16.8.70
00011008h	GPIO17CTL	GPIO17 Control	Section 16.8.71
0001100Ch	GPIO17ECTL	GPIO17 Event Control	Section 16.8.72
00012000h	GPIO18CFG	GPIO18 Configuration	Section 16.8.73
00012004h	GPIO18PCTL	Pull Control	Section 16.8.74
00012008h	GPIO18CTL	GPIO18 Control	Section 16.8.75
0001200Ch	GPIO18ECTL	GPIO18 Event Control	Section 16.8.76
00013000h	GPIO19CFG	GPIO19 Configuration	Section 16.8.77
00013004h	GPIO19PCTL	Pull Control	Section 16.8.78
00013008h	GPIO19CTL	GPIO19 Control	Section 16.8.79
0001300Ch	GPIO19ECTL	GPIO19 Event Control	Section 16.8.80
00014000h	GPIO20CFG	GPIO20 Configuration	Section 16.8.81
00014004h	GPIO20PCTL	Pull Control Configuration	Section 16.8.82
00014008h	GPIO20CTL	GPIO20 Control	Section 16.8.83
0001400Ch	GPIO20ECTL	GPIO20 Event Control	Section 16.8.84
00015000h	GPIO21CFG	GPIO21 Configuration	Section 16.8.85
00015004h	GPIO21PCTL	Pull Control	Section 16.8.86

Table 16-1. IOMUX Registers (continued)

Offset	Acronym	Register Name	Section
00015008h	GPIO21CTL	GPIO21 Control	Section 16.8.87
0001500Ch	GPIO21ECTL	GPIO21 Event Control	Section 16.8.88
00016000h	GPIO22CFG	GPIO22 Configuration	Section 16.8.89
00016004h	GPIO22PCTL	Pull Control	Section 16.8.90
00016008h	GPIO22CTL	GPIO22 Control	Section 16.8.91
0001600Ch	GPIO22ECTL	GPIO22 Event Control	Section 16.8.92
00017000h	GPIO23CFG	GPIO23 Configuration	Section 16.8.93
00017004h	GPIO23PCTL	Pull Control	Section 16.8.94
00017008h	GPIO23CTL	GPIO23 Control	Section 16.8.95
0001700Ch	GPIO23ECTL	GPIO23 Event Control	Section 16.8.96
00018000h	GPIO24CFG	GPIO24 Configuration	Section 16.8.97
00018004h	GPIO24PCTL	Pull Control	Section 16.8.98
00018008h	GPIO24CTL	GPIO 24 Control	Section 16.8.99
0001800Ch	GPIO24ECTL	GPIO24 Event Control	Section 16.8.100
00019000h	GPIO25CFG	GPIO25 Configuration	Section 16.8.101
00019004h	GPIO25PCTL	Pull Control	Section 16.8.102
00019008h	GPIO25CTL	GPIO25 Control	Section 16.8.103
0001900Ch	GPIO25ECTL	GPIO25 Event Control	Section 16.8.104
0001A000h	GPIO26CFG	GPIO26 Configuration	Section 16.8.105
0001A004h	GPIO26PCTL	Pull Control	Section 16.8.106
0001A008h	GPIO26CTL	GPIO26 Control	Section 16.8.107
0001A00Ch	GPIO26ECTL	GPIO26 Event Control	Section 16.8.108
0001B000h	GPIO27CFG	GPIO27 Configuration	Section 16.8.109
0001B004h	GPIO27PCTL	Pull Control	Section 16.8.110
0001B008h	GPIO27CTL	GPIO27 Control	Section 16.8.111
0001B00Ch	GPIO27ECTL	GPIO27 Event Control	Section 16.8.112
0001C000h	GPIO28CFG	GPIO28 Configuration	Section 16.8.113
0001C004h	GPIO28PCTL	Pull Control	Section 16.8.114
0001C008h	GPIO28CTL	GPIO28 Control	Section 16.8.115
0001C00Ch	GPIO28ECTL	GPIO28 Event Control	Section 16.8.116
0001D000h	GPIO29CFG	GPIO29 Configuration	Section 16.8.117
0001D004h	GPIO29PCTL	Pull Control Configuration	Section 16.8.118
0001D008h	GPIO29CTL	GPIO29 Control	Section 16.8.119
0001D00Ch	GPIO29ECTL	GPIO29 Event Control	Section 16.8.120
0001E000h	GPIO30CFG	GPIO30 Configuration	Section 16.8.121
0001E004h	GPIO30PCTL	Pull Control Configuration	Section 16.8.122
0001E008h	GPIO30CTL	GPIO30 Control	Section 16.8.123
0001E00Ch	GPIO30ECTL	GPIO30 Event Control	Section 16.8.124
0001F000h	GPIO31CFG	GPIO31 Configuration	Section 16.8.125
0001F004h	GPIO31PCTL	Pull Control	Section 16.8.126
0001F008h	GPIO31CTL	GPIO31 Control	Section 16.8.127
0001F00Ch	GPIO31ECTL	GPIO31 Event Control	Section 16.8.128
00020000h	GPIO32CFG	GPIO32 Configuration	Section 16.8.129
00020004h	GPIO32PCTL	Pull Control	Section 16.8.130
00020008h	GPIO32CTL	GPIO Pin Control	Section 16.8.131

Table 16-1. IOMUX Registers (continued)

Offset	Acronym	Register Name	Section
0002000Ch	GPIO32ECTL	GPIO32 Event Control	Section 16.8.132
00021000h	GPIO33CFG	GPIO33 Configuration	Section 16.8.133
00021004h	GPIO33PCTL	Pull Control	Section 16.8.134
00021008h	GPIO33CTL	GPIO33 Control	Section 16.8.135
0002100Ch	GPIO33ECTL	GPIO33 Event Control	Section 16.8.136
00022000h	GPIO34CFG	GPIO34 Configuration	Section 16.8.137
00022004h	GPIO34PCTL	Pull Control	Section 16.8.138
00022008h	GPIO34CTL	GPIO34 Control	Section 16.8.139
0002200Ch	GPIO34ECTL	GPIO34 Event Control	Section 16.8.140
00023000h	GPIO35CFG	GPIO35 Configuration	Section 16.8.141
00023004h	GPIO35PCTL	Pull Control	Section 16.8.142
00023008h	GPIO35CTL	GPIO35 Control	Section 16.8.143
0002300Ch	GPIO35ECTL	GPIO35 Event Control	Section 16.8.144
00024000h	GPIO36CFG	GPIO36 Configuration	Section 16.8.145
00024004h	GPIO36PCTL	Pull Control	Section 16.8.146
00024008h	GPIO36CTL	GPIO36 Control	Section 16.8.147
0002400Ch	GPIO36ECTL	GPIO36 Event Control	Section 16.8.148
00025000h	GPIO37CFG	GPIO37 Configuration	Section 16.8.149
00025004h	GPIO37PCTL	Pull Control	Section 16.8.150
00025008h	GPIO37CTL	GPIO37 Control	Section 16.8.151
0002500Ch	GPIO37ECTL	GPIO37 Event Control	Section 16.8.152
00026000h	GPIO38CFG	GPIO38 Configuration	Section 16.8.153
00026004h	GPIO38PCTL	Pull Control	Section 16.8.154
00026008h	GPIO38CTL	GPIO38 Control	Section 16.8.155
0002600Ch	GPIO38ECTL	GPIO38 Event Control	Section 16.8.156
00027000h	GPIO39CFG	GPIO39 Configuration	Section 16.8.157
00027004h	GPIO39PCTL	GPIO39 Pull Control	Section 16.8.158
00027008h	GPIO39CTL	GPIO39 Control	Section 16.8.159
0002700Ch	GPIO39ECTL	GPIO39 Event Control	Section 16.8.160
00028000h	GPIO40CFG	GPIO40 Configuration	Section 16.8.161
00028004h	GPIO40PCTL	Pull Control Configuration	Section 16.8.162
00028008h	GPIO40CTL	GPIO40 Control	Section 16.8.163
0002800Ch	GPIO40ECTL	GPIO40 Event Control	Section 16.8.164
00029000h	GPIO41CFG	GPIO41 Configuration	Section 16.8.165
00029004h	GPIO41PCTL	Pull Control	Section 16.8.166
00029008h	GPIO41CTL	GPIO41 Control	Section 16.8.167
0002900Ch	GPIO41ECTL	GPIO41 Event Control	Section 16.8.168
0002A000h	GPIO42CFG	GPIO42 Configuration	Section 16.8.169
0002A004h	GPIO42PCTL	Pull Control	Section 16.8.170
0002A008h	GPIO42CTL	GPIO42 Control	Section 16.8.171
0002A00Ch	GPIO42ECTL	GPIO42 Event Control	Section 16.8.172
0002B000h	GPIO43CFG	GPIO43 Configuration	Section 16.8.173
0002B004h	GPIO43PCTL	Pull Control	Section 16.8.174
0002B008h	GPIO43CTL	GPIO 43 Control	Section 16.8.175
0002B00Ch	GPIO43ECTL	GPIO43 Event Control	Section 16.8.176

Table 16-1. IOMUX Registers (continued)

Offset	Acronym	Register Name	Section
0002C000h	GPIO44CFG	GPIO44 Configuration	Section 16.8.177
0002C004h	GPIO44PCTL	Pul Control	Section 16.8.178
0002C008h	GPIO44CTL	GPIO44 Control	Section 16.8.179
0002C00Ch	GPIO44ECTL	GPIO44 Event Control	Section 16.8.180
0002D004h	SCLKIPCFG	Slow Clock Port Configuration	Section 16.8.181
0002D008h	LFXTNPCFG	LFXTALN Port Control	Section 16.8.182
0002D00Ch	GPIO2PCFG	GPIO2 Port Configuration	Section 16.8.183
0002D010h	GPIO3PCFG	GPIO3 Port Configuration	Section 16.8.184
0002D014h	GPIO4PCFG	GPIO4 Port Configuration	Section 16.8.185
0002D018h	GPIO5PCFG	GPIO5 Port Configuration	Section 16.8.186
0002D01Ch	GPIO6PCFG	GPIO6 Port Configuration	Section 16.8.187
0002D020h	SWDIOPCFG	Serial Wire Debug control	Section 16.8.188
0002D024h	SWCLKPCFG	SWD Clock Configuration	Section 16.8.189
0002D028h	LOGGERPCFG	Logger Configuration	Section 16.8.190
0002D02Ch	GPIO10PCFG	GPIO10 Port Configuration	Section 16.8.191
0002D030h	GPIO11PCFG	GPIO11 Port Configuration	Section 16.8.192
0002D034h	GPIO12PCFG	GPIO12 Port Configuration	Section 16.8.193
0002D038h	GPIO13PCFG	GPIO13 Port Configuration	Section 16.8.194
0002D03Ch	GPIO14PCFG	GPIO14 Configuration	Section 16.8.195
0002D040h	GPIO15PCFG	GPIO15 Port Configuration	Section 16.8.196
0002D044h	GPIO16PCFG	GPIO16 Port Configuration	Section 16.8.197
0002D048h	GPIO17PCFG	GPIO17 Port Configuration	Section 16.8.198
0002D04Ch	GPIO18PCFG	GPIO18 Port Configuration	Section 16.8.199
0002D050h	GPIO19PCFG	GPIO19 Port Configuration	Section 16.8.200
0002D054h	GPIO20PCFG	GPIO20 Port Configuration	Section 16.8.201
0002D058h	GPIO21PCFG	GPIO21 Port Configuration	Section 16.8.202
0002D05Ch	GPIO22PCFG	GPIO22 Port Configuration	Section 16.8.203
0002D060h	GPIO23PCFG	GPIO23 Port Configuration	Section 16.8.204
0002D064h	GPIO24PCFG	GPIO24 Port Configuration	Section 16.8.205
0002D068h	GPIO25PCFG	GPIO25 Port Configuration	Section 16.8.206
0002D06Ch	GPIO26PCFG	GPIO26 Port Configuration	Section 16.8.207
0002D070h	GPIO27PCFG	GPIO27 Port Configuration	Section 16.8.208
0002D074h	GPIO28PCFG	GPIO28 Port Configuration	Section 16.8.209
0002D078h	GPIO29PCFG	GPIO29 Port Configuration	Section 16.8.210
0002D07Ch	GPIO30PCFG	GPIO30 Port Configuration	Section 16.8.211
0002D080h	GPIO31PCFG	GPIO31 Port Configuration	Section 16.8.212
0002D084h	GPIO32PCFG	GPIO32 Port Configuration	Section 16.8.213
0002D088h	GPIO33PCFG	GPIO33 Port Configuration	Section 16.8.214
0002D08Ch	GPIO34PCFG	GPIO34 Port Configuration	Section 16.8.215
0002D090h	GPIO35PCFG	GPIO35 Port Configuration	Section 16.8.216
0002D094h	GPIO36PCFG	GPIO36 Port Configuration	Section 16.8.217
0002D098h	GPIO37PCFG	GPIO37 Port Configuration	Section 16.8.218
0002D09Ch	GPIO38PCFG	GPIO39 Port Configuration	Section 16.8.219
0002D0A0h	GPIO39PCFG	GPIO39 Port Configuration	Section 16.8.220
0002D0A4h	GPIO40PCFG	GPIO40 Port Configuration	Section 16.8.221

Table 16-1. IOMUX Registers (continued)

Offset	Acronym	Register Name	Section
0002D0A8h	GPIO41PCFG	GPIO41 Port Configuration	Section 16.8.222
0002D0ACh	GPIO42PCFG	GPIO42 Port Configuration	Section 16.8.223
0002D0B0h	GPIO43PCFG	GPIO43 Port Configuration	Section 16.8.224
0002D0B4h	GPIO44PCFG	GPIO44 Port Configuration	Section 16.8.225
0002D0C0h	GPIO45PCFG	GPIO45 Port Configuration	Section 16.8.226
0002D0C4h	GPIO46PCFG	GPIO46 Port Configuration	Section 16.8.227
0002D0C8h	GPIO47PCFG	GPIO47 Port Configuration	Section 16.8.228
0002D0CCh	GPIO48PCFG	GPIO48 Port Configuration	Section 16.8.229
0002E000h	GPIO45CFG	GPIO45 Configuration	Section 16.8.230
0002E004h	GPIO45PCTL	Pull Control Configuration	Section 16.8.231
0002E008h	GPIO45CTL	GPIO45 Control	Section 16.8.232
0002E00Ch	GPIO45ECTL	GPIO45 Event Control	Section 16.8.233
0002F000h	GPIO46CFG	GPIO46 Configuration	Section 16.8.234
0002F004h	GPIO46PCTL	Pull Control Configuration	Section 16.8.235
0002F008h	GPIO46CTL	GPIO46 Control	Section 16.8.236
0002F00Ch	GPIO46ECTL	GPIO46 Event Control	Section 16.8.237
00030000h	GPIO47CFG	GPIO47 Configuration	Section 16.8.238
00030004h	GPIO47PCTL	Pull Control	Section 16.8.239
00030008h	GPIO47CTL	GPIO47 Control	Section 16.8.240
0003000Ch	GPIO47ECTL	GPIO47 Event Control	Section 16.8.241
00031000h	GPIO48CFG	GPIO48 Configuration	Section 16.8.242
00031004h	GPIO48PCTL	Pull Control	Section 16.8.243
00031008h	GPIO48CTL	GPIO48 Control	Section 16.8.244
0003100Ch	GPIO48ECTL	GPIO48 Event Control	Section 16.8.245

Complex bit access types are encoded to fit into small table cells. Table 16-2 shows the codes that are used for access types in this section.

Table 16-2. IOMUX Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

16.8.1 SCLKICFG Register (Offset = 0h) [Reset = 00000000h]

SCLKICFG is shown in Table 16-3.

Return to the Summary Table.

CFG register for IO SLOW_CLOCK_IN. This register configures the corresponding pad

Table 16-3. SCLKICFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
13	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
12	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.2 SCLKIPCTL Register (Offset = 4h) [Reset = 00000000h]

SCLKIPCTL is shown in Table 16-4.

Return to the Summary Table.

Pull control register of IO SLOW_CLOCK_IN This register configures the pull control

Table 16-4. SCLKIPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	2h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = RESERVED 3h = Pull disable

16.8.3 SCLKICTL Register (Offset = 8h) [Reset = 00000000h]

SCLKICTL is shown in Table 16-5.

Return to the Summary Table.

Control register of IO SLOW_CLOCK_IN This register controls the IO state

Table 16-5. SCLKICTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.4 SCLKIECTL Register (Offset = Ch) [Reset = 00000000h]

SCLKIECTL is shown in Table 16-6.

Return to the Summary Table.

Event control register for IO SLOW_CLOCK_IN This register controls the Event configuration and behaviour

Table 16-6. SCLKIECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.5 LFXTNCFG Register (Offset = 1000h) [Reset = 00000000h]

LFXTNCFG is shown in Table 16-7.

Return to the Summary Table.

CFG register for IO LFXTAL_N. This register configures the corresponding pad

Table 16-7. LFXTNCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	0h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9	ANASWOVREN	R/W	1h	This field controls the analog switch override 0h = Analog switch is controlled by IP 1h = Enable override on analog switch control
8	ANASW	R/W	0h	This field defines the Ana switch state. If the switch is enabled, the analog signal is routed to the IO pad Note: This field is applicable when [ANASWOVREN] is enabled 0h = Analog switch open 1h = Analog switch closed
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.6 LFXTNPCTL Register (Offset = 1004h) [Reset = 00000000h]

LFXTNPCTL is shown in Table 16-8.

Return to the Summary Table.

Pull control register of IO LFXTAL_N This register configures the pull control

Table 16-8. LFXTNPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	2h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.7 LFXTNCTL Register (Offset = 1008h) [Reset = 00000000h]

LFXTNCTL is shown in Table 16-9.

Return to the Summary Table.

Control register of IO LFXTAL_N This register controls the IO state

Table 16-9. LFXTNCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.8 LFXTNECTL Register (Offset = 100Ch) [Reset = 00000000h]

LFXTNECTL is shown in Table 16-10.

Return to the Summary Table.

Event control register for IO LFXTAL_N This register controls the Event configuration and behaviour

Table 16-10. LFXTNECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.9 GPIO2CFG Register (Offset = 2000h) [Reset = 00000000h]

GPIO2CFG is shown in Table 16-11.

Return to the Summary Table.

CFG register for IO GPIO2. This register configures the corresponding pad

Table 16-11. GPIO2CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	0h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9	ANASWOVREN	R/W	1h	This field controls the analog switch override 0h = Analog switch is controlled by IP 1h = Enable override on analog switch control
8	ANASW	R/W	0h	This field defines the Ana switch state. If the switch is enabled, the analog signal is routed to the IO pad Note: This field is applicable when [ANASWOVREN] is enabled 0h = Analog switch open 1h = Analog switch closed
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.10 GPIO2PCTL Register (Offset = 2004h) [Reset = 00000000h]

GPIO2PCTL is shown in Table 16-12.

Return to the Summary Table.

Pull control register of IO GPIO2 This register configures the pull control

Table 16-12. GPIO2PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.11 GPIO2CTL Register (Offset = 2008h) [Reset = 00000000h]

GPIO2CTL is shown in Table 16-13.

Return to the Summary Table.

Control register of IO GPIO2 This register controls the IO state

Table 16-13. GPIO2CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.12 GPIO2ECTL Register (Offset = 200Ch) [Reset = 00000000h]

GPIO2ECTL is shown in Table 16-14.

Return to the Summary Table.

Event control register for IO GPIO2 This register controls the Event configuration and behaviour

Table 16-14. GPIO2ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.13 GPIO3CFG Register (Offset = 3000h) [Reset = 00000000h]

GPIO3CFG is shown in Table 16-15.

Return to the Summary Table.

CFG register for IO GPIO3. This register configures the corresponding pad

Table 16-15. GPIO3CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	0h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9	ANASWOVREN	R/W	1h	This field controls the analog switch override 0h = Analog switch is controlled by IP 1h = Enable override on analog switch control
8	ANASW	R/W	0h	This field defines the Ana switch state. If the switch is enabled, the analog signal is routed to the IO pad Note: This field is applicable when [ANASWOVREN] is enabled 0h = Analog switch open 1h = Analog switch closed
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.14 GPIO3PCTL Register (Offset = 3004h) [Reset = 00000000h]

GPIO3PCTL is shown in Table 16-16.

Return to the Summary Table.

Pull control register of IO GPIO3 This register configures the pull control

Table 16-16. GPIO3PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.15 GPIO3CTL Register (Offset = 3008h) [Reset = 00000000h]

GPIO3CTL is shown in Table 16-17.

Return to the Summary Table.

Control register of IO GPIO3 This register controls the IO state

Table 16-17. GPIO3CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.16 GPIO3ECTL Register (Offset = 300Ch) [Reset = 00000000h]

GPIO3ECTL is shown in Table 16-18.

Return to the Summary Table.

Event control register for IO GPIO3 This register controls the Event configuration and behaviour

Table 16-18. GPIO3ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.17 GPIO4CFG Register (Offset = 4000h) [Reset = 00000000h]

GPIO4CFG is shown in Table 16-19.

Return to the Summary Table.

CFG register for IO GPIO4. This register configures the corresponding pad

Table 16-19. GPIO4CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	0h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9	ANASWOVREN	R/W	1h	This field controls the analog switch override 0h = Analog switch is controlled by IP 1h = Enable override on analog switch control
8	ANASW	R/W	0h	This field defines the Ana switch state. If the switch is enabled, the analog signal is routed to the IO pad Note: This field is applicable when [ANASWOVREN] is enabled 0h = Analog switch open 1h = Analog switch closed
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.18 GPIO4PCTL Register (Offset = 4004h) [Reset = 00000000h]

GPIO4PCTL is shown in Table 16-20.

Return to the Summary Table.

Pull control register of IO GPIO4 This register configures the pull control

Table 16-20. GPIO4PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.19 GPIO4CTL Register (Offset = 4008h) [Reset = 00000000h]

GPIO4CTL is shown in Table 16-21.

Return to the Summary Table.

Control register of IO GPIO4 This register controls the IO state

Table 16-21. GPIO4CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.20 GPIO4ECTL Register (Offset = 400Ch) [Reset = 00000000h]

GPIO4ECTL is shown in Table 16-22.

Return to the Summary Table.

Event control register for IO GPIO4 This register controls the Event configuration and behaviour

Table 16-22. GPIO4ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.21 GPIO5CFG Register (Offset = 5000h) [Reset = 00000000h]

GPIO5CFG is shown in Table 16-23.

Return to the Summary Table.

CFG register for IO GPIO5. This register configures the corresponding pad

Table 16-23. GPIO5CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	0h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9	ANASWOVREN	R/W	1h	This field controls the analog switch override 0h = Analog switch is controlled by IP 1h = Enable override on analog switch control
8	ANASW	R/W	0h	This field defines the Ana switch state. If the switch is enabled, the analog signal is routed to the IO pad Note: This field is applicable when [ANASWOVREN] is enabled 0h = Analog switch open 1h = Analog switch closed
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.22 GPIO5PCTL Register (Offset = 5004h) [Reset = 00000000h]

GPIO5PCTL is shown in Table 16-24.

Return to the Summary Table.

Pull control register of IO GPIO5 This register configures the pull control

Table 16-24. GPIO5PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.23 GPIO5CTL Register (Offset = 5008h) [Reset = 00000000h]

GPIO5CTL is shown in Table 16-25.

Return to the Summary Table.

Control register of IO GPIO5 This register controls the IO state

Table 16-25. GPIO5CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.24 GPIO5ECTL Register (Offset = 500Ch) [Reset = 00000000h]

GPIO5ECTL is shown in Table 16-26.

Return to the Summary Table.

Event control register for IO GPIO5 This register controls the Event configuration and behaviour

Table 16-26. GPIO5ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.25 GPIO6CFG Register (Offset = 6000h) [Reset = 00000000h]

GPIO6CFG is shown in Table 16-27.

Return to the Summary Table.

CFG register for IO GPIO6. This register configures the corresponding pad

Table 16-27. GPIO6CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	0h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9	ANASWOVREN	R/W	1h	This field controls the analog switch override 0h = Analog switch is controlled by IP 1h = Enable override on analog switch control
8	ANASW	R/W	0h	This field defines the Ana switch state. If the switch is enabled, the analog signal is routed to the IO pad Note: This field is applicable when [ANASWOVREN] is enabled 0h = Analog switch open 1h = Analog switch closed
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.26 GPIO6PCTL Register (Offset = 6004h) [Reset = 00000000h]

GPIO6PCTL is shown in Table 16-28.

Return to the Summary Table.

Pull control register of IO GPIO6 This register configures the pull control

Table 16-28. GPIO6PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.27 GPIO6CTL Register (Offset = 6008h) [Reset = 00000000h]

GPIO6CTL is shown in Table 16-29.

Return to the Summary Table.

Control register of IO GPIO6 This register controls the IO state

Table 16-29. GPIO6CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.28 GPIO6ECTL Register (Offset = 600Ch) [Reset = 00000000h]

GPIO6ECTL is shown in Table 16-30.

Return to the Summary Table.

Event control register for IO GPIO6 This register controls the Event configuration and behaviour

Table 16-30. GPIO6ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.29 SWDIOCFG Register (Offset = 7000h) [Reset = 00000000h]

SWDIOCFG is shown in Table 16-31.

Return to the Summary Table.

CFG register for IO SWDIO. This register configures the corresponding pad

Table 16-31. SWDIOCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.30 SWDIOPCTL Register (Offset = 7004h) [Reset = 00000000h]

SWDIOPCTL is shown in Table 16-32.

Return to the Summary Table.

Pull control register of IO SWDIO This register configures the pull control

Table 16-32. SWDIOPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.31 SWDIOCTL Register (Offset = 7008h) [Reset = 00000000h]

SWDIOCTL is shown in Table 16-33.

Return to the Summary Table.

Control register of IO SWDIO This register controls the IO state

Table 16-33. SWDIOCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.32 SWDIOECTL Register (Offset = 700Ch) [Reset = 00000000h]

SWDIOECTL is shown in Table 16-34.

Return to the Summary Table.

Event control register for IO SWDIO This register controls the Event configuration and behaviour

Table 16-34. SWDIOECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.33 SWCLKCFG Register (Offset = 8000h) [Reset = 00000000h]

SWCLKCFG is shown in Table 16-35.

Return to the Summary Table.

CFG register for IO SWCLK. This register configures the corresponding pad

Table 16-35. SWCLKCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.34 SWCLKPCTL Register (Offset = 8004h) [Reset = 00000000h]

SWCLKPCTL is shown in Table 16-36.

Return to the Summary Table.

Pull control register of IO SWCLK This register configures the pull control

Table 16-36. SWCLKPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	2h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.35 SWCLKCTL Register (Offset = 8008h) [Reset = 00000000h]

SWCLKCTL is shown in Table 16-37.

Return to the Summary Table.

Control register of IO SWCLK This register controls the IO state

Table 16-37. SWCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.36 SWCLKECTL Register (Offset = 800Ch) [Reset = 00000000h]

SWCLKECTL is shown in Table 16-38.

Return to the Summary Table.

Event control register for IO SWCLK This register controls the Event configuration and behaviour

Table 16-38. SWCLKECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.37 LOGGERCFG Register (Offset = 9000h) [Reset = 00000000h]

LOGGERCFG is shown in Table 16-39.

Return to the Summary Table.

CFG register for IO LOGGER. This register configures the corresponding pad

Table 16-39. LOGGERCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.38 LOGGERPCTL Register (Offset = 9004h) [Reset = 00000000h]

LOGGERPCTL is shown in Table 16-40.

Return to the Summary Table.

Pull control register of IO LOGGER This register configures the pull control

Table 16-40. LOGGERPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.39 LOGGERCTL Register (Offset = 9008h) [Reset = 00000000h]

LOGGERCTL is shown in Table 16-41.

Return to the Summary Table.

Control register of IO LOGGER This register controls the IO state

Table 16-41. LOGGERCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.40 LOGGERECTL Register (Offset = 900Ch) [Reset = 00000000h]

LOGGERECTL is shown in Table 16-42.

Return to the Summary Table.

Event control register for IO LOGGER This register controls the Event configuration and behaviour

Table 16-42. LOGGERECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.41 GPIO10CFG Register (Offset = A000h) [Reset = 00000000h]

GPIO10CFG is shown in Table 16-43.

Return to the Summary Table.

CFG register for IO GPIO10. This register configures the corresponding pad

Table 16-43. GPIO10CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	0h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9	ANASWOVREN	R/W	1h	This field controls the analog switch override 0h = Analog switch is controlled by IP 1h = Enable override on analog switch control
8	ANASW	R/W	0h	This field defines the Ana switch state. If the switch is enabled, the analog signal is routed to the IO pad Note: This field is applicable when [ANASWOVREN] is enabled 0h = Analog switch open 1h = Analog switch closed
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.42 GPIO10PCTL Register (Offset = A004h) [Reset = 00000000h]

GPIO10PCTL is shown in Table 16-44.

Return to the Summary Table.

Pull control register of IO GPIO10 This register configures the pull control

Table 16-44. GPIO10PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.43 GPIO10CTL Register (Offset = A008h) [Reset = 00000000h]

GPIO10CTL is shown in Table 16-45.

Return to the Summary Table.

Control register of IO GPIO10 This register controls the IO state

Table 16-45. GPIO10CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.44 GPIO10ECTL Register (Offset = A00Ch) [Reset = 00000000h]

GPIO10ECTL is shown in Table 16-46.

Return to the Summary Table.

Event control register for IO GPIO10 This register controls the Event configuration and behaviour

Table 16-46. GPIO10ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.45 GPIO11CFG Register (Offset = B000h) [Reset = 00000000h]

GPIO11CFG is shown in Table 16-47.

Return to the Summary Table.

CFG register for IO GPIO11. This register configures the corresponding pad

Table 16-47. GPIO11CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	0h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9	ANASWOVREN	R/W	1h	This field controls the analog switch override 0h = Analog switch is controlled by IP 1h = Enable override on analog switch control
8	ANASW	R/W	0h	This field defines the Ana switch state. If the switch is enabled, the analog signal is routed to the IO pad Note: This field is applicable when [ANASWOVREN] is enabled 0h = Analog switch open 1h = Analog switch closed
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.46 GPIO11PCTL Register (Offset = B004h) [Reset = 00000000h]

GPIO11PCTL is shown in Table 16-48.

Return to the Summary Table.

Pull control register of IO GPIO11 This register configures the pull control

Table 16-48. GPIO11PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.47 GPIO11CTL Register (Offset = B008h) [Reset = 00000000h]

GPIO11CTL is shown in Table 16-49.

Return to the Summary Table.

Control register of IO GPIO11 This register controls the IO state

Table 16-49. GPIO11CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.48 GPIO11ECTL Register (Offset = B00Ch) [Reset = 00000000h]

GPIO11ECTL is shown in Table 16-50.

Return to the Summary Table.

Event control register for IO GPIO11 This register controls the Event configuration and behaviour

Table 16-50. GPIO11ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.49 GPIO12CFG Register (Offset = C000h) [Reset = 00000000h]

GPIO12CFG is shown in Table 16-51.

Return to the Summary Table.

CFG register for IO GPIO12. This register configures the corresponding pad

Table 16-51. GPIO12CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.50 GPIO12PCTL Register (Offset = C004h) [Reset = 00000000h]

GPIO12PCTL is shown in Table 16-52.

Return to the Summary Table.

Pull control register of IO GPIO12 This register configures the pull control

Table 16-52. GPIO12PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.51 GPIO12CTL Register (Offset = C008h) [Reset = 00000000h]

GPIO12CTL is shown in Table 16-53.

Return to the Summary Table.

Control register of IO GPIO12 This register controls the IO state

Table 16-53. GPIO12CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.52 GPIO12ECTL Register (Offset = C00Ch) [Reset = 00000000h]

GPIO12ECTL is shown in Table 16-54.

Return to the Summary Table.

Event control register for IO GPIO12 This register controls the Event configuration and behaviour

Table 16-54. GPIO12ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.53 GPIO13CFG Register (Offset = D000h) [Reset = 00000000h]

GPIO13CFG is shown in Table 16-55.

Return to the Summary Table.

CFG register for IO GPIO13. This register configures the corresponding pad

Table 16-55. GPIO13CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.54 GPIO13PCTL Register (Offset = D004h) [Reset = 00000000h]

GPIO13PCTL is shown in Table 16-56.

Return to the Summary Table.

Pull control register of IO GPIO13 This register configures the pull control

Table 16-56. GPIO13PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.55 GPIO13CTL Register (Offset = D008h) [Reset = 00000000h]

GPIO13CTL is shown in Table 16-57.

Return to the Summary Table.

Control register of IO GPIO13 This register controls the IO state

Table 16-57. GPIO13CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.56 GPIO13ECTL Register (Offset = D00Ch) [Reset = 00000000h]

GPIO13ECTL is shown in Table 16-58.

Return to the Summary Table.

Event control register for IO GPIO13 This register controls the Event configuration and behaviour

Table 16-58. GPIO13ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.57 GPIO14CFG Register (Offset = E000h) [Reset = 00000000h]

GPIO14CFG is shown in Table 16-59.

Return to the Summary Table.

CFG register for IO GPIO14. This register configures the corresponding pad

Table 16-59. GPIO14CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.58 GPIO14PCTL Register (Offset = E004h) [Reset = 00000000h]

GPIO14PCTL is shown in Table 16-60.

Return to the Summary Table.

Pull control register of IO GPIO14 This register configures the pull control

Table 16-60. GPIO14PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.59 GPIO14CTL Register (Offset = E008h) [Reset = 00000000h]

GPIO14CTL is shown in Table 16-61.

Return to the Summary Table.

Control register of IO GPIO14 This register controls the IO state

Table 16-61. GPIO14CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.60 GPIO14ECTL Register (Offset = E00Ch) [Reset = 00000000h]

GPIO14ECTL is shown in Table 16-62.

Return to the Summary Table.

Event control register for IO GPIO14 This register controls the Event configuration and behaviour

Table 16-62. GPIO14ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.61 GPIO15CFG Register (Offset = F000h) [Reset = 00000000h]

GPIO15CFG is shown in Table 16-63.

Return to the Summary Table.

CFG register for IO GPIO15. This register configures the corresponding pad

Table 16-63. GPIO15CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.62 GPIO15PCTL Register (Offset = F004h) [Reset = 00000000h]

GPIO15PCTL is shown in Table 16-64.

Return to the Summary Table.

Pull control register of IO GPIO15 This register configures the pull control

Table 16-64. GPIO15PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.63 GPIO15CTL Register (Offset = F008h) [Reset = 00000000h]

GPIO15CTL is shown in Table 16-65.

Return to the Summary Table.

Control register of IO GPIO15 This register controls the IO state

Table 16-65. GPIO15CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.64 GPIO15ECTL Register (Offset = F00Ch) [Reset = 00000000h]

GPIO15ECTL is shown in Table 16-66.

Return to the Summary Table.

Event control register for IO GPIO15 This register controls the Event configuration and behaviour

Table 16-66. GPIO15ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.65 GPIO16CFG Register (Offset = 00010000h) [Reset = 00000000h]

GPIO16CFG is shown in Table 16-67.

Return to the Summary Table.

CFG register for IO GPIO16. This register configures the corresponding pad

Table 16-67. GPIO16CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.66 GPIO16PCTL Register (Offset = 00010004h) [Reset = 00000000h]

GPIO16PCTL is shown in Table 16-68.

Return to the Summary Table.

Pull control register of IO GPIO16 This register configures the pull control

Table 16-68. GPIO16PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.67 GPIO16CTL Register (Offset = 00010008h) [Reset = 00000000h]

GPIO16CTL is shown in Table 16-69.

Return to the Summary Table.

Control register of IO GPIO16 This register controls the IO state

Table 16-69. GPIO16CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.68 GPIO16ECTL Register (Offset = 0001000Ch) [Reset = 00000000h]

GPIO16ECTL is shown in Table 16-70.

Return to the Summary Table.

Event control register for IO GPIO16 This register controls the Event configuration and behaviour

Table 16-70. GPIO16ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.69 GPIO17CFG Register (Offset = 00011000h) [Reset = 00000000h]

GPIO17CFG is shown in Table 16-71.

Return to the Summary Table.

CFG register for IO GPIO17. This register configures the corresponding pad

Table 16-71. GPIO17CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.70 GPIO17PCTL Register (Offset = 00011004h) [Reset = 00000000h]

GPIO17PCTL is shown in Table 16-72.

Return to the Summary Table.

Pull control register of IO GPIO17 This register configures the pull control

Table 16-72. GPIO17PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.71 GPIO17CTL Register (Offset = 00011008h) [Reset = 00000000h]

GPIO17CTL is shown in Table 16-73.

Return to the Summary Table.

Control register of IO GPIO17 This register controls the IO state

Table 16-73. GPIO17CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.72 GPIO17ECTL Register (Offset = 0001100Ch) [Reset = 00000000h]

GPIO17ECTL is shown in Table 16-74.

Return to the Summary Table.

Event control register for IO GPIO17 This register controls the Event configuration and behaviour

Table 16-74. GPIO17ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.73 GPIO18CFG Register (Offset = 00012000h) [Reset = 00000000h]

GPIO18CFG is shown in Table 16-75.

Return to the Summary Table.

CFG register for IO GPIO18. This register configures the corresponding pad

Table 16-75. GPIO18CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.74 GPIO18PCTL Register (Offset = 00012004h) [Reset = 00000000h]

GPIO18PCTL is shown in Table 16-76.

Return to the Summary Table.

Pull control register of IO GPIO18 This register configures the pull control

Table 16-76. GPIO18PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.75 GPIO18CTL Register (Offset = 00012008h) [Reset = 00000000h]

GPIO18CTL is shown in Table 16-77.

Return to the Summary Table.

Control register of IO GPIO18 This register controls the IO state

Table 16-77. GPIO18CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.76 GPIO18ECTL Register (Offset = 0001200Ch) [Reset = 00000000h]

GPIO18ECTL is shown in Table 16-78.

Return to the Summary Table.

Event control register for IO GPIO18 This register controls the Event configuration and behaviour

Table 16-78. GPIO18ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.77 GPIO19CFG Register (Offset = 00013000h) [Reset = 00000000h]

GPIO19CFG is shown in Table 16-79.

Return to the Summary Table.

CFG register for IO GPIO19. This register configures the corresponding pad

Table 16-79. GPIO19CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.78 GPIO19PCTL Register (Offset = 00013004h) [Reset = 00000000h]

GPIO19PCTL is shown in Table 16-80.

Return to the Summary Table.

Pull control register of IO GPIO19 This register configures the pull control

Table 16-80. GPIO19PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.79 GPIO19CTL Register (Offset = 00013008h) [Reset = 00000000h]

GPIO19CTL is shown in Table 16-81.

Return to the Summary Table.

Control register of IO GPIO19 This register controls the IO state

Table 16-81. GPIO19CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.80 GPIO19ECTL Register (Offset = 0001300Ch) [Reset = 00000000h]

GPIO19ECTL is shown in Table 16-82.

Return to the Summary Table.

Event control register for IO GPIO19 This register controls the Event configuration and behaviour

Table 16-82. GPIO19ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.81 GPIO20CFG Register (Offset = 00014000h) [Reset = 00000000h]

GPIO20CFG is shown in Table 16-83.

Return to the Summary Table.

CFG register for IO GPIO20. This register configures the corresponding pad

Table 16-83. GPIO20CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	0h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.82 GPIO20PCTL Register (Offset = 00014004h) [Reset = 00000000h]

GPIO20PCTL is shown in Table 16-84.

Return to the Summary Table.

Pull control register of IO GPIO20 This register configures the pull control

Table 16-84. GPIO20PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.83 GPIO20CTL Register (Offset = 00014008h) [Reset = 00000000h]

GPIO20CTL is shown in Table 16-85.

Return to the Summary Table.

Control register of IO GPIO20 This register controls the IO state

Table 16-85. GPIO20CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.84 GPIO20ECTL Register (Offset = 0001400Ch) [Reset = 00000000h]

GPIO20ECTL is shown in Table 16-86.

Return to the Summary Table.

Event control register for IO GPIO20 This register controls the Event configuration and behaviour

Table 16-86. GPIO20ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.85 GPIO21CFG Register (Offset = 00015000h) [Reset = 00000000h]

GPIO21CFG is shown in Table 16-87.

Return to the Summary Table.

CFG register for IO GPIO21. This register configures the corresponding pad

Table 16-87. GPIO21CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.86 GPIO21PCTL Register (Offset = 00015004h) [Reset = 00000000h]

GPIO21PCTL is shown in Table 16-88.

Return to the Summary Table.

Pull control register of IO GPIO21 This register configures the pull control

Table 16-88. GPIO21PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.87 GPIO21CTL Register (Offset = 00015008h) [Reset = 00000000h]

GPIO21CTL is shown in Table 16-89.

Return to the Summary Table.

Control register of IO GPIO21 This register controls the IO state

Table 16-89. GPIO21CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.88 GPIO21ECTL Register (Offset = 0001500Ch) [Reset = 00000000h]

GPIO21ECTL is shown in Table 16-90.

Return to the Summary Table.

Event control register for IO GPIO21 This register controls the Event configuration and behaviour

Table 16-90. GPIO21ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.89 GPIO22CFG Register (Offset = 00016000h) [Reset = 00000000h]

GPIO22CFG is shown in Table 16-91.

Return to the Summary Table.

CFG register for IO GPIO22. This register configures the corresponding pad

Table 16-91. GPIO22CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.90 GPIO22PCTL Register (Offset = 00016004h) [Reset = 00000000h]

GPIO22PCTL is shown in Table 16-92.

Return to the Summary Table.

Pull control register of IO GPIO22 This register configures the pull control

Table 16-92. GPIO22PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.91 GPIO22CTL Register (Offset = 00016008h) [Reset = 00000000h]

GPIO22CTL is shown in Table 16-93.

Return to the Summary Table.

Control register of IO GPIO22 This register controls the IO state

Table 16-93. GPIO22CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.92 GPIO22ECTL Register (Offset = 0001600Ch) [Reset = 00000000h]

GPIO22ECTL is shown in Table 16-94.

Return to the Summary Table.

Event control register for IO GPIO22 This register controls the Event configuration and behaviour

Table 16-94. GPIO22ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.93 GPIO23CFG Register (Offset = 00017000h) [Reset = 00000000h]

GPIO23CFG is shown in Table 16-95.

Return to the Summary Table.

CFG register for IO GPIO23. This register configures the corresponding pad

Table 16-95. GPIO23CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.94 GPIO23PCTL Register (Offset = 00017004h) [Reset = 00000000h]

GPIO23PCTL is shown in Table 16-96.

Return to the Summary Table.

Pull control register of IO GPIO23 This register configures the pull control

Table 16-96. GPIO23PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.95 GPIO23CTL Register (Offset = 00017008h) [Reset = 00000000h]

GPIO23CTL is shown in Table 16-97.

Return to the Summary Table.

Control register of IO GPIO23 This register controls the IO state

Table 16-97. GPIO23CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.96 GPIO23ECTL Register (Offset = 0001700Ch) [Reset = 00000000h]

GPIO23ECTL is shown in Table 16-98.

Return to the Summary Table.

Event control register for IO GPIO23 This register controls the Event configuration and behaviour

Table 16-98. GPIO23ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.97 GPIO24CFG Register (Offset = 00018000h) [Reset = 00000000h]

GPIO24CFG is shown in Table 16-99.

Return to the Summary Table.

CFG register for IO GPIO24. This register configures the corresponding pad

Table 16-99. GPIO24CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	0h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.98 GPIO24PCTL Register (Offset = 00018004h) [Reset = 00000000h]

GPIO24PCTL is shown in Table 16-100.

Return to the Summary Table.

Pull control register of IO GPIO24 This register configures the pull control

Table 16-100. GPIO24PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.99 GPIO24CTL Register (Offset = 00018008h) [Reset = 00000000h]

GPIO24CTL is shown in Table 16-101.

Return to the Summary Table.

Control register of IO GPIO24 This register controls the IO state

Table 16-101. GPIO24CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.100 GPIO24ECTL Register (Offset = 0001800Ch) [Reset = 00000000h]

GPIO24ECTL is shown in Table 16-102.

Return to the Summary Table.

Event control register for IO GPIO24 This register controls the Event configuration and behaviour

Table 16-102. GPIO24ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.101 GPIO25CFG Register (Offset = 00019000h) [Reset = 00000000h]

GPIO25CFG is shown in Table 16-103.

Return to the Summary Table.

CFG register for IO GPIO25. This register configures the corresponding pad

Table 16-103. GPIO25CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.102 GPIO25PCTL Register (Offset = 00019004h) [Reset = 00000000h]

GPIO25PCTL is shown in Table 16-104.

Return to the Summary Table.

Pull control register of IO GPIO25 This register configures the pull control

Table 16-104. GPIO25PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.103 GPIO25CTL Register (Offset = 00019008h) [Reset = 00000000h]

GPIO25CTL is shown in Table 16-105.

Return to the Summary Table.

Control register of IO GPIO25 This register controls the IO state

Table 16-105. GPIO25CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.104 GPIO25ECTL Register (Offset = 0001900Ch) [Reset = 00000000h]

GPIO25ECTL is shown in Table 16-106.

Return to the Summary Table.

Event control register for IO GPIO25 This register controls the Event configuration and behaviour

Table 16-106. GPIO25ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.105 GPIO26CFG Register (Offset = 0001A000h) [Reset = 00000000h]

GPIO26CFG is shown in Table 16-107.

Return to the Summary Table.

CFG register for IO GPIO26. This register configures the corresponding pad

Table 16-107. GPIO26CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.106 GPIO26PCTL Register (Offset = 0001A004h) [Reset = 00000000h]

GPIO26PCTL is shown in Table 16-108.

Return to the Summary Table.

Pull control register of IO GPIO26 This register configures the pull control

Table 16-108. GPIO26PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.107 GPIO26CTL Register (Offset = 0001A008h) [Reset = 00000000h]

GPIO26CTL is shown in Table 16-109.

Return to the Summary Table.

Control register of IO GPIO26 This register controls the IO state

Table 16-109. GPIO26CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.108 GPIO26ECTL Register (Offset = 0001A00Ch) [Reset = 00000000h]

GPIO26ECTL is shown in Table 16-110.

Return to the Summary Table.

Event control register for IO GPIO26 This register controls the Event configuration and behaviour

Table 16-110. GPIO26ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.109 GPIO27CFG Register (Offset = 0001B000h) [Reset = 00000000h]

GPIO27CFG is shown in Table 16-111.

Return to the Summary Table.

CFG register for IO GPIO27. This register configures the corresponding pad

Table 16-111. GPIO27CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.110 GPIO27PCTL Register (Offset = 0001B004h) [Reset = 00000000h]

GPIO27PCTL is shown in Table 16-112.

Return to the Summary Table.

Pull control register of IO GPIO27 This register configures the pull control

Table 16-112. GPIO27PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.111 GPIO27CTL Register (Offset = 0001B008h) [Reset = 00000000h]

GPIO27CTL is shown in Table 16-113.

Return to the Summary Table.

Control register of IO GPIO27 This register controls the IO state

Table 16-113. GPIO27CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.112 GPIO27ECTL Register (Offset = 0001B00Ch) [Reset = 00000000h]

GPIO27ECTL is shown in Table 16-114.

Return to the Summary Table.

Event control register for IO GPIO27 This register controls the Event configuration and behaviour

Table 16-114. GPIO27ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.113 GPIO28CFG Register (Offset = 0001C000h) [Reset = 00000000h]

GPIO28CFG is shown in Table 16-115.

Return to the Summary Table.

CFG register for IO GPIO28. This register configures the corresponding pad

Table 16-115. GPIO28CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.114 GPIO28PCTL Register (Offset = 0001C004h) [Reset = 00000000h]

GPIO28PCTL is shown in Table 16-116.

Return to the Summary Table.

Pull control register of IO GPIO28 This register configures the pull control

Table 16-116. GPIO28PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.115 GPIO28CTL Register (Offset = 0001C008h) [Reset = 00000000h]

GPIO28CTL is shown in Table 16-117.

Return to the Summary Table.

Control register of IO GPIO28 This register controls the IO state

Table 16-117. GPIO28CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.116 GPIO28ECTL Register (Offset = 0001C00Ch) [Reset = 00000000h]

GPIO28ECTL is shown in Table 16-118.

Return to the Summary Table.

Event control register for IO GPIO28 This register controls the Event configuration and behaviour

Table 16-118. GPIO28ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.117 GPIO29CFG Register (Offset = 0001D000h) [Reset = 00000000h]

GPIO29CFG is shown in Table 16-119.

Return to the Summary Table.

CFG register for IO GPIO29. This register configures the corresponding pad

Table 16-119. GPIO29CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.118 GPIO29PCTL Register (Offset = 0001D004h) [Reset = 00000000h]

GPIO29PCTL is shown in Table 16-120.

Return to the Summary Table.

Pull control register of IO GPIO29 This register configures the pull control

Table 16-120. GPIO29PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.119 GPIO29CTL Register (Offset = 0001D008h) [Reset = 00000000h]

GPIO29CTL is shown in Table 16-121.

Return to the Summary Table.

Control register of IO GPIO29 This register controls the IO state

Table 16-121. GPIO29CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.120 GPIO29ECTL Register (Offset = 0001D00Ch) [Reset = 00000000h]

GPIO29ECTL is shown in Table 16-122.

Return to the Summary Table.

Event control register for IO GPIO29 This register controls the Event configuration and behaviour

Table 16-122. GPIO29ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.121 GPIO30CFG Register (Offset = 0001E000h) [Reset = 00000000h]

GPIO30CFG is shown in Table 16-123.

Return to the Summary Table.

CFG register for IO GPIO30. This register configures the corresponding pad

Table 16-123. GPIO30CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.122 GPIO30PCTL Register (Offset = 0001E004h) [Reset = 00000000h]

GPIO30PCTL is shown in Table 16-124.

Return to the Summary Table.

Pull control register of IO GPIO30 This register configures the pull control

Table 16-124. GPIO30PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.123 GPIO30CTL Register (Offset = 0001E008h) [Reset = 00000000h]

GPIO30CTL is shown in Table 16-125.

Return to the Summary Table.

Control register of IO GPIO30 This register controls the IO state

Table 16-125. GPIO30CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.124 GPIO30ECTL Register (Offset = 0001E00Ch) [Reset = 00000000h]

GPIO30ECTL is shown in Table 16-126.

Return to the Summary Table.

Event control register for IO GPIO30 This register controls the Event configuration and behaviour

Table 16-126. GPIO30ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.125 GPIO31CFG Register (Offset = 0001F000h) [Reset = 00000000h]

GPIO31CFG is shown in Table 16-127.

Return to the Summary Table.

CFG register for IO GPIO31. This register configures the corresponding pad

Table 16-127. GPIO31CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.126 GPIO31PCTL Register (Offset = 0001F004h) [Reset = 00000000h]

GPIO31PCTL is shown in Table 16-128.

Return to the Summary Table.

Pull control register of IO GPIO31 This register configures the pull control

Table 16-128. GPIO31PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.127 GPIO31CTL Register (Offset = 0001F008h) [Reset = 00000000h]

GPIO31CTL is shown in Table 16-129.

Return to the Summary Table.

Control register of IO GPIO31 This register controls the IO state

Table 16-129. GPIO31CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.128 GPIO31ECTL Register (Offset = 0001F00Ch) [Reset = 00000000h]

GPIO31ECTL is shown in Table 16-130.

Return to the Summary Table.

Event control register for IO GPIO31 This register controls the Event configuration and behaviour

Table 16-130. GPIO31ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.129 GPIO32CFG Register (Offset = 00020000h) [Reset = 00000000h]

GPIO32CFG is shown in Table 16-131.

Return to the Summary Table.

CFG register for IO GPIO32. This register configures the corresponding pad

Table 16-131. GPIO32CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.130 GPIO32PCTL Register (Offset = 00020004h) [Reset = 00000000h]

GPIO32PCTL is shown in Table 16-132.

Return to the Summary Table.

Pull control register of IO GPIO32 This register configures the pull control

Table 16-132. GPIO32PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.131 GPIO32CTL Register (Offset = 00020008h) [Reset = 00000000h]

GPIO32CTL is shown in Table 16-133.

Return to the Summary Table.

Control register of IO GPIO32 This register controls the IO state

Table 16-133. GPIO32CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.132 GPIO32ECTL Register (Offset = 0002000Ch) [Reset = 00000000h]

GPIO32ECTL is shown in Table 16-134.

Return to the Summary Table.

Event control register for IO GPIO32 This register controls the Event configuration and behaviour

Table 16-134. GPIO32ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.133 GPIO33CFG Register (Offset = 00021000h) [Reset = 00000000h]

GPIO33CFG is shown in Table 16-135.

Return to the Summary Table.

CFG register for IO GPIO33. This register configures the corresponding pad

Table 16-135. GPIO33CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.134 GPIO33PCTL Register (Offset = 00021004h) [Reset = 00000000h]

GPIO33PCTL is shown in Table 16-136.

Return to the Summary Table.

Pull control register of IO GPIO33 This register configures the pull control

Table 16-136. GPIO33PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.135 GPIO33CTL Register (Offset = 00021008h) [Reset = 00000000h]

GPIO33CTL is shown in Table 16-137.

Return to the Summary Table.

Control register of IO GPIO33 This register controls the IO state

Table 16-137. GPIO33CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.136 GPIO33ECTL Register (Offset = 0002100Ch) [Reset = 00000000h]

GPIO33ECTL is shown in Table 16-138.

Return to the Summary Table.

Event control register for IO GPIO33 This register controls the Event configuration and behaviour

Table 16-138. GPIO33ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.137 GPIO34CFG Register (Offset = 00022000h) [Reset = 00000000h]

GPIO34CFG is shown in Table 16-139.

Return to the Summary Table.

CFG register for IO GPIO34. This register configures the corresponding pad

Table 16-139. GPIO34CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.138 GPIO34PCTL Register (Offset = 00022004h) [Reset = 00000000h]

GPIO34PCTL is shown in Table 16-140.

Return to the Summary Table.

Pull control register of IO GPIO34 This register configures the pull control

Table 16-140. GPIO34PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.139 GPIO34CTL Register (Offset = 00022008h) [Reset = 00000000h]

GPIO34CTL is shown in Table 16-141.

Return to the Summary Table.

Control register of IO GPIO34 This register controls the IO state

Table 16-141. GPIO34CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.140 GPIO34ECTL Register (Offset = 0002200Ch) [Reset = 00000000h]

GPIO34ECTL is shown in Table 16-142.

Return to the Summary Table.

Event control register for IO GPIO34 This register controls the Event configuration and behaviour

Table 16-142. GPIO34ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.141 GPIO35CFG Register (Offset = 00023000h) [Reset = 00000000h]

GPIO35CFG is shown in Table 16-143.

Return to the Summary Table.

CFG register for IO GPIO35. This register configures the corresponding pad

Table 16-143. GPIO35CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.142 GPIO35PCTL Register (Offset = 00023004h) [Reset = 00000000h]

GPIO35PCTL is shown in Table 16-144.

Return to the Summary Table.

Pull control register of IO GPIO35 This register configures the pull control

Table 16-144. GPIO35PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.143 GPIO35CTL Register (Offset = 00023008h) [Reset = 00000000h]

GPIO35CTL is shown in Table 16-145.

Return to the Summary Table.

Control register of IO GPIO35 This register controls the IO state

Table 16-145. GPIO35CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.144 GPIO35ECTL Register (Offset = 0002300Ch) [Reset = 00000000h]

GPIO35ECTL is shown in Table 16-146.

Return to the Summary Table.

Event control register for IO GPIO35 This register controls the Event configuration and behaviour

Table 16-146. GPIO35ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.145 GPIO36CFG Register (Offset = 00024000h) [Reset = 00000000h]

GPIO36CFG is shown in Table 16-147.

Return to the Summary Table.

CFG register for IO GPIO36. This register configures the corresponding pad

Table 16-147. GPIO36CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.146 GPIO36PCTL Register (Offset = 00024004h) [Reset = 00000000h]

GPIO36PCTL is shown in Table 16-148.

Return to the Summary Table.

Pull control register of IO GPIO36 This register configures the pull control

Table 16-148. GPIO36PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	2h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.147 GPIO36CTL Register (Offset = 00024008h) [Reset = 00000000h]

GPIO36CTL is shown in Table 16-149.

Return to the Summary Table.

Control register of IO GPIO36 This register controls the IO state

Table 16-149. GPIO36CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.148 GPIO36ECTL Register (Offset = 0002400Ch) [Reset = 00000000h]

GPIO36ECTL is shown in Table 16-150.

Return to the Summary Table.

Event control register for IO GPIO36 This register controls the Event configuration and behaviour

Table 16-150. GPIO36ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.149 GPIO37CFG Register (Offset = 00025000h) [Reset = 00000000h]

GPIO37CFG is shown in Table 16-151.

Return to the Summary Table.

CFG register for IO GPIO37. This register configures the corresponding pad

Table 16-151. GPIO37CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.150 GPIO37PCTL Register (Offset = 00025004h) [Reset = 00000000h]

GPIO37PCTL is shown in Table 16-152.

Return to the Summary Table.

Pull control register of IO GPIO37 This register configures the pull control

Table 16-152. GPIO37PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	2h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.151 GPIO37CTL Register (Offset = 00025008h) [Reset = 00000000h]

GPIO37CTL is shown in Table 16-153.

Return to the Summary Table.

Control register of IO GPIO37 This register controls the IO state

Table 16-153. GPIO37CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.152 GPIO37ECTL Register (Offset = 0002500Ch) [Reset = 00000000h]

GPIO37ECTL is shown in Table 16-154.

Return to the Summary Table.

Event control register for IO GPIO37 This register controls the Event configuration and behaviour

Table 16-154. GPIO37ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.153 GPIO38CFG Register (Offset = 00026000h) [Reset = 00000000h]

GPIO38CFG is shown in Table 16-155.

Return to the Summary Table.

CFG register for IO GPIO38. This register configures the corresponding pad

Table 16-155. GPIO38CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.154 GPIO38PCTL Register (Offset = 00026004h) [Reset = 00000000h]

GPIO38PCTL is shown in Table 16-156.

Return to the Summary Table.

Pull control register of IO GPIO38 This register configures the pull control

Table 16-156. GPIO38PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.155 GPIO38CTL Register (Offset = 00026008h) [Reset = 00000000h]

GPIO38CTL is shown in Table 16-157.

Return to the Summary Table.

Control register of IO GPIO38 This register controls the IO state

Table 16-157. GPIO38CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.156 GPIO38ECTL Register (Offset = 0002600Ch) [Reset = 00000000h]

GPIO38ECTL is shown in Table 16-158.

Return to the Summary Table.

Event control register for IO GPIO38 This register controls the Event configuration and behaviour

Table 16-158. GPIO38ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.157 GPIO39CFG Register (Offset = 00027000h) [Reset = 00000000h]

GPIO39CFG is shown in Table 16-159.

Return to the Summary Table.

CFG register for IO GPIO39. This register configures the corresponding pad

Table 16-159. GPIO39CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.158 GPIO39PCTL Register (Offset = 00027004h) [Reset = 00000000h]

GPIO39PCTL is shown in Table 16-160.

Return to the Summary Table.

Pull control register of IO GPIO39 This register configures the pull control

Table 16-160. GPIO39PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.159 GPIO39CTL Register (Offset = 00027008h) [Reset = 00000000h]

GPIO39CTL is shown in Table 16-161.

Return to the Summary Table.

Control register of IO GPIO39 This register controls the IO state

Table 16-161. GPIO39CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.160 GPIO39ECTL Register (Offset = 0002700Ch) [Reset = 00000000h]

GPIO39ECTL is shown in Table 16-162.

Return to the Summary Table.

Event control register for IO GPIO39 This register controls the Event configuration and behaviour

Table 16-162. GPIO39ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.161 GPIO40CFG Register (Offset = 00028000h) [Reset = 00000000h]

GPIO40CFG is shown in Table 16-163.

Return to the Summary Table.

CFG register for IO GPIO40. This register configures the corresponding pad

Table 16-163. GPIO40CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.162 GPIO40PCTL Register (Offset = 00028004h) [Reset = 00000000h]

GPIO40PCTL is shown in Table 16-164.

Return to the Summary Table.

Pull control register of IO GPIO40 This register configures the pull control

Table 16-164. GPIO40PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.163 GPIO40CTL Register (Offset = 00028008h) [Reset = 00000000h]

GPIO40CTL is shown in Table 16-165.

Return to the Summary Table.

Control register of IO GPIO40 This register controls the IO state

Table 16-165. GPIO40CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.164 GPIO40ECTL Register (Offset = 0002800Ch) [Reset = 00000000h]

GPIO40ECTL is shown in Table 16-166.

Return to the Summary Table.

Event control register for IO GPIO40 This register controls the Event configuration and behaviour

Table 16-166. GPIO40ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.165 GPIO41CFG Register (Offset = 00029000h) [Reset = 00000000h]

GPIO41CFG is shown in Table 16-167.

Return to the Summary Table.

CFG register for IO GPIO41. This register configures the corresponding pad

Table 16-167. GPIO41CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.166 GPIO41PCTL Register (Offset = 00029004h) [Reset = 00000000h]

GPIO41PCTL is shown in Table 16-168.

Return to the Summary Table.

Pull control register of IO GPIO41 This register configures the pull control

Table 16-168. GPIO41PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.167 GPIO41CTL Register (Offset = 00029008h) [Reset = 00000000h]

GPIO41CTL is shown in Table 16-169.

Return to the Summary Table.

Control register of IO GPIO41 This register controls the IO state

Table 16-169. GPIO41CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.168 GPIO41ECTL Register (Offset = 0002900Ch) [Reset = 00000000h]

GPIO41ECTL is shown in Table 16-170.

Return to the Summary Table.

Event control register for IO GPIO41 This register controls the Event configuration and behaviour

Table 16-170. GPIO41ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.169 GPIO42CFG Register (Offset = 0002A000h) [Reset = 00000000h]

GPIO42CFG is shown in Table 16-171.

Return to the Summary Table.

CFG register for IO GPIO42. This register configures the corresponding pad

Table 16-171. GPIO42CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.170 GPIO42PCTL Register (Offset = 0002A004h) [Reset = 00000000h]

GPIO42PCTL is shown in Table 16-172.

Return to the Summary Table.

Pull control register of IO GPIO42 This register configures the pull control

Table 16-172. GPIO42PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.171 GPIO42CTL Register (Offset = 0002A008h) [Reset = 00000000h]

GPIO42CTL is shown in Table 16-173.

Return to the Summary Table.

Control register of IO GPIO42 This register controls the IO state

Table 16-173. GPIO42CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.172 GPIO42ECTL Register (Offset = 0002A00Ch) [Reset = 00000000h]

GPIO42ECTL is shown in Table 16-174.

Return to the Summary Table.

Event control register for IO GPIO42 This register controls the Event configuration and behaviour

Table 16-174. GPIO42ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.173 GPIO43CFG Register (Offset = 0002B000h) [Reset = 00000000h]

GPIO43CFG is shown in Table 16-175.

Return to the Summary Table.

CFG register for IO GPIO43. This register configures the corresponding pad

Table 16-175. GPIO43CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.174 GPIO43PCTL Register (Offset = 0002B004h) [Reset = 00000000h]

GPIO43PCTL is shown in Table 16-176.

Return to the Summary Table.

Pull control register of IO GPIO43 This register configures the pull control

Table 16-176. GPIO43PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.175 GPIO43CTL Register (Offset = 0002B008h) [Reset = 00000000h]

GPIO43CTL is shown in Table 16-177.

Return to the Summary Table.

Control register of IO GPIO43 This register controls the IO state

Table 16-177. GPIO43CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.176 GPIO43ECTL Register (Offset = 0002B00Ch) [Reset = 00000000h]

GPIO43ECTL is shown in Table 16-178.

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Event control register for IO GPIO43 This register controls the Event configuration and behaviour

Table 16-178. GPIO43ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.177 GPIO44CFG Register (Offset = 0002C000h) [Reset = 00000000h]

GPIO44CFG is shown in Table 16-179.

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CFG register for IO GPIO44. This register configures the corresponding pad

Table 16-179. GPIO44CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.178 GPIO44PCTL Register (Offset = 0002C004h) [Reset = 00000000h]

GPIO44PCTL is shown in Table 16-180.

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Pull control register of IO GPIO44 This register configures the pull control

Table 16-180. GPIO44PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.179 GPIO44CTL Register (Offset = 0002C008h) [Reset = 00000000h]

GPIO44CTL is shown in Table 16-181.

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Control register of IO GPIO44 This register controls the IO state

Table 16-181. GPIO44CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.180 GPIO44ECTL Register (Offset = 0002C00Ch) [Reset = 00000000h]

GPIO44ECTL is shown in Table 16-182.

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Event control register for IO GPIO44 This register controls the Event configuration and behaviour

Table 16-182. GPIO44ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.181 SCLKIPCFG Register (Offset = 0002D004h) [Reset = 00000000h]

SCLKIPCFG is shown in Table 16-183.

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Port configuration register for IO SLOW_CLOCK_IN

Table 16-183. SCLKIPCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- slow_clock_in sel 5'd2 -- wifi_gpio_0 sel 5'd9 -- gpt1_1 sel 5'd10 -- gpt0_1 sel 5'd21 -- coex_req 0h = reserved 1h = slow_clock_in 2h = wifi_gpio_0 3h = reserved 4h = reserved 5h = reserved 6h = reserved 7h = reserved 8h = reserved 9h = gpt1_1 Ah = gpt0_1 Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = reserved 13h = reserved 14h = reserved 15h = coex_req 16h = reserved 17h = reserved 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.182 LFXTNPCFG Register (Offset = 0002D008h) [Reset = 00000000h]

LFXTNPCFG is shown in Table 16-184.

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Port configuration register for IO LFXTAL_N

Table 16-184. LFXTNPCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd0 -- lfxt_n sel 5'd2 -- wifi_gpio_1 sel 5'd7 -- gpt1_pre_event sel 5'd8 -- gpt0_pre_event sel 5'd9 -- gpt1_0 sel 5'd10 -- gpt0_0 sel 5'd11 -- gpt_infrared sel 5'd19 -- sdio_oob_irq sel 5'd20 -- coex_grant sel 5'd21 -- coex_req sel 5'd23 -- ant_sel_0 0h = lfxt_n 1h = reserved 2h = wifi_gpio_1 3h = reserved 4h = reserved 5h = reserved 6h = reserved 7h = gpt1_pre_event 8h = gpt0_pre_event 9h = gpt1_0 Ah = gpt0_0 Bh = gpt_infrared Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = reserved 13h = sdio_oob_irq 14h = coex_grant 15h = coex_req 16h = reserved 17h = ant_sel_0 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.183 GPIO2PCFG Register (Offset = 0002D00Ch) [Reset = 00000000h]

GPIO2PCFG is shown in Table 16-185.

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Port configuration register for IO GPIO2

Table 16-185. GPIO2PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- xspi_reset_ram sel 5'd2 -- wifi_gpio_2 sel 5'd3 -- sdio_mmc_cd sel 5'd6 -- i2c1_clk sel 5'd9 -- gpt1_3 sel 5'd10 -- dcan_tx sel 5'd11 -- wake_observe_bus_6 sel 5'd12 -- debug_bus_4 sel 5'd16 -- spi0_cs4 sel 5'd18 -- gpt1_pre_event sel 5'd19 -- sdio_oob_irq sel 5'd20 -- coex_grant sel 5'd21 -- coex_req sel 5'd22 -- ble_rftrc sel 5'd23 -- ant_sel_2 sel 5'd24 -- cca sel 5'd26 -- trclk 0h = reserved 1h = xspi_reset_ram 2h = wifi_gpio_2 3h = sdio_mmc_cd 4h = reserved 5h = reserved 6h = i2c1_clk 7h = reserved 8h = reserved 9h = gpt1_3 Ah = dcan_tx Bh = wake_observe_bus_6 Ch = debug_bus_4 Dh = reserved Eh = reserved Fh = reserved 10h = spi0_cs4 11h = reserved 12h = gpt1_pre_event 13h = sdio_oob_irq 14h = coex_grant 15h = coex_req 16h = ble_rftrc 17h = ant_sel_2 18h = cca 19h = reserved 1Ah = trclk 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.184 GPIO3PCFG Register (Offset = 0002D010h) [Reset = 00000000h]

GPIO3PCFG is shown in Table 16-186.

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Port configuration register for IO GPIO3

Table 16-186. GPIO3PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- uart1_tx sel 5'd2 -- wifi_gpio_3 sel 5'd3 -- sdio_mmc_wp sel 5'd4 -- spi1_clk sel 5'd5 -- uart1_rts sel 5'd6 -- i2s_mclk sel 5'd7 -- i2s_data0 sel 5'd8 -- pdm_data1 sel 5'd9 -- gpt1_0 sel 5'd10 -- dcan_rx sel 5'd11 -- wake_observe_bus_7 sel 5'd12 -- debug_bus_0 sel 5'd16 -- spi0_cs3 sel 5'd17 -- xspi_cs_ram sel 5'd18 -- gpt1_1_n sel 5'd19 -- sdio_clk sel 5'd20 -- coex_req sel 5'd21 -- gpt0_0_n sel 5'd22 -- gpt_infrared sel 5'd23 -- ant_sel_3 sel 5'd24 -- ble_rfc_gpo_7 sel 5'd25 -- swo_m3 sel 5'd27 -- swo_m33 sel 5'd28 -- i2c1_data sel 5'd30 -- uart2_tx 0h = reserved 1h = uart1_tx 2h = wifi_gpio_3 3h = sdio_mmc_wp 4h = spi1_clk 5h = uart1_rts 6h = i2s_mclk 7h = i2s_data0 8h = pdm_data1 9h = gpt1_0 Ah = dcan_rx Bh = wake_observe_bus_7 Ch = debug_bus_0 Dh = reserved Eh = reserved Fh = reserved 10h = spi0_cs3 11h = xspi_cs_ram 12h = gpt1_1_n 13h = sdio_clk 14h = coex_req 15h = gpt0_0_n 16h = gpt_infrared 17h = ant_sel_3 18h = ble_rfc_gpo_7 19h = swo_m3 1Ah = reserved 1Bh = swo_m33 1Ch = i2c1_data 1Dh = reserved 1Eh = uart2_tx 1Fh = reserved

16.8.185 GPIO4PCFG Register (Offset = 0002D014h) [Reset = 00000000h]

GPIO4PCFG is shown in Table 16-187.

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Port configuration register for IO GPIO4

Table 16-187. GPIO4PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- uart1_rx sel 5'd2 -- wifi_gpio_4 sel 5'd3 -- sdio_mmc_cd sel 5'd4 -- spi1_cs1 sel 5'd5 -- uart1_cts sel 5'd6 -- i2s_bclk sel 5'd7 -- i2s_data1 sel 5'd8 -- pdm_bclk sel 5'd9 -- gpt1_1 sel 5'd10 -- dcan_tx sel 5'd11 -- wake_observe_bus_8 sel 5'd12 -- debug_bus_1 sel 5'd16 -- spi0_cs2 sel 5'd17 -- ext_clk sel 5'd18 -- gpt1_0_n sel 5'd19 -- sdio_cmd sel 5'd20 -- coex_priority sel 5'd21 -- gpt0_1_n sel 5'd24 -- ble_rfc_gpo_6 sel 5'd28 -- i2c1_clk sel 5'd30 -- uart2_rx 0h = reserved 1h = uart1_rx 2h = wifi_gpio_4 3h = sdio_mmc_cd 4h = spi1_cs1 5h = uart1_cts 6h = i2s_bclk 7h = i2s_data1 8h = pdm_bclk 9h = gpt1_1 Ah = dcan_tx Bh = wake_observe_bus_8 Ch = debug_bus_1 Dh = reserved Eh = reserved Fh = reserved 10h = spi0_cs2 11h = ext_clk 12h = gpt1_0_n 13h = sdio_cmd 14h = coex_priority 15h = gpt0_1_n 16h = reserved 17h = reserved 18h = ble_rfc_gpo_6 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = i2c1_clk 1Dh = reserved 1Eh = uart2_rx 1Fh = reserved

16.8.186 GPIO5PCFG Register (Offset = 0002D018h) [Reset = 00000000h]

GPIO5PCFG is shown in Table 16-188.

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Port configuration register for IO GPIO5

Table 16-188. GPIO5PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- xspi_reset_ram sel 5'd2 -- wifi_gpio_5 sel 5'd3 -- sdio_mmc_pow2 sel 5'd4 -- spi1_miso sel 5'd5 -- uart1_tx sel 5'd6 -- i2c0_clk sel 5'd7 -- i2s_mclk sel 5'd8 -- pdm_bclk sel 5'd9 -- gpt1_2 sel 5'd10 -- dcan_tx sel 5'd11 -- jtag_tdi sel 5'd12 -- debug_bus_11 sel 5'd16 -- spi0_cs4 sel 5'd17 -- ext_clk sel 5'd18 -- gpt1_0_n sel 5'd19 -- sdio_d0 sel 5'd20 -- coex_req sel 5'd21 -- gpt0_2_n sel 5'd22 -- ble_rftrc sel 5'd23 -- ant_sel_1 sel 5'd25 -- ble_rfc_gpi_2 sel 5'd28 -- i2c1_data sel 5'd30 -- uart2_rts 0h = reserved 1h = xspi_reset_ram 2h = wifi_gpio_5 3h = sdio_mmc_pow2 4h = spi1_miso 5h = uart1_tx 6h = i2c0_clk 7h = i2s_mclk 8h = pdm_bclk 9h = gpt1_2 Ah = dcan_tx Bh = jtag_tdi Ch = debug_bus_11 Dh = reserved Eh = reserved Fh = reserved 10h = spi0_cs4 11h = ext_clk 12h = gpt1_0_n 13h = sdio_d0 14h = coex_req 15h = gpt0_2_n 16h = ble_rftrc 17h = ant_sel_1 18h = reserved 19h = ble_rfc_gpi_2 1Ah = reserved 1Bh = reserved 1Ch = i2c1_data 1Dh = reserved 1Eh = uart2_rts 1Fh = reserved

16.8.187 GPIO6PCFG Register (Offset = 0002D01Ch) [Reset = 00000000h]

GPIO6PCFG is shown in Table 16-189.

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Port configuration register for IO GPIO6

Table 16-189. GPIO6PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- xspi_cs_ram sel 5'd2 -- wifi_gpio_6 sel 5'd3 -- sdio_mmc_pow1 sel 5'd4 -- spi1_mosi sel 5'd5 -- uart1_rx sel 5'd6 -- i2c0_data sel 5'd7 -- i2s_wclk sel 5'd8 -- pdm_data0 sel 5'd9 -- gpt1_3 sel 5'd10 -- dcan_rx sel 5'd11 -- sdio_mmc_wp sel 5'd12 -- debug_bus_12 sel 5'd16 -- spi0_cs4 sel 5'd17 -- i2s_bclk sel 5'd18 -- gpt1_1_n sel 5'd19 -- sdio_d1 sel 5'd20 -- coex_priority sel 5'd21 -- gpt0_3_n sel 5'd22 -- gpt1_pre_event sel 5'd23 -- ant_sel_0 sel 5'd24 -- cca sel 5'd25 -- ble_rfc_gpi_3 sel 5'd26 -- coex_grant sel 5'd28 -- i2c1_clk sel 5'd29 -- sdio_mmc_pow2 sel 5'd30 -- uart2_cts 0h = reserved 1h = xspi_cs_ram 2h = wifi_gpio_6 3h = sdio_mmc_pow1 4h = spi1_mosi 5h = uart1_rx 6h = i2c0_data 7h = i2s_wclk 8h = pdm_data0 9h = gpt1_3 Ah = dcan_rx Bh = sdio_mmc_wp Ch = debug_bus_12 Dh = reserved Eh = reserved Fh = reserved 10h = spi0_cs4 11h = i2s_bclk 12h = gpt1_1_n 13h = sdio_d1 14h = coex_priority 15h = gpt0_3_n 16h = gpt1_pre_event 17h = ant_sel_0 18h = cca 19h = ble_rfc_gpi_3 1Ah = coex_grant 1Bh = reserved 1Ch = i2c1_clk 1Dh = sdio_mmc_pow2 1Eh = uart2_cts 1Fh = reserved

16.8.188 SWDIOPCFG Register (Offset = 0002D020h) [Reset = 00000000h]

SWDIOPCFG is shown in Table 16-190.

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Port configuration register for IO SWDIO

Table 16-190. SWDIOPCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd0 -- swdio sel 5'd2 -- wifi_gpio_7 sel 5'd3 -- sdio_mmc_pow2 sel 5'd4 -- jtag_tms sel 5'd23 -- ant_sel_0 0h = swdio 1h = reserved 2h = wifi_gpio_7 3h = sdio_mmc_pow2 4h = jtag_tms 5h = reserved 6h = reserved 7h = reserved 8h = reserved 9h = reserved Ah = reserved Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = reserved 13h = reserved 14h = reserved 15h = reserved 16h = reserved 17h = ant_sel_0 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.189 SWCLKPCFG Register (Offset = 0002D024h) [Reset = 00000000h]

SWCLKPCFG is shown in Table 16-191.

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Port configuration register for IO SWCLK

Table 16-191. SWCLKPCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd0 -- swclk sel 5'd2 -- wifi_gpio_8 sel 5'd3 -- sdio_mmc_pow1 sel 5'd4 -- jtag_tck sel 5'd23 -- ant_sel_1 0h = swclk 1h = reserved 2h = wifi_gpio_8 3h = sdio_mmc_pow1 4h = jtag_tck 5h = reserved 6h = reserved 7h = reserved 8h = reserved 9h = reserved Ah = reserved Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = reserved 13h = reserved 14h = reserved 15h = reserved 16h = reserved 17h = ant_sel_1 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.190 LOGGERPCFG Register (Offset = 0002D028h) [Reset = 00000000h]

LOGGERPCFG is shown in Table 16-192.

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Port configuration register for IO LOGGER

Table 16-192. LOGGERPCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- logger sel 5'd2 -- wifi_gpio_9 sel 5'd3 -- sdio_mmc_cd sel 5'd4 -- ble_rftrc sel 5'd11 -- jtag_tdo sel 5'd23 -- ant_sel_2 sel 5'd26 -- swo_m3 sel 5'd27 -- swo_m33 0h = reserved 1h = logger 2h = wifi_gpio_9 3h = sdio_mmc_cd 4h = ble_rftrc 5h = reserved 6h = reserved 7h = reserved 8h = reserved 9h = reserved Ah = reserved Bh = jtag_tdo Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = reserved 13h = reserved 14h = reserved 15h = reserved 16h = reserved 17h = ant_sel_2 18h = reserved 19h = reserved 1Ah = swo_m3 1Bh = swo_m33 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.191 GPIO10PCFG Register (Offset = 0002D02Ch) [Reset = 00000000h]

GPIO10PCFG is shown in Table 16-193.

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Port configuration register for IO GPIO10

Table 16-193. GPIO10PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- uart1_tx sel 5'd2 -- wifi_gpio_10 sel 5'd3 -- sdio_mmc_data_3 sel 5'd4 -- spi1_clk sel 5'd5 -- uart1_rts sel 5'd6 -- i2c1_data sel 5'd7 -- i2s_data1 sel 5'd8 -- pdm_data1 sel 5'd9 -- gpt1_0 sel 5'd10 -- dcan_rx sel 5'd11 -- uart_rs232_rx sel 5'd12 -- debug_bus_10 sel 5'd16 -- spi0_cs3 sel 5'd18 -- gpt1_3_n sel 5'd19 -- sdio_d3 sel 5'd20 -- coex_priority sel 5'd21 -- coex_grant sel 5'd23 -- ant_sel_2 sel 5'd24 -- cca sel 5'd25 -- ble_rfc_gpi_1 sel 5'd26 -- trdata_0 sel 5'd30 -- uart2_rts sel 5'd31 -- uart2_tx 0h = reserved 1h = uart1_tx 2h = wifi_gpio_10 3h = sdio_mmc_data_3 4h = spi1_clk 5h = uart1_rts 6h = i2c1_data 7h = i2s_data1 8h = pdm_data1 9h = gpt1_0 Ah = dcan_rx Bh = uart_rs232_rx Ch = debug_bus_10 Dh = reserved Eh = reserved Fh = reserved 10h = spi0_cs3 11h = reserved 12h = gpt1_3_n 13h = sdio_d3 14h = coex_priority 15h = coex_grant 16h = reserved 17h = ant_sel_2 18h = cca 19h = ble_rfc_gpi_1 1Ah = trdata_0 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = uart2_rts 1Fh = uart2_tx

16.8.192 GPIO11PCFG Register (Offset = 0002D030h) [Reset = 00000000h]

GPIO11PCFG is shown in Table 16-194.

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Port configuration register for IO GPIO11

Table 16-194. GPIO11PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- uart1_rx sel 5'd2 -- wifi_gpio_11 sel 5'd3 -- sdio_mmc_data_2 sel 5'd4 -- spi1_cs1 sel 5'd5 -- uart1_cts sel 5'd6 -- i2c1_clk sel 5'd7 -- i2s_data0 sel 5'd8 -- pdm_data0 sel 5'd9 -- gpt1_1 sel 5'd10 -- dcan_tx sel 5'd11 -- uart_rs232_tx sel 5'd12 -- debug_bus_9 sel 5'd16 -- spi0_cs2 sel 5'd17 -- ext_clk sel 5'd18 -- gpt1_2_n sel 5'd19 -- sdio_d2 sel 5'd20 -- coex_req sel 5'd23 -- ant_sel_3 sel 5'd24 -- cca sel 5'd25 -- swo_m3 sel 5'd26 -- trdata_1 sel 5'd30 -- uart2_cts sel 5'd31 -- uart2_rx 0h = reserved 1h = uart1_rx 2h = wifi_gpio_11 3h = sdio_mmc_data_2 4h = spi1_cs1 5h = uart1_cts 6h = i2c1_clk 7h = i2s_data0 8h = pdm_data0 9h = gpt1_1 Ah = dcan_tx Bh = uart_rs232_tx Ch = debug_bus_9 Dh = reserved Eh = reserved Fh = reserved 10h = spi0_cs2 11h = ext_clk 12h = gpt1_2_n 13h = sdio_d2 14h = coex_req 15h = reserved 16h = reserved 17h = ant_sel_3 18h = cca 19h = swo_m3 1Ah = trdata_1 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = uart2_cts 1Fh = uart2_rx

16.8.193 GPIO12PCFG Register (Offset = 0002D034h) [Reset = 00000000h]

GPIO12PCFG is shown in Table 16-195.

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Port configuration register for IO GPIO12

Table 16-195. GPIO12PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd2 -- wifi_gpio_12 sel 5'd3 -- sdio_mmc_data_1 sel 5'd4 -- spi1_cs1 sel 5'd5 -- uart1_rts sel 5'd6 -- uart0_rts sel 5'd7 -- i2s_wclk sel 5'd9 -- gpt1_2 sel 5'd10 -- uart_rs232_tx sel 5'd11 -- jtag_tdo sel 5'd12 -- debug_bus_8 sel 5'd16 -- gpt0_pre_event sel 5'd17 -- gpt1_pre_event sel 5'd18 -- gpt1_3_n sel 5'd19 -- sdio_clk sel 5'd22 -- ble_rfc_gpo_7 sel 5'd23 -- ant_sel_1 sel 5'd25 -- ble_rfc_gpi_2 sel 5'd26 -- trdata_2 sel 5'd31 -- uart2_tx 0h = reserved 1h = reserved 2h = wifi_gpio_12 3h = sdio_mmc_data_1 4h = spi1_cs1 5h = uart1_rts 6h = uart0_rts 7h = i2s_wclk 8h = reserved 9h = gpt1_2 Ah = uart_rs232_tx Bh = jtag_tdo Ch = debug_bus_8 Dh = reserved Eh = reserved Fh = reserved 10h = gpt0_pre_event 11h = gpt1_pre_event 12h = gpt1_3_n 13h = sdio_clk 14h = reserved 15h = reserved 16h = ble_rfc_gpo_7 17h = ant_sel_1 18h = reserved 19h = ble_rfc_gpi_2 1Ah = trdata_2 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = uart2_tx

16.8.194 GPIO13PCFG Register (Offset = 0002D038h) [Reset = 00000000h]

GPIO13PCFG is shown in Table 16-196.

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Port configuration register for IO GPIO13

Table 16-196. GPIO13PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd2 -- wifi_gpio_13 sel 5'd3 -- sdio_mmc_data_0 sel 5'd4 -- spi1_mosi sel 5'd5 -- uart1_cts sel 5'd6 -- uart0_tx sel 5'd7 -- i2s_bclk sel 5'd8 -- i2s_mclk sel 5'd9 -- gpt1_3 sel 5'd11 -- wake_observe_bus_14 sel 5'd12 -- debug_bus_7 sel 5'd18 -- gpt1_2_n sel 5'd19 -- sdio_cmd sel 5'd20 -- coex_priority sel 5'd21 -- ble_rftrc sel 5'd22 -- ble_rfc_gpo_6 sel 5'd23 -- ant_sel_0 sel 5'd25 -- ble_rfc_gpi_1 sel 5'd26 -- trdata_3 sel 5'd31 -- uart2_rx 0h = reserved 1h = reserved 2h = wifi_gpio_13 3h = sdio_mmc_data_0 4h = spi1_mosi 5h = uart1_cts 6h = uart0_tx 7h = i2s_bclk 8h = i2s_mclk 9h = gpt1_3 Ah = reserved Bh = wake_observe_bus_14 Ch = debug_bus_7 Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = gpt1_2_n 13h = sdio_cmd 14h = coex_priority 15h = ble_rftrc 16h = ble_rfc_gpo_6 17h = ant_sel_0 18h = reserved 19h = ble_rfc_gpi_1 1Ah = trdata_3 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = uart2_rx

16.8.195 GPIO14PCFG Register (Offset = 0002D03Ch) [Reset = 00000000h]

GPIO14PCFG is shown in Table 16-197.

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Port configuration register for IO GPIO14

Table 16-197. GPIO14PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd2 -- wifi_gpio_14 sel 5'd3 -- sdio_mmc_clk sel 5'd4 -- spi1_clk sel 5'd5 -- uart1_tx sel 5'd6 -- uart0_rx sel 5'd9 -- gpt1_0 sel 5'd11 -- wake_observe_bus_15 sel 5'd12 -- debug_bus_clk sel 5'd16 -- spi0_cs2 sel 5'd17 -- gpt1_pre_event sel 5'd18 -- gpt1_1_n sel 5'd19 -- sdio_d0 sel 5'd20 -- coex_grant sel 5'd22 -- ble_rfc_gpo_4 sel 5'd24 -- ble_rfc_gpi_2 sel 5'd25 -- ble_rfc_gpi_1 sel 5'd26 -- trclk sel 5'd27 -- digital_fast_clk_in 0h = reserved 1h = reserved 2h = wifi_gpio_14 3h = sdio_mmc_clk 4h = spi1_clk 5h = uart1_tx 6h = uart0_rx 7h = reserved 8h = reserved 9h = gpt1_0 Ah = reserved Bh = wake_observe_bus_15 Ch = debug_bus_clk Dh = reserved Eh = reserved Fh = reserved 10h = spi0_cs2 11h = gpt1_pre_event 12h = gpt1_1_n 13h = sdio_d0 14h = coex_grant 15h = reserved 16h = ble_rfc_gpo_4 17h = reserved 18h = ble_rfc_gpi_2 19h = ble_rfc_gpi_1 1Ah = trclk 1Bh = digital_fast_clk_in 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.196 GPIO15PCFG Register (Offset = 0002D040h) [Reset = 00000000h]

GPIO15PCFG is shown in Table 16-198.

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Port configuration register for IO GPIO15

Table 16-198. GPIO15PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd2 -- wifi_gpio_15 sel 5'd3 -- sdio_mmc_cmd sel 5'd4 -- spi1_miso sel 5'd5 -- uart1_rx sel 5'd6 -- uart0_cts sel 5'd9 -- gpt1_1 sel 5'd10 -- uart_rs232_rx sel 5'd11 -- jtag_tdi sel 5'd12 -- debug_bus_6 sel 5'd16 -- spi1_cs2 sel 5'd17 -- gpt0_pre_event sel 5'd18 -- gpt1_0_n sel 5'd19 -- sdio_d1 sel 5'd20 -- coex_req sel 5'd21 -- ble_rftrc sel 5'd22 -- ble_rfc_gpo_5 sel 5'd25 -- ble_rfc_gpi_3 sel 5'd26 -- swo_m3 sel 5'd27 -- swo_m33 0h = reserved 1h = reserved 2h = wifi_gpio_15 3h = sdio_mmc_cmd 4h = spi1_miso 5h = uart1_rx 6h = uart0_cts 7h = reserved 8h = reserved 9h = gpt1_1 Ah = uart_rs232_rx Bh = jtag_tdi Ch = debug_bus_6 Dh = reserved Eh = reserved Fh = reserved 10h = spi1_cs2 11h = gpt0_pre_event 12h = gpt1_0_n 13h = sdio_d1 14h = coex_req 15h = ble_rftrc 16h = ble_rfc_gpo_5 17h = reserved 18h = reserved 19h = ble_rfc_gpi_3 1Ah = swo_m3 1Bh = swo_m33 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.197 GPIO16PCFG Register (Offset = 0002D044h) [Reset = 00000000h]

GPIO16PCFG is shown in Table 16-199.

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Port configuration register for IO GPIO16

Table 16-199. GPIO16PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd2 -- wifi_gpio_16 sel 5'd3 -- sdio_mmc_data_7 sel 5'd4 -- spi0_cs1 sel 5'd5 -- uart0_rts sel 5'd6 -- i2c1_data sel 5'd7 -- i2s_wclk sel 5'd8 -- pdm_bclk sel 5'd9 -- gpt0_0 sel 5'd10 -- uart_rs232_rx sel 5'd11 -- wake_observe_bus_12 sel 5'd12 -- debug_bus_5 sel 5'd16 -- spi1_cs2 sel 5'd18 -- gpt0_1_n sel 5'd19 -- sdio_d2 sel 5'd21 -- gpt1_0_n sel 5'd22 -- gpt_infrared sel 5'd23 -- ant_sel_0 sel 5'd26 -- trdata_0 sel 5'd30 -- uart2_tx 0h = reserved 1h = reserved 2h = wifi_gpio_16 3h = sdio_mmc_data_7 4h = spi0_cs1 5h = uart0_rts 6h = i2c1_data 7h = i2s_wclk 8h = pdm_bclk 9h = gpt0_0 Ah = uart_rs232_rx Bh = wake_observe_bus_12 Ch = debug_bus_5 Dh = reserved Eh = reserved Fh = reserved 10h = spi1_cs2 11h = reserved 12h = gpt0_1_n 13h = sdio_d2 14h = reserved 15h = gpt1_0_n 16h = gpt_infrared 17h = ant_sel_0 18h = reserved 19h = reserved 1Ah = trdata_0 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = uart2_tx 1Fh = reserved

16.8.198 GPIO17PCFG Register (Offset = 0002D048h) [Reset = 00000000h]

GPIO17PCFG is shown in Table 16-200.

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Port configuration register for IO GPIO17

Table 16-200. GPIO17PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- sdio_mmc_wp sel 5'd2 -- wifi_gpio_17 sel 5'd3 -- sdio_mmc_data_6 sel 5'd4 -- spi0_clk sel 5'd5 -- uart0_tx sel 5'd6 -- i2c0_clk sel 5'd7 -- i2s_data1 sel 5'd8 -- pdm_data0 sel 5'd9 -- gpt0_1 sel 5'd10 -- uart_rs232_tx sel 5'd11 -- wake_observe_bus_9 sel 5'd12 -- debug_bus_2 sel 5'd16 -- spi1_cs3 sel 5'd17 -- sdio_oob_irq sel 5'd18 -- gpt0_0_n sel 5'd20 -- coex_grant sel 5'd21 -- gpt1_1_n sel 5'd23 -- ant_sel_1 sel 5'd26 -- trdata_1 0h = reserved 1h = sdio_mmc_wp 2h = wifi_gpio_17 3h = sdio_mmc_data_6 4h = spi0_clk 5h = uart0_tx 6h = i2c0_clk 7h = i2s_data1 8h = pdm_data0 9h = gpt0_1 Ah = uart_rs232_tx Bh = wake_observe_bus_9 Ch = debug_bus_2 Dh = reserved Eh = reserved Fh = reserved 10h = spi1_cs3 11h = sdio_oob_irq 12h = gpt0_0_n 13h = reserved 14h = coex_grant 15h = gpt1_1_n 16h = reserved 17h = ant_sel_1 18h = reserved 19h = reserved 1Ah = trdata_1 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.199 GPIO18PCFG Register (Offset = 0002D04Ch) [Reset = 00000000h]

GPIO18PCFG is shown in Table 16-201.

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Port configuration register for IO GPIO18

Table 16-201. GPIO18PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd2 -- wifi_gpio_18 sel 5'd3 -- sdio_mmc_data_5 sel 5'd4 -- spi0_miso sel 5'd5 -- uart0_rx sel 5'd6 -- i2c0_data sel 5'd7 -- i2s_data0 sel 5'd8 -- pdm_data1 sel 5'd9 -- gpt0_2 sel 5'd10 -- dcan_tx sel 5'd11 -- wake_observe_bus_10 sel 5'd12 -- debug_bus_3 sel 5'd16 -- spi1_cs4 sel 5'd17 -- sdio_oob_irq sel 5'd18 -- gpt0_0_n sel 5'd20 -- coex_req sel 5'd21 -- gpt1_2_n sel 5'd23 -- ant_sel_2 sel 5'd26 -- trdata_2 0h = reserved 1h = reserved 2h = wifi_gpio_18 3h = sdio_mmc_data_5 4h = spi0_miso 5h = uart0_rx 6h = i2c0_data 7h = i2s_data0 8h = pdm_data1 9h = gpt0_2 Ah = dcan_tx Bh = wake_observe_bus_10 Ch = debug_bus_3 Dh = reserved Eh = reserved Fh = reserved 10h = spi1_cs4 11h = sdio_oob_irq 12h = gpt0_0_n 13h = reserved 14h = coex_req 15h = gpt1_2_n 16h = reserved 17h = ant_sel_2 18h = reserved 19h = reserved 1Ah = trdata_2 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.200 GPIO19PCFG Register (Offset = 0002D050h) [Reset = 00000000h]

GPIO19PCFG is shown in Table 16-202.

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Port configuration register for IO GPIO19

Table 16-202. GPIO19PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd2 -- wifi_gpio_19 sel 5'd3 -- sdio_mmc_data_4 sel 5'd4 -- spi0_mosi sel 5'd5 -- uart0_cts sel 5'd6 -- i2c1_clk sel 5'd7 -- i2s_bclk sel 5'd8 -- pdm_data0 sel 5'd9 -- gpt0_3 sel 5'd10 -- dcan_rx sel 5'd11 -- wake_observe_bus_11 sel 5'd12 -- debug_bus_4 sel 5'd16 -- gpt0_pre_event sel 5'd17 -- sdio_oob_irq sel 5'd18 -- gpt0_1_n sel 5'd19 -- sdio_d3 sel 5'd20 -- coex_priority sel 5'd21 -- gpt1_3_n sel 5'd22 -- gpt_infrared sel 5'd23 -- ant_sel_3 sel 5'd26 -- trdata_3 sel 5'd30 -- uart2_rx 0h = reserved 1h = reserved 2h = wifi_gpio_19 3h = sdio_mmc_data_4 4h = spi0_mosi 5h = uart0_cts 6h = i2c1_clk 7h = i2s_bclk 8h = pdm_data0 9h = gpt0_3 Ah = dcan_rx Bh = wake_observe_bus_11 Ch = debug_bus_4 Dh = reserved Eh = reserved Fh = reserved 10h = gpt0_pre_event 11h = sdio_oob_irq 12h = gpt0_1_n 13h = sdio_d3 14h = coex_priority 15h = gpt1_3_n 16h = gpt_infrared 17h = ant_sel_3 18h = reserved 19h = reserved 1Ah = trdata_3 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = uart2_rx 1Fh = reserved

16.8.201 GPIO20PCFG Register (Offset = 0002D054h) [Reset = 00000000h]

GPIO20PCFG is shown in Table 16-203.

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Port configuration register for IO GPIO20

Table 16-203. GPIO20PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd0 -- xspi_cs_flash sel 5'd2 -- wifi_gpio_20 0h = xspi_cs_flash 1h = reserved 2h = wifi_gpio_20 3h = reserved 4h = reserved 5h = reserved 6h = reserved 7h = reserved 8h = reserved 9h = reserved Ah = reserved Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = reserved 13h = reserved 14h = reserved 15h = reserved 16h = reserved 17h = reserved 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.202 GPIO21PCFG Register (Offset = 0002D058h) [Reset = 00000000h]

GPIO21PCFG is shown in Table 16-204.

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Port configuration register for IO GPIO21

Table 16-204. GPIO21PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd0 -- xspi_data_1 sel 5'd2 -- wifi_gpio_21 0h = xspi_data_1 1h = reserved 2h = wifi_gpio_21 3h = reserved 4h = reserved 5h = reserved 6h = reserved 7h = reserved 8h = reserved 9h = reserved Ah = reserved Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = reserved 13h = reserved 14h = reserved 15h = reserved 16h = reserved 17h = reserved 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.203 GPIO22PCFG Register (Offset = 0002D05Ch) [Reset = 00000000h]

GPIO22PCFG is shown in Table 16-205.

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Port configuration register for IO GPIO22

Table 16-205. GPIO22PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd0 -- xspi_data_2 sel 5'd2 -- wifi_gpio_22 0h = xspi_data_2 1h = reserved 2h = wifi_gpio_22 3h = reserved 4h = reserved 5h = reserved 6h = reserved 7h = reserved 8h = reserved 9h = reserved Ah = reserved Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = reserved 13h = reserved 14h = reserved 15h = reserved 16h = reserved 17h = reserved 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.204 GPIO23PCFG Register (Offset = 0002D060h) [Reset = 00000000h]

GPIO23PCFG is shown in Table 16-206.

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Port configuration register for IO GPIO23

Table 16-206. GPIO23PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd0 -- xspi_data_3 sel 5'd2 -- wifi_gpio_23 0h = xspi_data_3 1h = reserved 2h = wifi_gpio_23 3h = reserved 4h = reserved 5h = reserved 6h = reserved 7h = reserved 8h = reserved 9h = reserved Ah = reserved Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = reserved 13h = reserved 14h = reserved 15h = reserved 16h = reserved 17h = reserved 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.205 GPIO24PCFG Register (Offset = 0002D064h) [Reset = 00000000h]

GPIO24PCFG is shown in Table 16-207.

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Port configuration register for IO GPIO24

Table 16-207. GPIO24PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd0 -- xspi_clk sel 5'd2 -- wifi_gpio_24 0h = xspi_clk 1h = reserved 2h = wifi_gpio_24 3h = reserved 4h = reserved 5h = reserved 6h = reserved 7h = reserved 8h = reserved 9h = reserved Ah = reserved Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = reserved 13h = reserved 14h = reserved 15h = reserved 16h = reserved 17h = reserved 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.206 GPIO25PCFG Register (Offset = 0002D068h) [Reset = 00000000h]

GPIO25PCFG is shown in Table 16-208.

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Port configuration register for IO GPIO25

Table 16-208. GPIO25PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd0 -- xspi_data_0 sel 5'd2 -- wifi_gpio_25 0h = xspi_data_0 1h = reserved 2h = wifi_gpio_25 3h = reserved 4h = reserved 5h = reserved 6h = reserved 7h = reserved 8h = reserved 9h = reserved Ah = reserved Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = reserved 13h = reserved 14h = reserved 15h = reserved 16h = reserved 17h = reserved 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.207 GPIO26PCFG Register (Offset = 0002D06Ch) [Reset = 00000000h]

GPIO26PCFG is shown in Table 16-209.

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Port configuration register for IO GPIO26

Table 16-209. GPIO26PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- xspi_data_4 sel 5'd2 -- wifi_gpio_26 sel 5'd4 -- spi0_cs1 sel 5'd5 -- uart0_rts sel 5'd6 -- i2c1_clk sel 5'd7 -- i2s_wclk sel 5'd8 -- pdm_bclk sel 5'd9 -- gpt0_0 sel 5'd10 -- dcan_tx sel 5'd11 -- wake_observe_bus_0 sel 5'd12 -- debug_bus_13 sel 5'd16 -- spi1_cs2 sel 5'd17 -- ext_clk sel 5'd18 -- gpt0_1_n sel 5'd19 -- gpt1_0_n sel 5'd20 -- coex_grant sel 5'd21 -- coex_req sel 5'd22 -- ble_rfc_gpo_4 sel 5'd23 -- ant_sel_0 sel 5'd24 -- gpt_infrared sel 5'd25 -- ble_rfc_gpi_1 sel 5'd26 -- ble_rfc_gpi_3 sel 5'd30 -- sdio_oob_irq sel 5'd31 -- uart2_tx 0h = reserved 1h = xspi_data_4 2h = wifi_gpio_26 3h = reserved 4h = spi0_cs1 5h = uart0_rts 6h = i2c1_clk 7h = i2s_wclk 8h = pdm_bclk 9h = gpt0_0 Ah = dcan_tx Bh = wake_observe_bus_0 Ch = debug_bus_13 Dh = reserved Eh = reserved Fh = reserved 10h = spi1_cs2 11h = ext_clk 12h = gpt0_1_n 13h = gpt1_0_n 14h = coex_grant 15h = coex_req 16h = ble_rfc_gpo_4 17h = ant_sel_0 18h = gpt_infrared 19h = ble_rfc_gpi_1 1Ah = ble_rfc_gpi_3 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = sdio_oob_irq 1Fh = uart2_tx

16.8.208 GPIO27PCFG Register (Offset = 0002D070h) [Reset = 00000000h]

GPIO27PCFG is shown in Table 16-210.

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Port configuration register for IO GPIO27

Table 16-210. GPIO27PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- xspi_data_5 sel 5'd2 -- wifi_gpio_27 sel 5'd4 -- spi0_clk sel 5'd5 -- uart0_tx sel 5'd6 -- i2c0_data sel 5'd7 -- i2s_data0 sel 5'd8 -- pdm_data0 sel 5'd9 -- gpt0_1 sel 5'd11 -- wake_observe_bus_1 sel 5'd12 -- debug_bus_14 sel 5'd16 -- spi1_cs3 sel 5'd18 -- gpt0_0_n sel 5'd19 -- gpt1_1_n sel 5'd20 -- coex_req sel 5'd22 -- ble_rfc_gpo_5 sel 5'd23 -- ant_sel_1 sel 5'd25 -- ble_rfc_gpi_2 sel 5'd31 -- uart2_rts 0h = reserved 1h = xspi_data_5 2h = wifi_gpio_27 3h = reserved 4h = spi0_clk 5h = uart0_tx 6h = i2c0_data 7h = i2s_data0 8h = pdm_data0 9h = gpt0_1 Ah = reserved Bh = wake_observe_bus_1 Ch = debug_bus_14 Dh = reserved Eh = reserved Fh = reserved 10h = spi1_cs3 11h = reserved 12h = gpt0_0_n 13h = gpt1_1_n 14h = coex_req 15h = reserved 16h = ble_rfc_gpo_5 17h = ant_sel_1 18h = reserved 19h = ble_rfc_gpi_2 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = uart2_rts

16.8.209 GPIO28PCFG Register (Offset = 0002D074h) [Reset = 00000000h]

GPIO28PCFG is shown in Table 16-211.

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Port configuration register for IO GPIO28

Table 16-211. GPIO28PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- xspi_data_6 sel 5'd2 -- wifi_gpio_28 sel 5'd4 -- spi0_miso sel 5'd5 -- uart0_rx sel 5'd6 -- i2c0_clk sel 5'd7 -- i2s_data1 sel 5'd8 -- pdm_bclk sel 5'd9 -- gpt0_2 sel 5'd11 -- wake_observe_bus_2 sel 5'd12 -- debug_bus_15 sel 5'd16 -- spi1_cs4 sel 5'd18 -- gpt0_0_n sel 5'd19 -- gpt1_2_n sel 5'd20 -- coex_priority sel 5'd22 -- ble_rfc_gpo_6 sel 5'd23 -- ant_sel_2 sel 5'd24 -- gpt0_pre_event sel 5'd25 -- ble_rfc_gpi_3 sel 5'd31 -- uart2_cts 0h = reserved 1h = xspi_data_6 2h = wifi_gpio_28 3h = reserved 4h = spi0_miso 5h = uart0_rx 6h = i2c0_clk 7h = i2s_data1 8h = pdm_bclk 9h = gpt0_2 Ah = reserved Bh = wake_observe_bus_2 Ch = debug_bus_15 Dh = reserved Eh = reserved Fh = reserved 10h = spi1_cs4 11h = reserved 12h = gpt0_0_n 13h = gpt1_2_n 14h = coex_priority 15h = reserved 16h = ble_rfc_gpo_6 17h = ant_sel_2 18h = gpt0_pre_event 19h = ble_rfc_gpi_3 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = uart2_cts

16.8.210 GPIO29PCFG Register (Offset = 0002D078h) [Reset = 00000000h]

GPIO29PCFG is shown in Table 16-212.

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Port configuration register for IO GPIO29

Table 16-212. GPIO29PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- xspi_data_7 sel 5'd2 -- wifi_gpio_29 sel 5'd4 -- spi0_mosi sel 5'd5 -- uart0_cts sel 5'd6 -- i2c1_data sel 5'd7 -- i2s_bclk sel 5'd8 -- pdm_data1 sel 5'd9 -- gpt0_3 sel 5'd10 -- dcan_rx sel 5'd11 -- wake_observe_bus_3 sel 5'd12 -- i2s_mclk sel 5'd16 -- spi1_cs4 sel 5'd17 -- ext_clk sel 5'd18 -- gpt0_1_n sel 5'd19 -- gpt1_3_n sel 5'd20 -- coex_grant sel 5'd22 -- ble_rfc_gpo_7 sel 5'd23 -- ant_sel_3 sel 5'd30 -- sdio_oob_irq sel 5'd31 -- uart2_rx 0h = reserved 1h = xspi_data_7 2h = wifi_gpio_29 3h = reserved 4h = spi0_mosi 5h = uart0_cts 6h = i2c1_data 7h = i2s_bclk 8h = pdm_data1 9h = gpt0_3 Ah = dcan_rx Bh = wake_observe_bus_3 Ch = i2s_mclk Dh = reserved Eh = reserved Fh = reserved 10h = spi1_cs4 11h = ext_clk 12h = gpt0_1_n 13h = gpt1_3_n 14h = coex_grant 15h = reserved 16h = ble_rfc_gpo_7 17h = ant_sel_3 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = sdio_oob_irq 1Fh = uart2_rx

16.8.211 GPIO30PCFG Register (Offset = 0002D07Ch) [Reset = 00000000h]

GPIO30PCFG is shown in Table 16-213.

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Port configuration register for IO GPIO30

Table 16-213. GPIO30PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- xspi_dqs sel 5'd2 -- wifi_gpio_30 sel 5'd3 -- xspi_reset_flash sel 5'd4 -- xspi_reset_ram sel 5'd5 -- i2c1_clk sel 5'd6 -- i2c0_clk sel 5'd7 -- i2s_data0 sel 5'd8 -- pdm_data0 sel 5'd9 -- gpt1_1 sel 5'd10 -- dcan_tx sel 5'd11 -- wake_observe_bus_4 sel 5'd12 -- xspi_cs_ram sel 5'd16 -- spi0_cs2 sel 5'd17 -- spi0_cs2 sel 5'd18 -- gpt0_2_n sel 5'd19 -- coex_grant sel 5'd20 -- coex_req sel 5'd21 -- ble_rftrc sel 5'd22 -- ble_rfc_gpo_4 sel 5'd23 -- ant_sel_0 sel 5'd24 -- cca sel 5'd25 -- ble_rfc_gpi_1 sel 5'd26 -- swo_m3 sel 5'd27 -- swo_m33 sel 5'd28 -- gpt1_pre_event sel 5'd29 -- gpt0_pre_event sel 5'd30 -- sdio_d3 sel 5'd31 -- uart2_tx 0h = reserved 1h = xspi_dqs 2h = wifi_gpio_30 3h = xspi_reset_flash 4h = xspi_reset_ram 5h = i2c1_clk 6h = i2c0_clk 7h = i2s_data0 8h = pdm_data0 9h = gpt1_1 Ah = dcan_tx Bh = wake_observe_bus_4 Ch = xspi_cs_ram Dh = reserved Eh = reserved Fh = reserved 10h = spi0_cs2 11h = spi0_cs2 12h = gpt0_2_n 13h = coex_grant 14h = coex_req 15h = ble_rftrc 16h = ble_rfc_gpo_4 17h = ant_sel_0 18h = cca 19h = ble_rfc_gpi_1 1Ah = swo_m3 1Bh = swo_m33 1Ch = gpt1_pre_event 1Dh = gpt0_pre_event 1Eh = sdio_d3 1Fh = uart2_tx

16.8.212 GPIO31PCFG Register (Offset = 0002D080h) [Reset = 00000000h]

GPIO31PCFG is shown in Table 16-214.

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Port configuration register for IO GPIO31

Table 16-214. GPIO31PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- xspi_cs_ram sel 5'd2 -- wifi_gpio_31 sel 5'd3 -- xspi_reset_flash sel 5'd4 -- spi1_cs1 sel 5'd5 -- uart1_rts sel 5'd6 -- i2c1_clk sel 5'd7 -- i2s_wclk sel 5'd8 -- pdm_bclk sel 5'd9 -- gpt1_0 sel 5'd10 -- dcan_tx sel 5'd16 -- spi0_cs3 sel 5'd17 -- ext_clk sel 5'd18 -- gpt1_1_n sel 5'd19 -- gpt0_0_n sel 5'd20 -- coex_grant sel 5'd22 -- ble_rfc_gpo_6 sel 5'd23 -- ant_sel_0 sel 5'd24 -- gpt_infrared sel 5'd25 -- ble_rfc_gpi_3 sel 5'd30 -- sdio_d2 sel 5'd31 -- uart2_tx 0h = reserved 1h = xspi_cs_ram 2h = wifi_gpio_31 3h = xspi_reset_flash 4h = spi1_cs1 5h = uart1_rts 6h = i2c1_clk 7h = i2s_wclk 8h = pdm_bclk 9h = gpt1_0 Ah = dcan_tx Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = spi0_cs3 11h = ext_clk 12h = gpt1_1_n 13h = gpt0_0_n 14h = coex_grant 15h = reserved 16h = ble_rfc_gpo_6 17h = ant_sel_0 18h = gpt_infrared 19h = ble_rfc_gpi_3 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = sdio_d2 1Fh = uart2_tx

16.8.213 GPIO32PCFG Register (Offset = 0002D084h) [Reset = 00000000h]

GPIO32PCFG is shown in Table 16-215.

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Port configuration register for IO GPIO32

Table 16-215. GPIO32PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- xspi_cs_ram sel 5'd2 -- wifi_gpio_32 sel 5'd3 -- spi1_cs1 sel 5'd4 -- spi1_clk sel 5'd5 -- uart1_tx sel 5'd6 -- i2c0_data sel 5'd7 -- i2s_data1 sel 5'd8 -- pdm_bclk sel 5'd9 -- gpt1_1 sel 5'd10 -- dcan_rx sel 5'd11 -- wake_observe_bus_5 sel 5'd16 -- spi0_cs3 sel 5'd18 -- gpt1_0_n sel 5'd19 -- gpt0_1_n sel 5'd20 -- coex_req sel 5'd23 -- ant_sel_1 sel 5'd30 -- sdio_d1 sel 5'd31 -- uart2_rts 0h = reserved 1h = xspi_cs_ram 2h = wifi_gpio_32 3h = spi1_cs1 4h = spi1_clk 5h = uart1_tx 6h = i2c0_data 7h = i2s_data1 8h = pdm_bclk 9h = gpt1_1 Ah = dcan_rx Bh = wake_observe_bus_5 Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = spi0_cs3 11h = reserved 12h = gpt1_0_n 13h = gpt0_1_n 14h = coex_req 15h = reserved 16h = reserved 17h = ant_sel_1 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = sdio_d1 1Fh = uart2_rts

16.8.214 GPIO33PCFG Register (Offset = 0002D088h) [Reset = 00000000h]

GPIO33PCFG is shown in Table 16-216.

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Port configuration register for IO GPIO33

Table 16-216. GPIO33PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd2 -- wifi_gpio_33 sel 5'd4 -- spi1_miso sel 5'd5 -- uart1_rx sel 5'd6 -- i2c0_clk sel 5'd7 -- i2s_data0 sel 5'd8 -- pdm_data0 sel 5'd9 -- gpt1_2 sel 5'd10 -- dcan_tx sel 5'd16 -- spi0_cs4 sel 5'd18 -- gpt1_0_n sel 5'd19 -- gpt0_2_n sel 5'd20 -- coex_grant sel 5'd23 -- ant_sel_2 sel 5'd24 -- gpt1_pre_event sel 5'd25 -- ble_rfc_gpi_2 sel 5'd30 -- sdio_d0 sel 5'd31 -- uart2_cts 0h = reserved 1h = reserved 2h = wifi_gpio_33 3h = reserved 4h = spi1_miso 5h = uart1_rx 6h = i2c0_clk 7h = i2s_data0 8h = pdm_data0 9h = gpt1_2 Ah = dcan_tx Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = spi0_cs4 11h = reserved 12h = gpt1_0_n 13h = gpt0_2_n 14h = coex_grant 15h = reserved 16h = reserved 17h = ant_sel_2 18h = gpt1_pre_event 19h = ble_rfc_gpi_2 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = sdio_d0 1Fh = uart2_cts

16.8.215 GPIO34PCFG Register (Offset = 0002D08Ch) [Reset = 00000000h]

GPIO34PCFG is shown in Table 16-217.

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Port configuration register for IO GPIO34

Table 16-217. GPIO34PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- xspi_reset_ram sel 5'd2 -- wifi_gpio_34 sel 5'd4 -- spi1_mosi sel 5'd5 -- uart1_cts sel 5'd6 -- i2c1_data sel 5'd7 -- i2s_bclk sel 5'd8 -- pdm_data1 sel 5'd9 -- gpt1_3 sel 5'd10 -- dcan_rx sel 5'd16 -- spi0_cs2 sel 5'd18 -- gpt1_1_n sel 5'd19 -- gpt0_3_n sel 5'd20 -- coex_req sel 5'd22 -- ble_rfc_gpo_7 sel 5'd23 -- ant_sel_3 sel 5'd25 -- ble_rfc_gpi_1 sel 5'd30 -- sdio_clk sel 5'd31 -- uart2_rx 0h = reserved 1h = xspi_reset_ram 2h = wifi_gpio_34 3h = reserved 4h = spi1_mosi 5h = uart1_cts 6h = i2c1_data 7h = i2s_bclk 8h = pdm_data1 9h = gpt1_3 Ah = dcan_rx Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = spi0_cs2 11h = reserved 12h = gpt1_1_n 13h = gpt0_3_n 14h = coex_req 15h = reserved 16h = ble_rfc_gpo_7 17h = ant_sel_3 18h = reserved 19h = ble_rfc_gpi_1 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = sdio_clk 1Fh = uart2_rx

16.8.216 GPIO35PCFG Register (Offset = 0002D090h) [Reset = 00000000h]

GPIO35PCFG is shown in Table 16-218.

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Port configuration register for IO GPIO35

Table 16-218. GPIO35PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- xspi_reset_flash sel 5'd2 -- wifi_gpio_35 sel 5'd3 -- spi1_clk sel 5'd4 -- xspi_reset_ram sel 5'd5 -- uart1_rx sel 5'd6 -- i2c0_data sel 5'd7 -- i2s_data1 sel 5'd8 -- pdm_bclk sel 5'd9 -- gpt0_1 sel 5'd10 -- dcan_rx sel 5'd11 -- i2c1_data sel 5'd12 -- xspi_cs_ram sel 5'd16 -- spi0_cs4 sel 5'd17 -- spi0_cs3 sel 5'd18 -- gpt0_2_n sel 5'd19 -- gpt1_2_n sel 5'd20 -- coex_priority sel 5'd21 -- ble_rftrc sel 5'd22 -- ble_rfc_gpo_5 sel 5'd23 -- ant_sel_0 sel 5'd24 -- gpt1_pre_event sel 5'd25 -- ble_rfc_gpi_2 sel 5'd26 -- swo_m3 sel 5'd27 -- swo_m33 sel 5'd28 -- xspi_dqs sel 5'd29 -- coex_req sel 5'd30 -- sdio_cmd sel 5'd31 -- uart2_rx 0h = reserved 1h = xspi_reset_flash 2h = wifi_gpio_35 3h = spi1_clk 4h = xspi_reset_ram 5h = uart1_rx 6h = i2c0_data 7h = i2s_data1 8h = pdm_bclk 9h = gpt0_1 Ah = dcan_rx Bh = i2c1_data Ch = xspi_cs_ram Dh = reserved Eh = reserved Fh = reserved 10h = spi0_cs4 11h = spi0_cs3 12h = gpt0_2_n 13h = gpt1_2_n 14h = coex_priority 15h = ble_rftrc 16h = ble_rfc_gpo_5 17h = ant_sel_0 18h = gpt1_pre_event 19h = ble_rfc_gpi_2 1Ah = swo_m3 1Bh = swo_m33 1Ch = xspi_dqs 1Dh = coex_req 1Eh = sdio_cmd 1Fh = uart2_rx

16.8.217 GPIO36PCFG Register (Offset = 0002D094h) [Reset = 00000000h]

GPIO36PCFG is shown in Table 16-219.

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Port configuration register for IO GPIO36

Table 16-219. GPIO36PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd0 -- fast_clk_req sel 5'd1 -- xspi_cs_ram sel 5'd2 -- wifi_gpio_36 sel 5'd3 -- sdio_mmc_pow2 sel 5'd4 -- sdio_mmc_wp sel 5'd11 -- wake_observe_bus_13 sel 5'd12 -- debug_bus_1 sel 5'd19 -- coex_req sel 5'd20 -- coex_grant sel 5'd21 -- fast_clk_req sel 5'd22 -- ble_rfc_gpo_5 sel 5'd23 -- ant_sel_1 sel 5'd24 -- cca sel 5'd25 -- ble_rfc_gpi_2 0h = fast_clk_req 1h = xspi_cs_ram 2h = wifi_gpio_36 3h = sdio_mmc_pow2 4h = sdio_mmc_wp 5h = reserved 6h = reserved 7h = reserved 8h = reserved 9h = reserved Ah = reserved Bh = wake_observe_bus_13 Ch = debug_bus_1 Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = reserved 13h = coex_req 14h = coex_grant 15h = fast_clk_req 16h = ble_rfc_gpo_5 17h = ant_sel_1 18h = cca 19h = ble_rfc_gpi_2 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.218 GPIO37PCFG Register (Offset = 0002D098h) [Reset = 00000000h]

GPIO37PCFG is shown in Table 16-220.

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Port configuration register for IO GPIO37

Table 16-220. GPIO37PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- xspi_cs_ram sel 5'd2 -- wifi_gpio_37 sel 5'd3 -- sdio_mmc_pow1 sel 5'd4 -- sdio_mmc_wp sel 5'd11 -- wake_observe_bus_12 sel 5'd12 -- debug_bus_0 sel 5'd18 -- coex_req sel 5'd19 -- sdio_oob_irq sel 5'd20 -- coex_grant sel 5'd21 -- fast_clk_req sel 5'd22 -- ble_rfc_gpo_4 sel 5'd23 -- ant_sel_0 sel 5'd24 -- cca sel 5'd25 -- ble_rfc_gpi_1 0h = reserved 1h = xspi_cs_ram 2h = wifi_gpio_37 3h = sdio_mmc_pow1 4h = sdio_mmc_wp 5h = reserved 6h = reserved 7h = reserved 8h = reserved 9h = reserved Ah = reserved Bh = wake_observe_bus_12 Ch = debug_bus_0 Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = coex_req 13h = sdio_oob_irq 14h = coex_grant 15h = fast_clk_req 16h = ble_rfc_gpo_4 17h = ant_sel_0 18h = cca 19h = ble_rfc_gpi_1 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.219 GPIO38PCFG Register (Offset = 0002D09Ch) [Reset = 00000000h]

GPIO38PCFG is shown in Table 16-221.

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Port configuration register for IO GPIO38

Table 16-221. GPIO38PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- xspi_cs_ram sel 5'd2 -- wifi_gpio_38 sel 5'd3 -- ext_clk sel 5'd4 -- spi1_clk sel 5'd5 -- uart0_cts sel 5'd6 -- i2c1_clk sel 5'd7 -- i2s_bclk sel 5'd8 -- pdm_bclk sel 5'd9 -- gpt1_0 sel 5'd10 -- dcan_tx sel 5'd18 -- gpt1_1_n sel 5'd20 -- coex_grant sel 5'd23 -- ant_sel_0 sel 5'd29 -- coex_req sel 5'd30 -- uart2_rx 0h = reserved 1h = xspi_cs_ram 2h = wifi_gpio_38 3h = ext_clk 4h = spi1_clk 5h = uart0_cts 6h = i2c1_clk 7h = i2s_bclk 8h = pdm_bclk 9h = gpt1_0 Ah = dcan_tx Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = gpt1_1_n 13h = reserved 14h = coex_grant 15h = reserved 16h = reserved 17h = ant_sel_0 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = coex_req 1Eh = uart2_rx 1Fh = reserved

16.8.220 GPIO39PCFG Register (Offset = 0002D0A0h) [Reset = 00000000h]

GPIO39PCFG is shown in Table 16-222.

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Port configuration register for IO GPIO39

Table 16-222. GPIO39PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- xspi_reset_ram sel 5'd2 -- wifi_gpio_39 sel 5'd3 -- uart0_rx sel 5'd4 -- spi1_miso sel 5'd5 -- uart0_rts sel 5'd6 -- i2c1_data sel 5'd7 -- i2s_wclk sel 5'd8 -- pdm_data0 sel 5'd9 -- gpt1_1 sel 5'd10 -- dcan_rx sel 5'd11 -- xspi_dqs sel 5'd18 -- gpt1_0_n sel 5'd20 -- coex_req sel 5'd21 -- coex_grant sel 5'd23 -- ant_sel_1 sel 5'd29 -- coex_priority sel 5'd30 -- uart2_tx 0h = reserved 1h = xspi_reset_ram 2h = wifi_gpio_39 3h = uart0_rx 4h = spi1_miso 5h = uart0_rts 6h = i2c1_data 7h = i2s_wclk 8h = pdm_data0 9h = gpt1_1 Ah = dcan_rx Bh = xspi_dqs Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = gpt1_0_n 13h = reserved 14h = coex_req 15h = coex_grant 16h = reserved 17h = ant_sel_1 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = coex_priority 1Eh = uart2_tx 1Fh = reserved

16.8.221 GPIO40PCFG Register (Offset = 0002D0A4h) [Reset = 00000000h]

GPIO40PCFG is shown in Table 16-223.

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Port configuration register for IO GPIO40

Table 16-223. GPIO40PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- xspi_cs_ram sel 5'd2 -- wifi_gpio_40 sel 5'd4 -- spi1_mosi sel 5'd5 -- uart0_tx sel 5'd7 -- i2s_data0 sel 5'd8 -- pdm_data1 sel 5'd9 -- gpt1_2 sel 5'd16 -- gpt1_pre_event sel 5'd17 -- gpt0_pre_event sel 5'd18 -- gpt1_2_n sel 5'd20 -- coex_priority sel 5'd22 -- gpt_infrared sel 5'd23 -- ant_sel_2 sel 5'd29 -- coex_grant sel 5'd30 -- uart2_rts 0h = reserved 1h = xspi_cs_ram 2h = wifi_gpio_40 3h = reserved 4h = spi1_mosi 5h = uart0_tx 6h = reserved 7h = i2s_data0 8h = pdm_data1 9h = gpt1_2 Ah = reserved Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = gpt1_pre_event 11h = gpt0_pre_event 12h = gpt1_2_n 13h = reserved 14h = coex_priority 15h = reserved 16h = gpt_infrared 17h = ant_sel_2 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = coex_grant 1Eh = uart2_rts 1Fh = reserved

16.8.222 GPIO41PCFG Register (Offset = 0002D0A8h) [Reset = 00000000h]

GPIO41PCFG is shown in Table 16-224.

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Port configuration register for IO GPIO41

Table 16-224. GPIO41PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- xspi_cs_ram sel 5'd2 -- wifi_gpio_41 sel 5'd4 -- spi1_miso sel 5'd5 -- uart1_cts sel 5'd7 -- i2s_data0 sel 5'd9 -- gpt0_0 sel 5'd16 -- gpt1_pre_event sel 5'd17 -- gpt0_pre_event sel 5'd18 -- gpt0_1_n sel 5'd20 -- coex_grant sel 5'd22 -- gpt_infrared sel 5'd23 -- ant_sel_0 sel 5'd29 -- coex_grant sel 5'd30 -- uart2_rx 0h = reserved 1h = xspi_cs_ram 2h = wifi_gpio_41 3h = reserved 4h = spi1_miso 5h = uart1_cts 6h = reserved 7h = i2s_data0 8h = reserved 9h = gpt0_0 Ah = reserved Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = gpt1_pre_event 11h = gpt0_pre_event 12h = gpt0_1_n 13h = reserved 14h = coex_grant 15h = reserved 16h = gpt_infrared 17h = ant_sel_0 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = coex_grant 1Eh = uart2_rx 1Fh = reserved

16.8.223 GPIO42PCFG Register (Offset = 0002D0ACh) [Reset = 00000000h]

GPIO42PCFG is shown in Table 16-225.

Return to the Summary Table.

Port configuration register for IO GPIO42

Table 16-225. GPIO42PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- xspi_reset_ram sel 5'd2 -- wifi_gpio_42 sel 5'd3 -- uart1_rx sel 5'd4 -- spi1_mosi sel 5'd5 -- uart1_rts sel 5'd6 -- i2c0_data sel 5'd7 -- i2s_wclk sel 5'd8 -- pdm_data0 sel 5'd9 -- gpt0_1 sel 5'd10 -- dcan_rx sel 5'd11 -- xspi_dqs sel 5'd18 -- gpt0_0_n sel 5'd20 -- coex_req sel 5'd21 -- coex_grant sel 5'd23 -- ant_sel_1 sel 5'd29 -- coex_req sel 5'd30 -- uart2_tx 0h = reserved 1h = xspi_reset_ram 2h = wifi_gpio_42 3h = uart1_rx 4h = spi1_mosi 5h = uart1_rts 6h = i2c0_data 7h = i2s_wclk 8h = pdm_data0 9h = gpt0_1 Ah = dcan_rx Bh = xspi_dqs Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = gpt0_0_n 13h = reserved 14h = coex_req 15h = coex_grant 16h = reserved 17h = ant_sel_1 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = coex_req 1Eh = uart2_tx 1Fh = reserved

16.8.224 GPIO43PCFG Register (Offset = 0002D0B0h) [Reset = 00000000h]

GPIO43PCFG is shown in Table 16-226.

Return to the Summary Table.

Port configuration register for IO GPIO43

Table 16-226. GPIO43PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd1 -- xspi_cs_ram sel 5'd2 -- wifi_gpio_43 sel 5'd4 -- spi1_clk sel 5'd5 -- uart1_tx sel 5'd6 -- i2c0_clk sel 5'd7 -- i2s_bclk sel 5'd8 -- pdm_bclk sel 5'd9 -- gpt0_2 sel 5'd10 -- dcan_tx sel 5'd18 -- gpt0_2_n sel 5'd20 -- coex_priority sel 5'd23 -- ant_sel_2 sel 5'd29 -- coex_priority sel 5'd30 -- uart2_rts 0h = reserved 1h = xspi_cs_ram 2h = wifi_gpio_43 3h = reserved 4h = spi1_clk 5h = uart1_tx 6h = i2c0_clk 7h = i2s_bclk 8h = pdm_bclk 9h = gpt0_2 Ah = dcan_tx Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = gpt0_2_n 13h = reserved 14h = coex_priority 15h = reserved 16h = reserved 17h = ant_sel_2 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = coex_priority 1Eh = uart2_rts 1Fh = reserved

16.8.225 GPIO44PCFG Register (Offset = 0002D0B4h) [Reset = 00000000h]

GPIO44PCFG is shown in Table 16-227.

Return to the Summary Table.

Port configuration register for IO GPIO44

Table 16-227. GPIO44PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd0 -- xspi_clk_input sel 5'd2 -- wifi_gpio_44 0h = xspi_clk_input 1h = reserved 2h = wifi_gpio_44 3h = reserved 4h = reserved 5h = reserved 6h = reserved 7h = reserved 8h = reserved 9h = reserved Ah = reserved Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = reserved 13h = reserved 14h = reserved 15h = reserved 16h = reserved 17h = reserved 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.226 GPIO45PCFG Register (Offset = 0002D0C0h) [Reset = 00000000h]

GPIO45PCFG is shown in Table 16-228.

Return to the Summary Table.

Port configuration register for IO GPIO45

Table 16-228. GPIO45PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd0 -- xspi_data_0_ram 0h = xspi_data_0_ram 1h = reserved 2h = reserved 3h = reserved 4h = reserved 5h = reserved 6h = reserved 7h = reserved 8h = reserved 9h = reserved Ah = reserved Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = reserved 13h = reserved 14h = reserved 15h = reserved 16h = reserved 17h = reserved 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.227 GPIO46PCFG Register (Offset = 0002D0C4h) [Reset = 00000000h]

GPIO46PCFG is shown in Table 16-229.

Return to the Summary Table.

Port configuration register for IO GPIO46

Table 16-229. GPIO46PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd0 -- xspi_data_1_ram 0h = xspi_data_1_ram 1h = reserved 2h = reserved 3h = reserved 4h = reserved 5h = reserved 6h = reserved 7h = reserved 8h = reserved 9h = reserved Ah = reserved Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = reserved 13h = reserved 14h = reserved 15h = reserved 16h = reserved 17h = reserved 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.228 GPIO47PCFG Register (Offset = 0002D0C8h) [Reset = 00000000h]

GPIO47PCFG is shown in Table 16-230.

Return to the Summary Table.

Port configuration register for IO GPIO47

Table 16-230. GPIO47PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd0 -- xspi_data_2_ram 0h = xspi_data_2_ram 1h = reserved 2h = reserved 3h = reserved 4h = reserved 5h = reserved 6h = reserved 7h = reserved 8h = reserved 9h = reserved Ah = reserved Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = reserved 13h = reserved 14h = reserved 15h = reserved 16h = reserved 17h = reserved 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.229 GPIO48PCFG Register (Offset = 0002D0CCh) [Reset = 00000000h]

GPIO48PCFG is shown in Table 16-231.

Return to the Summary Table.

Port configuration register for IO GPIO48

Table 16-231. GPIO48PCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	IOSEL	R/W	0h	Pinmux selection Control Mode can be used to select the IO functionality or drive 0/1/Hi-Z sel 5'd0 -- xspi_data_3_ram 0h = xspi_data_3_ram 1h = reserved 2h = reserved 3h = reserved 4h = reserved 5h = reserved 6h = reserved 7h = reserved 8h = reserved 9h = reserved Ah = reserved Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved 10h = reserved 11h = reserved 12h = reserved 13h = reserved 14h = reserved 15h = reserved 16h = reserved 17h = reserved 18h = reserved 19h = reserved 1Ah = reserved 1Bh = reserved 1Ch = reserved 1Dh = reserved 1Eh = reserved 1Fh = reserved

16.8.230 GPIO45CFG Register (Offset = 0002E000h) [Reset = 00000000h]

GPIO45CFG is shown in Table 16-232.

Return to the Summary Table.

CFG register for IO GPIO45. This register configures the corresponding pad

Table 16-232. GPIO45CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.231 GPIO45PCTL Register (Offset = 0002E004h) [Reset = 00000000h]

GPIO45PCTL is shown in Table 16-233.

Return to the Summary Table.

Pull control register of IO GPIO45 This register configures the pull control

Table 16-233. GPIO45PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.232 GPIO45CTL Register (Offset = 0002E008h) [Reset = 00000000h]

GPIO45CTL is shown in Table 16-234.

Return to the Summary Table.

Control register of IO GPIO45 This register controls the IO state

Table 16-234. GPIO45CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.233 GPIO45ECTL Register (Offset = 0002E00Ch) [Reset = 00000000h]

GPIO45ECTL is shown in Table 16-235.

Return to the Summary Table.

Event control register for IO GPIO45 This register controls the Event configuration and behaviour

Table 16-235. GPIO45ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.234 GPIO46CFG Register (Offset = 0002F000h) [Reset = 00000000h]

GPIO46CFG is shown in Table 16-236.

Return to the Summary Table.

CFG register for IO GPIO46. This register configures the corresponding pad

Table 16-236. GPIO46CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.235 GPIO46PCTL Register (Offset = 0002F004h) [Reset = 00000000h]

GPIO46PCTL is shown in Table 16-237.

Return to the Summary Table.

Pull control register of IO GPIO46 This register configures the pull control

Table 16-237. GPIO46PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.236 GPIO46CTL Register (Offset = 0002F008h) [Reset = 00000000h]

GPIO46CTL is shown in Table 16-238.

Return to the Summary Table.

Control register of IO GPIO46 This register controls the IO state

Table 16-238. GPIO46CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.237 GPIO46ECTL Register (Offset = 0002F00Ch) [Reset = 00000000h]

GPIO46ECTL is shown in Table 16-239.

Return to the Summary Table.

Event control register for IO GPIO46 This register controls the Event configuration and behaviour

Table 16-239. GPIO46ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.238 GPIO47CFG Register (Offset = 00030000h) [Reset = 00000000h]

GPIO47CFG is shown in Table 16-240.

Return to the Summary Table.

CFG register for IO GPIO47. This register configures the corresponding pad

Table 16-240. GPIO47CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.239 GPIO47PCTL Register (Offset = 00030004h) [Reset = 00000000h]

GPIO47PCTL is shown in Table 16-241.

Return to the Summary Table.

Pull control register of IO GPIO47 This register configures the pull control

Table 16-241. GPIO47PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.240 GPIO47CTL Register (Offset = 00030008h) [Reset = 00000000h]

GPIO47CTL is shown in Table 16-242.

Return to the Summary Table.

Control register of IO GPIO47 This register controls the IO state

Table 16-242. GPIO47CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.241 GPIO47ECTL Register (Offset = 0003000Ch) [Reset = 00000000h]

GPIO47ECTL is shown in Table 16-243.

Return to the Summary Table.

Event control register for IO GPIO47 This register controls the Event configuration and behaviour

Table 16-243. GPIO47ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

16.8.242 GPIO48CFG Register (Offset = 00031000h) [Reset = 00000000h]

GPIO48CFG is shown in Table 16-244.

Return to the Summary Table.

CFG register for IO GPIO48. This register configures the corresponding pad

Table 16-244. GPIO48CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
14	IOSTR	R/W	0h	This field controls the IO drive strength 0h = IO drives low power 1h = IO drives high power
13	OUTDISOVREN	R/W	0h	This field controls the [OUTDIS] override 0h = Disable the override 1h = Enable the override
12	OUTDIS	R/W	1h	This field configures the output from the pad Note:This field is applicable only if [OUTDISOVREN] is enabled 0h = Output from the pad is enabled 1h = Output from the pad is disabled
11	IE	R/W	1h	This field enables the receiver operation from the pad 0h = Disable the receiver operation 1h = Enable the receiver operation
10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
9-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	OUTDISVAL	R	0h	The field gives the status of [OUTDIS] 0h = Output is enabled 1h = Output is disabled
5-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

16.8.243 GPIO48PCTL Register (Offset = 00031004h) [Reset = 00000000h]

GPIO48PCTL is shown in Table 16-245.

Return to the Summary Table.

Pull control register of IO GPIO48 This register configures the pull control

Table 16-245. GPIO48PCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	PULLDWNSTA	R	0h	This field gives the IO pull down level status 0h = Pull disabled 1h = Pull down
8	PULLUPSTA	R	0h	This field gives the IO pull up level status 0h = Pull disabled 1h = Pull up
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	CTL	R/W	1h	The fields defines the pull control 0h = IP Pull Control 1h = Pull up 2h = Pull down 3h = Pull disable

16.8.244 GPIO48CTL Register (Offset = 00031008h) [Reset = 00000000h]

GPIO48CTL is shown in Table 16-246.

Return to the Summary Table.

Control register of IO GPIO48 This register controls the IO state

Table 16-246. GPIO48CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	OUTOVREN	R/W	0h	This field contols the override on output 0h = Output controlled by IP 1h = Enable override on output
8	OUT	R/W	0h	This field configures the IO drive out value. This field is valid only when [OUTOVREN] is configured ENABLE 0h = IO drives 0 1h = IO drives 1
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	PADVALSYNC	R	0h	This field captures the sychronized(to SOC clock) received value
0	PADVAL	R	0h	This field captures the received value from pad

16.8.245 GPIO48ECTL Register (Offset = 0003100Ch) [Reset = 00000000h]

GPIO48ECTL is shown in Table 16-247.

Return to the Summary Table.

Event control register for IO GPIO48 This register controls the Event configuration and behaviour

Table 16-247. GPIO48ECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	CLR	W	0h	This bit is to be used to generate CLR pulse for the event 0h = No effect 1h = Clear the event
2	TRGLVL	R/W	0h	This field configures the io event polarity. This field is applicable only when [EVTDETCFG] is configured LEVEL 0h = Non Inverted polarity 1h = Inverted polarity
1-0	EVTDETCFG	R/W	0h	This field is to be configured to define the IO detection method 0h = Masking the event 1h = Rising edge/Positive edge detection 2h = Falling edge/Negative edge detection 3h = Level detection

Chapter 17

Universal Asynchronous Receivers/Transmitters (UART)

This chapter describes the features and functions of the Universal Asynchronous Receiver/Transmitter (UART-LIN).

17.1 Introduction

The UART-LIN supports the following features:

- Programmable baud rate generator allowing speeds up to 4Mbps
- Separate 8 × 8 transmit (TX) and 8 × 8 receive (RX) first-in first-out (FIFO) buffers to reduce CPU interrupt service loading
- Programmable FIFO length, including 1-byte deep operation providing conventional double-buffered interface
- FIFO trigger levels of ¼, ½, ¾.
- Standard asynchronous communication bits for start, stop, and parity
- Line-break generation and detection
- Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8 data bits
  - Even, odd, stick, or no parity bit generation and detection
  - 1 or 2 stop-bit generation
- FIFO, RX FIFO RX time-out, modem status, and error conditions
- Standard FIFO-level and end-of-transmission interrupts
- Efficient transfers using direct memory access controller (Host DMA):
  - Separate channels for transmit and receive.
  - Receive single request asserted when data is in the FIFO; burst request asserted at programmed FIFO level.
  - Transmit single request is asserted when there is space in the FIFO; burst request is asserted at programmed FIFO level.
- Programmable hardware flow control
- Support for standard IrDA and low power IrDA modes.
- Provision to combine both TX and RX FIFOs in transmit mode.
- LIN protocol and features for data transmission and reception.
- In case of transmit operation, support generation of break or break and synch fields.
- Generation of break field with 13 bits (zeros) followed by delimiter and sync field.
- In case of receive operation, detection of break field and is able to automatically update baud rate based on sync field (only LIN mode).
- TXBRK control bit is used for generation of wake up signal on LIN bus.
- The control bits for break (TXBRK) and break/synch transmission (TXBRKSYNC) in LIN mode are automatically reset after transmission of break and break/synch fields respectively.
- Configuration bits to generate delimiter bit times of 1, 2, 3 and 4 (DELIMx).
- Configuration bit to enable automatic baud rate detection (ABDEN).
- Detect break field when 11 or more zeros are received.
- Generate break flag (LINBRK) when break field is successfully received.
- The break flag will be cleared by hardware when the data register is read.
- Generate break time out error flag (LINBTOE) when break field length exceeds 22 bit times.
- Generate synch time out error flag (LINSTOE) when length of synch field exceeds measurable time.
- When dormant mode is disabled, break and synch data are loaded to RX FIFO and associated interrupt flags shall be set as in normal UART operation.
- When dormant mode is enabled, break and synch data are not be loaded to RX FIFO and RX FIFO shall be updated with actual data (PID) only after successful reception of break/synch fields.
- When automatic baud rate detection is enabled, the minimum baud rate to be supported is 50 baud and maximum baud rate to be supported is 3M baud. LIN communication speed: 1kbps to 20kbps.
- Support proper reception of data while break or break/synch fields are transmitted (master role).
- Support transmission of data while receiving break/synch fields but transmission baud rate can change potentially due to automatic baud rate adjustment (slave role).
- UART is configured by software with 8 bit data, LSB first, no parity and 1 stop bit for operation in LIN mode.

17.2 Block Diagram

The block diagram below shows the UART module design for the CC35xx.

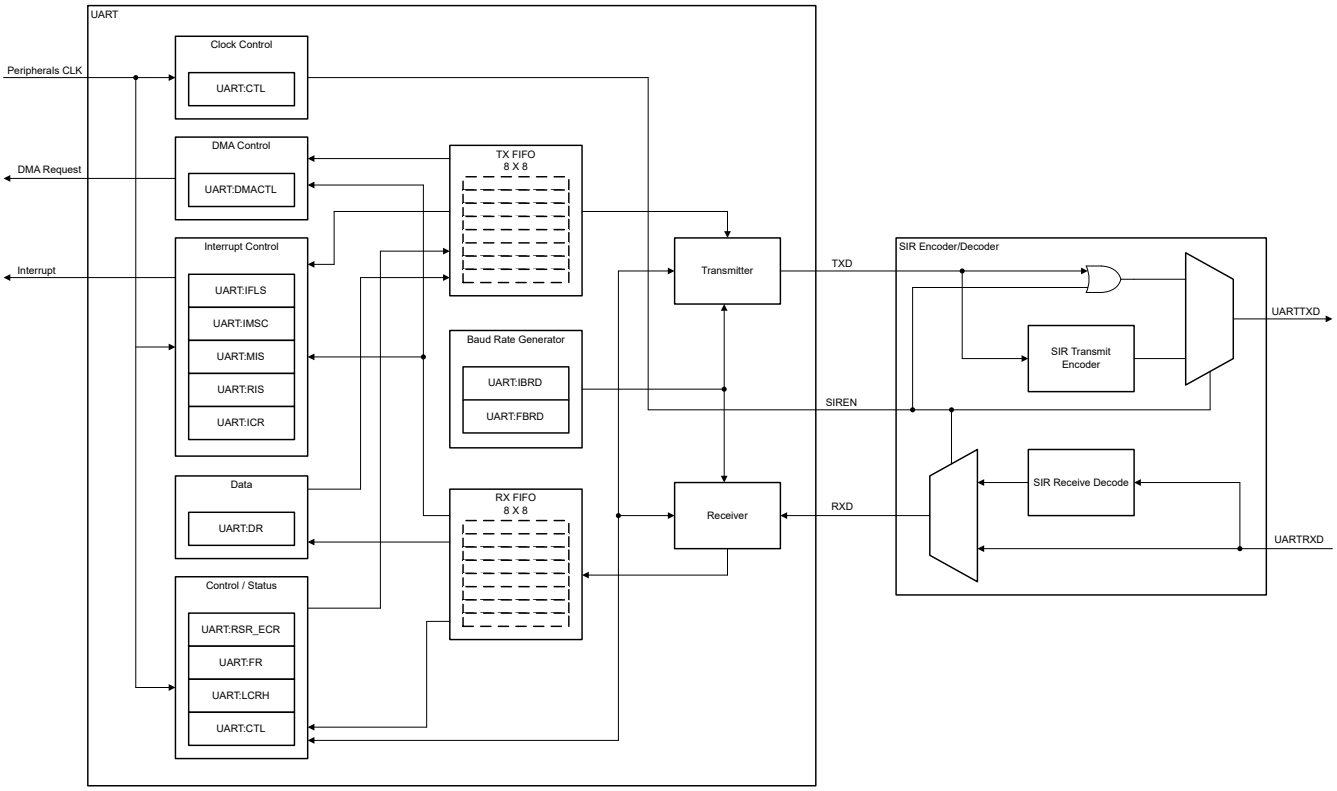

Figure 17-1. UART Block Diagram

17.3 UART Functional Description

The CC35xx UART performs the functions of parallel-to-serial and serial-to-parallel conversions. The UART is configured for transmit and receive through the UART Control Register (UART:CTL) TXE and RXE bits. Transmit and receive are both enabled out of reset. Before any control registers are programmed, the UART must be disabled by clearing the UART:CTL UARTEN register bit. If the UART is disabled during a transmit or receive operation, the current transaction completes before the UART stops.

17.3.1 Transmit and Receive Logic

The transmit logic performs parallel-to-serial conversion on the data read from the TX FIFO. The control logic outputs the serial bit stream beginning with a start bit and followed by the data bits (LSB first), parity bit, and the stop bits, according to the programmed configuration in the control registers. For details, see Figure 17-2 The receive logic performs serial-to-parallel conversion on the received bit stream after a valid start pulse is detected. Overrun, parity, frame error checking, and line-break detection are also performed, and their status accompanies the data written to the RX FIFO.

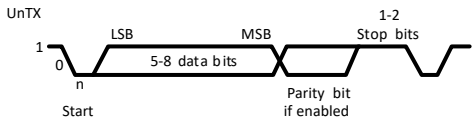

Figure 17-2. UART Character Frame

17.3.2 Baud Rate Generation

The baud rate divisor (BRD) is a 22-bit number consisting of a 16-bit integer and a 6-bit fractional part. The number formed by these two values is used by the baud rate generator to determine the bit period. Having a fractional baud rate divider allows the UART to generate all standard baud rates.

The 16-bit integer is loaded through the UART Integer Baud Rate Divisor Register (UART.IBRD), and the 6-bit fractional part is loaded with the UART Fractional Baud Rate Divisor Register (UART.FBRD).

The following equation shows the relationship of the BRD and the system clock.

where:

$$BRD = BRDI + BRDF = SOC\,CLK / (ClkDiv \times Baud\,Rate) \quad (2)$$

- BRDI is the integer part of the BRD
- BRDF is the fractional part, separated by a decimal place
- SOC CLK is the system clock connected to the UART
- ClkDiv is 16

The 6-bit fractional number that is loaded into the UART:FBRD.DIVFRAC bit field can be calculated by taking the fractional part of the baud rate divisor, multiplying by 64, and adding 0.5 to account for rounding errors, as shown by Equation 3

$$\text{UART.FBRD}[5:0]\ \text{DIVFRAC} = \text{integer}\,(\text{BRDF} \times 64 + 0.5) \quad (3)$$

Along with the UART Line Control High Byte Register (UART.LCRH), the UART.IBRD and the UART.FBRD registers form an internal 30-bit register. This internal register is updated only when a write operation to the UART.LCRH register is performed, so a write to the UART.LCRH register must follow any changes to the BRD for the changes to take effect.

The four possible sequences to update the baud-rate registers are as follows:

- UART.IBRD write, UART.FBRD write, and UART.LCRH write
- UART.FBRD write, UART.IBRD write, and UART.LCRH write
- UART.IBRD write and UART.LCRH write
- UART.FBRD write and UART.LCRH write

For an example calculation see Section 17.6.

17.3.3 FIFO Operation

The UART has two 8-entry FIFOs. One FIFO for transmit and one FIFO for receive. Both FIFOs are accessed through the UART Data Register, UART.DR. Read operations of the UART.DR register return a 8-bit value consisting of 8 data bits and 4 error flags, while write operations place 8-bit data in the TX FIFO.

Out of reset, both FIFOs are disabled and act as 1-byte-deep holding registers. The FIFOs are enabled by setting the UART.LCRH[4] FEN bit.

FIFO status can be monitored through the UART Flag Register, UART.FR and the UART Receive Status Register, UART.RSR_ECR. Hardware monitors empty, full, and overrun conditions. The UART.FR register contains empty and full flags (TXFE, TXFF, RXFE, and RXFF bits), and the UART.RSR_ECR register shows overrun status through the OE bit. If the FIFOs are disabled, the empty and full flags are set according to the status of the 1-byte deep holding registers.

The trigger points at which the FIFOs generate interrupts are controlled through the UART Interrupt FIFO Level Select Register (UART:IFLS). Both FIFOs can be individually configured to trigger interrupts at different levels. Available configurations include ¼, ½ and ¾. For example, if the ¼ option is selected for the receive FIFO, the UART generates a receive interrupt after 4 data bytes are received. Out of reset, both FIFOs are configured to trigger an interrupt at the ½ mark.

17.3.3.1 FIFO Remapping

The UART supports concatenation of TX and RX FIFOs in TX only mode - leading to 16 TX entries. Remapping and concatenation for RX only mode is not supported. This mode is enabled by setting the UART.CTL[6] FCEN bit to 1.

17.3.4 Data Transmission

Data received or transmitted is stored in two FIFOs, though the RX FIFO has an extra 4 bits per character for status information. For transmission, data is written into the TX FIFO. If the UART is enabled, a dataframe starts transmitting with the parameters indicated in the UART.LCRH register. Data transmission continues until no data is left in the TX FIFO. The UART Flag Register (UART.FR) BUSY bit is asserted as soon as data is written to the TX FIFO (that is, if the FIFO is not empty), and remains asserted while data is transmitting. The BUSY bit is negated only when the TX FIFO is empty, and the last character has been transmitted from the shift register, including the stop bits. The UART can indicate that it is busy even if the UART is no longer be enabled.

When the receiver is idle (the UARTRXD signal is continuously 1), and the data input goes low (a start bit was received), the receive counter begins running and data is sampled.

The start bit is valid and recognized if the UARTRXD signal is still low on the eighth cycle of the baud rate clock otherwise the start bit is ignored. After a valid start bit is detected, successive data bits are sampled on every sixteenth cycle of the baud rate clock. The parity bit is then checked if parity mode is enabled. Data length and parity are defined in the UART:LCRH register.

Lastly, a valid stop bit is confirmed if the UARTRXD signal is high; otherwise a framing error has occurred. When a full word is received, the data is stored in the receive FIFO with any error bits associated with that word.

17.3.5 Flow Control

Flow control can be accomplished by hardware and the following sections describe the implementation method. Hardware flow control between two devices is accomplished by connecting the RTS (Request-to-send) output to the CTS (Clear-to-send) input on the receiving device, and connecting the RTS output on the receiving device to the CTS input. The RTS output signal is low active, the CTS input expects a low signal on a send request as shown in Figure 17-3.

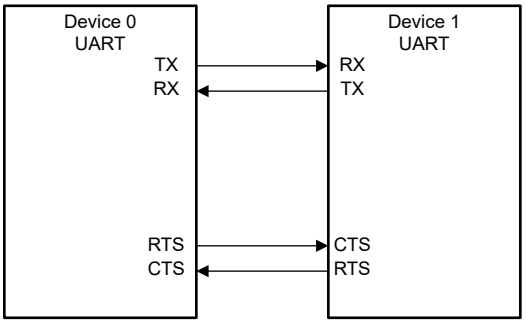

Figure 17-3. UART Flow Control

The CTS input controls the transmitter, the Device 0 and Device 1 transmitter can only transmit data when their CTS input is asserted low. When RTS flow control is enabled, the RTS output signal indicates the state of the receive FIFO. For example, the CTS of the Device 1 remains asserted low until the preprogrammed RX FIFO level of Device 0 is reached, indicating that the receive FIFO of Device 0 has no space to store additional characters.

The UART:CTL register bits CTSEN and RTSEN specify the flow control mode as shown in following table.

CTSEN	RTSEN	Description
1	1	RTS and CTS flow control enabled
1	0	Only CTS flow control enabled

CTSEN	RTSEN	Description
0	1	Only RTS flow control enabled
0	0	RTS and CTS flow control disabled

When RTSEN is set to 1, the value of the UART:CTL.RTS bit is ignored and the RTS output signal is generated by the hardware trigger levels as described below. When RTSEN bit is cleared, the RTS signal output is controlled by the UART:CTL.RTS bit for SW control.

RTS Flow Control

The RTS flow control logic is linked to the programmable receive FIFO trigger levels. The trigger level can be configured using the UART.IFLS register. When RTS flow control is enabled, the RTS is asserted (low) until the receive FIFO is filled up to the trigger level. When the receive FIFO trigger level is reached, the RTS signal is de-asserted (high), indicating that there is no more room to receive any more data. The transmission of data is expected to cease after the current character has been transmitted.

The RTS signal is reasserted (low) when data has been read out of the receive FIFO so that the FIFO is filled to less than the trigger level. If RTS flow control is disabled and the UART is still enabled, then data is received until the receive FIFO is full, or no more data is transmitted. The RTS signal is de-asserted when the FIFO trigger level is reached by putting the last received character into the FIFO. This means that on a back-to-back transmit, another character transfer can already be started by the sender prior to the RTS signal be de-asserted. In such cases the trigger level needs to be set to one level lower so that all data can be received and added into the FIFO.

CTS Flow Control

If CTS flow control is enabled, then the transmitter checks the CTS signal before transmitting the next byte. If the CTS signal is asserted (low), it transmits the byte otherwise transmission does not occur. The data continues to be transmitted while CTS is asserted (low), and the transmit FIFO is not empty. If the transmit FIFO is empty and the CTS signal is asserted (low) no data is transmitted. If the CTS signal is de-asserted (high) and CTS flow control is enabled, then the current character transmission is completed before stopping. If CTS flow control is disabled and the UART is enabled, then the data continues to be transmitted until the transmit FIFO is empty.

Software Flow Control

Software flow control between two devices is accomplished by using interrupts to indicate the status of the UART. Interrupts can be generated for the CTS signal by setting the UART.IMSC[1] CTSMIM bit. The raw and masked interrupt status can be checked using the UART.RIS and UART.MIS registers. These interrupts can be cleared using the UART.ICR register.

17.3.6 IrDA Encoding and Decoding

When the UART.CTL[1] SIREN bit is set, the IrDA (SIR) encoder and decoder are enabled and provide hardware bit shaping for IrDA communication. In this protocol, from the transmitter perspective, a zero is transmitted as a high pulse and a one is transmitted as a zero.

The width of the pulse is specified as 3/16th of the selected bit period. The SIR decoder converts the IrDA compliant receive signal into a bit stream for the UART core. The SIR receive logic interprets a high state as a logic one and low pulses as logic zeros. For more details please refer to the SIR Physical Layer Link Specification Version 1.1

Setting the UART.CTL SIRLP[2] bit enables low power mode. In the low power mode, the width of the pulse is set to 3 times the time period of the IrLPBaud16 signal. The IrLPBaud16 signal is generated by dividing down the SOC CLK (80MHz) according to the low-power divisor value written to the UARTILPR register. The low-power divisor value is calculated as follows:

$$low - power\ divisor\ (ILPDVSR)\ =\ (SOC\ CLK\ /(FIrLPBaud16 \times 3\ )) \quad (4)$$

where FIrLPBaud16 is nominally 1.8432 MHz.

The divisor must be selected such that 1.42 MHz < FIrLPBaud16 < 2.12 MHz, results in a low-power pulse duration of 1.41-2.11µs (three times the period of IrLPBaud16).

Note

In low-power IrDA mode the UART rejects random noise on the received serial data input by ignoring SIRIN pulses that are less than 3 periods of IrLPBaud16.

The time period of the nSIROUT bit stream is still equal to the programmed bit period and is governed by the period of the Baud16 signal.

The SIR receiver section contains a 4-bit binary counter, which operates on SOC CLK in the normal mode with the Baud16 signal as an enable signal. When the input SIRIN signal is high, the decoded output signal, RXD, is driven high to indicate a 1. A low on the SIRIN line is sampled multiple times on IrLPBaud16 for glitch rejection and converted into a low on the RXD line. The time period for which the RXD line is pulled low corresponds to approximately one bit period at the programmed bit rate. After the counter rolls over, input sampling restarts. The SIRLPSync signal is the SOC CLK-synchronised version of the SIRLP mode selection bit in the UART.CTL register. This signal determines the IrDA encoding strategy i.e. whether the IrDA transmitter block is to operate in the normal mode or in the low power mode. The SIRENSync signal is the SIREN bit in the UART.CTL register, which has been synchronised to SOC CLK. This signal enables / disables the SIR section.

17.3.7 Interrupts

The UART can generate interrupts when the following conditions are observed:

- Overrun error
- Break error
- Parity error
- Framing error
- Receive time-out
- Transmit (when the condition defined in the UART:IFLS TXSEL register bit is met)
- Receive (when the condition defined in the UART:IFLS RXSEL register bit is met)
- End of transmission (when no data on TX line and TX FIFO underflow

All of the interrupt events are ORed together before being sent to the Event Manager, so the UART can only generate a single interrupt request at any given time. Software can service multiple interrupt events in a single interrupt service routine (ISR) by reading the UART Masked Interrupt Status Register (UART.MIS).

The interrupt events that can trigger a controller-level interrupt are defined in the UART Interrupt Mask Register (UART.IMSC) by setting the corresponding bits. If interrupts are not used, the raw interrupt status is always visible through the UART Raw Interrupt Status Register (UART.RIS).

Interrupts can be cleared (for the UART.MIS and UART.RIS registers) by setting the corresponding bit in the UART Interrupt Clear Register (UART.ICR).

The receive time-out interrupt is asserted when the RX FIFO is not empty, and no further data is received over a 32-bit period. The receive time-out interrupt is cleared either when the FIFO becomes empty through reading all the data (or by reading the holding register), or when the corresponding bit in the UART.ICR register is set.

The UART module provides the possibility of setting and clearing masks for every individual interrupt source using the UART Interrupt Mask Set/Clear Register (UART.IMSC). The five events that can cause combined interrupts to CPU are:

- RX: The receive interrupt changes state when one of the following events occurs:
  - If the FIFOs are enabled and the receive FIFO reaches the programmed trigger level. When this happens, the receive interrupt is asserted high. The receive interrupt is cleared by reading data from the receive FIFO until it becomes less than the trigger level, or by clearing the interrupt.

  - If the FIFOs are disabled (have a depth of one location) and data is received, thereby filling the location, the receive interrupt is asserted high. The receive interrupt is cleared by performing a single read of the receive FIFO, or by clearing the interrupt.
- TX: The transmit interrupt changes state when one of the following events occurs:
  - If the FIFOs are enabled and the transmit FIFO is equal to or lower than the programmed trigger level, then the transmit interrupt is asserted high. The transmit interrupt is cleared by writing data to the transmit FIFO until it becomes greater than the trigger level, or by clearing the interrupt.
  - If the FIFOs are disabled (have a depth of one location) and there is no data present in the transmitters single location, the transmit interrupt is asserted high. The interrupt is cleared by performing a single write to the transmit FIFO, or by clearing the interrupt.
- RX time-out: The receive time-out interrupt is asserted when the receive FIFO is not empty, and no more data is received during a 32-bit period. The receive time-out interrupt is cleared either when the FIFO becomes empty through reading all the data (or by reading the holding register), or when 1 is written to the corresponding bit of the Interrupt Clear Register (UART:ICR).
- Modem status: The modem status interrupt is asserted if the modem status signal CTS toggles. It can be cleared using the corresponding clear bit in the UART.ICR register.
- Error: The error interrupt is asserted when an error occurs in the reception of data by the UART. The interrupt can be caused by a number of different error conditions:
  - framing
  - parity
  - break
  - overrun

The cause of the interrupt can be determined by reading the UART.RIS register or the UART.MIS register. The interrupt can be cleared by writing to the relevant bits of the UART.ICR register.

17.3.8 Loopback Operation

The UART can be placed into an internal loopback mode for diagnostic or debug work by setting the UART:CTL.LBE register bit. In loopback mode, data transmitted on the UARTTXD output is received on the UARTRXD input. The LBE bit must be set before the UART is enabled.

17.4 UART-LIN Specification

17.4.1 Break transmission in UART mode

- When TXBRK is set in LCRH and UART is idle, TXD pin is driven low and kept low until SW clears TXBRK bit.
- When TXBRK is set when transmission is active, ongoing data packet will be sent out and thenTXD pin is driven low and kept low until TXBRK is cleared by SW.
- If TXFIFO contains data, transmission will resume once TXBRK is cleared by SW.
- SW recommendation is to keep TXBRK set for two times the length of data packet for proper break operation.

17.4.2 Break reception in UART mode

- When RXD goes low, counter is started with preload value equal to length of data packet (start + data + parity + stop).
- Slave baud rate setting will be used to define bit time.
- If RXD goes high before counter expires, counter is cleared and break condition is ignored.
- If RXD is low until counter expires, break error condition is detected (set BE flag) and value 0 is moved to RX FIFO.

17.4.3 Break/Synch transmission in LIN mode

- UART and LIN modes have to be enabled.
- Master baud rate and desired delimiter value should be configured by SW.
- SW needs to set TXBRKSYNC bit in LCRH for break/synch transmission (TXBRKSYNC is redundant in UART mode).

- This should start break transmission if UART is idle else it completes ongoing transmission and starts break/synch transmission right after.
- Counter is preloaded with value 12 and decremented to achieve break duration of 13-bit time.
- Delimit duration should be based on delimit value configured.
- Synch field 0x55 transmission should begin automatically (start, 8-bit data and stop bit).
- When synch transmission is completed, TXBRKSYNC bit should be reset automatically by HW.
- SW can write PID value into TXFIFO immediately after setting the TXBRKSYNC.
- HW after synch transmission will check TXFE and if TXFE = 1 it does not transmit anything and if TXFE = 0 it transmits data from TXFIFO (In LIN mode it is only one-bytePID that will be written).

17.4.4 Break/Synch reception in LIN mode

- UART, LIN and ABD modes have to be enabled.
- Slave baud rate is configured to desired value by SW.
- When RXD pin goes low, counter is preloaded with value 21 and decremented on bit clock.
- If RXD goes high within 11-bittimes, counter is reset and break is ignored.
- If RXD goes high within 12 to 21-bittimes, stop counter and regard it as valid break field (set LINBRK).
- If RXD does not go high until counter expiry, generate break error condition (set LINBTOE).
- Start a counter on fall edge of synch field and count up to 5 edges (measurement is from first to last falling edges of synch field).
- Integer and fractional counters are started at first fall edge of synch field and stopped at last fall edge.
- Captured integer and fractional counters values are adjusted by suitable scaling factor and used to update baud rate register values.
- When the integer counter overflows during synch field baud rate measurement, synch timeout error flag is set.
- Calculate min and max baud rate that can be detected in LIN mode.
- LINBRK flag to be cleared upon read from DR (data register).

17.4.5 Dormant mode operation

- This mode is relevant onlyin LIN mode operation (LINEN = 1) else takes no effect.
- When disabled, break and synch data will be loaded to RX FIFO and related interrupt flags will be set (as in normal operation).
- When enabled, break only (wake signal) or break and synch data will not be loaded to RX FIFO.
- In this case RX FIFO will be updated with actual data (PID) after successful reception of break/synch fields.

17.4.6 Event signal generation

- Master or slave node can generate event signal on LIN cluster.
- Header alone can be transmitted as event signal.
- When TXBRK bit is set in LIN mode, break field alone is transmitted (13-bittimes of value 0).
- Configured baud rate shall be used for break field transmission.
- TXBRK bit shall be auto cleared at the end of break field transmission
- Expected software sequence for LIN master:
  - Set LIN mode, configure baud rate
  - Set TXBRK for event signal generation
  - Once TXBRK is auto cleared, SW can set TXBRKSYNC
  - This starts break/synch sequence in hardware
  - After setting TXBRKSYNC, SW can write PID into TXFIFO
  - Once synch field is transmitted out, hardware clears TXBRKSYNC bit and starts transmitting PID from TXFIFO

17.4.7 Event signal detection when device is in active/idle modes

- When RXD pin goes low, counter is started to detect break condition.
- If the break field duration is longer than 11-bittimes LINBRK will be set.
- If the break field duration is longer than 21-bit times LINBTOE will be set.

- If the break field duration is shorter than 11-bit times (minimum can be 150us as per LIN protocol) break condition is treated invalid and ignored.
- This will be fine since the purpose of event signal transmission is to wake up the device only and, in this case, device is already in active/idle state and UART is ready to receive break/synch fields.
- If necessary DIO based interrupt on RXD pin can also be generated for software use.
- RXD pin will not glitch as it is generated by the LIN transceiver.

17.4.8 Event signal detection when device is in sleep mode

- Software has to configure RXD pin for fall edge-basedwake fromstandby.
- When RXD pin goes low, IO MUX triggers PRCM for standby exit.
- Software has to reconfigure UART as necessary for LIN mode operation.
- UART is then ready to receive break/sync fields.
- Event condition will not be detected within UART module through LINBRK or LINBTOE bits.
- This will be fine since the purpose of event signal transmission is to wake up the device only.

17.5 Interface to Host DMA

The UART provides an interface to the DMA controller with two separate channels. The DMA operation of the UART is enabled through the UART event and DMA peripheral registers. When the DMA functionality is enabled, the UART asserts a DMA request on the selected channel when the associated FIFO can transfer data.

For the receive channel, a DMA transfer request is asserted whenever the amount of data in the receive FIFO is at or above the FIFO trigger level configured in the UART.FIFOLEV register. For the transmit channel, a request is asserted whenever the transmit FIFO contains fewer characters than the FIFO trigger level configured in the UART.FIFOLEV register.

Interupt registers are used to setup the trigger signaling for the DMA.This can be setup in a flexible way to trigger the DMA for Controller or Target and receive or transmit events. Software should avoid using the same trigger source for multiple interrupt lines concurrently.

Figure 17-4 shows the interface between the Host DMA and UART.

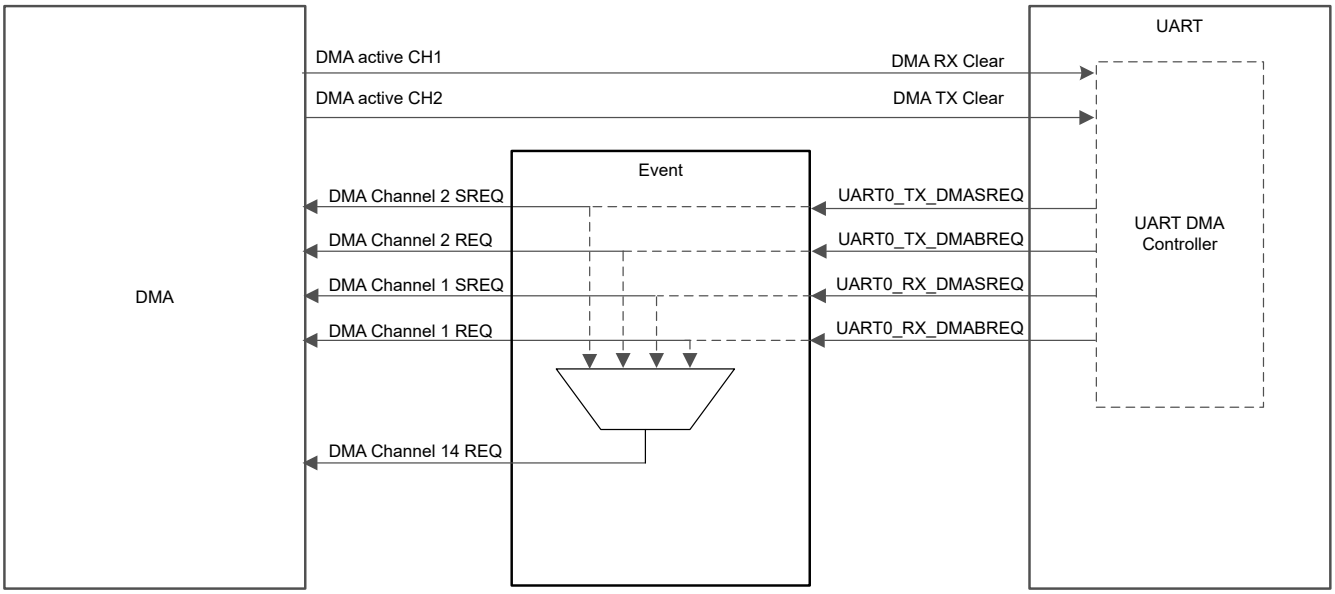

Figure 17-4. DMA Example

When the UART is in the FIFO enabled mode, data transfers can be made by either single or burst transfers depending on the programmed watermark level and the amount of data in the FIFO. Table 17-1 lists the trigger points for the transmit and receive FIFOs. In addition, if the UART.DMACTL[2] DMA ERR bit is set, the Host DMA receive request outputs (for single and burst requests) are disabled when the UART error interrupt is

asserted (more specifically if any of the error interrupts in the RIS register, PARITY, BREAK, FRMERR or OVRNERR are asserted). The Host DMA receive request outputs remain inactive until the error bit is cleared. The Host DMA transmit request outputs are unaffected.

Table 17-1. DMA Trigger Points for the Transmit and Receive FIFOs

Watermark Level	Transmit Burst Length (number of empty locations)	Receive Burst Length (number of filled locations)
1/4	6	2
1/2	4	4
3/4	2	6

17.6 Initialization and Configuration

The UART module provides four I/O signals to be routed to the GPIOs. The following signals are selected through the GPIOnPCFG registers in the IOMUX module.

- Inputs: RXD, CTS
- Outputs: TXD, RTS

CTS and RTS lines are active low.

Note

IOMUX must be configured before enabling the UART to avoid unwanted transitions on the input being processed as UART signals. When IOMUX is configured as UART-specific I/Os (RXD, CTS, TXD, or RTS), IOMUX sets static output driver enable to the GPIO (output driver enable = 1 for output TXD and RTS and output driver enable = 0 for inputs RXD and CTS).

To enable and initialize the UART, use the following steps:

1. Enable the clock to the UART module by setting the CLKCFG bit to 1.
2. Configure the IOMUX module to map UART signals to the correct GPIO pins. For more information on pin connections, see Chapter 16.

This section discusses the steps required to use a UART module. For this example, the UART clock is assumed to be 80MHz, and the desired UART configuration is the following:

- Baud rate: 115 200
- Data length of 8 bits
- One stop bit
- No parity
- FIFOs disabled
- No interrupts

The first thing to consider when programming the UART is the BRD because the UART.IBRD and UART.FBRD registers must be written before the UART.LCRH register. The BRD can be calculated using the equation described in Section 17.3.2.

$$BRD = 80\,000\,000 / (16 \times 115\,200) = 43.403 \quad (5)$$

The result of previous equation indicates that the UART.IBRD[15:0] DIVINT bit field must be set to 43 decimal or 0x2B.

$$UART.FBRD[5:0]\ DIVFRAC = integer(0.403 \times 64 + 0.5) = 26 \quad (6)$$

The previous equation calculates the value to be loaded into the UART.FBRD register.

With the BRD values available, the UART configuration is written to the module in the following order:

1. Disable the UART by clearing the UART.CTL[0] UARTEN bit
2. Write the integer portion of the BRD to the UART.IBRD register
3. Write the fractional portion of the BRD to the UART.FBRD register
4. Write the desired serial parameters to the UART.LCRH register (in this case, a value of 0x0000 0060)
5. Enable the UART by setting the UART.CTL[0] UARTEN bit

17.7 UART Registers

Table 17-2 lists the memory-mapped registers for the UART registers. All register offset addresses not listed in Table 17-2 should be considered as reserved locations and the register contents should not be modified.

Table 17-2. UART Registers

Offset	Acronym	Register Name	Section
0h	DATA	Data Register	Section 17.7.1
4h	RXSTAT	Receive Status Register	Section 17.7.2
18h	FLAG	Status Flags	Section 17.7.3
20h	LPWRDIV	IrDA Low-Power Counter	Section 17.7.4
24h	IBRD	Integer Baudrate Divisor	Section 17.7.5
28h	FBRD	Fractional Baudrate Divider	Section 17.7.6
2Ch	LINECON	Line Control	Section 17.7.7
30h	UARTCTL	Operation Control	Section 17.7.8
34h	FIFOLEV	FIFO Level Select	Section 17.7.9
38h	IMASK	Interrupt Mask Control	Section 17.7.10
3Ch	RISSTAT	Raw Interrupt Status	Section 17.7.11
40h	MIS	Masked Interrupt Status	Section 17.7.12
44h	ICLR	Interrupt Clear	Section 17.7.13
48h	DMACTL	DMA Control	Section 17.7.14
FE0h	PERID0	Peripheral Identifier 0	Section 17.7.15
FE4h	PERID1	Peripheral Identification 1	Section 17.7.16
FE8h	PERID2	Peripheral Identification 2	Section 17.7.17
FECh	PERID3	Peripheral Identification 3	Section 17.7.18
FF0h	CELLID0	Cell Identification Register	Section 17.7.19
FF4h	CELLID1	Cell Identification Register	Section 17.7.20
FF8h	CELLID2	Cell Identification Register	Section 17.7.21
FFCh	CELLID3	Cell Identification Register	Section 17.7.22
1000h	CLKCTL	Clock Configuration	Section 17.7.23

Complex bit access types are encoded to fit into small table cells. Table 17-3 shows the codes that are used for access types in this section.

Table 17-3. UART Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

17.7.1 DATA Register (Offset = 0h) [Reset = 00000000h]

DATA is shown in Table 17-4.

Return to the Summary Table.

Data Register (DATA) This register serves as the data interface for UART transmission and reception operations. Transmit Operation: - When FIFOs are enabled (FIFO EN = 1): Data written to this register is pushed onto the transmit First-In-First-Out (FIFO) buffer. - When FIFOs are disabled (FIFO EN = 0): Data is stored in the transmitter holding register (the bottom word of the transmit FIFO). Writing to this register automatically initiates data transmission from the Universal Asynchronous Receiver/Transmitter (UART). The data byte is formatted with a start bit, the appropriate parity bit (if parity is enabled), and a stop bit before transmission. Receive Operation: - When FIFOs are enabled: The data byte along with 4-bit status information (break, frame, parity, and overrun) is pushed onto the 12-bit wide receive FIFO. - When FIFOs are disabled: The data byte and status are stored in the receiving holding register (the bottom word of the receive FIFO). To read received data, perform reads from this register. This operation provides both the data byte and corresponding status information. Status information can also be accessed separately through the RSR register.

Table 17-4. DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	OVRERR	R	0h	UART Overrun Error: This read-only bit indicates whether a data overrun error has occurred. When set to 1, it indicates that new data was received while the receive First-In-First-Out (FIFO) buffer was already full. The existing FIFO contents remain valid because no additional data is written to a full FIFO; only the contents of the shift register are overwritten. The bit automatically clears to 0 when space becomes available in the FIFO, allowing a new character to be written to it.
10	BRKERR	R	0h	Break Error: This read-only bit indicates whether a break condition was detected on the UART receive line. When set to 1, it signals that the received data input (UARTRXD input pin) was held LOW for longer than a full-word transmission time (including start bit, data bits, parity bit, and stop bits). In FIFO (First-In-First-Out) mode, this error is associated with the character at the top of the FIFO (the oldest received data character since the last read operation). When a break condition occurs, a null character (0x00) is automatically loaded into the FIFO. Normal character reception resumes after the receive data input (UARTRXD input pin) returns to a logical 1 (marking state) and the next valid start bit is detected.
9	PERERR	R	0h	Parity Error (PE): Indicates a parity error in received data. When set to 1, the parity of the received data character does not match the expected parity as configured by the Line Control Register High (LCRH) fields for Even Parity Select (EPS) and Stick Parity Select (SPS). In First-In-First-Out (FIFO) mode, this error is associated with the character at the top of the FIFO (the oldest received data character since the last read operation). This read-only bit serves as an indicator for data integrity issues during transmission.
8	FRMERR	R	0h	UART Framing Error: This read-only bit indicates whether the received character has a valid stop bit (a valid stop bit is 1). When set to 1, a framing error has occurred, meaning the stop bit was invalid. In First-In-First-Out (FIFO) mode, this error is associated with the character at the top of the FIFO (the oldest received data character since the last read operation). The framing error typically indicates problems with clock synchronization between transmitter and receiver or incorrect baud rate settings.
7-0	DATA	R/W	0h	Data Character [7:0]. This 8-bit field contains the data being transmitted or received. When writing to this field, the data character is pushed into the First-In-First-Out (FIFO) buffer for transmission. When reading from this field, the oldest received data character that has not yet been read is returned from the receive FIFO. Each read operation advances the FIFO pointer to the next available character.

17.7.2 RXSTAT Register (Offset = 4h) [Reset = 00000000h]

RXSTAT is shown in Table 17-5.

Return to the Summary Table.

Status This register is mapped to the same address as RXSTAT.* register. Reads from this address are associated with [RSR_ECR.*] register and return the receive status. Writes to this address are associated with RXSTAT.* register and clear the receive status flags (framing, parity, break, and overrun errors). If the status is read from this register, then the status information for break, framing and parity corresponds to the data character read from the Data Register, [DR.*] prior to reading the [RSR_ECR.*]. The status information for overrun is set immediately when an overrun condition occurs.

Table 17-5. RXSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	OVRERR	R/W	0h	UART Overrun Error: This bit is set to 1 if data is received and the receive **FIFO** is already full. The **FIFO** contents remain valid because no more data is written when the **FIFO** is full, , only the contents of the shift register are overwritten. This is cleared to 0 once there is an empty space in the **FIFO** and a new character can be written to it. 0h (R) = Error flag is not set 0h (W) = Clears error flag if error is set. Write value is not important. 1h (R) = Error flag is set 1h (W) = Clears error flag if error is set. Write value is not important.
2	BRKERR	R/W	0h	UART Break Error: This bit is set to 1 if a break condition was detected, indicating that the received data input (**UARTRXD** input pin) was held LOW for longer than a full-word transmission time (defined as start, data, parity and stop bits). When a break occurs, a 0 character is loaded into the **FIFO**. The next character is enabled after the receive data input (**UARTRXD** input pin) goes to a 1 (marking state), and the next valid start bit is received. 0h (W) = Clears error flag if error is set. Write value is not important. 0h (R) = Error flag is not set 1h (W) = Clears error flag if error is set. Write value is not important. 1h (R) = Error flag is set
1	PERERR	R/W	0h	UART Parity Error: When set to 1, it indicates that the parity of the received data character does not match the parity that the EVPAR and STICKPAR select. 0h (R) = Error flag is not set 0h (W) = Clears error flag if error is set. Write value is not important. 1h (R) = Error flag is set 1h (W) = Clears error flag if error is set. Write value is not important.
0	FRMERR	R/W	0h	UART Framing Error: When set to 1, it indicates that the received character did not have a valid stop bit (a valid stop bit is 1). 0h (R) = Error flag is not set 0h (W) = Clears error flag if error is set. Write value is not important. 1h (R) = Error flag is set 1h (W) = Clears error flag if error is set. Write value is not important.

17.7.3 FLAG Register (Offset = 18h) [Reset = 00000000h]

FLAG is shown in Table 17-6.

Return to the Summary Table.

Status Flags Register (FLAG) This read-only register provides the current status of the Universal Asynchronous Receiver/Transmitter (UART) through various flags. These flags indicate the operational state of the UART, including buffer status, line conditions, and transmission states. Reading this register allows software to monitor UART status without affecting ongoing operations.

Table 17-6. FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	TXEMPTY	R	1h	UART Transmit FIFO Empty: This read-only bit indicates the empty status of the transmitter. The meaning of this bit depends on the state of the FIFO Enable bit (LCRH.FEN): - If the FIFO is disabled (LCRH.FEN = 0), this bit is set when the transmit holding register is empty. - If the FIFO is enabled (LCRH.FEN = 1), this bit is set when the transmit FIFO is empty. Note: This bit does not indicate if there is data in the transmit shift register, which may still be sending data when this bit is set.
6	RXFULL	R	0h	UART Receive First-In-First-Out (FIFO) Full. This read-only bit indicates whether the receive buffer is at capacity. The behavior of this bit depends on the state of the FIFO Enable (FEN) bit in the Line Control Register (LCRH): - When FIFO is disabled (LCRH.FEN = 0): This bit is set to 1 when the receive holding register contains data and cannot accept additional incoming data. - When FIFO is enabled (LCRH.FEN = 1): This bit is set to 1 when the receive FIFO buffer is completely full and cannot store additional bytes. This status bit can be used to prevent data loss by indicating when the receiver cannot accept more data.
5	TXFULL	R	0h	UART Transmit First-In-First-Out (FIFO) Full: This read-only bit indicates whether the transmit buffer is full. The specific behavior depends on the FIFO enable setting in the Line Control Register (LCRH.FEN): - When FIFO is disabled: This bit is set to 1 when the transmit holding register is full, indicating that no more data can be written until space becomes available. - When FIFO is enabled: This bit is set to 1 when the transmit FIFO buffer is completely full, indicating that no more data can be written until at least one byte has been transmitted. When this bit is set, attempts to write to the transmit buffer will result in data loss.
4	RXEMPTY	R	1h	UART Receive FIFO Empty (RXFE): This read-only bit indicates whether the receive First-In-First-Out (FIFO) buffer is empty. The interpretation of this bit depends on the FIFO Enable (FEN) setting in the Line Control Register (LCRH): - When FIFO is disabled (LCRH.FEN = 0): This bit is set to 1 when the receive holding register is empty. - When FIFO is enabled (LCRH.FEN = 1): This bit is set to 1 when the receive FIFO buffer is empty. When RXFE = 1, no more data is available to read. When RXFE = 0, at least one data entry is present in the receive buffer.
3	TXBUSY	R	0h	UART Busy (Transmitter Active): This read-only bit indicates whether the Universal Asynchronous Receiver/Transmitter (UART) is actively transmitting data. When set to 1, the UART is busy sending data through the transmission line. The bit remains set until the complete byte, including all stop bits, has been transmitted from the shift register. This bit is automatically set as soon as the transmit First-In-First-Out (FIFO) buffer becomes non-empty, regardless of whether the UART is enabled or disabled.
2-1	RESERVED	R	0h	Reserved

Table 17-6. FLAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CLEAR TO SEND	R	0h	Clear To Send (CTS): This read-only bit indicates the status of the active-low CTS input pin on the Universal Asynchronous Receiver/ Transmitter (UART). When the CTS input pin is in a LOW state, this bit reads as 1. Conversely, when the CTS input pin is in a HIGH state, this bit reads as 0. This field allows software to monitor the hardware flow control signal status without directly accessing the pin.

17.7.4 LPWRDIV Register (Offset = 20h) [Reset = 00000000h]

LPWRDIV is shown in Table 17-7.

Return to the Summary Table.

The IrDA Low-Power Counter Register (LPWRDIV) configures the divisor values used in the IrDA low-power mode. This 32-bit read-write register determines the pulse width duration when the UART is operating in IrDA low-power mode. The programmed value in this register sets the division factor for the low-power infrared transmissions, allowing the system to meet the IrDA SIR low-power specification timing requirements.

Table 17-7. LPWRDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	LPDIV	R/W	0h	Low Power Divisor (ILPDVSR) - An 8-bit value that determines the baud rate divisor for the UART when operating in low-power mode. This field configures the frequency division applied to the UART clock source, allowing for power optimization while maintaining communication at reduced rates. Writing to this field updates the divisor value immediately.

17.7.5 IBRD Register (Offset = 24h) [Reset = 00000000h]

IBRD is shown in Table 17-8.

Return to the Summary Table.

Integer Baud-Rate Divisor Register (IBRD) This register contains the integer portion of the baud-rate divisor value used to establish the UART communication speed. The baud-rate is calculated using the following formula: Baud Rate = UARTCLK / (16 x (IBRD + (FBRD/64))) When this register is modified while transmission or reception is in progress, the new baud-rate value will not take effect until the current character transmission or reception is complete. This prevents communication errors during active data transfer. Address offset: 0x36 Size: 32 bits Access: Read-Write

Table 17-8. IBRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	INTEGER DIVISOR	R/W	0h	Integer Baud Rate Divisor This 16-bit field specifies the integer component of the baud rate divisor used to configure the UART communication speed. The baud rate divisor is calculated using the following formula: Baud rate divisor = (UART reference clock frequency) / (16 x Baud rate) The valid range for the integer divisor is 1 to 65535. Setting INTEGER DIVISOR to 0 does not produce a valid baud rate. Additionally, if INTEGER DIVISOR is set to 0xFFFF, any non-zero values in the fractional baud rate divisor field FRAC will result in an invalid configuration. You must program a valid value to this field before performing any UART (Universal Asynchronous Receiver/Transmitter) receive (RX) or transmit (TX) operations.

17.7.6 FBRD Register (Offset = 28h) [Reset = 00000000h]

FBRD is shown in Table 17-9.

Return to the Summary Table.

Fractional Baud-Rate Divisor Register This register stores the fractional part of the baud-rate divisor value. Together with the integer part (stored in the IBRD register), it determines the UART baud rate. The fractional divisor is calculated as a 6-bit value (0-63) that represents m/64 where m is the fractional part. Important: If this register is modified while transmission or reception is ongoing, the baud rate will not be updated until the current character's transmission or reception is complete. This prevents data corruption during active communications. The FBRD register must be accessed using 32-bit word operations.

Table 17-9. FBRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	FRAC	R/W	0h	Fractional Baud-Rate Divisor: This 6-bit field contains the fractional component of the baud rate divisor value. The complete baud rate divisor is calculated using the formula: Baud rate divisor = (UART reference clock frequency) / (16 x Baud rate) The divisor consists of an integer part (stored in IBRD.DIVINT) and this fractional part. The divisor must be between 1 and 65535 to be valid. Note that setting IBRD.DIVINT to 0 results in an invalid baud rate. Similarly, if IBRD.DIVINT is set to 0xFFFF, any non-zero values in DIVFRAC would create an invalid value exceeding the maximum. A valid value must be written to this field before the Universal Asynchronous Receiver/Transmitter (UART) can be used for receiving (RX) or transmitting (TX) operations.

17.7.7 LINECON Register (Offset = 2Ch) [Reset = 00000000h]

LINECON is shown in Table 17-10.

Return to the Summary Table.

Line Control Register (LINECON) - Controls UART line parameters including word length, parity, stop bits, and FIFO operation. This register configures the serial communication format and enables or disables the transmit and receive FIFOs. Settings in this register determine how data is framed during transmission and how it should be interpreted during reception.

Table 17-10. LINECON Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-9	DELIMLEN	R/W	1h	Delimiter Length. This field defines the length of the delimiter field that must be transmitted in UART Local Interconnect Network (LIN) mode. The value in this field determines the number of bits used for the delimiter in LIN communication. 0h = 0 1h = 1 2h = 2 3h = 3
8	BRKSYNC	R/W	0h	Transmit Break Synchronization (TXBRKSYNC): Controls the transmission of synchronization field in Local Interconnect Network (LIN) mode. 0: Synchronization field will not be transmitted in LIN mode. 1: Synchronization field will be transmitted in LIN mode and this bit will be automatically reset after transmission. Note: This functionality is only effective when parity is enabled via the PEN bit. When parity checking is disabled, this bit has no effect on UART operation.
7	STICKPAR	R/W	0h	Stick Parity Select: Controls whether the UART uses stick parity mode. 0: Stick parity is disabled 1: Stick parity is enabled. The parity bit is transmitted and checked as the inverse of the Even Parity Select (EPS) field value. When EPS=0, the parity bit is fixed at 1; when EPS=1, the parity bit is fixed at 0. Note: This bit has no effect when the Parity Enable (PEN) bit is set to 0, which disables all parity checking and generation.
6-5	WORDLEN	R/W	0h	UART Word Length: These bits define the number of data bits transmitted or received in each frame. The WLEN field allows configuration of the data word size according to the following values: 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits (default) 0h = Word Length 5 bits 1h = Word Length 6 bits 2h = Word Length 7 bits 3h = Word Length 8 bits
4	FIFO EN	R/W	0h	FIFO Enable. This bit enables the transmit and receive FIFOs (First-In-First-Out buffers). When set to 1, the FIFOs are enabled. When set to 0, the FIFOs are disabled, and the UART operates in character mode where only the transmitter holding register and receiver buffer register are used. For normal operation, this bit should be set to 1. 0h = **FIFO**s are disabled (character mode) that is, the **FIFO**s become 1-byte-deep holding registers. 1h = Transmit and receive **FIFO** buffers are enabled (**FIFO** mode)
3	TWOSTBIT	R/W	0h	Two Stop Bits Select (STP2): When set to 1, the UART transmits two stop bits at the end of each frame instead of the standard single stop bit. When cleared to 0, the UART transmits one stop bit. Note that the receive logic does not verify the presence of two stop bits, regardless of this setting.

Table 17-10. LINECON Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EVPAR	R/W	0h	Even Parity Select. When set to 1, even parity generation and checking is enabled. When cleared to 0, odd parity is selected if the Parity Enable (PEN) bit is set. This bit has no effect when the PEN bit is cleared. 0h = Odd parity: The **UART** generates or checks for an odd number of 1s in the data and parity bits. 1h = Even parity: The **UART** generates or checks for an even number of 1s in the data and parity bits.
1	PAREN	R/W	0h	Parity Enable. When set to 1, this bit enables parity checking and generation during UART data transmission and reception. When cleared to 0, parity checking and generation are disabled. The type of parity used (odd, even, stick) is controlled by the EPS and SPS bits in this register. 0h = Parity is disabled and no parity bit is added to the data frame 1h = Parity checking and generation is enabled.
0	SBRK	R/W	0h	UART Send Break. When this bit is set to 1, the UARTTXD output pin is driven to a low-level continuously after completing the transmission of the current character. For the proper execution of the break command, software must maintain this bit at 1 for at least two complete frames. For normal UART operation, this bit must be cleared to 0. This feature is typically used to signal line breaks in serial communication protocols.

17.7.8 UARTCTL Register (Offset = 30h) [Reset = 00000000h]

UARTCTL is shown in Table 17-11.

Return to the Summary Table.

Control Register (UARTCTL) - This register controls the operation of the hardware module. It contains configuration bits that determine the operational behavior and features of the device. The CTL register allows users to enable or disable functionality, select operating modes, and configure runtime parameters. Changes to this register take effect immediately unless otherwise specified by individual field descriptions.

Table 17-11. UARTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	CTS EN	R/W	0h	Clear To Send (CTS) hardware flow control enable. When set to 1, this bit enables the CTS hardware flow control mechanism, allowing the peripheral to pause transmission when the CTS signal indicates the receiver is not ready. When cleared to 0, CTS hardware flow control is disabled, and the peripheral ignores the CTS input signal during data transmission. 0h = **CTS** hardware flow control disabled 1h = **CTS** hardware flow control enabled
14	RTSFLW	R/W	0h	Ready-to-Send (RTS) Hardware Flow Control Enable. When set to 1, this bit enables the RTS hardware flow control mechanism. When enabled, the UART asserts the RTS output signal when ready to receive data, and de-asserts it when the receive FIFO reaches the programmed threshold. When cleared to 0, RTS hardware flow control is disabled. 0h = **RTS** hardware flow control disabled 1h = **RTS** hardware flow control enabled
13-12	RESERVED	R	0h	Reserved
11	RTSEN	R/W	0h	Request To Send (RTS) - Controls the UART RTS (Request To Send) hardware flow control signal. When this bit is set to 1, the RTS output pin is driven LOW (active). When cleared to 0, the RTS output pin is driven HIGH (inactive). This bit directly controls the polarity of the external RTS signal used for hardware flow control to indicate to a connected device whether the UART is ready to receive data.
10	RESERVED	R	0h	Reserved
9	RXEN	R/W	1h	UART Receive Enable. When set to 1, this bit enables the receiver functionality of the UART. If the UART receiver is disabled during an active reception by clearing this bit, the current character will be completely received before the receiver stops operation. This allows for graceful disabling of the receiver without data loss. 0h = UART Receive disabled 1h = UART Receive enabled
8	TXEN	R/W	1h	Transmit Enable. When set, this bit enables the Universal Asynchronous Receiver/Transmitter (UART) transmission capability. When cleared, it disables transmission. If the UART is disabled during an active transmission, the hardware will complete the current character being transmitted before stopping the transmitter operation. This ensures that no partial characters are sent. 0h = UART Transmit disabled 1h = UART Transmit enabled
7	LPBACK	R/W	0h	Loop Back Enable: When set to 1, enables the UART loopback mode. In this mode, the UART Transmit Data (UARTTXD) output is internally connected to the UART Receive Data (UARTRXD) input, creating a closed testing circuit. This allows the transmission of data to be verified without external connections. When cleared to 0, the UART operates in normal mode with standard input/output paths. 0h = Loop Back disabled 1h = Loop Back enabled

Table 17-11. UARTCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	FIFOCNT	R/W	0h	UART FIFO Concatenation Enable. When this bit is set, the FIFO (First-In-First-Out) concatenation feature is enabled in transmit (TX) mode, effectively doubling the transmit buffer capacity to 16 entries. This allows for more efficient data transmission by reducing the frequency of buffer empty conditions. 0h = UART FIFO Concatenation disabled 1h = UART FIFO Concatenation enabled
5	DORM	R/W	0h	DORMEN bit is only functionally makes sense for LIN mode of operation. When dormant mode is disabled, break and sync data shall be loaded to RX FIFO and associated interrupt flags shall be set as in normal UART operation. When dormant mode is enabled, break and sync data shall not be loaded to RX FIFO and RX FIFO shall be updated with actual data (PID) only after successful reception of break/sync fields. 0h = 0 1h = 1
4	AUTBDEN	R/W	0h	Auto Baud Detection Enable. This bit enables or disables the automatic baud rate detection feature in Line Interface Network (LIN) mode. When set to 1, the controller automatically detects the baud rate from the incoming data stream. When cleared to 0, automatic baud rate detection is disabled and the baud rate must be manually configured. 0h = 0 1h = 1
3	LIN	R/W	0h	LIN Mode Enable. This bit configures the module to operate in Local Interconnect Network (LIN) mode. When set to 1, the module operates in LIN mode according to the LIN specification. When cleared to 0, the module operates in standard mode. This setting affects communication protocol parameters and timing characteristics. 0h = 0 1h = 1
2	IR LP MODE	R/W	0h	IrDA Low Power Mode Enable. This bit selects the Infrared Data Association (IrDA) encoding mode. When set to 1, the transmitter and receiver operate in low power mode. When cleared to 0, the standard IrDA mode is used. Low power mode reduces power consumption but may affect communication range. 0h = Low-level bits are transmitted as active high with a 3/16th period width, 1h = Low-level bits are transmitted with a pulse width of 3 times the period of IrLPBaud16, regardless of the selected bit rate.
1	IRDA	R/W	0h	Serial Infrared (SIR) Enable. When set to 1, enables the IrDA SIR modulation/demodulation functionality for transmitting and receiving data. When cleared to 0, the SIR function is disabled. Note that this bit has no effect if the UART is disabled via the UARTEN bit. Both UARTEN and SIREN must be set to enable SIR operation. 0h = IrDA SIR ENDEC is disabled 1h = IrDA SIR ENDEC is enabled. Data is transmitted and received via nSIROUT and SIRIN.
0	EN	R/W	0h	UART Enable - Controls the operating state of the UART module. When set to 1, the UART is enabled and fully functional. When cleared to 0, the UART is disabled and enters a low-power state. All UART registers can still be accessed while the module is disabled, but the transmitter and receiver are inactive. The UART must be enabled before any data transmission or reception can occur. 0h = UART disabled 1h = UART enabled

17.7.9 FIFOLEV Register (Offset = 34h) [Reset = 00000000h]

FIFOLEV is shown in Table 17-12.

Return to the Summary Table.

Interrupt **FIFO** Level Select

Table 17-12. FIFOLEV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-3	RXFIFOLV	R/W	2h	Receive interrupt **FIFO** level select: This field sets the trigger points for the receive interrupt. Values 0b101-0b111 are reserved. 1h = Receive **FIFO** becomes >= 1/4 full 2h = Receive **FIFO** becomes >= 1/2 full 3h = Receive **FIFO** becomes >= 3/4 full
2-0	TX FIFO LVL	R/W	2h	Transmit interrupt **FIFO** level select: This field sets the trigger points for the transmit interrupt. Values 0b101-0b111 are reserved. 1h = Transmit **FIFO** becomes <= 1/4 full 2h = Transmit **FIFO** becomes <= 1/2 full 3h = Transmit **FIFO** becomes <= 3/4 full

17.7.10 IMASK Register (Offset = 38h) [Reset = 00000000h]

IMASK is shown in Table 17-13.

Return to the Summary Table.

Interrupt Mask Set/Clear Register (IMASK) - This register controls which interrupts are enabled or inactive. When a bit is set to 1, the corresponding interrupt is enabled and can generate an interrupt request to the system. When a bit is set to 0, the corresponding interrupt is inactive and will not generate an interrupt request, although the interrupt status can still be read through the status registers. Writing to this register sets or clears individual mask bits based on the written value.

Table 17-13. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	LSYNCTO	R/W	0h	LIN Synchronization Timeout Error Interrupt Mask. This bit controls whether the Local Interconnect Network (LIN) synchronization timeout error generates an interrupt. When set to 1, the LINSYNCTOE interrupt is unmasked, and its state will be reflected in the MIS.LINSYNCTOE register. When cleared to 0, the LINSYNCTOE interrupt is masked, preventing it from being reflected in MIS.LINSYNCTOE. Reading this bit returns the current mask state for the LINSYNCTOE interrupt.
15	LINBTOE	R/W	0h	LIN Break Timeout Error Interrupt Mask. This bit controls the masking of the Linear Interface (LIN) Break Timeout Error interrupt. When read, it returns the current mask status for the UART's LINBRKTOE interrupt. Writing a 1 to this bit sets the interrupt mask, causing the interrupt state to be reflected in the MIS.LINBRKTOE register. Writing a 0 clears the mask, preventing the interrupt state from being reflected in MIS.LINBRKTOE. This allows software to selectively enable or disable interrupt generation for LIN break timeout error conditions.
14	LBRKM	R/W	0h	LIN Break Interrupt Mask. Controls whether a Local Interconnect Network (LIN) break field received or detected will generate an interrupt. When read, this bit returns the current mask state for the UART's LIN break interrupt. Writing a 1 enables the interrupt (the interrupt state will be reflected in MIS.LINBRK register field). Writing a 0 disables the interrupt (MIS.LINBRK will not reflect the interrupt state). When enabled, the interrupt is triggered when the UART detects a LIN break condition on the receive line.
13	RXDMIM	R/W	0h	Receive Direct Memory Access (DMA) Done Interrupt Mask. This bit controls whether the receive DMA completion interrupt is enabled. When set to 1, the RXDMADONE interrupt is unmasked, allowing its state to be reflected in the Masked Interrupt Status register (MIS.RXDMADONEMIS). When cleared to 0, the RXDMADONE interrupt is masked, preventing it from being reflected in MIS.RXDMADONEMIS. Reading this bit returns the current mask state for the receive DMA done interrupt.
12	TXDMAIM	R/W	0h	Transmit DMA Done Interrupt Mask. This bit controls whether the TXDMADONE interrupt is masked. When read, it returns the current mask state for the Transmit DMA Done interrupt. Writing a 1 enables the interrupt, causing its state to be reflected in the MIS.TXDMADONEMIS register. Writing a 0 disables the interrupt, preventing it from being reflected in MIS.TXDMADONEMIS. This interrupt is triggered when a DMA transfer to the transmit FIFO has completed.
11	EOTIM	R/W	0h	End of Transmission Interrupt Mask. Controls whether the End of Transmission (EoT) interrupt is enabled. When set to 1, the EoT interrupt is enabled, and its state will be reflected in the MIS.EOTMIS field of the Masked Interrupt Status Register. When cleared to 0, the EoT interrupt is disabled, and MIS.EOTMIS will not reflect the interrupt even if it occurs. Reading this bit returns the current mask state for the UART's EoT interrupt.

Table 17-13. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	OEIM	R/W	0h	Overrun Error Interrupt Mask. This bit controls whether the overrun error interrupt is enabled or masked. When read, it returns the current mask state for the UART (Universal Asynchronous Receiver/ Transmitter) overrun error interrupt. Writing 1 to this bit enables the interrupt (sets the mask), causing the interrupt state to be reflected in the MIS.OEMIS field of the Masked Interrupt Status Register. Writing 0 disables the interrupt (clears the mask), preventing the overrun error condition from generating an interrupt and MIS.OEMIS will not reflect the interrupt state.
9	BRKERRIM	R/W	0h	Break Error Interrupt Mask. This bit controls whether break errors generate an interrupt. When set to 1, break error interrupts are enabled and their status will be reflected in the Break Error Masked Interrupt Status (MIS.BEMIS) bit. When cleared to 0, break error interrupts are masked, preventing them from being reflected in MIS.BEMIS. Reading this bit returns the current mask state for the Universal Asynchronous Receiver/Transmitter (UART) break error interrupt.
8	PEERRM	R/W	0h	Parity Error Interrupt Mask. This bit controls whether parity errors generate an interrupt. When set to 1, the UART parity error interrupt is enabled, and parity error conditions will be reflected in the MIS.PEMIS (Masked Interrupt Status - Parity Error) bit. When cleared to 0, parity error interrupts are masked, preventing these conditions from being reflected in MIS.PEMIS. Reading this bit returns the current mask state for the UART's parity error interrupt.
7	FEIM	R/W	0h	Framing Error Interrupt Mask. This bit controls whether framing errors trigger an interrupt. When set to 1, the framing error interrupt is enabled, causing the interrupt status to be reflected in the Masked Interrupt Status register (MIS.FEMIS). When cleared to 0, framing error interrupts are masked and will not be reflected in MIS.FEMIS. Reading this bit returns the current mask state for the Universal Asynchronous Receiver/Transmitter (UART) framing error interrupt.
6	RXTOUT	R/W	0h	Receive Timeout Interrupt Mask. This bit controls the masking of the Universal Asynchronous Receiver/Transmitter (UART) receive timeout interrupt. When read, it returns the current mask state for the receive timeout interrupt. When written: - Writing 1: Enables the receive timeout interrupt. When enabled, the interrupt state will be reflected in the MIS.RTMIS register bit. - Writing 0: Disables the receive timeout interrupt, preventing it from being reflected in the interrupt status. Note: The raw interrupt status for receive timeout (RIS.RTRIS) can only be set when this mask is enabled (RTIM = 1). This behavior serves as a power-saving feature, as the interrupt detection logic remains inactive until masked. When the mask is enabled, the same interrupt status can be read from either MIS.RTMIS or RIS.RTRIS registers.
5	TXINT	R/W	0h	Transmit Interrupt Mask. Controls whether the transmit interrupt is masked. When this bit is set to 1, the transmit interrupt is unmasked, allowing the interrupt status to be reflected in the TXMIS bit of the Masked Interrupt Status (MIS) register. When cleared to 0, the transmit interrupt is masked, preventing it from being reflected in the MIS.TXMIS bit. Reading this bit returns the current mask state for the Universal Asynchronous Receiver/Transmitter (UART) transmit interrupt.
4	RXINT	R/W	0h	Receive Interrupt Mask. This bit controls whether the receive interrupt is enabled. When set to 1, the mask for the Universal Asynchronous Receiver/Transmitter (UART) receive interrupt is enabled, causing the interrupt state to be reflected in the Masked Interrupt Status register (MIS.RXMIS). When cleared to 0, the mask is disabled, preventing the receive interrupt from being reflected in MIS.RXMIS. Reading this bit returns the current mask status for the UART's receive interrupt.
3-2	RESERVED	R	0h	Reserved

Table 17-13. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CTSM	R/W	0h	Clear To Send (CTS) modem interrupt mask. When set to 1, this bit enables the CTS modem interrupt, allowing the interrupt state to be reflected in the Masked Interrupt Status register (MIS.CTSMMIS). When cleared to 0, the CTS modem interrupt is masked, preventing it from being reflected in MIS.CTSMMIS. Reading this bit returns the current mask state for the UART's Clear To Send interrupt.
0	RESERVED	R	0h	Reserved

17.7.11 RISSTAT Register (Offset = 3Ch) [Reset = 00000000h]

RISSTAT is shown in Table 17-14.

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Raw Interrupt Status

Table 17-14. RISSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	LINTOESY	R	0h	LIN SYNC field time out interrupt status: This field returns the raw interrupt state of whether sync field is measurable in UART's LIN mode of operation. This is set when the timer measuring the SYNC field overflows.
15	LINBKTMO	R	0h	LIN BRK field time out interrupt status: This field returns the raw interrupt state of whether break field is measurable in UART's LIN mode of operation. This is set when the timer measuring the Break field overflows.
14	LINBRK	R	0h	LIN BRK detected interrupt status: This field returns the raw interrupt state of whether break field is received/detected in UART's LIN mode of operation.
13	RXDMADN	R	0h	Rx DMA done interrupt status: This field returns the raw interrupt state of UART's rx dma done interrupt. RX DMA done flag is set when you receive rx dma done status from dma module.
12	DMADTX	R	0h	Tx DMA done interrupt status: This field returns the raw interrupt state of UART's tx dma done interrupt. TX DMA done flag is set when you receive tx dma done status from dma module.
11	TXEOT	R	0h	End of Transmission interrupt status: This field returns the raw interrupt state of UART's end of transmission interrupt. End of transmission flag is set when all the Transmit data in the FIFO and on the TX Line is transmitted.
10	OVRNERR	R	0h	Overrun error interrupt status: This field returns the raw interrupt state of **UART**'s overrun error interrupt. Overrun error occurs if data is received and the receive **FIFO** is full.
9	BREAK	R	0h	Break error interrupt status: This field returns the raw interrupt state of **UART**'s break error interrupt. Break error is set when a break condition is detected, indicating that the received data input (**UARTRXD** input pin) was held LOW for longer than a full-word transmission time (defined as start, data, parity and stop bits).
8	PARITY	R	0h	Parity error interrupt status: This field returns the raw interrupt state of **UART**'s parity error interrupt. Parity error is set if the parity of the received data character does not match the parity that the EVPAR and STICKPAR select.
7	FRMERR	R	0h	Framing error interrupt status: This field returns the raw interrupt state of **UART**'s framing error interrupt. Framing error is set if the received character does not have a valid stop bit (a valid stop bit is 1).
6	RXTO	R	0h	Receive timeout interrupt status: This field returns the raw interrupt state of **UART**'s receive timeout interrupt. The receive timeout interrupt is asserted when the receive **FIFO** is not empty, and no more data is received during a 32-bit period. The receive timeout interrupt is cleared either when the **FIFO** becomes empty through reading all the data, or when a 1 is written to RTIC. The raw interrupt for receive timeout cannot be set unless the mask is set (RXTOUT = 1). This is because the mask acts as an enable for power saving. That is, the same status can be read from RTOUT and RXTO.

Table 17-14. RISSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TXRIS	R	0h	Transmit interrupt status: This field returns the raw interrupt state of **UART**'s transmit interrupt. When **FIFO**s are enabled (FIFO EN = 1), the transmit interrupt is asserted if the number of bytes in transmit **FIFO** is equal to or lower than the programmed trigger level (TX FIFO LVL). The transmit interrupt is cleared by writing data to the transmit **FIFO** until it becomes greater than the trigger level, or by clearing the interrupt through TXCLR. When **FIFO**s are disabled (FIFO EN = 0), that is they have a depth of one location, the transmit interrupt is asserted if there is no data present in the transmitters single location. It is cleared by performing a single write to the transmit **FIFO**, or by clearing the interrupt through TXCLR.
4	RXINT	R	0h	Receive interrupt status: This field returns the raw interrupt state of **UART**'s receive interrupt. When **FIFO**s are enabled (FIFO EN = 1), the receive interrupt is asserted if the receive **FIFO** reaches the programmed trigger level (RXFIFOLV). The receive interrupt is cleared by reading data from the receive **FIFO** until it becomes less than the trigger level, or by clearing the interrupt through RXICLR. When **FIFO**s are disabled (FIFO EN = 0), that is they have a depth of one location, the receive interrupt is asserted if data is received thereby filling the location. The receive interrupt is cleared by performing a single read of the receive **FIFO**, or by clearing the interrupt through RXICLR.
3-2	RESERVED	R	0h	Reserved
1	CTSRIS	R	0h	Clear to Send (CTS) modem interrupt status: This field returns the raw interrupt state of **UART**'s clear to send interrupt.
0	RESERVED	R	0h	Reserved

17.7.12 MIS Register (Offset = 40h) [Reset = 00000000h]

MIS is shown in Table 17-15.

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Masked Interrupt Status (MIS) Register. This read-only register contains the masked interrupt status flags. A set bit (1) indicates that the corresponding interrupt is active and enabled in the interrupt mask register. A cleared bit (0) indicates that either the interrupt is not active or it is disabled by the mask register. Reading this register provides immediate visibility of all interrupt conditions that can trigger an interrupt request to the processor.

Table 17-15. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	LINSYNCTO	R	0h	LIN Synchronization Field Timeout Error Interrupt Status: This read-only bit returns the masked interrupt state of the Local Interconnect Network (LIN) synchronization field timeout error interrupt. The value is the logical AND of the raw interrupt state (RIS.LINSYNCTOERIS) and the interrupt mask setting (IMSC.LINSYNCTOEIM). When set to 1, it indicates that a masked LIN synchronization timeout error interrupt is active.
15	LINBRKTO	R	0h	LIN Break Field Timeout Error Interrupt Status: This read-only bit indicates the masked interrupt state of the Local Interconnect Network (LIN) Break Field timeout error. The value is determined by the logical AND of the raw interrupt state (RIS.LINBRKTOERIS) and the corresponding interrupt mask setting (IMSC.LINBRKTOEIM). When set to 1, it indicates that a masked LIN Break Field timeout error interrupt is active and requires service.
14	BRKM	R	0h	Local Interconnect Network (LIN) Break Masked Interrupt Status. This read-only field indicates the masked interrupt status of the LIN break detection mechanism. A value of 1 indicates that a LIN break has been detected and the interrupt is enabled. This value represents the logical AND of the raw interrupt status (RIS.LINBRKRIS) and the interrupt mask setting (IMSC.LINBRKIM). When this field is set, it means a valid LIN break condition has been detected on the interface and requires software attention.
13	DMARXDN	R	0h	Rx DMA done interrupt status: This field returns the masked interrupt state of the rx dma done interrupt which is the AND product of raw interrupt state RIS.RXDMADONERIS and the mask setting IMSC.RXDMADONEIM.
12	TXDMAIS	R	0h	Transmit DMA Done Masked Interrupt Status: This read-only field indicates the masked interrupt status of the Transmit DMA Done interrupt. It returns the logical AND result of the raw interrupt state (RIS.TXDMADONERIS) and the interrupt mask setting (IMSC.TXDMADONEIM). When this bit is set to 1, it indicates that a Transmit DMA Done interrupt is both active and enabled.
11	EOTTXM	R	0h	End of Transmission (EOT) Interrupt Status: This read-only field indicates the masked interrupt state of the End of Transmission interrupt. It represents the logical AND of the raw interrupt state (RIS.EOTRIS) and the interrupt mask setting (IMSC.EOTIM). When this bit is set to 1, it indicates that a transmission has completed and the associated interrupt is both active and enabled. This status can be used to determine if an End of Transmission interrupt is pending service.
10	OVRERR	R	0h	Overrun Error Masked Interrupt Status: Indicates the masked interrupt status of the overrun error condition. This bit is the logical AND of the raw interrupt state (RIS.OERIS) and the interrupt mask setting (IMSC.OEIM). When this bit is set to 1, it indicates that an overrun error has occurred and the interrupt is not masked. Read-only.

Table 17-15. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	BERR	R	0h	Break Error Masked Interrupt Status: This read-only field indicates the current masked interrupt state of the break error interrupt. The value represents the logical AND of the raw break error interrupt state (BREAK) and the corresponding interrupt mask setting (BRKERRIM). When set to 1, it indicates that both a break error has been detected and its interrupt is enabled. When set to 0, either no break error has occurred or the break error interrupt is masked.
8	PERR	R	0h	Parity Error Masked Interrupt Status: This read-only field indicates the current masked interrupt status of the parity error interrupt. It represents the logical AND between the raw interrupt state PARITY and the interrupt mask setting PEERRM. When this bit is set to 1, both a parity error has occurred and its interrupt is enabled. This field can be used to determine if a parity error is currently triggering an interrupt request to the system.
7	FEERR	R	0h	Framing Error Masked Interrupt Status: This read-only bit returns the masked interrupt state of the framing error interrupt. It represents the logical AND of the raw interrupt state FRMERR and the interrupt mask setting FEIM. When set to 1, it indicates that a framing error has occurred and the corresponding interrupt is enabled. This field can be used to determine if a framing error is contributing to an interrupt condition.
6	RTOUT	R	0h	Receive Timeout Masked Interrupt Status: This read-only bit returns the masked interrupt state of the receive timeout interrupt. The raw interrupt for receive timeout cannot be set unless the corresponding interrupt mask bit is enabled (RXTOUT = 1). This behavior is designed for power saving, as the mask functions as an enable control. As a result, the same status information can be read from both this bit (RTOUT) and the raw interrupt status bit (RXTO).
5	TXIS	R	0h	Transmit Masked Interrupt Status: This read-only bit indicates the current state of the masked transmit interrupt. It represents the logical AND between the raw transmit interrupt status TXRIS and the transmit interrupt mask TXINT. When this bit is set to 1, it indicates that a transmit interrupt is both active and enabled. This field can be used to determine if a transmit interrupt is currently requesting service.
4	RXIS	R	0h	Masked Receive Interrupt Status: This read-only field indicates the current status of the masked receive interrupt. It represents the logical AND operation between the raw receive interrupt state (RIS.RXRIS) and the receive interrupt mask setting (IMSC.RXIM). When this bit is set to 1, it indicates that both the raw receive interrupt is active and its corresponding mask is enabled, signaling that the interrupt requires service. When clear (0), either no receive interrupt is pending or the interrupt is masked.
3-2	RESERVED	R	0h	Reserved
1	CTSM	R	0h	Clear to Send (CTS) Modem Masked Interrupt Status: This read-only field indicates the masked interrupt status of the Clear to Send modem interrupt. It represents the logical AND between the raw interrupt state CTSRIS and the interrupt mask setting CTSM. When this bit is set to 1, it indicates that a CTS interrupt is pending and has been enabled via the mask register. When set to 0, either no CTS interrupt is pending or the interrupt is disabled by the mask.
0	RESERVED	R	0h	Reserved

17.7.13 ICLR Register (Offset = 44h) [Reset = 00000000h]

ICLR is shown in Table 17-16.

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Interrupt Clear Register (ICLR) This write-only register clears specific interrupts. Writing a '1' to any bit position clears the corresponding interrupt. Writing a '0' to any bit position has no effect. After writing to this register, the corresponding interrupt status bits in the interrupt status register will be cleared, indicating that the interrupt has been acknowledged. Note: This is a write-only register and will return undefined values when read.

Table 17-16. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18-17	RESERVED	R	0h	Reserved
16	SYNTOUT	W	0h	LIN SYNC Timeout Interrupt Clear: Writing 1 to this field clears the Local Interconnect Network (LIN) synchronization timeout error interrupt (RIS.LINSYNCTOERIS). Writing 0 has no effect. This bit is write-only.
15	LINBKTOC	W	0h	LIN Break Timeout Error Interrupt Clear: Writing 1 to this bit clears the LIN Break Timeout Error interrupt (indicated by RIS.LINBRKTOERIS). Writing 0 has no effect. This bit is write-only and is used to acknowledge and clear the timeout condition that occurs when a LIN break field is detected.
14	LINBRK	W	0h	LIN Break Interrupt Clear: Writing 1 to this field clears the Linear Integrated Network (LIN) break field detected interrupt (RIS.LINBRKRIS). Writing 0 has no effect. This field allows software to acknowledge and clear a detected LIN break condition.
13	RDMAIC	W	0h	Receive Direct Memory Access (DMA) Done Interrupt Clear: Writing 1 to this bit clears the Receive DMA Done interrupt status (indicated by RIS.RXDMADONERIS). Writing 0 to this bit has no effect. This field is write-only and is used to acknowledge and clear the interrupt after it has been serviced.
12	TXDMAIC	W	0h	Transmit DMA Done Interrupt Clear: Writing 1 to this field clears the Transmit DMA Done interrupt (indicated by RIS.TXDMADONERIS). Writing 0 to this field has no effect. This write-only bit allows software to acknowledge and clear the interrupt after the DMA has completed a transmit operation.
11	EOTC	W	0h	End of Transmission (EOT) Interrupt Clear: Writing 1 to this field clears the End of Transmission interrupt flag (RIS.EOTRIS). Writing 0 to this field has no effect. This bit is write-only and is used to acknowledge and clear the EOT interrupt after the transmission has completed.
10	OERCLR	W	0h	Overrun Error Interrupt Clear: Writing 1 to this bit clears the overrun error interrupt flag (indicated by RIS.OERIS). Writing 0 has no effect. This field allows software to acknowledge and clear the overrun error condition after it has been handled.
9	BEIC	W	0h	Break Error Interrupt Clear: Writing 1 to this field clears the break error interrupt flag (indicated by the BERIS bit in the Raw Interrupt Status register). Writing 0 has no effect. This bit is write-only and is used to acknowledge and clear break error conditions detected by the hardware.
8	PERICLR	W	0h	Parity Error Interrupt Clear: Writing a 1 to this bit clears the parity error interrupt flag (indicated by the PERIS bit in the Raw Interrupt Status register). Writing a 0 has no effect. This field is write-only and is used to acknowledge and clear parity error conditions detected by the hardware.
7	FEICLR	W	0h	Framing Error Interrupt Clear: Writing a 1 to this bit clears the Framing Error interrupt status bit (FRMERR). Writing a 0 has no effect. This bit is write-only and is used to acknowledge and clear the framing error condition after it has been detected and handled by software.

Table 17-16. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RTIC	W	0h	Receive Timeout Interrupt Clear: Writing a 1 to this bit clears the receive timeout interrupt flag (indicated by RIS.RTRIS). Writing a 0 has no effect. This field is write-only and is used to acknowledge and clear receive timeout interrupt conditions.
5	TXCLR	W	0h	Transmit Interrupt Clear: Writing a 1 to this bit clears the transmit interrupt status flag (RIS.TXRIS). Writing a 0 has no effect. This write-only bit allows software to acknowledge and clear pending transmit interrupts.
4	RXICLR	W	0h	Receive Interrupt Clear: Writing a 1 to this field clears the receive interrupt status, as indicated in the Receive Interrupt Status bit (RXINT). Writing a 0 to this field has no effect. This write-only field provides a mechanism for acknowledging and clearing receive-related interrupt conditions.
3-2	RESERVED	W	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior. Write 0
1	CTSIC	W	0h	Clear to Send (CTS) Modem Interrupt Clear: Writing 1 to this bit clears the CTS modem interrupt status indicated by the CTSRMIS bit in the Raw Interrupt Status (RIS) register. Writing 0 to this bit has no effect. This field is write-only and is used to acknowledge and clear pending CTS modem interrupts.
0	RESERVED	W	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior. Write 0.

17.7.14 DMACTL Register (Offset = 48h) [Reset = 00000000h]

DMACTL is shown in Table 17-17.

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Direct Memory Access (DMACTL) Control Register. This register configures and controls the operation of the DMA controller, which enables high-speed data transfers between memory locations and peripherals without CPU intervention. The DMA controller can be configured to perform memory-to-memory, memory-to-peripheral, or peripheral-to-memory transfers, optimizing system performance by freeing the CPU for other tasks during data movement operations.

Table 17-17. DMACTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	DMA ERR	R/W	0h	DMA on Error. When set to 1, this bit disables the Direct Memory Access (DMA) receive request outputs (both single and burst requests) when a UART error interrupt is asserted. Specifically, the DMA is disabled when any of the following error interrupts occur: parity error PARITY, break error BREAK, framing error FRMERR, or overrun error OVRNERR. When cleared to 0, DMA receive requests continue to function regardless of UART errors.
1	TX DMA EN	R/W	0h	Transmit DMA Enable. When this bit is set to 1, Direct Memory Access (DMA) for the transmit First-In-First-Out (FIFO) buffer is enabled. This allows data transfers to occur between memory and the transmit FIFO without CPU intervention, improving data throughput and reducing processor overhead.
0	RX DMA EN	R/W	0h	Receive Direct Memory Access (DMA) Enable. When set to 1, this bit enables DMA operations for the receive First-In-First-Out (FIFO) buffer. When enabled, data transfers from the receive FIFO can occur without CPU intervention. When cleared to 0, DMA operations for the receive FIFO are disabled, and the CPU must handle data transfers.

17.7.15 PERID0 Register (Offset = FE0h) [Reset = 00000000h]

PERID0 is shown in Table 17-18.

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Peripheral Identification 0 Register . This read-only register contains the least significant byte of the peripheral identification code. It is part of the standard ARM peripheral identification registers that uniquely identify the peripheral. This register is primarily used during system initialization and debugging to confirm the peripheral type and version.

Table 17-18. PERID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	PART	R	11h	The PARTNUMBER0 field contains bits 0-7 of the peripheral part number. This read-only field helps identify the specific peripheral device. It is used in conjunction with PARTNUMBER1 (in register PERIPHID1) to form the complete part number identification code.

17.7.16 PERID1 Register (Offset = FE4h) [Reset = 00000000h]

PERID1 is shown in Table 17-19.

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Peripheral Identification Register 1 contains bits 12:8 of the peripheral identification code. This read-only register is part of the standard ARM peripheral identification registers that help software identify the peripheral. It works together with other peripheral identification registers (PERIPHID0, PERIPHID2, PERIPHID3) to form a complete peripheral ID. The value stored in this register is fixed at manufacturing time and cannot be modified by software.

Table 17-19. PERID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-4	DESGNID	R	1h	Designer Identification [4:7]. This read-only field identifies the designer of the peripheral, which in this case is ARM (Advanced RISC Machines). The field contains the upper four bits of the JEP-106 code that uniquely identifies ARM as the designer.
3-0	PARTNUM1	R	0h	Identifies the peripheral

17.7.17 PERID2 Register (Offset = FE8h) [Reset = 00000000h]

PERID2 is shown in Table 17-20.

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Peripheral Identification 2 Register. This read-only register is part of the standard ARM peripheral identification register set. It contains the device revision number and the designer's JEP106 identification code for this peripheral. This information can be used for device detection, firmware compatibility verification, and hardware revision identification.

Table 17-20. PERID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-4	REV	R	3h	Revision Number (REVISION): This read-only field contains the revision number of the UART peripheral. It identifies the specific version of the hardware implementation, allowing software to adapt to different hardware capabilities or behaviors between revisions.
3-0	DESGN1	R	4h	Designer Identifier. This read-only field identifies the designer of the peripheral as ARM. The field occupies bits [3:0] of the Peripheral Identification Register 2 (PERIPHID2) and is hard-coded during manufacturing.

17.7.18 PERID3 Register (Offset = FECh) [Reset = 00000000h]

PERID3 is shown in Table 17-21.

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Peripheral Identification 3 Register contains component identification information defined by ARM. This read-only register is part of the standard peripheral identification registers that help software identify the peripheral. The register holds manufacturer-specific information and, along with other peripheral ID registers, forms the complete peripheral identification code. This register is located at offset 0x4076 and has a width of 32 bits.

Table 17-21. PERID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	CONFIG	R	0h	Configuration Option [7:0] - This read-only field identifies the specific configuration option of the Universal Asynchronous Receiver/ Transmitter (UART) peripheral. The value indicates the hardware implementation variant and features available in this UART instance.

17.7.19 CELLID0 Register (Offset = FF0h) [Reset = 00000000h]

CELLID0 is shown in Table 17-22.

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PrimeCell Identification Register 0 contains part of the fixed identification code (0x0000000D) that uniquely identifies this as an ARM PrimeCell component. This read-only register holds the least significant byte of the identification code and is used in conjunction with PCELLID1-3 registers for peripheral identification. Software can read this register to verify the presence and type of peripheral in the system.

Table 17-22. CELLID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	RESERVED	R	0h	Reserved

17.7.20 CELLID1 Register (Offset = FF4h) [Reset = 00000000h]

CELLID1 is shown in Table 17-23.

Return to the Summary Table.

PrimeCell Identification Register 1 contains part of the standard ARM PrimeCell component identification code. This read-only register, located at offset 0x4084, contains the second byte of the 32-bit component identifier. It is typically used in conjunction with other component ID registers (PCELLID0, PCELLID2, and PCELLID3) for peripheral identification and discovery during system initialization.

Table 17-23. CELLID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	RESERVED	R	0h	Reserved

17.7.21 CELLID2 Register (Offset = FF8h) [Reset = 00000000h]

CELLID2 is shown in Table 17-24.

Return to the Summary Table.

PrimeCell Identification Register 2 contains part of the standard ARM PrimeCell identification code. This read-only register holds the second byte of the component identification code, providing information about the component type and features. This register, along with PCELLID0, PCELLID1, and PCELLID3, forms the complete PrimeCell identification signature that software can use to identify the peripheral.

Table 17-24. CELLID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	RESERVED	R	0h	Reserved

17.7.22 CELLID3 Register (Offset = FFCh) [Reset = 00000000h]

CELLID3 is shown in Table 17-25.

Return to the Summary Table.

PrimeCell Identification Register 3 contains the third byte of the component identification code. This read-only register is part of the CoreSight identification scheme that uniquely identifies this peripheral as a PrimeCell component. The register is located at offset 0x4092 and contains a fixed 32-bit value, though typically only the least significant byte is used. This register, along with PCELLID0-PCELLID2, forms the complete PrimeCell identification code that software can read to confirm the peripheral type during system initialization or debug.

Table 17-25. CELLID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	RESERVED	R	0h	Reserved

17.7.23 CLKCTL Register (Offset = 1000h) [Reset = 00000000h]

CLKCTL is shown in Table 17-26.

Return to the Summary Table.

Clock Configuration Register. This register controls the activation and deactivation of the Universal Asynchronous Receiver/Transmitter with Local Interconnect Network (UART-LIN) bus clock. When activated, the clock signal is provided to the UART-LIN interface, allowing it to operate. When deactivated, the clock is stopped to reduce power consumption, which prevents any UART-LIN communication.

Table 17-26. CLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CLKEN	R/W	0h	Memory Clock Enable. This bit enables or disables the bus clock for UART Linear Interface (Uartlin). When set to 1, the memory clock is enabled. When set to 0, the memory clock is disabled, which reduces power consumption but makes the UART Linear Interface inaccessible. 0h = Disables the clock to *Uartlin* 1h = Enables the clock to *Uartlin*

Chapter 18

Serial Peripheral Interface (SPI)

This chapter describes the Serial Peripheral Interface (SPI) module.

18.1 Overview

The Serial Peripheral Interface (SPI) module provides a standardized serial interface to transfer data to and from external devices using the SPI protocol (such as sensors, memories, ADCs or DACs).

18.1.1 Features

The SPI module has the following features:

- Programmable interface operation for Motorola SPI (3-wire and 4-wire), MICROWIRE, or TI Synchronous Serial format
- Configurable as a controller or a peripheral on the interface
- Programmable clock bit rate and prescaler
- CRC8-CCITT or CRC16-CCITT CRC capability
- Separate transmit (TX) and receive (RX) first-in first-out buffers (FIFOs)
  - If Data Size Select (DSS) is 4 to 8 bits, FIFOs are 32 locations, 8 bits wide
  - If Data Size Select (DSS) is 9 to 16 bits, FIFOs are 16 locations, 16 bits wide
- Programmable data frame size from 4 bits to 16 bits (controller mode) or 7 to 16 bits (peripheral mode)
- Internal loop-back test mode for diagnostic and debug testing
- Interrupts for transmit and receive FIFOs, overrun and time-out interrupts, completed DMA interrupts

18.1.2 Block Diagram

Figure 18-1 shows the SPI block diagram.

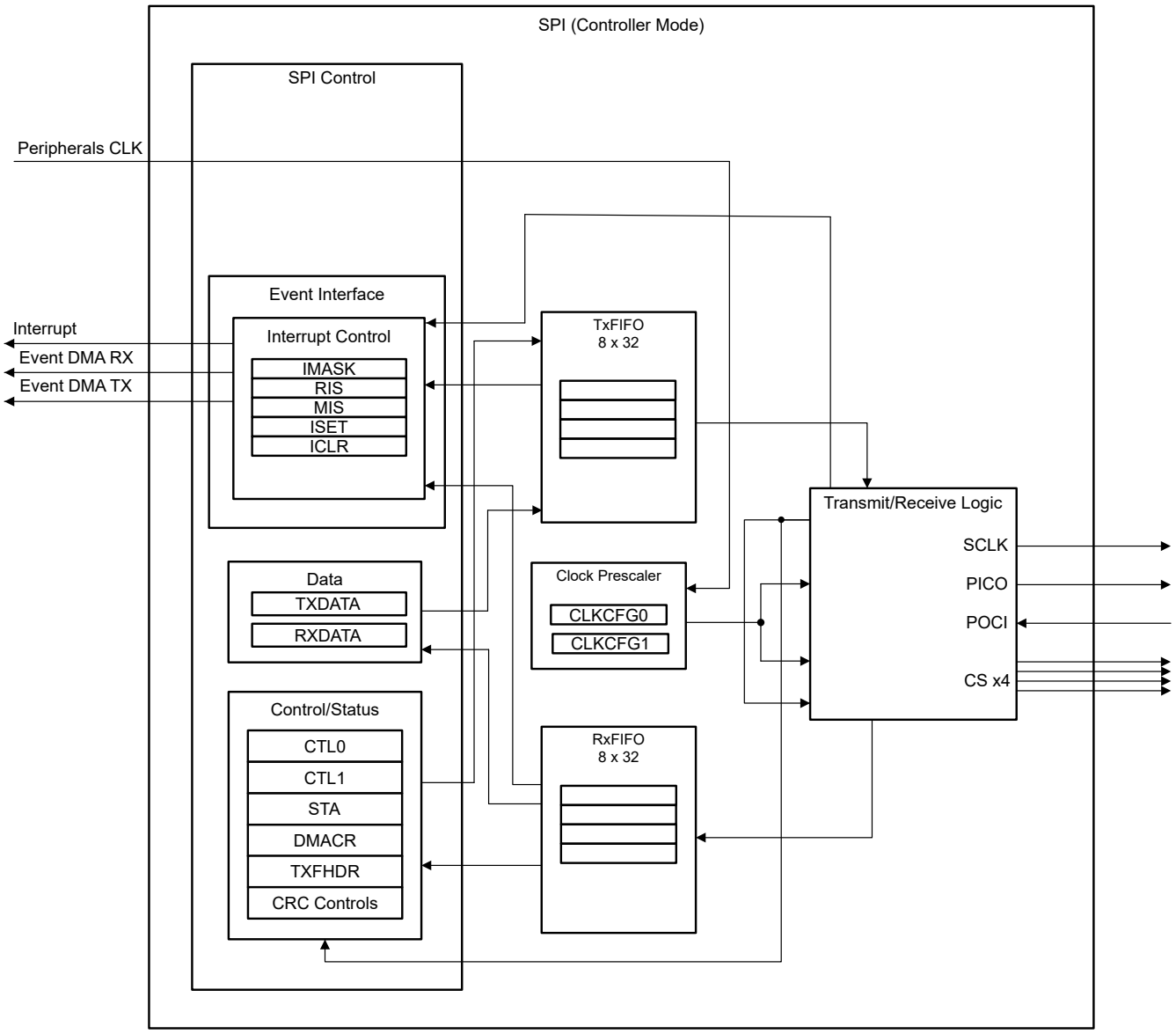


Figure 18-1. SPI Block Diagram

18.2 Signal Description

Table 18-1 lists the external SPI signals and describes the function of each. The SPI signals are selected in the IOC module through the IOCFGn registers. For more information on configuration of GPIOs, see Chapter 16.

Table 18-1. SPI Signal Description

Signal Name	Pin Number	Description
SCLK	Assigned in I/O controller	**SPI Clock** Controller Mode: SCLK is an output Peripheral Mode: SCLK is an input
CS		**SPI Chip Select** Controller Mode: CS is an output (4 CS available for 4 different peripherals) Peripheral Mode: CS is an input
PICO		**Peripheral In, Controller Out** Controller mode: PICO is the data output line Peripheral mode: PICO is the data input line
POCI		**Peripheral Out, Controller In** Controller mode: POCI is the data input line Peripheral mode: POCI is the data output line

18.3 Functional Description

SPI performs serial-to-parallel conversion on data received from a peripheral device. The CPU accesses data, control, and status information. Internal FIFO memories buffer the transmit and receive paths, allowing independent storage of up to eight 16-bit values in both transmit and receive modes. The SPI also supports the Host DMA interface. The TX and RX FIFOs can be programmed as destination or source addresses in the Host DMA module. The Host DMA operation is enabled by setting the appropriate bits in the SPI:DMACR register. The SPI module also includes a CRC engine that can be used for data checking during SPI transmission. If SPI is not being used, this can act as a general-purpose CRC engine. Additional capability is added to enable the SPI module to be used efficiently with an external controller in a transceiver setup by allowing atomic operations to update header information in the FIFO, including atomic FIFO pointers' reset capability.

18.3.1 Clock Control

The SPI includes a programmable bit rate clock divider and prescaler to generate the serial output clock.

The serial bit rate is derived by dividing down the input clock, SOC CLK (80MHz).

First, the clock is divided by a prescaler with a value from 1 to 8, which is programmed in the SPI.CLKCFG0[2:0] PRESC field (a value of 0x1 means that the clock is divided by 2). The clock is further divided by a value from 2 to 2048, which is 2×(1 + SCR), where SCR is the value programmed in the SPI.CLKCFG1[9:0] SCR field.

Equation 7 defines the frequency of the output clock SCLK.

$$\frac{SOC\ CLK}{(1 + PRESC) \times (2 \times (1 + SCR))} \quad (7)$$

Note

For both peripheral and controller modes, the core clock (SOC CLK) must be at least two times faster than SCLK.

The maximum SPI frequency supported with controller and peripheral modes depends on the device clock option and IO option. Please refer to the specific data sheet specification for more information.

18.3.2 FIFO Operation

18.3.2.1 Transmit FIFO

The common TX FIFO is a 16-bit wide, 16 location deep, first-in first-out memory buffer given the selected SPI data frame size is greater than 8 bits. The organization of this FIFO is modified dynamically if the selected SPI

data frame size is greater than 8 bits, the common TX FIFO is a 16-bit wide, 8 location deep, first-in first-out memory buffer. The CPU writes data to the FIFO via the SPI.TXDATA register and data is stored in the FIFO until the data is read out by the transmission logic.

When configured as a controller (or a peripheral), parallel data is written into the TX FIFO before serial conversion and transmission to the attached peripheral (or controller) through the PICO (or POCI) pin.

In peripheral mode, the SPI transmits data each time the controller initiates a transaction. If the TX FIFO is empty and the controller initiates a transaction, the peripheral will transmit garbage data. User or software is responsible for making valid data available in the FIFO as needed. The SPI can be configured to generate an interrupt when a configurable level within the FIFO is selected via SPI:IFLS, or a Host DMA request when the FIFO is not FULL.

18.3.2.2 Repeated Transmit Operation

Using the SPI.CTL1[23:16] REPTX bit field, the last data frame transmitted can be repeated as many times as configured within the field. The SPI transfer can be started by writing data once into the TX FIFO. This feature then transmits the same data repeatedly as if the data were written into the TXFIFO [SPI.CTL1[23:16] REPTX bit field] a number of times. The repeated transfer operation can be used to clean a transfer or to pull a certain amount of data from a peripheral. A value of 0 in the SPI.CTL1[23:16] REPTX bit field disables this mode. This function is only available in controller mode.

When repeated transmit is used, the function needs to be aligned with the data in the FIFO. The following sequence is used when setting up the repeated transmit operation:

- Check and wait till FIFO is empty
- Setup REPTX
- Write to TXDATA / TXFIFO
- Wait till requested data has been received

18.3.2.3 Receive FIFO

If the selected SPI data frame size is greater than 8 bits, the common RX FIFO is a 16-bit wide, 16 location deep, first-in first-out memory buffer. The organization of this FIFO is modified dynamically if the selected data size is less than or equal to 8 bits, and for better FIFO utilization behaves as an 8-bit wide, 32 locations deep FIFO. Received data from the serial interface is stored in the buffer until read out by the CPU, which accesses the read FIFO by reading the SPI.RXDATA register.

When configured as a controller (or peripheral), serial data received through the POCI (or PICO) pin is registered prior to parallel loading into the RX FIFO.

18.3.2.4 FIFO Flush

SPI includes a feature to reset the TX and RX FIFO pointers to flush FIFOs. This must be triggered when no SPI transactions are in progress. If a FIFO flush is triggered when a transaction is in progress, then a second FIFO flush is needed when no operations are ongoing, before restarting new SPI transfers.

The FIFO flush operation is atomic. When CPU writes into SPI.CTL0[11] FIFORST register bit, the SPI hardware internally ensures that TX and RX FIFO pointers are set to zero, and auto-clears the FIFORST bit after 4 SOC CLK clock cycles. CPU can poll the FIFORST bit to identify when the FIFO pointer reset operation has completed.

Note

FIFO pointers also get reset when SPI is disabled after the SPI.CTL1[0] EN bit toggles from 0x1 to 0x0.

18.3.3 Interrupts

The SPI can generate interrupts when the following conditions are observed:

- DMATX

- DMARX
- IDLE
- TXEMPTY
- TX
- RX
- RTOUT
- PEN
- RXOVF

All interrupt events are ORed together before being sent to the event manager, thus the SPI generates a single interrupt request regardless of the number of active interrupts. The interrupt conditions listed above can be masked by setting the appropriate bit in the SPI.IMASK register. Setting the appropriate mask bit in the SPI.IMASK register enables the interrupt. SPI.IMSET and SPI.IMCLR are alias registers which can be used to set and clear individual bits of SPI:IMASK register.

The status of the individual interrupt sources can be read from the SPI Raw Interrupt Status register (SPI.RIS) and the SPI Masked Interrupt Status register (SPI.MIS). SPI.ICLR can be used to clear interrupt flags within RIS and MIS. SPI.ISET can be used to set these interrupt flags for debug or test purposes.

The transmit FIFO service interrupt request SPI.RIS[4] TX bit is not gated with the SPI enable signal, which allows data to be written to the transmit FIFO before enabling the SPI by an interrupt service routine (ISR).

Note

TX and RX FIFO interrupts are best serviced by Host DMA rather than CPU. In case CPU services TX and RX FIFO interrupts, TXEMPTY and RXOVF can be configured as well, so that if the FIFO interrupt is missed by the CPU in corner cases, these act as a fail-safe.

The receive FIFO overflow interrupt SPI.RIS[0] RXOVF is asserted when the FIFO is already full and an additional data frame is received, causing an overflow of the FIFO. Data is overwritten in the receive shift register, but not in the FIFO.

The parity error interrupt SPI.RIS[1] PER bit is set when a parity error is detected. SPI.CTL1[5] PEN bit can be written to enable the parity check, where the last bit received is used as parity to test the integrity of the previous bits. SPI.CTL1[7] PBS bit selects the parity mode as even or odd. When a parity fault is detected, the interrupt flag SPI.RIS[1] PER bit is set (to mark the data as invalid).

The idle interrupt SPI.RIS[6] IDLE is set when the SPI transmission has concluded and SPI module moves back to idle mode. This is set when SPI.STA[4] BUSY goes low.

The SPI Receive Timeout interrupt is set when SPI is in peripheral mode and has not been receiving data for the number of functional clock cycles (SOC CLK) configured within SPI.CTL1[29:24] RTOUT bit field. A value of 0 disables this function. The countdown is started when SPI is in the peripheral mode and the first SCLK positive edge is detected and the countdown is restarted on each subsequent SCLK positive edge. A timeout error is asserted if the count reaches zero before the next SCLK toggles.

18.3.4 Data Format

Each data frame is between 4 and 16 bits long, depending on the size of the data programmed. The control bit SPI.CTL1[4] MSB field can be programmed to define the direction of the data input and output as mostsignificant-bit (MSB) or least-significant-bit (LSB) first. If parity is enabled, the parity bit is always received as the last bit.

With SPI.CTL0[3:0] DSS bit field, the bit length per transfer is defined between 4 – 16 bits for controller mode and 7 – 16 bits for peripheral mode.

18.3.5 Delayed Data Sampling

In cases when the input data arrives at the POCI pin with additional delay due to run-time conditions or path delays, on the following input data sampling stage, the previous data can be sampled at the sampling

clock edge. To compensate for this, sampling of input data in controller mode can be delayed using the SPI.CLKCFG1[19:16] DSAMPLE bit field. The delayed sampling is only available in controller mode. The delay can be adjusted in steps of undivided SPI input clocks (SOC CLK) programmed within the SPI.CLKCFG1[19:16] DSAMPLE bit field. The range of values of DSAMPLE is 0 to SCR+1. Typically, values of 1 and 2 are sufficient even for the highest supported SPI frequencies.

18.3.6 Chip Select Control

SPI can be configured to controller mode by setting the SPI.CTL1[2] MS bit to 1, and to peripheral mode by clearing the SPI.CTL1[2] MS bit.

The chip select signal needs to be provided by the controller in Motorola 4-wire mode.

Regardless of the configuration of PHA or POL, SPI includes a feature to keep the CS active low until all data has been transferred from TXFIFO in controller mode and Motorola 4-wire frame format. This feature is enabled by the SPI.CTL0[10] HWCSN bit. If SPI.CTL0[14] AUTOCRC is set, then CS is kept low until the CRC has been transferred as well.

In peripheral mode, the clock is provided by the controller and used by the SPI to capture the data. The peripheral has the option to operate in 3-wire or 4-wire mode. 4-wire mode only accepts data transfers if the CS is activated.

When SPI is in peripheral mode and the SPI.CTL0[12] CSCLR bit is set, the receive shift register is cleared automatically when CS goes to inactive state.

18.3.7 Command Data Control

When using the Motorola 3-wire frame format with the SPI.CTL0[3:0] DSS bit field programmed for 8 bits, the SPI.CTL1[11] CDEN bit can be set to use the CS line as a signal to distinguish between Command and Data information. This is often used for LCD or data storage devices.

- CS level low: command function
- CS level high: data function

The SPI.CTL1[15:12] CDMODE bit field can be written with a value of 1-14 to specify the number of bytes the CS line is set low for, starting with the next value to be transmitted. After the number of bytes are transmitted, CS is set high automatically. If a value of 0xF is set, CS stays low permanently. A value of 0 sets the CS line to high immediately after the current data byte has been transmitted.

This option is only available in controller mode. The SPI.CTL1[11] CDEN bit can only be updated when the SPI module is disabled. SPI.CTL1[15:12] CDMODE can be updated between the different data packages. The counter is reset with CDEN or SPI ENABLE set to disabled. Before setting a new value in CTL1.CDMODE, check that the FIFO is empty and that SPI is in IDLE state (SPI.STA[4] BUSY bit is cleared to 0).

When writing a new value into the SPI.CTL1[15:12] CDMODE bit field, the internal counter is reset and the new value is used for counting. If the counter counts down to 0 and another command package is sent, the CDMODE needs to be set again. Otherwise the next frames are sent as data with the CS pin signaling data mode.

18.3.8 Protocol Descriptions

The protocol format mode can be selected by using the SPI.CTL0[6:5] FRF bit field. The supported options include Motorola 3-wire, Motorola 4-wire, Texas Instruments Synchronous and MICROWIRE.

18.3.8.1 Motorola SPI Frame Format

The Motorola SPI is a 4-wire interface where the CS signal behaves as a peripheral select. In the 3-wire mode the CS signal is not required and the module behaves as if always selected. The main feature of the Motorola SPI format is that the inactive state and phase of the SCLK signal can be programmed through the SPO and SPH bits in the SPI.CTL0 control register.

SPO Clock Polarity Bit

If the SPI.CTL0[8] SPO clock polarity control bit is cleared, the SCLK pin outputs a steady-state low value when data is not being transferred. If the SPI.CTL0[8] SPO bit is set, the SCLK pin outputs a steady-state high value when data is not being transferred.

SPH Phase-Control Bit

The SPI.CTL0[9] SPH phase-control bit selects the clock edge that captures data. The state of this bit has the most impact on the first bit transmitted, by either allowing or not allowing a clock transition before the first data capture edge. If the SPI.CTL0[9] SPH phase-control bit is cleared, data is captured on the first clock edge transition. If the SPH bit is set, data is captured on the second clock edge transition.

Note

For all combinations of SPO and SPH, the minimum CS inactive period (where CS is held high) must be at least one SCLK period wide.

Motorola SPI Frame Format with SPO = 0 and SPH = 0

Figure 18-2 shows signal sequences for Motorola SPI format with SPO = 0 and SPH = 0.

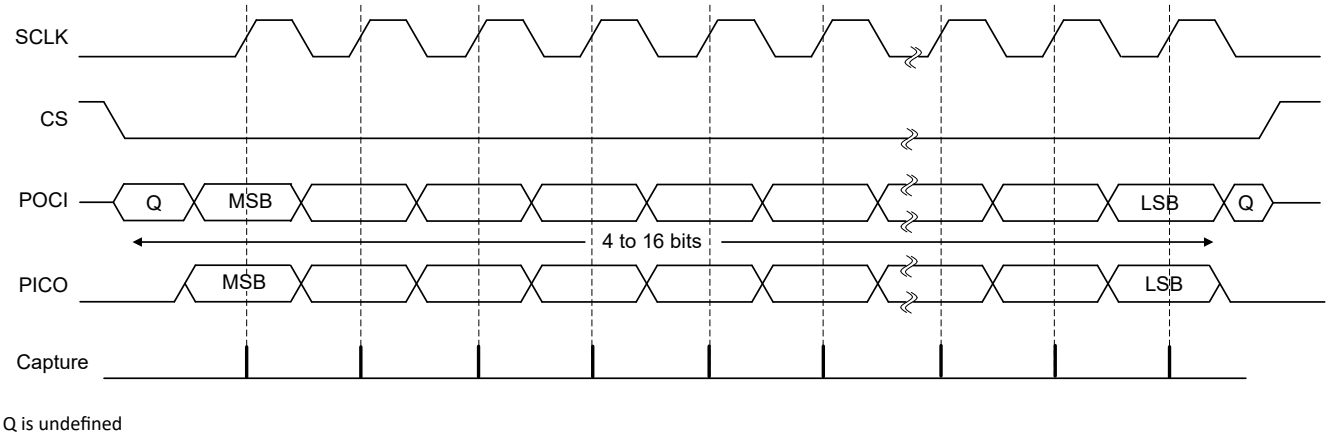


Figure 18-2. Motorola SPI Frame Format with SPO=0 and SPH=0

In this configuration, the following occurs during idle periods:

- SCLK is forced low
- CS is forced high
- The transmit data line PICO is forced low
- When the SPI is configured as a controller, the SCLK pin is enabled
- When the SPI is configured as a peripheral, the SCLK pin is disabled

If the SPI is enabled and valid data is in the TX FIFO, the CS controller signal is driven low at the start of transmission which causes enabling of peripheral data onto the POCI input line of the controller. The controller PICO output pin is enabled.

One-half SCLK period later, valid controller data is transferred to the PICO pin. Once both the controller and peripheral data is set, the SCLK controller clock pin goes high after an additional one-half SCLK period. The data is now captured on the rising edges and propagated on the falling edges of the SCLK signal.

For a single-word transmission after all bits of the data frame are transferred, the CS line is returned to the IDLE high state one SCLK period after the last bit is captured. For continuous back-to-back transmissions, the CS signal must pulse high between each data word transfer because the peripheral-select pin freezes the data in the serial peripheral register and does not allow altering of the data if the SPH bit is clear. The controller device must raise the CS pin of the peripheral device between each data transfer to enable the serial peripheral data write. SPI.CTL0[10] HWCSN described in Section 18.3.6 can be used to override this behavior. When the

continuous transfer completes, the CS pin is returned to the IDLE state one SCLK period after the last bit is captured.

Motorola SPI Frame Format with SPO = 0 and SPH = 1

Figure 18-3 shows the signal sequence for Motorola SPI format with SPO = 0 and SPH = 1.

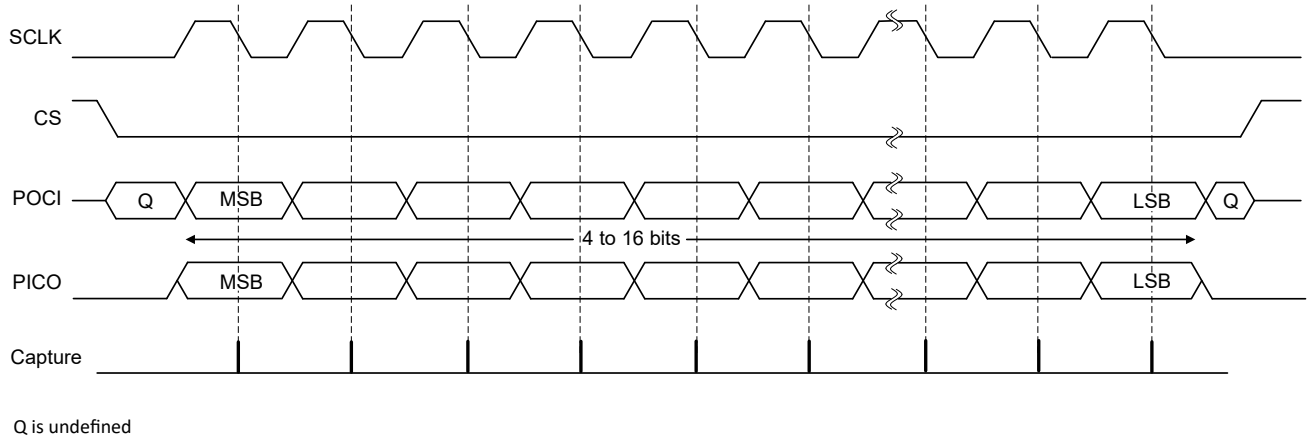


Figure 18-3. Motorola SPI Frame Format with SPO=0 and SPH=1

If the SPI is enabled and valid data is in the TX FIFO, the CS controller signal goes low at the start of transmission. The controller PICO output is enabled. After an additional one-half SCLK period, both controller and peripheral valid data are enabled onto their respective transmission lines. At the same time, SCLK is enabled with a rising-edge transition. Data is then captured on the falling edges and propagated on the rising edges of the SCLK signal.

For a single-word transfer, after all bits are transferred, the CS line is returned to the IDLE high state one SCLK period after the last bit is captured. For continuous back-to-back transfers, the CS pin is held low between successive data words and terminates like a single-word transfer.

Motorola SPI Frame Format with SPO = 1 and SPH = 0

Figure 18-4 shows signal sequences for Motorola SPI format with SPO = 1 and SPH = 0.

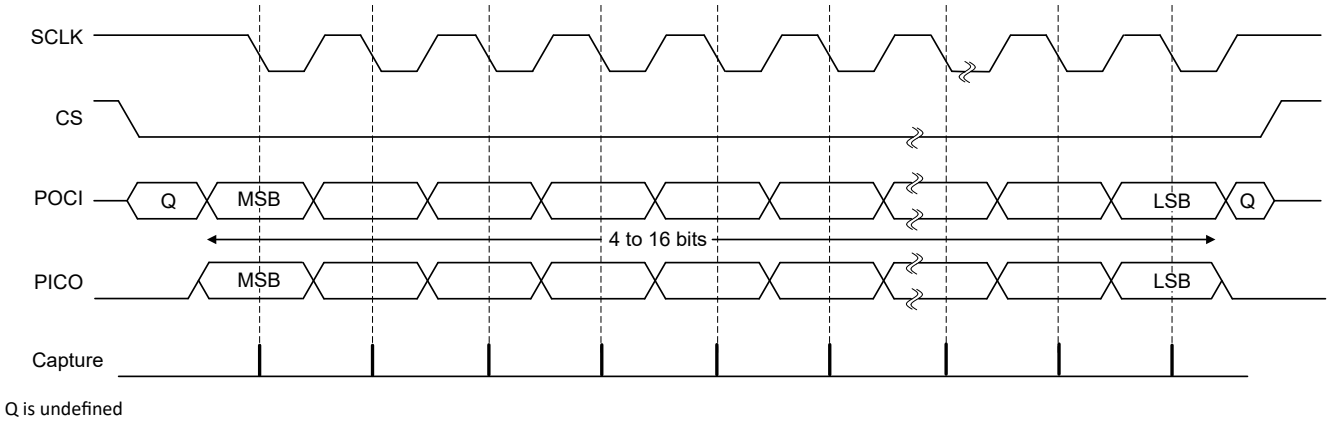


Figure 18-4. Motorola SPI Frame Format with SPO=1 and SPH=0

In this configuration, the following occurs during idle periods:

- SCLK is forced high
- CS is forced high
- The transmit data line PICO is forced low

- When the SPI is configured as a controller, the SCLK pin is enabled
- When the SPI is configured as a peripheral, the SCLK pin is disabled

If the SPI is enabled and valid data is in the TX FIFO, the SPI CS controller signal goes low at the start of transmission and transfers peripheral data onto the POCI line of the controller immediately. The controller PICO output pin is enabled.

One-half SCLK period later, valid controller data is transferred to the PICO line. When both the controller and peripheral data have been set, the SCLK controller clock pin becomes low after one additional half SCLK period. Data is captured on the falling edges and propagated on the rising edges of the SCLK signal.

For a single-word transmission after all bits of the data word are transferred, the CS line is returned to the IDLE high state one SCLK period after the last bit is captured. For continuous back-to-back transmissions, the CS signal must pulse high between each data word transfer as the peripheral-select pin freezes the data in the serial peripheral register and keeps it from being altered if the SPH bit is clear. The controller device must raise the CS pin of the peripheral device between each data transfer to enable the serial peripheral data write. SPI.CTL0[10] HWCSN described in Section 18.3.6 can be used to override this behavior. When the continuous transfer completes, the CS pin returns to its IDLE state one SCLK period after the last bit is captured.

Motorola SPI Frame Format with SPO = 1 and SPH = 1

Figure 18-5 shows the signal sequence for Motorola SPI format with SPO = 1 and SPH = 1.

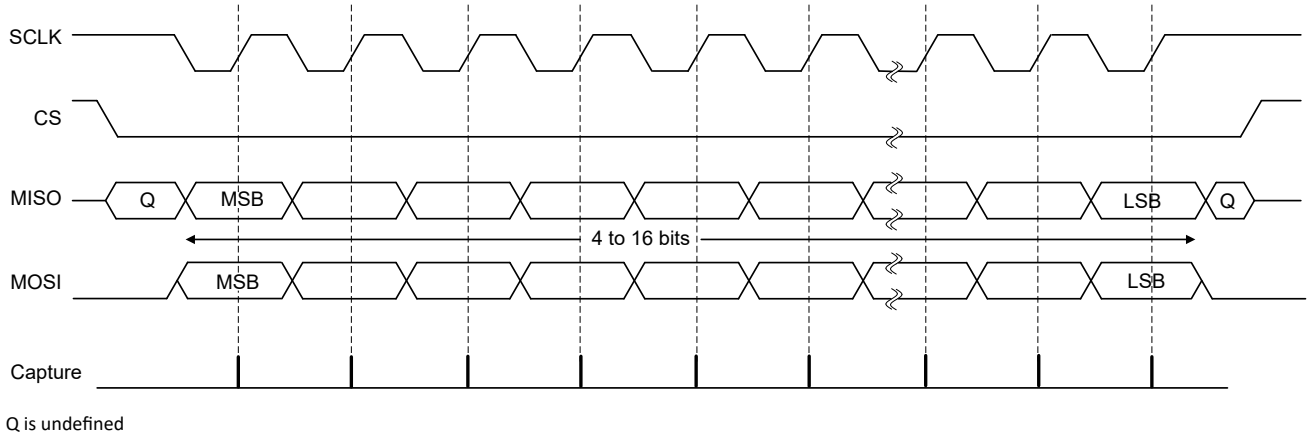


Figure 18-5. Motorola SPI Frame Format with SPO=1 and SPH=1

In this configuration, the following occurs during idle periods:

- SCLK is forced high
- CS is forced high
- The transmit data line PICO is forced low
- When the SPI is configured as a controller, the SCLK pin is enabled
- When the SPI is configured as a peripheral, the SCLK pin is disabled

If the SPI is enabled and valid data is in the TX FIFO, the start of transmission is signified by the CS controller signal going low. The controller PICO output pin is enabled. After an additional one-half SCLK period, both controller and peripheral data are enabled onto their respective transmission lines. At the same time, SCLK is enabled with a falling-edge transition. Data is then captured on the rising edges and propagated on the falling edges of the SCLK signal.

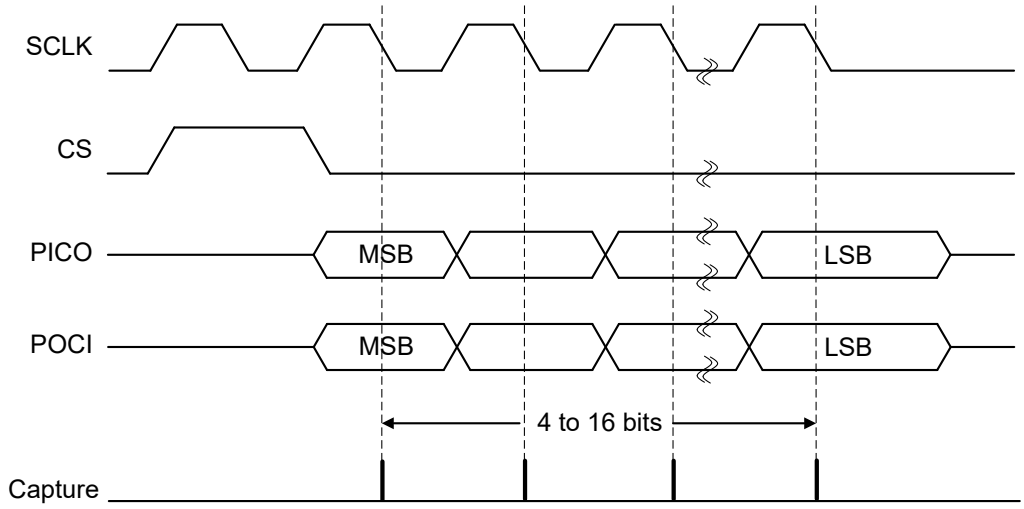
For a single word transmission, after all bits are transferred, the CS line returns to its IDLE high state one SCLK period after the last bit is captured. For continuous back-to-back transmissions, the CS pin remains in its active low state until the final bit of the last word is captured and then returns to its IDLE state. For continuous back-to-back transfers, the CS pin is held low between successive data words and terminates like a single-word transfer.

The serial clock (SCLK) is held inactive while the SPI is idle and SCLK transitions at the programmed frequency only during active transmission or reception of data. The IDLE state of SCLK provides a receive timeout indication that occurs when the RX FIFO still contains data after a timeout period.

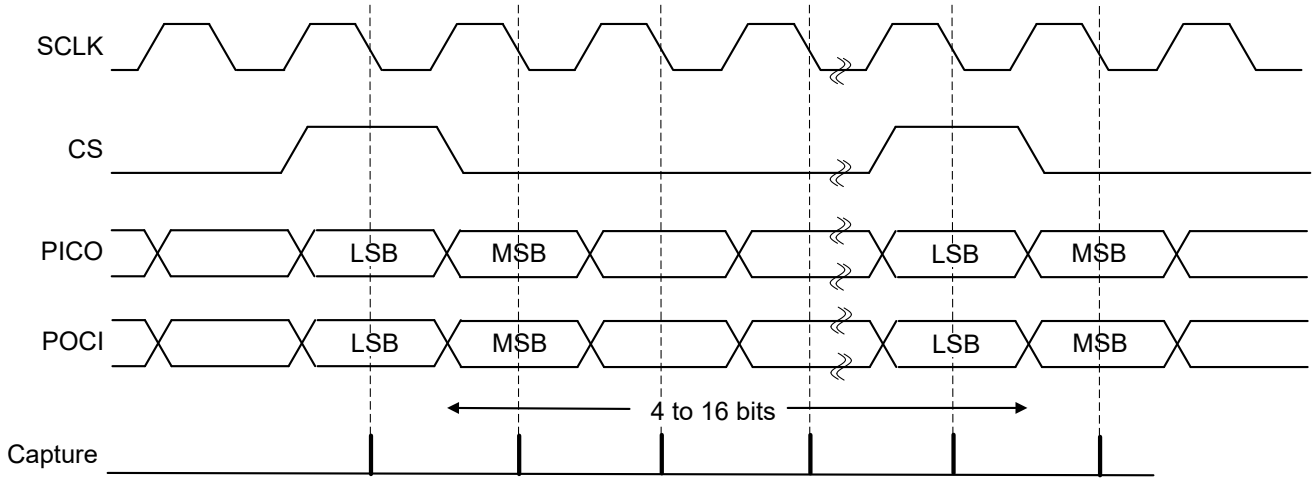
18.3.8.2 Texas Instruments Synchronous Serial Frame Format

The SPI module is compatible with Texas Instruments Synchronous Serial frame format.

Figure 18-6 shows the TI synchronous serial frame format for a single and continuous transmitted frame.



Single Transmission Signal Sequences



Continuous Transmission Signal Sequences

Figure 18-6. TI Synchronous Serial Frame Format

SCLK and CS are forced low and the transmit data line PICO is put in tristate whenever the SPI is idle. When the TX FIFO contains data, CS is pulsed high for one SCLK period. The transmitted value is also transferred from the TX FIFO to the serial shift register of the transmit logic. On the next rising edge of SCLK, the MSB of the 4- to 16-bit data frame is shifted out on the PICO pin. Likewise, the MSB of the received data is shifted onto the POCI pin by the off-chip serial peripheral device. Both the SPI and the off-chip serial peripheral device then

clock each data bit into their serial shifter on each falling edge of SCLK. The received data is transferred from the serial shifter to the RX FIFO on the first rising edge of SCLK after the least significant bit (LSB) is latched.

The serial clock (SCLK) is held inactive while the SPI is idle and SCLK transitions at the programmed frequency only during active transmission or reception of data. The IDLE state of SCLK provides a receive time-out indication that occurs when the RX FIFO still contains data after a time-out period.

18.3.8.3 MICROWIRE Frame Format

Figure 18-7 shows the MICROWIRE frame format for a single frame. Figure 18-8 shows the same format when back-to-back frames are transmitted.

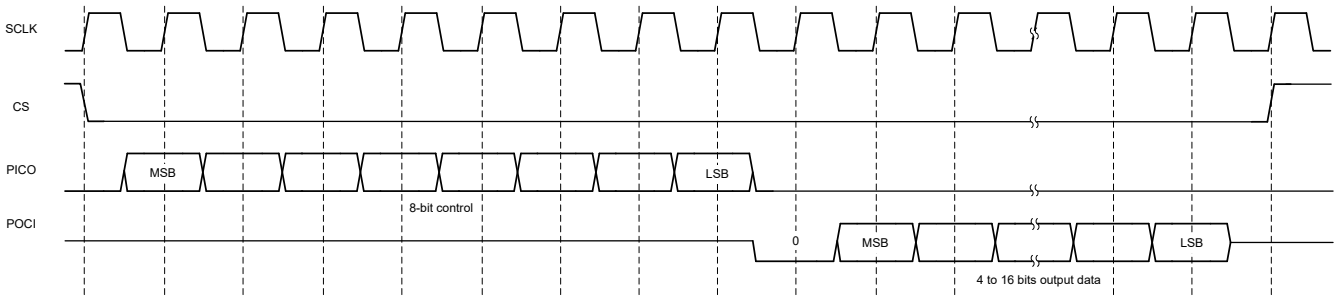


Figure 18-7. MICROWIARE Frame Format (Single Frame)

MICROWIRE format is similar to SPI format, except that transmission is half-duplex and uses a controllerperipheral message passing technique. Each serial transmission begins with an 8-bit control word that is transmitted from the SPI to the off-chip peripheral device. During this transmission, the SPI does not receive incoming data. After the message is sent, the off-chip peripheral decodes the message and waits one serial clock after the last bit of the 8-bit control message is sent. The off-chip peripheral then responds with the required data. The returned data is 4 to 16 bits long, making the total frame length anywhere from 13 to 25 bits.

In this configuration, the following occurs during idle periods:

- SCLK is forced low
- CS is forced high
- The transmit data line, PICO, is typically forced low

Writing a control byte to the TX FIFO triggers a transmission. The falling edge of CS transfers the value of the TX FIFO to the serial shift register of the transmit logic and shifts the MSB of the 8-bit control frame out onto the PICO pin. CS remains low for the duration of the frame transmission. The POCI pin remains in the tri-state condition during this transmission.

The off-chip serial peripheral device latches each control bit into the serial shifter on each rising edge of SCLK. After the last bit is latched by the peripheral device, the control byte is decoded during a one clock wait state and the peripheral responds by transmitting data back to the SPI. Each bit is driven onto the POCI line on the falling edge of SCLK. The SPI latches each bit on the rising edge of SCLK. At the end of the frame for single transfers, the CS signal is pulled high one clock period after the last bit is latched in the receive serial shifter transferring the data to the RX FIFO.

Note

The off-chip peripheral device can place the receive line in a tri-state condition either on the falling edge of SCLK (after the LSB has been latched by the receive shifter), or when the CS pin goes high.

For continuous transfers, data transmission begins and ends like a single transfer, but the CS line is held low and data transmits back-to-back. The control byte of the next frame follows the LSB of the received data from the current frame. After the LSB of the frame is latched into the SPI, each received value is transferred from the receive shifter on the falling edge of SCLK.

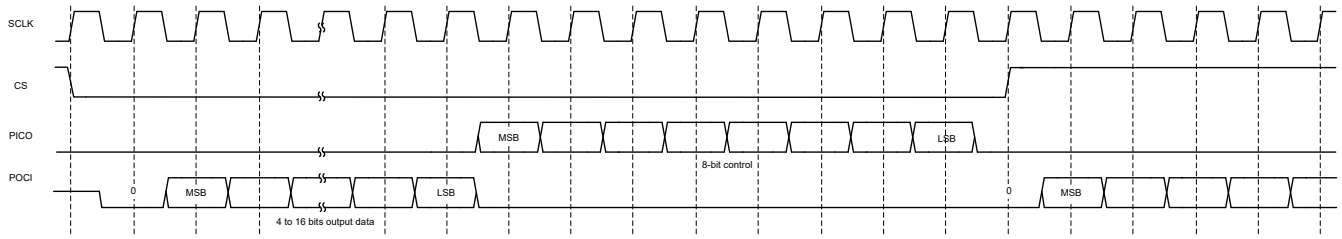


Figure 18-8. MICROWIRE Frame Format (Continuous Transfer)

In the MICROWIRE mode, the SPI peripheral samples the first bit of receive data on the rising edge of SCLK after CS has gone low. Controllers driving a free-running SCLK must ensure that the CS signal has sufficient setup and hold margins with respect to the rising edge of SCLK.

18.3.9 CRC Configuration

- CRC8-CCITT and CRC16-CCITT schemes are implemented in the SPI module independently for transmit and receive operations.
- CRC functionality shall be enabled by application when SPI frame size is only 8-bits or 16-bits.
- This is a software guideline and no specific check is done in hardware based on frame size configuration.
- For 8-bit transfers, CRC8 or CRC16 schemes can be selected by application.
- For 16-bit transfers, CRC16 scheme has to be selected.
- The CRC on TX and RX paths are always active and there is no need to enable CRC functionality explicitly in software.

Transmitter side operation (CRC8/CR16) :

- The TX CRC block is logically located between the SPI.TXDATA register and TXFIFO in the design.
- Select CRC polynomial (8 or 16) based on SPI data frame size (selection applies to both TX and RX CRC units).
- TX side CRC state register resets to the seed value of 0xFF or 0xFFFF.
- When the bus controller (CPU or µDMA) writes data into SPI.TXDATA register, the data is written into the TXFIFO and at the same time used to update the SPI.TXCRC register by hardware logic.
- Data from TXFIFO gets loaded into shift register and transmitted out.
- After the required amount of data has been written into SPI.TXDATA register, the software has to read the SPI.TXCRC state register.
- Software must write the obtained CRC checksum into the SPI.TXDATA register for transmission.
- Initialize SPI.TXCRC state register and repeat this sequence for every block of SPI data transmission.

Receiver side operation (CRC8/CRC16) :

- The RX CRC block is logically located between RXDATA and RXFIFO in the design.
- Select CRC polynomial (8 or 16) based on the SPI data frame size (selection applies to both TX and RX CRC units).
- The RX side CRC state register resets to the seed value of 0xFF or 0xFFFF.
- Data is received into shift register and gets loaded into RXFIFO during receive operation.
- When the bus controller (CPU or µDMA) reads data from the SPI.RXDATA register, the data is returned from RXFIFO and at the same time used to update the SPI.RXCRC state register by hardware logic.
- After the required amount of data have been read from SPI.RXDATA, software can either:
  - Read out the received checksum and then check the SPI.RXCRC state which is zero if there are no errors
  - Read out the SPI.RXCRC state and then read out the checksum through SPI.RXDATA and compare the two values
- Initialize SPI.RXCRC state register and repeat this sequence for every block of SPI data reception.

In case SPI functionality is not being used, the CRC engine can be used as a general-purpose CRC generator.

CTL0.GPCRCEN register bit can be set to enable this functionality. The transmit side CRC can then be used by application software when SPI enable is zero.

18.3.10 Auto CRC Functionality

The SPI includes a feature to automatically insert CRC when the TX FIFO underflows. This feature can be enabled by the SPI.CTL0[14] AUTOCRC bit.

When this bit is set, SPI module loads the calculated CRC checksum into the TX FIFO after all bytes are transmitted when TXFIFO underflow is signaled. This causes the CRC to be transmitted out automatically at the end of the data block.

There is no need for software to read and load this CRC value into the FIFO via a TXDATA register write.

Software must read the SPI.TXCRC[31] AUTOINS bit to reinitialize the TX CRC engine to a seed of all ones after the transfer of data and CRC is done.

Similarly, after reading all the received data via SPI.RXDATA register, software must read the SPI.RXCRC register to obtain the CRC value and auto-initialize the RX CRC engine to a seed value of all ones.

Note

Care must be taken to ensure that the TXFIFO does not empty and signal an underflow if FIFO filling and SPI transmission are occurring in parallel. This can lead to a CRC being automatically inserted at an unwanted instant. When operating at SPI rates 8 MHz or higher, it is advisable to ensure that the TXFIFO is loaded with all the required data (or at least two data frames) before enabling SPI transfers with Auto CRC enabled.

Note

In MICROWIRE frame format, the AUTOCRC feature only supports CRC8 configuration in controller mode.

18.3.11 SPI Status

The external controller is supposed to always send the number of clocks equal to the DSS value written, before de-asserting CS and ending transmission. In case CS is deactivated before the entire data frame has been sent out by the peripheral, then CSD error bit is set and can be read within SPI.STA[5] CSD. This bit, once set, must be cleared by software.

The TX FIFO full level indicating the number of entries written into the TXFIFO can be read out via the SPI.STA[13:8] TXFIFOLVL bit field.

Additional status bits related to peripheral mode transfer complete, SPI busy indication, TX and RX FIFO flags can be read out from the SPI.STA register. The peripheral mode transfer complete indication bit, once set, must be cleared by software.

18.3.12 Debug Halt

Debug halt is available in the SPI module and is controlled by the SPI.EMU register. When the SPI.EMU[0] HALT bit is set to 1, the SPI module freezes operations as described below.

- If SPI is configured in Controller mode, then debug halt freezes SPI operations at the next DSS boundary.
- If SPI is configured in Peripheral mode, then debug halt freezes SPI operations immediately.
- FIFO pointers are not incremented if RXDATA read is attempted during debug halt.

18.4 Host DMA Operation

The SPI module provides an interface to the Host DMA controller with separate channels for transmit and receive. The SPI DMA Control register (SPI.DMACR) allows the µDMA to operate with the SPI. When Host DMA operation is enabled, the SPI asserts a Host DMA request on the receive or transmit channel when the

associated FIFO can transfer data. For the receive channel, a single transfer request is asserted whenever any data is in the RX FIFO. Whenever data in the RX FIFO reaches the configured level set in the SPI.IFLS[10:8] RXSEL bit field, a burst transfer request is asserted. The supported settings for RX FIFO are: ¼, ½ (default), ¾, full, and at least one location is available in the FIFO. For the transmit channel, a single transfer request is asserted whenever at least one empty location is in the TX FIFO. Whenever the TX FIFO reaches the configured level set via SPI.IFLS[2:0] TXSEL, the burst request is asserted. The supported settings for TX FIFO are: ¼, ½ (default), ¾, empty, at least one location is available in the FIFO. The Host DMA controller handles the single and burst Host DMA transfer requests automatically depending on how the Host DMA channel is configured.

Note

Software must avoid ¾ threshold selection for Host DMA operation.

To enable Host DMA operation for the receive channel, set the SPI.DMACR[0] RXEN bit. To enable Host DMA operation for the transmit channel, set the SPI.DMACR[8] TXEN register bit. If the Host DMA is enabled and appropriate bits are cleared in the DMA Done Mask register (DMA.DONEMASK) the Host DMA controller triggers an interrupt when a transfer completes. This interrupt can be chosen as one of the sources of the combined SPI interrupt. If interrupts are used for SPI operation and the Host DMA is enabled, the SPI interrupt handler must be designed to handle the Host DMA completion interrupt. The status of TX and RX DMA done interrupts can be read from the Channel Request Done register (DMA.REQDONE). They can also be read from SPI.RIS[8] DMATX bit and the SPI.RIS[7] DMARX bit. For clearing the TX and RX DMA done interrupts, the corresponding bits in the DMA.REQDONE register must be set to 1.

For more details about programming the Host DMA controller, see Chapter 11.

18.5 Initialization and Configuration

The following describes the necessary steps to enable and initialize the SPI.

TI recommends using the SPI driver in the SimpleLink™ CC35xx Software Development Kit (SDK) when using the SPI.

1. Ensure the power domain is powered up properly.
2. Enable the SPI module clock in CLKCTL by setting the CLKCTL.CLKCFG0[10] SPI0 bit.
3. Configure the IO Mux module to route the PICO, POCI, CS, and SCLK functionality from I/Os to the SPI module. IOCFGn.PORTCFG must be written to the correct IDs.

For each of the frame formats, the SPI is configured using the following steps:

1. Make sure that the SPI.CTL1[0] ENABLE bit is cleared before making any configuration changes
2. Configure the clock pre-scaler divisor by writing to the SPI.CLKCFG0[2:0] PRESC and SPI.CLKCFG1[9:0] SCR bit fields
3. Write the SPI.CTL0 register with the following configuration:
   a. Desired clock phase and polarity, if using Motorola™ SPI mode (SPH and SPO)
   b. The protocol mode: Motorola SPI (4-wire or 3-wire) , TI SSF, MICROWIRE (FRF)
   c. The data size (DSS)
4. Select whether the SPI is a controller or peripheral:
   a. For controller operations, SPI.CTL1[2] MS is 1
   b. For peripheral mode (output enabled), SPI.CTL1[2] MS bit is 0
   c. For peripheral mode (output disabled), clear the SPI.CTL1[2] MS bit to 0 and set the SPI.CTL1[3] POD bit to 1
5. Optionally, configure the Host DMA channel (see Chapter 11) and enable the Host DMA options in the SPI.DMACR register
6. Enable the SPI by setting the EN bit in the SPI.CTL1 register

As an example, assume that the SPI configuration is required to operate with the following parameters:

- Controller operation
- Texas Instruments Synchronous SPI mode
- 1-Mbps bit rate
- 8 data bits

Assuming the system clock is 80 MHz, the bit-rate calculation is shown in Equation 8

$$\frac{SOC\ CLK}{(1 + PRESC) \times (2 \times (1 + SCR))} \quad (8)$$

Example: 1000000 bps = 80000000 Hz / [(1+3) × (2 × (1 + 9))]

In this case, if PRESC = 0x3, SCR must be 0x09.

The configuration sequence is:

- Verify that the EN bit in the SPI.CTL1 register is cleared
- Write the SPI.CLKCFG0 register with a value of 0x00000003
- Write the SPI.CLKCFG1 register with a value of 0x00000009
- Write the SPI.CTL0 register with a value of 0x00000047
- Write the SPI.CTL1 register with a value of 0x00000004
- The SPI is then enabled by setting the EN bit in the SPI.CTL1 register

18.6 SPI Registers

Table 18-2 lists the memory-mapped registers for the SPI registers. All register offset addresses not listed in Table 18-2 should be considered as reserved locations and the register contents should not be modified.

Table 18-2. SPI Registers

Offset	Acronym	Register Name	Section
0h	DESC	Module Description	Section 18.6.1
44h	IMASK	Interrupt Mask	Section 18.6.2
48h	RIS	Interrupt Status Flags	Section 18.6.3
4Ch	MIS	Masked Interrupt Status	Section 18.6.4
50h	ISET	Interrupt Set	Section 18.6.5
54h	ICLR	Interrupt Clear	Section 18.6.6
58h	IMSET	Interrupt Mask Set	Section 18.6.7
5Ch	IMCLR	Interrupt Mask Clear	Section 18.6.8
60h	EMU	Emulation	Section 18.6.9
100h	CTL0	SPI Control Register	Section 18.6.10
104h	CTL1	SPI Control	Section 18.6.11
108h	CLKCFG0	Clock Prescaler Configuration	Section 18.6.12
10Ch	CLKCFG1	Serial Clock Configuration	Section 18.6.13
110h	IFLS	FIFO Trigger Levels	Section 18.6.14
114h	DMACR	DMA Control	Section 18.6.15
118h	RXCRC	Receive Cyclic Redundancy Check	Section 18.6.16
11Ch	TXCRC	Transmit CRC Value	Section 18.6.17
120h	TXFHDR32	Header Data	Section 18.6.18
124h	TXFHDR24	Header Data 24-bit	Section 18.6.19
128h	TXFHDR16	Transmit Header Update	Section 18.6.20
12Ch	TXFHDR8	Transmit Header Data	Section 18.6.21
130h	TXFHDRC	Header Control	Section 18.6.22
140h	RXDATA	Receive Data	Section 18.6.23
150h	TXDATA	Transmit Data	Section 18.6.24
160h	STA	Status Register	Section 18.6.25
1000h	CLKCFG	Clock Enable	Section 18.6.26

Complex bit access types are encoded to fit into small table cells. Table 18-3 shows the codes that are used for access types in this section.

Table 18-3. SPI Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

18.6.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 18-4.

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Description Register. This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 18-4. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	604Dh	Module identifier used to uniquely identify this IP.
15-12	STDIPOFF	R	1h	Standard IP MMR block offset. Standard IP MMRs are the set of from aggregated IRQ registers till DTB. 0: Standard IP MMRs do not exist 0x1-0xF: Standard IP MMRs begin at offset of (64*STDIPOFF from the base IP address)
11-8	INSTIDX	R	0h	IP Instance ID number. If multiple instances of IP exist in the device, this field can identify the instance number (0-15).
7-4	MAJREV	R	1h	Major revision of IP (0-15).
3-0	MINREV	R	0h	Minor revision of IP (0-15).

18.6.2 IMASK Register (Offset = 44h) [Reset = 00000000h]

IMASK is shown in Table 18-5.

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Interrupt mask. This register selects interrupt sources which are allowed to pass from [RIS.*] to [MIS.*] when the corresponding bit-fields are set to 1.

Table 18-5. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	DMATX	R/W	0h	DMA Done TX event mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
7	DMARX	R/W	0h	DMA Done RX event mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
6	IDLE	R/W	0h	SPI Idle event mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
5	TXEMPTY	R/W	0h	Transmit FIFO Empty event mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
4	TX	R/W	0h	Transmit FIFO event mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
3	RX	R/W	0h	Receive FIFO event. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
2	RTOUT	R/W	0h	SPI Receive Time-Out event mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
1	PER	R/W	0h	Parity error event mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
0	RXOVF	R/W	0h	RXFIFO overflow event mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask

18.6.3 RIS Register (Offset = 48h) [Reset = 00000000h]

RIS is shown in Table 18-6.

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Raw interrupt status. This register reflects the state of all pending interrupts, regardless of masking. This register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the corresponding [ICLR.*] register bit.

Table 18-6. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	DMATX	R	0h	DMA Done event for TX. This interrupt is set if the TX DMA channel sends the DONE signal. This allows the handling of the TX DMA event inside SPI. 0h = Interrupt did not occur 1h = Interrupt occurred
7	DMARX	R	0h	DMA Done event for RX. This interrupt is set if the RX DMA channel sends the DONE signal. This allows handling of the DMA RX event inside SPI. 0h = Interrupt did not occur 1h = Interrupt occurred
6	IDLE	R	0h	SPI has completed transfers and moved to IDLE mode. This bit is set when [STA.BUSY] goes low. 0h = Interrupt did not occur 1h = Interrupt occurred
5	TXEMPTY	R	0h	Transmit FIFO Empty interrupt mask. This interrupt is set when all data in the Transmit FIFO has been moved to the shift register. 0h = Interrupt did not occur 1h = Interrupt occurred
4	TX	R	0h	Transmit FIFO event.This interrupt is set if the selected Transmit FIFO level has been reached. 0h = Interrupt did not occur 1h = Interrupt occurred
3	RX	R	0h	Receive FIFO event.This interrupt is set if the selected Receive FIFO level has been reached 0h = Interrupt did not occur 1h = Interrupt occurred
2	RTOUT	R	0h	SPI Receive Time-Out event. This interrupt is set if no activity is detected on the input clock line within the time period dictated by RTOUT value. This is applicable only in peripheral mode. 0h = Interrupt did not occur 1h = Interrupt occurred
1	PER	R	0h	Parity error event. This bit is set if a Parity error has been detected 0h = Interrupt did not occur 1h = Interrupt occurred
0	RXOVF	R	0h	RXFIFO overflow event. This interrupt is set if an RX FIFO overflow has been detected. 0h = Interrupt did not occur 1h = Interrupt occurred

18.6.4 MIS Register (Offset = 4Ch) [Reset = 00000000h]

MIS is shown in Table 18-7.

Return to the Summary Table.

Masked interrupt status. This register is simply a bitwise AND of the contents of [IMASK.*] and [RIS.*] registers. A flag set in this register can be cleared by writing 1 to the corresponding [ICLR.*] register bit.

Table 18-7. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	DMATX	R	0h	Masked DMA Done event for TX. 0h = Interrupt did not occur 1h = Interrupt occurred
7	DMARX	R	0h	Masked DMA Done event for RX. 0h = Interrupt did not occur 1h = Interrupt occurred
6	IDLE	R	0h	Masked SPI IDLE event. 0h = Interrupt did not occur 1h = Interrupt occurred
5	TXEMPTY	R	0h	Masked Transmit FIFO Empty event. 0h = Interrupt did not occur 1h = Interrupt occurred
4	TX	R	0h	Masked Transmit FIFO event. 0h = Interrupt did not occur 1h = Interrupt occurred
3	RX	R	0h	Masked receive FIFO event. 0h = Interrupt did not occur 1h = Interrupt occurred
2	RTOUT	R	0h	Masked SPI Receive Time-Out event. 0h = Interrupt did not occur 1h = Interrupt occurred
1	PER	R	0h	Masked Parity error event. 0h = Interrupt did not occur 1h = Interrupt occurred
0	RXOVF	R	0h	Masked RXFIFO overflow event. 0h = Interrupt did not occur 1h = Interrupt occurred

18.6.5 ISET Register (Offset = 50h) [Reset = 00000000h]

ISET is shown in Table 18-8.

Return to the Summary Table.

Interrupt set register. This register can used by software for diagnostics and safety checking purposes. Writing a 1 to a bit in this register will set the event and the corresponding [RIS.*] bit also gets set. If the corresponding [IMASK.*] bit is set, then the corresponding [MIS.*] register bit also gets set.

Table 18-8. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	DMATX	W	0h	Set DMA Done event for TX. 0h = NOEFF : Writing 0 has no effect 1h = Set Interrupt
7	DMARX	W	0h	Set DMA Done event for RX. 0h = NOEFF : Writing 0 has no effect 1h = Set Interrupt
6	IDLE	W	0h	Set SPI IDLE event. 0h = NOEFF : Writing 0 has no effect 1h = Set Interrupt
5	TXEMPTY	W	0h	Set Transmit FIFO Empty event. 0h = NOEFF : Writing 0 has no effect 1h = Set Interrupt
4	TX	W	0h	Set Transmit FIFO event. 0h = NOEFF : Writing 0 has no effect 1h = Set Interrupt
3	RX	W	0h	Set Receive FIFO event. 0h = NOEFF : Writing 0 has no effect 1h = Set Interrupt
2	RTOUT	W	0h	Set SPI Receive Time-Out Event. 0h = NOEFF : Writing 0 has no effect 1h = Set Interrrupt Mask
1	PER	W	0h	Set Parity error event. 0h = NOEFF : Writing 0 has no effect 1h = Set Interrupt
0	RXOVF	W	0h	Set RXFIFO overflow event. 0h = NOEFF : Writing 0 has no effect 1h = Set Interrupt

18.6.6 ICLR Register (Offset = 54h) [Reset = 00000000h]

ICLR is shown in Table 18-9.

Return to the Summary Table.

Interrupt clear register. This register allows software to clear interrupts. Writing a 1 to a bit in this register will clear the event and the corresponding [RIS.*] bit also gets cleared. If the corresponding [IMASK.*] bit is set, then the corresponding [MIS.*] register bit also gets cleared.

Table 18-9. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	DMATX	W	0h	Clear DMA Done event for TX. 0h = NOEFF : Writing 0 has no effect 1h = Clear Interrupt
7	DMARX	W	0h	Clear DMA Done event for RX. 0h = NOEFF : Writing 0 has no effect 1h = Clear Interrupt
6	IDLE	W	0h	Clear SPI IDLE event. 0h = NOEFF : Writing 0 has no effect 1h = Clear Interrupt
5	TXEMPTY	W	0h	Clear Transmit FIFO Empty event. 0h = NOEFF : Writing 0 has no effect 1h = Clear Interrupt
4	TX	W	0h	Clear Transmit FIFO event. 0h = NOEFF : Writing 0 has no effect 1h = Clear Interrupt
3	RX	W	0h	Clear Receive FIFO event. 0h = NOEFF : Writing 0 has no effect 1h = Clear Interrupt
2	RTOUT	W	0h	Clear SPI Receive Time-Out Event. 0h = NOEFF : Writing 0 has no effect 1h = Set Interrrupt Mask
1	PER	W	0h	Clear Parity error event. 0h = NOEFF : Writing 0 has no effect 1h = Clear Interrupt
0	RXOVF	W	0h	Clear RXFIFO overflow event. 0h = NOEFF : Writing 0 has no effect 1h = Clear Interrupt

18.6.7 IMSET Register (Offset = 58h) [Reset = 00000000h]

IMSET is shown in Table 18-10.

Return to the Summary Table.

Interrupt mask set register. Writing a 1 to a bit in this register will set the corresponding [IMASK.*] bit.

Table 18-10. IMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	DMATX	W	0h	Set DMA Done for TX event mask 0h = NOEFF : Writing 0 has no effect 1h = Set interrupt mask
7	DMARX	W	0h	Set DMA Done for RX event mask 0h = NOEFF : Writing 0 has no effect 1h = Set interrupt mask
6	IDLE	W	0h	Set SPI IDLE event mask 0h = NOEFF : Writing 0 has no effect 1h = Set interrupt mask
5	TXEMPTY	W	0h	Set Transmit FIFO Empty event mask 0h = NOEFF : Writing 0 has no effect 1h = Set interrupt mask
4	TX	W	0h	Set Transmit FIFO event mask 0h = NOEFF : Writing 0 has no effect 1h = Set interrupt mask
3	RX	W	0h	Set Receive FIFO event mask 0h = NOEFF : Writing 0 has no effect 1h = Set interrupt mask
2	RTOUT	W	0h	Set SPI Receive Time-Out event mask 0h = NOEFF : Writing 0 has no effect 1h = Set interrupt mask
1	PER	W	0h	Set Parity error event mask 0h = NOEFF : Writing 0 has no effect 1h = Set interrupt mask
0	RXOVF	W	0h	Set RXFIFO overflow event mask 0h = NOEFF : Writing 0 has no effect 1h = Set interrupt mask

18.6.8 IMCLR Register (Offset = 5Ch) [Reset = 00000000h]

IMCLR is shown in Table 18-11.

Return to the Summary Table.

Interrupt mask clear register. Writing a 1 to a bit in this register will clear the corresponding [IMASK.*] bit.

Table 18-11. IMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	DMATX	W	0h	Clear DMA Done for TX event mask 0h = NOEFF : Writing 0 has no effect 1h = Clear interrupt mask
7	DMARX	W	0h	Clear DMA Done for RX event mask 0h = NOEFF : Writing 0 has no effect 1h = Clear interrupt mask
6	IDLE	W	0h	Clear SPI IDLE event mask 0h = NOEFF : Writing 0 has no effect 1h = Clear interrupt mask
5	TXEMPTY	W	0h	Clear Transmit FIFO Empty event mask 0h = NOEFF : Writing 0 has no effect 1h = Clear interrupt mask
4	TX	W	0h	Clear Transmit FIFO event mask 0h = NOEFF : Writing 0 has no effect 1h = Clear interrupt mask
3	RX	W	0h	Clear Receive FIFO event mask 0h = NOEFF : Writing 0 has no effect 1h = Clear interrupt mask
2	RTOUT	W	0h	Clear SPI Receive Time-Out event mask 0h = NOEFF : Writing 0 has no effect 1h = Clear interrupt mask
1	PER	W	0h	Clear Parity error event mask 0h = NOEFF : Writing 0 has no effect 1h = Clear interrupt mask
0	RXOVF	W	0h	Clear RXFIFO overflow event mask 0h = NOEFF : Writing 0 has no effect 1h = Clear interrupt mask

18.6.9 EMU Register (Offset = 60h) [Reset = 00000000h]

EMU is shown in Table 18-12.

Return to the Summary Table.

Emulation control register. This register controls the behavior of the IP related to core halted input.

Table 18-12. EMU Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	HALT	R/W	0h	Halt control 0h = Free run option. The IP ignores the state of the core halted input. 1h = Freeze option. The IP freezes functionality when the core halted input is asserted, and resumes when it is deasserted. The freeze can either be immediate or after the IP has reached a boundary (end of word boundary, based on DSS configuration) from where it can resume without corruption.

18.6.10 CTL0 Register (Offset = 100h) [Reset = 00000000h]

CTL0 is shown in Table 18-13.

Return to the Summary Table.

SPI control register 0

Table 18-13. CTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-18	CSSEL	R/W	0h	CS select for Multi SPI support 00 - CS0 01 - CS1 10 - CS2 11 - CS3 0h (R/W) = Select CS0 1h (R/W) = Select CS1 2h (R/W) = Select CS2 3h (R/W) = Select CS3
17	IDLEPOCI	R/W	0h	The Idle value of POCI - when TXFIFO is empty and before data is written into TXFIFO - can be controlled by this field. 0h (R/W) = POCI output idle value of '0' 1h (R/W) = POCI outputs idle value of '1'
16	GPCRCEN	R/W	0h	General purpose CRC enable. This bit enables transmit side CRC unit for general purpose use by software when SPI is disabled (CTL1.EN = 0). This bit must be 0 when SPI is enabled. 0h = DIS : Transmit side CRC unit is not available for general purpose software use 1h = EN : Transmit side CRC unit is available for general purpose software use
15	CRCPOLY	R/W	0h	CRC polynomial selection. 0h = Selects 8-bit CCITT CRC polynomial 1h = Selects 16-bit CCITT CRC polynomial
14	AUTOCRC	R/W	0h	Auto insert CRC 0h (R/W) = DIS : Do not insert CRC into TXFIFO upon TXFIFO underflow 1h (R/W) = EN : Insert CRC into TXFIFO upon TXFIFO underflow
13	CRCEND	R/W	0h	CRC16 Endianness 0h (R/W) = Auto-insertion of CRC16 is most-significant byte first 1h (R/W) = Auto-insertion of CRC16 is least-significant byte first
12	CSCLR	R/W	0h	Clear shift register counter on CS inactive. This bit is relevant only in the peripheral mode, when MS=0. 0h = DIS : Disable automatic clear of shift register when CS goes inactive. 1h = EN : Enable automatic clear of shift register when CS goes inactive.
11	FIFORST	R/W	0h	This bit is used to reset transmit and receive FIFO pointers. This bit is auto cleared once the FIFO pointer reset operation is completed. 0h = FIFO pointers reset completed when 0 is read 1h = Trigger FIFO pointers reset when written to 1.
10	HWCSN	R/W	0h	Hardware controlled chip select (CS) value. When set CS is zero till TX FIFO is empty, as in - a. CS is de-asserted b. All data bytes are transmitted c. CS is asserted 0h (R/W) = DIS : HWCS Disable 1h (R/W) = EN : HWCS Enable
9	SPH	R/W	0h	CLKOUT phase (Motorola SPI frame format only). This bit selects the clock edge that captures data and enables it to change state. It has the most impact on the first bit transmitted by either permitting or not permitting a clock transition before the first data capture clock edge. 0h = Data is captured on the first clock edge transition. 1h = Data is captured on the second clock edge transition.
8	SPO	R/W	0h	CLKOUT polarity (Motorola SPI frame format only). 0h = LO : SPI produces a steady state LOW value on the CLKOUT 1h = HI : SPI produces a steady state HIGH value on the CLKOUT

Table 18-13. CTL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-5	FRF	R/W	0h	Frame format select 0h = Motorola SPI frame format (3 wire mode) 1h = Motorola SPI frame format (4 wire mode) 2h = TI synchronous serial frame format 3h = National Microwire frame format
4	RESERVED	R	0h	Reserved
3-0	DSS	R/W	0h	Data size select. The applicable DSS values for controller mode operation are 0x3 to 0xF and for peripheral mode operation are 0x6 to 0xF. DSS values 0x0 to 0x2 are reserved and must not be used. 3h (R/W) = 4-bits data size 4h (R/W) = 5-bits data size 5h (R/W) = 6-bits data size 6h (R/W) = 7-bits data size 7h (R/W) = 8-bits data size 8h (R/W) = 9-bits data size 9h (R/W) = 10-bits data size Ah (R/W) = 11-bits data size Bh (R/W) = 12-bits data size Ch (R/W) = 13-bits data size Dh (R/W) = 14-bits data size Eh (R/W) = 15-bits data size Fh (R/W) = 16-bits data size

18.6.11 CTL1 Register (Offset = 104h) [Reset = 00000004h]

CTL1 is shown in Table 18-14.

Return to the Summary Table.

SPI control register 1

Table 18-14. CTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-24	RTOUT	R/W	0h	Receive Timeout (only for Peripheral mode) Defines the number of Clock Cycles before after which the Receive Timeout flag RTOUT is set. The time is calculated using the control register for the clock selection and divider in the Controller mode configuration. A value of 0 disables this function.
23-16	REPTX	R/W	0h	Counter to repeat last transfer 0: repeat last transfer is disabled. x: repeat the last transfer with the provided value. The transfer will be started with writing a data into the TX FIFO. Sending the data will be repeated provided value number of times, so the data will be transferred x+1 times in total. The behavior would be as if the data were be written into the TX FIFO as many times as defined by the value here additionally. It can be used to clean a transfer or to pull a certain amount of data by a peripheral.
15-12	CDMODE	R/W	0h	Command Data Mode. This bit field value determines the behavior of C/D or CS signal when CDEN = 1. CS pin held low indicates command phase and CS pin held high indicates data phase. When CDMODE = 0x0, the CS pin is always held high during transfer indicating data phase only operation (manual mode). When CDMODE = 0xF, the CS pin is always held low during transfer indicating command phase only operation (manual mode). When CDMODE = 0x1 to 0xE, the CS pin is held low for the number of bytes indicated by CDMODE value for the command phase and held high for the remaining transfers in the data phase (automatic mode). When CDMODE is set to value 0x1 to 0xE, reading CDMODE during operation indicates the remaining bytes to be transferred in the command phase. 0h = Manual mode: Data Fh = Manual mode: Command
11	CDEN	R/W	0h	Command/Data mode enable. This feature is applicable only in controller mode and for 8-bit transfers (DSS = 7). The chip select pin is used for command/data signaling in Motorola SPI frame format (3-wire) operation. 0h = DIS : C/D Mode Disable 1h = EN : C/D Mode Enable
10-8	RESERVED	R	0h	Reserved
7	PBS	R/W	0h	Parity bit select 0h = Bit 0 is used for Parity 1h = Bit 1 is used for Parity, Bit 0 is ignored
6	PES	R/W	0h	Even parity select. 0h = Odd Parity mode 1h = Even Parity mode
5	PEN	R/W	0h	Parity enable. If enabled the last bit will be used as parity to evaluate the correct reception of the previous bits. In case of parity mismatch the parity error flag PER will be set. This feature is available only in SPI controller mode. 0h = DIS : Disable Parity function 1h = EN : Enable Parity function
4	MSB	R/W	0h	MSB first select. Controls the direction of receive and transmit shift register. MSB first configuration (MSB = 1) must be selected when CRC feature is used for SPI communication. 0h = LSB first 1h = MSB first

Table 18-14. CTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	POD	R/W	0h	Peripheral data output disable. This bit is relevant only in the peripheral mode, MS=1. In multiple-peripheral systems, it is possible for a SPI controller to broadcast a message to all peripherals in the system while ensuring that only one peripheral drives data onto its serial output line. In such systems the POCI lines from multiple peripherals could be tied together. To operate in such systems, this bit field can be set if the SPI peripheral is not supposed to drive the POCI output. 0h = DIS : SPI can drive the POCI output in peripheral mode. 1h = EN : SPI cannot drive the POCI output in peripheral mode.
2	MS	R/W	1h	Controller or peripheral mode select. This bit can be modified only when SPI is disabled, CTL1.EN=0. 0h = PERIPHERAL : Select Peripheral mode 1h = CONTROLLER : Select Controller mode
1	LBM	R/W	0h	Loop back mode control 0h = DIS : Disable loopback mode. Normal serial port operation enabled. 1h = EN : Enable loopback mode. Output of transmit serial shifter is connected to input of receive serial shifter internally.
0	EN	R/W	0h	SPI enable. 0h = DIS : SPI is disabled 1h = EN : SPI Enabled and released for operation.

18.6.12 CLKCFG0 Register (Offset = 108h) [Reset = 00000000h]

CLKCFG0 is shown in Table 18-15.

Return to the Summary Table.

Clock configuration register 0. This register is used to configure the clock prescaler.

Table 18-15. CLKCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	PRESC	R/W	0h	Prescaler configuration 0h = Do not divide clock source 1h = Divide clock source by 2 2h = Divide clock source by 3 3h = Divide clock source by 4 4h = Divide clock source by 5 5h = Divide clock source by 6 6h = Divide clock source by 7 7h = Divide clock source by 8

18.6.13 CLKCFG1 Register (Offset = 10Ch) [Reset = 00000000h]

CLKCFG1 is shown in Table 18-16.

Return to the Summary Table.

Clock configuration register 1. This register is used to configure serial clock rate and clock count for delayed sampling in controller mode.

Table 18-16. CLKCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	DSAMPLE	R/W	0h	Delayed sampling. In controller mode the data on the input pin will be delayed sampled by the defined clock cycles. DSAMPLE values can range from 0 to SCR+1. Typically, values of 1 or 2 would suffice.
15-10	RESERVED	R	0h	Reserved
9-0	SCR	R/W	0h	Serial clock divider. This is used to generate the transmit and receive bit rate of the SPI. The SPI bit rate: (SPI functional clock frequency)/((SCR+1)*2). SCR value can be from 0 to 1023.

18.6.14 IFLS Register (Offset = 110h) [Reset = 00000202h]

IFLS is shown in Table 18-17.

Return to the Summary Table.

Interrupt FIFO level select register. This register can be used to define the levels at which the TX, RX flags are triggered. The interrupts are generated based on FIFO level. Out of reset, the TXSEL and RXSEL bits are configured so that the FIFOs trigger an interrupt at the half-way mark.

Table 18-17. IFLS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-8	RXSEL	R/W	2h	Receive FIFO Level Select. The trigger points for the receive interrupt are as follows: 0h = Reserved 1h = RX FIFO >= 1/4 full 2h = RX FIFO >= 1/2 full (default) 3h = RX FIFO >= 3/4 full 4h = Reserved 5h = RX FIFO is full 6h = Reserved 7h = Trigger when RX FIFO contains >= 1 byte
7-3	RESERVED	R	0h	Reserved
2-0	TXSEL	R/W	2h	Transmit FIFO Level Select. The trigger points for the transmit interrupt are as follows: 0h = Reserved 1h = TX FIFO <= 3/4 empty 2h = TX FIFO <= 1/2 empty (default) 3h = TX FIFO <= 1/4 empty 4h = Reserved 5h = TX FIFO is empty 6h = Reserved 7h = Trigger when TX FIFO has >= 1 byte free

18.6.15 DMACR Register (Offset = 114h) [Reset = 00000000h]

DMACR is shown in Table 18-18.

Return to the Summary Table.

DMA Control Register

Table 18-18. DMACR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	TXEN	R/W	0h	Transmit DMA enable. If this bit is set to 1, DMA for the transmit FIFO is enabled. 0h = DIS : Disable TX DMA 1h = EN : Enable TX DMA
7-1	RESERVED	R	0h	Reserved
0	RXEN	R/W	0h	Receive DMA enable. If this bit is set to 1, DMA for the receive FIFO is enabled. 0h = DIS : Disable RX DMA 1h = EN : Enable RX DMA

18.6.16 RXCRC Register (Offset = 118h) [Reset = 00000000h]

RXCRC is shown in Table 18-19.

Return to the Summary Table.

Receive CRC register. Reading this register provides the computed CRC value from the receive side CRC unit. Reading this register or writing to this register with any value auto initializes the seed. The seed value is 0xFF when CRCPOLY = 0 and 0xFFFF when CRCPOLY = 1 for CCITT CRC polynomials. Bits[15:8] are a don't care when CRCPOLY = 0.

Table 18-19. RXCRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	DATA	R/W	0h	CRC value

18.6.17 TXCRC Register (Offset = 11Ch) [Reset = 00000000h]

TXCRC is shown in Table 18-20.

Return to the Summary Table.

Transmit CRC register. Reading this register provides the computed CRC value from the transmit side CRC unit. Reading this register or writing to this register with any value auto initializes the seed. The seed value is 0xFF when CRCPOLY = 0 and 0xFFFF when CRCPOLY = 1 for CCITT CRC polynomials. Bits[15:8] are a don't care when CRCPOLY = 0.

Table 18-20. TXCRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTOCRCINS	RC	0h	Status to indicate if Auto CRC has been inserted into TXFIFO. This is applicable only if CTL0.AUTOCRC enable bit is set 0h (R) = NOTINS : Auto CRC not yet inserted 1h (R) = INS : Auto CRC inserted
30-16	RESERVED	R	0h	Reserved
15-0	DATA	R/W	0h	CRC value

18.6.18 TXFHDR32 Register (Offset = 120h) [Reset = 00000000h]

TXFHDR32 is shown in Table 18-21.

Return to the Summary Table.

Header update reigster for 32 bits of header data.

Table 18-21. TXFHDR32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	This field can be used to write four bytes of header data

18.6.19 TXFHDR24 Register (Offset = 124h) [Reset = 00000000h]

TXFHDR24 is shown in Table 18-22.

Return to the Summary Table.

Header update reigster for 24 bits of header data.

Table 18-22. TXFHDR24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	This field can be used to write three bytes of header data

18.6.20 TXFHDR16 Register (Offset = 128h) [Reset = 00000000h]

TXFHDR16 is shown in Table 18-23.

Return to the Summary Table.

Header update reigster for 16 bits of data.

Table 18-23. TXFHDR16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	This field can be used to write two bytes of header data

18.6.21 TXFHDR8 Register (Offset = 12Ch) [Reset = 00000000h]

TXFHDR8 is shown in Table 18-24.

Return to the Summary Table.

Header update reigster for 8 bits of header data.

Table 18-24. TXFHDR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	This field can be used to write one byte of header data

18.6.22 TXFHDRC Register (Offset = 130h) [Reset = 00000000h]

TXFHDRC is shown in Table 18-25.

Return to the Summary Table.

Atomic Header control register

Table 18-25. TXFHDRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	CSGATE	R/W	0h	Chip Select Gating control register. If this bit is set header update register writes are blocked when chip select (CS) is active low, and [HDRIGN] bit is set. This bit resets to 0. 0h = UNBLK : The first header update register write is not blocked based on CS active status (low). If no header update occurred when CS was high (inactive), the first header update is allowed when CS is low (active), and the HDRCMT bit is set. The use case is for the external controller to ensure that the SCLK is not driven during this header update. If the header is already updated when CS is high and inactive, HDRCMT is set immediately when CS drops to active low state, and header writes when CS is low are ignored even if this UNBLK bit is set. 1h = BLK : Header update register writes are blocked when CS is active (low)
2	HDRCMT	R/W	0h	Header Committed field. This bit is set when the [HDREN] bit is set and CS is sampled low. This bit remains 0 otherwise. When set, this bit can be written to a value of 0 to clear. 0h = Header update is not committed 1h = Header update is committed
1	HDRIGN	R/W	0h	Header Ignored field. When [CSGATE] is set to BLK, this bit is set when the last Header update register [TXFHDRn.*] is written when CS is low or [HDRCMT] is already set. When [CSGATE] is set to UNBLK, this bit is set only when the header update register is written when [HDRCMT] is already set. This bit remains 0 otherwise. When set, this bit can be written to a value of 0 to clear. 1h = CLEAR : Header update is not ignored
0	HDREN	R/W	0h	Header enable field. When [CSGATE] is set to BLK, this bit has to be set by software to enable this feature. When [CSGATE] is set to UNBLK, this field is set automatically whenever a write to header update registers occurs [TXFHDRn.*] 0h = DIS : Atomic header update feature disable 1h = EN : Atomic header update feature enable

18.6.23 RXDATA Register (Offset = 140h) [Reset = 00000000h]

RXDATA is shown in Table 18-26.

Return to the Summary Table.

RXDATA Register. Reading this register returns first value in the RX FIFO. If the FIFO is empty the last read value is returned. Writing has no effect and is ignored.

Table 18-26. RXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	DATA	R	0h	Received Data. When read, the entry in the receive FIFO, pointed to by the current FIFO read pointer is accessed. As data values are read by the receive logic from the incoming data frame, they are placed into the entry in the receive FIFO, pointed to by the current RX FIFO write pointer. Received data less than 16 bits is automatically right-justified in the receive buffer.

18.6.24 TXDATA Register (Offset = 150h) [Reset = 00000000h]

TXDATA is shown in Table 18-27.

Return to the Summary Table.

TXDATA Register. Writing a value in this register puts the data into the TX FIFO. Reading this register returns the last written value.

Table 18-27. TXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	DATA	R/W	0h	Transmit Data. When read, the last entry in the transmit FIFO, pointed to by the current FIFO write pointer is accessed. When written, the entry in the TX FIFO pointed to by the write pointer, is written to. Data values are read from the transmit FIFO by the transmit logic. It is loaded into the transmit serial shifter, then serially shifted out onto the output pin at the programmed bit rate. When a data size of less than 16 bits is selected, the user must right-justify data written to the transmit FIFO. The transmit logic ignores the unused bits.

18.6.25 STA Register (Offset = 160h) [Reset = 00000000h]

STA is shown in Table 18-28.

Return to the Summary Table.

Status Register

Table 18-28. STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-8	TXFIFOLVL	R	0h	Indicates how many locations of TXFIFO are currently filled with data
7	RESERVED	R	0h	Reserved
6	TXDONE	R/W	0h	Transmit done. Indicates whether the last bit left the Shift register after a transmission 0h (R/W) = TX_ONGOING : Last bit has not yet left the Shift register, and the transmission is ongoing. 1h (R/W) = TX_DONE : Last bit has been shifted out, and the transmission is done
5	CSD	R/W	0h	Detection of CS deassertion in the middle of a word transmission results in this error being set. This feature is only available in the peripheral mode. 0h (R/W) = NOERR : No CS posedge is detected before the entire word has been transmitted. 1h (R/W) = ERR : An error is generated when CS posedge (deassertion) is detected before the entire word is transmitted.
4	BUSY	R	0h	SPI Busy status 0h = SPI is in idle mode. 1h = SPI is currently transmitting and/or receiving data, or transmit FIFO is not empty.
3	RNF	R	1h	Receive FIFO not full status. 0h = Receive FIFO is full. 1h = Receive FIFO is not full.
2	RFE	R	1h	Receive FIFO empty status. 0h = Receive FIFO is not empty. 1h = Receive FIFO is empty.
1	TNF	R	1h	Transmit FIFO not full status. 0h = Transmit FIFO is full. 1h = Transmit FIFO is not full.
0	TFE	R	1h	Transmit FIFO empty status. 0h = Transmit FIFO is not empty. 1h = Transmit FIFO is empty.

18.6.26 CLKCFG Register (Offset = 1000h) [Reset = 00000000h]

CLKCFG is shown in Table 18-29.

Return to the Summary Table.

Clock Enable Register

Table 18-29. CLKCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	ENABLE	R/W	0h	SPI main clock Enable

Chapter 19

Inter-Integrated Circuit (I2C) Interface

This chapter describes the inter-integrated circuit (I^2C) interface.

19.1 Introduction

The I^2C bus provides bidirectional data transfer through a 2-wire design, a serial data line (SDA) and a serial clock line (SCL), and interfaces to external I^2C devices such as serial memory (RAM and ROM), networking devices, LCDs, tone generators, and so on. The I^2C bus can also be used for system testing and diagnostic purposes in product development and manufacture.

The I^2C module has following features:

- Devices on the I^2C bus can be designated as either a Controller or a Target.
- Supports both transmitting and receiving data as either a Controller or Target.
- Four I2C modes
  - Controller-transmit
  - Controller-receive
  - Target-transmit
  - Target-receive
- FIFO support in Controller and Target modes for receive and transmit data with each location being 8-bits wide
- 7-bit and 10-bit addressing support
- Supported transmission speeds:
  - Standard (100 kbps)
  - Fast Mode (400 kbps)
  - Fast Mode + (1 Mbps)
- Glitch suppression using digital glitch filters
- Multi Target address capability
- Quick command capability
- Support for host notify protocol, alert response protocol, address resolution protocol addresses
- Independent Controller and Target interrupt generation
- Controller operation with arbitration, clock synchronization, multi-Controller support
- Hardware support for DMA with separate channels for transmit and receive

19.2 Block Diagram

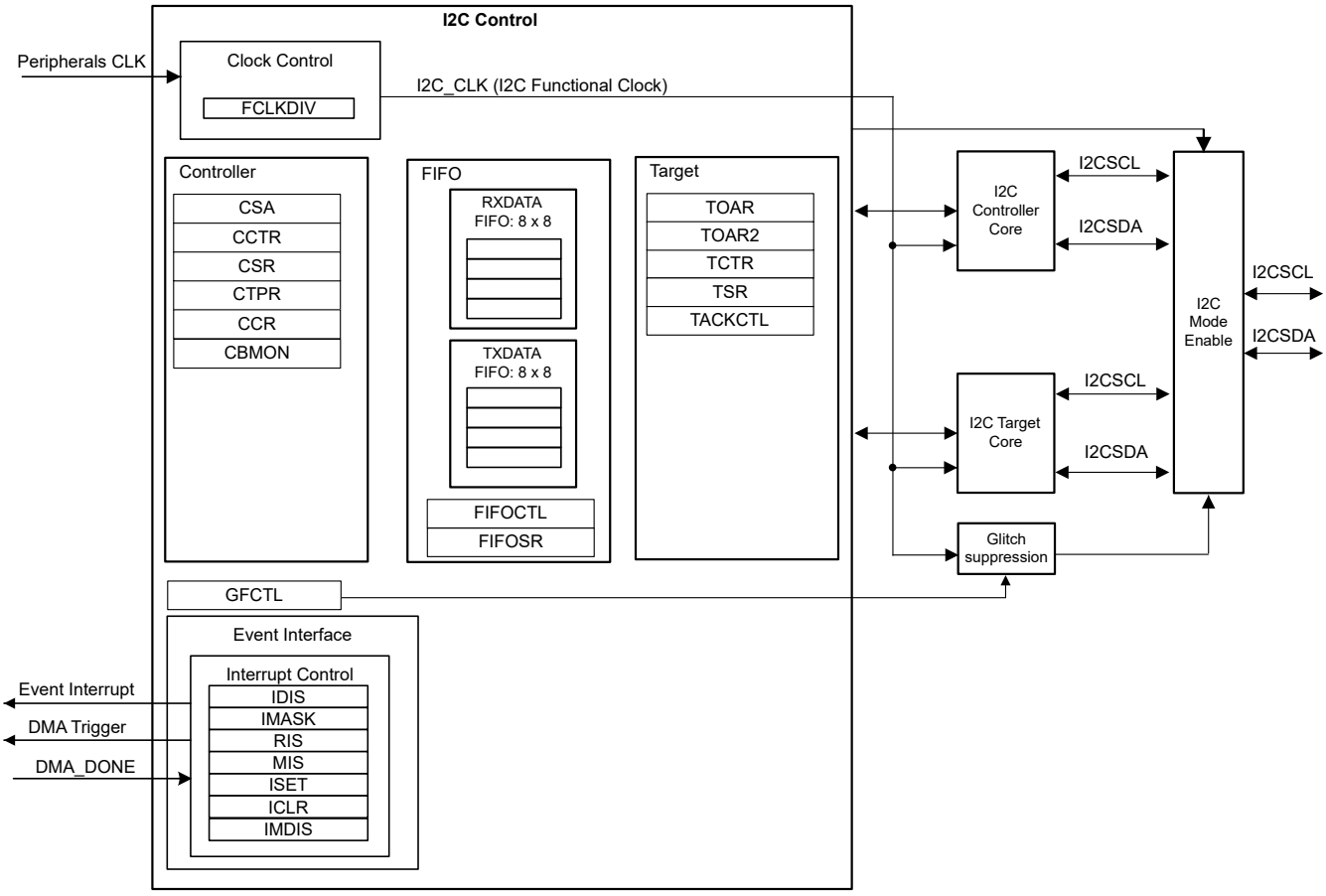


Figure 19-1. I2C Block Diagram

19.3 Functional Description

Each I^{2}C peripheral instance is comprised of both Controller and Target functions where the Target can be addressed with multiple independent user defined addresses – exact and mask matches. A device connected to the I^{2}C bus can be considered as the Controlleror the Target when performing data transfers. A Controller initiates a data transfer and generates the clock signal SCL. Any device addressed by a Controller is considered a Target.

I2C data is communicated using the serial data (SDA) pin and the serial clock (SCL) pin. Both SDA and SCL are bidirectional and must be connected to a positive supply voltage using a pullup resistor that will almost always be external to the IP on the board.

See Chapter 16 for more information on configuring pin functions. Figure 19-2 shows a typical I^{2}C bus configuration.

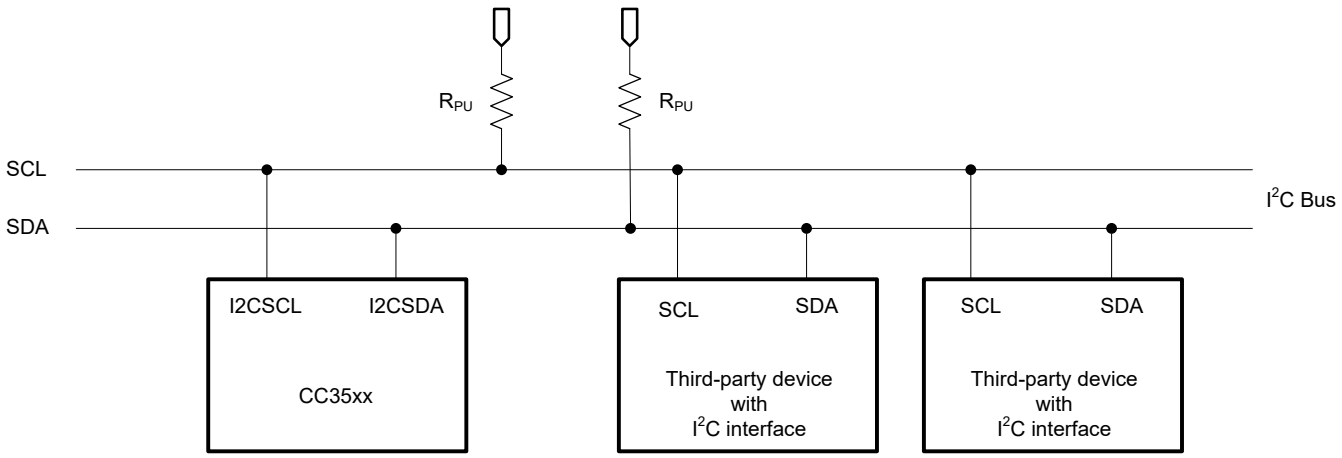


Figure 19-2. I²C Bus Configuration

19.3.1 Clock Control

19.3.1.1 Internal Clock

The I²C internal functional clock is selected and divided from the functional clock of the IP.

- Use CLKSEL register to select the source of the I²C functional clock – One of medium frequency or high frequency clocks
- Use CLKDIV register to select the divide ratio of the I²C function clock.

The selected source clock is always available and the frequency depends on the power mode, for more information please refers to Chapter 7.

19.3.1.2 External Clock

Standard, Fast, and Fast Plus modes are selected using a value in the I2C Controller Timer Period (I2Cx.CTPR) register that results in an SCL frequency of:

- 100 kbps for Standard mode,
- 400 kbps for Fast mode,
- 1 Mbps for Fast mode plus

The I2C clock rate is determined by the parameters INT_CLK_PRD, TPR, SCL_LP, and SCL_HP where:

- INT_CLK_PRD is the internal functional clock period to the I2C module.
- SCL_LP is the low phase of SCL (fixed at 6)
- SCL_HP is the high phase of SCL (fixed at 4)
- TPR is the programmed value of the TPR bits in the CTPR register. This value is determined by replacing the known variables in the equation below and solving for TPR

Table 19-1. Functional clock division

I2Cx.CTPR Value	Division factor	I2C_CLK (SOC_CLK [1] / division factor)
0000	1	80
0001	2	40
0010	4	20
0011	5	16
0100	8	10
0101	10	8
0110	16	5
0111	20	4
1000	25	3.2

Table 19-1. Functional clock division (continued)

I2Cx.CTPR Value	Division factor	I2C_CLK (SOC_CLK [1] / division factor)
1001	32	2/5
1010	40	2
1011	80	1
Reserved	-	-

(1) SOC_CLK = 80MHz

I2C clock period can be calculated as follows:

$$SCL\_PERIOD = (1 + TPR) * (SCL\_LP + SCL\_HP) * INT\_CLK\_PRD \quad (9)$$

For example:

INT_CLK_PRD = 1/20 MHz = 50 ns

TPR = 19 (0x13)

SCL_LP = 6

SCL_HP = 4

yields a SCL frequency of:

1/SCL_PERIOD = 100 kHz

Some more examples:

Table 19-2. Examples of Controller Clock Setting for Typical Clock Configurations

Functional Clock	Timer Period	Standard Mode	Timer Period	Fast Mode	Timer Period	Fast Mode Plus
4 MHz	0x03	100 kHz	-	-	-	-
8 MHz	0x07	100 kHz	0x01	400 kHz	-	-
20 MHz	0x13	100 kHz	0x04	400 kHz	0x01	1 MHz
40 MHz	0x27	100 kHz	0x09	400 kHz	0x03	1 MHz
80 MHz	0x4F	100 kHz	0x13	400 kHz	0x07	1 MHz

The IP has a 20x clock frequency requirement both in Controller and Target modes. Therefore, the following minimum functional clock frequencies are required in different modes:

Functional Clock >= 2MHz when working with I2C speed 0-100KHz,

Functional Clock >= 8MHz when working with I2C speed 100KHz-400KHz,

Functional Clock >= 20MHz when working with I2C speed 400KHz-1MHz

Note

The final frequency of functional clock will depend on tVD;DATA timing parameter of I2C spec. If the Open Drain IO delays are high, the delay inside the IP will have to be reduced which would mean a faster functional clock.

19.3.2 General Architecture

The I2C bus uses only two signals: SDA and SCL.

SDA is the bidirectional serial data line and SCL is the bidirectional serial clock line. The bus is considered idle when both lines are high and no transfer is ongoing.

Every transaction on the I2C bus is nine bits long, consisting of eight data bits and a single acknowledge bit. A transfer is defined as the time between a valid START and STOP condition—as described in Figure 19-3.The number of bytes per transfer is unrestricted; however, each data byte must be followed by an acknowledge bit and data must be transferred MSB first. When a receiver cannot receive another complete byte, it can hold the clock line SCL low and force the transmitter into a wait state. The data transfer continues when the receiver releases the clock SCL. This mode is called clock strecthing and is configurable.

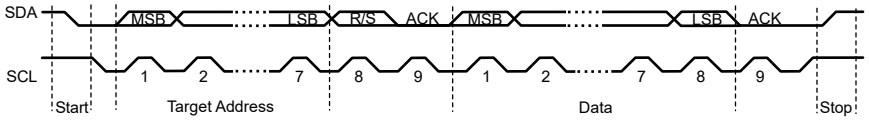


Figure 19-3. I2C Transaction Format

The data on the SDA line must be stable during the high period of the clock, and the data line can only change when SCL is Low (see Figure 19-4), otherwise START or STOP conditions are generated.

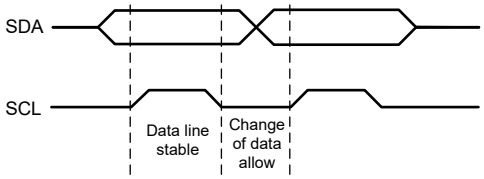


Figure 19-4. SDA stable condition

19.3.2.1 Start and Stop Conditions

The protocol of the I2C bus defines two states to begin and end a transaction: START and STOP(see Figure 19-5).

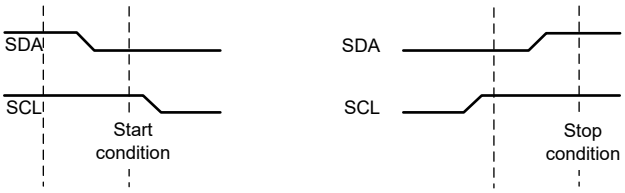


Figure 19-5. Start and Stop Conditions

A High-to-Low transition on the SDA line while the SCL is High is defined as a **START** condition, and a Low-to-High transition on the SDA line while SCL is High is defined as a **STOP** condition. START and STOP conditions are always generated by the master. The bus is considered busy after a START condition and free after a STOP condition.

Note

The Target mode logic should be designed to handle abrupt START and STOP conditions on the bus.

- In case of an unexpected STOP, the logic must go back to IDLE state and wait for the next START
- In case of an unexpected START, the logic must check for address on the bus

The STOP bit determines if the transaction stops at the end of the data cycle or continues on to a repeated START condition.

To generate a single transaction:

- I2C Controller target address (CSA) register is written with the desired address
- DIR bit is cleared to ‘0’
- Control register CCTR is written with ACK = X (0 or 1), STOP = 1, START = 1, and BURSTRUN = 1 to perform the operation and stop

- When the operation is completed (or aborted due an error) the interrupt flag(s) are set.

Note

- ACK bit only controls the ACK of last byte of MBLEN transfer. All other bytes are auto-ACKed by hardware.
- The details of all memory mapped registers of the IP can be found in Section 19.6.

When the I2C module operates in Controller receiver mode, the ACK bit is normally (in case of no error) set causing the I2C bus controller to transmit an acknowledge automatically after each byte. This bit must be cleared when the I2C bus controller requires no further data to be transmitted from the Target transmitter i.e. after the last byte of transfer and then immediately generate the STOP bit.

19.3.2.2 Data Format with 7-Bit Address

7-bit address data transfers follow the format shown in Figure 19-6. After the START condition, a Target address is transmitted. This address is 7-bits long followed by an eighth bit, which is a data direction bit (DIR bit in the CSA register). If the DIR bit is clear, it indicates a transmit operation (send), and if it is set, it indicates a request for data (receive). A data transfer is always terminated by a STOP condition generated by the master; however, a Controller can initiate communications with another device on the bus by generating a repeated START condition and addressing another Target without first generating a STOP condition. Various combinations of receive/transmit formats are then possible within a single transfer.

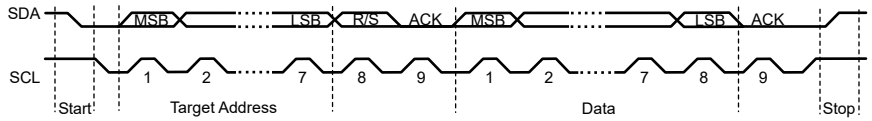


Figure 19-6. 7-Bit addressing format

Complete data transfer with a 7-Bit address, DIR (R/W) Bit in first byte and the ninth bit is the acknowledge bit.

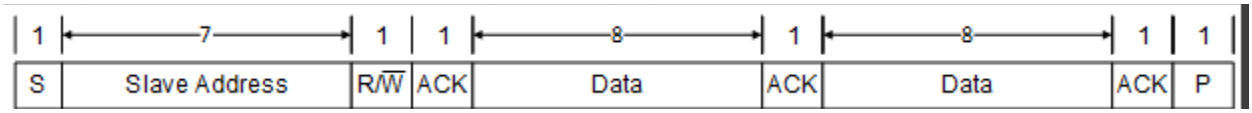


Figure 19-7. Frame Format

19.3.2.3 Data Format with 10-Bit Addressing

In order to prevent address clashes, due to the limited range of the 7-bit addresses, 10-bit address support is added. After the start condition, a leading ***'11110'*** introduces the 10-bit addressing scheme. The last two address bits of the first byte concatenated with the eight bits of the second byte of the whole 10-bit address. Devices which only use 7-bit addressing simply ignore messages with the leading '11110'.

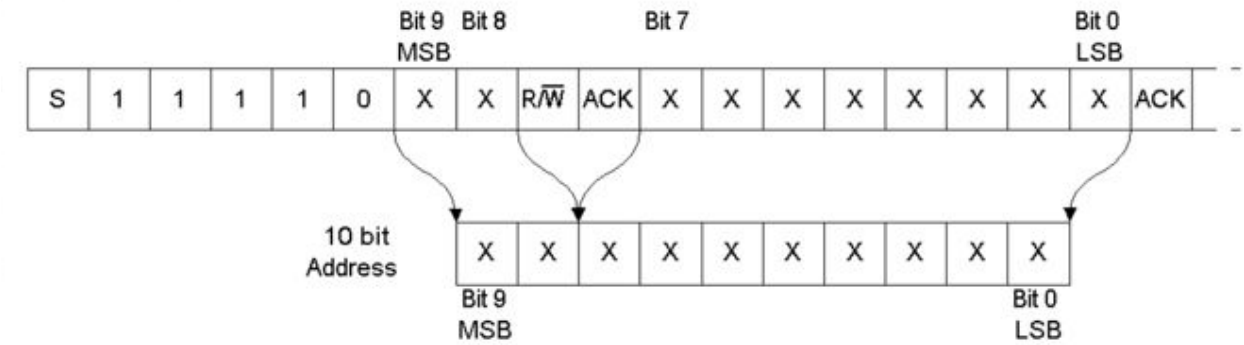


Figure 19-8. I2C 10-Bit Address Structure

A ***Controller transmitter*** addresses the Target with two address bytes as described above with the RW-Bit='0′ followed by data bytes from the Controller.

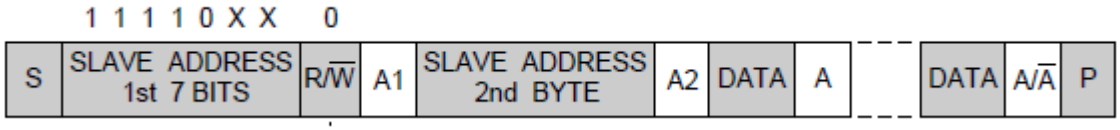


Figure 19-9. Controller Transmit 10-bit addressing

The ***Controller receiver*** transfer is only possible with a Combined Transfer due to the fact that the second address byte can only be transmitted if the RW-Bit of the first address byte is '0'. Hence, the start of a Controller receiver transfer will be the same as a Controller transmitter transfer followed by a repeated start condition and the first byte of address byte with RW-Bit='1′ (switching to Target transmitter mode).

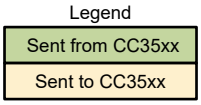
Figure 19-10. Controller Receiver 10-bit Addressing

Refer to the following Controller receiver sequence:

- Start condition
- First address byte, RW-Bit='0′, ACK from the Target
- Second address byte, ACK from the Target
- Repeated start condition (no stop condition!)
- First address byte again, RW-Bit='1′, ACK from the Target, Target switches to transmit mode
- Target transmits data bytes, ACK from Controller
- After the last data byte, the Controller sends a NACK
- Stop condition

19.3.2.3.1 Additional 10-Bit Scenarios

The below scenarios need to be supported by the IP and Target START (TSTART) and Target STOP (TSTOP) interrupts need to be generated at the right time after the address match.



Target Receiver

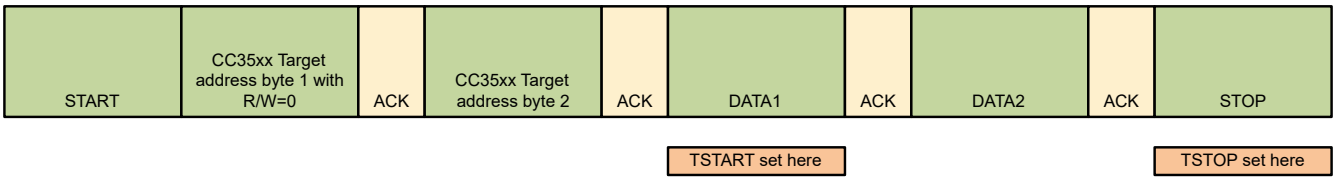


Figure 19-11. Target Reciever in 10-bit addressing

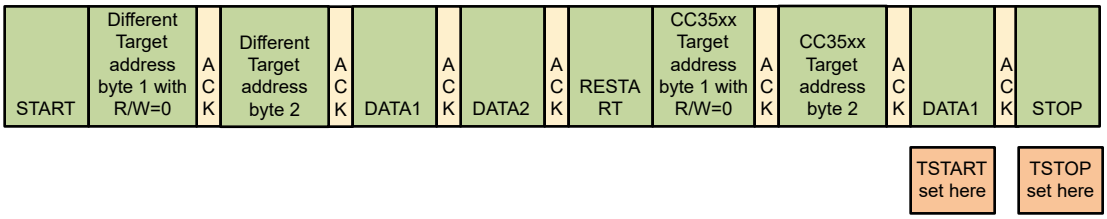


Figure 19-12. Target Reciever Scenario 2 in 10-bit addressing

Target Transmit

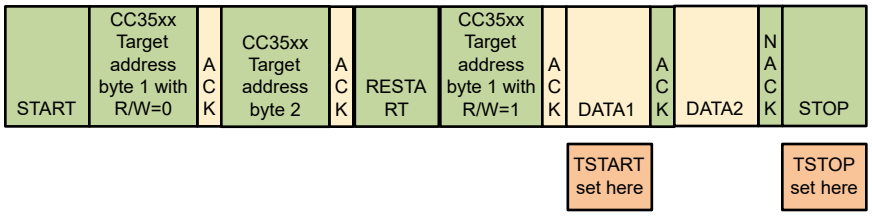


Figure 19-13. Target Transmitter in 10-bit addressing

Mixed Transfer (Target receive followed by Target transmit)

Scenario A

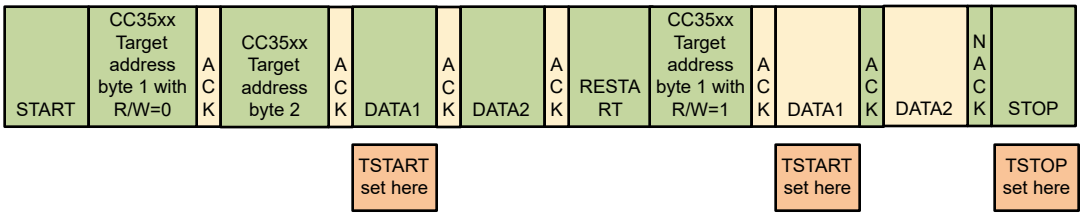


Figure 19-14. Mixed 10-bit addressing transfer scenario A

Scenario B

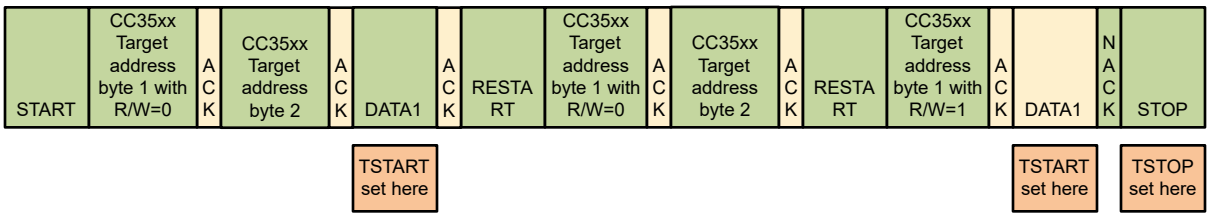


Figure 19-15. Mixed 10-bit addressing transfer scenario B

Mixed Transfer (Target transmit followed by Target receive)

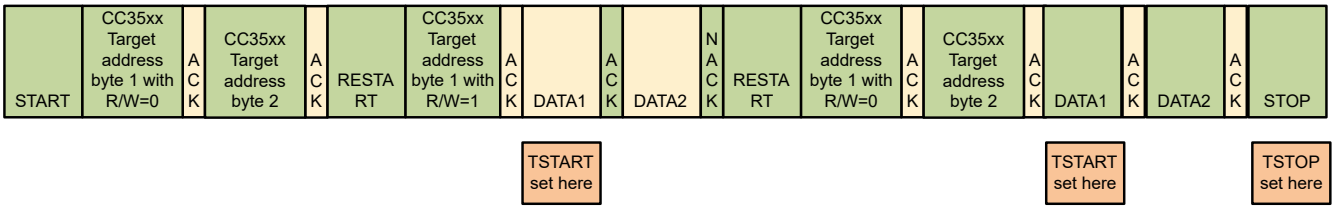


Figure 19-16. Mixed 10-bit addressing transfer scenario C

To support 10-bit addressing, below functionality is required inside the IP:

- For Target mode, extend TOAR.OAR field from 7-bits to 10-bits i.e. TOAR[9:0]. Also add TOAR.MODE control bit at TOAR[15] to select between 7-bit and 10-bit addressing modes. The Target logic accounts for 10-bit addressing (if programmed).

Note

Only 1 Target address (TOAR) supports 10-bit addressing. TOAR2 is 7-bit address only.

- For Controller mode, extend CSA.TADDR field from 7-bits to 10-bits i.e. CSA[10:1]. Also add CSA.MMODE control bit at CSA[15] to select between 7-bit and 10-bit addressing modes. This also results in corresponding

changes in ControllerFSM, which now needs to account for 10-bit addressing (if programmed) and add more states.

19.3.2.4 Acknowledge

All bus transactions have a required acknowledge clock cycle that is generated by the controller. During the acknowledge cycle, the transmitter (which can be the Controller or Target) releases the SDA line. To acknowledge [ACK] the transaction, the receiver must pull down SDA during the acknowledge clock cycle. The acknowledge cycle must comply with the data validity requirements.

Target Behavior

When a Target receiver does not acknowledge [NACK] the Target address, SDA must be left high by the Target so that the Controller can generate a STOP condition and abort the current transfer or generate a repeated START condition to start a new transfer. If the Controller device is acting as a receiver during a transfer, it is responsible for acknowledging each transfer made by the Target. Because the Controller controls the number of bytes in the transfer, it signals the end of data to the Target transmitter by not generating an acknowledge on the last data byte. The Target transmitter must then release SDA to allow the Controller to generate the STOP or a repeated START condition.

If the Target is required to provide a manual (software/firmware) ACK or NACK, the I2C Target ACK Control (TACKCTL) register allows the Target to NACK for invalid data or command, or ACK for valid data or command. Refer to section Section 19.3.2.14.5 for more details.

Controller Behavior

If the Controller receives a NACK while transmitting data, the NACK and CTXDONE bit will be set in the RIS registers. If there is still data in the FIFO, the TXEMPTY bit will not be set to inform software that a TX FIFO flush may be required. Controller also has the capability to send a manual (software/firmware) ACK/NACK. Refer to section Section 19.3.2.14.5 for more details. IP doesn't generate a STOP on every NACK.

- Generate a STOP when NACK received during Tx operation
- Don't generate a STOP during Rx on a NACK

19.3.2.5 Repeated Start

The direction of data flow on SDA can be changed by the controller, without first stopping a transfer, by issuing a repeated START condition. This is called a RESTART. After a RESTART is issued, the Target address is again sent out with the new data direction specified by the R/W bit.

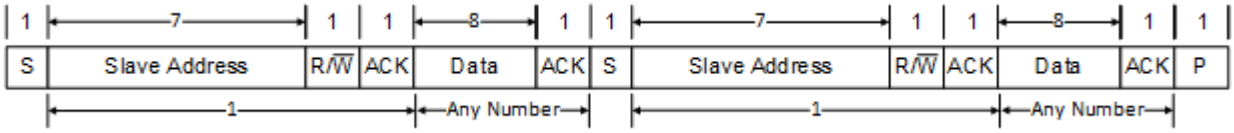


Figure 19-17. Repeated start format

A repeated start sequence for a ***Controller transmit*** is as follows:

- When the device is in the idle state, the Controller writes the Target address to the CSA register and configures the DIR bit for the desired transfer type.
- Data is written to the TXDATA register.
- When the BUSY bit in the CSR register is 0, the BURSTRUN and START bit in the CCTR register need to be set to initiate a transfer.
- STOP bit needs to be 0
- Wait until the BUSY bit in the CSR register gets 0.
- The Controller does not generate a STOP condition but instead writes another Target address to the CSA register and then sets the BURSTRUN and START bit again with a write operation to initiate the repeated START.

A repeated start sequence for a ***Controller receive*** is similar:

- When the device is in idle, the Controller writes the Target address to the CSA register and configures the DIR bit for the desired transfer type.
- When the BUSY bit in the CSR register is 0, the BURSTRUN and START bit in the CCTR register need to be set to initiate a transfer.
- STOP bit needs to be 0
- The Controller reads data from the RXDATA register.
- Wait until the BUSY bit in the CSR register gets 0.
- The Controller does not generate a STOP condition but instead writes another Target address to the CSA register and then sets the BURSTRUN and START bit again with a write operation to initiate the repeated START.

19.3.2.6 Clock Stretching

The Clock Stretching can be disabled if no Targets on the bus support clock stretching, allowing the Controller to reach the maximum speed on the bus. Otherwise the clock may be slowed by a Target keeping the clock Low or due to the clock status detection delay within the I2C module.

To ensure compliance to the I2C specification, clock stretching needs to be enabled. Clock stretching is activated when either the RX FIFO full or TX FIFO empty is set.

Clock stretching support can be enabled or disabled by configuring the CLKSTRETCH bit within the I2C ControllerConfiguration Register (I2CCCR). In the Target, Clock stretching is signaled by the TREQ and RREQ bits of the I2C Target Status Register (I2CTSR).

Disable Target Clock Stretching

Some I2C devices do not support clock stretching. So, it is important for IP to not clock stretch if it is on a bus with non-clock stretch devices. This is to avoid complications inside such devices and breaking the communication.

Add TCTR.SCLKSTRETCH field at bit position TCTR[2] to enable or disable clock stretching in Target mode. Below is the expected behavior when clock stretching is disabled:

- When receiving, do not clock stretch if RX FIFO is full and retain the content of the FIFO while raising an overflow interrupt. Raise new Rx FIFO overflow interrupt (RX_OVFL_T) at bit position 29 of RIS
- When transmitting, do not clock stretch if TX FIFO is empty, let the FIFO underrun and send out stale data for Tx FIFO (oldest or newest as is easier for implementation). Raise new Tx FIFO underrun interrupt (TX_UNFL_T) at bit position 28 of RIS
- Software byte ACK is not allowed when TCTR.CLKSTRETCH bit is set i.e. TACKCTL has no effect

The above behavior requires Target FSM to never go in WAIT states.

19.3.2.7 Arbitration

A Controller may start a transfer only if the bus is idle. It's possible for two or more masters to generate a START condition within minimum hold time of the START condition. In these situations, an arbitration scheme takes place on the SDA line, while SCL is High. During arbitration, the first of the competing Controller devices to place a 1 (High) on SDA, while another Controller transmits a 0 (Low), switches off its data output stage and retires until the bus is idle again.

Arbitration can take place over several bits. Its first stage is a comparison of address bits, and if both masters are trying to address the same device, arbitration continues on to the comparison of data bits.

When an arbitration lost is detected the I2CTSR.TARBLST flag is set. It will be reset by the hardware with the next STOP condition detected on the bus. Additionally, the TARBLOST flags in INT_EVENTx.RIS registers are set.

If arbitration is lost when the I2C Controller has initiated a transfer, the application should execute the following steps to correctly handle the arbitration loss:

- Flush TX FIFO

- Clear and mask the TX Empty interrupt by the TXEMPTY bit through the IMASK and ICLR register.
- Once the bus is IDLE, the TXFIFO can be filled and enabled, the TXEMPTY bit can be unmasked and a new transaction can be initiated.

19.3.2.8 Multi-Controller mode

When operating in a Multi Controllersystem the I2Cx.CCR.MMST bit needs to be set.In Multi-Controllermode the SCL high time counts once the SCL line has been detected high. If not enabled, the high time counts as soon as the SCL line has been set high by the I2C controller which allows the I2C to reach the maximum by the I2Cx.CTPR register specified speed.

19.3.2.9 Glitch Suppression

The I2C module supports glitch suppression on the SCL and SDA lines to meet the 50ns glitch suppression as specified in the I2C specification.

Digital Glitch Filter

The GFSEL bits in the I2Cx.GFCTL register can be programmed to provide glitch suppression on the SCL and SDA lines and assure proper signal values. The glitch suppression value is in terms of the I2C functional clocks. All signals are delayed internally when glitch suppression is nonzero.

GFSEL bits value	Glitch Filter Width (in clock cycles). Clock referred here is functional clock which is the otuput of clock divider (refer to Table 19-1)
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	10
1010	12
1011	14
1100	16
1101	20
1110	24
1111	31

19.3.2.10 FIFO Operation

The receive-data register I2Cx.RXDATA is user accessible and contains the current character to be read from the RX FIFO stack. The last received character from the receive shift register will be push to the end of the FIFO Stack.

The transmit data register I2Cx.TXDATA is user accessible and holds the data last written data to the TX FIFO. The TX FIFO contains the data waiting to be moved into the transmit shift register and transmitted on SDA.

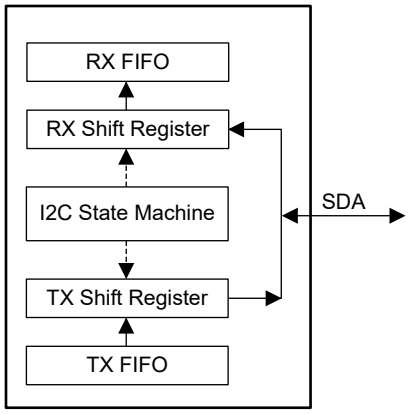


Figure 19-18. FIFO Operation

FIFOs are common for the Controller and Target receive and transmit. Each FIFO entry has a width of 8 bits and should be accessed in Byte mode. Each FIFO has a programmable threshold point (configured by RX/TXTRIG bits in the I2Cx.FIFOCTL registers) which indicates when the FIFO service interrupt should be generated. Additionally, a FIFO receive full and transmit empty interrupt can be enabled in the interrupt mask (IMASK) registers for the Controller and Target.

The content of the FIFO can be erased with setting TXFLUSH or RXFLUSH bit to 1 in the I2Cx.FIFOCTL registers. When the I2C gets reset the content of the FIFO needs also to be cleared.

Note

FIFO clear should only be executed while the I2C is in IDLE mode. Before triggering the flush, the FIFO interrupts should be disabled and after flush has completed the interrupt flags needs to be checked.

19.3.2.11 Burst Mode Operation

A burst mode is provided for the Controller module which allows a sequence of data transfers using the DMA or software to handle the data in the FIFO. The burst mode is enabled by setting the MBLEN bits in the Controller Control register I2Cx.CCTR to a value greater then '1'.

This sets the number of bytes transferred by a burst. A copy of this value is automatically written to the MBCNT bits in the I2C Controller Status register I2Cx.CSR to be used as a down-counter during the burst transfer. The bytes written to the I2C FIFO are transferred to the RX FIFO or TX FIFO depending on whether a transmit or receive is being executed.

If data is NACK'd during a BURST and the STOP bit is set in the I2Cx.CCTR register, the transfer terminates. If the STOP bit is not set, software must issue a STOP or repeated START when a NACK interrupt is asserted. In the case of a NACK, the MBCNT bits in the I2Cx.CSR register can be used to determine the amount of data that was transferred prior to the burst termination. If the address is NACK'd during a transfer, then a STOP is issued.

19.3.2.12 DMA Operation

The I2C provides an interface to the DMA controller with two separate channels. The DMA operation of the I2C is enabled through the I2C event and DMA peripheral registers. When the DMA functionality is enabled, the I2C asserts a DMA request on the selected channel when the associated FIFO can transfer data.

For the receive channel, a DMA transfer request is asserted whenever the amount of data in the receive FIFO is at or above the FIFO trigger level configured in the I2Cx.FIFOCTL register.

For the transmit channel, a request is asserted whenever the transmit FIFO contains fewer characters than the FIFO trigger level configured in the I2Cx.FIFOCTL register.

EVENT0 register are used to setup the trigger signaling for the DMA.This can be setup in a flexible way to trigger the DMA for Controller or Target and receive or transmit events. Software should avoid using the same trigger source for multiple EVENT lines concurrently.

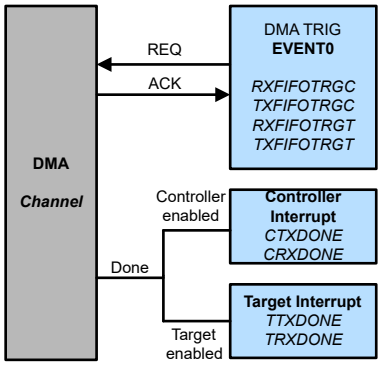


Figure 19-19. DMA Interface

19.3.2.13 Flush Stale Tx Data in Target Mode

Many use cases don't want to transmit leftover data of Target Tx FIFO from previous frame of in the next frame. To achieve this in current design, user has to rely on controlled single byte transfers to avoid putting extra data in FIFO. This limits throughout and introduces clock stretch every cycle. A mechanism in needed to flush stale data from Target Tx FIFO before starting a new transaction.

The CC35xx implements a solution to achieve this which gives the flexibility to choose whether to flush or not without adding new interrupt bits. The Target TXEMPTY interrupt is repurposed for this feature.

A status bit ***TSR.STALE_TXFIFO*** that tells the software whether the data present inside Target TX FIFO is stale or not.

A control bit ***TCTR.TXWAIT_STALE_FIFO*** to enable modified empty indication to Target logic - indicate empty to Target FSM when Tx FIFO is empty **OR** stale data present in Tx FIFO.

A control bit ***TCTR.TXEMPTY_ON_TREQ*** that allows RIS.STXEMPTY interrupt to be used for indicating TREQ condition i.e. the condition when SCL is being stretched waiting for transmit data from the Target.

19.3.2.13.1 Recommended Sequence

- When TCTR.TXWAIT_STALE_TXFIFO is set, on STOP, restart, or timeout, Target FSM gets an empty indication even though stale data is present inside Target Tx FIFO.
- Logic doesn't immediately generate an empty interrupt/DMA request. Instead, it waits until Controller asks for data from Target and then clock stretches.
- At this point Target issues clock stretch (TREQ) interrupt to CPU when TCTR.TXEMPTY_ON_TREQ is set.
- CPU in ISR checks for TSR.STALE_TXFIFO flag and flushes the FIFO using FIFOCTL.TXFLUSH – This also clears the status of TSR.STALE_TXFIFO

If the user wants to send the leftover data from previous frame in the next frame, it should clear the field ***TCTR.TXWAIT_STALE_TXFIFO.***

19.3.2.14 SMBUS 3.0 Support

The SMBus protocol reuses a number of features of I2C protocol such that the same controller can be used to support SMBUS as well. SMBUS protocol is used in a lot of industrial applications: Battery management system uses SMBUS for communication, Memory SSD system also use SMBUS for communication among others.

19.3.2.14.1 Quick Command

Quick Command is a simple, compact SMBus protocol that sends an address and 1-bit of data in the DIR bit of the I2C header byte to communicate a command to the Target, typically a "turn off" or "turn on". The I2C Controller peripheral has the ability to send a Quick Command by writing the target address and DIR value into

the CSA register followed by a write to the CCTR register with a value of 0x07 such that the MBLEN bit field is set to 0. The Target logic also has quick command support built in.

19.3.2.14.2 Acknowledge Control

The current IP provides software the capability to acknowledge the received transaction using TACKCTL register in the Target mode. This is limited in functionality and there is lack of ACK support in master.

To support host notify protocol, the IP implements default host address inside Target logic. For this, ***TCTR.EN_DEFHOSTADR*** bit is implemented. When this bit is set, default host address of **7'b000_1000** is always matched by the Target address match logic. When this bit is reset, the default host address is not matched.

19.3.2.14.3 Alert Response protocol

A Target-only device can signal the host through GPIO that it wants to transfer data. The host processes the interrupt and simultaneously accesses all compliant devices through the Alert Response Address. Only the device(s) which generated the request will acknowledge the Alert Response Address.

To support alert response protocol, the IP implements alert response address inside Target logic. For this, ***TCTR.EN_ALRESPADR*** bit is implemented. When this bit is set, alert response address of **7'b000_1100** is always matched by the Target address match logic. When this bit is reset, the alert response address is not matched.

19.3.2.14.4 Address Resolution Protocol

SMBus Target address conflicts can be resolved by dynamically assigning a new unique address to each Target device. The Address Resolution Protocol (ARP) is used for this.

ARP Flow

Step 1:Prepare to ARP

- Controller sends Prepare to ARP command to all the Targets on the bus by using Default Device Address
- All Targets will ACK this command and Targets will clear its own address
- All this can be done in software

Step 2: Get UDID

- Controller sends the Get UDID command to all the Targets on the bus
- All Targets return the unique UDID to controller
- Target arbitration happens since all Target are trying to send UDID to master. **This arbitration needs to happen in hardware.**

Step 3: Assign address

- Controller sends the Assign Address command to all the Targets.
- This command assigns an address to a specific device. Address ->UDID
- Controller will need to keep track of the used address pool and corresponding to UDID.
- All Targets will need to monitor the UDID bytes and if it matches then Target will change the own address to assigned address.
- This step can also be done in software

Repeat Step 2 and 3, till no Ack from the Target on Get UDID command. We can assume all ARP-capable devices have valid assigned Target addresses.

To support ARP, IP implements:

- Default device address inside Target logic. For this, EN_DEFDEVADR bit is implemented. When this bit is set, default device address of 7'b110_0001 is always matched by the Target address match logic. When this bit is reset, the default device address is not matched.
- Target arbitration. This is similar to the arbitration that happens currently inside the IP in Controller mode. If the arbitration is lost, TARBLOST interrupt is set.

19.3.2.14.5 Enhanced Acknowledge Control

The devices on the bus must have the capability to hold the bus after data reception and transmission and wait for software to acknowledge the transaction.

In Target mode, there are a number of software ACK controls implemented inside the IP in TACKCTL register.

TACKCTL.TACKOEN

This allows I2C Target to Not Acknowledge (NACK) for invalid data or command or Acknowledge (ACK) for valid data or command. The I2C clock is pulled low after the last data bit of the byte until Target_TACKCTL.ACKOVAL is written.

TACKCTL.ACKOEN_ON_START

When set this bit will automatically turn on the Target SACKOEN field following a Start Condition.

Sequence:

1. Set ACKOEN_ON_START to 1
2. The START bit is received which sets ACKOEN bit
3. Continue to receive bytes using software till remaining bytes are known
4. Reset ACKOEN to 0
5. Receive the rest of the frame using automatic hardware ACK till the next START

General Notes:

- S/W is allowed to ACK a byte and disabling ACKOEN in the same cycle by writing into TACKCTL register.
- But S/W is not allowed to NACK and disabling ACKOEN in the same cycle. In this case, S/W has to wait for a bit duration on NACK cycle before trying to disable TACKCTL.ACKOEN.

CCTR.TACKOEN

Similarly, the Controller in receive mode is capable of getting software ACK/NACK after ‘n’ number of bytes received.

When set and the Controller is receiving data and the number of bytes indicated in MBLEN have been received, the state machine will generate RXDONE interrupt and wait at the start of the ACK for FW/SW to indicate if an ACK or NACK should be sent. The ACK or NACK is selected by writing the CCTR.ACK bit and setting ACK accordingly. The software should write 1 to CCTR.STOP to stop the transaction. Otherwise, it can update the MBLEN to new value to continue with the transaction.

Note

The SCL High ***Bus Busy*** Timeout is different from SCL high Timeout. While SCL high Timeout counts only during active transactions, SCL High Busy Bust Timeout counts when the bus is IDLE. It also only affects the state of this status bit and doesn't generate any interrupt.

Both of them share the same s/w programmed count value.

SCL High ***Bus Busy*** Timeout counter enable condition is:

assign scl_high_bb_detect_en = enable_i & |scl_high_cnt_i & scl_i & idle_i & bus_busy_i & ~scl_high_bb_detect;

where,

enable_i= mmr_MASTER_I2CCCR_ACTIVE | mmr_Target_I2CTCTR_ACTIVE

scl_high_cnt_i = S/w programmed count value

scl_i = State of SCL line

idle_i = i2c_CSR_s[5] & ~i2c_sfsm_busy_o (IDLE status from Controllerand Target FSM)

bus_busy_i = State of this status bit

scl_high_timeout = Signal that flags a SCL high bus busy timeout event;

19.4 Initialization and Configuration

The following example shows how to configure the I2C module to transmit a single byte as a master. This assumes the functional clock is 20 MHz (80MHz peripherals clock is divided by 4).

- Select and configure the I2C clock using the CLKCTL and CLKDIV registers.
- Connect the SDA and SCL pins by configuring the IOMUX aperture
- Configure the SDA and SCL pins through their respective IOMUX PINCM registers as open-drain inputs.
- Initialize the I2C Controllerby writing the CCTR register with a value of 00000000h.
- Set the desired SCL clock speed of 100 kbps by writing the CTPR register with the correct value. The value written to the CTPR register represents the number of functional clock periods in one SCL clock period. The TPR value is determined by the following equation:

$$TPR = \frac{INT_{CLK}}{(SCL_{LP} + SCL_{HP}) \times SCL_{CLK}} - 1 \quad (10)$$

$$TPR = \frac{20\ MHz}{(6+4) \times 100000} - 1 \quad (11)$$

$$TPR = 19\ (0x13) \quad (12)$$

- Write the CTPR register with the value of 0x00000013.
- Specify the Target address and write mode (transmit) for the next operation by writing the CSA register with a value of 0x00000076. This sets the Target address to 0x3B and the DIR bit to 0x0.
- Place data (byte) to be transmitted in the data register by writing the TXDATA register with the desired data.
- Initiate a single byte transmit of the data from Controllerto Target by writing the CCTR register with a value of 0x00010007 (BLEN=1, STOP, START, BURSTRUN).
- Wait until the transmission completes by polling the CSR register's BUSY bit until it has been cleared.
- Check the ERROR bit in the CSR register to confirm the transmission was successful.

19.5 Interrupts

The I2C can generate interrupts when the following conditions are observed:

Table 19-3. Controller Mode Interrupts

0	CRXDONE	Controller Receive Transaction completed Interrupt
1	CTXDONE	Controller Transmit Transaction completed Interrupt
2	CRXFIFOTRG	RX FIFO trigger in controller modeTrigger when RX FIFO contains >= defined bytes
3	CTXFIFOTRG	TX FIFO Trigger in Transmit ModeTrigger when TX FIFO contains <= defined bytes
4	RXFIFOFULLC	RX FIFO full event in controller mode. This interrupt is set if an RX FIFO is full in controller mode.
5	TXEMPTYC	TX FIFO empty interrupt mask in controller mode. This interrupt is set if all data in the TX FIFO in controller mode have been shifted out and the transmit goes into idle mode.
6	CNACK	Address/Data NACK Interrupt
7	CSTART	START Detection Interrupt
8	CSTOP	STOP Detection Interrupt
9	CARBLOST	ControllerArbitration Lost Interrupt
10:15	Reserved	-

Table 19-4. Target Mode Interrupts

16	TRXDONE	Target Receive Data Interrupt
17	TTXDONE	Target Transmit Data Interrupt
18	TRXFIFOTRG	Target Receive FIFO Trigger.Trigger when RX FIFO contains >= defined bytes
19	TTXFIFOTRG	Target Transmit FIFO Trigger.Trigger when Transmit FIFO contains <= defined bytes
20	TXFIFOFULLT	RXFIFO full event in Target Mode. This interrupt is set if an RX FIFO is full.
21	TXEMPTYT	Transmit FIFO Empty interrupt in Target mode. This interrupt is set if all data in the Transmit FIFO have been shifted out and the transmit goes into idle mode.
22	TSTART	START Detection Interrupt
23	TSTOP	STOP Detection Interrupt
24	TGENCALL	General Call Interrupt
25	TX_UNFL_T	TX FIFO underflow in Target Mode
26	RX_OVFL_T	RX FIFO overflow in Target Mode
27	SARBLOST	Target Arbitration Lost
28:31	Reserved	-

19.6 I2C Registers

Table 19-5 lists the memory-mapped registers for the I2C registers. All register offset addresses not listed in Table 19-5 should be considered as reserved locations and the register contents should not be modified.

Table 19-5. I2C Registers

Offset	Acronym	Register Name	Section
100h	GFCTL	Glitch Filter Control	Section 19.6.1
104h	CSA	I2C Controller Target Address Register	Section 19.6.2
108h	CCTR	Host Control	Section 19.6.3
10Ch	CSR	Controller Status	Section 19.6.4
110h	CTPR	Timer Period	Section 19.6.5
114h	CCR	Controller Configuration	Section 19.6.6
118h	CBMON	Bus Signal Status	Section 19.6.7
11Ch	TOAR	Target Own Address	Section 19.6.8
120h	TOAR2	I2C Target Own Address 2	Section 19.6.9
124h	TCTR	I2C Target Control Register	Section 19.6.10
128h	TSR	I2C Target Status Register	Section 19.6.11
12Ch	RXDATA	Receive Data	Section 19.6.12
130h	TXDATA	Transmit Data	Section 19.6.13
134h	TACKCTL	Acknowledgment Control	Section 19.6.14
138h	FIFOCTL	FIFO Control	Section 19.6.15
13Ch	FIFOSR	FIFO Status	Section 19.6.16
140h	FCLKDIV	Clock Divider	Section 19.6.17
400h	PDBGCTL	Debug Control	Section 19.6.18
404h	EVENT0_IMASK	Interrupt Mask Register	Section 19.6.19
408h	EVENT0_RIS	Raw Interrupt Status	Section 19.6.20
40Ch	EVENT0_MIS	Masked Interrupt Status	Section 19.6.21
410h	EVENT0_IEN	Interrupt Enable	Section 19.6.22
414h	EVENT0_IDIS	Interrupt Disable	Section 19.6.23
418h	EVENT0_IMEN	Interrupt Mask Enable	Section 19.6.24
41Ch	EVENT0_IMDIS	Interrupt Disable	Section 19.6.25
420h	EVT_MODE	Event Mode Selection	Section 19.6.26
424h	DESC	Module Identification	Section 19.6.27
1000h	CLKCFG	Clock Configuration	Section 19.6.28

Complex bit access types are encoded to fit into small table cells. Table 19-6 shows the codes that are used for access types in this section.

Table 19-6. I2C Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

19.6.1 GFCTL Register (Offset = 100h) [Reset = 00000000h]

GFCTL is shown in Table 19-7.

Return to the Summary Table.

This register controls the glitch filter on the SCL and SDA lines

Table 19-7. GFCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3-0	GFSEL	R/W	0h	Glitch suppression pulse width This field controls the pulse width select for glitch suppression on the SCL and SDA lines. The following values are the glitch suppression values in terms of functional clocks. 0h = Bypass 1h = 1 clock 2h = 2 clocks 3h = 3 clocks 4h = 4 clocks 5h = 5 clocks 6h = 6 clocks 7h = 7 clocks 8h = 8 clocks 9h = 10 clocks Ah = 12 clocks Bh = 14 clocks Ch = 16 clocks Dh = 20 clocks Eh = 24 clocks Fh = 31 clocks

19.6.2 CSA Register (Offset = 104h) [Reset = 00000000h]

CSA is shown in Table 19-8.

Return to the Summary Table.

Controller target address register

Table 19-8. CSA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
15	CMODE	R/W	0h	This field selects the addressing mode(7-field/10-field) to be used in controller mode 0h = 7-field addressing mode 1h = 10-field addressing mode
14-11	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
10-1	TADDR	R/W	0h	*I2C* Target Address This field specifies bits A9 through A0 of the target address. In 7-field addressing mode as selected by MODE field, the top 3 bits are don't care 0h = Smallest value 3FFh = Highest possible value
0	DIR	R/W	0h	This field specifies if the next controller operation is a Receive or Transmit 0h = The controller is in transmit mode. 1h = The controller is in receive mode.

19.6.3 CCTR Register (Offset = 108h) [Reset = 00000000h]

CCTR is shown in Table 19-9.

Return to the Summary Table.

This control register configures the *I2C* controller operation. The START field generates the START or REPEATED START condition. The STOP field determines if the cycle stops at the end of the data cycle or continues to the next transfer cycle, which could be a repeated START. To generate a single transmit cycle, the *I2C* Controller Target Address CSA register is written with the desired address, the RS field is cleared, and this register is written with ACK = X (0 or 1), STOP = 1, START = 1, and RUN = 1 to perform the operation and stop. When the operation is completed (or aborted due an error), an byte transaction completed interrupt becomes active and the data may be read from the RXDATA register. When the I2C module operates in Controller receiver mode, a set ACK field causes the I2C bus controller to transmit an acknowledge automatically after each byte. This field must be cleared when the *I2C* bus controller requires no further data to be transmitted from the target transmitter.

Table 19-9. CCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
27-16	MBLEN	R/W	0h	Transaction length This field contains the programmed length of bytes of the Transaction. 0h = Smallest value FFFh = Highest possible value
15-6	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
5	RDONTXEMPTY	R/W	0h	Read on TXFIFO empty 0h = No special behaviour 1h = When 1 the controller will transmit all bytes from the TX FIFO before continuing with the programmed Burst Run Read. If the DIR is not set to read, then this field is ignored. The Start must be set in the CCTR for proper *I2C* protocol. The controller will first send the Start Condition, *I2C* Address with R/W field set to write, before sending the bytes in the TX FIFO. When the TX FIFO is empty, the *I2C* transaction will continue as programmed in CCTR and CSA without sending a Stop Condition. This is intended to be used to perform simple *I2C* command based reads transition that will complete after initiating them without having to get an interrupt to turn the bus around.
4	CACKOEN	R/W	0h	Controller ACK overrride enable 0h = No special behavior 1h = When 1 and the controller is receiving data and the number of bytes indicated in MBLEN have been received, the state machine will generate an rxdone interrupt and wait at the start of the ACK for FW to indicate if an ACK or NACK should be sent. The ACK or NACK is selected by writing the CCTR register and setting ACK accordingly. The other fields in this register can also be written at this time to continue on with the transaction. If a NACK is sent the state machine will automatically send a Stop.
3	ACK	R/W	0h	Data Acknowledge Enable. Configure this field to send the ACK or NACK. 0h = The last received data byte of a transaction is not acknowledged automatically by the controller. 1h = The last received data byte of a transaction is acknowledged automatically by the controller.
2	STOP	R/W	0h	Generate STOP 0h = The controller does not generate the STOP condition. 1h = The controller generates the STOP condition

Table 19-9. CCTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	START	R/W	0h	Generate START 0h = The controller does not generate the START condition. 1h = The controller generates the START or repeated START condition
0	BURSTRUN	R/W	0h	Controller enable and start transaction 0h = In standard mode, the controller will be unable to transmit or receive data. 1h = The controller will be able to transmit or receive data

19.6.4 CSR Register (Offset = 10Ch) [Reset = 00000000h]

CSR is shown in Table 19-10.

Return to the Summary Table.

The status register indicates the state of the bus controller.

Table 19-10. CSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
27-16	CBCNT	R	0h	Controller Transaction Count This field contains the current count-down value of the transaction. 0h = Smallest value FFFh = Highest possible value
15-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	BUSBSY	R	0h	Bus is busy Controller state machine will wait until this field is cleared before starting a transaction. When first enabling the controller in multi controller environments, FW should wait for one I2C clock period after setting ACTIVE high before writing to the CCTR register to start the transaction so that if SCL goes low it will trigger the BUSBSY. 0h = The bus is idle. 1h = This Status field is set on a START or when SCL goes low. It is cleared on a STOP, or when a SCL high bus busy timeout occurs and SCL and SDA are both high. This status is cleared when the ACTIVE field is low. Note that the controller state machine will wait until this field is cleared before starting a transaction. When first enabling the controller in multi controller environments, FW should wait for one I2C clock period after setting ACTIVE high before writing to the CCTR register to start the transaction so that if SCL goes low it will trigger the BUSBSY.
5	IDLE	R	1h	*I2C* Idle 0h = The controller is not idle. 1h = The controller is idle.
4	ARBLST	R	0h	Arbitration lost 0h = The controller won arbitration. 1h = The controller lost arbitration.
3	DATACK	R	0h	Acknowledge data 0h = The transmitted data was acknowledged 1h = The transmitted data was not acknowledged.
2	ADRACK	R	0h	Acknowledge address 0h = The transmitted address was acknowledged 1h = The transmitted address was not acknowledged.
1	ERR	R	0h	Error The error can be from the target address not being acknowledged or the transmit data not being acknowledged. 0h = No error was detected on the last operation. 1h = An error occurred on the last operation.
0	BUSY	R	0h	Controller FSM busy The field is set during an ongoing transaction, so is set during the transmit/receive of the amount of data set in MBLEN including START, RESTART, Address and STOP signal generation when required for the current transaction. 0h = The controller is idle. 1h = The controller is busy.

19.6.5 CTPR Register (Offset = 110h) [Reset = 00000001h]

CTPR is shown in Table 19-11.

Return to the Summary Table.

This register is programmed to set the timer period for the SCL clock and assign the SCL clock to standard mode.

Table 19-11. CTPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6-0	TPR	R/W	1h	Timer Period This field is used in the equation to configure SCL_PERIOD : SCL_PERIOD = (1 + TPR) x (SCL_LP + SCL_HP) x INT_CLK_PRD where: SCL_PRD is the SCL line period (I2C clock). TPR is the Timer Period register value (range of 1 to 127). SCL_LP is the SCL Low period (fixed at 6). SCL_HP is the SCL High period (fixed at 4). INT_CLK_PRD is the functional clock period in ns. Note: INT_CLK_PRD is based on divider value selected in [FCLK_DIV:FCLK:DIV] 0h = Smallest value 7Fh = Highest possible value

19.6.6 CCR Register (Offset = 114h) [Reset = 00000000h]

CCR is shown in Table 19-12.

Return to the Summary Table.

Controller configuration register

Table 19-12. CCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reads to this field return zero.Writes to this field are ignored.
8	LPBK	R/W	0h	I2C Loopback 0h = Normal operation. 1h = The controller in a test mode loopback configuration.
7-3	RESERVED	R	0h	Reads to this field return zero.Writes to this field are ignored.
2	CLKSTRETCH	R/W	0h	Clock Stretching. This field controls the support for clock stretching of the *I2C* bus. 0h = Disables the clock stretching detection. This can be disabled if no target on the bus does support clock streching, so that the maximum speed on the bus can be reached. 1h = Enables the clock stretching detection. Enabling the clock strechting ensures compliance to the I2C standard but could limit the speed due the clock stretching.
1	MCST	R/W	0h	Multicontroller mode. In Multicontroller mode the SCL high time counts once the SCL line has been detected high. If this is not enabled the high time counts as soon as the SCL line has been set high by the *I2C* controller. 0h = Disable Multicontroller mode. 1h = Enable Multicontroller mode.
0	ACTIVE	R/W	0h	Device Active After this field has been set, it should not be set again unless it has been cleared by writing a 0 or by a reset, otherwise transfer failures may occur. 0h = Disables the *I2C* controller operation. 1h = Enables the *I2C* controller operation.

19.6.7 CBMON Register (Offset = 118h) [Reset = 00000003h]

CBMON is shown in Table 19-13.

Return to the Summary Table.

This register is used to determine the SCL and SDA signal status.

Table 19-13. CBMON Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	SDA	R	1h	SDA status 0h = The SDA signal is low. 1h = The SDA signal is high. Note: During and right after reset, the SDA pin is in GPIO input mode without the internal pull enabled. For proper *I2C* operation, the user should have the external pull-up resistor in place.
0	SCL	R	1h	SCL status 0h = The SCL signal is low. 1h = The SCL signal is high Note: During and right after reset, the SCL pin is in GPIO input mode without the internal pull enabled. For proper *I2C* operation, the user should have the external pull-up resistor in place.

19.6.8 TOAR Register (Offset = 11Ch) [Reset = 00004000h]

TOAR is shown in Table 19-14.

Return to the Summary Table.

This register consists of seven address bits that identify the I2C device on the I2C bus.

Table 19-14. TOAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
15	MODE	R/W	0h	This field selects the addressing mode(7-field/10-field) to be used in target mode. 0h = Enable 7-field addressing 1h = Enable 10-field addressing
14	OAREN	R/W	1h	Target own address enable 0h = Disable OAR address 1h = Enable OAR address
13-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9-0	OAR	R/W	0h	Target own address: This field specifies bits A9 through A0 of the target address. In 7-field addressing mode as selected by MODE field, the top 3 bits are don't care 0h = Smallest value 3FFh = Highest possible value

19.6.9 TOAR2 Register (Offset = 120h) [Reset = 00000000h]

TOAR2 is shown in Table 19-15.

Return to the Summary Table.

This register consists of seven address bits that identify the alternate address for the *I2C* device on the *I2C* bus.

Table 19-15. TOAR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
22-16	OAR2_MASK	R/W	0h	Target own address 2 mask: This field specifies bits A6 through A0 of the target address. The bits with value '1' in this field will make the corresponding incoming address bits to match by default regardless of the value inside this field i.e. corresponding bits of this field are don't care. 0h = Minimum Value 7Fh = Maximum Value
15-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	OAR2EN	R/W	0h	Target own address 2 enable 0h = The alternate address is disabled. 1h = Enables the use of the alternate address in the OAR2 field.
6-0	OAR2	R/W	0h	Target own address 2 This field specifies the alternate target own address. 0h = Smallest value 7Fh = Highest possible value

19.6.10 TCTR Register (Offset = 124h) [Reset = 00000004h]

TCTR is shown in Table 19-16.

Return to the Summary Table.

Target control register

Table 19-16. TCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	ENDEFDEVADR	R/W	0h	Enable default device address 0h = When this field is 0, the default device address is not matched. NOTE: it may still be matched if programmed inside TOAR/TOAR2. 1h = When this field is 1, default device address of 7'h110_0001 is always matched by the target address match logic.
8	ENALRESPADR	R/W	0h	Enable alert response address 0h = The alert response address is not matched. NOTE: It may still be matched if programmed inside TOAR/TOAR2 1h = Alert response address of 7'h000_1100 is always matched by the target address match logic.
7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	RXFULLONRREQ	R/W	0h	Rx full interrupt generated based on RREQ filed. 0h = EVENT0_RIS.TRXFULL will be set when only the Target RX FIFO is full. This allows the EVENT0_RIS.TRXFULL interrupt to be used to indicate that the I2C bus is being clock stretched and that the FW must either read the RX FIFO or ACK/NACK the current RX byte. 1h = EVENT0_RIS.SRXFULL will be set when the target state machine is in the RX_WAIT or RX_ACK_WAIT states which occurs when the transaction is clock stretched because the RX FIFO is full or the ACKOEN has been set and the state machine is waiting for FW to ACK/NACK the current byte.
5	TXWAITSTALETXFIFO	R/W	0h	Tx transfer waits when stale data in Tx FIFO. This prevents stale bytes left in the TX FIFO from automatically being sent on the next I2C packet. Note: this should be used with [TCTR:TXEMPTY_ON_TREQ] set to prevent the Target State Machine from waiting for TX FIFO data without an interrupt notification when the FIFO data is stale. 0h = The TX FIFO empty signal to the Target State Machine indicates that the TX FIFO is empty. 1h = The TX FIFO empty signal to the Target State Machine will indicate that the TX FIFO is empty or that the TX FIFO data is stale. The TX FIFO data is determined to be stale when there is data in the TX FIFO when the target state machine leaves the TXMODE field. This can occur is a stop or timeout occur when there are bytes left in the TX FIFO.
4	TXTRIGXMODE	R/W	0h	Tx trigger when target FSM is in TX mode 0h = No special behavior 1h = EVENT0_RIS.TXFIFOTRG will be set when the Target TX FIFO has reached the trigger level AND the target state machine is in the as defined in the TXMODE field. When cleared EVENT0_RIS.TXFIFOTRG will be set when the Target TX FIFO is at or above the trigger level. This setting can be used to hold off the TX DMA until a transaction starts. This allows the DMA to be configured when the *I2C* is idle but have it wait till the transaction starts to load the Target TX FIFO, so it can load from a memory buffer that might be changing over time.

Table 19-16. TCTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TXEMPTYONTREQ	R/W	0h	Tx Empty Interrupt on TREQ 0h = EVENT0_RIS.TTXEMPTY will be set when only the target TX FIFO is empty. This allows the EVENT0_RIS.TTXEMPTY interrupt to be used to indicate that the bus is being clock stretched and that target TX data is required. 1h = EVENT0_RIS.STXEMPTY will be set when the Target State Machine is in the TX_WAIT state which occurs when the TX FIFO is empty and the transaction is clock stretched waiting for the FIFO to receive data.
2	CLKSTRETCH	R/W	1h	Target clock stretch enable 0h = Target clock stretching is disabled 1h = Target clock stretching is enabled
1	GENCALL	R/W	0h	General call response enable. 0h = Do not respond to a general call 1h = Respond to a general call
0	ACTIVE	R/W	0h	Device active. Setting this field enables the target functionality. 0h = Disables the target operation. 1h = Enables the target operation.

19.6.11 TSR Register (Offset = 128h) [Reset = 00000000h]

TSR is shown in Table 19-17.

Return to the Summary Table.

Target status register

Table 19-17. TSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
18-9	ADDRMATCH	R	0h	Indicates the address for which target address match happened 0h = Minimum Value 3FFh = Maximum Value
8	STALETXFIFO	R	0h	Stale TX FIFO 0h = Tx FIFO is not stale 1h = The TX FIFO is stale. This occurs when the TX FIFO was not emptied during the previous transaction.
7	TXMODE	R	0h	Target FSM is in TX MODE 0h = The target state machine is not in TX_DATA, TX_WAIT, TX_ACK or ADDR_ACK state with the bus direction set to read. 1h = The target state machine is in TX_DATA, TX_WAIT, TX_ACK or ADDR_ACK state with the bus direction set to read.
6	BUSBSY	R	0h	Bus is busy 0h = Bus is not busy 1h = Bus is busy. This is cleared on a timeout.
5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	OAR2SEL	R	0h	OAR2 address matched This field gets re-evaluated after every address comparison. 0h = Either the OAR2 address is not matched or the match is in legacy mode. 1h = OAR2 address matched and acknowledged by the target.
2	RXMODE	R	0h	Target FSM is in RX MODE 0h = The target state machine is not in the RX_DATA, RX_ACK, RX_WAIT, RX_ACK_WAIT or ADDR_ACK state with the bus direction set to write. 1h = The target state machine is in the RX_DATA, RX_ACK, RX_WAIT, RX_ACK_WAIT or ADDR_ACK state with the bus direction set to write.
1	TREQ	R	0h	Transmit Request 0h = No outstanding transmit request. 1h = The controller has been addressed as a target transmitter and is using clock stretching to delay the controller until data has been written to the TXDATA FIFO (Target TX FIFO is empty).
0	RREQ	R	0h	Receive Request 0h = No outstanding receive data. 1h = The controller has outstanding receive data and is using clock stretching to delay the controller until the data has been read from the RXDATA FIFO (target RX FIFO is full).

19.6.12 RXDATA Register (Offset = 12Ch) [Reset = 00000000h]

RXDATA is shown in Table 19-18.

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RX FIFO read data byte This field contains the current byte being read in the RX FIFO stack. If the FIFO is disabled, the data byte and status are stored in the receiving holding register (the bottom word of the receive FIFO). The received data can be retrieved by reading this register.

Table 19-18. RXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7-0	VALUE	R	0h	Received Data. This field contains the last received data. 0h = Smallest value FFh = Highest possible value

19.6.13 TXDATA Register (Offset = 130h) [Reset = 00000000h]

TXDATA is shown in Table 19-19.

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Transmit data register. This register is the transmit data register (the interface to the FIFOs). For transmitted data, if the FIFO is enabled, data written to this location is pushed onto the transmit FIFO. If the FIFO is disabled, data is stored in the transmitter holding register (the bottom word of the transmit FIFO).

Table 19-19. TXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7-0	VALUE	R/W	0h	Transmit data This byte contains the data to be transferred during the next transaction. 0h = Smallest value FFh = Highest possible value

19.6.14 TACKCTL Register (Offset = 134h) [Reset = 00000000h]

TACKCTL is shown in Table 19-20.

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This register enables the target to not acknowledge (NACK) for invalid data or command or acknowledge (ACK) for valid data or command. The *I2C* clock is pulled low after the last data field until this register is written.

Table 19-20. TACKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
2	ACKOENONSTART	R/W	0h	When set this field will automatically turn on the target ACKOEN field following a start condition. 0h = No special behavior 1h = When set this field will automatically turn on the Target ACKOEN field following a start condition.
1	ACKOVAL	R/W	0h	Target ACK override Value Note: For general call this field will be ignored if set to NACK and target continues to receive data. 0h = An ACK is sent indicating valid data or command. 1h = A NACK is sent indicating invalid data or command.
0	ACKOEN	R/W	0h	Target ACK override enable 0h = A response in not provided. 1h = An ACK or NACK is sent according to the value written to the ACKOVAL field.

19.6.15 FIFOCTL Register (Offset = 138h) [Reset = 00000000h]

FIFOCTL is shown in Table 19-21.

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Target FIFO control

Table 19-21. FIFOCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reads to this field return zero.Writes to this field are ignored.
15	RXFLUSH	R/W	0h	RX FIFO flush Setting this field will flush the RX FIFO. Before resetting this field to stop flush the RXFIFOCNT should be checked to be 0 and indicating that the flush has completed. 0h = Do not flush FIFO 1h = Flush FIFO
14-11	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
10-8	RXTRIG	R/W	0h	RX FIFO trigger Indicates at what fill level in the RX FIFO a trigger will be generated. Note: Programming this field to 0x0 has no effect since no data is present to transfer out of RX FIFO. 4h = Trigger when RX FIFO contains >= 5 byte 5h = Trigger when RX FIFO contains >= 6 byte 6h = Trigger when RX FIFO contains >= 7 byte 7h = Trigger when RX FIFO contains >= 8 byte
7	TXFLUSH	R/W	0h	TX FIFO flush Setting this field will flush the TX FIFO. Before resetting this field to stop flush the TXFIFOCNT should be checked to be 8 and indicating that the flush has completed. 0h = Do not flush FIFO 1h = flush FIFO
6-3	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
2-0	TXTRIG	R/W	0h	TX FIFO trigger Indicates at what fill level in the TX FIFO a trigger will be generated. 4h = Trigger when TX FIFO contains bigger or equal to 4 byte 5h = Trigger when TX FIFO contains bigger or equal to 5 byte 6h = Trigger when TX FIFO contains bigger or equal to 6 byte 7h = Trigger when TX FIFO contains bigger or equal to 7 byte

19.6.16 FIFOSR Register (Offset = 13Ch) [Reset = 00000800h]

FIFOSR is shown in Table 19-22.

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FIFO status register Note: This register should only be read when BUSY is 0

Table 19-22. FIFOSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
15	TXFLUSH	R	0h	TX FIFO flush When this field is set a flush operation for the TX FIFO is active. Clear TXFLUSH to stop. 0h = FIFO flush not active 1h = FIFO flush active
14-12	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
11-8	TXFIFOCNT	R	8h	Number of bytes which could be put into the TX FIFO 0h = Smallest value 8h = Highest possible value
7	RXFLUSH	R	0h	RX FIFO flush When this field is set a flush operation for the RX FIFO is active. Clear the RXFLUSH field to stop. 0h = FIFO flush not active 1h = FIFO flush active
6-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3-0	RXFIFOCNT	R	0h	Number of bytes which could be read from the RX FIFO 0h = Smallest value 8h = Highest possible value

19.6.17 FCLKDIV Register (Offset = 140h) [Reset = 00000000h]

FCLKDIV is shown in Table 19-23.

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Register for the selection of divider value to generate functional clock from SVT clock

Table 19-23. FCLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3-0	FCLKDIV	R/W	0h	Divider value selection 0h = Divide by 1 = 80MHz 1h = Divide by 2 = 40MHz 2h = Divide by 4 = 20MHz 3h = Divide by 5 = 16MHz 4h = Divide by 8 = 10MHz 5h = Divide by 10 = 8MHz 6h = Divide by 16 = 5MHz 7h = Divide by 20 = 4MHz 8h = Divide by 25 = 3.2MHz 9h = Divide by 32 = 2.5MHz Ah = Divide by 40 = 2MHz Bh = Divide by 80 = 1MHz

19.6.18 PDBGCTL Register (Offset = 400h) [Reset = 00000000h]

PDBGCTL is shown in Table 19-24.

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This register can be used by the software developer to control the behavior of the peripheral relative to the 'Core Halted' input

Table 19-24. PDBGCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	SOFT	R/W	1h	Soft halt boundary control. This function is only available, if FREE is set to 'STOP' 0h = The peripheral will halt immediately, even if the resultant state will result in corruption if the system is restarted 1h = The peripheral blocks the debug freeze until it has reached a boundary where it can resume without corruption
0	FREE	R/W	1h	Free run control 0h = The peripheral freezes functionality while the Core Halted input is asserted and resumes when it is deasserted. 1h = The peripheral ignores the state of the Core Halted input

19.6.19 EVENT0_IMASK Register (Offset = 404h) [Reset = 00000000h]

EVENT0_IMASK is shown in Table 19-25.

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Interrupt Mask. If a field is set, then corresponding interrupt is masked. Un-masking the interrupt causes the raw interrupt to be visible in [RIS], as well as [MIS].

Table 19-25. EVENT0_IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
27	TARBLOST	R/W	0h	Target arbitration lost 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
26	RX_OVFL_T	R/W	0h	RX FIFO overflow in target mode 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
25	TX_UNFL_T	R/W	0h	TX FIFO underflow in target mode 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
24	TGENCALL	R/W	0h	General call interrupt 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
23	TSTOP	R/W	0h	Stop condition interrupt 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
22	TSTART	R/W	0h	Target start condition interrupt. Asserted when the received address matches the target address 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
21	TXEMPTYT	R/W	0h	TX FIFO empty interrupt mask in target mode. This interrupt is set if all data in the Transmit FIFO in target mode have been shifted out and the transmit goes into idle mode. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
20	RXFIFOFULLT	R/W	0h	RX FIFO full event. This interrupt is set if an target RX FIFO is full in target mode. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
19	TXFIFOTRGT	R/W	0h	TX FIFO trigger in target mode 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
18	RXFIFOTRGMT	R/W	0h	RX FIFO trigger in target mode 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
17	TTXDONE	R/W	0h	Target transmit transaction completed interrupt 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
16	TRXDONE	R/W	0h	Target receive data interrupt. Signals that a byte has been received 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
15-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	CARBLOST	R/W	0h	Arbitration lost interrupt 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
8	CSTOP	R/W	0h	STOP detection interrupt 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask

Table 19-25. EVENT0_IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CSTART	R/W	0h	START detection interrupt 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
6	CNACK	R/W	0h	Address/Data NACK interrupt 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
5	TXEMPTYC	R/W	0h	TXFIFO empty interrupt in controller mode. This interrupt is set if all data in the TX FIFO in controller mode have been shifted out and the transmit goes into idle mode. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
4	RXFIFOFULLC	R/W	0h	RXFIFO full event in controller mode. This interrupt is set if an RX FIFO is full in controller mode. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
3	TXFIFOTRGC	R/W	0h	Transmit FIFO trigger in controller mode Trigger when TX FIFO contains <= defined bytes 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
2	RXFIFOTRGC	R/W	0h	Receive FIFO trigger in controller code Trigger when RX FIFO contains >= defined bytes 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
1	CTXDONE	R/W	0h	Controller transmit transaction completed Interrupt 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
0	CRXDONE	R/W	0h	Controller receive transaction completed Interrupt 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask

19.6.20 EVENT0_RIS Register (Offset = 408h) [Reset = 00000000h]

EVENT0_RIS is shown in Table 19-26.

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Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the [ICLR] register field even if the corresponding [IMASK] field is not enabled.

Table 19-26. EVENT0_RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
27	TARBLOST	R	0 h	Target arbitration lost 0h = Interrupt did not occur 1h = Interrupt occured
26	RX_OVFL_T	R	0h	RX FIFO overflow in target mode 0h = Interrupt did not occur 1h = Interrupt Occured
25	TX_UNFL_T	R	0h	TX FIFO underflow in target mode 0h = Interrupt did not occur 1h = Interrupt occured
24	TGENCALL	R	0h	General call interrupt 0h = Interrupt did not occur 1h = Interrupt occured
23	TSTOP	R	0h	Stop condition interrupt 0h = Interrupt did not occur 1h = Interrupt occured
22	TSTART	R	0h	Target start condition interrupt.When the received address matches the target address, this interrupt asserted. 0h = Interrupt did not occur 1h = Interrupt occured
21	TXEMPTYT	R	0h	TX FIFO empty interrupt mask in target mode. This interrupt is set if all data in the TX FIFO in target mode have been shifted out and the transmit goes into idle mode. 0h = Interrupt did not occur 1h = Interrupt occured
20	RXFIFOFULLT	R	0h	RX FIFO full event in target mode. This interrupt is set if an RX FIFO is full in target mode. 0h = Interrupt did not occur 1h = Interrupt occured
19	TXFIFOTRGT	R	0h	TX FIFO trigger in target mode 0h = Interrupt did not occur 1h = Interrupt occured
18	RXFIFOTRGT	R	0h	RX FIFO trigger in target mode 0h = Interrupt did not occur 1h = Interrupt occured
17	TTXDONE	R	0h	Target transmit transaction completed interrupt 0h = Interrupt did not occur 1h = Interrupt occured
16	TRXDONE	R	0h	Target receive data interrupt. Signals that a byte has been received 0h = Interrupt did not occur 1h = Interrupt occured
15-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	CARBLOST	R	0h	Arbitration lost interrupt 0h = Interrupt did not occur 1h = Interrupt occured

Table 19-26. EVENT0_RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CSTOP	R	0h	STOP detection interrupt 0h = Interrupt did not occur 1h = Interrupt occured
7	CSTART	R	0h	START detection interrupt 0h = Interrupt did not occur 1h = Interrupt occured
6	CNACK	R	0h	Address/Data NACK interrupt 0h = Interrupt did not occur 1h = Interrupt occured
5	TXEMPTYC	R	0h	TX FIFO empty interrupt mask in controller mode. This interrupt is set if all data in the TX FIFO in controller mode have been shifted out and the transmit goes into idle mode. 0h = Interrupt did not occur 1h = Interrupt occured
4	RXFIFOFULLC	R	0h	RX FIFO full event in controller mode. This interrupt is set if an RX FIFO is full in controller mode. 0h = Interrupt did not occur 1h = Interrupt occured
3	TXFIFOTRGC	R	0h	TX FIFO Trigger in Transmit Mode Trigger when TX FIFO contains <= defined bytes 0h = Interrupt did not occur 1h = Interrupt occured
2	RXFIFOTRGC	R	0h	RX FIFO trigger in controller mode Trigger when RX FIFO contains >= defined bytes 0h = Interrupt did not occur 1h = Interrupt occured
1	CTXDONE	R	0h	Controller transmit transaction completed interrupt 0h = Interrupt did not occur 1h = Interrupt occured
0	CRXDONE	R	0h	Controller receive transaction completed interrupt 0h = Interrupt did not occur 1h = Interrupt occured

19.6.21 EVENT0_MIS Register (Offset = 40Ch) [Reset = 00000000h]

EVENT0_MIS is shown in Table 19-27.

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Masked interrupt status. This is an AND of the [IMASK] and [RIS] registers.

Table 19-27. EVENT0_MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
27	TARBLOST	R	0h	Target arbitration lost 0h = Clear interrupt mask 1h = Masked interrupt occured
26	TRX_OVFL	R	0h	RX FIFO overflow in target mode 0h = Masked Interrupt did not occur 1h = Masked interrupt occured
25	TTX_UNFL	R	0h	TX FIFO underflow in target mode 0h = Masked Interrupt did not occur 1h = Masked interrupt occured
24	TGENCALL	R	0h	General call interrupt 0h = Masked Interrupt did not occur 1h = Masked interrupt occured
23	TSTOP	R	0h	Target STOP detection interrupt 0h = Masked Interrupt did not occur 1h = Masked interrupt occured
22	TSTART	R	0h	Target start condition interrupt. Asserted when the received address matches the target address 0h = Masked Interrupt did not occur 1h = Masked interrupt occured
21	TXEMPTYT	R	0h	TX FIFO empty interrupt mask in target mode. This interrupt is set if all data in the TX FIFO in target mode have been shifted out and the transmit goes into idle mode. 0h = Masked Interrupt did not occur 1h = Masked interrupt occured
20	RXFIFOFULLT	R	0h	RXFIFO full event in Target mode. This interrupt is set if an RX FIFO is full in target mode. 0h = Masked Interrupt did not occur 1h = Masked interrupt occured
19	TXFIFOTRGT	R	0h	TX FIFO trigger in target mode 0h = Masked Interrupt did not occur 1h = Masked interrupt occured
18	RXFIFOTRGT	R	0h	Target RX FIFO trigger 0h = Masked Interrupt did not occur 1h = Masked interrupt occured
17	TTXDONE	R	0h	Target transmit transaction completed interrupt 0h = Masked Interrupt did not occur 1h = Masked interrupt occured
16	TRXDONE	R	0h	Target receive data interrupt. Signals that a byte has been received 0h = Masked Interrupt did not occur 1h = Masked interrupt occured
15-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	CARBLOST	R	0h	Arbitration lost interrupt 0h = Masked Interrupt did not occur 1h = Masked interrupt occured
8	CSTOP	R	0h	STOP detection interrupt 0h = Masked Interrupt did not occur 1h = Masked interrupt occured

Table 19-27. EVENT0_MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CSTART	R	0h	START detection interrupt 0h = Masked Interrupt did not occur 1h = Masked interrupt occured
6	CNACK	R	0h	Address/Data NACK interrupt 0h = Masked Interrupt did not occur 1h = Masked interrupt occured
5	TXEMPTYC	R	0h	TX FIFO Empty interrupt mask in controller mode. This interrupt is set if all data in the TX FIFO in controller mode have been shifted out and the transmit goes into idle mode. 0h = Masked Interrupt did not occur 1h = Masked interrupt occured
4	RXFIFOFULLC	R	0h	RX FIFO full event. This interrupt is set if the RX FIFO is full in controller mode. 0h = Masked Interrupt did not occur 1h = Masked interrupt occured
3	TXFIFOTRGC	R	0h	TX FIFO trigger in controller mode Trigger when TX FIFO contains <= defined bytes 0h = Masked Interrupt did not occur 1h = Masked interrupt occured
2	RXFIFOTRGC	R	0h	RX FIFO trigger in controller mode Trigger when RX FIFO contains >= defined bytes 0h = Masked Interrupt did not occur 1h = Masked interrupt occured
1	CTXDONE	R	0h	Controller transmit transaction completed interrupt 0h = Masked Interrupt did not occur 1h = Masked interrupt occured
0	CRXDONE	R	0h	Controller receive data interrupt 0h = Masked Interrupt did not occur 1h = Masked interrupt occured

19.6.22 EVENT0_IEN Register (Offset = 410h) [Reset = 00000000h]

EVENT0_IEN is shown in Table 19-28.

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Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a field in IEN will set the event and therefore the related RIS field also gets set. If the interrupt is enabled through the mask, then the corresponding MIS field is also set.

Table 19-28. EVENT0_IEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	W	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
27	TARBLOST	W	0h	Target arbitration lost 0h = Writing 0 has no effect 1h = Set Interrupt
26	RX_OVFL_T	W	0h	RX FIFO overflow in target mode 0h = Writing 0 has no effect 1h = Set Interrrupt
25	TX_UNFL_T	W	0h	TX FIFO underflow in target mode 0h = Writing 0 has no effect 1h = Set interrupt
24	TGENCALL	W	0h	General call interrupt 0h = Writing 0 has no effect 1h = Set Interrrupt
23	TSTOP	W	0h	Stop condition interrupt 0h = Writing 0 has no effect 1h = Set Interrrupt
22	TSTART	W	0h	Target start condition interrupt. Asserted when the received address matches the target address 0h = Writing 0 has no effect 1h = Set Interrrupt
21	TXEMPTYT	W	0h	TX FIFO empty interrupt mask in target mode. This interrupt is set if all data in the TX FIFO in target mode have been shifted out and the transmit goes into idle mode. 0h = Writing 0 has no effect 1h = Set Interrrupt
20	RXFIFOFULLT	W	0h	RXFIFO full event in Target mode. This interrupt is set if an RX FIFO is full in Target mode. 0h = Writing 0 has no effect 1h = Set Interrrupt
19	TXFIFOTRGT	W	0h	TX FIFO trigger in target mode 0h = Writing 0 has no effect 1h = Set Interrrupt
18	RXFIFOTRGT	W	0h	RX FIFO trigger in target mode 0h = Writing 0 has no effect 1h = Set Interrrupt
17	TTXDONE	W	0h	Target transmit transaction completed Interrupt 0h = Writing 0 has no effect 1h = Set Interrrupt
16	TRXDONE	W	0h	Target receive data interrupt. Signals that a byte has been received 0h = Writing 0 has no effect 1h = Set Interrrupt
15-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	CARBLOST	W	0h	Arbitration lost interrupt 0h = Writing 0 has no effect 1h = Set Interrrupt

Table 19-28. EVENT0_IEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CSTOP	W	0h	STOP detection interrupt 0h = Writing 0 has no effect 1h = Set Interrrupt
7	CSTART	W	0h	START detection interrupt 0h = Writing 0 has no effect 1h = Set Interrrupt
6	CNACK	W	0h	Address/Data NACK interrupt 0h = Writing 0 has no effect 1h = Set Interrrupt
5	TXEMPTYC	W	0h	TX FIFO empty interrupt mask in controller mode. This interrupt is set if all data in the TX FIFO in controller mode have been shifted out and the transmit goes into idle mode. 0h = Writing 0 has no effect 1h = Set Interrrupt
4	RXFIFOFULLC	W	0h	RXFIFO full event in controller mode. 0h = Writing 0 has no effect 1h = Set Interrrupt
3	TXFIFOTRGC	W	0h	TX FIFO trigger in controller mode Trigger when TX FIFO contains <= defined bytes 0h = Writing 0 has no effect 1h = Set Interrrupt
2	RXFIFOTRGC	W	0h	RX FIFO trigger in controller mode Trigger when RX FIFO contains >= defined bytes 0h = Writing 0 has no effect 1h = Set Interrrupt
1	CTXDONE	W	0h	Controller transmit transaction completed interrupt 0h = Writing 0 has no effect 1h = Set Interrrupt
0	CRXDONE	W	0h	Controller receive data interrupt Signals that a byte has been received 0h = Writing 0 has no effect 1h = Set Interrrupt

19.6.23 EVENT0_IDIS Register (Offset = 414h) [Reset = 00000000h]

EVENT0_IDIS is shown in Table 19-29.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Table 19-29. EVENT0_IDIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
27	TARBLOST	W	0h	Target arbitration lost 0h = Writing 0 has no effect 1h = Clear Interrupt
26	RX_OVFL_T	W	0h	RX FIFO overflow in target mode 0h = Writing 0 has no effect 1h = Clear Interrupt
25	TX_UNFL_T	W	0h	TX FIFO underflow in target mode 0h = Writing 0 has no effect 1h = Clear Interrupt
24	TGENCALL	W	0h	General call interrupt 0h = Writing 0 has no effect 1h = Clear Interrupt
23	TSTOP	W	0h	Target STOP detection interrupt 0h = Writing 0 has no effect 1h = Clear Interrupt
22	TSTART	W	0h	Target start condition interrupt. Asserted when the received address matches the target address 0h = Writing 0 has no effect 1h = Clear Interrupt
21	TXEMPTYT	W	0h	TX FIFO empty interrupt mask in target mode. This interrupt is set if all data in the TX FIFO in target mode have been shifted out and the transmit goes into idle mode. 0h = Writing 0 has no effect 1h = Clear Interrupt
20	RXFIFOFULLT	W	0h	RXFIFO full event in target mode. This interrupt is set if an RX FIFO is full in target mode. 0h = Writing 0 has no effect 1h = Clear Interrupt
19	TXFIFOTRGT	W	0h	TX FIFO trigger in target mode 0h = Writing 0 has no effect 1h = Clear Interrupt
18	RXFIFOTRGT	W	0h	RX FIFO trigger in target mode 0h = Writing 0 has no effect 1h = Clear Interrupt
17	TTXDONE	W	0h	Target transmit transaction completed interrupt 0h = Writing 0 has no effect 1h = Clear Interrupt
16	TRXDONE	W	0h	Target receive data interrupt Signals that a byte has been received 0h = Writing 0 has no effect 1h = Clear Interrupt
15-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	CARBLOST	W	0h	Arbitration lost interrupt 0h = Writing 0 has no effect 1h = Clear Interrupt
8	CSTOP	W	0h	STOP detection interrupt 0h = Writing 0 has no effect 1h = Clear Interrupt

Table 19-29. EVENT0_IDIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CSTART	W	0h	START detection interrupt 0h = Writing 0 has no effect 1h = Clear Interrupt
6	CNACK	W	0h	Address/Data NACK interrupt 0h = Writing 0 has no effect 1h = Clear Interrupt
5	TXEMPTYC	W	0h	TX FIFO empty interrupt mask. This interrupt is set if all data in the TX FIFO have been shifted out and the transmit goes into idle mode. 0h = Writing 0 has no effect 1h = Clear Interrupt
4	RXFIFOFULLC	W	0h	RXFIFO full event in controller mode. 0h = Writing 0 has no effect 1h = Clear Interrupt
3	TXFIFOTRGC	W	0h	TX FIFO trigger in controller mode Trigger when TX FIFO contains <= defined bytes 0h = Writing 0 has no effect 1h = Clear Interrupt
2	RXFIFOTRGC	W	0h	RX FIFO trigger in controller mode Trigger when RX FIFO contains >= defined bytes 0h = Writing 0 has no effect 1h = Clear Interrupt
1	CTXDONE	W	0h	Controller transmit transaction completed interrupt 0h = Writing 0 has no effect 1h = Clear Interrupt
0	CRXDONE	W	0h	Controller receive data interrupt. Signals that a byte has been received 0h = Writing 0 has no effect 1h = Clear Interrupt

19.6.24 EVENT0_IMEN Register (Offset = 418h) [Reset = 00000000h]

EVENT0_IMEN is shown in Table 19-30.

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Interrupt mask set. Writing a 1 to a field in IMEN will set the related IMASK field.

Table 19-30. EVENT0_IMEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	W	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
27	TARBLOST	W	0h	Target srbitration lost 0h = Writing 0 has no effect 1h = Set masked interrrupt
26	RX_OVFL_T	W	0h	RX FIFO overflow in target mode 0h = Writing 0 has no effect 1h = Set masked interrrupt
25	TX_UNFL_T	W	0h	TX FIFO underflow in target mode 0h = Writing 0 has no effect 1h = Set masked interrrupt
24	TGENCALL	W	0h	General call interrupt 0h = Writing 0 has no effect 1h = Set masked interrrupt
23	TSTOP	W	0h	Stop condition interrupt 0h = Writing 0 has no effect 1h = Set masked interrrupt
22	TSTART	W	0h	Target start condition interrupt. Asserted when the received address matches the target address 0h = Writing 0 has no effect 1h = Set masked interrrupt
21	TXEMPTYT	W	0h	TX FIFO Empty interrupt mask in target mode. This interrupt is set if all data in the TX FIFO in target mode have been shifted out and the transmit goes into idle mode. 0h = Writing 0 has no effect 1h = Set masked interrrupt
20	RXFIFOFULLT	W	0h	RXFIFO full event in target mode. This interrupt is set if an RX FIFO is full in target mode. 0h = Writing 0 has no effect 1h = Set masked interrrupt
19	TXFIFOTRGST	W	0h	TX FIFO trigger in target mode 0h = Writing 0 has no effect 1h = Set masked interrrupt
18	RXFIFOTRGT	W	0h	RX FIFO trigger in target mode 0h = Writing 0 has no effect 1h = Set masked interrrupt
17	TTXDONE	W	0h	Target transmit transaction completed interrupt 0h = Writing 0 has no effect 1h = Set masked interrrupt
16	SRXDONE	W	0h	Target receive data interrupt. Signals that a byte has been received 0h = Writing 0 has no effect 1h = Set masked interrrupt
15-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	CARBLOST	W	0h	Arbitration lost interrupt 0h = Writing 0 has no effect 1h = Set masked interrrupt
8	CSTOP	W	0h	STOP detection interrupt 0h = Writing 0 has no effect 1h = Set masked interrrupt

Table 19-30. EVENT0_IMEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CSTART	W	0h	START detection interrupt 0h = Writing 0 has no effect 1h = Set masked interrrupt
6	CNACK	W	0h	Address/Data NACK interrupt 0h = Writing 0 has no effect 1h = Set masked interrrupt
5	TXEMPTYC	W	0h	TX FIFO empty interrupt mask in controller mode. This interrupt is set if all data in the TX FIFO in controller mode have been shifted out and the transmit goes into idle mode. 0h = Writing 0 has no effect 1h = Set masked interrrupt
4	RXFIFOFULLC	W	0h	RXFIFO full event in controller mode. 0h = Writing 0 has no effect 1h = Set masked interrrupt
3	TXFIFOTRGC	W	0h	TX FIFO trigger in Controller mode Trigger when TX FIFO contains <= defined bytes 0h = Writing 0 has no effect 1h = Set masked interrrupt
2	RXFIFOTRGC	W	0h	RX FIFO trigger in controller mode Trigger when RX FIFO contains >= defined bytes 0h = Writing 0 has no effect 1h = Set masked interrrupt
1	CTXDONE	W	0h	Controller transmit transaction completed interrupt 0h = Writing 0 has no effect 1h = Set masked interrrupt
0	CRXDONE	W	0h	Controller receive data interrupt. Signals that a byte has been received 0h = Writing 0 has no effect 1h = Set masked interrrupt

19.6.25 EVENT0_IMDIS Register (Offset = 41Ch) [Reset = 00000000h]

EVENT0_IMDIS is shown in Table 19-31.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Table 19-31. EVENT0_IMDIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
27	TARBLOST	W	0h	Target arbitration lost 0h = Writing 0 has no effect 1h = Clear masked interrupt
26	RX_OVFL_T	W	0h	RX FIFO overflow in target mode 0h = Writing 0 has no effect 1h = Clear masked interrupt
25	TX_UNFL_T	W	0h	TX FIFO underflow in target mode 0h = Writing 0 has no effect 1h = Clear masked interrupt
24	TGENCALL	W	0h	General call interrupt 0h = Writing 0 has no effect 1h = Clear masked interrupt
23	TSTOP	W	0h	Target STOP detection interrupt 0h = Writing 0 has no effect 1h = Clear masked interrupt
22	TSTART	W	0h	Target start condition interrupt. Asserted when the received address matches the target address. 0h = Writing 0 has no effect 1h = Clear masked interrupt
21	TXEMPTYT	W	0h	TX FIFO empty interrupt mask in target mode. This interrupt is set if all data in the TX FIFO in target mode have been shifted out and the transmit goes into idle mode. 0h = Writing 0 has no effect 1h = Clear masked interrupt
20	RXFIFOFULLT	W	0h	RXFIFO full event in target mode. This interrupt is set if an RX FIFO is full in target mode. 0h = Writing 0 has no effect 1h = Clear masked interrupt
19	TXFIFOTRGT	W	0h	TX FIFO trigger in target mode 0h = Writing 0 has no effect 1h = Clear masked interrupt
18	RXFIFOTRGT	W	0h	RX FIFO trigger in target mode 0h = Writing 0 has no effect 1h = Clear masked interrupt
17	TTXDONE	W	0h	Target transmit transaction completed interrupt 0h = Writing 0 has no effect 1h = Clear masked interrupt
16	TRXDONE	W	0h	Target receive data interrupt. Signals that a byte has been received 0h = Writing 0 has no effect 1h = Clear masked interrupt
15-10	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
9	CARBLOST	W	0h	Arbitration lost interrupt 0h = Writing 0 has no effect 1h = Clear masked interrupt
8	CSTOP	W	0h	STOP detection interrupt 0h = Writing 0 has no effect 1h = Clear masked interrupt

Table 19-31. EVENT0_IMDIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CSTART	W	0h	START detection interrupt 0h = Writing 0 has no effect 1h = Clear masked interrupt
6	CNACK	W	0h	Address/Data NACK interrupt 0h = Writing 0 has no effect 1h = Clear masked interrupt
5	TXEMPTYC	W	0h	TX FIFO empty interrupt mask. This interrupt is set if all data in the TX FIFO have been shifted out and the transmit goes into idle mode. 0h = Writing 0 has no effect 1h = Clear masked interrupt
4	RXFIFOFULLC	W	0h	RX FIFO full event in controller mode. 0h = Writing 0 has no effect 1h = Clear masked interrupt
3	TXFIFOTRGC	W	0h	TX FIFO trigger in controller mode Trigger when TX FIFO contains <= defined bytes 0h = Writing 0 has no effect 1h = Clear masked interrupt
2	RXFIFOTRGC	W	0h	RX FIFO trigger in controller mode Trigger when RX FIFO contains >= defined bytes 0h = Writing 0 has no effect 1h = Clear masked interrupt
1	CTXDONE	W	0h	Controller transmit transaction completed interrupt 0h = Writing 0 has no effect 1h = Clear masked interrupt
0	CRXDONE	W	0h	Controller receive data interrupt. Signals that a byte has been received 0h = Writing 0 has no effect 1h = Clear masked interrupt

19.6.26 EVT_MODE Register (Offset = 420h) [Reset = 00000000h]

EVT_MODE is shown in Table 19-32.

Return to the Summary Table.

Event mode register. It is used to select whether each line is disabled, in software mode (software clears the [RIS]) or in hardware mode (hardware clears the [RIS])

Table 19-32. EVT_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	
1-0	INT0_CFG	R	1h	Event line mode select for event corresponding to [INT_EVENT0] 0h = The interrupt or event line is disabled. 1h = The interrupt or event line is in software mode. Software must clear the RIS. 2h = The interrupt or event line is in hardware mode. The hardware (another module) clears automatically the associated RIS flag.

19.6.27 DESC Register (Offset = 424h) [Reset = 00000000h]

DESC is shown in Table 19-33.

Return to the Summary Table.

This register identifies the peripheral and its exact version.

Table 19-33. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODULEID	R	1511h	Module identification contains a unique peripheral identification number. The assignments are maintained in a central database for all of the platform modules to ensure uniqueness. 0h = Smallest value FFFFh = Highest possible value
15-12	FEATUREVER	R	0h	Feature Set for the module *instance* 0h = Smallest value Fh = Highest possible value
11-8	INSTNUM	R	0h	Instance Number within the device. This will be a parameter to the RTL for modules that can have multiple instances 0h = Smallest value Fh = Highest possible value
7-4	MAJREV	R	1h	Major rev of the IP 0h = Smallest value Fh = Highest possible value
3-0	MINREV	R	0h	Minor rev of the IP 0h = Smallest value Fh = Highest possible value

19.6.28 CLKCFG Register (Offset = 1000h) [Reset = 00000000h]

CLKCFG is shown in Table 19-34.

Return to the Summary Table.

This register controls the bus clock to *I2C*

Table 19-34. CLKCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reads to this field return zero.Writes to this field are ignored.
0	ENABLE	R/W	0h	This field enables or disables the bus clock to *I2C* 0h = I2C clock disabled 1h = I2C clock disabled

Chapter 20

Secure Digital Multimedia Card (SDMMC)

This chapter describes the SDMMC module of the device.

20.1 Introduction

20.1.1 SDMMC Features

The general features of the SDMMC host controller IP are:

- Built-in 1024-byte buffer for read or write
- 512 byte block size
- Single DMA channel, used for both RX and TX
- Clock support
  - up to 40MHz clock (5, 10, 20, or 40MHz) to SD card
  - up to 160Mbit/sec (20MByte/sec) in High-Speed SD mode 4-bit data transfer
  - up to 20Mbit/sec (2MByte/sec) in Default SD mode 1-bit data transfer
- Write Protect
- Card Detect
- Power Supply Control
- Support for SDA 3.0 Part A2 programming model
- Serial link supports full compliance with:
  - SD command/response sets as defined in the SD Physical Layer specification v2.00
  - SD Host Controller Standard Specification sets as defined in the SD card specification Part A2v2.00

20.1.2 Integration

This device contains one instance of the Secure Digital Multimedia Card (SDMMC) high speed interface. The controller provides an interface to a SD memory card.

The application interface is responsible for managing transaction semantics; the SDMMC host controller deals with SD protocol at transmission level, packing data, adding CRC, start/end bit and checking for syntactical correctness.

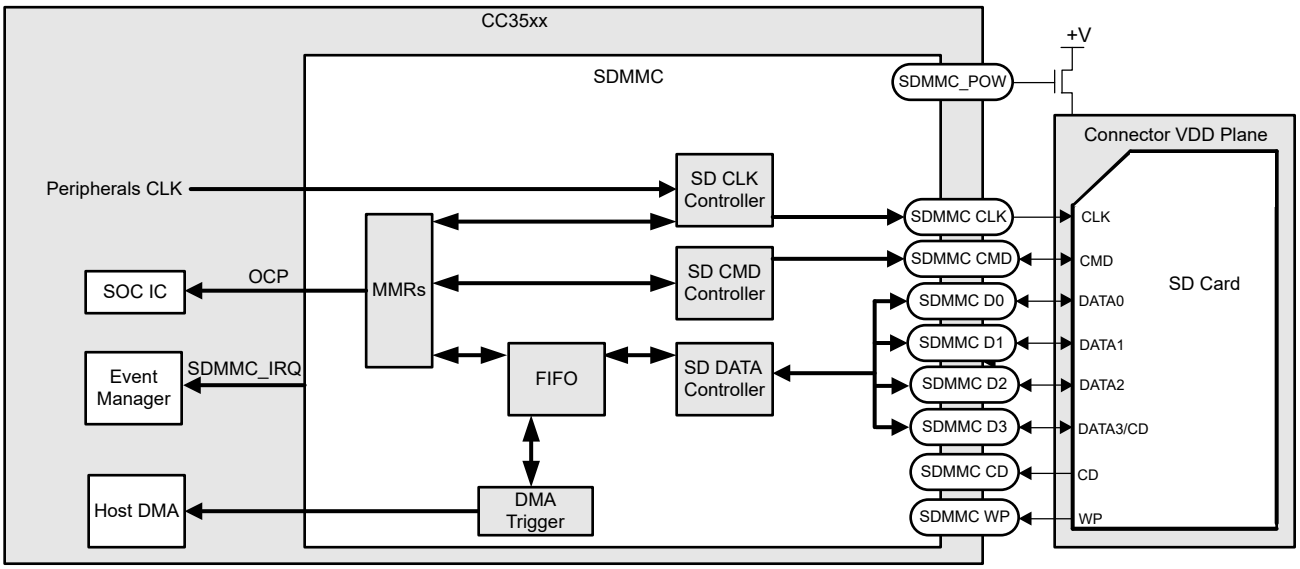

Figure 20-1. SD Card (4-bit) Application

Note

The SDMMC interface on the CC35xx is intended for embedded functions co-located on the same PCB with the device and not plug add-in cards.

SDMMC Connectivity Attributes

The general connectivity attributes for the three MMCHS modules are shown in Table 20-1.

Table 20-1. SDMMC Connectivity Attributes

Attributes	Type
Power Domain	Host Domain
Clock Domain	Peripherals clock
Reset Signals	Host_rstn
Interrupt Requests	1 interrupt per instance to Host MCU
DMA Requests	2 DMA requests per instance to single DMA channel (RX and TX request)

SDMMC Pin List

The SDMMC interface pins are summarized in Table 20-2.

Table 20-2. SDMMC Pin List

Pin	Type	Description
SDMMC_CLK	I/O (1)	SD serial clock input
SDMMC_CMD	I/O	SD command signal
SDMMC_DAT0	I/O	SD data signal
SDMMC_DAT1	I/O	SD data signal
SDMMC_DAT2	I/O	SD data signal
SDMMC_DAT3	I/O	SD data signal
SDMMC_POW	O	SD power supply control
SDMMC_CD	I	SD card detect (from connector)
SDMMC_WP	I	SD write protect (from connector)

(1) This output signal is also used as a retiming input.

The direction of the data lines depends on the selected data transfer mode as summarized in Table 20-3.

Table 20-3. DAT Line Direction for Data Transfer Modes

	SD 1-bit mode	SD 4-bit mode
DAT[0]	I/O	I/O
DAT[1]	I (1)	I/O
DAT[2]	I (1)	I/O
DAT[3]	I (1)	I/O

(1) Hi-Z to avoid bus conflict.

The direction of the SDMMC data buffers are controlled by ADPDATDIROQ signals. ADPDATDIROQ[i] =1 sets the corresponding DAT signal(s) in read position (input) and ADPDATDIROQ[i] = 0 sets thecorresponding DAT signal(s) in write position (output). Additionally, the ADPDATDIRLS signals areprovided (with opposite polarity) to control the direction of external level shifters. The value of thesecontrol signals for the various data modes are summarized in Table 20-4.

Table 20-4. ADPDATDIROQ and ADPDATDIRLS Signal States (1) (2) (3)

	SD 1-bit mode	SD 4-bit mode
DAT[0]	ADPDATDIRLS[0] =0 / 1 ADPDATDIROQ[0]= 1 / 0	ADPDATDIRLS[0] =0 / 1 ADPDATDIROQ[0]= 1 / 0
DAT[2]	ADPDATDIRLS[2] =0 ADPDATDIROQ[2]= 1	ADPDATDIRLS[2] =0 / 1 ADPDATDIROQ[2]= 1 / 0

Table 20-4. ADPDATDIROQ and ADPDATDIRLS Signal States [1] [2] [3] (continued)

	SD 1-bit mode	SD 4-bit mode
DAT[1]	ADPDATDIRLS[1] =0 ADPDATDIROQ[1]= 1	ADPDATDIRLS[1] =0 / 1 ADPDATDIROQ[1]= 1 / 0
DAT[3]		

(1) ADPDATDIRLSx = 0 for input and 1 for output — these signals are not pinned out on this device.
(2) ADPDATDIROQx = 0 for output and 1 for input.
(3) Grayed cells indicate that the data line is not used in the selected transfer mode.

20.2 Functional Description

One SDMMC can support one SD card.

20.2.1 SDMMC Functional Modes

20.2.1.1 SDMMC Connected to an SD Card

Figure 20-2 shows the SDMMC host controllers connected to an SD card and its related external connections.

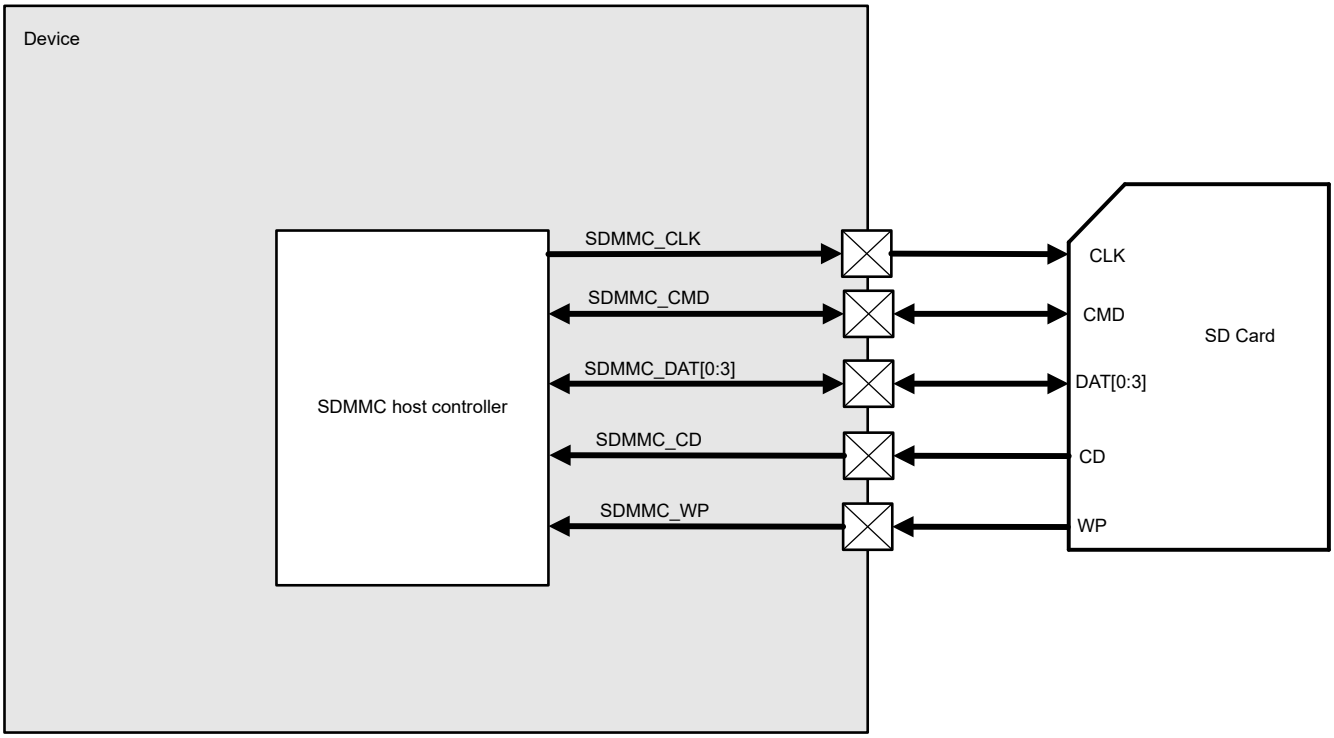

Figure 20-2. SDMMC connectivity to SD card

Figure 20-2 shows the SDMMC host controller connected to an SD card and its related external connections.

The following SDMMC pins are used

- **SDMMC_CMD** This pin is used for two-way communication between the connected card and the SDMMC. The SDMMC transmits commands to the card and thememory card drives responses to the commands on this pin.
- **SDMMC_DAT3-0** Depending on which type of card you are using, you may need to connect 1 or 4 data lines. The number of DAT pins (the data bus width) is set by the Data Transfer Width (DTW) bit in the SDMMC control register (SD_HCTL). For more information, see Section 20.4
- **SDMMC_CLK** This pin provides the clock to the memory card from the SD controller.
- **SDMMC_POW** Used for SD card's cards on/off power supply control. When high, denotes power-oncondition.

- **SDMMC_CD** This input pin serves as the SD carrier detect. This signal is received from amechanical switch on the slot.
- **SDMMC_WP** This input pin is used for the SD card's write protect. This signal is received from amechanical protect switch on the slot (system dependant). Applicable only for SD cards that have a mechanical sliding tablet on the side of the card.

Note

The SDMMC_CLK pin functions as an output but must be configured as an I/O to internally loopback the clock to time the inputs.

Table 20-5 provides a summary of these pins.

Table 20-5. SDMMC Pins and Descriptions

Pin	Type	1-Bit Mode	4-Bit Mode	Reset Value
SDMMC_CLK (1)	O	Clock Line	Clock Line	0
SDMMC_CMD	I/O	Command Line	Command Line	1
SDMMC_DAT0	I/O	Data Line 0	Data Line 0	1
SDMMC_DAT1	I/O	(not used)	Data Line 1	1
SDMMC_DAT2	I/O	(not used)	Data Line 2	1
SDMMC_DAT3	I/O	(not used)	Data Line 3	1

(1) The SDMMC_CLK pin functions as an output but must be configured as an I/O to internally loopback the clock to time the inputs.

20.2.1.2 Protocol and Data Format

The bus protocol between the SDMMC host controller and the card is message-based. Each message is represented by one of the following parts:

Command: A command starts an operation. The command is transferred serially from the SDMMC to the card on the sdmmc_cmd line.

Response: A response is an answer to a command. The response is sent from the card to the SDMMC. It is transferred serially on the sdmmc_cmd line.

Data: Data are transferred from the SDMMC to the card or from a card to the SDMMC using the DATA lines.

Busy: The sdmmc_dat0 signal is maintained low by the card as far as it is programming the data received.

CRC status: CRC result is sent by the card through the sdmmc_dat0 line when executing a write transfer. In the case of transmission error, occurring on any of the active data lines, the card sends a negative CRC status on sdmmc_dat0. In the case of successful transmission, over all active data lines, the card sends apositive CRC status on sdmmc_dat0 and starts the data programming procedure.

20.2.1.2.1 Protocol

The SDMMC module supports one type of data transfer: Block-oriented operation. There are specific commands for each type of operation. See the SD Memory Card Specifications for details about commands and programming sequences supported by the SD Card.

Figure 20-3 and Figure 20-4 show how multiple block-oriented operations are defined. A multiple block-oriented operation sends a data block plus CRC bits. The transfer terminates when a stop command follows on the sdmmc_cmd line. These operations are available for all kinds of cards.

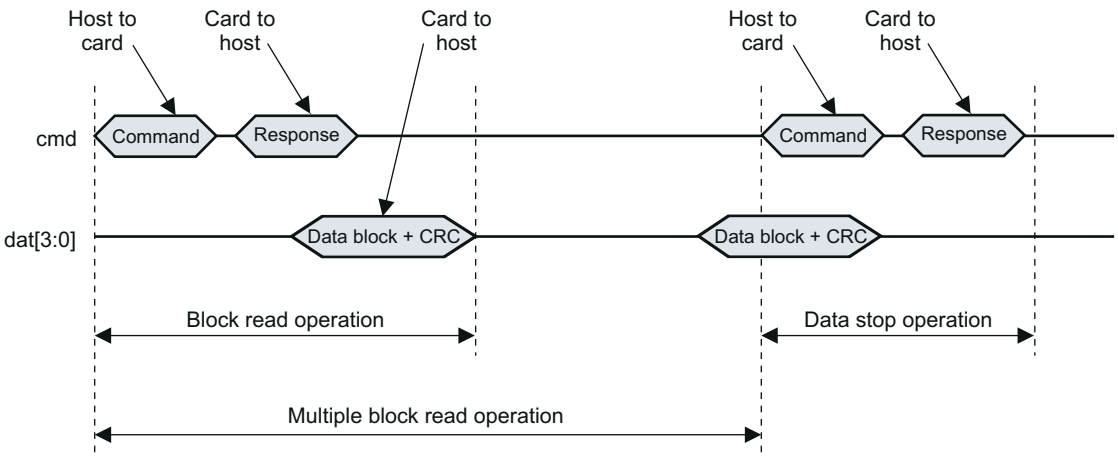

Figure 20-3. Multiple Block Read Operation

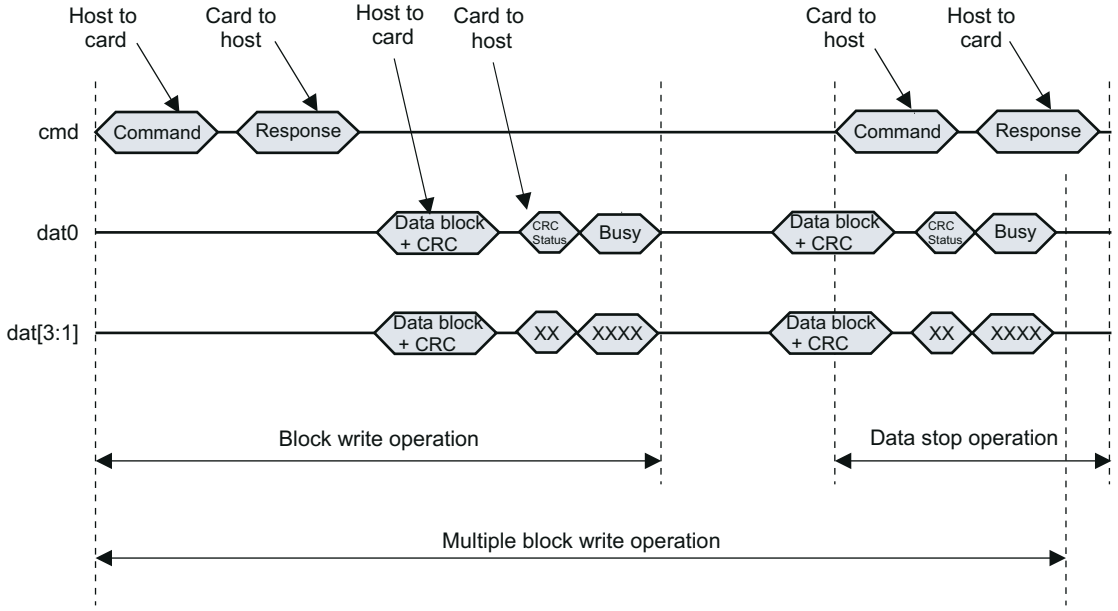

Figure 20-4. Multiple Block Write Operation

Note

1. The card busy signal is not always generated by the card; the previous examples showa particular case.
2. It is the software's responsibility to do a software reset after a data timeout to ensure that sdmmc_clk is stopped. The software reset is done by setting bit 26 in the SD_SYSCTL register to 1
3. For multiblock transfer you can abort a transfer without using a stop command. Use a CMD23 before a data transfer to define the number ofblocks that will be transferred, then the transfer stops automatically after the last block(provided the SD card supports this feature).

20.2.1.2.2 Data Format

Coding Scheme for Command Token

Command packets always start with 0 and end with 1. The second bit is a transmitter bit1 for a host command. The content is the command index (coded by 6 bits) and an argument (for example, an address), coded by 32 bits. The content is protected by 7-bit CRC checksum (see Figure 20-5).

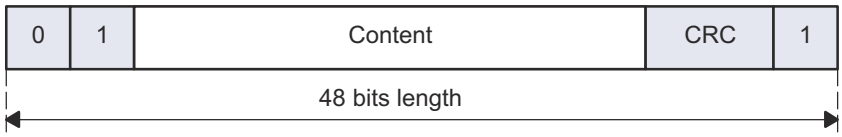

Figure 20-5. Command Token Format

Coding Scheme for Response Token

Response packets always start with 0 and end with a 1. The second bit is a transmitter bit0 for a card response. The content is different for each type of response (R1, R2, R3, R4, R5, and R6) and the content is protected by 7-bit CRC checksum. Depending on the type of commands sent to the card, the SD_CMD register must be configured differently to avoid false CRC or index errors to be flagged on command response (see Table 20-6). For more details about response types, see the SD Memory Card Specification.

Table 20-6. Response Type Summary

Response Type SD_CMD[17:16] RSP_TYPE	Index Check Enable SD_CMD[20] CICE	CRC Check Enable SD_CMD[19] CCCE	Name of Response Type
00	0	0	No Reponse
01	0	1	R2
10	0	0	R3, R4
10	1	1	R1, R6, R5, R7
11	1	1	R1b, R5b

Figure 20-6 and Figure 20-7 depict the 48-bit and 136-bit response packets.

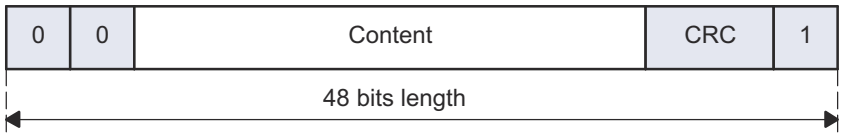

Figure 20-6. 48-Bit Response Packet (R1, R3, R4, R5, R6)

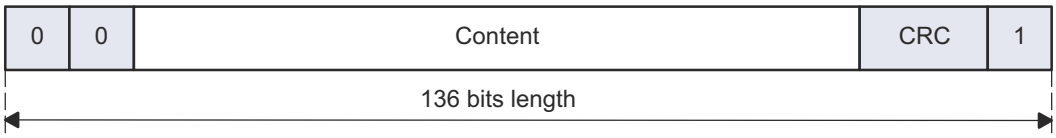

Figure 20-7. 136-Bit Response Packet (R2)

Coding Scheme for Data Token

Data tokens always start with 0 and end with 1 (see Figure 20-8 and Figure 20-9).

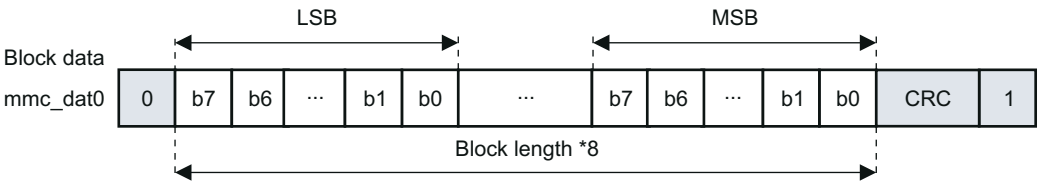

Figure 20-8. Data Packet for Block Transfer (1-Bit)

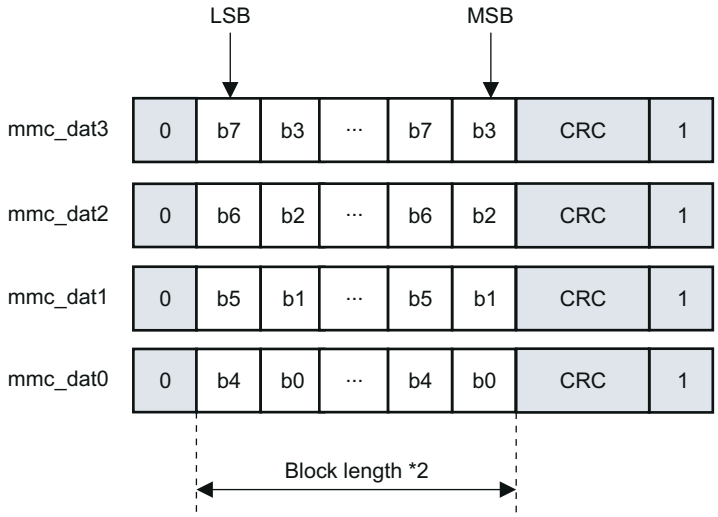

Figure 20-9. Data Packet for Block Transfer (4-Bit)

20.2.2 SD Card Feedback

There are two types of feedback received from the SD card to the SDMMC module, card detect and write protect.

Card detect indicates that the SD card is connected inside the slot. This feature is not supported in all slots. The SDMMC module has the ability to be configured to recognize rising edge or falling edge, depending on the SD slot used.

Write protect indicates that the SD card will not allow the SDMMC module to write to its memory card. This feature is not supported in all SD cards.

20.2.3 Resets

20.2.3.1 Hardware Reset

The module is reinitialized by the hardware.

The SD_SYSSTATUS[0] RESETDONE bit can be monitored by the software to check if the module is ready-to-use after a hardware reset.

This hardware reset signal has a global reset action on the module. All configuration registers and all state machines are reset in all clock domains.

20.2.3.2 Software Reset

The module is reinitialized by software through the SD_SYSCONFIG[1] SOFTRESET bit. This bit has the same action on the module logic as the hardware signal except for:

- Debounce logic
- SD_PSTATE, SD_CAPA, and SD_CUR_CAPA registers (see corresponding register descriptions)

The SOFTRESET bit is active high. The bit is automatically reinitialized to 0 by the hardware. The SD_SYSCTL[24] SRA bit has the same action as the SOFTRESET bit on the design.

The SD_SYSSTATUS[0] RESETDONE bit can be monitored by the software to check if the module is ready-to-use after a software reset.

Moreover, two partial software reset bits are provided:

- SD_SYSCTL[26] SRD bit
- SD_SYSCTL[25] SRC bit

These two reset bits are useful to reinitialize data or command processes respectively in case of line conflict. When set to 1, a reset process is automatically released when the reset completes:

- The SD_SYSCTL[26] SRD bit resets all finite state-machines and status management that handle data transfers on both the interface and functional side.
- The SD_SYSCTL[25] SRC bit resets all finite state-machines and status management that handle command transfers on both the interface and functional side.

Note

If any of the clock inputs are not present for the SDMMC peripheral, the software reset will not complete.

20.2.4 Interrupt Requests

Several internal module events can generate an interrupt. Each interrupt has a status bit, an interrupt enable bit, and a signal status enable:

- The status of each type of interrupt is automatically updated in the SD_STAT register; it indicates which service is required.
- The interrupt status enable bits of the SD_IE register enable/disable the automatic update of the SD_STAT register on an event-by-event basis.
- The interrupt signal enable bits of the SD_ISE register enable/disable the transmission of an interrupt request on the interrupt line SDMMC_IRQ (from the SDMMC host controller to the MPU subsystem interrupt controller) on an event-by-event basis.

If an interrupt status is disabled in the SD_IE register, then the corresponding interrupt request is not transmitted, and the value of the corresponding interrupt signal enable in the SD_ISE register is ignored.

When an interrupt event occurs, the corresponding status bit is automatically set to 1 (the SDMMC updates the status bit) in the SD_STAT register. If later a mask is applied on the interrupt inthe SD_ISE register, the interrupt request is deactivated.

When the interrupt source has not been serviced, if the interrupt status is cleared in the SD_STAT register and the corresponding mask is removed from the SD_ISE register, the interrupt status is not asserted again in the SD_STAT register and the SDMMC does not transmit an interrupt request.

CAUTION

If the buffer write ready interrupt (BWR) or the buffer read ready only interrupt (BRR) are not serviced and are cleared in the SD_STAT register, and the corresponding mask is removed, then the SDMMC will wait for the service of the interrupt without updating the status SD_STAT or transmitting an interrupt request.

Table 20-7 lists the event flags, and their mask, that can cause module interrupts.

Table 20-7. Events

Event Flag	Event Mask	Map To	Description
SD_STAT[29] BADA	SD_IE[29] BADA_ENABLE	SDMMC_IRQ	Bad Access to Data space. This bit is set automatically to indicate a bad access to buffer when not allowed. This bit is set during a read access to the data register (SD_DATA) while buffer reads are not allowed (SD_PSTATE[11] BRE=0). This bit is set during a write access to the data register (SD_DATA) while buffer writes are not allowed (SD_STATE[10]BWE=0)
SD_STAT[28] CERR	SD_IE[28] CERR_ENABLE	SDMMC_IRQ	Card Error. This bit is set automatically when there is at least one error in a response of type R1, R1b, R6, R5 or R5b. Only bits referenced as typeE(error) in status field in the response can set a card status error. An error bit in the response is flagged only if corresponding bit in card status response errors SD_CSRE is set. There is not card detection for auto CMD12 command.
SD_STAT[24] ACE	SD_IE[24] ACE_ENABLE	SDMMC_IRQ	Auto CMD12 error. This bit is set automatically when one of the bits in Auto CMD12 Error status register has changed from 0 to 1
SD_STAT[22] DEB	SD_IE[22] DEB_ENABLE	SDMMC_IRQ	Data End Bit error. This bit is set automatically when detecting a 0 at the end bit position of read data on DAT line or at the end position of the CRC status in write mode.
SD_STAT[21] DCRC	SD_IE[21] DCRC_ENABLE	SDMMC_IRQ	Data CRC error. This bit is set automatically when there is a CRC16 error in the data phase response following a block read command or if there is a 3-bit CRC status different of a position "010" token during a block write command.
SD_STAT[20] DTO	SD_IE[20] DTO_ENABLE	SDMMC_IRQ	Data Timeout error. This bit is set automatically according to the following conditions: A) busy timeout for R1b, R5b response. B) busy timeout after write CRC status. C) write CRC status timeout, or D) read data timeout.
SD_STAT[19] CIE	SD_IE[19] CIE_ENABLE	SDMMC_IRQ	Command Index Error. This bit is set automatically when response index differs from corresponding command index previously emitted. The check is enabled through SD_CMD[20] CICE bit.
SD_STAT[18] CEB	SD_IE[18] CEB_ENABLE	SDMMC_IRQ	Command End Bit error. This bit is set automatically when detecting a 0 at the end bit position of a command response.
SD_STAT[17] CCRC	SD_IE[17] CCRC_ENABLE	SDMMC_IRQ	Command CRC error. This bit is set automatically when there is a CRC7 error in the command response. CRC check is enabled through the SD_CMD[19] CCCE bit.
SD_STAT[16] CTO	SD_IE[16] CTO_ENABLE	SDMMC_IRQ	Command Timeout error. This bit is set automatically when no response is received within 64 clock cycles from the end bit of the command. For commands the reply within 5 clock cycles, the timeout is still detected at 64 clock cycles.
SD_STAT[15] ERRI	SD_IE[15] ERRI_ENABLE	SDMMC_IRQ	Error Interrupt. If any of the bits in the Error Interrupt Status register (SD_STAT[24:15]) are set, the this bit is set to 1.
SD_STAT[8] CIRQ	SD_IE[8] CIRQ_ENABLE	SDMMC_IRQ	Card Interrupt. This bit is only used for SD cards. In 1-bit mode, interrupt source is asynchronous (can be a source of asynchronous wake-up). In 4-bit mode, interrupt source is sampled during the interrupt cycle. In CE-ATA mode, interrupt source is detected when the card drive CMD line to zero during one cycle after data transmission end.
SD_STAT[7] CREM	SD_IE[7] CREM_ENABLE	SDMMC_IRQ	Card Removal. This bit is set automatically when SD_PSTATE[CINS] changes from 1 to 0. A clear of this bit doesn't affect Card inserted present state (SD_PSTATE[CINS]).
SD_STAT[6] CINS	SD_IE[6] CINS_ENABLE	SDMMC_IRQ	Card Insertion. This bit is set automatically when SD_PSTATE[CINS] changes from 0 to 1. A clear of this bit doesn't affect Card inserted present state (SD_PSTATE[CINS]).

Table 20-7. Events (continued)

Event Flag	Event Mask	Map To	Description
SD_STAT[5] BRR	SD_IE[5] BRR_ENABLE	SDMMC_IRQ	Buffer Read ready. This bit is set automatically during a read operation to the card when one block specified by SD_BLK[10:0] BLEN is completely written in the buffer. It indicates that the memory card has filled out the buffer and the local host needs to empty the buffer by reading it.
SD_STAT[4] BWR	SD_IE[4] BWR_ENABLE	SDMMC_IRQ	Buffer Write ready. This bit is automatically set during a write operation to the card when the host can write a complete block as specified by SD_BLK[10:0] BLEN. It indicates that the memory card has emptied one block from the bugger and the local host is able to write one block of data into the buffer.
SD_STAT[2] BGE	SD_IE[2] BGE_ENABLE	SDMMC_IRQ	Block Gap event. When a stop at block gap is requested (SD_HCTL[16] SBGR), this bit is automatically set when transaction is stopped at the block gap during a read or write operation.
SD_STAT[1] TC	SD_IE[1] TC_ENABLE	SDMMC_IRQ	Transfer completed. This bit is always set when a read/ write transfer is completed or between two blocks when the transfer is stopped due to a stop at block gap requested (SD_HCTL[16] SBGR). In read mode this bit is automatically set on completion of a read transfer (SD_PSTATE[9] RTA). In write mode, this bit is automatically set on completion of the DAT line use (SD_PSTATE[2] DLA).
SD_STAT[0] CC	SD_IE[0] CC_ENABLE	SDMMC_IRQ	Command complete. This bit is set when a 1-to-0 transition occurs in the register command inhibit (SD_PSTATE[0] CMDI). If the command is a type for which no response is expected, then the command complete interrupt is generated at the end of the command. A command timeout error (SD_STAT[16] CTO) has higher priority than command complete (SD_STAT[0] CC). If a response is expected but none is received, the a Command Timeout error is detected and signaled instead of the Command Complete interrupt.

20.2.4.1 Interrupt-Driven Operation

An interrupt enable bit must be set in the SD_IE register to enable the module internal source of interrupt.

When an interrupt event occurs, the single interrupt line is asserted and the SW must:

- Read the SD_STAT register to identify which event occurred.
- Write 1 into the corresponding bit of the SD_STAT register to clear the interrupt status and release the interrupt line (if a read is done after this write, this would return 0).

Note

In the SD_STAT register, Card Interrupt (CIRQ) and Error Interrupt (ERRI) bits cannot be cleared.

The SD_STAT[15] ERRI bit is automatically cleared when all status bits in SD_STAT[31:16]are cleared.

20.2.4.2 Polling

When the interrupt capability of an event is disabled in the SD_ISE register, the interrupt line is not asserted:

- Software can poll the status bit in the SD_STAT register to detect when the corresponding event occurs.
- Writing 1 into the corresponding bit of the SD_STAT register clears the interrupt status and does not affect the interrupt line state.

Note

Please see the note in Section 20.2.4.1 concerning CIRQ and ERRI bits clearing.

20.2.5 DMA Modes

The device supports DMA peripheral mode only. In this case, the controller is slave on DMA transaction managed by two separated requests (SDMAWREQN and SDMARREQN)

20.2.5.1 DMA Peripheral Mode Operations

The SDMMC can be interfaced with a DMA controller. At system level, the advantage is to discharge the SW of the data transfers.

The DMA request is issued if the following conditions are met:

- The SD_CMD[0] DE bit is set to 1 to trigger the initial DMA request (the write must be done when running the data transfer command).
- A command was emitted on the SD_cmd line.
- There is enough space in the buffer of the SDMMC to write an entire block (BLEN writes).

20.2.5.1.1 DMA Receive Mode

In a DMA block read operation (single or multiple), the request signal SDMARREQN is asserted to its active level when a complete block is written in the buffer. The block size transfer is specified in the SD_BLK[10:0] BLEN field.

The SDMARREQN signal is deasserted to its inactive level when the DMA has read one single word from the buffer. Only one request is sent per block; the DMA controller can make a 1-shot read access or several DMA bursts, in which case the DMA controller must manage the number of burst accesses, according to block size BLEN field.

New DMA requests are internally masked if the DMA has not read exactly BLEN bytes and a new complete block is not ready. As DMA accesses are in 32-bit, then the number of DMA read is Integer(BLEN/4)+1.

The receive buffer never overflows. In multiple block transfers for block size above 512 bytes, when the buffer gets full, the SDMMC_CLK clock signal (provided to the card) is momentarily stopped until the DMA or the MCU performs a read access, which reads a complete block in the buffer.

Figure 20-10 provides a summary:

- DMA transfer size = BLEN buffer size in one shot or by burst
- One DMA request per block

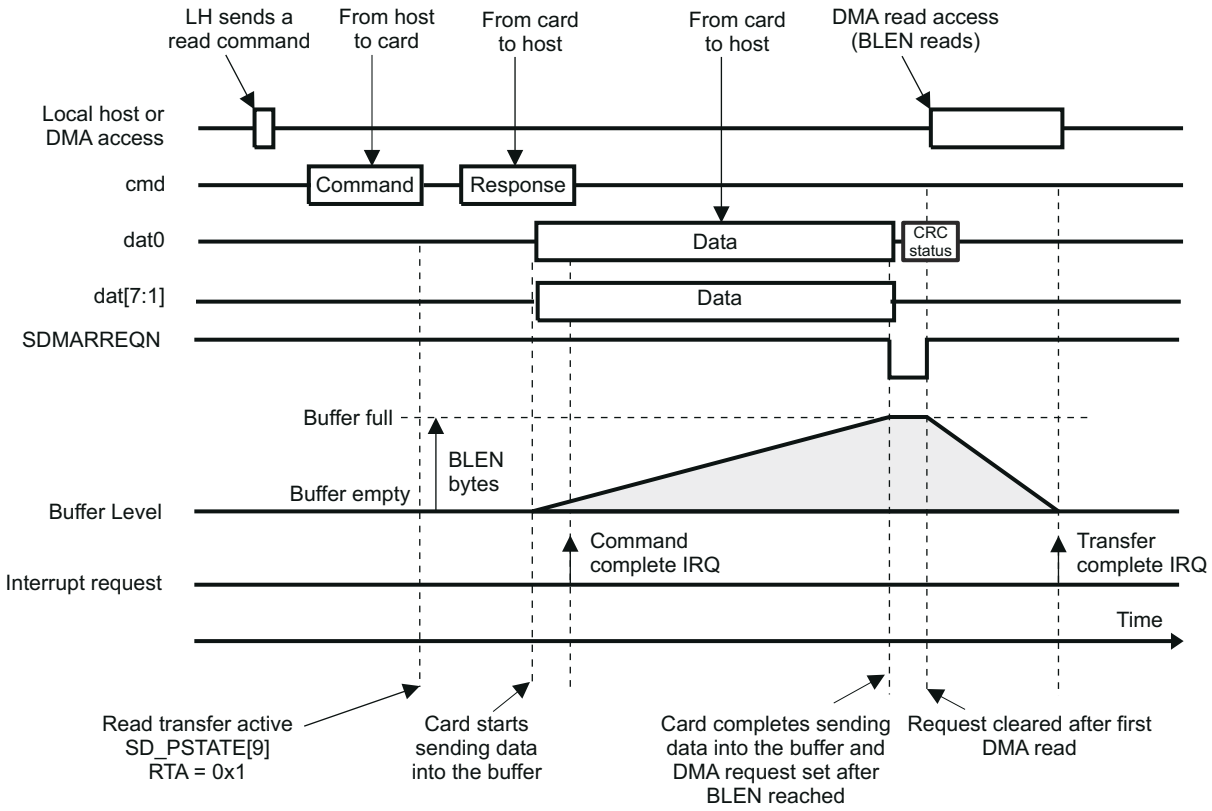

Figure 20-10. DMA Receive Mode

20.2.5.1.2 DMA Transmit Mode

In a DMA block write operation (single or multiple), the request signal SDMAWREQN is asserted to its active level when a complete block is to be written to the buffer. The block size transfer is specified in the SD_BLK[10:0] BLEN field.

The SDMAWREQN signal is deasserted to its inactive level when the DMA has written one single word to the buffer.

Only one request is sent per block; the DMA controller can make a 1-shot write access or multiple write DMA bursts, in which case the DMA controller must manage the number of burst accesses, according to block size BLEN field.

New DMA requests are internally masked if the DMA has not written exactly BLEN bytes (as DMA accesses are in 32-bit, then the number of DMA read is Integer(BLEN/4)+1) and if there is not enough memory space to write a complete block in the buffer.

Figure 20-11 provides a summary:

- DMA transfer size = BLEN buffer size in one shot or by burst
- One DMA request per block

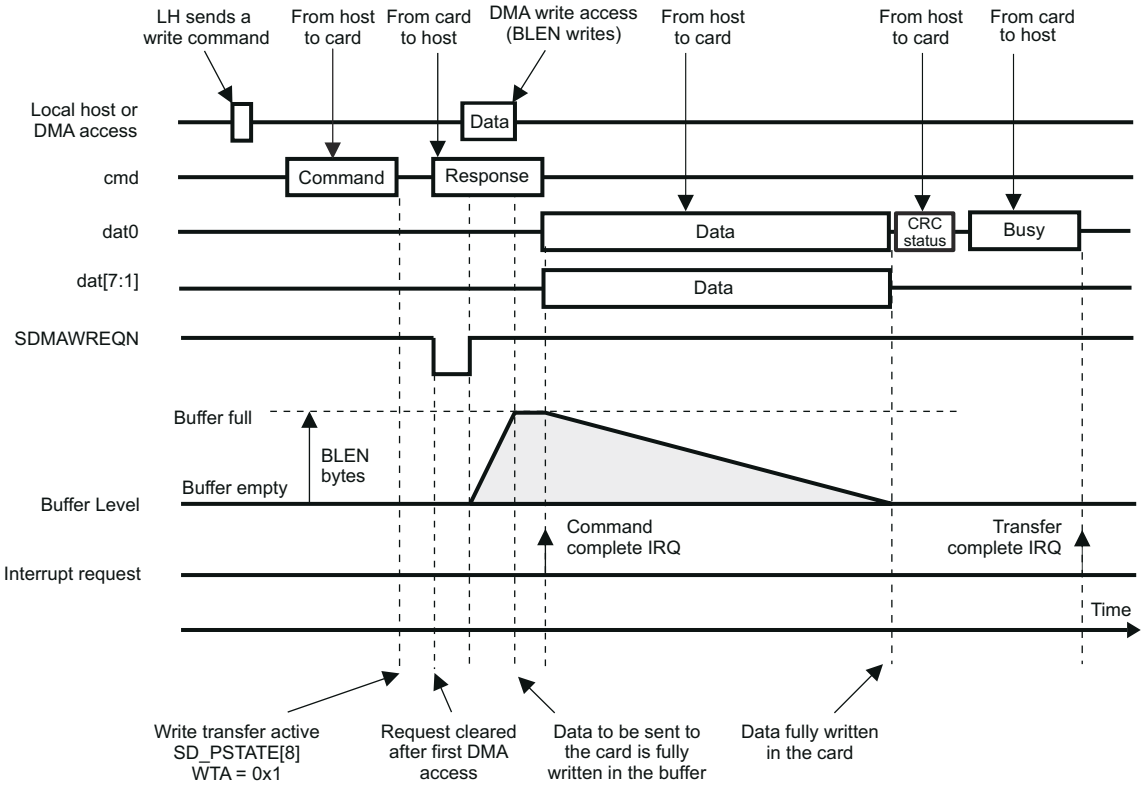

Figure 20-11. DMA Transmit Mode

20.2.6 Buffer Management

20.2.6.1 Data Buffer

The SDMMC uses a data buffer. This buffer transfers data from one data bus (Interconnect) to another data bus (SD card bus) and vice versa.

The buffer is the heart of the interface and ensures the transfer between the two interfaces (L4 and the card). To enhance performance, the data buffer is completed by a prefetch register and a post-write buffer that are not accessible by the host controller.

The read access time of the prefetch register is faster than the one of the data buffer. The prefetch register allows data to be read from the data buffer at an increased speed by preloading data into the prefetch register.

The entry point of the data buffer, the prefetch buffer, and the post-write buffer is the 32-bit register SD_DATA. A write access to the SD_DATA register followed by a read access from the SD_DATA register corresponds to a write access to the post-write buffer followed by a read access to the prefetch buffer. As a consequence, it is normal that the data of the write access to the SD_DATA register and the data of the read access to the SD_DATA register are different.

The number of 32-bit accesses to the SD_DATA register that are needed to read (or write) a data block with a size of SD_BLK[10:0] BLEN, and equals the rounded up result of BLEN divided by 4. The maximum block size supported by the host controller is hard-coded in the register SD_CAPA[17:16] MBL field and cannot be changed.

A read access to the SD_DATA register is allowed only when the buffer read enable status is set to 1 (SD_PSTATE[11] BRE); otherwise, a bad access (SD_STAT[29] BADA) is signaled.

A write access to the SD_DATA register is allowed only when the buffer write enable status is set to 1 (SD_PSTATE[10] BWE); otherwise, a bad access (SD_STAT[29] BADA) is signaled and the data is not written.

The data buffer has two modes of operation to store and read of the first and second portions of the data buffer:

- When the size of the data block to transfer is less than or equal to MEM_SIZE/2 (in double buffering), two data transfers can occur from one data bus to the other data bus and vice versa at the same time. The SDMMC uses the two portions of the data buffer in a ping-pong manner so that storing and reading of the first and second portions of the data buffer are automatically interchanged from time to time so that data may be read from one portion (for instance, through a DMA read access on the interconnect bus) while data (for instance, from the card) is being stored into the other portion and vice versa. When BLEN is less than or equal to 200h (that is, less or equal to 512Bytes), each of the two portions of the buffer that can be used have a size of BLEN (that is, 32-bits x BLEN div by 4). Not more than this total size of 2 times 32-bits × BLEN div by 4 can be used.
- When the size of the data block to transfer is larger than MEM_SIZE/2, only one data transfer can occur from one data bus to the other data bus at a time. The SDMMC uses the entire data buffer as a single portion. In this mode, a bad access (SD_STAT[29] BADA) is signaled when two data transfers occur from one data bus to the other data bus and vice versa at the same time.

CAUTION

The SD_CMD[4] DDIR bit must be configured before a transfer to indicate the direction of the transfer.

Figure 20-12 shows the buffer management for writing and Figure 20-13 shows the buffer management for reading.

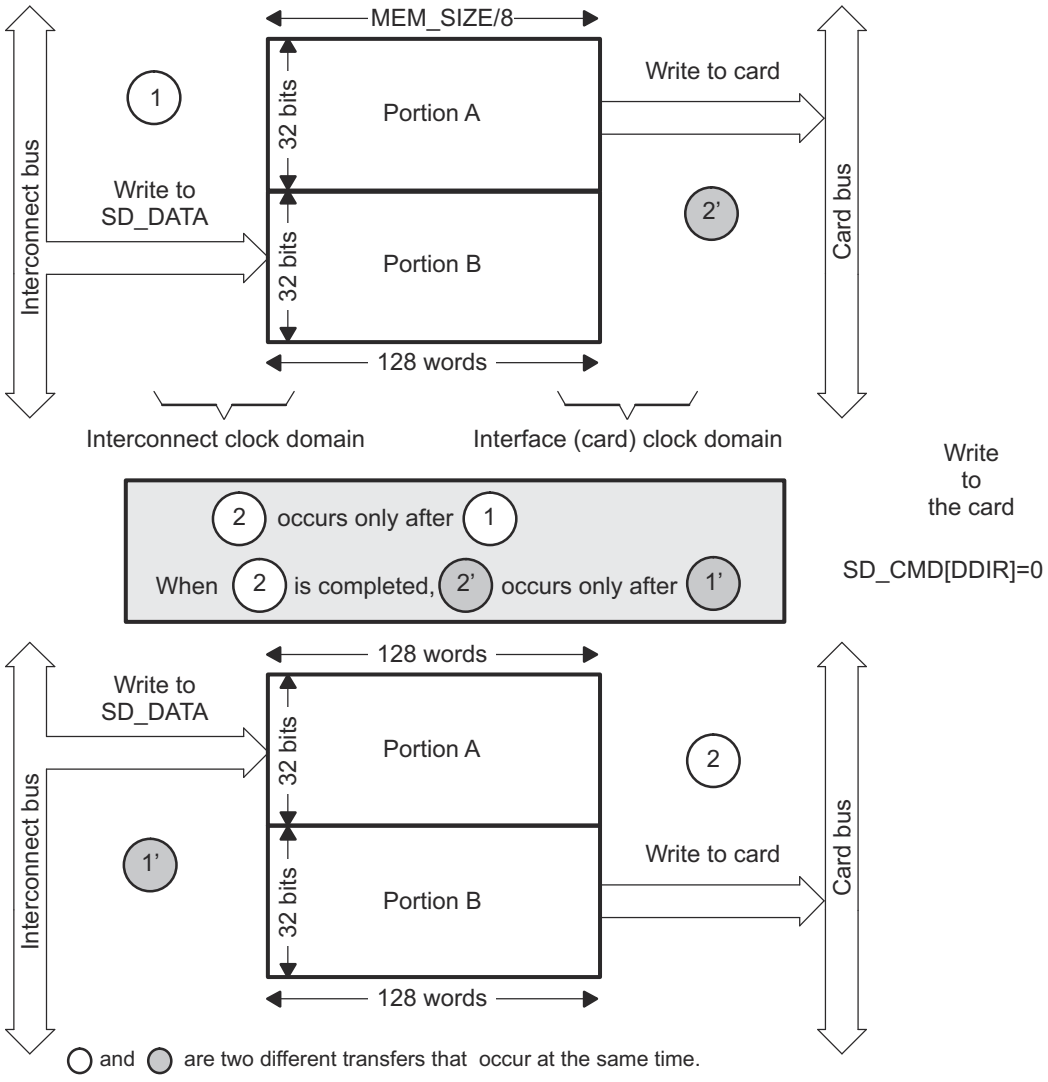

Figure 20-12. Buffer Management for a Write

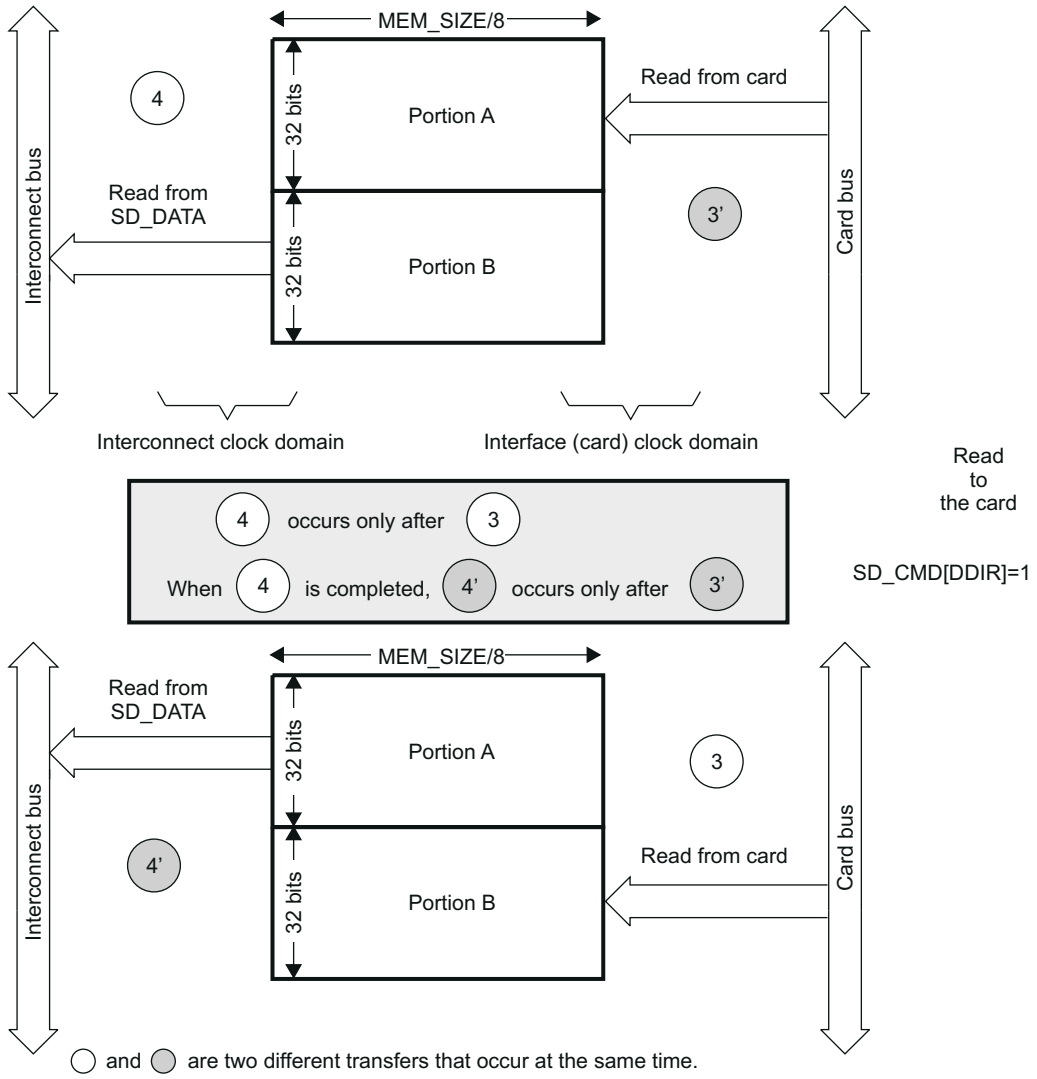

Figure 20-13. Buffer Management for a Read

20.2.6.1.1 Memory Size and Block Length

The memory size of the internal FIFO is 1024 bytes, and the block length is 512 bytes.

20.2.6.1.2 Data Buffer Status

The data buffer status is defined in the following interrupt status register and status register:

- Interrupt status registers (see Section 20.4):
  - SD_STAT[29] BADA Bad access to data space
  - SD_STAT[5] BRR Buffer read ready
  - SD_STAT[4] BWR Buffer write ready
- Status registers (see Section 20.4):
  - SD_PSTATE[11] BRE Buffer read enable
  - SD_PSTATE[10] BWE Buffer write enable

20.2.7 Transfer Process

The process of a transfer is dependent on the type of command. It can be with or without a response, with or without data.

20.2.7.1 Different Types of Commands

Different types of commands are specific to SD cards. See the SD Memory Card Specifications or the SD Card Specification, Part A2, SD Host Controller Standard Specification for more details.

20.2.7.2 Different Types of Responses

Different types of responses are specific to SD cards. See the SD Memory Card Specifications or the SD Card Specification, Part A2, SD Host Controller Standard Specification for more details.

Table 20-8 shows how the SD responses are stored in the SD_RSPxx registers.

Table 20-8. SD Responses in the SD_RSPxx Registers

Kind of Response	Response Field	Response Register
R1, R1b (normal response), R3, R4, R5, R5b, R6, R7	RESP[39:8] (1)	SD_RSP10[31:0]
R1b (Auto CMD12 response)	RESP[39:8] (1)	SD_RSP76[31:0]
R2	RESP[127:0] (1)	SD_RSP76 [31:0] SD_RSP54[31:0] SD_RSP32[31:0] SD_RSP10[31:0]

(1) RESP refers to the command response format described in the specifications mentioned above.

When the host controller modifies part of the SD_RSPxx registers, it preserves the unmodified bits.

The host controller stores the Auto CMD12 response in the SD_RSP76[31:0] register because the Host Controller may have a multiple block data DAT line transfer executing concurrently with a command. This allows the host controller to avoid overwriting the Auto CMD12 response with the command response stored in SD_RSP10 register and vice versa.

20.2.8 Transfer or Command Status and Error Reporting

Flags in the SDMMC show status of communication with the card:

- A timeout (of a command, a data, or a response)
- A CRC

Error conditions generate interrupts. See Table 20-9 and register description for more details.

Table 20-9. CC and TC Values Upon Error Detected

Error hold in the SD_STAT Register		CC	TC	Comments
29	BADA			No dependency with CC or TC. BADA is related to the register accesses. Its assertion is not dependent of the ongoing transfer.
28	CERR	1		CC is set upon CERR.
22	DEB		1	TC is set upon DEB.
21	DCRC		1	TC is set upon DCRC.
20	DTO			DTO and TC are mutually exclusive.DCRC and DEB cannot occur with DTO
19	CIE	1		CC is set upon CIE.
18	CEB	1		CC is set upon CEB.
17	CCRC	1		CC can be set upon CCRC - See CTO comment
16	CTO			CTO and CC are mutually exclusive. CIE, CEB and CERR cannot occur with CTO. CTO can occur at the same time as CCRC it indicates a command abort due to a contention on CMD line. In this case no CC appears.

SD_STAT[21] DCRC event can be asserted in the following conditions:

- Busy timeout for R1b, R5b response type

- Busy timeout after write CRC status
- Write CRC status timeout
- Read data timeout
- Boot acknowledge timeout

20.2.8.1 Busy Timeout for R1b, R5b Response Type

Figure 20-14 shows DCRD event condition asserted when there is a busy timeout for R1b or R5b responses.

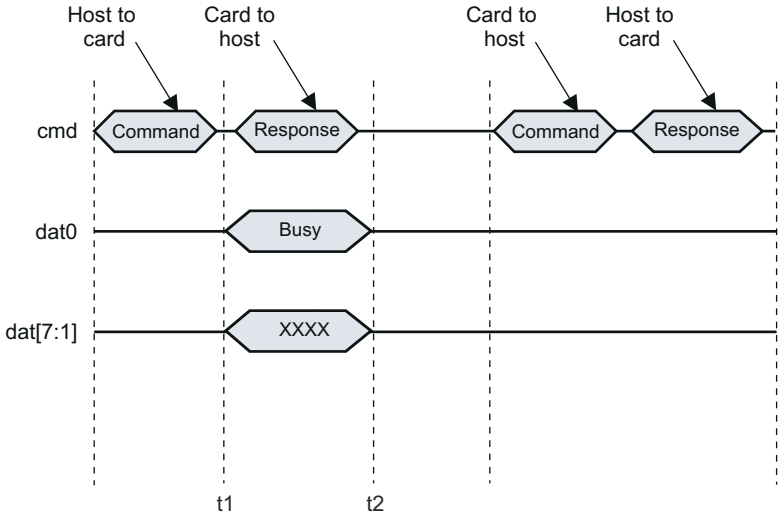

Figure 20-14. Busy Timeout for R1b, R5b Responses

t1 - Data timeout counter is loaded and starts after R1b, R5b response type.

t2 - Data timeout counter stops and if it is 0, SD_STAT[21] DCRC is generated.

20.2.8.2 Busy Timeout After Write CRC Status

Figure 20-15 shows DCRC event condition asserted when there is busy timeoutafter write CRC status.

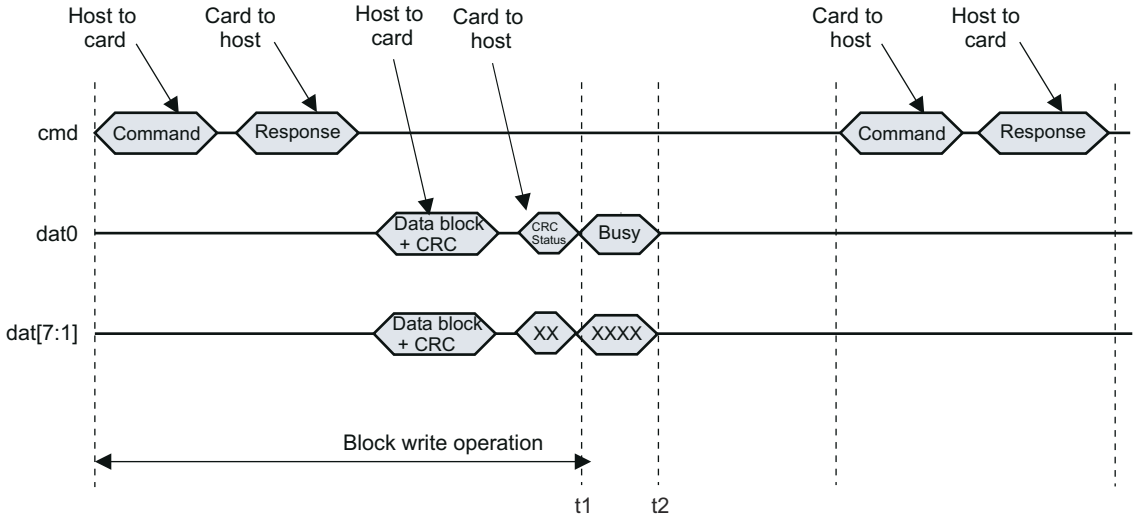

Figure 20-15. Busy Timeout After Write CRC Status

t1 - Data timeout counter is loaded and starts after CRC status.

t2 - Data timeout counter stops and if it is 0, SD_STAT[21] DCRC is generated.

20.2.8.3 Write CRC Status Timeout

Figure 20-16 shows DCRC event condition asserted when there is write CRC status timeout.

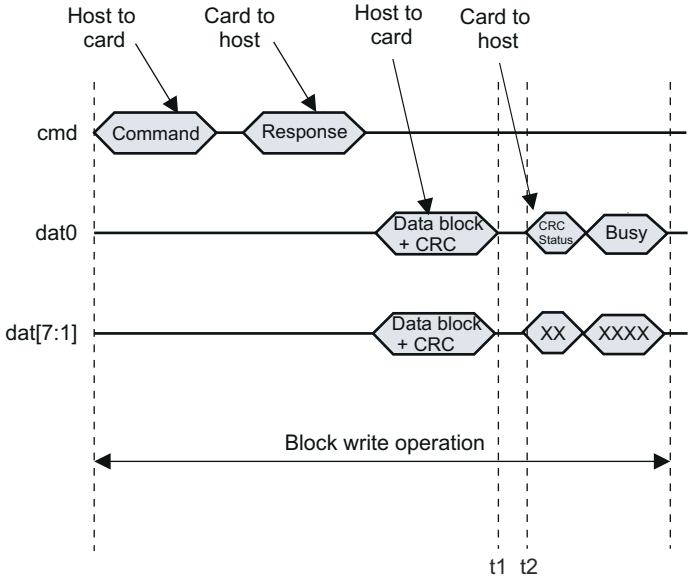

Figure 20-16. Write CRC Status Timeout

t1 - Data timeout counter is loaded and starts after Data block + CRC.

t2 - Data timeout counter stops and if it is 0, SD_STAT[21] DCRC is generated.

20.2.8.4 Read Data Timeout

Figure 20-17 shows DCRC event condition asserted when there is read data timeout.

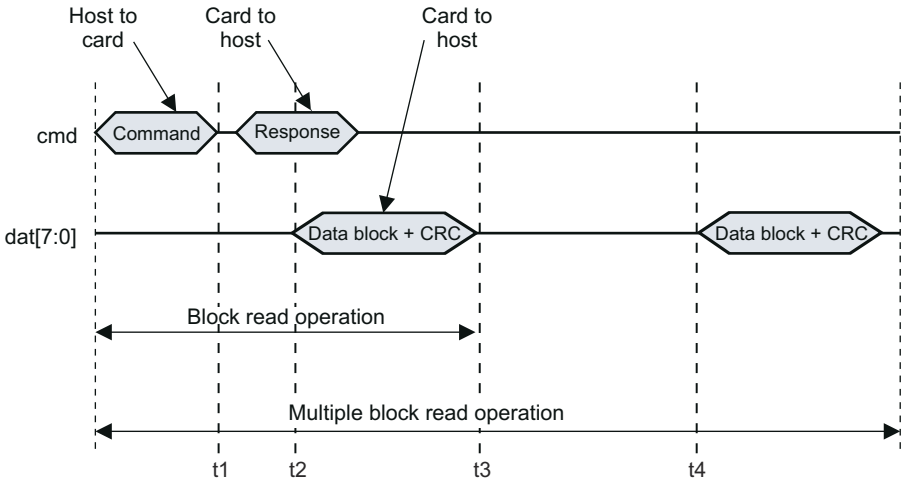

Figure 20-17. Read Data Timeout

t1 - Data timeout counter is loaded and starts after Command transmission.

t2 - Data timeout counter stops and if it is 0, SD_STAT[21] DCRC is generated.

t3 - Data timeout counter is loaded and starts after Data block + CRC transmission.

t4 - Data timeout counter stops and if it is 0, SD_STAT[21] DCRC is generated.

20.2.9 Auto Command 12 Timings

With the UHS definition of SD cards with higher frequency for SD clocks up to 208, SD standard imposes a specific timing for Auto CMD12 "end bit" arrival.

20.2.9.1 Auto Command 12 Timings During Write Transfer

A margin named Ncrc in range of 2 to 8 cycles has been defined for SDR50 and SDR104 card components for write data transfers, as auto command 12 'end bit' shall arrive after the CRC status "end bit".

Figure 20-18 shows auto CMD12 timings during write transfer.

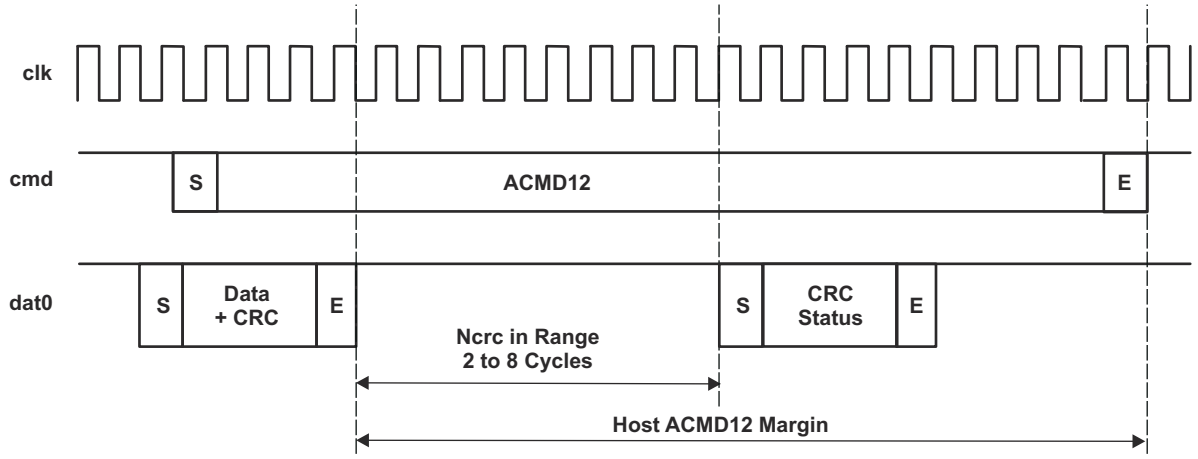

Figure 20-18. Auto CMD12 Timing During Write Transfer

The Host controller has a margin of 18 clock cycles to make sure that auto CMD12 'end bit' arrives after the CRC status. This margin does not depend on SDMMC bus configuration, 1 or 4 bus width.

20.2.9.2 Auto Command 12 Timings During Read Transfer

With UHS very high speed cards gap timing between 2 successive cards has been extended to 4 cycles instead of 2. By the way it gives more flexibility for Host Auto CMD12 arrival in order to receive the last complete and reliable block. SDMMC only follows the 'Left Border Case' defined by SD UHS specification.

Figure 20-19 shows ACMD12 timings during read transfer.

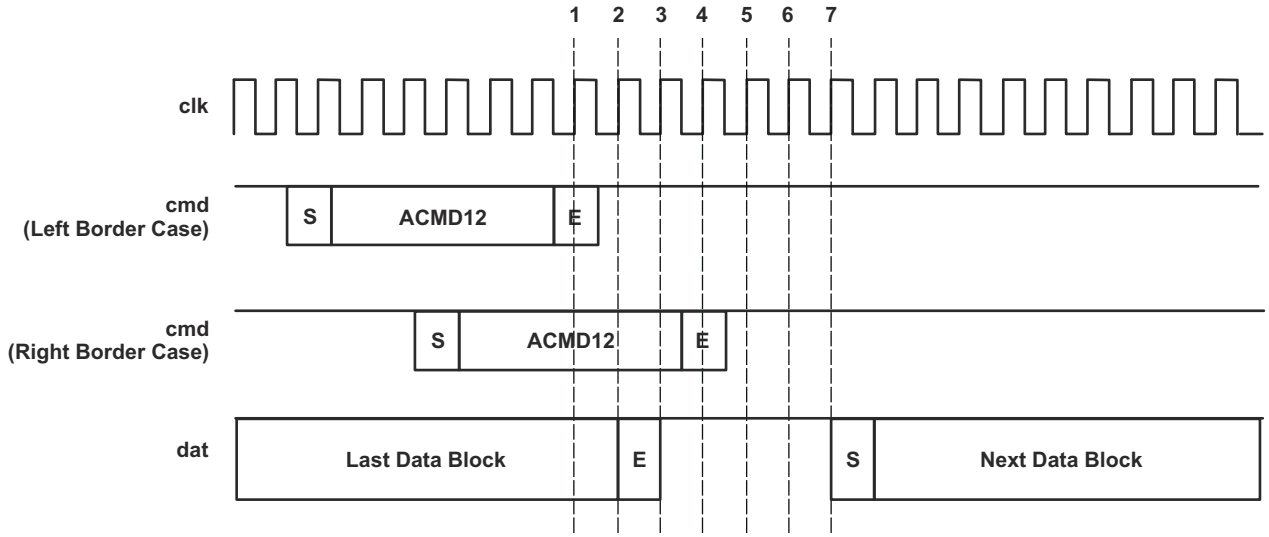

Figure 20-19. Auto Command 12 Timings During Read Transfer

The Auto CMD12 arrival sent by the Host controller is not sensitive to the SDMMC bus configuration whether it is a 1 or 4 bit bus width transfer.

20.2.10 Transfer Stop

Whenever a transfer is initiated, the transmission may be willed to stop whereas it is still not finished. Several cases can be faced depending on the transfer type:

- Multiple blocks oriented transfers (for which transfer length is known)

Note

Since the SDMMC manages transfers based on a block granularity, the buffer will accept a block only if there is enough space to completely store it. Consequently, if a block is pending in the buffer, no command will be sent to the card because the card clock will be shut off by the controller.

The SDMMC includes two features which make a transfer stop more convenient andeasier to manage:

- Auto CMD12:

  This feature is enabled by setting the SD_CMD[2] ACEN bit to 1 (this setting is relevant for a SD transfer with a known number of blocks to transfer). When the Auto CMD12 feature is enabled, the SDMMC will automatically issue a CMD12 command when the expected number of blocks has been exchanged.
- Stop at block gap

  This feature is enabled by setting the SD_HCTL[16] SBGR bit to 1. When enabled, this capability holds the transfer on until the end of a block boundary. If a stop transmission is needed, software can use this pause to send a CMD12 to the card.

Table 20-10 shows the common ways to stop a transfer, indicating command to send and features to enable.

Table 20-10. SDMMC Transfer Stop Command Summary

		WRITE Transfer	READ Transfer
Single block		Transfer ends automatically Wait TC	Transfer ends automatically Wait TC
Multi blocks (finite or infinite)	Before the programmed block boundary	Send CMD12 Wait TC	Send CMD12 Wait TC
	Stop at the end of the transfer (finite transfer only)	Auto CMD12 active Transfer ends automatically Wait TC	Auto CMD12 active Transfer ends automatically Wait TC

Note

The SDMMC will send the stop command to the card on a block boundary, regardless the moment the command was written to the controller registers.

20.2.11 Output Signals Generation

The SDMMC output signals can be driven on either falling edge or rising edge depending on the SD_HCTL[2] HSPE bit. This feature allows to reach better timing performance, and thus to increase data transfer frequency.

20.2.11.1 Generation on Falling Edge of SDMMC Clock

The controller is by default in this mode to maximize hold timings. In this case, SD_HCTL[2] HSPE bit is cleared to 0.

Figure 20-20 shows the output signals of the module when generating from the falling edge of the SDMMC clock.

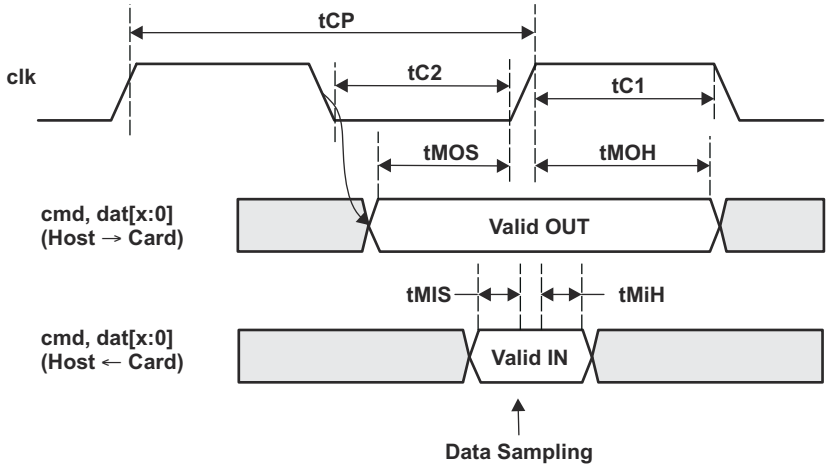

Figure 20-20. Output Driven on Falling Edge

20.2.11.2 Generation on Rising Edge of SDMMC Clock

This mode increases setup timings and allows reaching higher bus frequency. This feature is activated by setting SD_HCTL[2] HSPE bit to 1. The controller shall be set in this mode to support SDR transfers.

Figure 20-21 shows the output signals of the module when generating from the rising edge of the SDMMC clock.

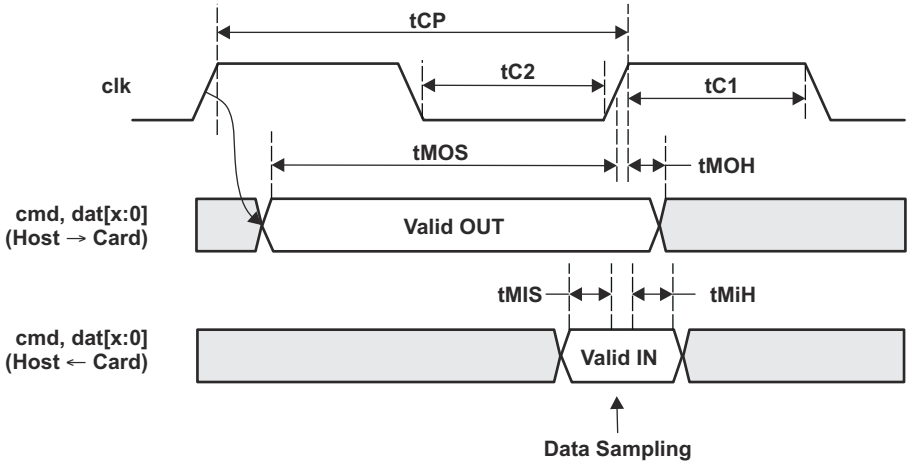

Figure 20-21. Output Driven on Rising Edge

20.2.12 Test Registers

Test registers are available to be compliant with SD Host controller specification. This feature is useful to generate interrupts manually for driver debugging. The Force Event register (SD_FE) is used to control the Error Interrupt Status and Auto CMD12 Error Status. The System Test register (SD_SYSTEST) is used to control the signals that connect to I/O pins when the module is configured in system test (SD_CON[4] MODE = 1) mode for boundary connectivity verification.

20.2.13 SDMMC Hardware Status Features

Table 20-11 summarizes the SDMMC hardware status features.

Table 20-11. SDMMC Hardware Status Features

Feature	Type	Register/Bit Field/Observability Control	Description
Interrupt flags		See Section 20.2.4	
CMD line signal level	Status	[24] CLEV	Indicates the level of the cmd line

Table 20-11. SDMMC Hardware Status Features (continued)

Feature	Type	Register/Bit Field/Observability Control	Description
DAT lines signal level	Status	[23:20] DLEV	Indicates the level of the data lines
Buffer read enable	Status	[11] BRE	Readable data exists in the buffer.
Buffer write enable	Status	[10] BWE	Indicates whether there is enough space in the buffer to write BLEN bytes of data
Read transfer active	Status	[9] RTA	This status is used for detecting completion of a read transfer.
Write transfer active	Status	[8] WTA	This status indicates a write transfer active.
Data line active	Status	[2] DLA	Indicates whether the data lines are active
Command Inhibit (data lines)	Status	[1] DATI	Indicates whether issuing of command using data lines is allowed
Command inhibit (CMD line)	Status	[0] CMDI	Indicates whether issuing of command usingCMD line is allowed

20.3 Low-Level Programming Models

20.3.1 SDMMC Initialization Flow

The next sections outline the three steps to initialize the SDMMC:

- Initialize Clocks
- Software reset of the controller
- Set module's hardware capabilities

20.3.1.1 Enable OCP and CLKADPI Clocks

Prior to any SDMMC register access one must enable the SD OCP clock and CLKADPI clock in PRCM module registers. For more information, see Chapter 7.

20.3.1.2 SD Soft Reset Flow

Figure 20-22 shows the soft reset process of SDMMC.

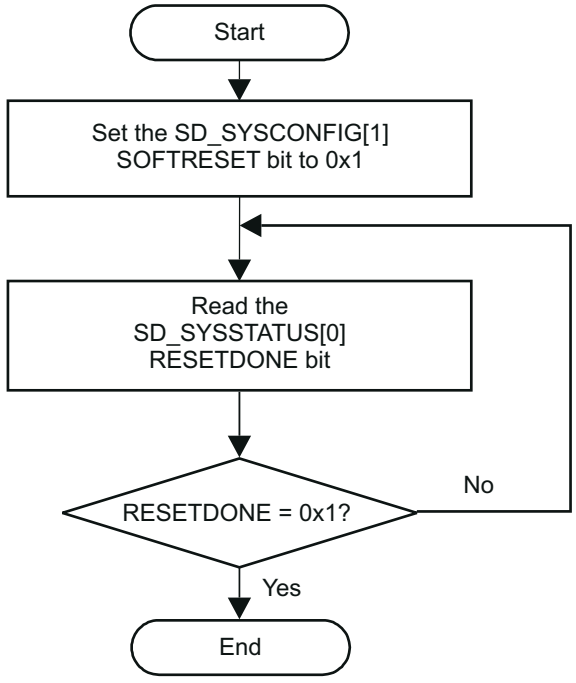

Figure 20-22. SDMMC Controller Software Reset Flow

20.3.1.3 Set SD Default Capabilities

Software must read capabilities (in boot ROM for instance) and is allowed to set (write) SD_CAPA[26:24] and SD_CUR_CAPA[23:0] registers before the SDMMC host driver is started.

20.3.1.4 SDMMC Host and Bus Configuration

Figure 20-23 details the SDMMC bus configuration process.

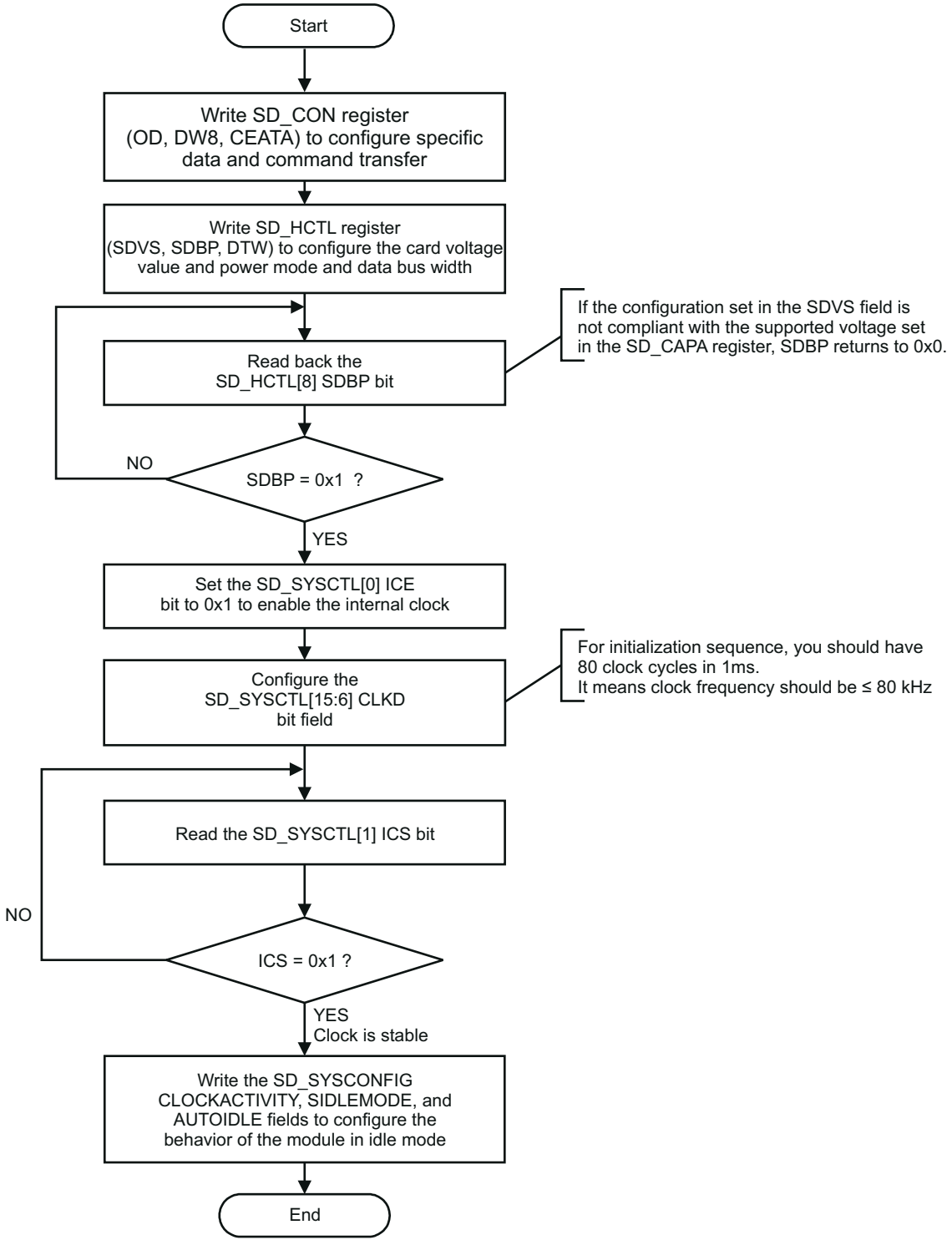

Figure 20-23. SDMMC Bus Configuration Flow

20.3.2 Operational Modes Configuration

20.3.2.1 Basic Operations for SDMMC

The SDMMC performs data transfers: data to card (referred to as write transfers) and data from card (referred to as read transfers).

The host controller requires transfers to run on a block-by-block basis, rather than on a DMA burst size basis. A single DMA request (or block request interrupt) is signaled for each block. Pipelining is supported as long as the block size is less than one half of the memory buffer size.

20.3.2.2 Card Detection, Identification, and Selection

Figure 20-24 and Figure 20-25 show the card identification and selection process.

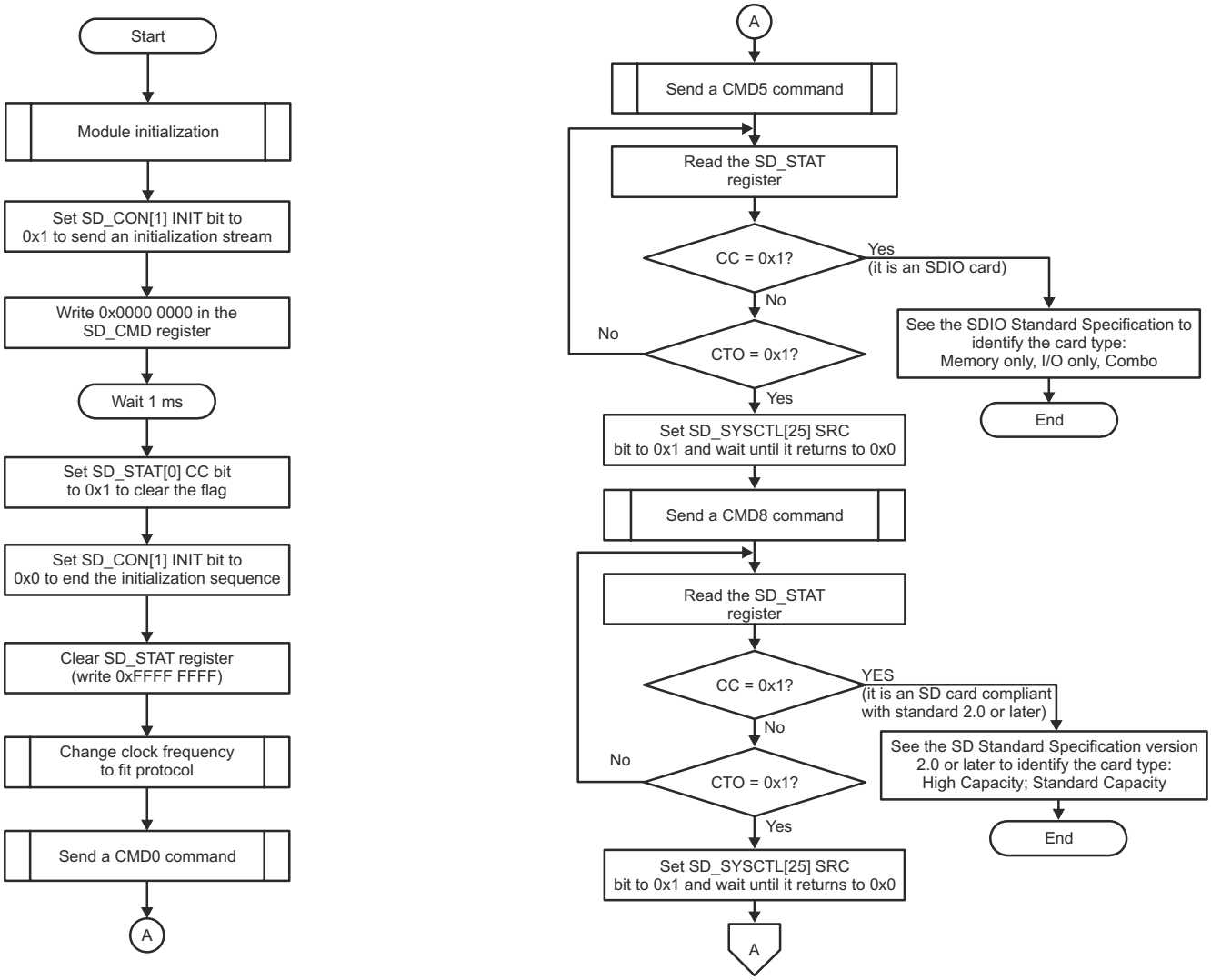

Figure 20-24. SD Card Identification and Selection - Part 1

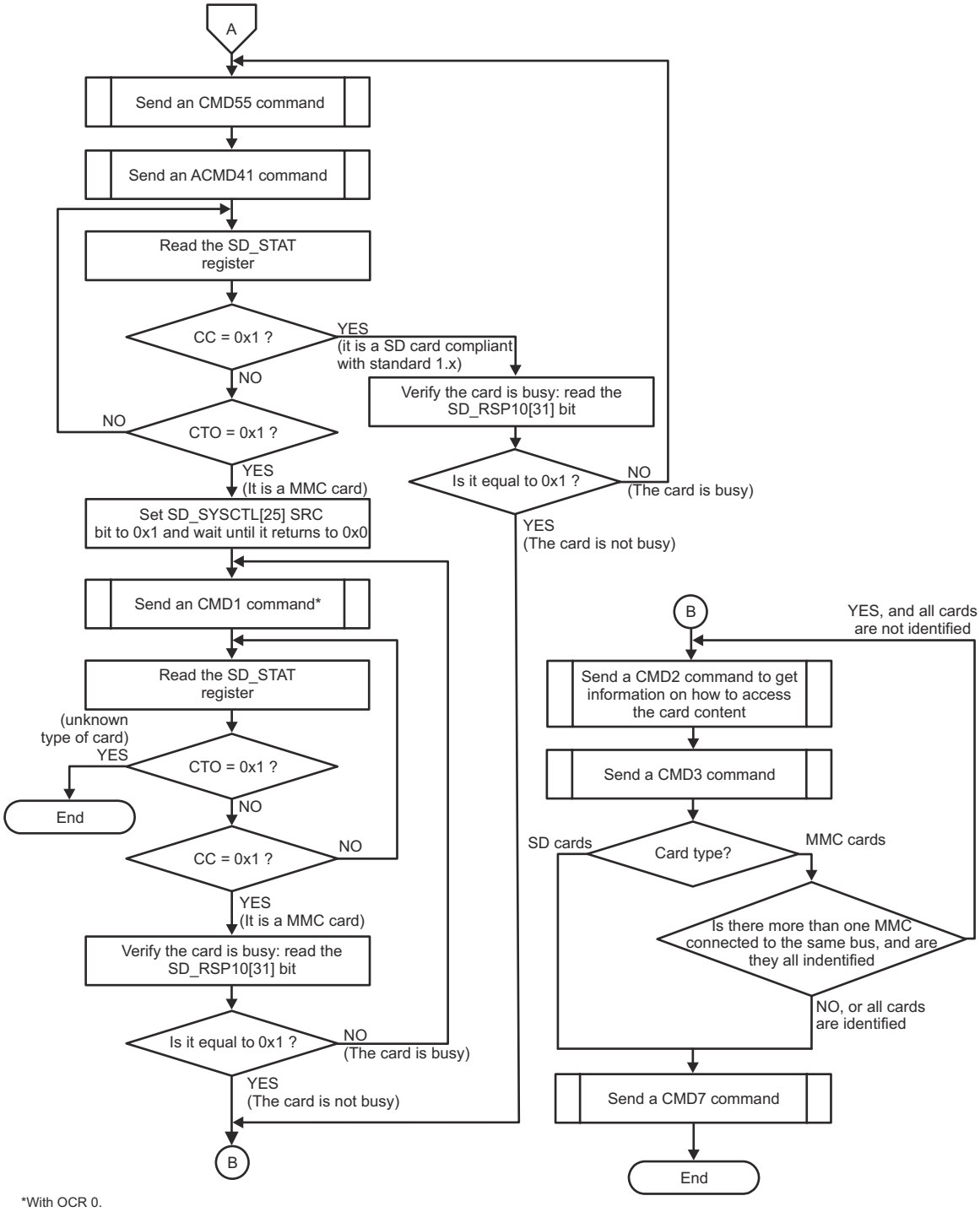

Figure 20-25. SD Card Identification and Selection - Part 2

20.4 SDMMC Registers

Table 20-12 lists the memory-mapped registers for the SDMMC registers. All register offset addresses not listed in Table 20-12 should be considered as reserved locations and the register contents should not be modified.

Table 20-12. SDMMC Registers

Offset	Acronym	Register Name	Section
110h	SYSCFG	System Configuration	Section 20.4.1
114h	SYSSTA	Module Status	Section 20.4.2
124h	CSRE	Status Error Detection	Section 20.4.3
128h	SYSTEST	System Test Control	Section 20.4.4
12Ch	CON	SD Configuration	Section 20.4.5
130h	PWCNT	Power Delay Counter	Section 20.4.6
200h	SDMASA	DMA System Address	Section 20.4.7
204h	BLK	Transfer Size Configuration	Section 20.4.8
208h	ARG	Command Argument	Section 20.4.9
20Ch	CMD	Command Transfer Control	Section 20.4.10
210h	RSP10	Command Response Register	Section 20.4.11
214h	RSP32	Command Response Upper	Section 20.4.12
218h	RSP54	Command Response Bits	Section 20.4.13
21Ch	RSP76	Response Data 4	Section 20.4.14
220h	DATA	Data Buffer	Section 20.4.15
224h	PSTATE	Controller Status	Section 20.4.16
228h	HCTL	Host Control Settings	Section 20.4.17
22Ch	SYSCTL	Clock and Timeout	Section 20.4.18
230h	STAT	Interrupt Status	Section 20.4.19
234h	IE	Interrupt Enable	Section 20.4.20
238h	ISE	Interrupt Signal Enable	Section 20.4.21
23Ch	AC12	Auto Command 12 Error	Section 20.4.22
240h	CAPA	Controller Capabilities	Section 20.4.23
248h	CURCAPA	Current Capabilities	Section 20.4.24
250h	FE	Force Error Interrupt	Section 20.4.25
2FCh	REV	Version Information	Section 20.4.26
1040h	TPSEL	Test Port Selection	Section 20.4.27
1048h	DMAMODE	DMA Mode Configuration	Section 20.4.28
1050h	DMAIND	DMA Trigger Selection	Section 20.4.29
1054h	CLKSEL	Memory Clock Selection	Section 20.4.30
10E0h	EVTMODE	Event Mode	Section 20.4.31
10FCh	DESC	Module Identification Register	Section 20.4.32
1100h	SDMMCSTAT	Status Register	Section 20.4.33
1110h + formula	BUFIF_y	Buffer Interface	Section 20.4.34
4000h	CLKCFG	Primary Configuration	Section 20.4.35

Complex bit access types are encoded to fit into small table cells. Table 20-13 shows the codes that are used for access types in this section.

Table 20-13. SDMMC Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

20.4.1 SYSCFG Register (Offset = 110h) [Reset = 00002015h]

SYSCFG is shown in Table 20-14.

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This register allows controlling various parameters of the OCP interface.

Table 20-14. SYSCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-12	RESERVED	R	0h	Reserved
11-10	RESERVED	R	0h	Reserved
9-8	RESERVED	R	0h	Reserved
7-5	RESERVED	R	0h	Reserved
4-3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	SOFTRST	R/W	0h	Software reset. The bit is automatically reset by the hardware. During reset, it always returns 0.
0	RESERVED	R	0h	Reserved

20.4.2 SYSSTA Register (Offset = 114h) [Reset = 00000000h]

SYSSTA is shown in Table 20-15.

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This register provides status information about the module excluding the interrupt status information.

Table 20-15. SYSSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RSTDONE	R	0h	Internal Reset Monitoring Note: The debounce clock , the interface clock and the functional clock must be provided to the SDMMC host controller to allow the internal reset monitoring. 0h = Internal module reset is on-going 1h = Reset completed

20.4.3 CSRE Register (Offset = 124h) [Reset = 00000000h]

CSRE is shown in Table 20-16.

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Card Status Response Error Detection This register enables the host controller to detect card status errors of response type R1, R1b for all cards and of R5, R5b and R6 response for cards types SD or SDIO. When a bit SD_SD_CSRE[i] is set to 1, if the corresponding bit at the same position in the response RSP10[i] is set to 1, the host controller indicates a card error (SD_STAT.CERR bit) interrupt status to avoid the host driver reading the response register (RSP10). No automatic card error detection for autoCMD12 is implemented; the host system has to check autoCMD12 response register (RSP76) for possible card errors.

Table 20-16. CSRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STA	R/W	0h	Card status response error 0h = Minimum value FFFFFFFFh = Maximum value

20.4.4 SYSTEST Register (Offset = 128h) [Reset = 00000000h]

SYSTEST is shown in Table 20-17.

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SDMMC System Test Register This register is used to control the signals that connect to I/O pins when the module is configured in system test (SD_SYSTEST) mode for boundary connectivity verification. In SD_SYSTEST mode, a write into SD_CMD register will not start a transfer.

Table 20-17. SYSTEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	OBI	R	0h	Out-Of-Band Interrupt (OBI) data value Note: Out-Of-Band Interrupt (OBI) is not supported.
15	SDCD	R	0h	Card detect input signal (SDCD) data value 0h = The card detect pin is driven low 1h = The card detect pin is driven high
14	SDWP	R	0h	Write protect input signal (SDWP) data value 0h = The write protect pin SDWP is driven low 1h = The write protect pin SDWP is driven high
13	WAKD	R/W	0h	Wake request output signal data value 0h = The pin SWAKEUP is driven low 1h = The pin SWAKEUP is driven high
12	SSB	R/W	0h	Set status bit This bit must be cleared prior attempting to clear a status bit of the interrupt status register (SD_STAT). 0h = Clears this SSB bit field. Writing 0 does not clear already set status bits 1h = Force to 1 all status bits of the interrupt status register (SD_STAT) only if the corresponding bit field in the Interrupt signal enable register (SD_ISE) is set.
11	D7D	R/W	0h	DAT7 input/output signal data value 0h = If SD_SYSTEST.DDIR bit = 0 (output mode direction), the DAT7 line is driven low. If SD_SYSTEST.DDIR bit = 1 (input mode direction), no effect. 1h = If SD_SYSTEST.DDIR bit = 0 (output mode direction), the DAT7 line is driven high. If SD_SYSTEST.DDIR bit = 1 (input mode direction), no effect.
10	D6D	R/W	0h	DAT6 input/output signal data value 0h = If SD_SYSTEST.DDIR bit = 0 (output mode direction), the DAT6 line is driven low. If SD_SYSTEST.DDIR bit = 1 (input mode direction), no effect. 1h = If SD_SYSTEST.DDIR bit = 0 (output mode direction), the DAT6 line is driven high. If SD_SYSTEST.DDIR bit = 1 (input mode direction), no effect.
9	D5D	R/W	0h	DAT5 input/output signal data value 0h = If SD_SYSTEST.DDIR bit = 0 (output mode direction), the DAT5 line is driven low. If SD_SYSTEST.DDIR bit = 1 (input mode direction), no effect. 1h = If SD_SYSTEST.DDIR bit = 0 (output mode direction), the DAT5 line is driven high. If SD_SYSTEST.DDIR bit = 1 (input mode direction), no effect.
8	D4D	R/W	0h	DAT4 input/output signal data value 0h = If SD_SYSTEST.DDIR bit = 0 (output mode direction), the DAT4 line is driven low. If SD_SYSTEST.DDIR bit = 1 (input mode direction), no effect. 1h = If SD_SYSTEST.DDIR bit = 0 (output mode direction), the DAT4 line is driven high. If SD_SYSTEST.DDIR bit = 1 (input mode direction), no effect.

Table 20-17. SYSTEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	D3D	R/W	0h	DAT3 input/output signal data value 0h = If SD_SYSTEST.DDIR bit = 0 (output mode direction), the DAT3 line is driven low. If SD_SYSTEST.DDIR bit = 1 (input mode direction), no effect. 1h = If SD_SYSTEST.DDIR bit = 0 (output mode direction), the DAT3 line is driven high. If SD_SYSTEST.DDIR bit = 1 (input mode direction), no effect.
6	D2D	R/W	0h	DAT2 input/output signal data value 0h = If SD_SYSTEST.DDIR bit = 0 (output mode direction), the DAT2 line is driven low. If SD_SYSTEST.DDIR bit = 1 (input mode direction), no effect. 1h = If SD_SYSTEST.DDIR bit = 0 (output mode direction), the DAT2 line is driven high. If SD_SYSTEST.DDIR bit = 1 (input mode direction), no effect.
5	D1D	R/W	0h	DAT1 input/output signal data value 0h = If SD_SYSTEST.DDIR bit = 0 (output mode direction), the DAT1 line is driven low. If SD_SYSTEST.DDIR bit = 1 (input mode direction), no effect. 1h = If SD_SYSTEST.DDIR bit = 0 (output mode direction), the DAT1 line is driven high. If SD_SYSTEST.DDIR bit = 1 (input mode direction), no effect.
4	D0D	R/W	0h	DAT0 input/output signal data value 0h = If SD_SYSTEST.DDIR bit = 0 (output mode direction), the DAT0 line is driven low. If SD_SYSTEST.DDIR bit = 1 (input mode direction), no effect. 1h = If SD_SYSTEST.DDIR bit = 0 (output mode direction), the DAT0 line is driven high. If SD_SYSTEST.DDIR bit = 1 (input mode direction), no effect.
3	DDIR	R/W	0h	Control of the DAT[7:0] pins direction 0h = The DAT lines are outputs (host to card) 1h = The DAT lines are inputs (card to host)
2	CDAT	R/W	0h	CMD input/output signal data value 0h = If SD_SYSTEST.CDIR bit = 0 (output mode direction), the CMD line is driven low. If SD_SYSTEST.CDIR bit = 1 (input mode direction), no effect. 1h = If SD_SYSTEST.CDIR bit = 0 (output mode direction), the CMD line is driven high. If SD_SYSTEST.CDIR bit = 1 (input mode direction), no effect.
1	CDIR	R/W	0h	Control of the CMD pin direction 0h = The CMD line is an output (host to card) 1h = The CMD line is an input (card to host)
0	MCKD	R/W	0h	MMC clock output signal data value 0h = The output clock is driven low 1h = The output clock is driven high

20.4.5 CON Register (Offset = 12Ch) [Reset = 00000600h]

CON is shown in Table 20-18.

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SDMMC Configuration Register. This register is used: - to select the functional mode or the SYSTEST mode for any card. - to send an initialization sequence to any card. - to enable the detection on DAT[1] of a card interrupt for SDIO cards only. and also to configure : - specific data and command transfers for MMC cards only. - the parameters related to the card detect and write protect input signals.

Table 20-18. CON Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0h	Reserved
21	SDMALNE	R/W	0h	Peripheral DMA Level/Edge Request The waveform of the DMA request can be configured either edge sensitive with early de-assertion on first access to SD_DATA register or late de-assertion, request remains active until last allowed data written into SD_DATA. 0h = peripheral DMA edge sensitive 1h = peripheral DMA level sensitive
20	REVERVED	R/W	0h	DMA Master or Slave selection Note: these bit fields are *not used*, since the IP not support MDMA.
19	RESERVED	R/W	0h	Dual Data Rate mode Note: these bit fields are *not used*, Only Standard mode is supported.
18-17	RESERVED	R/W	0h	Note: these bit fields are *not used*.
16	CLKEXTFREE	R/W	0h	External clock free running This register is used to maintain card clock out of transfer transaction to enable peripheral module (for example to generate a synchronous interrupt on mmc_dat[1]). The Clock will be maintained only if SD_SYSCTL.CEN bit is set. 0h = External card clock is cut off outside active transaction period 1h = External card clock is maintained even out of active transaction period only if SD_SYSCTL.CEN bit is set.
15	PADEN	R/W	0h	Control Power for MMC Lines. Note: Power control is not supported using this bit. 0h = Minimum value 1h = Maximum value
14	OBIE	R/W	0h	Out-of-Band Interrupt Enable. Note: The Out-of-Band (OBI) interrupt is not supported. 0h = Minimum value 1h = Maximum value
13	OBIP	R/W	0h	Out-of-Band Interrupt Polarity Note: The Out-of-Band (OBI) interrupt is not supported. 0h = Minimum value 1h = Maximum value
12	CEATA	R/W	0h	CE-ATA control mode (MMC cards compliant with CE-ATA) This bit is used to indicate that next commands are considered as specific CE-ATA commands that potentially use 'command completion' features. 0h = Standard MMC/SD/SDIO mode 1h = CE-ATA mode. Next commands are considered as CE-ATA commands.
11	CTPL	R/W	0h	Control Power for DAT[1] line MMC and SD cards: By default, this bit is set to 0 and the host controller automatically disables all the input buffers outside of a transaction to minimize the leakage current. SDIO cards: When this bit is set to 1, the host controller automatically disables all the input buffers except the buffer of DAT[1] outside of a transaction in order to detect asynchronous card interrupt on DAT[1] line and minimize the leakage current of the buffers. 0h = Disable all the input buffers outside of a transaction 1h = Disable all the input buffers except the buffer of DAT[1] outside of a transaction

Table 20-18. CON Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-9	DVAL	R/W	3h	Debounce filter value (all cards) This register is used to define a debounce period to filter the card detect input signal (SDCD). The usage of the card detect input signal (SDCD) is optional and depends on the system integration and the type of the connector housing that accommodates the card. 0h = 33 us debounce period 1h = 231 us debounce period 2h = 1 ms debounce period 3h = 8.4 ms debounce period
8	WPP	R/W	0h	Write protect polarity For SD and SDIO cards only This bit selects the active level of the write protect input signal (SDWP). The usage of the write protect input signal (SDWP) is optional and depends on the system integration and the type of the connector housing that accommodates the card. 0h = Active low level 1h = Active high level
7	CDP	R/W	0h	Card detect polarity All cards This bit selects the active level of the card detect input signal (SDCD). The usage of the card detect input signal (SDCD) is optional and depends on the system integration and the type of the connector housing that accommodates the card. 0h = Active low level 1h = Active high level
6	MIT	R/W	0h	MMC interrupt command (MMC cards only). This bit must be set to 1, when the next write access to the command register (SD_CMD) is for writing a MMC interrupt command (CMD40) requiring the command timeout detection to be disabled for the command response. 0h = MMC interrupt command not possible, command timeout enabled 1h = MMC interrupt command possible, Command timeout disabled
5	DW8	R/W	0h	8-bit mode MMC select (MMC cards only) For SD/SDIO cards, this bit must be cleared to 0. For MMC card, this bit must be set following a valid SWITCH command (CMD6) with the correct value and extend CSD index written in the argument. Prior to this command, the MMC card configuration register (CSD and EXT_CSD) must be verified for compliancy with MMC standard specification. 0h = 1-bit or 4-bit data width 1h = Open drain or broadcast host response
4	MODE	R/W	0h	Mode select (all cards) This bit selects the functional mode. 0h = Functional mode. Transfers to the MMC/SD/SDIO cards follow the card protocol. The MMC clock is enabled. MMC/SD transfers are operated under the control of the SD_CMD register. 1h = SYSTEST mode. The signal pins are configured as general-purpose input/output and the 1024-byte buffer is configured as a stack memory accessible only by the local host or system DMA. The pins retain their default type (input, output or inout). SYSTEST mode is operated under the control of the SD_SYSTEST register.
3	STR	R/W	0h	Stream command (MMC cards only) This bit must be set to 1 only for the stream data transfers (read or write) of the adtc commands. Stream read is a class 1 command (CMD11READ_DAT_UNTIL_STOP). Stream write is a class 3 command (CMD20WRITE_DAT_UNTIL_STOP). 0h = Block oriented data transfer 1h = Stream oriented data transfer

Table 20-18. CON Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	HR	R/W	0h	Broadcast host response (MMC cards only) This register is used to force the host to generate a 48-bit response for bc command type. It can be used to terminate the interrupt mode by generating a CMD40 response by the core. In order to have the host response to be generated in open drain mode, the IO must be configured accordingly in EXT_IOMUX. When SD_CON.CEATA bit is set to 1 and SD_ARG cleared to 0, when writing the value of 0 into SD_CMD register, the host controller performs a 'command completion signal disable' token (i.e., mmc_cmd line held to 0 during 47 cycles followed by a 1). 0h = The host does not generate a 48-bit response instead of a command 1h = The host generates a 48-bit response instead of a command or a command completion signal disable token
1	INIT	R/W	0h	Send initialization stream (all cards) When this bit is set to 1, and the card is idle, an initialization sequence is sent to the card. An initialization sequence consists of setting the mmc_cmd line to 1 during 80 clock cycles. The initialization sequence is mandatory - but it is not required to do it through this bit - this bit makes it easier. Clock divider should be set to ensure that 80 clock periods are greater than 1ms. Note: In this mode, there is no command sent to the card and no response is expected. A command complete interrupt will be generated once the initialization sequence is completed. 0h = The host does not send an initialization sequence 1h = The host sends an initialization sequence
0	OD	R/W	0h	Card open drain mode This bit must be set to 1 for MMC card commands 1, 2, 3 and 40, and if the MMC card bus is operating in open-drain mode during the response phase to the command sent. Typically, during card identification mode when the card is either in idle, ready or ident state. It is also necessary to set this bit to 1, for a broadcast host response (see Broadcast host response register SD_CON.HR). 0h = No Open Drain 1h = Open Drain or Broadcast host response

20.4.6 PWCNT Register (Offset = 130h) [Reset = 00000000h]

PWCNT is shown in Table 20-19.

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SDMMC Power counter register This register is used to program a MMC counter to delay command transfers after activating the PAD power, this value depends on PAD characteristics and voltage.

Table 20-19. PWCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	NUMDEL	R/W	0h	Power counter This register is used to introduce a delay between the PAD ACTIVE pin assertion and the command issued. 0h = No additional delay added 1h = TCF delay (card clock period) 2h = TCF x 2 delay (card clock period) FFFEh = TCF x 65534 delay (card clock period) FFFFh = TCF x 65535 delay (card clock period) 0h = Minimum value of PWCNT FFFFh = Maximum value of PWCNT

20.4.7 SDMASA Register (Offset = 200h) [Reset = 00000000h]

SDMASA is shown in Table 20-20.

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DMA System Address This register contains the system memory address for a SDMA transfer. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value. The Host Driver shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at the every boundary specified by the Host SDMA Buffer Boundary in the Block Size register. The Host Controller generates DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register (003h) is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by the Resume command or by setting Continue Request in the Block Gap Control register, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register.

Table 20-20. SDMASA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR	R/W	0h	SDMA System Address register 0h = Minimum value FFFFFFFFh = Maximum value

20.4.8 BLK Register (Offset = 204h) [Reset = 00000000h]

BLK is shown in Table 20-21.

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Transfer Length Configuration Register BLEN is the block size register. NBLK is the block count register. This register shall be used for any card.

Table 20-21. BLK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	NBLK	R/W	0h	Block count for current transfer This register is enabled when Block count Enable (SD_CMD.BCE bit) is set to 1 and is valid only for multiple block transfers. Setting the block count to 0 results no data blocks being transferred. Note: The host controller decrements the block count after each block transfer and stops when the count reaches zero. This register can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value and write operation will be ignored. 0h = Stop count 1h = 1 block 2h = 2 blocks FFFFh = 65535 blocks 0h = Minimum value FFFFh = Maximum value
15-11	RESERVED	R	0h	Reserved
10-0	BLEN	R/W	0h	Transfer block size This register is enabled when Block Count Enable (SD_CMD.BCE) is set to 1 and is valid only for multiple block transfers. It specifies the block size for block data transfers. Read operations during transfers may return an invalid value, and write operations are ignored. 0h = No data transfer 1h = 1 byte block length 2h = 2 bytes block length 3h = 3 bytes block length 1FFh = 511 bytes block length 200h = 512 bytes block length 3FFh = 1023 bytes block length 400h = 1024 bytes block length 0h = Minimum value 7FFh = Maximum value

20.4.9 ARG Register (Offset = 208h) [Reset = 00000000h]

ARG is shown in Table 20-22.

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Command argument register This register contains command argument specified as bit 39-8 of Command-Format. These registers must be initialized prior to sending the command itself to the card (write action into the register SD_CMD register). Only exception is for a command index specifying stuff bits in arguments, making a write unnecessary.

Table 20-22. ARG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMDARG	R/W	0h	Command argument 0h = Minimum value FFFFFFFFh = Maximum value

20.4.10 CMD Register (Offset = 20Ch) [Reset = 00000000h]

CMD is shown in Table 20-23.

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Command and data transfer register This register configures the data and command transfers. A write into the most significant byte send the command. A write into SD_CMD[15:0] during data transfer has no effect. This register can be used for any card. In SYSTEST mode, a write to the SD_CMD register will not start a transfer.

Table 20-23. CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-24	IDX	R/W	0h	Command index Binary encoded value from 0 to 63 specifying the command number to send to card. Examples: - INDEX = 7h, sends CMD7 to the card - INDEX = 29h, sends CMD41 to the card 0h = Minimum value 3Fh = Maximum value
23-22	CMDTYP	R/W	0h	Command type This bitfield specifies three types of special commands: - Suspend - Resume - Abort The bitfield is cleared to 0 for all other commands. 0h = Others commands 1h = Upon CMD52 "Bus Suspend" operation 2h = Upon CMD52 "Function Select" operation 3h = Upon CMD12 or CMD52 "I/O Abort" command
21	DP	R/W	0h	Data present select This register indicates that data is present and DAT line(s) shall be used. It must be cleared to 0 in the following conditions: - Command using only CMD line - Command with no data transfer but using busy signal on DAT[0] line - Resume command 0h = Command with no data transfer 1h = Command with data transfer
20	CICE	R/W	0h	Command Index check enable If this bit is set to 1, the host checks the index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked. 0h = Index check disable 1h = Index check enable
19	CCCE	R/W	0h	Command CRC check enable If this bit is set to 1, the host checks the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. 0h = CRC field check disable 1h = CRC field check enable
18	RESERVED	R	0h	Reserved
17-16	RSPTYPE	R/W	0h	Response type This bits defines the response type of the command. 0h = No response 1h = Response Length 136 bits 2h = Response Length 48 bits 3h = Response Length 48 bits with busy after response
15-6	RESERVED	R	0h	Reserved
5	MSBS	R/W	0h	Multi/Single block select This bit must be set to 1 for data transfer in case of multi block command. For any others command this bit must be cleared to 0. 0h = Single block 1h = Multiple block
4	DDIR	R/W	0h	Data transfer Direction Select This bit defines the data transfer direction 0h = Data Write (host to card) 1h = Data Read (card to host)

Table 20-23. CMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	ACEN	R/W	0h	Auto CMD Enable This field determines use of auto command functions. There are two methods to stop Multiple-block read and write operation (1) Auto CMD12 Enable When this field is set to 01b, the Host Controller issues CMD12 automatically when last block transfer is completed. Auto CMD12 error is indicated to the Auto CMD Error Status register. The Host Driver shall not set this bit if the command does not require CMD12. In particular, secure commands defined in the Part 3 File Security specification do not require CMD12. (2) Auto CMD23 Enable When this bit field is set to 10b, the Host Controller issues a CMD23 automatically before issuing a command specified in the Command Register. The Host Controller Version 3.00 and later shall support this function. The following conditions are required to use the Auto CMD23. - Auto CMD23 Supported (Host Controller Version is 3.00 or later) - A memory card that supports CMD23 (SCR[33]=1) - If DMA is used, it shall be ADMA. - Only when CMD18 or CMD25 is issued (Note, the Host Controller does not check command index.) Auto CMD23 can be used with or without ADMA. By writing the Command register, the Host Controller issues a CMD23 first and then issues a command specified by the Command Index in Command register. If response errors of CMD23 are detected, the second command is not issued. A CMD23 error is indicated in the Auto CMD Error Status register. 32-bit block count value for CMD23 is set to SDMA System Address / Argument 2 register. 0h = Auto CMD12 disable 1h = Auto CMD12 enable or CCS detection enabled 2h = Auto CMD23 enable
1	BCE	R/W	0h	Block Count Enable This bit is used to enable the Block count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer. 0h = Block count disabled for infinite transfer 1h = Block count enabled for multiple block transfer with known number of blocks
0	DE	R/W	0h	DMA enable DMA can be enabled only if DMA Support bit in the Capabilities register is set. If this bit is set to 1, a DMA operation starts when the host writes to the upper byte of Command register (00Fh). 0h = DMA mode disable 1h = DMA mode enable

20.4.11 RSP10 Register (Offset = 210h) [Reset = 00000000h]

RSP10 is shown in Table 20-24.

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Response register 10 This 32-bit register holds bits positions [31:0] of command response type R1, R1b, R2, R3, R4, R5, R5b or R6.

Table 20-24. RSP10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RSP1	R	0h	Command Response [31:16] 0h = Minimum value FFFFh = Maximum value
15-0	RSP0	R	0h	Command Response [15:0] 0h = Minimum value FFFFh = Maximum value

20.4.12 RSP32 Register (Offset = 214h) [Reset = 00000000h]

RSP32 is shown in Table 20-25.

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Response register 32 This 32-bit register holds bits positions [63:32] of command response type R2.

Table 20-25. RSP32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RSP3	R	0h	Command Response [63:48] 0h = Minimum value FFFFh = Maximum value
15-0	RSP2	R	0h	Command Response [47:32] 0h = Minimum value FFFFh = Maximum value

20.4.13 RSP54 Register (Offset = 218h) [Reset = 00000000h]

RSP54 is shown in Table 20-26.

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Response register 54 This 32-bit register holds bits positions [95:64] of command response type R2.

Table 20-26. RSP54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RSP5	R	0h	Command Response [95:80] 0h = Minimum value FFFFh = Maximum value
15-0	RSP4	R	0h	Command Response [79:64] 0h = Minimum value FFFFh = Maximum value

20.4.14 RSP76 Register (Offset = 21Ch) [Reset = 00000000h]

RSP76 is shown in Table 20-27.

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Response register 76 This 32-bit register holds bits positions [127:96] of command response type R2.

Table 20-27. RSP76 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RSP7	R	0h	Command Response [127:112] 0h = Minimum value FFFFh = Maximum value
15-0	RSP6	R	0h	Command Response [111:96] 0h = Minimum value FFFFh = Maximum value

20.4.15 DATA Register (Offset = 220h) [Reset = 00000000h]

DATA is shown in Table 20-28.

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Data register This register is the 32-bit entry point of the buffer for read or write data transfers. The buffer size is 32bits x 256 (1024 bytes). Bytes within a word are stored and read in little endian format. This buffer can be used as two 512 byte buffers to transfer data efficiently without reducing the throughput. Sequential and contiguous access is necessary to increment the pointer correctly. Random or skipped access is not allowed. If the local host accesses this register byte-wise or 16bit-wise, the least significant byte (bits [7:0]) must always be written/read first. The update of the buffer address is done on the most significant byte write.

Table 20-28. DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Buffer data register In functional mode (SD_CON.MODE = FUNC): - a read access to this register is allowed only when the buffer read enable status is set to 1 (SD_PSTATE.BREN), otherwise a bad access (SD_STAT.BADA) is signaled. - a write access to this register is allowed only when the buffer write enable status is set to 1 (SD_PSTATE.BWEN), otherwise a bad access (SD_STAT.BADA) is signaled and the data is not written. 0h = Minimum value FFFFFFFFh = Maximum value

20.4.16 PSTATE Register (Offset = 224h) [Reset = 00000000h]

PSTATE is shown in Table 20-29.

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SDMMC controller status register The host can get the status of the SDMMC controller from this 32-bit read only register.

Table 20-29. PSTATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	CLEV	R	0h	Command line signal level This status is used to check the CMD line level to recover from errors, and for debugging. 0h = The mmc_cmd line level is 0 1h = The mmc_cmd line level is 1
23-20	DLEV	R	0h	DATA line 0 to 3 signal level Bit 3 reflects DATA[3] signal level. Bit 2 reflects DATA[2] signal level. Bit 1 reflects DATA[1] signal level. Bit 0 reflects DATA[0] signal level. This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. 0h = Minimum value Fh = Maximum value
19	WP	R	0h	Write Protect This bit reflects the write protect input pin (SDWP) level. 0h = The card is write protected. Note: SD_CON.WPP need to reflect the correct active setting of the write protect input signal (SDWP). 1h = The card is not write protected Note: SD_CON.WPP need to reflect the correct active setting of the write protect input signal (SDWP).
18	CDPL	R	0h	Card Detect Pin Level This bit reflects the inverse value of the card detect input pin (SDCD). 0h = The value of the card detect input pin (SDCD) is 1 1h = The value of the card detect input pin (SDCD) is 0
17	CSS	R	0h	Card State Stable This bit is used for testing. It is set to 1 only when Card Detect Pin Level is stable (SD_PSTATE.CPDL). Debouncing is performed on the card detect input pin (SDCD) to detect card stability. This bit is not affected by software reset. 0h = Card detect pin level is debouncing 1h = Card detect pin level is stable
16	CINS	R	0h	Card inserted This bit is the debounced value of the card detect input pin (SDCD). An inactive to active transition of the card detect input pin (SDCD) will generate a card insertion interrupt (SD_STAT.CINS). An active to inactive transition of the card detect input pin (SDCD) will generate a card removal interrupt (SD_STAT.REM). This bit is not affected by a software reset. 0h = No card is detected Note: SD_CON.CDP need to reflect the correct active level of the write protect input signal (SDCD). 1h = Card is detected Note: SD_CON.CDP need to reflect the correct active level of the write protect input signal (SDCD).
15-12	RESERVED	R	0h	Reserved
11	BRE	R	0h	Buffer read enable This bit is used for non-DMA read transfers. This read only flag indicates that valid data exists in the host side buffer status. If this bit is 1, readable data exists in the buffer. A change of this bit from 1 to 0 occurs when all the block data is read from the buffer. A change of this bit from 0 to 1 occurs when all the block data is ready in the buffer and generates the Buffer Read Ready Interrupt. 0h = Read BLEN bytes disable 1h = Read BLEN bytes enable. Readable data exists in the buffer.

Table 20-29. PSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	BWE	R	0h	Buffer write enable This status is used for non-DMA write transfers. This read only flag indicates if space is available for write data. If this bit is 1, data can be written to the buffer. A change of this bit from 1 to 0 occurs when all the block data is written to the buffer. A change of this bit from 0 to 1 occurs when top of block data can be written to the buffer and generates the Buffer Write Ready Interrupt. 0h = There is no room left in the buffer to write BLEN bytes of data. 1h = There is enough space in the buffer to write BLEN bytes of data
9	RTA	R	0h	Read transfer active (SD mode only) This status is used for detecting completion of a read transfer. This bit is set to 1 for either of the following conditions: - After the end bit of the read command - When writing a 1 to continue Request in the Block Gap Control register to restart a read transfer This bit is cleared to 0 for either of the following conditions: - When the last data block as specified by block length is transferred to the system. - When all valid data blocks have been transferred to the system and no current block transfers are being sent as a result of the Stop At Block Gap Request set to 1. A transfer complete interrupt is generated when this bit changes to 0. 0h = No valid data 1h = Read data transfer on going
8	WTA	R	0h	Write transfer active This status indicates a write transfer active. If this bit is 0, it means no valid write data exists. This bit is set in either of the following cases: - After the end bit of the write command. - When writing a 1 to Continue Request in the Block Gap Control register to restart a write transfer. This bit is cleared in either of the following cases: - After getting the CRC status of the last data block as specified by the transfer count (Single or Multiple) - After getting a CRC status of any block where data transmission is about to be stopped by a Stop At Block Gap Request. During a write transaction, a Block Gap Event interrupt is generated when this bit is changed to 0, as a result of the Stop At Block Gap Request being set. This status is useful for the host to determine when to issue commands during write busy. 0h = No valid data 1h = Write data transfer on going
7-3	RESERVED	R	0h	Reserved
2	DLA	R	0h	DATA Line Active (SD Mode only) This bit indicates whether one of the DATA lines on SD bus is in use. 0h = mmc_data line inactive 1h = mmc_data line active
1	DATI	R	0h	Command Inhibit (DAT) (SD Mode Only) This status bit is generated if either the DAT Line Active or the Read transfer Active is set to 1. If this bit is 0, it indicates the host can issue the next SD command. Commands with busy signal belong to Command Inhibit (DAT) (ex. R1b, R5b type). Changing from 1 to 0 generates a Transfer Complete interrupt. Note: The SD Host Driver can save registers in the range of 000-00Dh for a suspend transaction after this bit has changed from 1 to 0. 0h = Issuing of command using the DAT lines is allowed 1h = Issuing of command using DAT lines is not allowed

Table 20-29. PSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CMDI	R	0h	Command Inhibit (CMD) (SD Mode Only) If this bit is 0, it indicates the CMD line is not in use and the host can issue a SD command using the CMD line. This bit is set immediately after the Command register (00Fh) is written. This bit is cleared when the command response is received. Even if the Command Inhibit (DAT) is set to 1, Commands using only the CMD line can be issued if this bit is 0. Changing from 1 to 0 generates a Command complete interrupt. If the host cannot issue the command because of a command conflict error or because of Command Not Issued By Auto CMD12 Error, this bit shall remain 1 and the Command Complete is not set. Status issuing Auto CMD12 is not read from this bit. Auto CMD12 and Auto CMD23 consist of two responses. In this case, this bit is not cleared by the response of CMD12 or CMD23 but cleared by the response of a read/write command. Status issuing Auto CMD12 is not read from this bit. So if a command is issued during Auto CMD12 operation, Host Controller shall manage to issue two commands: CMD12 and a command set by Command register. 0h = Issuing of command using mmc_cmd line is allowed 1h = Issuing of command using mmc_cmd line is not allowed

20.4.17 HCTL Register (Offset = 228h) [Reset = 00000000h]

HCTL is shown in Table 20-30.

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Host Control Register This register defines the host controls to set power, wakeup and transfer parameters. SD_HCTL[31:24] = Wakeup control SD_HCTL[23:16] = Block gap control SD_HCTL[15:8] = Power control SD_HCTL[7:0] = Host control

Table 20-30. HCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27	RESERVED	R	0h	Reserved
26	RESERVED	R	0h	Reserved
25	RESERVED	R	0h	Reserved
24	RESERVED	R	0h	Reserved
23-20	RESERVED	R	0h	Reserved
19	IBG	R/W	0h	Interrupt block at gap This bit is valid only in 4-bit mode of SDIO card to enable interrupt detection in the interrupt cycle at block gap for a multiple block transfer. For MMC cards and for SD card this bit should be cleared to 0. 0h = Disable interrupt detection at the block gap in 4-bit mode 1h = Enable interrupt detection at the block gap in 4-bit mode
18	RWC	R/W	0h	Read wait control The read wait function is optional only for SDIO cards. If the card supports read wait, this bit must be enabled, then requesting a stop at block gap (SD_HCTL.SBGR) generates a read wait period after the current end of block. Note: If read wait is not supported it may cause a conflict on mmc_dat line. 0h = Disable read wait control. Suspend/resume cannot be supported 1h = Enable read wait control
17	CR	R/W	0h	Continue request This bit is used to restart a transaction that was stopped by requesting a stop at block gap (SD_HCTL[16] SBGR bit). Set this bit to 1 restarts the transfer. The bit is automatically cleared to 0 by the host controller when transfer has restarted, that is, mmc_dat line is active (SD_PSTATE.DLA) or transferring data (SD_PSTATE.WTA). The Stop at block gap request must be disabled (SD_HCTL[16] SBGR bit =0) before setting this bit. 0h = No effect 1h = Transfer restart
16	SBGR	R/W	0h	Stop at block gap request This bit is used to stop executing a transaction at the next block gap. The transfer can restart with a continue request (SD_HCTL.CR) or during a suspend/resume sequence. In case of read transfer, the card must support read wait control. In case of write transfer, the host driver must set this bit after all block data written. Until the transfer completion (SD_STAT.TC bit set to 1), the host driver must leave this bit set to 1. If this bit is set, the local host may not write to the data register (DATA). 0h = Transfer mode 1h = Stop at block gap
15-12	RESERVED	R	0h	Reserved
11-9	SDVS	R/W	0h	SD bus voltage select (All cards). The host driver should set these bits to select the voltage level for the card according to the voltage supported by the system (SD_CAPA[26] VS18 bit, SD_CAPA[25] VS30 bit, SD_CAPA[24] VS33 bit) before starting a transfer. 5h = 1.8V (Typical) 6h = 3.0V (Typical) 7h = 3.3V (Typical)

Table 20-30. HCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SDBP	R/W	0h	SD bus power. Before setting this bit, the host driver shall select the SD bus voltage (SD_HCTL[11:9] SDVS bits). If the host controller detects the No card state, this bit is automatically cleared to 0. If the module is power off, a write in the command register (SD_CMD) will not start the transfer. A write to this bit has no effect if the selected SD bus voltage is not supported according to capability register (SD_CAPA[26] VS18 bit, SD_CAPA[25] VS30 bit or SD_CAPA[24] VS33 bit). 0h = Power off 1h = Power on
7	CDSS	R/W	0h	Card Detect Signal Selection This bit selects the source for the card detection. When the source for the card detection is switched, the Card insertion and removal interrupts should be disabled to avoid unexpected interrupts. In Card Detect Test Level mode, the card insertion and removal signal can be controlled by SD_HCTL.CDTL. 0h = SDCD signal is selected (for normal use) 1h = The Card Detect Test Level is selected (for test purposes)
6	CDTL	R/W	0h	Card Detect Test Level This bit is only functional when the Card Detect Signal Selection selects the Card Detect Test Level mode (SD_HCTL.CDSS = 1). 0h = No card 1h = Card inserted
5	RESERVED	R	0h	Reserved
4-3	RESERVED	R	0h	Reserved
2	HSPE	R/W	0h	High Speed Enable Before setting this bit, the Host Driver shall check the High Speed Support in the Capabilities register. If this bit is cleared to 0 (default), the Host Controller outputs CMD line and DAT lines at the falling edge of the SD Clock. If this bit is set to 1, the Host Controller outputs CMD line and DAT lines at the rising edge of the SD Clock. 0h = Normal speed mode 1h = High speed mode
1	DTW	R/W	0h	Data transfer width This bit must be set following a valid SET_BUS_WIDTH command (ACMD6) with the value written in bit 1 of the argument. Prior to this command, the SD card configuration register (SCR) must be verified for the supported bus width by the SD card. 0h = 1-bit Data width (mmc_dat0 used) 1h = 4-bit Data width (mmc_dat[3:0] used)
0	RESERVED	R	0h	Reserved

20.4.18 SYSCTL Register (Offset = 22Ch) [Reset = 00000000h]

SYSCTL is shown in Table 20-31.

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SD System Control Register This register defines the system controls clock frequency management and data timeout. SD_SYSCTL[23:16] = Timeout control SD_SYSCTL[15:0] = Clock control

Table 20-31. SYSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26	SRD	R/W	0h	Software reset for mmc_dat line This bit is set to 1 for reset and released to 0 when completed. Note: This subreset should not to be used by software, as it can lead to unexpected side-effects. Reset of the SDMMC module should always be through GPRCM.RSTCTL.RESETASSERT 0h = Reset completed 1h = Reset asserted
25	SRC	R/W	0h	Software reset for mmc_cmd line This bit is set to 1 for reset and released to 0 when completed. Note: This subreset should not to be used by software, as it can lead to unexpected side-effects. Reset of the SDMMC module should always be through GPRCM.RSTCTL.RESETASSERT 0h = Reset completed 1h = Reset asserted
24	SRA	R/W	0h	Software reset for all This bit is set to 1 for reset, and released to 0 when completed. Note: This subreset should not to be used by software, as it can lead to unexpected side-effects. Reset of the SDMMC module should always be through GPRCM.RSTCTL.RESETASSERT 0h = Reset completed 1h = Reset asserted
23-20	RESERVED	R	0h	Reserved
19-16	DTO	R/W	0h	Data timeout counter value and busy timeout This value determines the interval to detect mmc_dat lines timeouts. The host driver needs to set this bitfield based on: - the maximum read access time (NAC) (Refer to the SD Specification Part1 Physical Layer) - the data read access time values (TAAC and NSAC) in the card specific data register (CSD) of the card - the timeout clock base frequency (SD_CAPA.TCF) If the card does not respond within the specified number of cycles, a data timeout error occurs (SD_STAT.DTO). The Data timeout counter can also be used to check busy duration, to generate busy timeout for commands with busy response or for busy programming during a write command. Timeout on CRC status is generated if no CRC token is present after a block write. 0h = TCF x 2^{13} 1h = TCF x 2^{14} Eh = TCF x 2^{27} Fh = Reserved 0h = Minimum value Eh = Maximum value
15-6	CLKD	R/W	0h	Clock frequency select This bitfield defines the ratio between a reference clock frequency (system dependent) and the output clock frequency on the mmc_clk pin of the memory card (MMC, SD, or SDIO). 0h = Clock Ref bypass 1h = Clock Ref bypass 2h = Clock Ref / 2 3h = Clock Ref / 3 3FFh = Clock Ref / 1023 0h = Minimum value 3FFh = Maximum value
5-3	RESERVED	R	0h	Reserved
2	CEN	R/W	0h	Card clock enable This bit controls the clock to the card. 0h = The clock is not provided to the card . Clock frequency can be changed. 1h = The clock is provided to the card and can be automatically gated when SD_SYSCONFIG.AUTOIDLE bit is set to 1 (default value). The host driver must wait to set this bit to 1 until the internal clock is stable (SYSSTAT.ICS).

Table 20-31. SYSCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ICS	R	0h	Internal clock stable (status) This bit indicates that the internal clock is stable 0h = The internal clock is not stable 1h = The internal clock is stable after enabling the clock (SD_SYSCTL.ICEN) or after changing the clock ratio (SD_SYSCTL.CLKD).
0	ICE	R/W	0h	Internal clock enable This bit controls the internal clock activity. In very low power state, the internal clock is stopped. Note: The activity of the debounce clock (used for wake-up events) and the interface clock (used for reads and writes to the module register map) are not affected by this register. 0h = The internal clock is stopped (very low power state). 1h = The internal clock oscillates and can be automatically gated when SD_SYSCONFIG.AUTOIDLE bit is set to 1 (default value).

20.4.19 STAT Register (Offset = 230h) [Reset = 00000000h]

STAT is shown in Table 20-32.

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The interrupt status regroups all the status of the module internal events that can generate an interrupt. SD_STAT[31:16] = Error Interrupt Status SD_STAT[15:0] = Normal Interrupt Status The error bits are located in the upper 16 bits of the SD_STAT register. All bits are cleared by writing a 1 to them. Additionally, bits 15 and 8 serve as special error bits. These cannot be cleared by writing a 1 to them. Bit 15 (ERRI) is automatically cleared when the error causing to ERRI to be set is handled. (that is, when bits 31:16 are cleared, bit 15 will be automatically cleared). Bit 8 (CIRQ) is cleared by writing a 0 to SD_IE[8] (masking the interrupt) and servicing the interrupt.

Table 20-32. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	BADA	R/W	0h	Bad access to data space. This bit is set automatically to indicate a bad access to buffer when not allowed: During a read access to the data register (SD_DATA) while buffer reads are not allowed (SD_PSTATE[11] BRE bit =0). During a write access to the data register (SD_DATA) while buffer writes are not allowed (SD_PSTATE[10] BWE bit=0). 0h (W) = Status bit unchanged 0h (R) = No interrupt 1h (W) = Status is cleared. 1h (R) = Bad access 0h = No interrupt occured 1h = Interrupt occured
28	CERR	R/W	0h	Card error. This bit is set automatically when there is at least one error in a response of type R1, R1b, R6, R5 or R5b. Only bits referenced as type E (error) in status field in the response can set a card status error. An error bit in the response is flagged only if corresponding bit in card status response error SD_CSRE in set. There is no card error detection for autoCMD12 command. The host driver shall read SD_RSP76 register to detect error bits in the command response. 0h (W) = Status bit unchanged 0h (R) = No error 1h (W) = Status is cleared. 1h (R) = Card error 0h = No interrupt occured 1h = Interrupt occured
27-25	RESERVED	R	0h	Reserved
24	ACE	R/W	0h	Auto CMD12 error. This bit is set automatically when one of the bits in Auto CMD12 Error status register has changed from 0 to 1. 0h (W) = Status bit unchanged 0h (R) = No error 1h (W) = Status is cleared. 1h (R) = AutoCMD12 error 0h = No interrupt occured 1h = Interrupt occured
23	RESERVED	R	0h	Reserved
22	DEB	R/W	0h	Data End Bit error. This bit is set automatically when detecting a 0 at the end bit position of read data on mmc_dat line or at the end position of the CRC status in write mode. 0h (W) = Status bit unchanged 0h (R) = No error 1h (W) = Status is cleared. 1h (R) = Data end bit error 0h = No interrupt occured 1h = Interrupt occured
21	DCRC	R/W	0h	Data CRC Error. This bit is set automatically when there is a CRC16 error in the data phase response following a block read command or if there is a 3-bit CRC status different of a position "010" token during a block write command. 0h (W) = Status bit unchanged 0h (R) = No error 1h (W) = Status is cleared. 1h (R) = Data CRC error 0h = No interrupt occured 1h = Interrupt occured

Table 20-32. STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DTO	R/W	0h	Data timeout error. This bit is set automatically according to the following conditions: Busy timeout for R1b, R5b response type. Busy timeout after write CRC status. Write CRC status timeout. Read data timeout. 0h (W) = Status bit unchanged 0h (R) = No error 1h (W) = Status is cleared. 1h (R) = Time out 0h = No interrupt occured 1h = Interrupt occured
19	CIE	R/W	0h	Command index error. This bit is set automatically when response index differs from corresponding command index previously emitted. It depends on the enable bit (SD_CMD[20] CICE). 0h (W) = Status bit unchanged 0h (R) = No error 1h (W) = Status is cleared. 1h (R) = Command index error 0h = No interrupt occured 1h = Interrupt occured
18	CEB	R/W	0h	Command end bit error. This bit is set automatically when detecting a 0 at the end bit position of a command response. 0h (W) = Status bit unchanged 0h (R) = No error 1h (W) = Status is cleared. 1h (R) = Command end bit error 0h = No interrupt occured 1h = Interrupt occured
17	CCRC	R/W	0h	Command CRC error. This bit is set automatically when there is a CRC7 error in the command response depending on the enable bit (SD_CMD[19] CCCE). 0h (W) = Status bit unchanged 0h (R) = No error 1h (W) = Status is cleared. 1h (R) = Command CRC error 0h = No interrupt occured 1h = Interrupt occured
16	CTO	R/W	0h	Command timeout error. This bit is set automatically when no response is received within 64 clock cycles from the end bit of the command. For commands that reply within 5 clock cycles - the timeout is still detected at 64 clock cycles. 0h (W) = Status bit unchanged 0h (R) = No error 1h (W) = Status is cleared. 1h (R) = Time Out 0h = No interrupt occured 1h = Interrupt occured
15	ERRI	R	0h	Error interrupt. If any of the bits in the Error Interrupt Status register (SD_STAT [31:16]) are set, then this bit is set to 1. Therefore the host driver can efficiently test for an error by checking this bit first. Writes to this bit are ignored. 0h (R) = No interrupt 1h (R) = Error interrupt event(s) occurred 0h = No interrupt occured 1h = Interrupt occured
14-10	RESERVED	R	0h	Reserved
9	OBI	R/W	0h	Out-of-band interrupt (This interrupt is only useful for MMC card). Note: Out-of-band interrupt (OBI) is not supported. 0h = No interrupt occured 1h = Interrupt occured
8	CIRQ	R	0h	Card interrupt. This bit is only used for SD and SDIO cards. In 1-bit mode, interrupt source is asynchronous (can be a source of asynchronous wake-up). In 4-bit mode, interrupt source is sampled during the interrupt cycle. In CE-ATA mode, interrupt source is detected when the card drives mmc_cmd line to zero during one cycle after data transmission end. All modes above are fully exclusive. The controller interrupt must be clear by setting SD_IE[8] CIRQ_ENABLE to 0, then the host driver must start the interrupt service with card (clearing card interrupt status) to remove card interrupt source. Otherwise the Controller interrupt will be reasserted as soon as SD_IE[8] CIRQ_ENABLE is set to 1. Writes to this bit are ignored. 0h (R) = No card interrupt 1h (R) = Generate card interrupt 0h = No interrupt occured 1h = Interrupt occured

Table 20-32. STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CREM	R/W	0h	Card Removal. This bit is set automatically when SD_PSTATE[CINS] changes from 1 to 0. A clear of this bit doesn't affect Card inserted present state (SD_PSTATE[CINS]). 0h (W) = Status bit unchanged 0h (R) = Card State stable or debouncing 1h (W) = Status is cleared 1h (R) = Card Removed 0h = No interrupt occured 1h = Interrupt occured
6	CINS	R/W	0h	Card Insertion. This bit is set automatically when SD_PSTATE[CINS] changes from 0 to 1. A clear of this bit doesn't affect Card inserted present state (SD_PSTATE[CINS]). 0h (W) = Status bit unchanged 0h (R) = Card State stable or debouncing 1h (W) = Status is cleared. 1h (R) = Card inserted 0h = No interrupt occured 1h = Interrupt occured
5	BRR	R/W	0h	Buffer read ready. This bit is set automatically during a read operation to the card (see class 2 - block oriented read commands) when one block specified by the SD_BLK [10:0] BLEN bit field is completely written in the buffer. It indicates that the memory card has filled out the buffer and that the local host needs to empty the buffer by reading it. Note: If the DMA receive-mode is enabled, this bit is never set instead a DMA receive request to the main DMA controller of the system is generated. 0h (W) = Status bit unchanged 0h (R) = Not ready to read buffer 1h (W) = Status is cleared. 1h (R) = Ready to read buffer 0h = No interrupt occured 1h = Interrupt occured
4	BWR	R/W	0h	Buffer write ready. This bit is set automatically during a write operation to the card (see class 4 - block oriented write command) when the host can write a complete block as specified by SD_BLK [10:0] BLEN. It indicates that the memory card has emptied one block from the buffer and that the local host is able to write one block of data into the buffer. Note: If the DMA transmit mode is enabled, this bit is never set instead, a DMA transmit request to the main DMA controller of the system is generated. 0h (W) = Status bit unchanged 0h (R) = Not ready to write buffer 1h (W) = Status is cleared. 1h (R) = Ready to write buffer 0h = No interrupt occured 1h = Interrupt occured
3	DMA	R/W	0h	DMA Interrupt This status is set when an interrupt is required after the data transfer is complete. 0h = No interrupt occured 1h = Interrupt occured
2	BGE	R/W	0h	Block gap event. When a stop at block gap is requested (SD_HCTL[16] SBGR bit), this bit is automatically set when transaction is stopped at the block gap during a read or write operation. 0h (W) = Status bit unchanged 0h (R) = No block gap event 1h (W) = Status is cleared 1h (R) = Transaction stopped at block gap 0h = No interrupt occured 1h = Interrupt occured
1	TC	R/W	0h	Transfer completed. This bit is always set when a read/write transfer is completed or between two blocks when the transfer is stopped due to a stop at block gap request (SD_HCTL[16] SBGR bit). 0h (W) = Status bit unchanged 0h (R) = No transfer complete 1h (W) = Status is cleared 1h (R) = Data transfer complete 0h = No interrupt occured 1h = Interrupt occured

Table 20-32. STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CC	R/W	0h	Command complete. This bit is set when a 1-to-0 transition occurs in the register command inhibit (SD_PSTATE[0] CMDI bit) 0h (W) = Status bit unchanged 0h (R) = No command complete 1h (W) = Status is cleared 1h (R) = Command complete 0h = No interrupt occured 1h = Interrupt occured

20.4.20 IE Register (Offset = 234h) [Reset = 00000000h]

IE is shown in Table 20-33.

Return to the Summary Table.

This register allows to enable/disable the module to set status bits on an event-by-event basis. SD_IE[31:16] = Error Interrupt Status Enable SD_IE[15:0] = Normal Interrupt Status Enable

Table 20-33. IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	BADAEN	R/W	0h	Bad access to data space interrupt enable 0h = Interrupt masked 1h = Interrupt enabled
28	CERREN	R/W	0h	Card error interrupt enable 0h = Interrupt masked 1h = Interrupt enabled
27	RESERVED	R	0h	Reserved
26	NOUSE1	R/W	0h	No use Note: Writing values other than 0 might produce undesired results. Always set this bits to 0. 0h = Minimum value 1h = Maximum value
25	ADMAEEN	R/W	0h	ADMA Error Status Enable Note: This functionality is not supported, since MADMA_EN is set to 0 in the design. 0h = Interrupt masked 1h = Interrupt enabled
24	ACEEN	R/W	0h	Auto CMD12 error interrupt enable 0h = Interrupt masked 1h = Interrupt enabled
23	RESERVED	R	0h	Reserved
22	DEBEN	R/W	0h	Data end bit error interrupt enable 0h = Interrupt masked 1h = Interrupt enabled
21	DCRCEN	R/W	0h	Data CRC error interrupt enable 0h = Interrupt masked 1h = Interrupt enabled
20	DTOEN	R/W	0h	Data timeout error interrupt enable 0h = Interrupt masked 1h = Interrupt enabled
19	CIEEN	R/W	0h	Command index error interrupt enable 0h = Interrupt masked 1h = Interrupt enabled
18	CEBEN	R/W	0h	Command end bit error interrupt enable 0h = Interrupt masked 1h = Interrupt enabled
17	CCRCEN	R/W	0h	Command CRC error interrupt enable 0h = Interrupt masked 1h = Interrupt enabled
16	CTOEN	R/W	0h	Command timeout error interrupt enable 0h = Interrupt masked 1h = Interrupt enabled
15	NULL	R	0h	Fixed to 0. The host driver shall control error interrupts using the Error Interrupt Signal Enable register. Writes to this bit are ignored. 0h = Interrupt masked 1h = Interrupt enabled
14-11	RESERVED	R	0h	Reserved

Table 20-33. IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NOUSE0	R/W	0h	No use Note: Writing values other than 0 might produce undesired results. Always set this bits to 0. 0h = Minimum value 1h = Maximum value
9	OBIEN	R/W	0h	Out-of-band interrupt enable A write to this register when SD_CON[14] OBIE is cleared to 0 is ignored. Note: The OBI functionallity is not supported! 0h = Interrupt masked 1h = Interrupt enabled
8	CIRQEN	R/W	0h	Card interrupt enable. A clear of this bit also clears the corresponding status bit. During 1-bit mode, if the interrupt routine does not remove the source of a card interrupt in the SDIO card, the status bit is reasserted when this bit is set to 1. 0h = Interrupt masked 1h = Interrupt enabled
7	CREMEN	R/W	0h	Card Removal interrupt Enable 0h = Interrupt masked 1h = Interrupt enabled
6	CINSEN	R/W	0h	Card Insertion interrupt Enable 0h = Interrupt masked 1h = Interrupt enabled
5	BRREN	R/W	0h	Buffer read ready interrupt enable 0h = Interrupt masked 1h = Interrupt enabled
4	BWREN	R/W	0h	Buffer write ready interrupt enable 0h = Interrupt masked 1h = Interrupt enabled
3	DMAEN	R/W	0h	DMA interrupt enable 0h = Interrupt masked 1h = Interrupt enabled
2	BGEEN	R/W	0h	Block gap event interrupt enable 0h = Interrupt masked 1h = Interrupt enabled
1	TCEN	R/W	0h	Transfer completed interrupt enable 0h = Interrupt masked 1h = Interrupt enabled
0	CCEN	R/W	0h	Command completed interrupt enable 0h = Interrupt masked 1h = Interrupt enabled

20.4.21 ISE Register (Offset = 238h) [Reset = 00000000h]

ISE is shown in Table 20-34.

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This register allows to enable/disable the module internal interrupt signaling on an event-by-event basis. SD_ISE[31:16] = Error Interrupt Signal Enable SD_ISE[15:0] = Normal Interrupt Signal Enable

Table 20-34. ISE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	BADASEN	R/W	0h	Bad access to data space interrupt enable 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled
28	CERRSEN	R/W	0h	Card error interrupt signal status enable 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled
27	RESERVED	R	0h	Reserved
26	NOUSE1	R/W	0h	No use Note: Writing values other than 0 might produce undesired results. Always set this bit to 0. 0h = Always set this bit to 0 1h = Do not set this bit
25	ADMAESEN	R/W	0h	ADMA Error Signal Enable Note: This functionality is not supported, since MADMA_EN is set to 0 in the design. 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled
24	ACESEN	R/W	0h	Auto CMD12 error signal status enable 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled
23	RESERVED	R	0h	Reserved
22	DEBSEN	R/W	0h	Data end bit error signal status enable 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled
21	DCRCSEN	R/W	0h	Data CRC error signal status enable 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled
20	DTOSEN	R/W	0h	Data timeout error signal status enable 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled
19	CIESEN	R/W	0h	Command index error signal status enable 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled
18	CEBSEN	R/W	0h	Command end bit error signal status enable 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled
17	CCRCSEN	R/W	0h	Command CRC error signal status enable 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled
16	CTOSEN	R/W	0h	Command timeout error signal status enable 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled
15	NULL	R	0h	Fixed to 0. The host driver shall control error interrupts using the Error Interrupt Signal Enable register. Writes to this bit are ignored. 0h = Interrupt masked 1h = Interrupt enabled
14-11	RESERVED	R	0h	Reserved

Table 20-34. ISE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NOUSE0	R/W	0h	No use Note: Writing values other than 0 might produce undesired results. Always set this bit to 0. 0h = Always set this bit to 0 1h = Do not set this bit
9	OBISEN	R/W	0h	Out-of-band interrupt signal status enable. A write to this register when SD_CON[14] OBIE is cleared to 0 is ignored. Note: The OBI functionallity is not supported! 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled
8	CIRQSEN	R/W	0h	Card interrupt signal status enable. A clear of this bit also clears the corresponding status bit. During 1-bit mode, if the interrupt routine does not remove the source of a card interrupt in the SDIO card, the status bit is reasserted when this bit is set to 1. 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled
7	CREMSEN	R/W	0h	Card Removal signal status enable 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled
6	CINSSEN	R/W	0h	Card Insertion signal status enable. 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled
5	BRRSEN	R/W	0h	Buffer read ready signal status enable 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled
4	BWRSEN	R/W	0h	Buffer write ready signal status enable 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled
3	DMASEN	R/W	0h	DMA signal status enable 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled
2	BGESEN	R/W	0h	Block gap event signal status enable 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled
1	TCSEN	R/W	0h	Transfer completed signal status enable 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled
0	CCSEN	R/W	0h	Command completed signal status enable 0h = Status Interrupt signaling disabled 1h = Status Interrupt signaling enabled

20.4.22 AC12 Register (Offset = 23Ch) [Reset = 00000000h]

AC12 is shown in Table 20-35.

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SD_AC12 Error register The host driver may determine which of the errors cases related to Auto CMD12 has occurred by checking this SD_AC12 register when an auto CMD12 error interrupt occurs. This register is valid only when auto CMD12 is enabled (SD_CMD.ACEN) and auto CMD12Error (SD_STAT.ACE) is set to 1. These bits are automatically reset when starting a new adtc command with data.

Table 20-35. AC12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOUSE1	R/W	0h	No use Note: Writing values other than 0 might produce undesired results. Always set this bit to 0. 0h = Always set this bit to 0 1h = Do not set this bit
30	AIEN	R/W	0h	Asynchronous Interrupt Enable This bit can be set to 1 if a card supports asynchronous interrupts and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode (and zero is set to Interrupt Pin Select in the Shared Bus Control register). If this bit is set to 1, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver the Card Interrupt to the host when it is asserted by the Card. 0h = Asynchronous Interrupt disabled 1h = Asynchronous Interrupt enabled
29-24	RESERVED	R	0h	Reserved
23-22	NOUSE0	R/W	0h	No use Note: Writing values other than 0 might produce undesired results. Always set this bit to 0. 0h = Always set this bit to 0 1h = Do not set this bit
21-20	DSSEL	R/W	0h	Driver Strength Select Host Controller output driver in 1.8V signaling is selected by this bit. In 3.3V signaling, this field is not effective. This field can be set depends on Driver Type A, C and D support bits in the Capabilities register. 0h = Driver Type B is selected 1h = Driver Type A is selected 2h = Driver Type C is selected 3h = Driver Type D is selected
19	V1P8SEN	R/W	0h	1.8V Signaling Enable This bit controls voltage regulator for I/O cell. 3.3V is supplied to the card regardless of signaling voltage. Setting this bit from 0 to 1 starts changing signal voltage from 3.3V to 1.8V. 1.8V regulator output shall be stable within 5ms. Host Controller clears this bit if switching to 1.8V signaling fails. Clearing this bit from 1 to 0 starts changing signal voltage from 1.8V to 3.3V. 3.3V regulator output shall be stable within 5ms. Host Driver can set this bit to 1 when Host Controller supports 1.8V signaling (One of support bits is set to 1: SDR50, SDR104 or DDR50 in the Capabilities register) and the card or device supports UHS-I (S18A=1. Refer to Bus Signal Voltage Switch Sequence in the Physical Layer Specification Version 3.0x). Note: Dragon supports only 3.3V. Always set this bit to 0. 0h = 3.3V Signaling 1h = 1.8V Signaling

Table 20-35. AC12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-16	UHSMS	R/W	0h	UHS Mode Select This field is used to select one of UHS-I modes or e.MMC HS200 mode and effective when 1.8V Signaling Enable is set to 1. Note: Dragon does not support 1.8V signaling and UHS modes. Always set this bitfield to 0. 0h = SDR12 1h = SDR25 2h = SDR50 3h = SDR104 / HS200 4h = DDR50
15-8	RESERVED	R	0h	Reserved
7	CNI	R	0h	Command not issue by auto CMD12 error If this bit is set to 1, a pending command is not executed due to auto CMD12 error ACEB, ACCE, ACTO, or ACNE. 0h = No error 1h = Error occurred
6-5	RESERVED	R	0h	Reserved
4	ACIE	R	0h	Auto CMD12 index error This bit is a set to 1 when response index differs from corresponding command auto CMD12 index previously emitted. This bit depends on the command index check enable (SD_CMD.CICEN). 0h = No error 1h = Error occurred
3	ACEB	R	0h	Auto CMD12 end bit error. This bit is set to 1 when detecting a 0 at the end bit position of auto CMD12 command response. 0h = No error 1h = Error occurred
2	ACCE	R	0h	Auto CMD12 CRC error. This bit is set to 1 when a CRC7 error is detected in the auto CMD12 command response. 0h = No error 1h = Error occurred
1	ACTO	R	0h	Auto CMD12 timeout error. This bit is set to 1 if no response is received within 64 clock cycles from the end bit of the auto CMD12 command. 0h = No error 1h = Error occurred
0	ACNE	R	0h	Auto CMD12 not executed. This bit is set to 1 if multiple block data transfer command has started and if an error occurs in command before auto CMD12 starts. 0h = Auto CMD12 executed 1h = Auto CMD12 not executed

20.4.23 CAPA Register (Offset = 240h) [Reset = 20E10080h]

CAPA is shown in Table 20-36.

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Capability register This register lists the capabilities of the MMC/SD/SDIO host controller.

Table 20-36. CAPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	AIS	R	1h	Asynchronous Interrupt Support Refer to SDIO Specification Version 3.00 about asynchronous interrupt. 0h = Not supported 1h = Supported
28	BUS64BIT	R	0h	64 Bit System Bus Support Setting 1 to this bit indicates that the Host Controller supports 64-bit address descriptor mode and is connected to 64-bit address system bus. 0h (R) = 32-bit System bus address 1h (R) = 64-bit System bus address 0h = Not supported 1h = Supported
27	RESERVED	R	0h	Reserved
26	VS18	R/W	0h	Voltage support 1.8 V Initialization of this register (via a write access to this register) depends on the system capabilities. The host driver shall not modify this register after the initialization. This register is only reinitialized by a hard reset (via mmc_RESET signal). 0h (W) = 1.8 V not supported 0h (R) = 1.8 V not supported 1h (W) = 1.8 V supported 1h (R) = 1.8 V supported 0h = Not supported 1h = Supported
25	VS30	R/W	0h	Voltage support 3.0V Initialization of this register (via a write access to this register) depends on the system capabilities. The host driver shall not modify this register after the initialization. This register is only reinitialized by a hard reset (via mmc_RESET signal). 0h (W) = 3.0 V not supported 0h (R) = 3.0 V not supported 1h (W) = 3.0 V supported 1h (R) = 3.0 V supported 0h = Not supported 1h = Supported
24	VS33	R/W	0h	Voltage support 3.3V Initialization of this register (via a write access to this register) depends on the system capabilities. The host driver shall not modify this register after the initialization. This register is only reinitialized by a hard reset (via mmc_RESET signal). 0h (W) = 3.3 V not supported 0h (R) = 3.3 V not supported 1h (W) = 3.3 V supported 1h (R) = 3.3 V supported 0h = Not supported 1h = Supported
23	SRS	R	1h	Suspend/resume support (SDIO cards only). This bit indicates whether the host controller supports suspend/resume functionality. 0h = Not supported 1h = Supported
22	DS	R	1h	DMA support This bit indicates that the Host controller is able to use DMA to transfer data between system memory and the Host controller directly. 0h = Not supported 1h = Supported
21	HSS	R	1h	High-speed support This bit indicates that the host controller supports high speed operations and can supply an up-to-52 MHz clock to the card. 0h = Not supported 1h = Supported
20	RESERVED	R	0h	Reserved

Table 20-36. CAPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	AD2S	R	0h	This bit indicates whether the Host Controller is capable of using ADMA2. 0h = Not supported 1h = Supported
18	RESERVED	R	0h	Reserved
17-16	MBL	R	1h	Maximum block length This value indicates the maximum block size that the host driver can read and write to the buffer in the host controller. The host controller supports 512 bytes and 1024 bytes block transfers. 0h = 512 bytes 1h = 1024 bytes 2h = 2048 bytes 0h = Minimum value 3h = Maximum value
15-14	RESERVED	R	0h	Reserved
13-8	BCF	R	0h	Base clock frequency for clock provided to the card. ARRAY(0x1bfe1b0) 0h = Minimum value 3Fh = Maximum value
7	TCU	R	1h	Timeout clock unit This bit shows the unit of base clock frequency used to detect Data Timeout Error. 0h = kHz 1h = MHz
6	RESERVED	R	0h	Reserved
5-0	TCF	R	0h	Timeout clock frequency The timeout clock frequency is used to detect Data Timeout Error (DTO interrupt). The timeout clock frequency depends on the frequency of the clock provided to the card. The value of the timeout clock frequency is not available in this register. 0h = Minimum value 3Fh = Maximum value

20.4.24 CURCAPA Register (Offset = 248h) [Reset = 00000000h]

CURCAPA is shown in Table 20-37.

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Current capability register This register indicates the maximum current capability for each voltage.

Table 20-37. CURCAPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	CUR18	R/W	0h	Maximum current for 1.8V The maximum current capability for this voltage is not available. Feature not implemented. 0h = Minimum value FFh = Maximum value
15-8	CUR30	R/W	0h	Maximum current for 3.0V The maximum current capability for this voltage is not available. Feature not implemented. 0h = Minimum value FFh = Maximum value
7-0	CUR33	R/W	0h	Maximum current for 3.3V The maximum current capability for this voltage is not available. Feature not implemented. 0h = Minimum value FFh = Maximum value

20.4.25 FE Register (Offset = 250h) [Reset = 00000000h]

FE is shown in Table 20-38.

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The Force Event register is not a physically implemented register. Rather, it is an address at which the Error Interrupt Status register can be written. The effect of a write to this address will be reflected in the Error Interrupt Status Register, if corresponding bit of the Error Interrupt Status Enable Register is set.

Table 20-38. FE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	BADA	W	0h	Force Event Bad access to data space 0h = No interrupt 1h = Interrupt forced
28	CERR	W	0h	Force Event Card error 0h = No interrupt 1h = Interrupt forced
27-25	RESERVED	R	0h	Reserved
24	ACE	W	0h	Force Event Auto CMD12 error 0h = No interrupt 1h = Interrupt forced
23	RESERVED	R	0h	Reserved
22	DEB	W	0h	Force Event Data End Bit error 0h = No interrupt 1h = Interrupt forced
21	DCRC	W	0h	Force Event Data CRC error 0h = No interrupt 1h = Interrupt forced
20	DTO	W	0h	Force Event Data timeout error 0h = No interrupt 1h = Interrupt forced
19	CIE	W	0h	Force Event Command index error 0h = No interrupt 1h = Interrupt forced
18	CEB	W	0h	Force Event Command end bit error 0h = No interrupt 1h = Interrupt forced
17	CCRC	W	0h	Force Event Comemand CRC error 0h = No interrupt 1h = Interrupt forced
16	CTO	W	0h	Force Event Command Timeout error 0h = No interrupt 1h = Interrupt forced
15-8	RESERVED	R	0h	Reserved
7	CNI	W	0h	Force Event Command not issue by Auto CMD12 error 0h = No interrupt 1h = Interrupt forced
6-5	RESERVED	R	0h	Reserved
4	ACIE	W	0h	Force Event Auto CMD12 index error 0h = No interrupt 1h = Interrupt forced
3	ACEB	W	0h	Force Event Auto CMD12 end bit error 0h = No interrupt 1h = Interrupt forced
2	ACCE	W	0h	Force Event Auto CMD12 CRC error 0h = No interrupt 1h = Interrupt forced

Table 20-38. FE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ACTO	W	0h	Force Event Auto CMD12 timeout error 0h = No interrupt 1h = Interrupt forced
0	ACNE	W	0h	Force Event Auto CMD12 not executed. 0h = No interrupt 1h = Interrupt forced

20.4.26 REV Register (Offset = 2FCh) [Reset = 33020000h]

REV is shown in Table 20-39.

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Revision register This register contains the hard coded RTL vendor revision number, the version number of SD specification compliancy.

Table 20-39. REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	VREV	R	33h	Vendor Version Number Bits 7 to 4 are the major revision, bits 3 to 0 are the minor revision. Examples: 0x10 for 1.0 and 0x21 for 2.1. Reset value is 0x31. 0h = Minimum value FFh = Maximum value
23-16	SREV	R	2h	Specification Version Number This status indicates the Standard SD Host Controller Specification Version. The upper and lower 4 bits indicate the version. 0h: SD Host Specification Version 1.00. 1h: SD Host Specification Version 2.00. 2h: SD Host Specification Version 3.00. 3h: Reserved 0h = Minimum value FFh = Maximum value
15-1	RESERVED	R	0h	Reserved
0	SIS	R	0h	Slot Interrupt Status This status bit indicates the inverted state of interrupt signal for the module. By a power on reset or by setting a software reset for all, the interrupt signal shall be deasserted and this status shall read 0. 0h = No interrupt is asserted 1h = Interrupt is asserted

20.4.27 TPSEL Register (Offset = 1040h) [Reset = 00000000h]

TPSEL is shown in Table 20-40.

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Test-Port select.

Table 20-40. TPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	VAL	R/W	0h	Test port 0 or 1 0h = 0 1h = 1

20.4.28 DMAMODE Register (Offset = 1048h) [Reset = 00000001h]

DMAMODE is shown in Table 20-41.

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DMA mode select: This register define the behavior of DMA request signal that allow tranmission of data.

Table 20-41. DMAMODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	VAL	R/W	1h	0h = In this case, DMA required to read/write data from SD_DATA register, the value of DMA_INDICATION_SELECT register is d'ont care and the trigger to transmit data from the internal FIFO defined by SD_BLK.BLEN register as a threshold. 1h = DMA required to read/write data from BUFIF register the value of DMA_INDICATION_SELECT define the trigger of the internal FIFO. 0h = Disable to trig the internal FIFO with threshold, using DMA indication instead 1h = Enable to trig the internal FIFO with threshold

20.4.29 DMAIND Register (Offset = 1050h) [Reset = 00000001h]

DMAIND is shown in Table 20-42.

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DMA indication select: This register define the behavior of transmitting data from/to the card using DMA If DMA_MODE_SELECT =1, then the value of of this register is d'ont care, else it define the trigger of the internal FIFO

Table 20-42. DMAIND Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	VAL	R/W	1h	0h = IP transmit the data to/from the card after each DMA 'BLOCK' transmitted. In this case SDMMC.SD_BLK.BLEN shoud be equal to HOST_DMA.JOB_CTRL_CH7.MEM_JOB_CTRL_CHAN_7_BLOCK_SIZE 1h = IP transmit the data to the card after each DMA 'JOB' transmitted. In this case SDMMC.SD_BLK.BLEN shoud be equal to HOST_DMA.TRANS_CTRL_CH7.MEM_TRANS_CTRL_CHAN_7_TRANS_NUM_B 0h = The IP transmit the data to/from the card, after each DMA transmitted block. 1h = The IP transmit the data to/from the card, only in the end of the DMA job.

20.4.30 CLKSEL Register (Offset = 1054h) [Reset = 00000000h]

CLKSEL is shown in Table 20-43.

Return to the Summary Table.

This register define the functional clock frequency, and whether the clock is synchronized to main clock.

Table 20-43. CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	VAL	R/W	0h	0h = 40MHz post-swallowing 1h = 80MHz pro-swallowing 0h = post-swallowing 40MHz clock to main clock 1h = pre-swallowing 80MHz clock

20.4.31 EVTMODE Register (Offset = 10E0h) [Reset = 00000001h]

EVTMODE is shown in Table 20-44.

Return to the Summary Table.

Event mode register. It is used to select whether each line is disabled, in software mode (software clears the RIS) or in hardware mode (hardware clears the RIS)

Table 20-44. EVTMODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	INT0CFG	R/W	1h	Event line mode select for event corresponding to [IPSTANDARD.INT_EVENT0] 0h = The interrupt or event line is disabled. 1h = The interrupt or event line is in software mode. Software must clear the RIS. 2h = The interrupt or event line is in hardware mode. The hardware (another module) clears automatically the associated RIS flag.

20.4.32 DESC Register (Offset = 10FCh) [Reset = 02111000h]

DESC is shown in Table 20-45.

Return to the Summary Table.

This register identifies the peripheral and its exact version.

Table 20-45. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODULEID	R	2111h	Module identification contains a unique peripheral identification number. The assignments are maintained in a central database for all of the platform modules to ensure uniqueness. 0h = Smallest value FFFFh = Highest possible value
15-12	FEATURST	R	0h	Feature Set for the module *instance* 0h = Smallest value Fh = Highest possible value
11-8	INSTNUM	R	0h	Instance Number within the device. This will be a parameter to the RTL for modules that can have multiple instances 0h = Smallest value Fh = Highest possible value
7-4	MAJREV	R	0h	Major rev of the IP 0h = Smallest value Fh = Highest possible value
3-0	MINREV	R	0h	Minor rev of the IP 0h = Smallest value Fh = Highest possible value

20.4.33 SDMMCSTAT Register (Offset = 1100h) [Reset = X0000000h]

SDMMCSTAT is shown in Table 20-46.

Return to the Summary Table.

SDMMC Status register

Table 20-46. SDMMCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	STATE	R	Xh	SDMMC state indication 0h = IP is active but is not transmitting 1h = IP is active and transmitting

20.4.34 BUFIF_y Register (Offset = 1110h + formula) [Reset = 00000000h]

BUFIF_y is shown in Table 20-47.

Return to the Summary Table.

SRAM Data Access Registers These registers are the 32-bit entry point of the SRAM buffer for read or write data transfers to and from the SDMMC card. Data[1] register is an alias for the SD_BUFIF register and needs to be used for normal (non safety, non burst) buffer accesses. Data[1..4] registers need to be used for non safety, incremental VBUSP burst accesses. For safety accesses (write with readback and double read), DataS[1..4] registers need to be used. The SRAM buffer size is 32bits x 256 (1024 bytes). Bytes within a word are stored and read in little endian format. This buffer can be used as two 512 byte buffers to transfer data efficiently without reducing the throughput. Sequential and contiguous access is necessary to increment the pointer correctly. Random or skipped access is not allowed. If the local host accesses this register byte-wise or 16bit-wise, the least significant byte (bits [7:0]) must always be written/read first. The update of the buffer address is done on the most significant byte write.

Offset = 1110h + (y * 4h); where y = 0h to 3h

Table 20-47. BUFIF_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Buffer data register In functional mode (SD_CON.MODE = FUNC): - a read access to this register is allowed only when the buffer read enable status is set to 1 (SD_PSTATE.BREN), otherwise a bad access (SD_STAT.BADA) is signaled. - a write access to this register is allowed only when the buffer write enable status is set to 1 (SD_PSTATE.BWEN), otherwise a bad access (SD_STAT.BADA) is signaled and the data is not written. 0h = Minimum value FFFFFFFFh = Maximum value

20.4.35 CLKCFG Register (Offset = 4000h) [Reset = 00000000h]

CLKCFG is shown in Table 20-48.

Return to the Summary Table.

Clock Enable Register

Table 20-48. CLKCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EN	R/W	0h	Clock Disable / Enable for: * bus_clk (main clock) - 80MHz ; * card_clk (pll_clk) - 40MHz ; * lf_clk (slow_clk) - 32KHz ;

Chapter 21

Secure Digital Input/Output (SDIO)

This section describes the Secure Digital Input/Output (SDIO) module.

21.1 Introduction

The SDIO module in the CC35xx acts as a SDIO card peripheral to an external SDIO host. In this case the "M33" references in this chapter are in regard to the CC35xx applications CPU.

The general features of the SDIO card peripheral IP are:

- 2 built-in buffers
  - 256 bytes for Rx (Host write)
  - 128 bytes for Tx (Host read)
- Two DMA channels
- Support for 4 Data bus
- Clock Support:
  - Max 52MHz functional clock source input from SDIO host
  - Up to 208Mbit/sec (26MByte/sec) in High-Speed mode (52MHz) 4-bit data transfer
  - Up to 20Mbit/sec (2.8MByte/sec) in Default mode (20MHz) 1-bit data transfer
- Data transaction Block/Byte mode
- Support in band and out band IRQ to the external host
- Interrupts for transmit and receive FIFOs, overrun and underrun interrupts
- Support busy state on SDIO Data bus

21.2 Block Diagram

Figure 21-1 below shows the SDIO module design for the CC35xx.

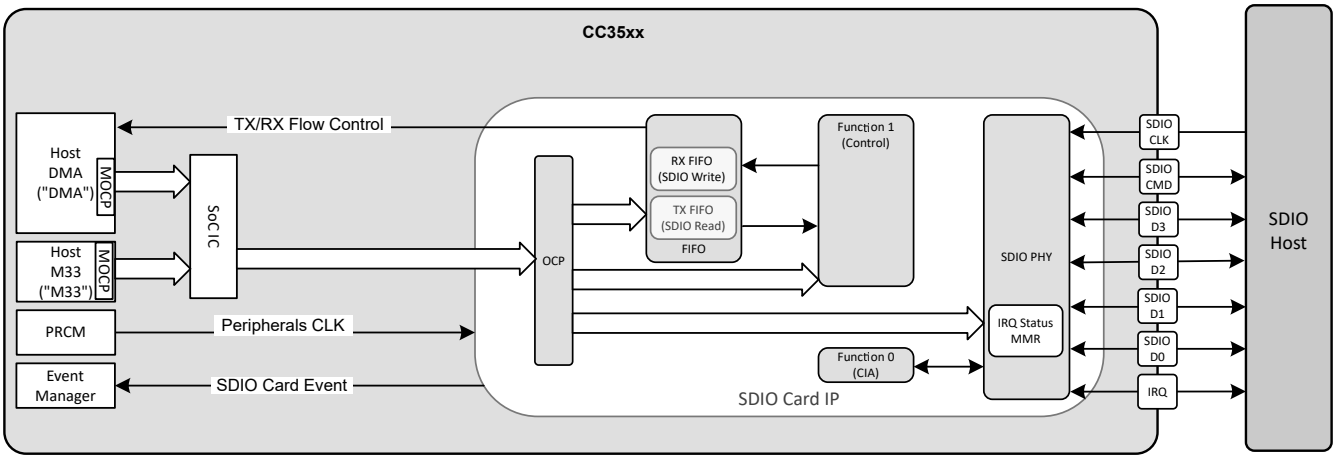

Figure 21-1. SDIO Module Block Diagram

As shown above, the physical SDIO (PHY SDIO) module, including SDIO function #0, are located separately from function #1 which is used for the data transfer buffers. An OCP interface will enable access to the different functions.

PHY SDIO is mainly responsible for SDIO protocol handling:

- **Function #0:** Located entirely in the PHY and is used for common configuration.
- **Function #1:** Dedicated for data transfer. Like every SDIO function, it is assigned a 128 Kbytes register address space for configuration and operation. The function #1 address space is partitioned between the PHY SDIO (control) and the DATA SDIO module (Data path).
- **Initializations**
- **SDIO command handling:** the PHY receives SDIO commands from the SDIO Host, parses them transmits the relevant information of each command to the corresponding SDIO function.
- **SDIO command response generation:** the PHY generates SDIO command responses and sends them to the SDIO Host.

- **Data transmission:** SDIO PHY transfers data from the SDIO host to the proper function (function #0 or #1) and vice versa.
- **CRC handling:** In SDIO host write direction, SDIO PHY checks each CRC that was sent by the SDIO host (at the end of each data block / data transaction). In SDIO host read direction, the PHY calculates the CRC of each block / data transaction and sends it to the SDIO host.
- **M33/DMA packets division to blocks:** In SDIO host read direction, SDIO PHY receives data from the TX FIFO (Host read) and divides it to SDIO blocks.
- **SDIO "busy" indication:** In SDIO host write direction, SDIO PHY may generate a "busy" indication according to a request from the RX FIFO module.

21.3 Functional Description

The CC35xx SDIO performs the functions of parallel-to-serial and serial-to-parallel conversions. Internal FIFO memories store the transmit and receive paths, allowing independent storage of up to two blocks in receive mode and a block in transmit mode (in case of the max block length – 128Bytes). The SDIO also supports two Host DMA interface, one for Tx and the other for Rx. SDIO module also includes a CRC engine that can be used for data checking during SDIO transmission.

21.3.1 SDIO Interface Description

- **SDIO_CLK** This pin provides the clock to the SDIO card from the external SDIO host.
- **SDIO_CMD** This pin is used for two-way communication between SDIO peripheral and the host. The host transmits commands to the peripheral and the SDIO peripheral drives responses to the commands on this pin.
- **SDIO_DAT[3:0]** SDIO data lines establish the crucial pathway for information exchange between host systems and peripheral devices.
- **SDIO_OBI** Depending on the configuration of the host in the initialization, host interrupt is presented on the data bus (IBI – in band interrupt) or on dedicated pin (OBI – out band interrupt).

21.3.2 Protocol and Data Format

The bus protocol between the host controller and SDIO peripheral is message-based. Each message is represented by one of the following parts:

Command: A command starts an operation. The command is transferred serially from the host to the peripheral on the sdio_cmd line.

Response: A response is an answer to a command. The response is sent from the peripheral to the host. It is transferred serially on the sdio_cmd line.

Data: Data are transferred from the host to the peripheral or from the peripheral to the host using the DATA lines.

Busy: The sdio_data[0] signal is maintained low by the peripheral as far as it is programming the data received.

CRC status: CRC result is sent by the peripheral through the sdio_data[0] line when the host is executing a write transfer. In the case of transmission error occurring on any of the active data lines, the peripheral sends a negative CRC status on sdio_data[0]. In the case of successful transmission, the card sends a positive CRC status on sdio_data[0] and starts the data programming procedure.

21.3.3 I/O Read/Write Command

Two additional data transfer instructions have been added to support I/O. IO_WR_DIRECT and IO_RW_EXTENDED, which allows fast access with byte or block address.

21.3.3.1 IO_WR_DIRECT Command (CMD52)

CMD52 is the simplest means to access a single register within the total 128K of register space in any I/O function, including the common I/O area (CIA).

When the external host reads from the SDIO IP registers, the addressing is in byte mode. Therefore the addresses for each register are different than the ones outlined in Section 21.4 and Section 21.5, which are addresses read from the CC35xx M33 core.

Table 21-1. SDIO_CORE Registers - External Host Read

Register Name (see Section 21.4)	Byte Address	Field Name	Bit Width	Type	Reset Value
CCCR00	0x0	CCCR	[3:0]	RO	0x3
		SDIO	[7:4]	RO	0x4
	0x1	SD	[3:0]	RO	0x3
		RESERVED	[7:4]	RO	0x0
	0x2	RESERVED	[0]	RO	0x0
		FN1EN	[1]	RW	0x0
		RESERVED	[7:2]	RO	0x0
	0x3	RESERVED	[0]	RO	0x0
		FN1RDY	[1]	RW	0x0
		RESERVED	[7:3]	RO	0x0
CCCR04	0x4	CINTEN	[0]	RW	0x0
		FN1INTEN	[1]	RW	0x0
		RESERVED	[7:2]	RO	0x0
	0x5	RESERVED	[0]	RO	0x0
		FN1INTPEND	[1]	RO	0x0
		RESERVED	[7:2]	RO	0x0
	0x6	SDIOABORT	[2:0]	WO	0x0
		SDIORSTREQ	[3]	WO	0x0
		RESERVED	[7:4]	RO	0x0
	0x7	BW	[1:0]	RW	0x0
		RESERVED	[6:2]	RO	0x0
		CDDIS	[7]	RW	0x0
CCCR08	0x8	SDC	[0]	RO	0x0
		SMB	[1]	RO	0x1
		SRW	[2]	RO	0x0
		SBS	[3]	RO	0x0
		S4MI	[4]	RO	0x1
		E4MI	[5]	RW	0x0
		LSC	[6]	RO	0x0
		BLS4	[7]	RO	0x0
	0x9	CISPTR0	[7:0]	RO	0x0
	0xA	CISPTR1(LSB)	[7:0]	RO	0x10
	0xB	CISPTR1(MSB)	[7:0]	RO	0x0
CCCR10	0x10	FN0BLKSIZE(LSB)	[7:0]	RW	0x0
	0x11	FN0BLKSIZE(MSB)	[3:0]	RW	0x0
		RESERVED	[7:4]	RO	0x0
	0x13	SHS	[0]	RO	0x1
		EHS	[1]	RW	0x0
		RESERVED	[7:2]	RO	0x0

Table 21-1. SDIO_CORE Registers - External Host Read (continued)

Register Name (see Section 21.4)	Byte Address	Field Name	Bit Width	Type	Reset Value
CCCR14	0x16	SAI	[0]	RO	0x1
		EAI	[1]	RW	0x0
		RESERVED	[7:2]	RO	0x0
CCCR40	0x42	FN1ELPSTA	[0]	RW	0x1
		RESERVED	[7:1]	RO	0x0
CCCR44	0x44	FN1OBIEN	[0]	RW	0x1
		FN1OBIINV	[1]	RW	0x0
		RESERVED	[7:2]	RO	0x0
	0x45	FN1GPIMSK	[6:0]	RW	0x3F
		FN1STA	[7]	RO	0x0
	0x46	FN1GPISTA	[6:0]	RO	0x0
		RESERVED	[7]	RO	0x0
	0x47	FN1GPICLR	[5:0]	WO	0x0
		RESERVED	[7:6]	RO	0x0
CCCR48	0x48	FN1BUSY	[0]	RW	0x0
		FN1BUSYOV	[1]	RW	0x0
		RESERVED	[7:2]	RO	0x0
CCCR68	0x6A	CMDERR	[5:0]	RO	0x0
		RESERVED	[7:6]	RO	0x0
CCCR80	0x80	OCR	[7:0]	RW	0xC0
	0x81	OCR	[7:0]	RW	0xFF
	0x82	OCR	[7:0]	RW	0xFF
CCCR84	0x84	SDCMDST	[4:0]	RO	0x1
		SDRESPST	[7:5]	RO	0x1
	0x85	SDDAT3ST	[3:0]	RO	0x1
		RESERVED	[7:4]	RO	0x0
	0x86	SDDAT0ST	[4:0]	RO	0x1
		SDDAT1ST(LSB)	[7:5]	RO	0x3
	0x87	SDDAT1ST(MSB)	[1:0]	RO	0x0
		SDDAT2ST	[5:2]	RO	0x2
		RESERVED	[7:6]	RO	0x0
CCCR88	0x88	WSPI_STATE	[3:0]	RO	0x0
		WSPI_ERROR	[4]	RO	0x0
		RESERVED	[7:5]	RO	0x0
	0x8A	RCA(LSB)	[7:0]	RO	0x0
	0x8B	RCA(MSB)	[7:0]	RO	0x0
CCCRA0	0xA2	OCPSTA0	[3:0]	RO	0x0
		OCPSTA1	[7:4]	RO	0x0
CCCRA4	0xA4	RAWTMRVAL	[4:0]	RW	0x1F
		RESERVED	[7:5]	RO	0x0
	0xA5	USECTMRVAL	[5:0]	RW	0x27
		RESERVED	[7:6]	RO	0x0

Table 21-1. SDIO_CORE Registers - External Host Read (continued)

Register Name (see Section 21.4)	Byte Address	Field Name	Bit Width	Type	Reset Value
CCCRC0	0xC2	WUCMD53	[0]	RW	0x1
		WUHOSTRD	[1]	RW	0x1
		WUHOSTWR	[2]	RW	0x1
		WUADDR	[3]	RW	0x1
		WUELP	[4]	RW	0x0
		WUAUT	[5]	RW	0x1
		RESERVED	[7:6]	RW	0x0
CCCRC4	0xC4	FN1GPISTA	[6:0]	RO	0x0
		RESERVED	[7]	RO	0x0
FBR1R100	0x100	SDIO	[3:0]	RO	0x2
		RESERVED	[5:4]	RO	0x0
		CSA	[6]	RO	0x0
		RESERVED	[7]	RO	0x0
FBR1R108	0x109	CISPTR0	[7:0]	RO	0x0
	0x10A	CISPTR1(LSB)	[7:0]	RO	0x20
	0x10B	CISPTR1(MSB)	[7:0]	RO	0x0
FBR1R110	0x110	FNBLKSIZE(LSB)	[7:0]	RW	0x0
	0x111	FNBLKSIZE(MSB)	[3:0]	RW	0x0
		RESERVED	[7:4]	RO	0x0
CISP1ADDR	0x1FFE0	PCH1ADDR(LSB)	[7:0]	RW	0x0
	0x1FFE1	PCH1ADDR(MSB)	[7:0]	RW	0x0
	0x1FFE2	PCH1DAT	[7:0]	RW	0x0
CISP2ADDR	0x1FFE4	PCH2ADDR(LSB)	[7:0]	RW	0x0
	0x1FFE5	PCH2ADDR(MSB)	[7:0]	RW	0x0
	0x1FFE6	PCH2DAT	[7:0]	RW	0x0
CISP3ADDR	0x1FFE8	PCH3ADDR(LSB)	[7:0]	RW	0x0
	0x1FFE9	PCH3ADDR(MSB)	[7:0]	RW	0x0
	0x1FFEA	PCH3DAT	[7:0]	RW	0x0
CISP4ADDR	0x1FFEC	PCH4ADDR(LSB)	[7:0]	RW	0x0
	0x1FFED	PCH4ADDR(MSB)	[7:0]	RW	0x0
	0x1FFEE	PCH4DAT	[7:0]	RW	0x0
CISP5ADDR	0x1FFF0	PCH5ADDR(LSB)	[7:0]	RW	0x0
	0x1FFF1	PCH5ADDR(MSB)	[7:0]	RW	0x0
	0x1FFF2	PCH5DAT	[7:0]	RW	0x0

Table 21-2. SDIO_CARD_FN1 Registers - External Host Read

Register Name (see Section 21.5)	Byte Address	Field Name	Bit Width	Type	Reset Value
FLUSHCMD	0x0	RXBUF	[0]	WO	0x0
		TXBUF	[1]	WO	0x0
		RESERVED	[7:2]	RO	0x0
RXTHR	0x4	RESERVED	[1:0]	RO	0x0
		VAL	[7:2]	RW	0x1
TXIRQTHR	0xC	VAL	[7:0]	RW	0x80

Table 21-2. SDIO_CARD_FN1 Registers - External Host Read (continued)

Register Name (see Section 21.5)	Byte Address	Field Name	Bit Width	Type	Reset Value
DMABLKTHR	0x10	RXDMABLK	[2:0]	RW	0x2
		RESERVED	[7:3]	RO	0x0
	0x12	TXDMABLK	[2:0]	RW	0x2
		RESERVED	[7:3]	RO	0x0
IRQSTA	0x14	RXALMSFULL	[0]	RO	0x0
		FN1EN	[1]	RO	0x0
		RXBUFOVR	[2]	RO	0x0
		RXBUFUNR	[3]	RO	0x0
		TXBUFOVR	[4]	RO	0x0
		TXBUFUNR	[5]	RO	0x0
		HCIACK	[6]	RO	0x0
		HCINACK	[7]	RO	0x0
	0x15	HCIWRRET	[0]	RO	0x0
		PHYIFERR	[1]	RO	0x0
		CARDRST	[2]	RO	0x0
		PHYINT	[3]	RO	0x0
		CRCERR	[4]	RO	0x0
		HOST2CORE	[5]	RO	0x0
		RESERVED	[7:6]	RO	0x0
IRQMASK	0x18	RXALMSFULL	[0]	RW	0x1
		FN1EN	[1]	RW	0x1
		RXBUFOVR	[2]	RW	0x1
		RXBUFUNR	[3]	RW	0x1
		TXBUFOVR	[4]	RW	0x1
		TXBUFUNR	[5]	RW	0x1
		HCIACK	[6]	RW	0x1
		HCINACK	[7]	RW	0x1
	0x19	HCIWRRET	[0]	RW	0x1
		PHYIFERR	[1]	RW	0x1
		CARDRST	[2]	RW	0x1
		PHYMASK	[3]	RW	0x1
		CRCERR	[4]	RW	0x1
		HOST2CORE	[5]	RW	0x1
		RESERVED	[7:6]	RO	0x0
CTRL	0x1C	SDIOEN	[0]	RW	0x1
		BACE	[1]	RW	0x1
		TXFLEN	[2]	RW	0x1
		HIRQSYNC	[3]	RW	0x0
		RESERVED	[7:4]	RO	0x0
RXPACS	0x20	VAL (LSB)	[7:0]	RO	0x0
	0x21	VAL (MSB)	[1:0]	RO	0x0
		RESERVED	[7:2]	RO	0x0

Table 21-2. SDIO_CARD_FN1 Registers - External Host Read (continued)

Register Name (see Section 21.5)	Byte Address	Field Name	Bit Width	Type	Reset Value
RXBBUF	0x24	VAL (LSB)	[7:0]	RO	0x0
	0x25	VAL (MSB)	[2:0]	RO	0x0
		RESERVED	[7:3]	RO	0x0
RXBLFT	0x28	VAL (LSB)	[7:0]	RO	0x0
	0x29	VAL (MSB)	[2:0]	RO	0x0
		RESERVED	[6:3]	RO	0x0
		BLIL	[7]	RO	0x0
RETCTL	0x2C	VAL	[0]	RW	0x0
		RESERVED	[7:1]	RO	0x0
C2HMSG	0x30	C2HSTS (LSB)	[7:0]	RW	0x0
	0x31	C2HSTS (MSB)	[7:0]	RW	0x0
	0x32	C2HIRQ	[0]	WO	0x0
		RESERVED	[7:1]	RO	0x0
H2CMSG	0x34	H2CSTS (LSB)	[7:0]	RO	0x0
	0x35	H2CSTS (MSB)	[6:0]	RO	0x0
		RESERVED	[7]	RO	0x0
CLKEN	0x38	VAL	[0]	RW	0x0
		RESERVED	[7:1]	RO	0x0
IRQCLR	0x40	RXALMSFULL	[0]	WO	0x0
		FN1EN	[1]	WO	0x0
		RXBUFOVR	[2]	WO	0x0
		RXBUFUNR	[3]	WO	0x0
		TXBUFOVR	[4]	WO	0x0
		TXBUFUNR	[5]	WO	0x0
		HCIACK	[6]	WO	0x0
		HCINACK	[7]	WO	0x0
	0x41	HCIWRRET	[0]	WO	0x0
		PHYIFERR	[1]	WO	0x0
		CARDRST	[2]	WO	0x0
		PHYCLEAR	[3]	WO	0x0
		CRCERR	[4]	WO	0x0
		HOST2CORE	[5]	WO	0x0
		RESERVED	[7:6]	RO	0x0
RSTREQ	0x44	EN	[0]	RW	0x0
		RESERVED	[7:1]	RO	0x0

21.3.3.2 IO_WR_EXTENDED Command (CMD53)

The host will use CMD53 to send/receive data to the peripheral.

The host must configure CMD53 with the following fields:

- CMD53 can be sent to function 1 only
- Host can transmit data in two different modes:
  - Block mode: In this mode the host must send complete block that defined in the initialization with CMD52 SDIO_CORE:FBR1R110[11:0]FNBLKSIZE. The number of bytes must be divided by 4.

– Byte mode: Host can use this mode to read or write up to 128 bytes. Above that the host must use Block mode.

  For example: If the block length is 128 bytes and the host wants to transmit 136 bytes the transmission can be done in two ways:
  1. Send a single CMD53 with number of blocks = 2, and pad the second block with junk data.
  2. Send CMD53 with number of blocks = 1, and after the transmission is end send another CMD53 in byte mode.

– When the host sends CMD53 the address must be 0x0000 (FIFO address).

21.3.4 Reset

By sending CMD52 to register SDIO_CORE:CCCR04[19]SDIORSTREQ, the host can reset the SDIO peripheral. Writing to that register will generate an interrupt to M33, and then M33 SW will reset SDIO peripheral by writing to register SDIO_CARD_FN1:RSTREQ[0]EN.

21.3.5 FIFO Operation

SDIO peripheral has two entry FIFOs. One FIFO for transmit and one FIFO for receive. Both FIFOs are accessed through the SDIO Data Register, SDIO_CARD_FN1:DATAFIFO.

21.3.5.1 Rx FIFO (For Host Write)

The RX FIFO in the SDIO peripheral serves as a temporary buffer for incoming data received from the SDIO host via the SDIO data bus protocol. It has a total capacity of 256 bytes and is designed to efficiently handle data flow between the SDIO interface and system memory. The FIFO features a configurable threshold SDIO_CARD_FN1:RXTHR[7:2]VAL, allowing software to define the number of bytes that should accumulate before triggering an interrupt to notify the M33. This mechanism helps optimize data processing by reducing the frequency of interrupts while ensuring timely data handling. To facilitate high-speed data transfer, the FIFO supports DMA, enabling efficient movement of data to system memory without excessive M33 intervention. The DMA block size, which determines how much data is transferred in each operation, must be configured in both the DMA controller and the corresponding SDIO register SDIO_CARD_FN1:DMABLKTHR[2:0]RXDMABLK to ensure proper synchronization between the FIFO and memory. Additionally, a dedicated register SDIO_CARD_FN1:FLUSHCMD[0]RXBUF allows software to flush the FIFO when necessary, ensuring that unwanted or stale data does not interfere with new transmissions. A status register SDIO_CARD_FN1:RXBBUF[10:0]VAL provides real-time visibility into the number of bytes currently stored in the FIFO, allowing software to monitor and manage data flow effectively. These features together ensure robust and efficient handling of received SDIO data, minimizing latency and maximizing system performance.

21.3.5.2 Tx FIFO (For Host Read)

The TX FIFO in the SDIO hardware peripheral is responsible for temporarily storing outgoing data before transmission to the SDIO host via the SDIO data bus protocol. It has a total capacity of 128 bytes and is designed to facilitate efficient data movement between system memory and the SDIO interface. The FIFO primarily relies on DMA for data transfer, with DMA requests being issued when there is sufficient space in the FIFO to accommodate a complete SDIO block. This mechanism ensures that data is efficiently loaded into the FIFO without unnecessary M33 intervention, reducing processing overhead and improving overall performance.

The TX FIFO also features a configurable threshold register SDIO_CARD_FN1:TXIRQTHR[7:0]VAL, which allows software to define the number of bytes that should accumulate before triggering an interrupt to the SDIO host. This interrupt mechanism enables the host to manage data flow effectively and ensures that transmission proceeds without unnecessary delays. Additionally, the FIFO can be flushed by writing to a dedicated register SDIO_CARD_FN1:FLUSHCMD[1]TXBUF, allowing software to clear its contents when needed, such as during error handling or reinitialization scenarios. These features collectively ensure smooth and efficient data transmission, optimizing SDIO communication while maintaining flexibility in system design.

21.3.6 Interrupt Request

There are 2 kinds of interrupts that are derived from SDIO peripheral, an IRQ to M33 and an IRQ to the external host.

21.3.6.1 External Host IRQ

IRQ trigger register SDIO_CARD_FN1:TXIRQTHR[7:0]VAL is a register containing a value in bytes, which states how many bytes must be present at the SDIO Tx FIFO in order to trigger the SDIO host IRQ. This ensures that the FIFO has enough bytes to withstand any delays that might occur. The trigger mechanism is armed before the SW attempts to write a packet, dis-armed when the threshold configured on the IRQ trigger register is crossed, and can be re-armed again when the SW writes to the trigger register again.

Logically, this trigger can be re-armed after a successful / unsuccessful transaction, notified to the device by the host read acknowledgment.

The diagram below depicts the process HW and SW needs to follow for Host read scenario:

1. The SW wants to transmit a packet N to the host. The packet length is known so first it needs to configure the IRQ trigger threshold. SW uses the following reasoning to decide what the trigger should be:
   a. If packet length > SDIO block (max 128-byte) trigger is set to 128 Byte (entire block)
   b. If packet length < SDIO block, SW sets packet length in bytes as the trigger value.
2. SW now preparing for DMA transfer, starts the DMA and bytes from the first block are copied from memory to SDIO TX FIFO.
3. Once the trigger threshold been reached, SDIO sets the Host IRQ line.
4. Host writes to function #1 register in order to clear the IRQ SDIO_CARD_FN1.ICLR, such that the IRQ is lowered. Please note, that until the next time IRQ trigger is armed, the threshold value is being ignored by SDIO FIFO and crossing it shall result in no action.
5. The host issues command 53 to read the data in block/bytes mode.
6. Blocks are being transferred to host on the Memory → DMA → SDIO TX FIFO → SDIO PHY → Data lines path.
7. Optional: SW can start writing the next packet even before the previous one has been read. Host IRQ will not be generated till #10 below.
8. Whenever the host finished reading the data, since the CC35xx is a device with mandatory read ack, it writes a function #1 register in order to indicate Ack/Nack, which trigger IRQ to SW. (If SDIO TX buffer is already above threshold due to #7 above, IRQ will be generted)
9. At this point in time, the IRQ trigger can be re-armed (If another packet is pending).

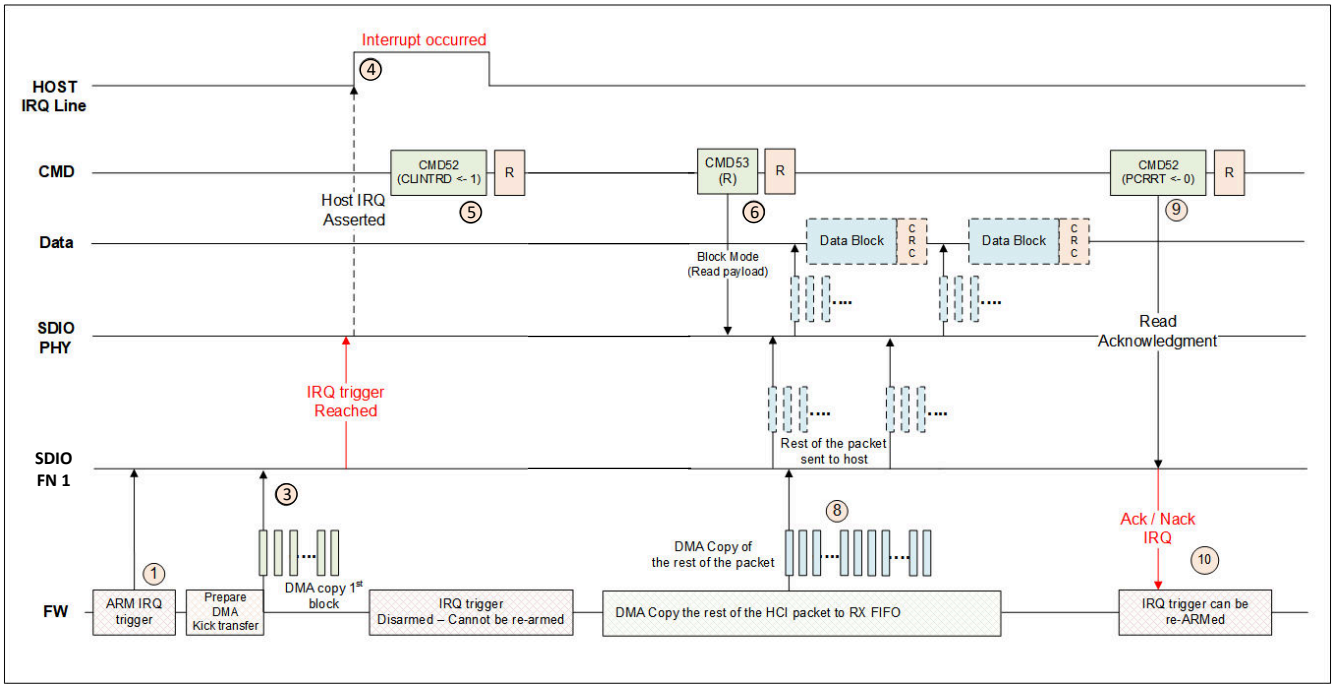

Figure 21-2. External Host SDIO IRQ

21.3.6.2 M33 IRQ

Several internal module events can generate an interrupt.

Each interrupt has a status bit, an interrupt enables bit and a clear status register:

- Each status is masked by default. To enable the interrupt SW need to unmask the interrupt by write zero in SDIO_CARD_FN1:IRQMASK register
- The status of each type of interrupt is automatically updated in the SDIO_CARD_FN1:IRQSTA register it indicates which service is required.
- After served SW will clear the interrupt by write 1 to SDIO_CARD_FN1:IRQCLR register.

21.3.7 Transaction Details

Transaction always starts with command 53 that sent from the external host.

21.3.7.1 Host write to SDIO IP (Rx FIFO)

In order to initiate transfer, host issues CMD53 with the following parameters:

Table 21-3. CMD53 Parameters

CMD53	Function = #1	Write flag = 0x1	Mode = Block Mode	Block Count = [L/B]	Address = 0x00 (TX FIFO)

1. SDIO PHY parse the command, if it's valid and addressed to fucntion#1, it sends response to the host and issues an OCP write commands towards SDIO FIFO.
2. After seeing the command response, the host starts sending data blocks to SDIO PHY.
3. The SDIO PHY transmits this data to the SDIO FIFO: for each 8 bits of received data, it issues write command and at the same time transmits the address and the data byte (using the OCP interface). The address is the SDIO RX FIFO address (0x0) and the data is the host's data. SDIO FIFO responds to every command with 'command accept S'. At this point in time, host data bytes are accumulating in the SDIO RX FIFO.
4. RX FIFO has a configurable threshold associated with it to generate "Not Empty" IRQ to SW. This threshold is configurable.

5. Once triggered, SW first mask "Not empty" IRQ. According to the received length as well as a const max packet size value, SW:
   a. Allocates an empty memory space
   b. Prepare a DMA transaction to copy new packet from RX FIFO to memory.
   c. Kick the DMA transfer.
6. At this point in time, the DMA copies the entire packet to memory. SW continues it's other tasks.
7. Upon copy completion, DMA would generate "DMA DONE" IRQ to SW. SW then checks the RX FIFO contents. If the FIFO is not empty another DMA copy is prepared. If not, "Not Empty" IRQ is unmasked.
8. SW forwards the packet to next stage in the pipeline.

Note

- Packet of length L is being divided into as many SDIO blocks of length B as possible ([L/B], B < L). If there is a remaining data, the remainder of the packet is sent via a following CMD53 in byte mode. The SDIO FIFO is completely agnostic to this fact, since the remainder (L mod B) is being taken care of by the DMA as part of the total copy transfer.
- At the end of each data block (in block-basis operations) or data transaction (in byte-basis operations), the host sends CRC. The SDIO PHY checks the CRC and sends response to the host, including CRC_OK field. The CRC_OK status is given to the SDIO FIFO as well, using a dedicated status line in the PHY interface. If the CRC is not okay SW needs to handle CRC error.

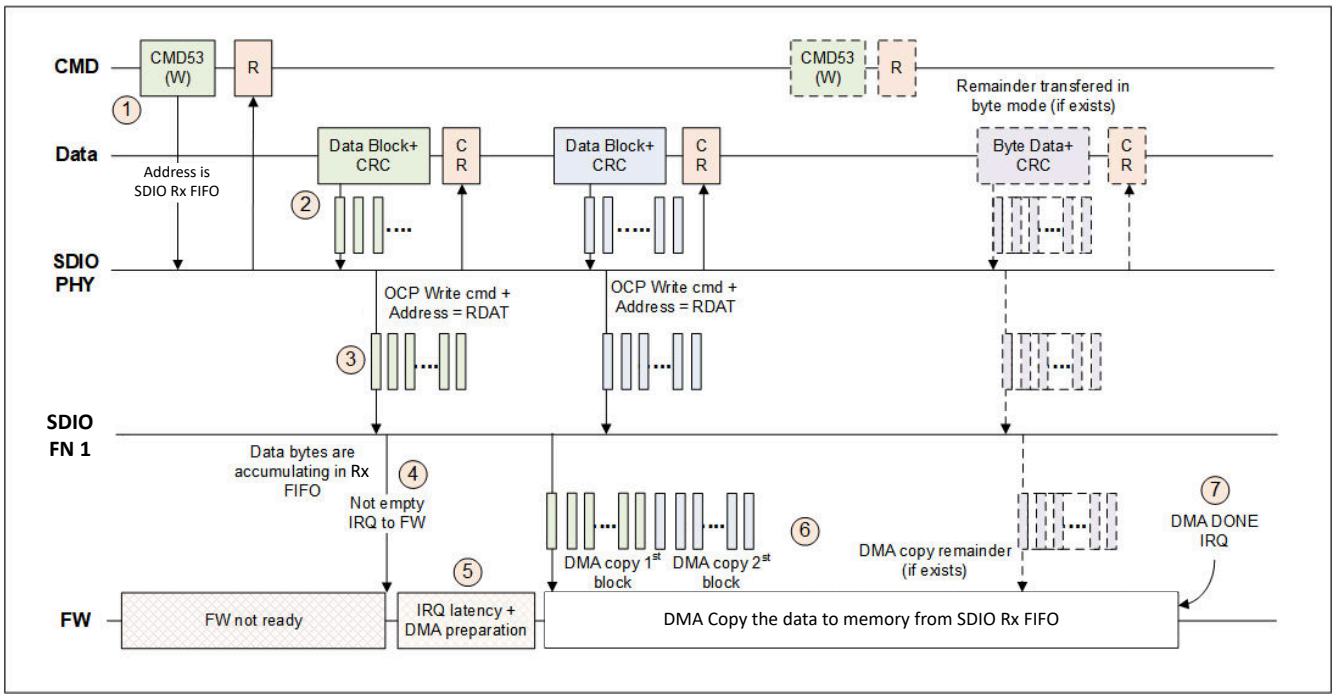

Figure 21-3. Host write SDIO

21.3.7.1.1 Host write to SDIO IP (Rx FIFO) – Long SW latency case

As mentioned in the previous chapter, SW response might take long time (can be ~40 uSec), depending on current running activities, contexts, etc. Furthermore, sometimes servicing the IRQ in itself might take time waiting for buffers to get free, etc. In order to support robust design, the flow below depicts high SW latency host write flow. In a nutshell, the lines "BUSY" signaling is used as well as "buffering" any incoming data in buffer.

1. Host initiates a transfer and sends data bytes to SDIO FIFO, until "Not empty" threshold is crossed, as previously described. Data bytes are sent to SDIO RX FIFO.

2. Since SW has longer response time, data bytes have accumulated in RX FIFO such that it is now full. Once full, assert the line BUSY (Data [0] is held low). This prevents the host from sending any more data, thus protecting the already received blocks from overruns. Also, this gives SW enough time to respond and service the RX FIFO not empty IRQ.
3. Once SW is available, it prepares the DMA descriptor and initiates a DMA transfer. Bytes are being emptied from SDIO buffer. Once SDIO RX FIFO is not full and has enough space for additional packet BUSY line is de-asserted.

21.3.7.1.2 Host write to SDIO IP (Rx FIFO) – CRC Error Case

This chapter describes how SDIO recovers from CRC errors in host write flow. In general, when a CRC error occurs in an SDIO transmission, the Host recognize it through the transmission result sent by the card after each block \ byte basis transfers. When such event occurs, the entire packet (Not only the specific block) is discarded and re-transmitted by the corresponding side:

- At the end of each data block (in block-basis operations) or data transaction (in byte-basis operations), the host also sends CRC. SDIO PHY then calculate the CRC result and compare it to CRC field sent by the host. This comparison result is then sent to the host in a CRC response packet, including CRC_OK field. If the CRC is NOT OKAY and the configuration allows, the SDIO FIFO sets the busy interface line.
- The motivation behind that, is to let the SW enough time to prepare for packet re-transmission and to terminate the current packet reception.

The flow is described by the following steps:

1. Host initiate a data transfer using CMD53.
2. Once the SDIO PHY finds out there is a CRC error, it sends to the host response with CRC error indication. It also updated the CRC_OK status of the SDIO PHY interface and issues at interrupt to the SW.
3. SDIO receives the CRC error indication and if its configuration allows, it sets the busy line.
4. SW receives the SDIO PHY's interrupt and prepares itself to the retransmission.
5. When the SW is ready (DMA has been aborted, packet memory was freed, HOST RX FIFO were flushed), it gives the HW command to clear the busy indication.

   At this point in time, the host should start re-transmitting the entire packet again:

   According to specification, when the host receives the PHY response that includes CRC error indication, it sends CMD52 to the PHY, in order to indicate packet, write retry (PCWRT→ 1). Note that according to Spec some hosts can send in addition CMD52 (I/O aborts) between data blocks. This doesn't change the flow, since as far as SW is concerned, writing to PCWRT serves the same purpose.
6. The command’s parameters are:
   a. function number 1 (SDIO function #1), write flag, write packet control register address (0x11), data = 1. (Step 6)

Table 21-4. CMD52

CMD52	Function = #1	Write Flag = 0x1	Address = write packet control register address (0x11)	DATA = 0x1

   b. SDIO PHY parses the command and sends SDIO command response to the host. Note that SW already knows a retransmission needs to take place.
7. The packet re-transmission is performed like any other typical host write (CMD53) such that SDIO PHY nor SDIO HW are aware of this re-transmission.

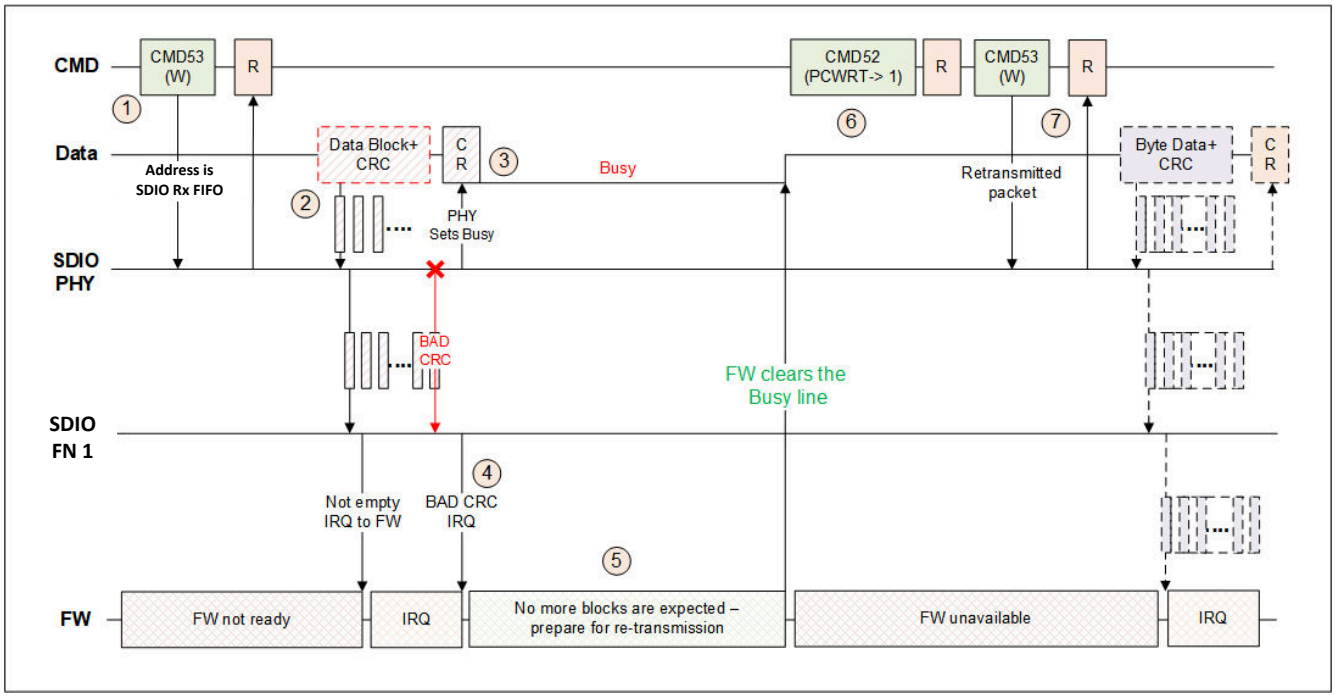

Figure 21-4. Host Write to SDIO with CRC Error

21.3.7.2 Host reads from SDIO (TX buffer)

In general, the M33 transmits data to the host packet-by-packet, i.e. packet N+1 is handled (i.e. copied from internal memory) only after packet N is ACKED. This also implies that CC35xx SDIO interface is a card with necessary read acknowledgement.

The diagram below describes the transport layer Host read:

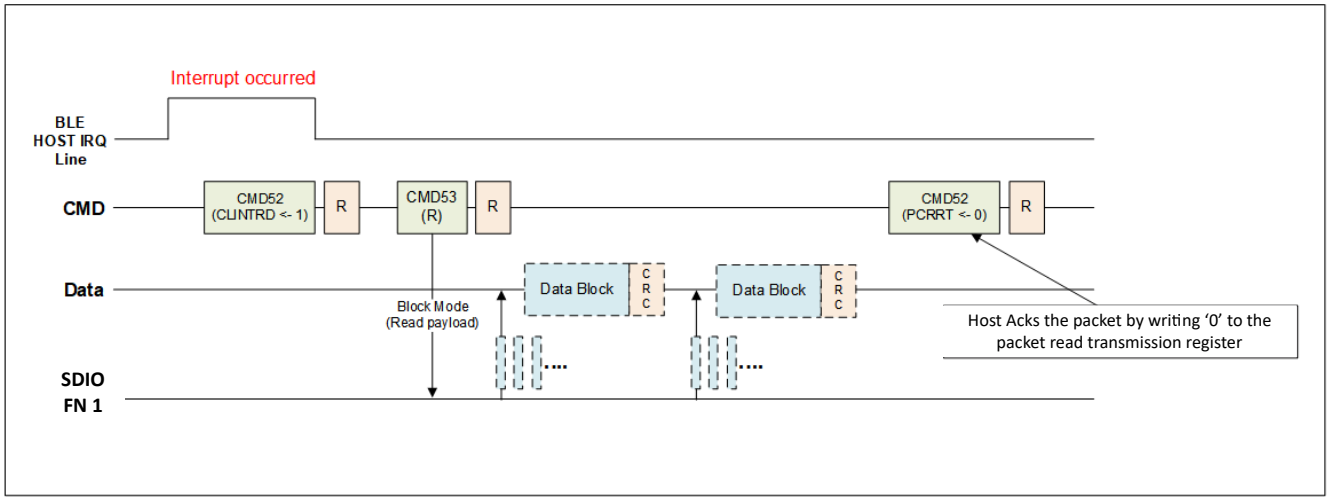

Figure 21-5. Host read from SDIO

Transfer is initiated by the card, asserting an IRQ line* to the host. Once the host sees this IRQ, it writes to a function #1 register, CLINTRD to clear the pending IRQ.

At this point in time host now issues command 53 for read packet payload:

Table 21-5. CMD53 params

CMD53	Function = #1	Read Flag (0x0)	Mode = Block Mode	Block Count = [L/B]	Address = 0x0 (RX FIFO)

After reading the entire packet, SDIO expects a read acknowledgment. The host does this by writing "0" to Packet read retransmission register. At this point in time, if the device has another packet to transmit to the host, it sets the IRQ line again, and the process repeats itself.

21.4 SDIO_CORE Registers

Table 21-6 lists the memory-mapped registers for the SDIO_CORE registers. All register offset addresses not listed in Table 21-6 should be considered as reserved locations and the register contents should not be modified.

Table 21-6. SDIO_CORE Registers

Offset	Acronym	Register Name	Section
0h	CCCR00	Version and FN1 ENABLE	Section 21.4.1
4h	CCCR04	Interrupt Control Register	Section 21.4.2
8h	CCCR08	Card Capabilities And CIS Pointer	Section 21.4.3
10h	CCCR10	Function 0 Control	Section 21.4.4
14h	CCCR14	Interrupt Control	Section 21.4.5
44h	CCCR44	Function 1 Control	Section 21.4.6
48h	CCCR48	Function 1 Busy Control Register	Section 21.4.7
68h	CCCR68	Command Error Status Register	Section 21.4.8
80h	CCCR80	Operation Conditions Register	Section 21.4.9
84h	CCCR84	Function Configuration Control	Section 21.4.10
88h	CCCR88	RCA Configuration Control Register	Section 21.4.11
A0h	CCCRA0	OCP Status Register	Section 21.4.12
A4h	CCCRA4	Timer Configuration Register	Section 21.4.13
100h	FBR1R100	Function 1 Basic Register	Section 21.4.14
108h	FBR1R108	Function 1 Cis Pointer Register	Section 21.4.15
110h	FBR1R110	Function 1 Block Size Register	Section 21.4.16
0001FFE0h	CISP1ADDR	Fn1 CIS Address	Section 21.4.17
0001FFE4h	CISP2ADDR	Fn1 CIS Address	Section 21.4.18
0001FFE8h	CISP3ADDR	Card Information Patch	Section 21.4.19
0001FFECh	CISP4ADDR	Camera Image Sensor	Section 21.4.20
0001FFF0h	CISP5ADDR	Function CIS Address	Section 21.4.21

Complex bit access types are encoded to fit into small table cells. Table 21-7 shows the codes that are used for access types in this section.

Table 21-7. SDIO_CORE Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

21.4.1 CCCR00 Register (Offset = 0h) [Reset = 00000343h]

CCCR00 is shown in Table 21-8.

Return to the Summary Table.

CCCR and SDIO Revision Register. Contains version information fields: CCCR (CCCR/FBR format version), SDIO (SDIO specification version), and SD (Physical Layer specification version). This register identifies the specification versions supported by the card for proper host compatibility.

Table 21-8. CCCR00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26	RESERVED	R	0h	Reserved
25	FN1RDY	R/W	0h	Function 1 Ready
24-19	RESERVED	R	0h	Reserved
18	RESERVED	R	0h	Reserved
17	FN1EN	R/W	0h	Enable Function 1
16-12	RESERVED	R	0h	Reserved
11-8	SD	R	3h	SD Format Version number
7-4	SDIO	R	4h	SDIO Specification Revision number
3-0	CCCR	R	3h	4 CCCRx bits defines the version used by CCCR and the FBR format it supports

21.4.2 CCCR04 Register (Offset = 4h) [Reset = 00000000h]

CCCR04 is shown in Table 21-9.

Return to the Summary Table.

Interrupt Control Register. Contains interrupt enable and pending status fields: controller_int_en (IENM - controller interrupt enable), fn1_int_en (IEN1 - function 1 interrupt enable), fn1_int_pend (INT1 - function 1 interrupt pending), sdio_abort (ASx - abort select), and sdio_reset_req (RES - I/O card reset). Controls interrupt generation and allows aborting or resetting I/O functions.

Table 21-9. CCCR04 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CDDIS	R/W	0h	Connect/Disconnect (0/1) the pull-up resistor on SDIO data line 3
30-26	RESERVED	R	0h	Reserved
25-24	BW	R/W	0h	Defines SDIO data bus width
23-20	RESERVED	R	0h	Reserved
19	SDIORSTREQ	W	0h	reset sdio IP due to a SDIO Card Reset command
18-16	SDIOABORT	W	0h	Abort read or write transaction and free the SDIO bus.
15-11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	FN1INTPEND	R	0h	Interrupt pending for function 1
8-3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	FN1INTEN	R/W	0h	Interrupt Enable for function 1
0	CINTEN	R/W	0h	Interrupt Enable controller

21.4.3 CCCR08 Register (Offset = 8h) [Reset = 00100012h]

CCCR08 is shown in Table 21-10.

Return to the Summary Table.

Card Capability and CIS Pointer Register. Contains capability flags (SDC, SMB, SRW, SBS, S4MI, E4MI, LSC, 4BLS) that report card abilities for direct commands, multi-block transfer, read wait, suspend/resume, and interrupt support. Also includes the 24-bit common CIS pointer (FN0_CIS_PTR) indicating the location of the Card Information Structure.

Table 21-10. CCCR08 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CISPTR1	R	10h	Bits 23:8 of cards common CIS pointer
15-8	CISPTR0	R	0h	Bits 7:0 of cards common CIS pointer
7	BLS4	R	0h	4 bit support for low speed cards
6	LSC	R	0h	Card is a low speed card
5	E4MI	R/W	0h	Enable interrupt between blocks of data in SDIO 4 bit mode
4	S4MI	R	1h	Supports interrupt between blocks of data in SDIO 4 bit mode
3	SBS	R	0h	Card support Suspend/Resume
2	SRW	R	0h	Card support read wait
1	SMB	R	1h	Card support Multi-Block
0	SDC	R	0h	Card support direct commands during data transfer

21.4.4 CCCR10 Register (Offset = 10h) [Reset = 01000000h]

CCCR10 is shown in Table 21-11.

Return to the Summary Table.

Function 0 Block Size and Speed Control Register. Contains fn0_blk_size (block size for function 0 I/O operations, max 2048 bytes), shs (Support High-Speed flag), and ehs (Enable High-Speed flag). Controls block transfer size for function 0 and manages high-speed mode capabilities up to 50MHz.

Table 21-11. CCCR10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	EHS	R/W	0h	Enable High Speed
24	SHS	R	1h	Support High Speed
23-12	RESERVED	R	0h	Reserved
11-0	FN0BLKSIZE	R/W	0h	Function 0 block size

21.4.5 CCCR14 Register (Offset = 14h) [Reset = 00010000h]

CCCR14 is shown in Table 21-12.

Return to the Summary Table.

Asynchronous Interrupt Control Register. Contains SAI (Support Asynchronous Interrupt) and EAI (Enable Asynchronous Interrupt) fields. Controls the card's ability to generate interrupts in SD 4-bit mode without requiring SD clock, enabling asynchronous interrupt signaling.

Table 21-12. CCCR14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17	EAI	R/W	0h	Enable Asynchronous Interrupt: Enable bit of asynchronous interrupt. When Sai is set to 0, writing to this bit is ignored and always indicates 0. This bit is effective in in SD 4-bit mode.
16	SAI	R	1h	Support Asynchronous Interrupt: Support bit of Asynchronous Interrupt. If the card supports asynchronous interrupt in SD 4-bit mode, this bit is set to 1.
15-0	RESERVED	R	0h	Reserved

21.4.6 CCCR44 Register (Offset = 44h) [Reset = 00003F01h]

CCCR44 is shown in Table 21-13.

Return to the Summary Table.

Function 1 Interrupt Control and Status Register. Contains out-of-band interrupt control (fn1_obi_en, fn1_obi_inv), general purpose interrupt mask (fn1_gpi_msk), status (fn1_gpi_sts), clear (fn1_gpi_clr), and function interrupt status (fn1_sts). Manages various interrupt sources including ELP transitions, host writes, data block completion, and CRC errors.

Table 21-13. CCCR44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-24	FN1GPICLR	W	0h	General Purpose clear Interrupt sources. Write '1' to clear the desire source. bit 0 - ELP signal transition from '0' to '1' bit 1 - ELP signal transition from '1' to '0' bit 2 - Host write to IOE1 register (Function 0 address 0x2) bit 3 - Host write to function 0 CCCR area bit 4 - Function 1 data block completion bit 5 - Function 1 data block with CRC error
23	RESERVED	R	0h	Reserved
22-16	FN1GPISTA	R	0h	General Purpose Interrupt sources status. bit 0 - ELP signal transition from '0' to '1' bit 1 - ELP signal transition from '1' to '0' bit 2 - Host write to IOE1 register (Function 0 address 0x2) bit 3 - Host write to function 0 CCCR area bit 4 - Function 1 data block completion bit 5 - Function 1 data block with CRC error bit 6 - Autonomous mode: cmd 53 valid WR command to data FIFO
15	FN1STA	R	0h	Function 1 interrupt status.
14-8	FN1GPIMSK	R/W	7Fh	General Purpose Interrupt source mask. bit 0 - ELP signal transition from '0' to '1' bit 1 - ELP signal transition from '1' to '0' bit 2 - Host write to IOE1 register (Function 0 address 0x2) bit 3 - Host write to function 0 CCCR area bit 4 - Function 1 data block completion bit 5 - Function 1 data block with CRC error bit 6 - Autonomous mode: cmd 53 valid WR command to data FIFO
7-2	RESERVED	R	0h	Reserved
1	FN1OBIINV	R/W	0h	Invert Out Band Interrupt polarity
0	FN1OBIEN	R/W	1h	Enable Out Band Interrupt

21.4.7 CCCR48 Register (Offset = 48h) [Reset = 00000000h]

CCCR48 is shown in Table 21-14.

Return to the Summary Table.

Function 1 Busy Control Register. Contains fn1_busy (busy signal value) and fn1_busy_override (override enable) fields. Allows manual control and override of the function 1 busy signal to manage data transfer flow control.

Table 21-14. CCCR48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	FN1BUSYOV	R/W	0h	Override function 1 busy signal value. 0 - Do not override. 1 - Override.
0	FN1BUSY	R/W	0h	Set function 1 busy signal override value

21.4.8 CCCR68 Register (Offset = 68h) [Reset = 02000000h]

CCCR68 is shown in Table 21-15.

Return to the Summary Table.

Command Error Status Register. Contains cmd_error field with a 6-bit bitmap indicating various command errors: address error, function number error, general error, illegal command error, CRC error, and out of range error. Reports the status of the last command execution.

Table 21-15. CCCR68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26	RESERVED	R	0h	Reserved
25	RESERVED	R	0h	Reserved
24-22	RESERVED	R	0h	Reserved
21-16	CMDERR	R	0h	Bit map: 0 - Address error 1 - Function number error 2 - General error 3 - Illegal command error 4 - CRC error 5 - Out of range error
15-2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

21.4.9 CCCR80 Register (Offset = 80h) [Reset = 00FFFFC0h]

CCCR80 is shown in Table 21-16.

Return to the Summary Table.

Operation Conditions Register (OCR). Contains the 24-bit OCR field indicating the supported voltage ranges and operation conditions for the SDIO card. Specifies the minimum and maximum VDD values the card can operate with.

Table 21-16. CCCR80 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	OCR	R/W	00FFFFC0h	Bits 23:0 of Operation Conditions Register

21.4.10 CCCR84 Register (Offset = 84h) [Reset = 09610121h]

CCCR84 is shown in Table 21-17.

Return to the Summary Table.

SDIO State Status Register. Contains multiple state machine status fields: sdio_cmd_state (command decoder state), sdio_resp_state (response state), sdio_dat3_state (data line 3 state), sdio_dat0_state (data line 0 state), sdio_dat1_state (data line 1 state), and sdio_dat2_state (data line 2 state). Provides visibility into the current state of various SDIO protocol state machines for debugging.

Table 21-17. CCCR84 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-26	SDDAT2ST	R	2h	Data line 2 state machine
25-21	SDDAT1ST	R	Bh	Data line 1 state machine
20-16	SDDAT0ST	R	1h	Data line 0 state machine
15-12	RESERVED	R	0h	Reserved
11-8	SDDAT3ST	R	1h	Data line 3 state machine
7-5	SDRESPST	R	1h	Response state machine
4-0	SDCMDST	R	1h	SDIO command decoder state machine

21.4.11 CCCR88 Register (Offset = 88h) [Reset = 00000000h]

CCCR88 is shown in Table 21-18.

Return to the Summary Table.

RCA Status Register. Contains rca (Relative Card Address - 16 bits) The RCA uniquely identifies the card on the SD bus.

Table 21-18. CCCR88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RCA	R	0h	Relative Card Address
15-5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3-0	RESERVED	R	0h	Reserved

21.4.12 CCCRA0 Register (Offset = A0h) [Reset = 00000000h]

CCCRA0 is shown in Table 21-19.

Return to the Summary Table.

OCP Status Register. Contains ocp_status_3_0 (OCP write command status) and ocp_status_7_4 (OCP read command status) fields. Reports the status of OCP (Open Core Protocol) read and write commands, cleared on read.

Table 21-19. CCCRA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-20	OCPSTA1	R	0h	ocp status 7-4 OCP read command status. Clear on read
19-16	OCPSTA0	R	0h	ocp status 3-0 OCP write command status. Clear on read
15-0	RESERVED	R	0h	Reserved

21.4.13 CCCRA4 Register (Offset = A4h) [Reset = 0000271Fh]

CCCRA4 is shown in Table 21-20.

Return to the Summary Table.

Timer Configuration Register. Contains raw_timer_val (duration between CMD52 write and read in RAW mode) and usec_timer_val (microsecond timer count value running at sys_ocp_clk_aod_i clock). Configures timing parameters for raw command operations and general timing functions.

Table 21-20. CCCRA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20-16	RESERVED	R	0h	Reserved
15-14	RESERVED	R	0h	Reserved
13-8	USECTMRVAL	R/W	27h	Set usec timer count value. This timer is running at sys_ocp_clk_aod_i clock.
7-5	RESERVED	R	0h	Reserved
4-0	RAWTMRVAL	R/W	1Fh	Determine the duration between write and read request in CMD52 raw.

21.4.14 FBR1R100 Register (Offset = 100h) [Reset = 00000002h]

FBR1R100 is shown in Table 21-21.

Return to the Summary Table.

Function 1 Basic Register - Interface Code. Contains SDIO (standard function interface code) and CSA (Code Storage Area support) fields. Identifies the type of SDIO function (e.g., UART, Bluetooth, WLAN) and indicates if the function supports a Code Storage Area.

Table 21-21. FBR1R100 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	CSA	R	0h	Function 1 Supports CSA
5-4	RESERVED	R	0h	Reserved
3-0	SDIO	R	2h	SDIO standard function 1 interface code

21.4.15 FBR1R108 Register (Offset = 108h) [Reset = 00000000h]

FBR1R108 is shown in Table 21-22.

Return to the Summary Table.

Function 1 CIS Pointer Register. Contains FN_CIS_PTR_7_0 (bits 7:0) and FN_CIS_PTR_23_8 (bits 23:8) forming a 24-bit pointer to the start of the Card Information Structure (CIS) for function 1. The CIS contains detailed function capabilities and requirements.

Table 21-22. FBR1R108 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CISPTR1	R	20h	Bits 23:8 of address pointer to function 1 CIS
15-8	CISPTR0	R	00h	Bits 7:0 of address pointer to function 1 CIS
7-0	RESERVED	R	0h	Reserved

21.4.16 FBR1R110 Register (Offset = 110h) [Reset = 00000000h]

FBR1R110 is shown in Table 21-23.

Return to the Summary Table.

Function 1 Block Size Register. Contains fn_blk_size field (12 bits) that sets the block size for I/O block operations for function 1. Valid range is 1 to 2048 bytes. The host must set this value before performing block-mode transfers.

Table 21-23. FBR1R110 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	FNBLKSIZE	R/W	0h	function 1 block size register

21.4.17 CISP1ADDR Register (Offset = 0001FFE0h) [Reset = 00000000h]

CISP1ADDR is shown in Table 21-24.

Return to the Summary Table.

FN0 CIS patch1 address

Table 21-24. CISP1ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	PCH1DAT	R/W	0h	CIS data patch 1
15-0	PCH1ADDR	R/W	0h	CIS address patch 1

21.4.18 CISP2ADDR Register (Offset = 0001FFE4h) [Reset = 00000000h]

CISP2ADDR is shown in Table 21-25.

Return to the Summary Table.

FN0 CIS patch2 address

Table 21-25. CISP2ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	PCH2DAT	R/W	0h	CIS data patch 2
15-0	PCH2ADDR	R/W	0h	CIS address patch 2

21.4.19 CISP3ADDR Register (Offset = 0001FFE8h) [Reset = 00000000h]

CISP3ADDR is shown in Table 21-26.

Return to the Summary Table.

FN0 CIS patch3 address

Table 21-26. CISP3ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	PCH3DAT	R/W	0h	CIS data patch 3
15-0	PCH3ADDR	R/W	0h	CIS address patch 3

21.4.20 CISP4ADDR Register (Offset = 0001FFECh) [Reset = 00000000h]

CISP4ADDR is shown in Table 21-27.

Return to the Summary Table.

FN0 CIS patch4 address

Table 21-27. CISP4ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	PCH4DAT	R/W	0h	CIS data patch 4
15-0	PCH4ADDR	R/W	0h	CIS address patch 4

21.4.21 CISP5ADDR Register (Offset = 0001FFF0h) [Reset = 00000000h]

CISP5ADDR is shown in Table 21-28.

Return to the Summary Table.

FN0 CIS patch5 address

Table 21-28. CISP5ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	PCH5DAT	R/W	0h	CIS data patch 5
15-0	PCH5ADDR	R/W	0h	CIS address patch 5

21.5 SDIO_CARD_FN1 Registers

Table 21-29 lists the memory-mapped registers for the SDIO_CARD_FN1 registers. All register offset addresses not listed in Table 21-29 should be considered as reserved locations and the register contents should not be modified.

Table 21-29. SDIO_CARD_FN1 Registers

Offset	Acronym	Register Name	Section
0h	FLUSHCMD	Buffer Flush Control	Section 21.5.1
4h	RXTHR	Receive Buffer Threshold	Section 21.5.2
Ch	TXIRQTHR	Transmit Interrupt Threshold	Section 21.5.3
10h	DMABLKTHR	DMA Block Threshold	Section 21.5.4
14h	IRQSTA	Interrupt Status	Section 21.5.5
18h	IRQMASK	Interrupt Control Register	Section 21.5.6
1Ch	CTRL	SDIO Control	Section 21.5.7
20h	RXPACS	Receive Packet Length	Section 21.5.8
24h	RXBBUF	Receive Buffer Status	Section 21.5.9
28h	RXBLFT	Receive Bytes Remaining	Section 21.5.10
2Ch	RETCTL	Retry Control	Section 21.5.11
30h	C2HMSG	Controller Message	Section 21.5.12
34h	H2CMSG	Host Message Status	Section 21.5.13
38h	CLKEN	SDIO Clock Inactive	Section 21.5.14
40h	IRQCLR	Interrupt Clear	Section 21.5.15
44h	RSTREQ	SDIO Reset Request	Section 21.5.16
1000h	DATAFIFO	Data Buffer	Section 21.5.17

Complex bit access types are encoded to fit into small table cells. Table 21-30 shows the codes that are used for access types in this section.

Table 21-30. SDIO_CARD_FN1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

21.5.1 FLUSHCMD Register (Offset = 0h) [Reset = 00000000h]

FLUSHCMD is shown in Table 21-31.

Return to the Summary Table.

A write only register. Flush command of the RX / TX buffers

Table 21-31. FLUSHCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TXBUF	W	0h	TX BUFFER FLUSH: Writing to this address triggers the flush command of the TX buffer (data value is irrelevant).
0	RXBUF	W	0h	RX BUFFER FLUSH: Writing to this address triggers the flush command of the RX buffer (data value is irrelevant).

21.5.2 RXTHR Register (Offset = 4h) [Reset = 00000004h]

RXTHR is shown in Table 21-32.

Return to the Summary Table.

A R/W register that stores one of the RX buffer thresholds.

Table 21-32. RXTHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-2	VAL	R/W	1h	Buffer almost full threshold - When passing threshold an interrupt is generated (used by the software to indicate packets in buffer) The threshold is configured to allow receiving a completer packet header including packet length. Typical packet header could be 1 - 128 Bytes however the threshold must be 32bits aligned since SDIO FIFO supports 32bits aligned read only.
1-0	RESERVED	R	0h	Reserved

21.5.3 TXIRQTHR Register (Offset = Ch) [Reset = 00000080h]

TXIRQTHR is shown in Table 21-33.

Return to the Summary Table.

TX IRQ TRIG THR: A R/W register that stores the Threshold in bytes to raise host irq.

Table 21-33. TXIRQTHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VAL	R/W	80h	8-bit value describing the number of bytes needed to trigger host irq 1. If HCI packet length > SDIO block (128-bytes) trigger is set to 128 Byte (entire block) 2. If HCI packet length < SDIO block, FW sets packet length in bytes as the trigger value

21.5.4 DMABLKTHR Register (Offset = 10h) [Reset = 00020002h]

DMABLKTHR is shown in Table 21-34.

Return to the Summary Table.

A R/W register setting the BLOCK SIZE for the RX and TX DMA flow control

Table 21-34. DMABLKTHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18-16	TXDMABLK	R/W	2h	TX DMA BLOCK SIZE SEL: HOST reads from FIFO Determine when to assert flow control to DMA. The flow should be asserted when FIFO has enough free buffer >= Threshold. The threshold is determined according to the DMA block size 0 - 4 Bytes 1 - 8 Bytes 2 - 16 Bytes (Default) 3 - 32 Bytes 4 - 64 Bytes 5 - 128 Bytes 6,7 - Reserved
15-3	RESERVED	R	0h	Reserved
2-0	RXDMABLK	R/W	2h	RX DMA BLOCK SIZE SEL: HOST Writes to FIFO Determine when to assert flow control to DMA. The flow should be asserted when num of bytes in FIFO > Threshold. The threshold is determined according to the DMA block size 0 - 4 Bytes 1 - 8 Bytes 2 - 16 Bytes (Default) 3 - 32 Bytes 4 - 64 Bytes 5 - 128 Bytes 6,7 - Reserved HOST Writes to FIFO Determine when to assert flow control to DMA. The flow should be asserted when num of bytes in FIFO > Threshold. The threshold is determined according to the DMA block size 0 - 4 Bytes 1 - 8 Bytes 2 - 16 Bytes (Default) 3 - 32 Bytes 4 - 64 Bytes 5 - 128 Bytes 6,7 - Reserved

21.5.5 IRQSTA Register (Offset = 14h) [Reset = 00000000h]

IRQSTA is shown in Table 21-35.

Return to the Summary Table.

A RO register. Holds the status of the different interrupts of the SDIO. This register is cleared by writing to IRQ_CLEAR register Each interrupt is set when the event is active. In the case of ACKINT the software has to read the ACKNAK bit value to see if an ACK event was received or a read retry is starting.

Table 21-35. IRQSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13	HOST2CORE	R	0h	Host to Card 15 bit message ready indication
12	CRCERR	R	0h	'1' = CRC Error was detected for rx flow
11	PHYINT	R	0h	SDIO PHY interrupt
10	CARDRST	R	0h	Card Reset interrupt
9	PHYIFERR	R	0h	Error in the OCP interface of the SDIO PHY
8	HCIWRRET	R	0h	HCI packet write retry
7	HCINACK	R	0h	HCI packet NACK interrupt
6	HCIACK	R	0h	HCI packet ACK interrupt
5	TXBUFUNR	R	0h	TX Buffer under-run interrupt
4	TXBUFOVR	R	0h	TX Buffer overrun interrupt
3	RXBUFUNR	R	0h	RX Buffer under-run interrupt
2	RXBUFOVR	R	0h	RX Buffer overrun interrupt
1	FN1EN	R	0h	Function #1 enable interrupt
0	RXALMSFULL	R	0h	RX Buffer almost full interrupt

21.5.6 IRQMASK Register (Offset = 18h) [Reset = 00003FFFh]

IRQMASK is shown in Table 21-36.

Return to the Summary Table.

A R/W register. Holds the mask bits of the different interrupts of the SDIO.

Table 21-36. IRQMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13	HOST2CORE	R/W	1h	Host to Card 15 bit message ready indication
12	CRCERR	R/W	1h	'1' = CRC Error was detected for rx flow
11	PHYMASK	R/W	1h	SDIO PHY interrupt
10	CARDRST	R/W	1h	Card Reset interrupt
9	PHYIFERR	R/W	1h	Error in the OCP interface of the SDIO PHY
8	HCIWRRET	R/W	1h	HCI packet write retry
7	HCINACK	R/W	1h	HCI packet NACK interrupt
6	HCIACK	R/W	1h	HCI packet ACK interrupt
5	TXBUFUNR	R/W	1h	TX Buffer under-run interrupt
4	TXBUFOVR	R/W	1h	TX Buffer overrun interrupt
3	RXBUFUNR	R/W	1h	RX Buffer under-run interrupt
2	RXBUFOVR	R/W	1h	RX Buffer overrun interrupt
1	FN1EN	R/W	1h	Function #1 enable interrupt
0	RXALMSFULL	R/W	1h	RX Buffer almost full interrupt

21.5.7 CTRL Register (Offset = 1Ch) [Reset = 00000007h]

CTRL is shown in Table 21-37.

Return to the Summary Table.

A R/W register to control SDIO operation.

Table 21-37. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	HIRQSYNC	R/W	0h	HOST IRQ SYNCHRONIZATION: This bit controls the synchronization of the host interrupt (interrupt from BT to host through the PHY). '1' - interrupt is synchronized to sdio_clk. '0' - interrupt is not synchronized to sdio_clk (and thus synchronized to ocp_clk)
2	TXFLEN	R/W	1h	TX BUFFER FLUSH ENABLE: Enables the module to flush the TX buffer after receiving packet-read-retry indication (ACK or NACK). When this bit is '0', FW must flush the buffer manually (by writing to FLUSH_CMD register) upon receiving ACK/NACK interrupt. It is needed for the correct operation of the TX FIFO
1	BACE	R/W	1h	BUSY AFTER CRC ERROR: Enables the module to activate the busy signal after CRC error on data only if sdio_enable was set
0	SDIOEN	R/W	1h	SDIO enable - Enable SDIO after CRC error. Cleared by HW after CRC error; Set by FW to de-assert the busy signal

21.5.8 RXPACS Register (Offset = 20h) [Reset = 00000000h]

RXPACS is shown in Table 21-38.

Return to the Summary Table.

RX SDIO PACKET SIZE: A read only register. Holds the length of the current received SDIO packet. Updated at the beginning of each SDIO packet.

Table 21-38. RXPACS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	VAL	R	0h	Length of the current received SDIO packet. Updated at the beginning of each SDIO packet

21.5.9 RXBBUF Register (Offset = 24h) [Reset = 00000000h]

RXBBUF is shown in Table 21-39.

Return to the Summary Table.

RX BYTES IN BUFF: A read only status register. Holds the current number of bytes in SDIO RX buffer.

Table 21-39. RXBBUF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R	0h	Current number of bytes in SDIO RX buffer

21.5.10 RXBLFT Register (Offset = 28h) [Reset = 00000000h]

RXBLFT is shown in Table 21-40.

Return to the Summary Table.

RX BYTES LEFT: A read only status register. A down-count counter. Holds the number of bytes in current SDIO packet that were not transmitted to RX buffer yet. Please notice: Before reading this register, the FW MUST read RX_BYTES_IN_BUFFER register.

Table 21-40. RXBLFT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	BLIL	R	0h	BYTES LEFT IS LOCKED: When '0' - the value that is read from rx_bytes_left is the current number of bytes left to transfer to the end of the block. When '1' - the value that is read from rx_bytes_left is the number of bytes left to transfer to the end of the block that was locked on the last read from RX_BYTES_IN_BUF.
14-11	RESERVED	R	0h	Reserved
10-0	VAL	R	0h	A counter that is loaded with SDIO packet length and decremented the same as the incrementing of bytes-in-buffer status register

21.5.11 RETCTL Register (Offset = 2Ch) [Reset = 00000001h]

RETCTL is shown in Table 21-41.

Return to the Summary Table.

A read/write register. The value states if the BT-SDIO is working with Retry Control mechanism as specified in SDIO spec.

Table 21-41. RETCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	VAL	R/W	1h	When FW writes '1' to this bit, it states that the BT-SDIO is using retry control mechanism. When FW reads this bit, it actually reads the value of the Function 1's RETRY_CONTROL register (the value that the host configured). Default value is '1' because BT FW MUST have retry control mechanism working

21.5.12 C2HMSG Register (Offset = 30h) [Reset = 00000000h]

C2HMSG is shown in Table 21-42.

Return to the Summary Table.

IRQ2Host Message 16b

Table 21-42. C2HMSG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	C2HIRQ	W	0h	CARD TO HOST IRQ: To Host: 16bits MMR which can be written/ read by M33 and read/clear (bit map) by host
15-0	C2HSTS	R/W	0h	CARD TO HOST STS: To Host: 16bits MMR which can be written/ read by M33 and read/clear (bit map) by host Cleared by HOST writing to CLINTERD (Interrupt Clear 0x13)

21.5.13 H2CMSG Register (Offset = 34h) [Reset = 00000000h]

H2CMSG is shown in Table 21-43.

Return to the Summary Table.

IRQ from Host to card Message 16b

Table 21-43. H2CMSG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14-0	H2CSTS	R	0h	HOST TO CARD STS: From Host: 15bits MMR which can be written by host and read/clear (bit map) by M33. (bit 16 is the host_to_card_irq that is generated by the HOST and goes to IRQSTA.HOST_TO_CARD_INT)

21.5.14 CLKEN Register (Offset = 38h) [Reset = 00000000h]

CLKEN is shown in Table 21-44.

Return to the Summary Table.

Clock gating control

Table 21-44. CLKEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	VAL	R/W	0h	1'b0 - disable clk 1'b1 - enable clk

21.5.15 IRQCLR Register (Offset = 40h) [Reset = 00000000h]

IRQCLR is shown in Table 21-45.

Return to the Summary Table.

A write-only register. When written, it clears all SDIO pending interrupts

Table 21-45. IRQCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13	HOST2CORE	W	0h	Host to Card 15 bit message ready indication
12	CRCERR	W	0h	CRC Error clear
11	PHYCLEAR	W	0h	SDIO PHY interrupt clear
10	CARDRST	W	0h	Card Reset interrupt clear
9	PHYIFERR	W	0h	Error in the OCP interface of the SDIO PHY clear
8	HCIWRRET	W	0h	HCI packet write retry clear
7	HCINACK	W	0h	HCI packet NACK interrupt clear
6	HCIACK	W	0h	HCI packet ACK interrupt clear
5	TXBUFUNR	W	0h	TX Buffer under-run interrupt clear
4	TXBUFOVR	W	0h	TX Buffer overrun interrupt clear
3	RXBUFUNR	W	0h	RX Buffer under-run interrupt clear
2	RXBUFOVR	W	0h	RX Buffer overrun interrupt clear
1	FN1EN	W	0h	Function #1 enable interrupt
0	RXALMSFULL	W	0h	RX Buffer almost full interrupt clear

21.5.16 RSTREQ Register (Offset = 44h) [Reset = 00000000h]

RSTREQ is shown in Table 21-46.

Return to the Summary Table.

reset sdio IP due to a SDIO Card Reset command: 0 - do not reset / de-assert initiated sdio reset 1 - initiate reset sdio reset (both PHY and SDIO System)

Table 21-46. RSTREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EN	R/W	0h	Function #1 enable interrupt

21.5.17 DATAFIFO Register (Offset = 1000h) [Reset = 00000000h]

DATAFIFO is shown in Table 21-47.

Return to the Summary Table.

Common shadow register to access SDIO-Card RX-Fifo or TX-Fifo

Table 21-47. DATAFIFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RDRXWRTX	R/W	0h	Common access for either: 1. Reading 'sdio_rxfifo' 2. Writing 'sdio_txfifo' Can be used either as local ocp rd/wr commands, or transactions through DMA machine.

Chapter 22

Inter-Integrated Circuit Sound (I^2S)

This section describes the Inter-IC Sound (I^2S) module.

22.1 Introduction

The I^2S module provides a standardized serial interface to transfer audio samples between the CC35xx device platform and the external audio devices.

The I^2S module has the following features:

- One or two data pins, which can be configured independently as input or output
- I^2S, left-justified (LJF), and right-justified (RJF) serial interface formats that support up to two audio channels per data pin
- Single phased DSP serial interface format that supports up to eight audio channels per data pin
- Up to 32-bit sample word length, with truncation or zero-padding if not matching
- Serial interface to transfer audio samples between wireless devices and external audio devices (Codec or DAC or ADC)
- Support interfacing with PDM digital microphones and generation of PCM samples through software based decimation filtering
- Receive audio source clock from PRCM and generate MCLK, BCLK and WCLK
  - Support up to 5.2MHz on BCLK ouptut
- Configurable sampling frequency (8kHz, 16kHz, 32kHz, 44.1kHz, 48kHz, 64kHz)
- Separate clock enable control bits, one for MCLK and another for BCLK and WCLK
- Two audio channels per data pin (left and right channels) in dual phased communication modes
- Bus master with data buffering for each of the channels and built-in DMA capabilities
- Peripheral port accesses and master port transactions at 80MHz
- Performs direct 32-bit read/write transactions on the master port when sample size is more than 16-bits
  - Adds 8 zeros at LSB for write to SRAM and remove 8 LSB bits for read from SRAM when 32-bit DMA transfer type is selected
- Error detection for DMA and audio clock signal integrity
- Samplestamp generator to maintain correct and constant audio latency between I^2S nodes on the wireless network
  - Samplestamp capture interrupt condition for event based capture operation

22.2 Block Diagram

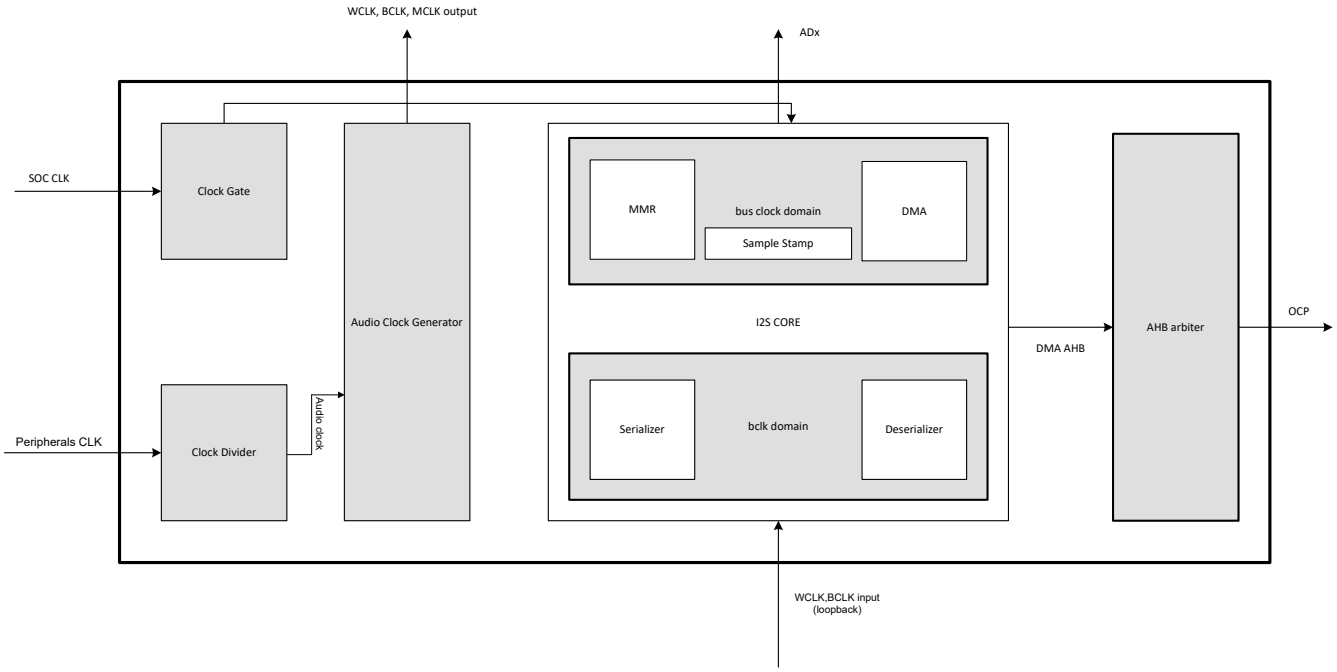

Figure 22-1. I^2S Block Diagram

22.3 Signal Descriptions

- The serial audio interface consists of two or three clock signals and one or two data signals(AD0,AD1), depending on how the I^2S module is used. The clock signals(MCLK,BCLK,WCLK) can be generated either internally (by the I2S module) or externally (by the audio device or another clock source).
- The ADx pins cannot be dynamically placed in a tri-state condition. Therefore, TDM mode is supported for ADx input pins where only external audio devices drive these signals, but TDM mode is not supported for ADx output pins.

22.4 Functional Description

22.4.1 Pin Configuration

The AIFDIRCFG register configures whether each ADx signal is input, output, or unused. Each used I^2S signal must be mapped to a physical I/O pin.

22.4.2 Serial Format Configuration

The WCLK and ADx signals are updated on one edge of the BCLK and sampled on the opposite edge. The sample words transferred on the ADx pins are aligned with the WCLK signal, according to the configured serial interface format. The first WCLK edge of a sample word is either rising or falling, depending on the configured serial interface format. The period from the first WCLK edge of an audio sample (one or more channels) to the first WCLK edge of the next audio sample is called a frame. A frame consists of either one or two phases. A phase is divided into the following intervals:

- Data delay (optional): The BCLK periods between the first WCLK edge and MSB of the (first) audio channel data transferred during the phase
- Word: The BCLK periods during which sample words are transferred on the ADx pin or pins
  - For single-phase, from 1 to 8 sample words are transferred back-to-back.
  - For dual-phase, one sample word is transferred. The least significant bit (LSB) of the sample word can extend into the data delay interval of the next phase.
- Idle (optional): The BCLK periods between the word interval and the next phase.

A sample word on the serial interface can contain from 8 to 32 bits.

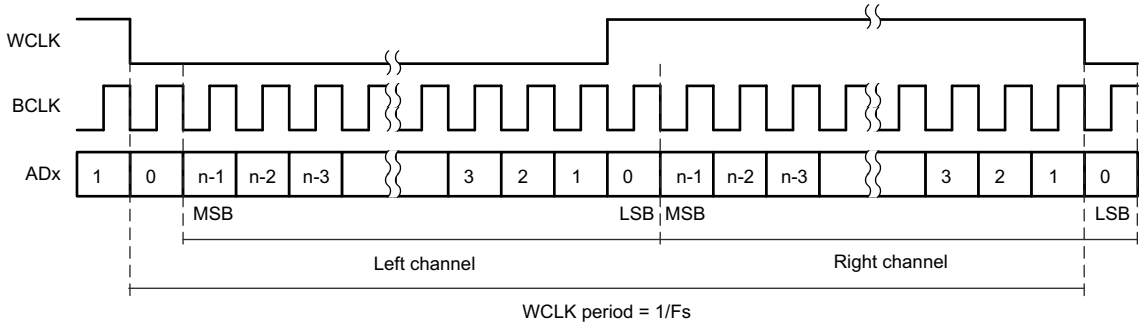

Figure 22-2. I^2S Serial Format

22.4.2.1 Register Configuration

The register configuration follows:

- AIFWCLKSRC.WCLK_INV = 1
- AIFFMTCFG.DUAL_PHASE = 1
- AIFFMTCFG.SMPL_EDGE = 1
- AIFFMTCFG.WORD_LEN = Maximum number of bits per sample word
- AIFFMTCFG.DATA_DELAY = 1

22.4.3 Left-Justified (LJF)

LJF is a dual-phase format with a 50% WCLK duty cycle and the start of an MSB of each sample word aligned with each edge of WCLK. For any given frame, the left channel is transferred first when WCLK is high, and the right channel is transferred next when WCLK is low. Data is sampled on the rising edge of BCLK and updated on the falling edge of BCLK. The below figure shows the LJF serial format.

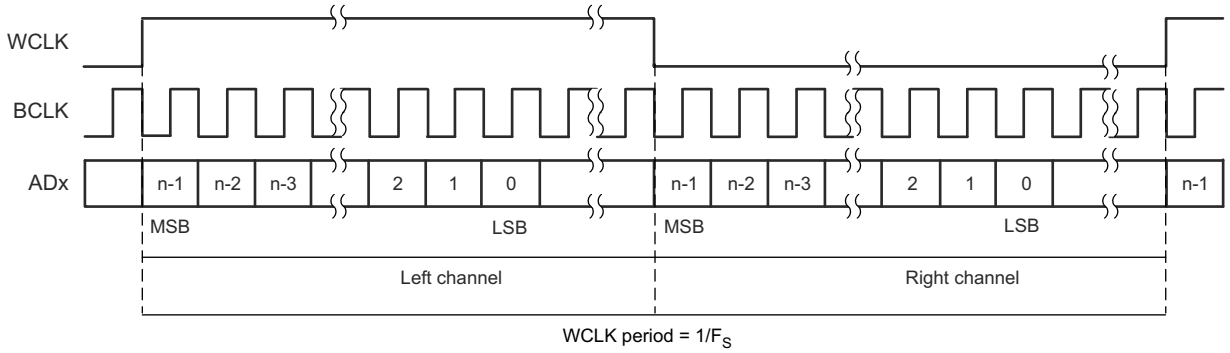

Figure 22-3. Left-Justified Serial Format

22.4.3.1 Register Configuration

The register configuration follows:

- AIFWCLKSRC.WCLK_INV = 0
- AIFFMTCFG.DUAL_PHASE = 1
- AIFFMTCFG.SMPL_EDGE = 1
- AIFFMTCFG.WORD_LEN = Maximum number of bits per sample word
- AIFFMTCFG.DATA_DELAY =0

WORD_LEN must be equal to or less than the number of BCLK periods per phase.

22.4.4 Right-Justified (RJF)

RJF is a dual-phase format with a 50% WCLK duty cycle and the end of an LSB of each sample word aligned with each edge of WCLK. For any given frame, the left channel is transferred first when WCLK is high, and the right channel is transferred next when WCLK is low. Data is sampled on the rising edge of BCLK and updated on the falling edge of BCLK. The below figure showsthe RJF serial format.

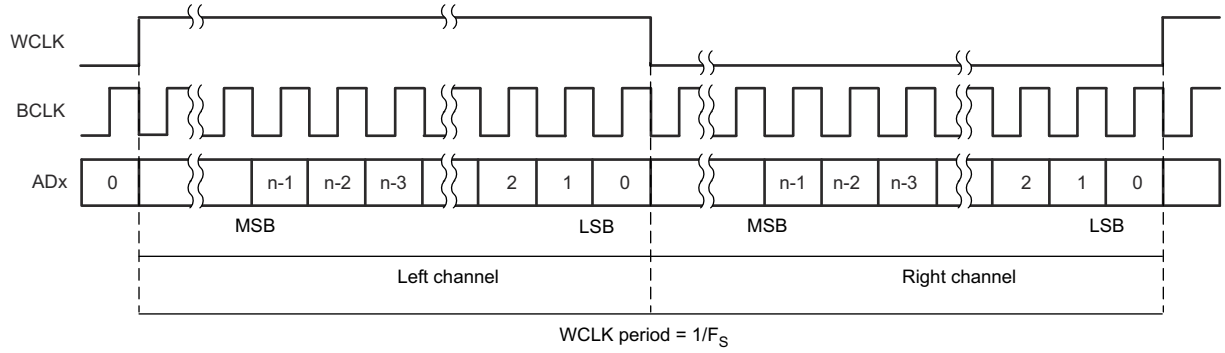

Figure 22-4. Right-Justified Serial Format

22.4.4.1 Register Configuration

The register configuration follows:

- AIFWCLKSRC.WCLK_INV = 0
- AIFFMTCFG.DUAL_PHASE = 1
- AIFFMTCFG.SMPL_EDGE = 1

- AIFFMTCFG.WORD_LEN = Exact number of bits per sample word
- AIFFMTCFG.DATA_DELAY = Number of BCLK periods per phase minus the value of I2S:AIFFMTCFG.WORD_LEN

DATA_DELAY + WORD_LEN must be equal to or less than the number of BCLK periods per phase.

22.4.5 DSP

DSP is a single-phase format where WCLK is high for one BCLK period, and the MSB of the first sample word is typically aligned with this WCLK pulse, or it follows in the next BCLK period. Sample words for subsequent audio channels are then transferred back-to-back, followed by an idle period until the next phase or frame begins. Data is sampled on the falling edge of BCLK and updated on the rising edge of BCLK. The below figure shows the DSP serial format with zero data delay.

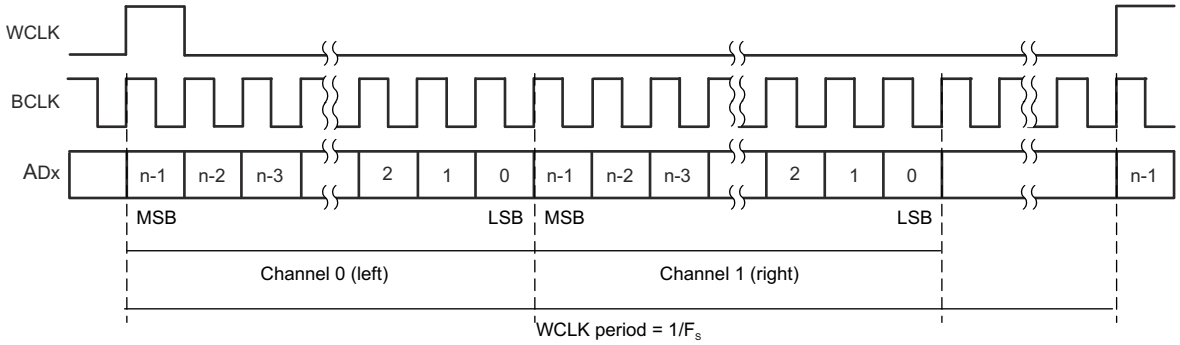

Figure 22-5. DSP Serial Format

22.4.5.1 Register Configuration

The register configuration follows:

- AIFWCLKSRC.WCLK_INV = 0
- AIFFMTCFG.DUAL_PHASE = 0
- AIFFMTCFG.SMPL_EDGE = 0
- AIFFMTCFG.WORD_LEN = Exact number of bits per sample word
- AIFFMTCFG.DATA_DELAY = 0 or 1

DATA_DELAY + (WORD_LEN × channel count) must be equal to or less than the number of BCLK periods per phase.

The channel count is determined by the MSB set in the I2S:AIFWMASK0 and I2S:AIFWMASK1 registers.

22.4.6 Clock Configuration

The audio clocks signals, MCLK, BCLK, and WCLK, can be generated either internally by the PRCM module or by an external clock source. The internally generated audio clock signals might not be suitable for all applications for the reasons that follow:

- Jitter performance
- Clock configuration only provides support for frequencies that can be divided down from 80 MHz.
- Frequency that cannot be tuned to maintain constant audio latency

Internal audio clock source: AIFWCLKSRC = 2

External audio clock source: AIFWCLKSRC = 1

22.5 Memory Interface

The integrated direct memory access controller (DMA) independently handles input samples (from one or two ADx pins to SRAM) and output samples (from SRAM or flash to one or two ADx pins). There is one shift-register and one sample word buffer for each ADx pin. The DMA stores input sample words to memory while the next

sample words are received, and it loads output sample words from memory while the last loaded sample words are transmitted. The DMA operates on blocks of memory. While the DMA works on one block of memory, software must write the start address of the next memory block to AIFINPTRNEXT for input samples and to AIFOUTPTRNEXT for output samples.

22.5.1 Sample Word Length

The sample word length in memory (16 or 32 bits) is configured independently of sample word length on the serial interface (8 to 24 bits). Sample words are truncated when the destination is shorter than the source and zero-padded when the destination is longer than the source. The AIFFMTCFG.MEM_LEN_32 field configures whether sample words in memory are 16 bit or 32 bit:

- 0: Each 16-bit sample word is moved to or from memory using one 16-bit transfer. The DMA pointers written to the AIFINPTRNEXT and AIFOUTPTRNEXT registers must be halfword aligned.
- 1: Each 32-bit sample word is moved to or from memory using one 32-bit transfer. The DMA pointers written to the AIFINPTRNEXT and AIFOUTPTRNEXT registers do not need to be aligned to any memory size.

22.5.2 Padding Mechanism

Padding mechanism:

- **Data Reception:**
  - word len = 24 and mem len = 16; transfer only 16 MSB bits to the memory from DMA and drop 8 LSB bits.
  - 16<=word len<=24 and mem len = 16; transfer only 16 MSB bits to the memory from DMA.
  - 8<=word len < 16 and mem len = 16; Pad the remaining MSB bits with zeros and make a 16 bit data and transfer it to the memory
  - word len = 24 and mem len = 32; Pad additional 8 bits at the LSB with zeros to make a 32-bit data and transfer it to the memory.
  - 8<=word len<=24 and mem len = 32; Pad all the remaining bits at the LSB with zero to make a 32-bit data and transfer it to the memory.
- **Data Transmission:**
  - mem len = 16; Add 8 zeros at the LSB to generate a 24-bit packet for serializer buffer. Depending upon the word len configuration same number of bits will be transferred over AD pins.
  - mem len = 32; Drop the LSB 8-bits and generate a 24-bit packet for serializer buffer. Depending upon the word len configuration same number of bits will be transferred over AD pins.

22.5.3 Channel Mapping

For each ADx pin, the corresponding AIFWMASKx register determines which sample words are present in memory:

- For each frame when AIFFMTCFG.DUAL_PHASE = 0 (DSP format):
  - Input: The AIFWMASKx.MASK register determines whether or not channels are stored to memory.
  - Output: The AIFWMASKx.MASK register determines whether or not channels are fetched from memory. The ADx output is low for excluded channels.
- For each frame when AIFFMTCFG.DUAL_PHASE = 1 (I^2S, LJF, and RJF formats):
  - Mono: AIFWMASKx.MASK = 0x01
    - Input: Left (0) channel is stored to memory.
    - Output: Left (0) channel is fetched from memory and is repeated for the right channel.
  - Stereo: AIFWMASKx.MASK = 0x03
    - Input: Left (0) and right (1) channels are stored to memory.
    - Output: Left (0) and right (1) channels are fetched from memory.

22.5.4 Sample Storage in Memory

Sample words are stored to memory in little-endian byte order, meaning that the least significant byte (LSByte) is stored at the lower byte address, and the most significant byte (MSByte) is stored at the higher byte address.

If both ADx pins are configured as input or both ADx pins are configured as output, the sample words for each audio channel are stored AD0 first and AD1 last.

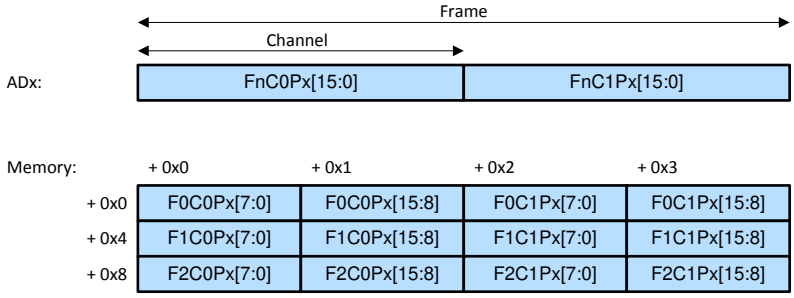

Figure 22-6. 16-Bit Stereo I^2S, LJF, and RJF Formats on One ADx Pin, Showing Three Frames in Memory

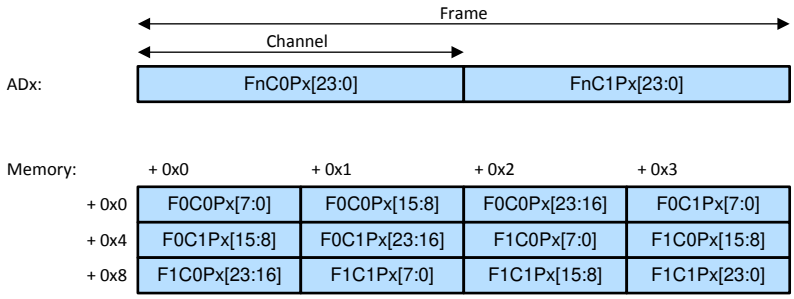

Figure 22-7. 24-Bit Stereo I^2S, LJF, and RJF Formats on One ADx Pin, Showing Two Frames in Memory

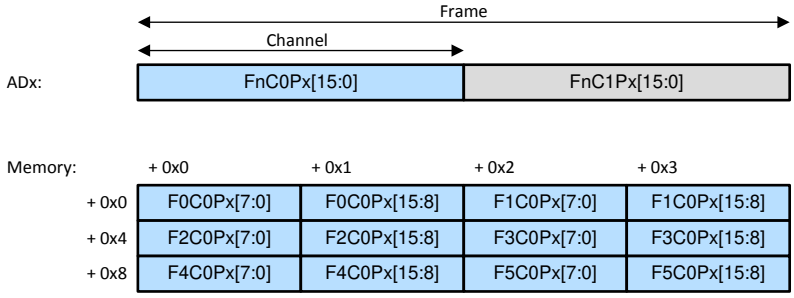

Figure 22-8. 16-Bit Mono I^2S, LJF, and RJF Formats on One ADx Pin, Showing Six Frames in Memory

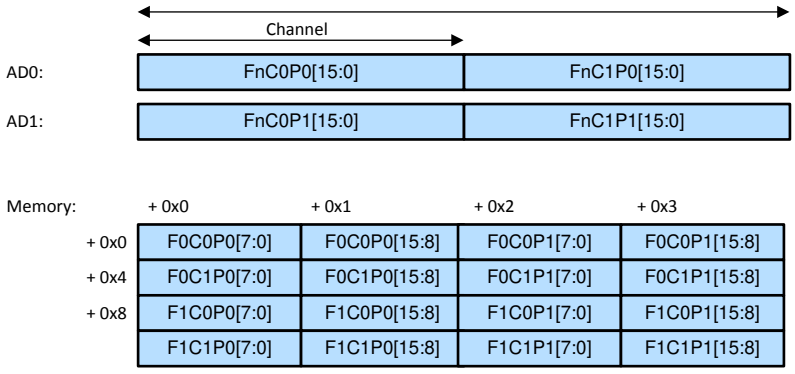

Figure 22-9. 16-Bit I^2S Format on AD0 and AD1 Pins, Showing Two Frames in Memory

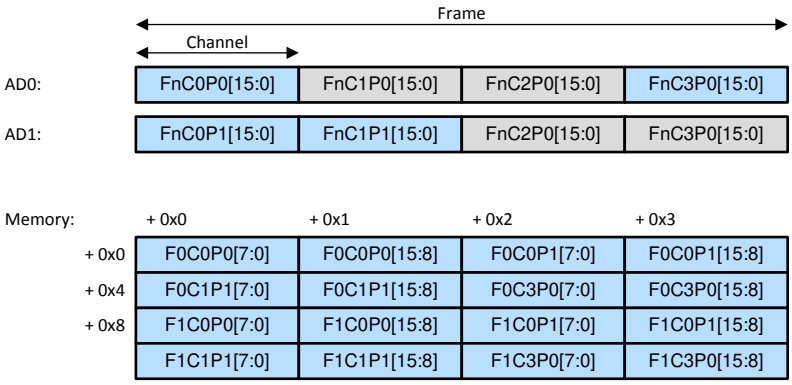

Figure 22-10. 16-Bit DSP Format on AD0 and AD1 Pins, Showing Two Frames in Memory

22.5.5 DMA Operation

The DMA operates on blocks of memory. Each input and output DMA memory block contains the input and output sample words, respectively, for AIFDMACFG.END_FRAME_IDX + 1 frames.

Writing a nonzero value to AIFDMACFG.END_FRAME_IDX initializes the DMA and prepares it to be started. Writing zero to AIFDMACFG.END_FRAME_IDX disables the DMA and resets the serial audio interface.

If input ADx pins are used, software must write memory block start addresses for input DMA to AIFINPTRNEXT. The current input DMA memory location can be observed in AIFINPTR.

If output ADx pins are used, software must write memory block start addresses for output DMA to AIFOUTPTRNEXT. The current output DMA memory location can be observed in AIFOUTPTR.

This writing operation or DMA operation allows the software to implement sample block ring buffers in memory with an arbitrary number of blocks for input and output samples.

22.5.5.1 Start-Up

All other audio interface-related register configuration (pins, serial format, clocks, sample word sizes, and channel mapping) must be completed before writing a nonzero value to theAIFDMACFG.END_FRAME_IDX register. To prepare input and output DMA for start-up, the software must preload the first and second DMA pointers to be used and must arm the DMA:

- Write the first memory block start addresses to be used to AIFINPTRNEXT and (or) AIFOUTPTRNEXT
- Set AIFDMACFG.END_FRAME_IDX = the number of frames per block minus one.
  - This loads AIFINPTRNEXT into AIFINPTR, and AIFOUTPTRNEXT into AIFOUTPTR, and the output DMA will immediately prefetch sample words for the first two audio channels.
- Write the second memory block start addresses to be used to AIFINPTRNEXT and (or) AIFOUTPTRNEXT.

22.5.5.2 Operation

To maintain DMA operation, software must provide new memory block start addresses each time a memory block is finished. When a block is finished, the following occurs:

- For the input memory interface block:
  - AIFINPTR = AIFINPTRNEXT
  - AIFINPTRNEXT = 0x0000 0000
  - IRQFLAGS.AIF_DMA_IN is set to generate an I2S_IRQ interrupt.
- For the output memory interface block:
- AIFOUTPTR = AIFOUTPTRNEXT
- AIFOUTPTRNEXT = 0x0000 0000
- IRQFLAGS.AIF_DMA_OUT is set to generate an I2S_IRQ interrupt.

To handle this operation, software must either poll if the AIFINPTRNEXT and (or) AIFOUTPTRNEXT registers are zero, or use the IRQFLAGS.AIF_DMA_IN and (or) IRQFLAGS.AIF_DMA_OUT interrupt requests.

Software must write the new memory block start addresses to AIFINPTRNEXT and (or) AIFOUTPTRNEXT before the running block finishes. If the running block finishes while AIFINPTRNEXT and (or) AIFOUTPTRNEXT are zero, the affected DMA channels stop and IRQFLAGS.PTR_ERR is set.

22.5.5.3 Shutdown

Before DMA shutdown, all output external audio devices (for example, a DAC) should be muted, or silence should the transmitted on output ADx pins. The DMA must not be stopped while there could be an ongoing DMA memory transfer.. When using the internal audio clock source or an external audio clock source that cannot stop unexpectedly, software should use the following procedure to stop the DMA:

- Stop writing to the AIFINPTRNEXT and/or AIFOUTPTRNEXT registers.
- Optional: Wait for IRQFLAGS.PTR_ERR to occur.
- Wait for AIFINPTRNEXT and AIFOUTPTRNEXT to become zero.
- Write AIFDMACFG.END_FRAME_IDX = 0.

When using an external audio clock source that can stop unexpectedly, software should use the following procedure to stop the DMA:

- Stop writing to the AIFINPTRNEXT and (or) AIFOUTPTRNEXT registers.
- Stop the external audio clock source.
- Wait for IRQFLAGS.WCLK_TIMEOUT to occur, or for AIFINPTRNEXT and AIFOUTPTRNEXT to become zero, whichever happens first.
- Write AIFDMACFG.END_FRAME_IDX = 0.

22.6 Samplestamp Generator

The samplestamp generator is used to start input and output DMA operation. The samplestamp generator is also used to synchronize I^2S modules over a wireless network, so correct and fixed audio latency can be achieved. Synchronization over a wireless network is an optional feature that can be bypassed. The samplestamp generator is enabled and is running while STMPCTL.STMP_EN = 1. Counter and capture registers are reset when software writes STMPCTL.STMP_EN = 0.

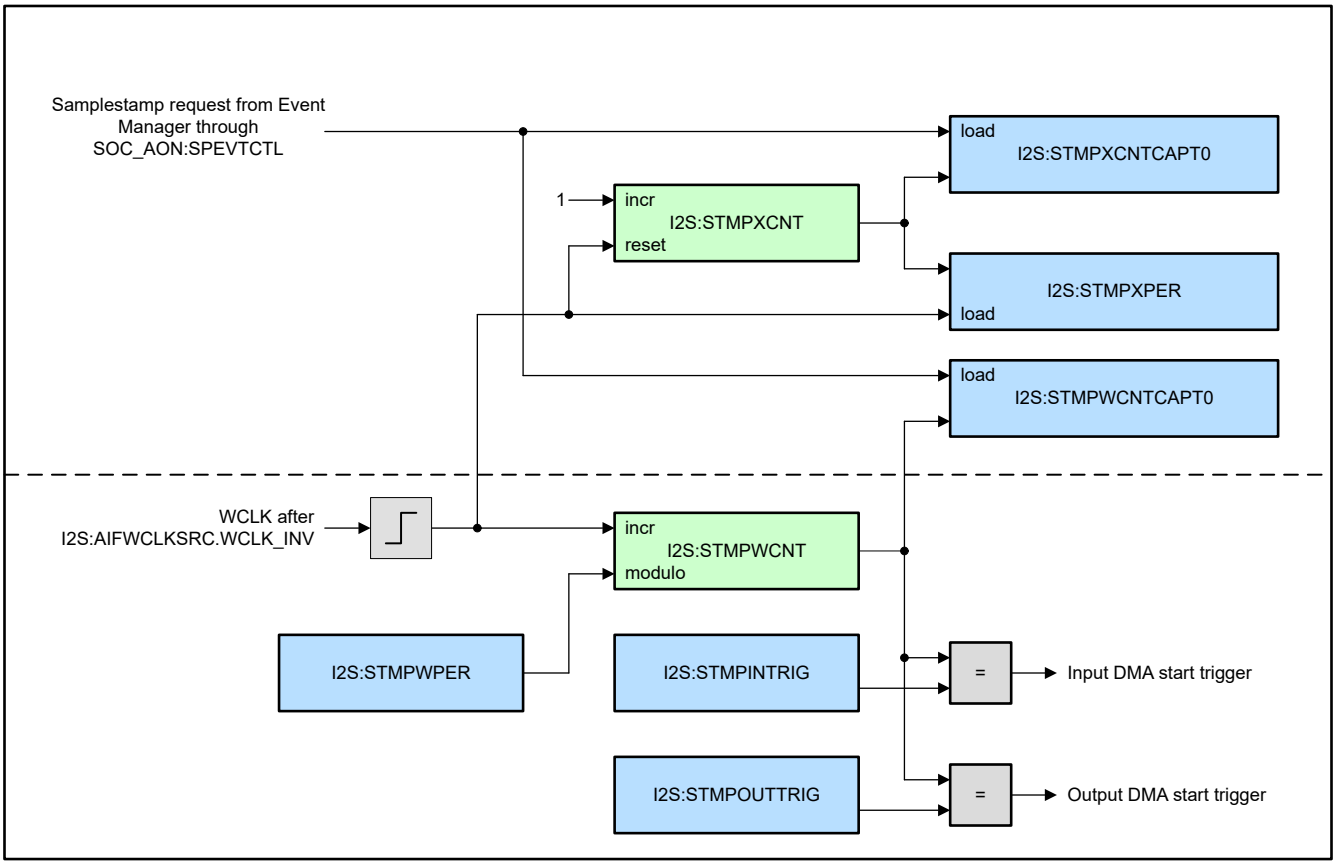

Figure 22-11. Samplestamp Generator

22.6.1 Samplestamp Counters

The samplestamp generator counts frames (WCLK periods) and 80 MHz clock cycles (crystal oscillator periods) within each frame:

- STMPWCNT increments at the first WCLK edge of each frame, module the period value STMPWPER.
- STMPXCNT resets to 0 at the first WCLK edge of each frame, and then increments by 1 for each 80 MHz clock cycle. Reading STMPWCNT latches the read value of STMPXCNT.

Software can modify the value of STMPWCNT by writing an absolute value to STMPWSET or a relative value to STMPWADD.

22.6.2 Start-Up Triggers

The STMPINTRIG and STMPOUTTRIG registers contain STMPWCNT compare values that are used to start the input and output DMA, respectively:

- When STMPWCNT equals STMPINTRIG, the input DMA begins storing sample words to memory in the next frame: (STMPINTRIG + 1) % STMPWPER
- When STMPWCNT equals STMPOUTTRIG, the output DMA begins outputting sample words from memory in the next frame: (STMPOUTTRIG + 1) % STMPWPER

To avoid false start-up triggers, STMPINTRIG and STMPOUTTRIG must initially be equal to or higher than STMPWPER.

The STMPCTL.IN_RDY and STMPCTL.OUT_RDY status bits are set when the input and output DMA are ready to be started and cleared when DMA start triggers have occurred.

22.6.3 Samplestamp Capture

A capture request signal can be routed from connectivity core to trigger samplestamp capture. Whenever the event - samplestamp request(pulse detection inside the IP) signal is high:

- The current value of STMPXCNT is copied into STMPXCNTCAPT0.
- The current value of STMPWCNT is copied into STMPWCNTCAPT0.

Also, on the first WCLK edge of each frame, the current value of STMPXCNT is captured in STMPXPER, and STMPXCNT then restarts counting from 0.

Using these values, a fixed-point samplestamp value can be calculated:

STMPWCNTCAPT0 + (STMPXCNTCAPT0 / STMPXPER)

Notice that the value of STMPXPER will not normally be captured at the same time as the other values. Therefore, STMPXPER can be less than STMPXCNTCAPT0.

22.6.4 Achieving constant audio latency

The following actions can be taken to achieve the same constant audio latency in either direction over a wireless network (from the I^2S pins on one wireless device platform to the I^2S pins on another wireless device platform):

- One node must be defined as audio clock master and the other node must be defined as audio clock slave. The slave must use an external audio clock source with adjustable rate.
- For both nodes, set STMPWPER = N × (AIFDMACFG.END_FRAME_IDX + 1), where N is a whole number.
  - The value of STMPWPER equals audio latency in number of frames.
  - The value of STMPWPER also equals the memory buffer size in number of samples.
- Perform samplestamp capture on the master when it transmits the RF packet synchronization word, and include the value of the fixed-point samplestamp in the transmitted packet.
- Perform samplestamp capture on the slave when it receives the RF packet synchronization word, and store the samplestamp value of the master in the RF packet. Calculate the difference between the samplestamp values of the master and slave, which is used to:
  - Initially offset the STMPWCNT counter of the slave so that it matches the samplestamp value of the master.
  - While running, adjust the external audio clock source rate so that the difference between the samplestamp values of the slave and the master approach 0.
- For both nodes, set up DMA pointers and DMA start triggers so that the value of STMPWCNT represents the input and output buffer positions of the current frame on the ADx pins.

22.7 Error Detection

The I^2S module can detect errors related to the following:

- DMA operation
- Audio clock signal integrity

The following errors are detected:

- WCLK frequency error (STMPXPERMIN:VALUE)
- Noise on the WCLK signal (IRQFLAGS:WCLK_ERR)
- Audio clock loss (IRQFLAGS:WCLK_TIMEOUT)
- DMA pointer not loaded in time (IRQFLAGS:PTR_ERR)
- DMA transfer not completed in time (IRQFLAGS:BUS_ERR)

22.8 Usage

22.8.1 Start-Up Sequence

Perform the following steps in the indicated order to begin I^2S module operation:

1. Set up dependencies

2. Configure the pins
3. Configure the serial format
4. Configure the clock
5. Configure the sample word length
6. Configure the channel mapping
7. Perform the DMA start-up sequence
8. Set up the samplestamp generator:
   a. Set the STMPWPER register.
   b. Set the STMPINTRIG and STMPOUTTRIG > STMPWPER to avoid false DMA start triggers.
   c. Set STMPCTL.EN = 1
   d. If needed, follow the guidelines for achieving constant audio latency.
   e. Otherwise, just set STMPINTRIG and STMPOUTTRIG to match the current (STMPWCNT + 2) % STMPWPER.

Note

DMA interrupts will begin after the DMA has completed the first sample block or blocks.

22.8.2 Shutdown Sequence

Perform the following steps in the indicated order to end I^2S module operation:

1. DMA shutdown sequence
2. Set STMPCTL.EN = 0
3. Disable the internal or external audio clock source
4. Disable dependencies

22.9 I^2S Configuration Guideline

1. On reset, all the MMRs will be initialized to their default values and clocks are disabled.
2. Enable the SOC CLK and pull the I^2S clock enable high to configure the MMRs. Don't configure the I^2S clock generation MMR at PRCM module at this point.
3. For I^2S BCLK loop back configure the loopback pad as input for BCLK to pass through
4. Configuration sequence of I^2S MMR:
   a. All the general configurations of I^2S to be done (pins, serial format, clocks, sample word sizes, channel mapping, div values for audio clock gen)
   b. Once the I^2S audio clock gen unit related configuration is done, configure the audio clock MMR in ckmdig. [Note: Optional if internally generated clocks are to be used for I^2S operation.]
   c. Make AIFCLKCTL.WB_EN = 1 to enable the generation of wclk and bclk. [Note: Optional if we want to enable the internal generation of clocks.]
   d. AIFWCLKSRC.WCLK_SRC can be configured to select either internal or external clock generator source. After this, bclk will be provided to bclk domain and its configuration cannot change. Otherwise, it will lead to metastability issues.
   e. Configure the DMA sequence. This will enable the AIF module.
   f. Configure the MMRs related with the samplestamp generator.

22.10 I2S Registers

Table 22-1 lists the memory-mapped registers for the I2S registers. All register offset addresses not listed in Table 22-1 should be considered as reserved locations and the register contents should not be modified.

Table 22-1. I2S Registers

Offset	Acronym	Register Name	Section
0h	AIFWCLKSRC	Wordclock Source Selection	Section 22.10.1
4h	AIFDMACFG	DMA Buffer Size Configuration	Section 22.10.2
8h	AIFDIRCFG	Pin Direction Configuration	Section 22.10.3
Ch	AIFFMTCFG	Format Configuration	Section 22.10.4
10h	AIFWMASK0	Word Selection Mask	Section 22.10.5
14h	AIFWMASK1	Audio Input Mask	Section 22.10.6
20h	AIFINPTNXT	Input Buffer Pointer	Section 22.10.7
24h	AIFINPTR	Input Buffer Pointer	Section 22.10.8
28h	AIFOPTNXT	Output Buffer Pointer	Section 22.10.9
2Ch	AIFOUTPTR	Output Buffer Pointer	Section 22.10.10
34h	STMPCTL	Timestamp Control	Section 22.10.11
38h	STMPXCPT0	Capture Value Ch0	Section 22.10.12
3Ch	STMPXPER	Crystal Oscillator Period	Section 22.10.13
40h	STMPWCPT0	Clock Counter Capture	Section 22.10.14
44h	STMPWPER	Clock Counter Period	Section 22.10.15
48h	STMPINTRIG	Word Clock Counter Value	Section 22.10.16
4Ch	STMPOTRIG	Output Trigger Value	Section 22.10.17
50h	STMPWSET	Timestamp Set	Section 22.10.18
54h	STMPWADD	Clock Counter Add	Section 22.10.19
58h	STMPXPRMIN	Oscillator Minimum Period	Section 22.10.20
5Ch	STMPWCNT	Watch Counter Value	Section 22.10.21
60h	STMPXCNT	X Counter Value	Section 22.10.22
70h	IRQMASK	Interrupt Mask	Section 22.10.23
74h	IRQFLAGS	Interrupt Status	Section 22.10.24
78h	IRQSET	Interrupt Set	Section 22.10.25
7Ch	IRQCLR	Interrupt Clear	Section 22.10.26
80h	AIFMCLKDIV	Main Clock Divider	Section 22.10.27
84h	AIFBCLKDIV	Bit Clock Divider	Section 22.10.28
88h	AIFWCLKDIV	WCLK Division Ratio	Section 22.10.29
8Ch	AIFCLKCTL	Internal Audio Clock Control	Section 22.10.30
1000h	CLKCFG	Clock Configuration	Section 22.10.31
1004h	ADFSCTRL1	Reference Time Control	Section 22.10.32
1008h	ADFSCTRL2	Configuration Control	Section 22.10.33

Complex bit access types are encoded to fit into small table cells. Table 22-2 shows the codes that are used for access types in this section.

Table 22-2. I2S Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		

Table 22-2. I2S Access Type Codes (continued)

Access Type	Code	Description
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

22.10.1 AIFWCLKSRC Register (Offset = 0h) [Reset = 00000000h]

AIFWCLKSRC is shown in Table 22-3.

Return to the Summary Table.

WCLK Source Selection

Table 22-3. AIFWCLKSRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	WCLKINV	R/W	0h	Inverts **WCLK** source (pad or internal) when set. 0: Not inverted 1: Inverted
1-0	WBCLKSRC	R/W	0h	Selects **WCLK**/**BCLK** source for **AIF**. 0h = None ('0') 1h = External **WCLK** generator, from pad 2h = Internal **WCLK** generator, from module PRCM 3h = Not supported. Will give same **WCLK** as 'NONE' ('00')

22.10.2 AIFDMACFG Register (Offset = 4h) [Reset = 00000000h]

AIFDMACFG is shown in Table 22-4.

Return to the Summary Table.

DMA Buffer Size Configuration

Table 22-4. AIFDMACFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	ENDFRAMIDX	R/W	0h	Defines the length of the DMA buffer. Writing a non-zero value to this register field enables and initializes AIF. Note that before doing so, all other configuration must have been done, and [AIFINPTRNEXT.*]/[AIFOUTPTRNEXT.*] must have been loaded.

22.10.3 AIFDIRCFG Register (Offset = 8h) [Reset = 00000000h]

AIFDIRCFG is shown in Table 22-5.

Return to the Summary Table.

Pin Direction

Table 22-5. AIFDIRCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-6	RESERVED	R	0h	Reserved
5-4	AD1	R/W	0h	Configures the **AD1** audio data pin usage: 0x3: Reserved 0h = Not in use (disabled) 1h = Input mode 2h = Output mode
3-2	RESERVED	R	0h	Reserved
1-0	AD0	R/W	0h	Configures the **AD0** audio data pin usage: 0x3: Reserved 0h = Not in use (disabled) 1h = Input mode 2h = Output mode

22.10.4 AIFFMTCFG Register (Offset = Ch) [Reset = 00000000h]

AIFFMTCFG is shown in Table 22-6.

Return to the Summary Table.

Serial Interface Format Configuration

Table 22-6. AIFFMTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	DATADELAY	R/W	1h	The number of **BCLK** periods between a **WCLK** edge and **MSB** of the first word in a phase: 0x00: **LJF** and **DSP** format 0x01: **I2S** and **DSP** format 0x02: **RJF** format ... 0xFF: **RJF** format Note: When 0, **MSB** of the next word will be output in the idle period between **LSB** of the previous word and the start of the next word. Otherwise logical 0 will be output until the data delay has expired.
7	LEN32	R/W	0h	The size of each word stored to or loaded from memory: 0h = 16BIT : 16-bit (one 16 bit access per sample) 1h = 32BIT : 32-bit(one 32-bit access per sample)
6	SMPLEDGE	R/W	1h	On the serial audio interface, data (and wclk) is sampled and clocked out on opposite edges of BCLK. 0h = Data is sampled on the negative edge and clocked out on the positive edge. 1h = Data is sampled on the positive edge and clocked out on the negative edge.
5	DUALPHASE	R/W	1h	Selects dual- or single-phase format. 0: Single-phase: **DSP** format 1: Dual-phase: **I2S**, **LJF** and **RJF** formats
4-0	WORDLEN	R/W	10h	Number of bits per word (8-24): In single-phase format, this is the exact number of bits per word. In dual-phase format, this is the maximum number of bits per word. Values below 8 and above 24 give undefined behavior. Data written to memory is always aligned to 16 or 24 bits as defined by [MEM_LEN_24]. Bit widths that differ from this alignment will either be truncated or zero padded.

22.10.5 AIFWMASK0 Register (Offset = 10h) [Reset = 00000000h]

AIFWMASK0 is shown in Table 22-7.

Return to the Summary Table.

Word Selection Bit Mask for Pin 0

Table 22-7. AIFWMASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	MASK	R/W	3h	Bit-mask indicating valid channels in a frame on AD0. In single-phase mode, each bit represents one channel, starting with **LSB** for the first word in the frame. A frame can contain up to 8 channels. Channels that are not included in the mask will not be sampled and stored in memory, and clocked out as '0'. In dual-phase mode, only the two **LSB**s are considered. For a stereo configuration, set both bits. For a mono configuration, set bit 0 only. In mono mode, only channel 0 will be sampled and stored to memory, and channel 0 will be repeated when clocked out. In mono mode, only channel 0 will be sampled and stored to memory, and channel 0 will be repeated in the second phase when clocked out. If all bits are zero, no input words will be stored to memory, and the output data lines will be constant '0'. This can be utilized when **PWM** debug output is desired without any actively used output pins.

22.10.6 AIFWMASK1 Register (Offset = 14h) [Reset = 00000000h]

AIFWMASK1 is shown in Table 22-8.

Return to the Summary Table.

Word Selection Bit Mask for Pin 1

Table 22-8. AIFWMASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	MASK	R/W	3h	Bit-mask indicating valid channels in a frame on AD1. In single-phase mode, each bit represents one channel, starting with **LSB** for the first word in the frame. A frame can contain up to 8 channels. Channels that are not included in the mask will not be sampled and stored in memory, and clocked out as '0'. In dual-phase mode, only the two **LSB**s are considered. For a stereo configuration, set both bits. For a mono configuration, set bit 0 only. In mono mode, only channel 0 will be sampled and stored to memory, and channel 0 will be repeated when clocked out. In mono mode, only channel 0 will be sampled and stored to memory, and channel 0 will be repeated in the second phase when clocked out. If all bits are zero, no input words will be stored to memory, and the output data lines will be constant '0'. This can be utilized when **PWM** debug output is desired without any actively used output pins.

22.10.7 AIFINPTNXT Register (Offset = 20h) [Reset = 00000000h]

AIFINPTNXT is shown in Table 22-9.

Return to the Summary Table.

DMA Input Buffer Next Pointer

Table 22-9. AIFINPTNXT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTR	R/W	0h	Pointer to the first byte in the next **DMA** input buffer. The read value equals the last written value until the currently used **DMA** input buffer is completed, and then becomes null when the last written value is transferred to the **DMA** controller to start on the next buffer. This event is signalized by [IRQFLAGS-AIF_DMA_IN]. At startup, the value must be written once before and once after configuring the **DMA** buffer size in [AIFDMACFG.*]. The next pointer must be written to this register while the **DMA** function uses the previously written pointer. If not written in time, PTRERR will be raised and all input pins will be disabled.

22.10.8 AIFINPTR Register (Offset = 24h) [Reset = 00000000h]

AIFINPTR is shown in Table 22-10.

Return to the Summary Table.

DMA Input Buffer Current Pointer

Table 22-10. AIFINPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTR	R	0h	Value of the **DMA** input buffer pointer currently used by the **DMA** controller. Incremented by 1 (byte) or 2 (word) for each **AHB** access.

22.10.9 AIFOPTNXT Register (Offset = 28h) [Reset = 00000000h]

AIFOPTNXT is shown in Table 22-11.

Return to the Summary Table.

DMA Output Buffer Next Pointer

Table 22-11. AIFOPTNXT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTR	R/W	0h	Pointer to the first byte in the next **DMA** output buffer. The read value equals the last written value until the currently used **DMA** output buffer is completed, and then becomes null when the last written value is transferred to the **DMA** controller to start on the next buffer. This event is signalized by AIFDMAOUT. At startup, the value must be written once before and once after configuring the **DMA** buffer size in [AIFDMACFG.*]. At this time, the first two samples will be fetched from memory. The next pointer must be written to this register while the **DMA** function uses the previously written pointer. If not written in time, PTRERR will be raised and all output pins will be disabled.

22.10.10 AIFOUTPTR Register (Offset = 2Ch) [Reset = 00000000h]

AIFOUTPTR is shown in Table 22-12.

Return to the Summary Table.

DMA Output Buffer Current Pointer

Table 22-12. AIFOUTPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTR	R	0h	Value of the **DMA** output buffer pointer currently used by the **DMA** controller Incremented by 1 (byte) or 2 (word) for each **AHB** access.

22.10.11 STMPCTL Register (Offset = 34h) [Reset = 00000000h]

STMPCTL is shown in Table 22-13.

Return to the Summary Table.

Samplestamp Generator Control Register

Table 22-13. STMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	OUTRDY	R	0h	Low until the output pins are ready to be started by the samplestamp generator. When started (that is [STMPOUTTRIG.*] equals the **WCLK** counter) the bit goes back low.
1	INRDY	R	0h	Low until the input pins are ready to be started by the samplestamp generator. When started (that is [STMPINTRIG.*] equals the **WCLK** counter) the bit goes back low.
0	STMPEN	R/W	0h	Enables the samplestamp generator. The samplestamp generator must only be enabled after it has been properly configured. When cleared, all samplestamp generator counters and capture values are cleared.

22.10.12 STMPXCPT0 Register (Offset = 38h) [Reset = 00000000h]

STMPXCPT0 is shown in Table 22-14.

Return to the Summary Table.

Captured **XOSC** Counter Value, Capture Channel 0

Table 22-14. STMPXCPT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CAPTVAL	R	0h	The value of the samplestamp **XOSC** counter (CURRVAL) last time an event was pulsed (event source selected in [EVENT.I2SSTMPSEL0.EV] for channel 0). This number corresponds to the number of 24 MHz clock cycles since the last positive edge of the selected **WCLK**. The value is cleared when STMPEN = 0. Note: Due to buffering and synchronization, **WCLK** is delayed by a small number of **BCLK** periods and clk periods. Note: When calculating the fractional part of the sample stamp, [STMPXPER.*] may be less than this bit field.

22.10.13 STMPXPER Register (Offset = 3Ch) [Reset = 00000000h]

STMPXPER is shown in Table 22-15.

Return to the Summary Table.

XOSC Period Value

Table 22-15. STMPXPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALUE	R	0h	The number of 24 MHz clock cycles in the previous **WCLK** period (that is - the next value of the **XOSC** counter at the positive **WCLK** edge, had it not been reset to 0). The value is cleared when STMPEN = 0.

22.10.14 STMPWCPT0 Register (Offset = 40h) [Reset = 00000000h]

STMPWCPT0 is shown in Table 22-16.

Return to the Summary Table.

Captured **WCLK** Counter Value, Capture Channel 0

Table 22-16. STMPWCPT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CAPTVAL	R	0h	The value of the samplestamp **WCLK** counter (CURRVAL) last time an event was pulsed (event source selected in [EVENT:I2SSTMPSEL0.EV] for channel 0). This number corresponds to the number of positive **WCLK** edges since the samplestamp generator was enabled (not taking modification through [STMPWADD.*]/[STMPWSET.*] into account). The value is cleared when STMPEN = 0.

22.10.15 STMPWPER Register (Offset = 44h) [Reset = 00000000h]

STMPWPER is shown in Table 22-17.

Return to the Summary Table.

WCLK Counter Period Value

Table 22-17. STMPWPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALUE	R/W	0h	Used to define when [STMPWCNT.*] is to be reset so number of **WCLK** edges are found for the size of the sample buffer. This is thus a modulo value for the **WCLK** counter. This number must correspond to the size of the sample buffer used by the system (that is the index of the last sample plus 1).

22.10.16 STMPINTRIG Register (Offset = 48h) [Reset = 00000000h]

STMPINTRIG is shown in Table 22-18.

Return to the Summary Table.

WCLK Counter Trigger Value for Input Pins

Table 22-18. STMPINTRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	INSTRTWCNT	R/W	0h	Compare value used to start the incoming audio streams. This bit field shall equal the **WCLK** counter value during the **WCLK** period in which the first input word(s) are sampled and stored to memory (that is the sample at the start of the very first **DMA** input buffer). The value of this register takes effect when the following conditions are met: - One or more pins are configured as inputs in [AIFDIRCFG.*]. - [AIFDMACFG.*] has been configured for the correct buffer size, and at least 32 **BCLK** cycle ticks have happened. Note: To avoid false triggers, this bit field should be set higher than VALUE.

22.10.17 STMPOTRIG Register (Offset = 4Ch) [Reset = 00000000h]

STMPOTRIG is shown in Table 22-19.

Return to the Summary Table.

WCLK Counter Trigger Value for Output Pins

Table 22-19. STMPOTRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	OSTRTWCNT	R/W	0h	OUT START WCNT: Compare value used to start the outgoing audio streams. This bit field must equal the **WCLK** counter value during the **WCLK** period in which the first output word(s) read from memory are clocked out (that is the sample at the start of the very first **DMA** output buffer). The value of this register takes effect when the following conditions are met: - One or more pins are configured as outputs in [AIFDIRCFG.*]. - [AIFDMACFG.*] has been configured for the correct buffer size, and 32 **BCLK** cycle ticks have happened. - 2 samples have been preloaded from memory (examine the [AIFOUTPTR.*] register if necessary). Note: The memory read access is only performed when required, that is channels 0/1 must be selected in [AIFWMASK0.*]/[AIFWMASK1.*]. Note: To avoid false triggers, this bit field should be set higher than VALUE.

22.10.18 STMPWSET Register (Offset = 50h) [Reset = 00000000h]

STMPWSET is shown in Table 22-20.

Return to the Summary Table.

WCLK Counter Set Operation

Table 22-20. STMPWSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALUE	W	0h	**WCLK** counter modification: Sets the running **WCLK** counter equal to the written value.

22.10.19 STMPWADD Register (Offset = 54h) [Reset = 00000000h]

STMPWADD is shown in Table 22-21.

Return to the Summary Table.

WCLK Counter Add Operation

Table 22-21. STMPWADD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALINC	W	0h	**WCLK** counter modification: Adds the written value to the running **WCLK** counter. If a positive edge of **WCLK** occurs at the same time as the operation, this will be taken into account. To add a negative value, write 'VALUE - value'.

22.10.20 STMPXPRMIN Register (Offset = 58h) [Reset = 00000000h]

STMPXPRMIN is shown in Table 22-22.

Return to the Summary Table.

XOSC Minimum Period Value Minimum Value of [STMPXPER.*]

Table 22-22. STMPXPRMIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALUE	R/W	FFFFh	Each time [STMPXPER.*] is updated, the value is also loaded into this register, provided that the value is smaller than the current value in this register. When written, the register is reset to 0xFFFF (65535), regardless of the value written. The minimum value can be used to detect extra **WCLK** pulses (this registers value will be significantly smaller than VALUE).

22.10.21 STMPWCNT Register (Offset = 5Ch) [Reset = 00000000h]

STMPWCNT is shown in Table 22-23.

Return to the Summary Table.

Current Value of WCNT

Table 22-23. STMPWCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CURRVAL	R	0h	Current value of the **WCLK** counter

22.10.22 STMPXCNT Register (Offset = 60h) [Reset = 00000000h]

STMPXCNT is shown in Table 22-24.

Return to the Summary Table.

Current Value of XCNT

Table 22-24. STMPXCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CURRVAL	R	0h	Current value of the **XOSC** counter, latched when reading [STMPWCNT.*].

22.10.23 IRQMASK Register (Offset = 70h) [Reset = 00000000h]

IRQMASK is shown in Table 22-25.

Return to the Summary Table.

Interrupt Mask Register Selects mask states of the flags in [IRQFLAGS.*] that contribute to the **I2S_IRQ** event.

Table 22-25. IRQMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	XCNTCPT	R/W	0h	XCNTCPT interrupt mask 0: Disable 1: Enable
5	AIFDMAIN	R/W	0h	AIFDMAIN interrupt mask 0: Disable 1: Enable
4	AIFDMAOUT	R/W	0h	AIFDMAOUT interrupt mask 0: Disable 1: Enable
3	WCLKTOUT	R/W	0h	WCLKTOUT interrupt mask 0: Disable 1: Enable
2	BUSERR	R/W	0h	BUSERR interrupt mask 0: Disable 1: Enable
1	WCLKERR	R/W	0h	WCLKERR interrupt mask 0: Disable 1: Enable
0	PTRERR	R/W	0h	PTRERR interrupt mask. 0: Disable 1: Enable

22.10.24 IRQFLAGS Register (Offset = 74h) [Reset = 00000000h]

IRQFLAGS is shown in Table 22-26.

Return to the Summary Table.

Raw Interrupt Status Register

Table 22-26. IRQFLAGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	XCNTCPT	R	0h	Will be set when xcnt counter is captured either by events or software. Needs to be cleared by software.
5	AIFDMAIN	R	0h	Set when condition for this bit field event occurs (auto cleared when input pointer is updated - [AIFINPTRNEXT.*]), see description of [AIFINPTRNEXT.*] register for details.
4	AIFDMAOUT	R	0h	Set when condition for this bit field event occurs (auto cleared when output pointer is updated - [AIFOUTPTRNEXT.*]), see description of [AIFOUTPTRNEXT.*] register for details
3	WCLKTOUT	R	0h	Set when the sample stamp generator does not detect a positive **WCLK** edge for 65535 clk periods. This signalizes that the internal or external **BCLK** and **WCLK** generator source has been disabled. The bit is sticky and may only be cleared by software (by writing '1' to WCLKTOUT).
2	BUSERR	R	0h	Set when a **DMA** operation is not completed in time (that is audio output buffer underflow, or audio input buffer overflow). This error requires a complete restart since word synchronization has been lost. The bit is sticky and may only be cleared by software (by writing '1' to BUSERR). Note that DMA initiated transactions to illegal addresses will not trigger an interrupt. The response to such transactions is undefined. INTERNAL_NOTE: The I2S module is not monitoring the AHB bus error response, hence bus faults resulting from access to illegal addresses are not generated. It is best practice to detect and report such errors and, therefore, a ticket has been entered into the CDDS bug tracking database for the I2S module. The reference is CC26_I2S--BUG00011. All versions of CC13xx/CC26xx Chameleon and Lizard are impacted, and there is no plans to change this behavior.
1	WCLKERR	R	0h	Set when: - An unexpected **WCLK** edge occurs during the data delay period of a phase. Note unexpected **WCLK** edges during the word and idle periods of the phase are not detected. - In dual-phase mode, when two **WCLK** edges are less than 4 **BCLK** cycles apart. - In single-phase mode, when a **WCLK** pulse occurs before the last channel. This error requires a complete restart since word synchronization has been lost. The bit is sticky and may only be cleared by software (by writing '1' to WCLKERR).
0	PTRERR	R	0h	Set when [AIFINPTRNEXT.*] or [AIFOUTPTRNEXT.*] has not been loaded with the next block address in time. This error requires a complete restart since word synchronization has been lost. The bit is sticky and may only be cleared by software (by writing '1' to PTRERR).

22.10.25 IRQSET Register (Offset = 78h) [Reset = 00000000h]

IRQSET is shown in Table 22-27.

Return to the Summary Table.

Interrupt Set Register

Table 22-27. IRQSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	XCNTCPT	W	0h	1: Sets the interrupt of XCNTCPT (unless a auto clear criteria was given at the same time, in which the set will be ignored)
5	AIFDMAIN	W	0h	1: Sets the interrupt of AIFDMAIN (unless a auto clear criteria was given at the same time, in which the set will be ignored)
4	AIFDMAOUT	W	0h	1: Sets the interrupt of AIFDMAOUT (unless a auto clear criteria was given at the same time, in which the set will be ignored)
3	WCLKTOUT	W	0h	1: Sets the interrupt of WCLKTOUT
2	BUSERR	W	0h	1: Sets the interrupt of BUSERR
1	WCLKERR	W	0h	1: Sets the interrupt of WCLKERR
0	PTRERR	W	0h	1: Sets the interrupt of PTRERR

22.10.26 IRQCLR Register (Offset = 7Ch) [Reset = 00000000h]

IRQCLR is shown in Table 22-28.

Return to the Summary Table.

Interrupt Clear Register

Table 22-28. IRQCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	XCNTCPT	W	0h	1: Clears the interrupt of XCNTCPT (unless a set criteria was given at the same time in which the clear will be ignored)
5	AIFDMAIN	W	0h	1: Clears the interrupt of AIFDMAIN (unless a set criteria was given at the same time in which the clear will be ignored)
4	AIFDMAOUT	W	0h	1: Clears the interrupt of AIFDMAOUT (unless a set criteria was given at the same time in which the clear will be ignored)
3	WCLKTOUT	W	0h	1: Clears the interrupt of WCLKTOUT (unless a set criteria was given at the same time in which the clear will be ignored)
2	BUSERR	W	0h	1: Clears the interrupt of BUSERR (unless a set criteria was given at the same time in which the clear will be ignored)
1	WCLKERR	W	0h	1: Clears the interrupt of WCLKERR (unless a set criteria was given at the same time in which the clear will be ignored)
0	PTRERR	W	0h	1: Clears the interrupt of PTRERR (unless a set criteria was given at the same time in which the clear will be ignored)

22.10.27 AIFMCLKDIV Register (Offset = 80h) [Reset = 00000000h]

AIFMCLKDIV is shown in Table 22-29.

Return to the Summary Table.

MCLK Division Ratio

Table 22-29. AIFMCLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	MDIV	R/W	0h	An unsigned factor of the division ratio used to generate **MCLK** [2-1024]: **MCLK** = MCUCLK/MDIV[Hz] **MCUCLK** is upto 96MHz. A value of 0 is interpreted as 1024. A value of 1 is invalid. If MDIV is odd the low phase of the clock is one **MCUCLK** period longer than the high phase.

22.10.28 AIFBCLKDIV Register (Offset = 84h) [Reset = 00000000h]

AIFBCLKDIV is shown in Table 22-30.

Return to the Summary Table.

BCLK Division Ratio

Table 22-30. AIFBCLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	BDIV	R/W	0h	An unsigned factor of the division ratio used to generate **BCLK** [2-1024]: **BCLK** = MCUCLK/BDIV[Hz] **MCUCLK** can be upto 96MHz. A value of 0 is interpreted as 1024. A value of 1 is invalid. If BDIV is odd and [AIFCLKCTL.SMPL_ON_POSEDGE.*] = 0, the low phase of the clock is one **MCUCLK** period longer than the high phase. If BDIV is odd and [AIFCLKCTL.SMPL_ON_POSEDGE.*] = 1 , the high phase of the clock is one **MCUCLK** period longer than the low phase.

22.10.29 AIFWCLKDIV Register (Offset = 88h) [Reset = 00000000h]

AIFWCLKDIV is shown in Table 22-31.

Return to the Summary Table.

WCLK Division Ratio

Table 22-31. AIFWCLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	WDIV	R/W	0h	If WCLKPHASE = 0, Single phase. **WCLK** is high one **BCLK** period and low WDIV[9:0] (unsigned, [1-1023]) **BCLK** periods. **WCLK** = **MCUCLK** / BDIV*(WDIV[9:0] + 1) [Hz] **MCUCLK** upto 96MHz. If WCLKPHASE = 1, Dual phase. Each phase on **WCLK** (50% duty cycle) is WDIV[9:0] (unsigned, [1-1023]) **BCLK** periods. **WCLK **= **MCUCLK **/ BDIV*(2*WDIV[9:0]) [Hz] If WCLKPHASE = 2, User defined. **WCLK** is high WDIV[7:0] (unsigned, [1-255]) **BCLK** periods and low WDIV[15:8] (unsigned, [1-255]) **BCLK** periods. **WCLK** = **MCUCLK **/ (BDIV*(WDIV[7:0] + WDIV[15:8]) [Hz]

22.10.30 AIFCLKCTL Register (Offset = 8Ch) [Reset = 00000000h]

AIFCLKCTL is shown in Table 22-32.

Return to the Summary Table.

Internal Audio Clock Control

Table 22-32. AIFCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	MEN	R/W	0h	0: **MCLK** geneartion disabled, 1: **MCLK** generation enabled
2-1	WCLKPHASE	R/W	0h	Decides how the WCLK division ratio is calculated and used to generate different duty cycles (See WDIV).
0	WBEN	R/W	0h	0: WCLK/BCLK geneartion disabled, 1: WCLK/BCLK generation enabled

22.10.31 CLKCFG Register (Offset = 1000h) [Reset = 00000000h]

CLKCFG is shown in Table 22-33.

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Audio clock source selection and **I2S** enable register Note: Disable the [CLKCFG.MEM_CLK_EN] and [CLKCFG.ADFS_EN] to change CLKSEL After changing CLKSEL, enable [CLKCFG.ADFS_EN] followed by [CLKCFG.MEM_CLK_EN]

Table 22-33. CLKCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	ADFSEN	R/W	0h	ADFS enable field
6-4	CLKSEL	R/W	0h	Audio clock selection 0h = No Clock 1h = SOC Clock(80MHz) 2h = SOC PLL Clock(un-swallowed 80MHz) 3h = HFXT
3-1	RESERVED	R	0h	Reserved
0	EN	R/W	0h	0: **I2S** clock disabled 1: **I2S** clock enabled

22.10.32 ADFSCTRL1 Register (Offset = 1004h) [Reset = 00000000h]

ADFSCTRL1 is shown in Table 22-34.

Return to the Summary Table.

ADFS TREF control register

Table 22-34. ADFSCTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20-0	TREF	R/W	0h	TREF value for ADFS

22.10.33 ADFSCTRL2 Register (Offset = 1008h) [Reset = 00000000h]

ADFSCTRL2 is shown in Table 22-35.

Return to the Summary Table.

ADFS general configuration register

Table 22-35. ADFSCTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-20	DIV	R/W	0h	ADFS div value field
19-18	RESERVED	R	0h	Reserved
17	DELTASIGN	R/W	0h	ADFS delta sign field
16-0	DELTA	R/W	0h	ADFS delta value field

Chapter 23

Pulse Density Modulation (PDM)

This chapter describes the Pulse Density Modulation (PDM) module.

23.1 Introduction

The Pulse Density Modulation (PDM) module handles data streams from PDM microphones. The input data is decimated and converted to PCM format with a configurable sinc filter. Data is made available in various formats, sample rates and bit-widths.

Features

- 2 PDM channels
- 1 PDM clock output and 2 PDM data input pins
- Support for operation with single mono, dual mono or stereo mic arrangements
- Selectable sampling rate
  - Minimum 8kHz
  - Common 16kHz
  - Maximum 48kHz
- Configurable sinc-filter order
  - 1 to 4
- Configurable oversampling ratio
  - 2 to 256
- Independent configurable clock sources per data line
  - HFXT
  - SOC PLL CLK
- Independent FIFO for each PDM channel
- Support for FIFO data access in 8-bit, 16-bit and 32-bit modes
- Supported input formats
  - PDM
  - Manchester-encoded
- Supported storage formats
  - Right/left aligned
  - Bipolar offset-binary
  - 2’s-complement
- Support for operation with Host DMA
- Availability of sample stamp generator
- AGC accelerator for calculation of signal average value, average power and peak values

23.2 Block Diagram

The high level block diagram of the PDM module is shown in the figure below.

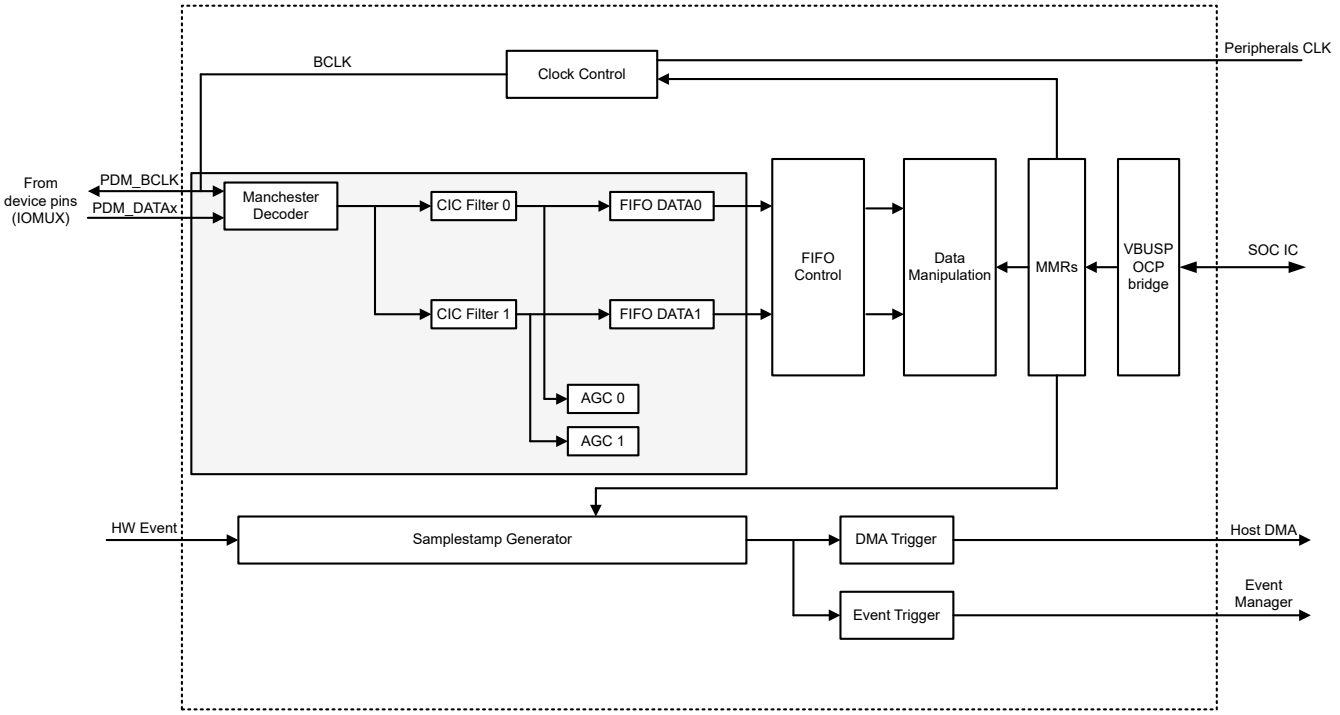

Figure 23-1. PDM Block Diagram

23.3 Input Selection

Digital microphones produce a PDM output that can be fed into the decimation filter. Up to two microphones may be attached to each PDM data line (one per channel). Two microphones can share a clock and data line, with data transmitted on either the low (channel 1) or high (channel 2) clock phase. Typical connection and protocol diagrams are provided.

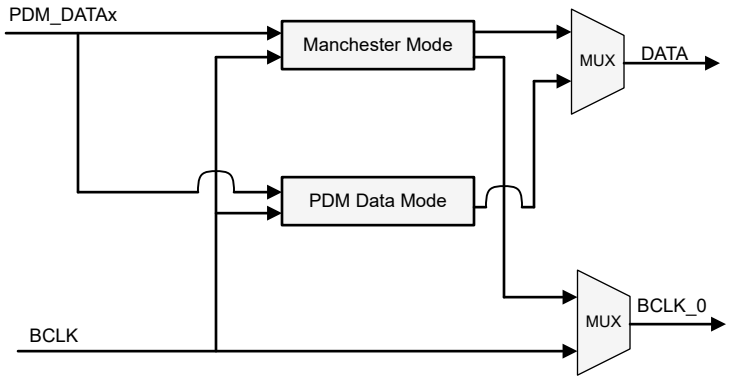

Figure 23-2. PDM Input Selection

23.3.1 PDM Data Mode

In PDM Data Mode, data is sampled on the BCLK internally. BCLK is also sent out for the digital mic to send the data in. Half cycle latency is allowed between BCLK and Rx data. Rx data should meet setup/hold requirement of half cycle for the BCLK round trip.

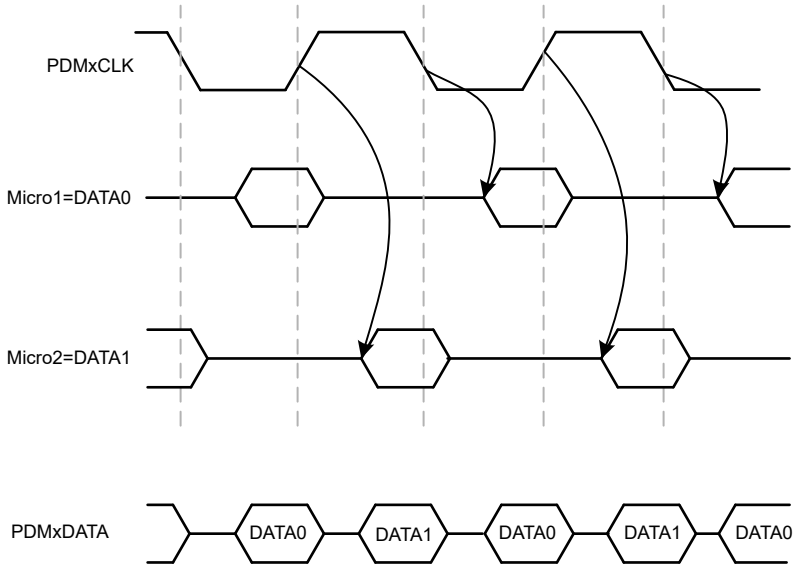

Figure 23-3. PDM Data Mode

23.3.2 Manchester Input Mode

The PDM module can accept a Manchester-encoded bitstream. The format is selected using PDM.CCTL register. The decoder requires a zero-to-one or one-to-zero transition to lock.

In Manchester Input Mode, the oversampling ratio is fixed at 16 and the input data will be synchronized. The first transition could be ignored due to synchronization overhead and on the following transition/second transition, counter is started to count pulses between samples and total samples. Counter on every new sample should be between a fixed window. A variable window can be designed to accommodate initial variations and reduce window size as sample count goes up. Initial sequence is planned to be back to back opposite values. After “X” transitions if the window is not violated, status is issued and data decoding starts. Till then output data and clock are 0. A new sample triggers clock edge and another new sample within window limit or 3/4th clock pulse width would result in edge switch. The window comparison is done during clock generation and the Data_out is same as Data_in, according to IEEE standard.

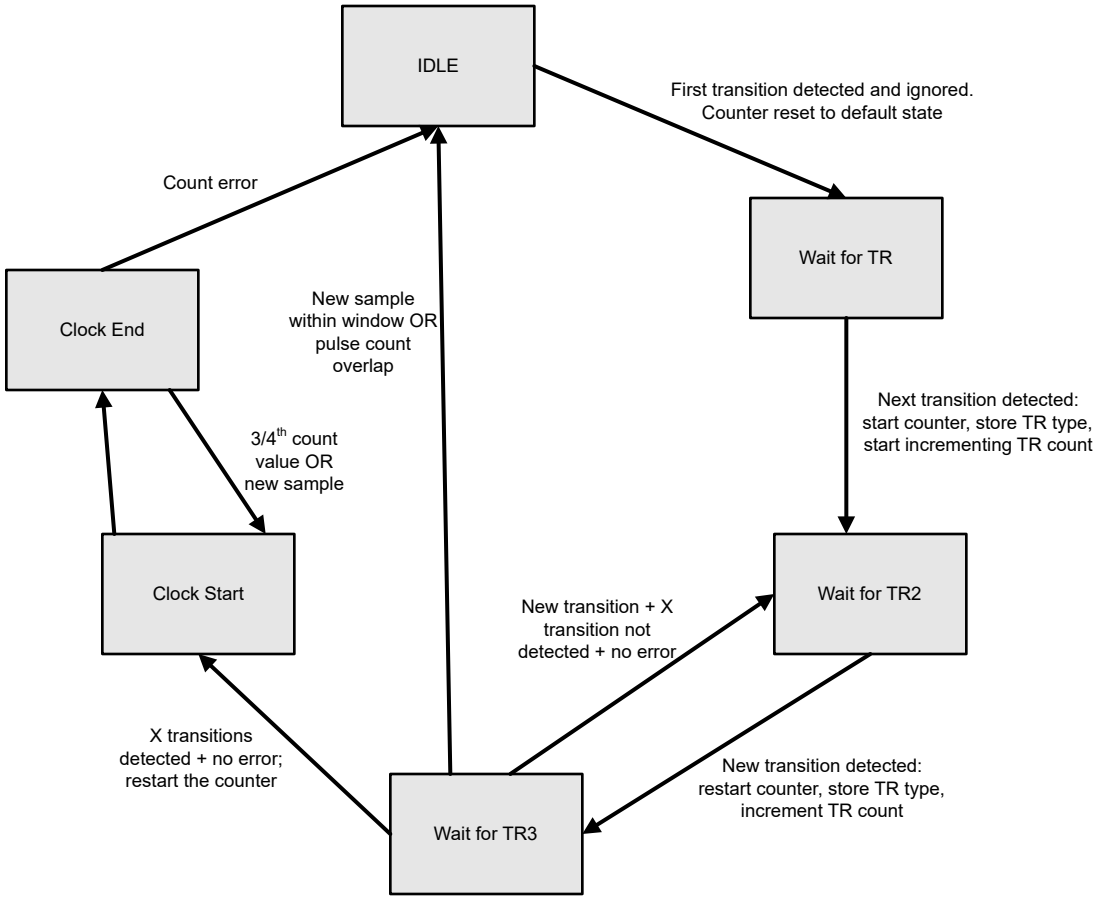

Figure 23-4. Manchester Input Mode

23.4 CIC Filter

Each PDM channel has its own Cascaded Integrator-Comb (CIC) filter, a digital filter that decimates the digital bit stream. The filter accepts the one-bit-input-signal stream to get a down-sampled output signal with an increased data width. It is designed with 32 bits for accumulators and differentiators to nullify rounding effects and accommodate bit growth. For signed operation, output is 25 bits with 24 bits of data and 25th bit as sign. Data is right shifted to FIFO. Based on configuration, input bit stream is decoded as +1/-1 or 1/0 and based on the filter order, appropriate accumulators and differentiators are chosen to output the correct filter value. Over sampling ratio is used to build up the accumulator value before applying them to differentiators. FIFO write happens on the clock divided by over sampling ratio and 24 bits will be written.

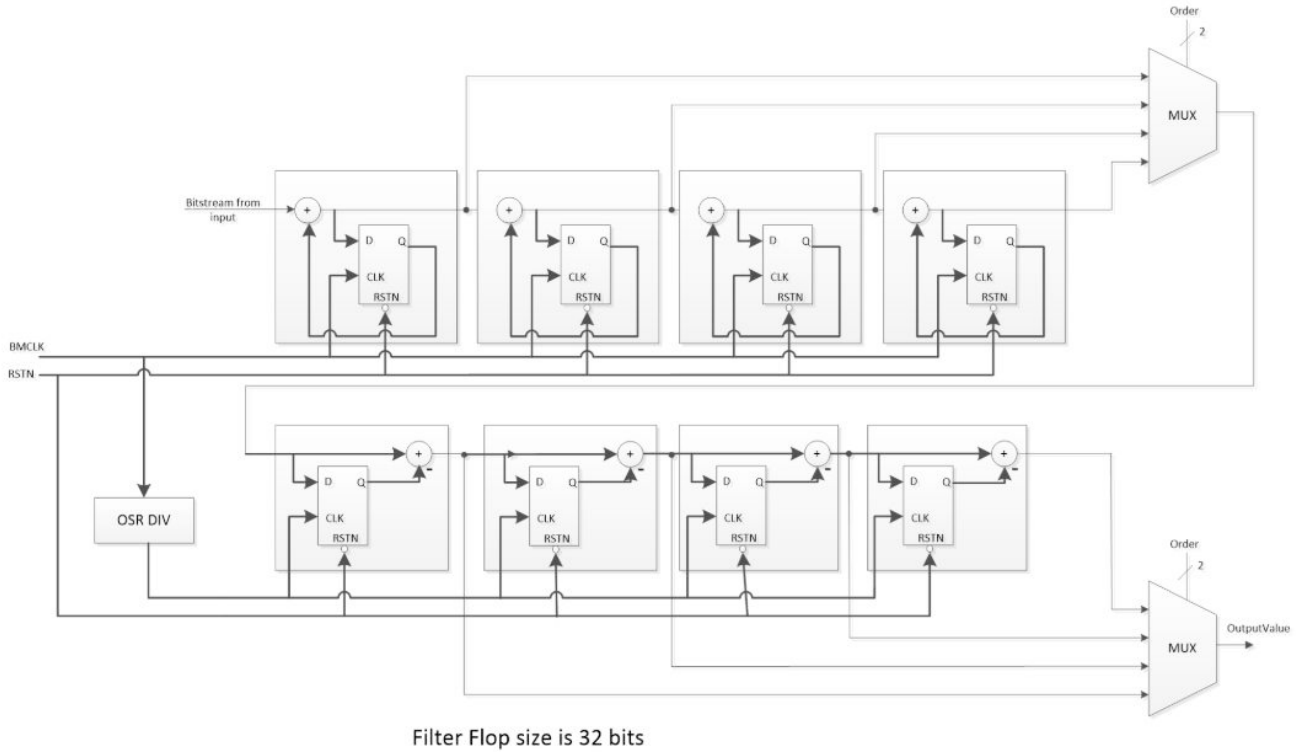

Figure 23-5. CIC Filter

23.4.1 Filter Design

The input filter is designed as CIC filter with the below transfer function:

$$H(z) = \left[\frac{1}{OSR}\left(1 - z^{-OSR}\right)/\left(1 - \frac{1}{z}\right)\right]^{X} \quad (13)$$

$$H(f) = \left[sinc\left(OSR \times \pi \times \frac{f}{f_B}\right)/sinc\left(\pi \times \frac{f}{f_B}\right)\right]^{X} = \left[\frac{1}{OSR} \times sin\left(OSR \times \pi \times \frac{f}{f_B}\right)/\ sin\left(\pi \times \frac{f}{f_B}\right)\right]^{X} \quad (14)$$

where:

X = Selected number of filter stage

f = frequency of the input signal at the microphone

f_B= the bit clock frequency (BCLK), clock at PDMxCLK pin

f_S = the sample frequency (SCLK), $f_B = f_s * OSR$

OSR = Oversampling rate, the ratio of the bit clock frequency f_B to the sample frequency f_S.

F_S = full scale variable output

The digital filter for each channel completes the decimation of the digital bit stream and outputs a new conversion result to the corresponding PDMx.DATAx register at the sample frequency f_S.

23.4.2 Digital Filter Output

The full-scale value output F_S by the SINC ^{X} digital filter is dependent on the oversampling ratio OSR and is given by:

$$F_S = 2^{x\log_2 OSR} \quad (15)$$

Table 23-1. Number of data bits depending on filter order and OSR

OSR	Sinc filter order			
	1	2	3	4
4	2	4	6	8
8	3	6	9	12
32	5	10	15	20
64	6	12	18	24
128	7	14	21	Not Applicable
256	6	16	24	Not Applicable

For example, the OSR of 256 with a SINC filter order of 3 results in a full-scale value of 224 or 100:0000h; that is, a value that can be represented by 24 bits. All 24 bits can be accessed using the PDMx.DATAx registers. Depending on the selected data format and alignment, the representation within the PDMx.DATAx registers differs.

With mapping the filter output into the FIFO access mode of 8, 16 and 24 Bits the below max OSR and Filter Order should be selected for the corresponding access mode.

Table 23-2. Max OSR with filter order and data size

Data Size [bits]	Data Format: Offset				Data Format: Two's-complement			
	Order				Order			
	1	2	3	4	1	2	3	4
8	256	16	6	4	128	11	5	3
16	256	256	40	16	256	181	32	13
24	256	256	256	64	256	256	203	53

Filter should be implemented with 32 bit registers for accumulators and differentiators to increase the accuracy during calculation and to avoid losing bits with rounding effects.

23.4.3 Offset Binary Mode

In offset binary mode (PDMx.CCTL.DATAFORMAT = 0b), the full-scale range is from 0 to F_S. The bitstream coming from the input is interpreted as a stream of ones (1) and zeros (0).

23.4.4 Twos-Complement Mode

In twos-complement mode (PDMx.CCTL.DATAFORMAT = 1b), the full-scale range is from $-F_S$ to $+F_S$. The bitstream input is interpreted as ones (1) and minus ones (-1).

23.5 FIFO Organization in Different Modes

23.5.1 Single Mono Microphone Configuration

In this configuration only one channel is used and the FIFO from both channels are concatenated to make it work as a single logical FIFO. Up to four 16-bit or 24-bit samples can be stored or up to twelve 8-bit samples can be stored in the FIFOs in this mode of operation. FIFO threshold setting shall consider concatenated total size of the FIFO and sample size. Data generated by CIC filter is written first to channel-0 FIFO locations based on the sample size followed by channel-1 FIFO locations. When FIFODATA register is read by CPU or DMA, the data is first provided from channel-0 FIFO followed by channel-1 FIFO.

23.5.1.1 24-bit Sample Size

23.5.1.1.1 32-bit Data Read

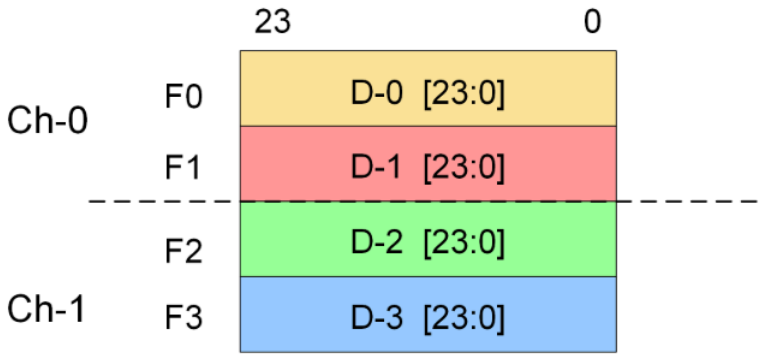

Figure 23-6. Single Mono Configuration, 24-bit Sample Size

Consider offset binary data format and right justified data alignment. In this configuration when FIFODATA is read, PDM pads 0 for bits 31 to 24 and data[23:0] is taken from the FIFO. The data is returned from FIFO in this order for reads from FIFODATA register.

23.5.1.2 16-bit Sample Size

23.5.1.2.1 32-bit Data Read

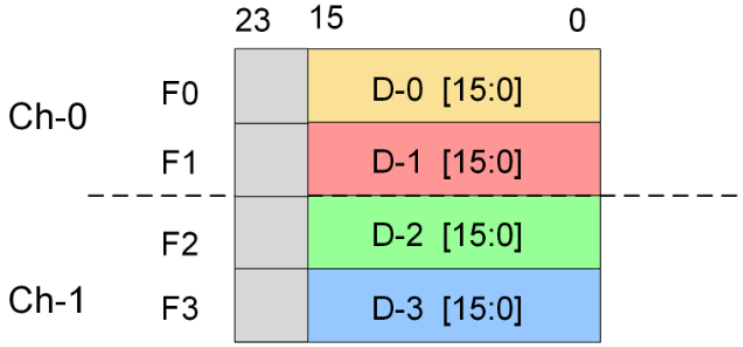

Figure 23-7. Single Mono Configuration, 16-bit Sample Size

In this configuration when FIFODATA is read, PDM compacts two 16-bit samples from FIFO to provide 32-bit data to host. The data is returned from FIFO in this order for reads from FIFODATA register.

23.5.1.2.2 16-bit Data Read

In this configuration when FIFODATA is read, PDM provides data[15:0] from the FIFO. The data is returned from FIFO in this order for reads from FIFODATA register.

23.5.1.3 8-bit Sample Size

23.5.1.3.1 32-bit Data Read

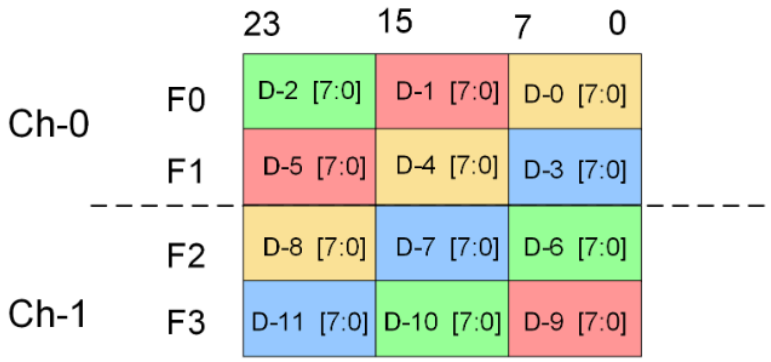

Figure 23-8. Single Mono Configuration, 8-bit Sample Size

In this configuration when FIFODATA is read, PDM compacts four 8-bit samples from FIFO to provide 32-bit data to host. The data is returned from FIFO in this order for reads from FIFODATA register.

23.5.1.3.2 16-bit Data Read

In this configuration when FIFODATA is read, PDM compacts two 8-bit samples from FIFO to provide 16-bit data to host. The data is returned from FIFO in this order for reads from FIFODATA register.

23.5.1.3.3 8-bit Data Read

In this configuration when FIFODATA is read, PDM provides data[7:0] from the FIFO. The data is returned from FIFO in this order for reads from FIFODATA register.

23.5.2 Stereo or Dual Mono Microphone Configuration

In this configuration both channel-0 and channel-1 are used and the data is simultaneously written into channel-0 and channel-1 FIFOs from the respective filters. Up to two 16-bit or 24-bit samples can be stored or up to six 8-bit samples can be stored in the FIFOs in this mode of operation. FIFO threshold setting shall consider the size of single channel FIFO and sample size. When the FIFODATA register is read by CPU or DMA, the data is returned from channel-0 FIFO and channel-1 FIFO alternatively.

23.5.2.1 24-bit Sample Size

23.5.2.1.1 32-bit Data Read

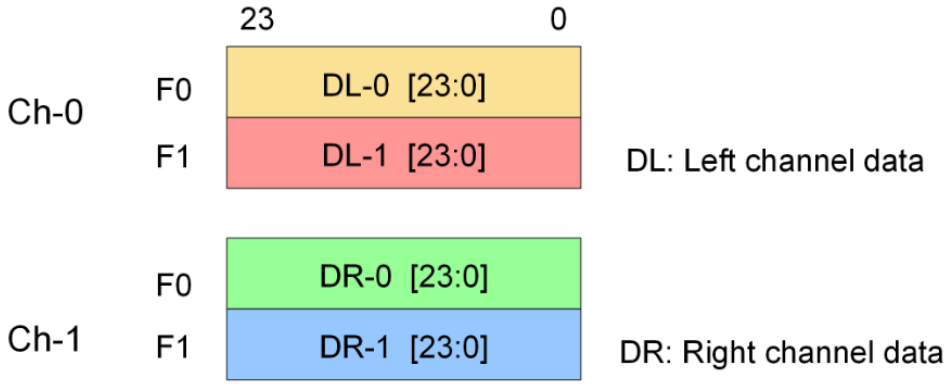

Figure 23-9. Stereo/Dual Mono Configuration, 24-bit Sample Size

Consider offset binary data format and right justified data alignment. In this configuration when FIFODATA is read, PDM pads 0 for bits 31 to 24 and data[23:0] is taken from the FIFO. The data is returned from channel FIFOs in this order for reads from FIFODATA register.

FIFO Read is done in the following order:

1. DL-0[23:0]
2. DR-0[23:0]
3. DL-1[23:0]
4. DR-1[23:0]

23.5.2.2 16-bit Sample Size

23.5.2.2.1 32-bit Data Read

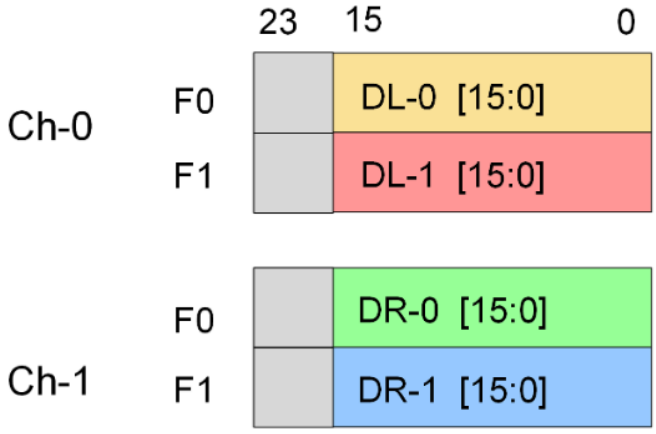

Figure 23-10. Stereo/Dual Mono Configuration, 16-bit Sample Size

In this configuration when FIFODATA is read, PDM compacts two 16-bit samples from FIFO to provide 32-bit data to host. The data is returned from channel FIFOs in this order for reads from FIFODATA register.

FIFO Read is done in the following order:

1. {MSB: DR-0[15:0], LSB: DL-0[15:0]}
2. {MSB: DR-1[15:0], LSB: DL-1[15:0]}

23.5.2.2.2 16-bit Data Read

In this configuration when FIFODATA is read, PDM provides data[15:0] from the FIFO. The data is returned from channel FIFOs in this order for reads from FIFODATA register.

FIFO Read is done in the following order:

1. DL-0[23:0]
2. DR-0[23:0]
3. DL-1[23:0]
4. DR-1[23:0]

23.5.2.3 8-bit Sample Size

23.5.2.3.1 32-bit Data Read

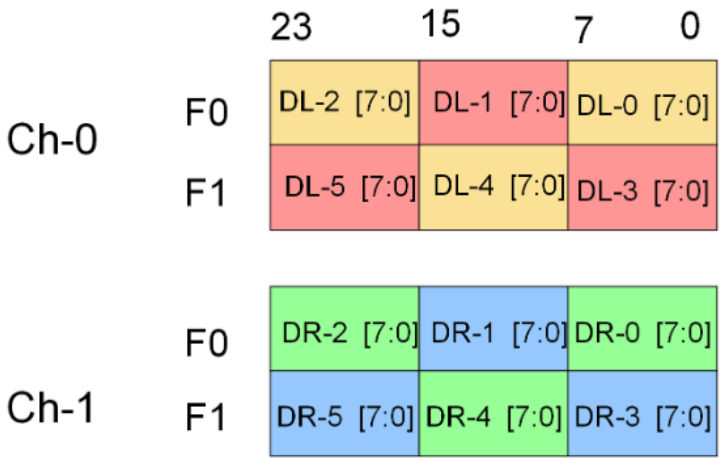

Figure 23-11. Stereo/Dual Mono Configuration, 8-bit Sample Size

In this configuration when FIFODATA is read, PDM compacts four 8-bit samples from FIFO to provide 32-bit data to host. The data is returned from channel FIFOs in this order for reads from FIFODATA register.

FIFO Read is done in the following order:

1. {DL-3[7:0], DL-2[7:0], DL-1[7:0], DL-0[7:0]}
2. {DR-3[7:0], DR-2[7:0], DR-1[7:0], DR-0[7:0]}
3. {DL-1[7:0], DL-0[7:0], DL-5[7:0], DL-4[7:0]}
4. {DR-1[7:0], DR-0[7:0], DR-5[7:0], DR-4[7:0]}
5. {DL-5[7:0], DL-4[7:0], DL-3[7:0], DL-2[7:0]}
6. {DR-5[7:0], DR-4[7:0], DR-3[7:0], DR-2[7:0]}

23.5.2.3.2 16-bit Data Read

In this configuration when FIFODATA is read, PDM compacts two 8-bit samples from FIFO to provide 16-bit data to host. The data is returned from channel FIFOs in this order for reads from FIFODATA register.

FIFO Read is done in the following order:

1. {MSB: DL-1[7:0], LSB: DL-0[7:0]}
2. {MSB: DR-1[7:0], LSB: DR-0[7:0]}
3. {MSB: DL-3[7:0], LSB: DL-2[7:0]}
4. {MSB: DR-3[7:0], LSB: DR-2[7:0]}
5. {MSB: DL-5[7:0], LSB: DL-4[7:0]}
6. {MSB: DR-5[7:0], LSB: DR-4[7:0]}

23.5.2.3.3 8-bit Data Read

In this configuration when FIFODATA is read, PDM provides data[7:0] from the FIFO. The data is returned from channel FIFOs in this order for reads from FIFODATA register.

FIFO Read is done in the following order:

1. DL-0[7:0]
2. DR-0[7:0]
3. DL-1[7:0]
4. DR-1[7:0]
5. DL-2[7:0]
6. DR-2[7:0]

7. DL-3[7:0]
8. DR-3[7:0]
9. DL-4[7:0]
10. DR-4[7:0]
11. DL-5[7:0]
12. DR-5[7:0]

23.5.3 FIFO Threshold Setting

PDM channel FIFOs are organized as 2x24-bit. It can store variable number of samples depending on sample size and configuration of PDM for single mono, dual mono or stereo operations. DMA trigger or CPU interrupt is generated based on FIFO threshold setting. The value of FIFO threshold has different meaning depending on the number of samples that can be stored in the PDM channel FIFOs.

In the case of single mono configuration with 8-bit sample size, both FIFOs are combined to provide 12 entries in the FIFO. Valid threshold values are from 0 to 11. When threshold is set to 0, event is generated once first element is filled in the FIFO. When threshold is set to 11, event is generated when all 12 elements are filled in the FIFO.

In the case of single mono configuration with 16-bit or 24-bit sample size, both FIFOs are combined to provide 4 entries in the FIFO.. Valid threshold values are from 0 to 3. When threshold is set to 0, event is generated once first element is filled in the FIFO. When threshold is set to 3, event is generated when all 4 elements are filled in the FIFO.

In the case of dual mono or stereo configuration with 8-bit sample size, both channel FIFOs operate independently and each channel FIFO provide 6 entries to store the samples. Valid threshold values are from 0 to 5. When threshold is set to 0, event is generated once first element is filled in the FIFO. When threshold is set to 5, event is generated when all 6 elements are filled in the FIFO.

In the case of dual mono or stereo configuration with 16-bit or 24-bit sample size, both channel FIFOs operate independently and each channel FIFO provide 2 entries to store the samples. Valid threshold values are 0 and 1. When threshold is set to 0, event is generated once first element is filled in the FIFO. When threshold is set to 1, event is generated when both the elements are filled in the FIFO.

23.5.4 Reset FIFO

The FIFO can be cleared by writing 1 to FIFOCTL.FIFOFLUSH (which reads back 0 after one cycle). When the PDM is reset, the FIFO must also be cleared.

23.6 Automatic Gain Control (AGC)

PDM has an Automatic Gain Control (AGC) accelerator block on each of the two channels to calculate the average value, peak value and average power of the samples. The data from CIC filter shall be routed to the AGC accelerator to generate the above values that are available for software to analyze signal clipping or adjust the signal gain in the feed forward or feedback paths using software AGC routines. The AGC accelerator shall implement first order IIR filter (leaky integrator) for moving average calculation of samples generated by CIC filter and the average value shall be stored in a register for software use. The internal storage in the averaging block shall be 34-bits out of which 32-bits shall be mapped to register for CPU read out and MSB 24-bits shall be used for internal computations for peak value calculation.

For sample peak value calculation, each sample output from CIC filter is subtracted from the moving average value and the absolute value of the difference is generated. This absolute value is then compared against the previously stored peak value and the new value is stored if it is greater than the previously stored peak value. The peak value is stored in a register that is made available for software use. The peak value register is reset when software reads the peak value register and the new peak value is then computed from the next sample. There is an enable bit for peak value detector which when set enables sample averaging and peak value calculations. For 2's complement format, the output from absolute difference calculation block is 23-bits and the result stored in peak sample value register is 23-bits. For offset binary format, the output from absolute difference calculation block is 24-bits and the result stored in peak sample value register is 24-bits.

A First order IIR filter (leaky integrator) calculates the moving average of sample power. The squared value of the sample is 48-bit out of which only MSB 24-bits are presented to the sample power averaging block. The averaging block has a 34-bit internal storage for accumulation of sample power values out of which 32-bits are mapped to average sample power register for CPU read out. The scaling factor alpha is programmable by software to one of the pre-defined values (1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, 1/1024) and the selected scaling factor is applied to leaky integrators of both sample average and sample average power calculation blocks. The power accumulator and average power register resets when software reads average power register and operation of power accumulation restarts from that time. There is an enable bit for sample average power calculation block which when set enables sample average power calculations.

23.6.1 Operation in 2's Complement Format

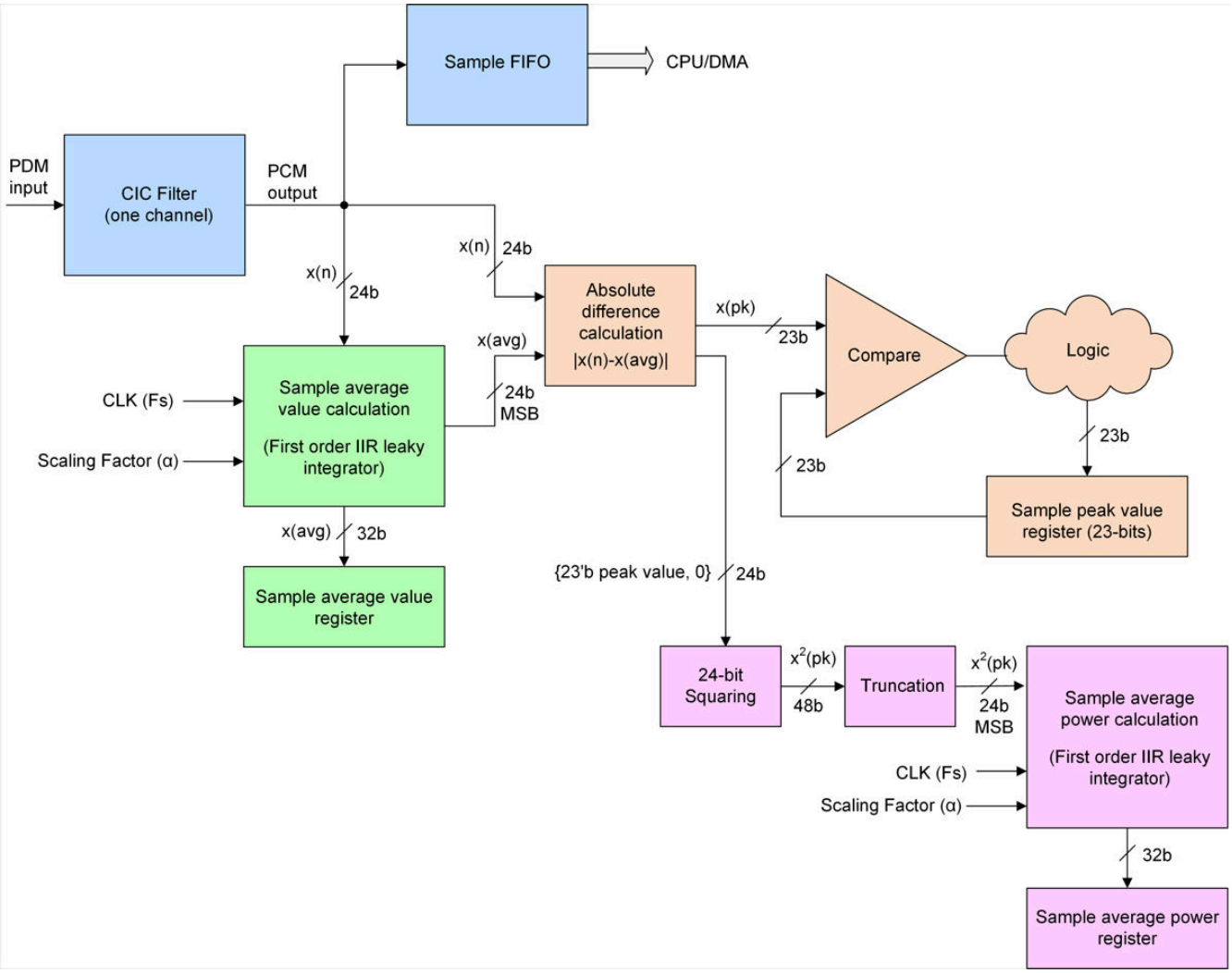

Figure 23-12. 2's Complement Format

23.6.2 Operation in Offset Binary Format

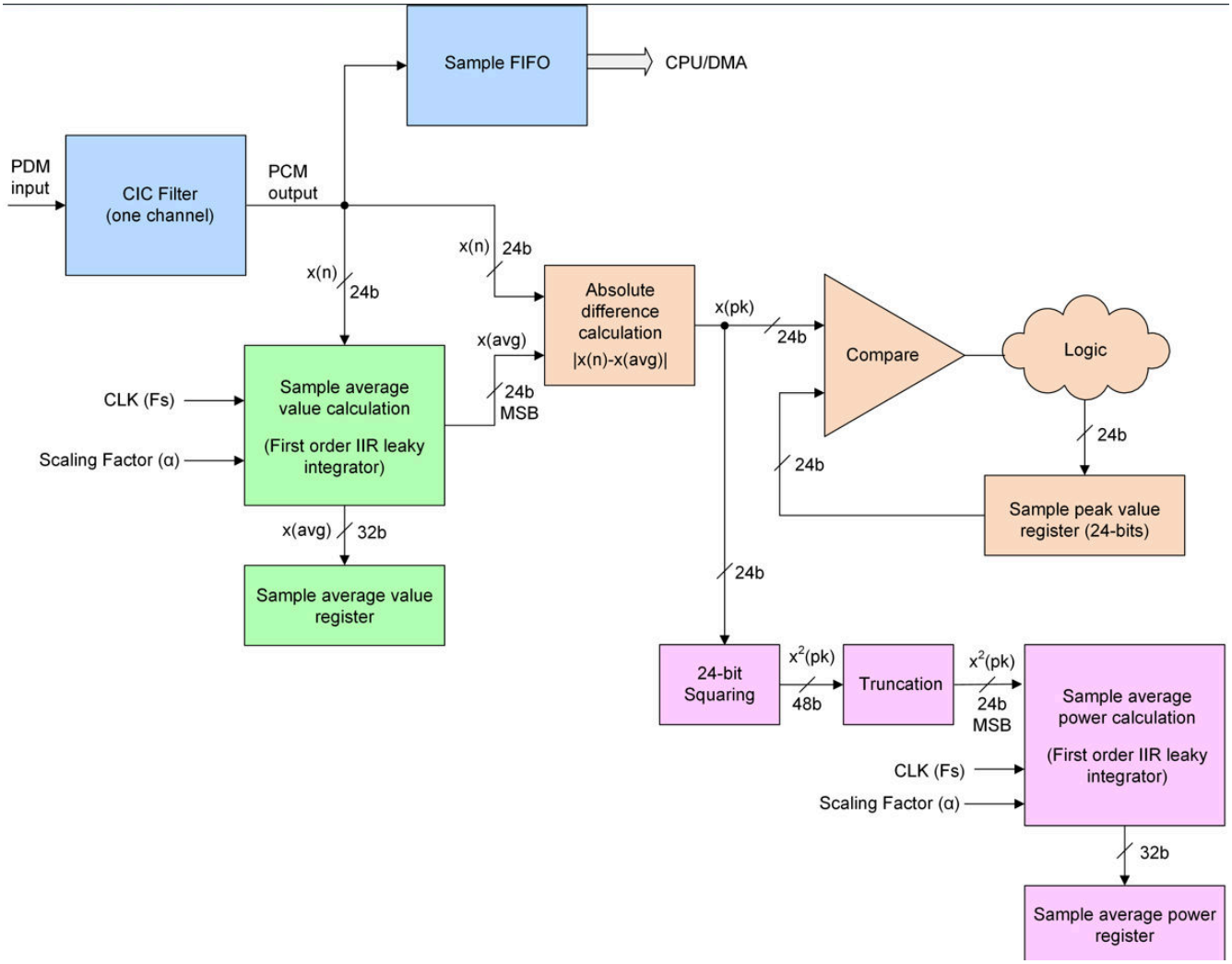

Figure 23-13. Offset Binary Format

23.7 Interrupts

The PDM can generate two interrupts: overflow and underflow. The interrupt is shared by both channels.

23.8 Clock Select and Control

Clock sources for PDM are SOC CLK, SOC PLL CLK, or HFXT oscillator clock. Internal audio clocks may suffer from jitter, limited divisor options, or inability to maintain constant latency; using the HFXT clock reduces jitter.

Internal audio clock selection: CLKCFG[6:4] CLKSEL =

0h = No Clock

1h = SOC Clock

2h = SOC PLL Clock

3h = HFXT

The output PDM_BCLK can be configured using INCLKCTL.

23.9 DMA Operation

The PDM can trigger DMA to move data from the receive FIFO. DMA reads the FIFODATA register; the FIFOCTL0 register maps specific FIFOs to FIFODATA. FIFO-mapped channels for DMA must not be accessed via the CPU PDMx.DATAy registers. Data registers are offset-aligned so that a single DMA trigger can move data from multiple synchronized channels.

23.10 Samplestamp Generator

The samplestamp generator is used to start input and output DMA operation. The samplestamp generator is also used to synchronize PDM modules over a wireless network, so correct and fixed audio latency can be achieved. Synchronization over a wireless network is an optional feature that can be bypassed.

The samplestamp generator is enabled and is running while PDM:STPCTL.STP_EN = 1. Counter and capture registers are reset when software writes PDM:STPCTL.STP_EN = 0.

The below block diagram below shows as the the samplestamp generator:

- The lower part of the diagram is related to start-up of input and output DMA.
- The upper part of the diagram is related to RFCORE event capture for PDM module synchronization.

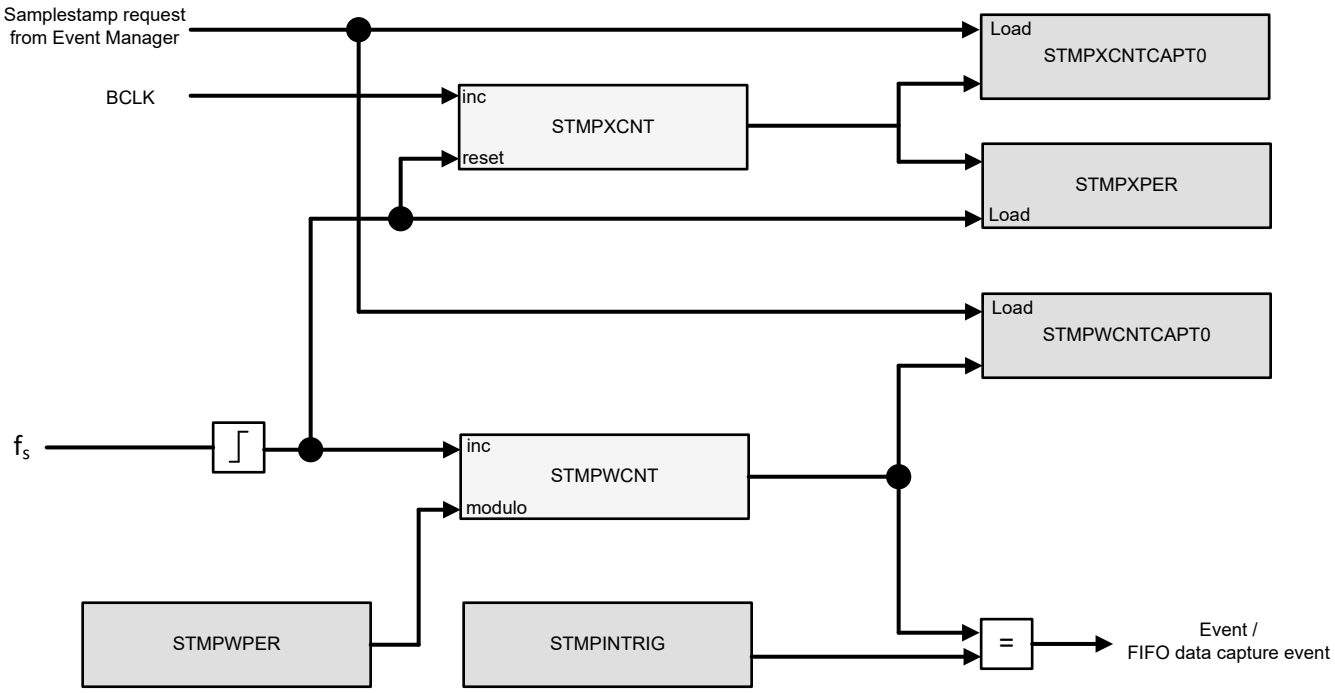

Figure 23-14. Samplestamp Generator

23.10.1 Samplestamp Counters

The samplestamp generator counts frames (Sample Clock periods) and REF clock cycles (crystal oscillator periods) within each frame.

- PDM:STPWCNT increments at the first Sample edge of each frame, module the period value PDM:STPWPER
- PDM:STPXCNT resets to 0 at the first Sample edge of each frame, and then increments by 1 for each REF clock cycle.

Reading PDM:STPWCNT latches the read value of PDM:STPXCNT. Software can modify the value of PDM:STPWCNT by writing an absolute value to PDM:STPWSET or a relative value to PDM:STPWADD.

23.10.2 Start-Up Triggers

The PDM:STPINTRIG and PDM:STPOUTTRIG registers contain PDM:STPWCNT compare values that are used to start the input and output DMA, respectively:

- When PDM:STPWCNT equals PDM:STPINTRIG, the input DMA begins storing sample words to memory in the next frame: (PDM:STPINTRIG + 1) % PDM:STPWPER
- When PDM:STPWCNT equals PDM:STPOUTTRIG, the output DMA begins outputting sample words from memory in the next frame: (PDM:STPOUTTRIG + 1) % PDM:STPWPER

To avoid false start-up triggers, PDM:STPINTRIG and PDM:STPOUTTRIG must initially be equal to or higher than PDM:STPWPER.

The PDM:STPCTL.IN_RDY and PDM:STPCTL.OUT_RDY status bits are set when the input and output.

DMA are ready to be started and cleared when DMA start triggers have occurred.

23.10.3 Samplestamp Capture

A capture request signal can be routed from RFCORE to trigger samplestamp capture. The EVENT:PDMSTPSEL0 register selects the RFCORE signal to be used. Whenever this capture request signal is high:

- The current value of PDM:STPXCNT is copied into PDM:STPXCNTCAPT.
- The current value of PDM:STPWCNT is copied into PDM:STPWCNTCAPT.

Also, on the first WCLK edge of each frame, the current value of PDM:STPXCNT is captured in PDM:STPXPER, and PDM:STPXCNT then restarts counting from 0.

Using these values, a fixed-point samplestamp value can be calculated:

PDM:STPWCNTCAPT0 + (PDM:STPXCNTCAPT0 / PDM:STPXPER)

Notice that the value of PDM:STPXPER will not normally be captured at the same time as the other values. Therefore, PDM:STPXPER can be less than PDM:STPXCNTCAPT.

23.10.4 Achieving Constant Audio Latency

The following actions can be taken to achieve the same constant audio latency in either direction over a wireless network (from the PDM pins on one CC35xx device platform to the PDM pins on another CC35xx device platform):

- One node must be defined as audio clock controller and the other node must be defined as audio clock peripheral. The peripheral must use an external audio clock source with adjustable rate.
- For both nodes, set PDM:STPWPER = N × (PDM:FIFOCTL2.TRGLVL), where N is a whole number.
  - The value of PDM:STPWPER equals audio latency in number of frames.
  - The value of PDM:STPWPER also equals the memory buffer size in number of samples.
- Perform samplestamp capture on the controller when it transmits the RF packet synchronization word, and include the value of the fixed-point samplestamp in the transmitted packet.
- Perform samplestamp capture on the peripheral when it receives the RF packet synchronization word, and store the samplestamp value of the master in the RF packet. Calculate the difference between the samplestamp values of the controller and peripheral, which is used to:
  - Initially offset the PDM:STPWCNT counter of the peripheral so that it matches the samplestamp value of the master.
  - While running, adjust the external audio clock source rate so that the difference between the samplestamp values of the peripheral and the controller approach 0.
- For both nodes, set up DMA pointers and DMA start triggers so that the value of STPWCNT represents the input and output buffer positions of the current frame on the ADx pins.

23.11 Debug-Mode Flag Behavior

When the device is in debug halt mode, status flags and FIFO pointers are not automatically updated/cleared on reads. The PDBGCTL register configures whether the module continues operation (FREE = 1) or stops immediately (FREE = 0) when DEBUG STOP is asserted.

23.12 Software Guidelines

Configuration of the PDM IP must be done while the module is inactive (PDMCTL.ENPDMx = 0). Configurable fields are in CHCTL MMR. OSR and ADFSCTLx should also be configured. Use INCLKCTL as source for Manchester recovery, set its frequency to 16 × the external clock, send at least 16 alternating samples at start.

23.13 PDM Registers

Table 23-3 lists the memory-mapped registers for the PDM registers. All register offset addresses not listed in Table 23-3 should be considered as reserved locations and the register contents should not be modified.

Table 23-3. PDM Registers

Offset	Acronym	Register Name	Section
0h	DESC	Module Identity	Section 23.13.1
4h	DESCEX	Module Configuration Details	Section 23.13.2
44h	IMASK	Interrupt Mask	Section 23.13.3
48h	RIS	Unmasked Interrupt Status	Section 23.13.4
4Ch	MIS	Masked Interrupt Status	Section 23.13.5
50h	ISET	Interrupt Set	Section 23.13.6
54h	ICLR	Interrupt clear	Section 23.13.7
60h	EMU	Debug Control	Section 23.13.8
100h	CTL	PDM Control	Section 23.13.9
104h	ICLKCTL	Input Clock Control	Section 23.13.10
108h	FIFOCTL1	FIFO Control 1	Section 23.13.11
10Ch	FIFODATA	FIFO Data	Section 23.13.12
110h	CCTL	Channel Control	Section 23.13.13
114h	OSR	Oversampling Control	Section 23.13.14
118h	STA	Status Register	Section 23.13.15
120h	FIFOCTL2	FIFO Control	Section 23.13.16
124h	FIFOSR	FIFO Status	Section 23.13.17
200h	AVGVAL0	Channel 0 Average	Section 23.13.18
204h	PKVAL0	Peak sample value for channel-0	Section 23.13.19
208h	AVGPOW0	Average Power Measurement	Section 23.13.20
20Ch	AVGVAL1	Channel-1 Average Value	Section 23.13.21
210h	PKVAL1	Peak Value	Section 23.13.22
214h	AVGPOW1	Channel 1 Power	Section 23.13.23
300h	STPCTL	Timestamp Control	Section 23.13.24
304h	STPXCAPT	Reference Clock Capture	Section 23.13.25
308h	STPXPER	Reference Clock Period	Section 23.13.26
30Ch	STPSCAPT	Captured Ch 0 Sample Clock Counter Value	Section 23.13.27
310h	STPSPER	Sample Clock Period	Section 23.13.28
314h	STPINTRG	Input Pin Trigger Value	Section 23.13.29
318h	STPSSET	Counter Set Operation	Section 23.13.30
31Ch	STPSADD	Step Width Add	Section 23.13.31
320h	STPXMIN	Reference Clock Minimum	Section 23.13.32
324h	STPWCNT	Sample Timer Count	Section 23.13.33
328h	STPXCNT	X-Position Counter	Section 23.13.34
32Ch	STPSTAT	Timestamp Status	Section 23.13.35
1000h	CLKCFG	Clock Configuration	Section 23.13.36
1004h	ADFSCTL1	Antenna Diversity Control	Section 23.13.37
1008h	ADFSCTL2	Adaptive Filter Control	Section 23.13.38

Complex bit access types are encoded to fit into small table cells. Table 23-4 shows the codes that are used for access types in this section.

Table 23-4. PDM Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Wmodify	W modify	Write
Reset or Default Value		
-n		Value after reset or the default value

23.13.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 23-5.

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Description Register This register identifies the peripheral and its exact version.

Table 23-5. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	3342h	Module identification contains a unique peripheral identification number. The assignments are maintained in a central database for all of the platform modules to ensure uniqueness. 0h = Smallest value FFFFh = Highest possible value
15-12	STDIPOFF	R	1h	Standard IP offset 64 Bit standard IP MMR block (beginning with aggregated IRQ registers) 0: STDIP MMRs do not exist 1:15: These MMRs begin at offset 64*STDIPOFF from IP base address 0h = Smallest value Fh = Highest possible value
11-8	INSTIDX	R	0h	Instance Number within the device. This will be a parameter to the RTL for modules that can have multiple instances 0h = Smallest value Fh = Highest possible value
7-4	MAJREV	R	1h	Major revision of the IP 0h = Smallest value Fh = Highest possible value
3-0	MINREV	R	0h	Minor revision of the IP 0h = Smallest value Fh = Highest possible value

23.13.2 DESCEX Register (Offset = 4h) [Reset = 00000000h]

DESCEX is shown in Table 23-6.

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This register reflects the configuration of this peripheral instance

Table 23-6. DESCEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	NUMCHAN	R	0h	Number of available PDM Channels. Value 1 indicates two channels that can be used for stereo or dual mono microphone connections. 0h = Smallest value 7h = Highest possible value

23.13.3 IMASK Register (Offset = 44h) [Reset = 00000000h]

IMASK is shown in Table 23-7.

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Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in MIS.

Table 23-7. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9	DMADONE	R/W	0h	DMA Done event mask. 0h = Interrupt disable 1h = Interrrupt Enable
8	STPTRIG	R/W	0h	Samplestamp Trigger event mask 0h = Clear Interrupt Mask 1h = Interrrupt Enable
7	UNFL	R/W	0h	Data Underflow event mask. 0h = Interrupt disable 1h = Interrrupt Enable
6	OVFL	R/W	0h	Data Overflow event mask. 0h = Interrupt disable 1h = Interrrupt Enable
5-1	RESERVED	R	0h	Reserved
0	PDMDATA	R/W	0h	*PDM* data event mask 0h = Interrupt disable 1h = Interrupt Enable

23.13.4 RIS Register (Offset = 48h) [Reset = 00000000h]

RIS is shown in Table 23-8.

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Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Table 23-8. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9	DMADONE	R	0h	DMA Done event. 0h = Interrupt disable 1h = Interrrupt Enable
8	STPTRIG	R	0h	Samplestamp Trigger event 0h = Interrupt did not occur 1h = Interrrupt Enable
7	UNFL	R	0h	Data Underflow event. Data has been read from an emty FIFO. This flag gets set if one of the channel UNDERFLOW flags gets set. 0h = Interrupt disable 1h = Interrrupt Enable
6	OVFL	R	0h	Data Overflow event. Data has been written to the buffer before the previous values was read. This flag gets set if one of the channel OVERFLOW flags gets set 0h = Interrupt disable 1h = Interrrupt Enable
5-1	RESERVED	R	0h	Reserved
0	PDMDATA	R	0h	PDM DATA event 0h = Interrupt disable 1h = Interrrupt Enable

23.13.5 MIS Register (Offset = 4Ch) [Reset = 00000000h]

MIS is shown in Table 23-9.

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Masked interrupt status. This is an AND of the IMASK and RIS registers.

Table 23-9. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9	DMADONE	R	0h	Masked DMA Done event. 0h = Interrupt disable 1h = Interrrupt Enable
8	STPTRIG	R	0h	Masked Samplestamp Trigger event. 0h = Interrupt did not occur 1h = Interrrupt Enable
7	UNFL	R	0h	Masked Data Underflow event. 0h = Interrupt disable 1h = Interrrupt Enable
6	OVFL	R	0h	Masked Data Overflow event. 0h = Interrupt disable 1h = Interrrupt Enable
5-1	RESERVED	R	0h	Reserved
0	PDMDATA	R	0h	Masked PDMDATA event 0h = Interrupt disable 1h = Interrrupt Enable

23.13.6 ISET Register (Offset = 50h) [Reset = 00000000h]

ISET is shown in Table 23-10.

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Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Table 23-10. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9	DMADONE	W	0h	Set DMA Done event. 0h = Interrupt disable 1h = Interrrupt Enable
8	STPTRIG	W	0h	Set Samplestamp Trigger event. 0h = Writing 0 has no effect 1h = Interrrupt Enable
7	UNFL	W	0h	Set Data Underflow event. 0h = Interrupt disable 1h = Interrrupt Enable
6	OVFL	W	0h	Set Data Overflow event. 0h = Interrupt disable 1h = Interrrupt Enable
5-1	RESERVED	R	0h	Reserved
0	PDMDATA	W	0h	Set PDMDATA event. 0h = Interrupt disable 1h = Interrrupt Enable

23.13.7 ICLR Register (Offset = 54h) [Reset = 00000000h]

ICLR is shown in Table 23-11.

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Interrupt clear. Write a 1 to clear corresponding Interrupt.

Table 23-11. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9	DMADONE	W	0h	Clear DMA Done event. 0h = Interrupt disable 1h = Interrrupt Enable
8	STPTRIG	W	0h	Clear Samplestamp Trigger event. 0h = Writing 0 has no effect 1h = Interrrupt Enable
7	UNFL	W	0h	Clear Data Underflow event. 0h = Interrupt disable 1h = Interrrupt Enable
6	OVFL	W	0h	Clear Data Overflow event. 0h = Interrupt disable 1h = Interrrupt Enable
5-1	RESERVED	R	0h	Reserved
0	PDMDATA	W	0h	Clear PDMDATA event. 0h = Interrupt disable 1h = Interrrupt Enable

23.13.8 EMU Register (Offset = 60h) [Reset = 00000000h]

EMU is shown in Table 23-12.

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This register can be used by the software developer to control the behavior of the peripheral relative to the 'Core Halted' input

Table 23-12. EMU Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	HALT	R/W	0h	Free run control 0h = The peripheral ignores the state of the Core Halted input 1h = The peripheral freezes functionality while the Core Halted input is asserted and resumes when it is deasserted.

23.13.9 CTL Register (Offset = 100h) [Reset = 00000000h]

CTL is shown in Table 23-13.

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PDM control register

Table 23-13. CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	ENPDM	R/W	0h	Enable conversion on *PDM* 0h = Disable Channel 1h = Enable Channel

23.13.10 ICLKCTL Register (Offset = 104h) [Reset = 00000000h]

ICLKCTL is shown in Table 23-14.

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Input clock Control Register

Table 23-14. ICLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	BCLKEN	R/W	0h	This bit is used to enable BCLK to Sigma-Delta Modulator on-chip. 0h = BCLK is disabled 1h = BCLK is enabled
15-10	RESERVED	R	0h	Reserved
9-0	IDIV	R/W	0h	Divider for ICLK iclk = PLLCLK/(ICLK +1) 0h = Minimum value of BDIV 3FFh = Maximum value of BDIV

23.13.11 FIFOCTL1 Register (Offset = 108h) [Reset = 00000000h]

FIFOCTL1 is shown in Table 23-15.

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PDM FIFO control register

Table 23-15. FIFOCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	ENFIFO1	R/W	0h	Enable FIFO1 for DMA access through the FIFODATA Register 0h = Disable Channel 1h = Enable Channel
0	ENFIFO0	R/W	0h	Enable FIFO0 for DMA access through the FIFODATA Register 0h = Disable Channel 1h = Enable Channel

23.13.12 FIFODATA Register (Offset = 10Ch) [Reset = 00000000h]

FIFODATA is shown in Table 23-16.

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FIFO Data Register (FIFO read) This register provides the Data of the FIFO based on [FIFOCTL.ENFIFO0] and [FIFOCTL.ENFIFO1] This allows the DMA to just have single address to read all the FIFO content when triggered.

Table 23-16. FIFODATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALUE	R	0h	FIFO Read Register 0h = Smallest value FFFFFFFFh = Highest possible value

23.13.13 CCTL Register (Offset = 110h) [Reset = 00700000h]

CCTL is shown in Table 23-17.

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PDM Channel control register

Table 23-17. CCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30-29	CH1IPSEL	R/Wmodify	0h	Channel 1 Data Input Select 0h = Data pin 0 selected as source for channel 1. 1h = Data pin 1 selected as source for channel 1. 2h = SDM output selected as source for channel 1. 3h = Data pin 0 selected as source for channel 1.
28	CH1CLKEG	R/W	0h	Select the clock edge for data channel 1 0h = Rising edge is selected 1h = Failing edge is selected
27	RESERVED	R	0h	Reserved
26-25	CH0IPSEL	R/W	0h	Channel 0 Data Input Select 0h = Data pin 0 selected as source for channel 0. 1h = Data pin 1 selected as source for channel 0. 2h = SDM output selected as source for channel 0. 3h = Data pin 0 selected as source for channel 0.
24	CH0CLKEG	R/W	0h	Select the clock edge for data channel 0 0h = Rising edge is selected 1h = Failing edge is selected
23	RESERVED	R	0h	Reserved
22-20	SELSCALE	R/W	7h	Select scaling factor for the averaging blocks. Selscale value used internally is $1/(2^{3+VALUE})$ Ex: When value is 0, selscale is 1/8, and when value is 7, selscale is 1/1024 0h = Scaling factor is 1/8 1h = Scaling factor is 1/16 2h = Scaling factor is 1/32 3h = Scaling factor is 1/64 4h = Scaling factor is 1/128 5h = Scaling factor is 1/256 6h = Scaling factor is 1/512 7h = Scaling factor is 1/1024
19	ENPOWCH1	R/W	0h	Enables average power calculation for channel-1 0h = Enables average power calculation for channel-1 1h = Enables average power calculation for channel-1
18	ENPOWCH0	R/W	0h	Enables average power calculation for channel-0 0h = Disables average power calculation for channel-0 1h = Enables average power calculation for channel-0
17	ENPKCH1	R/W	0h	Enables peak value detection for channel-0 0h = Enables peak value detection for channel-1 1h = Enables peak value detection for channel-1
16	ENPKCH0	R/W	0h	Enables peak value detection for channel-0 0h = Disables peak value detection for channel-0 1h = Enables peak value detection for channel-0
15-12	RESERVED	R	0h	Reserved
11	DATAFMT	R/W	0h	Data Format 0h = Offset binary 1h = Twos complement
10	ALIGN	R/W	0h	Data alignment 0h = Right-aligned. LSB of filter output is bit 0. 1h = Left-aligned. MSB of filter output (depending on OSR) is bit 31.

Table 23-17. CCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-8	DFS	R/W	0h	Digital Filter Select 0h = SINC1 filter 1h = SINC2 filter 2h = SINC3 filter 3h = SINC4 filter
7-3	RESERVED	R	0h	Reserved
2-0	CHEN	R/W	0h	Data Input Configuration 0h = Both Channels are disabled. 1h = Input channel 0 is enabled. 2h = Input channel 1 is enabled. 4h = Input from Manchester Decoder, also enables Manchester Coding of bitstream. CH0 is enabled by default as the operation and CH1 enable bit is discarded.

23.13.14 OSR Register (Offset = 114h) [Reset = 0000003Fh]

OSR is shown in Table 23-18.

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Oversampling Control Register

Table 23-18. OSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VALUE	R/W	3Fh	Oversampling rate. The oversampling rate is defined as OSRx + 1. Applicable oversampling rates are 2 to 256. Default is 64. 1h = Smallest value FFh = Highest possible value

23.13.15 STA Register (Offset = 118h) [Reset = 00000000h]

STA is shown in Table 23-19.

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PDM control register

Table 23-19. STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17	MANCLK	R	0h	Manchester Clock status. Indicates that Manchester mode is in locked mode or not. 0h = Manchester clock not locked. 1h = Manchester clock locked.
16-1	RESERVED	R	0h	Reserved
0	AGCRDY	R	1h	*AGC* accelerator ready status. Software must read AGCVALx, PKVALx and AVGPOWx registers only when AGCRDY is '1'. Reading these registers while AGCRDY is 0 may provide incorrect values. 0h = Not ready 1h = Ready

23.13.16 FIFOCTL2 Register (Offset = 120h) [Reset = 00000000h]

FIFOCTL2 is shown in Table 23-20.

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FIFO Control

Table 23-20. FIFOCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	FIFOFLSH	R/W	0h	FIFO Flush Setting this bit will Flush the FIFO. This bit will self-clear when the flush has completed. 0h = Do not Flush FIFO 1h = Flush FIFO
6-4	RESERVED	R	0h	Reserved
3-0	TRGLVL	R/W	0h	FIFO Trigger Level Select Sets the trigger points for the FIFO events. Note: FIFO depth is only 2 the level 1/4 and 3/4 default to 1/2. 0h = Trigger when RX FIFO contains >= 1 byte 1h = Trigger when RX FIFO contains >= 2 byte 2h = Trigger when RX FIFO contains >= 3 byte 3h = Trigger when RX FIFO contains >= 4 byte 4h = Trigger when RX FIFO contains >= 5 byte 5h = Trigger when RX FIFO contains >= 6 byte 6h = Trigger when RX FIFO contains >= 7 byte 7h = Trigger when RX FIFO contains >= 8 byte 8h = Trigger when RX FIFO contains >= 9 byte 9h = Trigger when RX FIFO contains >= 10 byte Ah = Trigger when RX FIFO contains >= 11 byte Bh = Trigger when RX FIFO contains >= 12 byte

23.13.17 FIFOSR Register (Offset = 124h) [Reset = 00000000h]

FIFOSR is shown in Table 23-21.

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FIFO Status Register.

Table 23-21. FIFOSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	CH1FFULL	R	0h	CH1 FIFO Full 0h = The transmitter is not full. 1h = If the FIFO is disabled (FEN is 0), the transmit holding register is full. If the FIFO is enabled (FEN is 1), the transmit FIFO is full.
14	CH1FEMP	R	1h	CH1 FIFO Empty 0h = The transmitter has data to transmit. 1h = If the FIFO is disabled (FEN is 0), the transmit holding register is empty. If the FIFO is enabled (FEN is 1), the transmit FIFO is empty.
13-12	RESERVED	R	0h	Reserved
11-8	CH1FCNT	R	0h	Number of Bytes which could be read from the CH1 FIFO 0h = Smallest value Fh = Highest possible value
7	CH0FFULL	R	0h	CH0 FIFO Full 0h = The receiver can receive data. 1h = If the FIFO is disabled (FEN is 0), the receive holding register is full. If the FIFO is enabled (FEN is 1), the receive FIFO is full.
6	CH0FEMP	R	1h	CH0 FIFO Empty 0h = The receiver is not empty. 1h = If the FIFO is disabled (FEN is 0), the receive holding register is empty. If the FIFO is enabled (FEN is 1), the receive FIFO is empty.
5-4	RESERVED	R	0h	Reserved
3-0	CH0FCNT	R	0h	Number of Bytes which could be read from the CH0 FIFO 0h = Smallest value Fh = Highest possible value

23.13.18 AVGVAL0 Register (Offset = 200h) [Reset = 00000000h]

AVGVAL0 is shown in Table 23-22.

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Average sample value for channel-0, 32-bit register.

Table 23-22. AVGVAL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALUE	R	0h	Average sample value for channel-0 0h = Minimum value of register FFFFFFFFh = Highest value

23.13.19 PKVAL0 Register (Offset = 204h) [Reset = 00000000h]

PKVAL0 is shown in Table 23-23.

Return to the Summary Table.

Peak sample value for channel-0

Table 23-23. PKVAL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	VALUE	R	0h	Peak sample value for channel-0. Bits [22:0] applicable for operation in 2's complement format and bits [23:0] applicable for operation in offset binary format. 0h = Smallest value 007FFFFFh = Largest value

23.13.20 AVGPOW0 Register (Offset = 208h) [Reset = 00000000h]

AVGPOW0 is shown in Table 23-24.

Return to the Summary Table.

Average sample power for channel-0

Table 23-24. AVGPOW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALUE	R	0h	Average sample power for channel-0 0h = Smallest value FFFFFFFFh = Highest value

23.13.21 AVGVAL1 Register (Offset = 20Ch) [Reset = 00000000h]

AVGVAL1 is shown in Table 23-25.

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Average sample value for channel-1, 32-bit register.

Table 23-25. AVGVAL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALUE	R	0h	Average sample value for channel-1 0h = Minimum value of register FFFFFFFFh = Highest value

23.13.22 PKVAL1 Register (Offset = 210h) [Reset = 00000000h]

PKVAL1 is shown in Table 23-26.

Return to the Summary Table.

Peak sample value for channel-1

Table 23-26. PKVAL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	VALUE	R	0h	Peak sample value for channel-1. Bits [22:0] applicable for operation in 2's complement format and bits [23:0] applicable for operation in offset binary format. 0h = Smallest value 007FFFFFh = Largest value

23.13.23 AVGPOW1 Register (Offset = 214h) [Reset = 00000000h]

AVGPOW1 is shown in Table 23-27.

Return to the Summary Table.

Average sample power for channel-1

Table 23-27. AVGPOW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALUE	R	0h	Average sample power for channel-1 0h = Smallest value FFFFFFFFh = Highest value

23.13.24 STPCTL Register (Offset = 300h) [Reset = 00000000h]

STPCTL is shown in Table 23-28.

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Samplestamp Generator Control Register

Table 23-28. STPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	STPEN	R/W	0h	Enables the samplestamp generator. The samplestamp generator must only be enabled after it has been properly configured.;When cleared, all samplestamp generator counters and capture values are cleared. 0h = Disable the samplestamp generator 1h = Enable the samplestamp generator

23.13.25 STPXCAPT Register (Offset = 304h) [Reset = 00000000h]

STPXCAPT is shown in Table 23-29.

Return to the Summary Table.

Captured REFCLK Counter Value, Capture Channel 0

Table 23-29. STPXCAPT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CAPTVAL	R	0h	The value of the samplestamp XOSC counter [STMPXCNT.CURR_VALUE] last time an event was pulsed. The value is cleared when [STMPCTL.STMP_EN] = 0. Note: When calculating the fractional part of the sample stamp, [STMPXPER] may be less than this bit field. 0h = Smallest value FFFFh = Highest possible value

23.13.26 STPXPER Register (Offset = 308h) [Reset = 00000000h]

STPXPER is shown in Table 23-30.

Return to the Summary Table.

REFCLK Period Value

Table 23-30. STPXPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALUE	R	0h	The number of REFCLK clock cycles in the previous Sample Clock period (that is - the next value of the REFCLK counter at the positive Sample Clock edge, had it not been reset to 0).;The value is cleared when [STMPCTL.STMP_EN] = 0. 0h = Smallest value FFFFh = Highest possible value

23.13.27 STPSCAPT Register (Offset = 30Ch) [Reset = 00000000h]

STPSCAPT is shown in Table 23-31.

Return to the Summary Table.

Captured Sample Clock Counter Value, Capture Channel 0

Table 23-31. STPSCAPT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CAPTVAL	R	0h	The value of the samplestamp Sample Clock counter [STMPWCNT.CURR_VALUE] last time an event was pulsed. This number corresponds to the number of positive Sample Clock edges since the samplestamp generator was enabled;The value is cleared when [STMPCTL.STPEN] = 0. 0h = Smallest value FFFFh = Highest possible value

23.13.28 STPSPER Register (Offset = 310h) [Reset = 00000000h]

STPSPER is shown in Table 23-32.

Return to the Summary Table.

Sample Clock Counter Period Value

Table 23-32. STPSPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALUE	R/W	0h	Used to define when [STMPWCNT] is to be reset so number of Sample Clock edges are found for the size of the sample buffer. This is thus a modulo value for the Sample Clock counter. This number must correspond to the size of the sample buffer used by the system (that is the index of the last sample plus 1). 0h = Smallest value FFFFh = Highest possible value

23.13.29 STPINTRG Register (Offset = 314h) [Reset = 00000000h]

STPINTRG is shown in Table 23-33.

Return to the Summary Table.

WS Counter Trigger Value for Input Pins

Table 23-33. STPINTRG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	INSTRWCT	R/W	0h	In Start W Count Compare value used to start the incoming audio streams.;This bit field must equal the Sample Clock counter value during the Sample Clock period in which the first input word(s) are sampled and stored to memory (that is the sample at the start of the very first DMA input buffer).;The value of this register takes effect when at least 32 PDMxCLK cycle ticks have happened.;Note: To avoid false triggers, this bit field must be set higher than VALUE. 0h = Smallest value FFFFh = Highest possible value

23.13.30 STPSSET Register (Offset = 318h) [Reset = 00000000h]

STPSSET is shown in Table 23-34.

Return to the Summary Table.

Sample Clock Counter Set Operation

Table 23-34. STPSSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALUE	R/W	0h	Sample Clock counter modification: Sets the running Sample Clock counter equal to the written value. 0h = Smallest value FFFFh = Highest possible value

23.13.31 STPSADD Register (Offset = 31Ch) [Reset = 00000000h]

STPSADD is shown in Table 23-35.

Return to the Summary Table.

Sample Clock Counter Add Operation

Table 23-35. STPSADD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALINC	R/W	0h	Sample Clock counter modification: Adds the written value to the running Sample Clock counter. If a positive edge of Sample Clock occurs at the same time as the operation, this will be taken into account.;To add a negative value, write "[STMPWPER.VALUE] - value".; 0h = Smallest value FFFFh = Highest possible value

23.13.32 STPXMIN Register (Offset = 320h) [Reset = 00000000h]

STPXMIN is shown in Table 23-36.

Return to the Summary Table.

REFCLK Minimum Period Value;Minimum Value of STPXPER

Table 23-36. STPXMIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALUE	R/W	FFFFh	Each time [STMPXPER] is updated, the value is also loaded into this register, provided that the value is smaller than the current value in this register.;When written, the register is reset to 0xFFFF (65535), regardless of the value written.;The minimum value can be used to detect extra Sample Clock pulses (this registers value will be significantly smaller than [STMPXPER.VALUE]). 0h = Smallest value FFFFh = Highest possible value

23.13.33 STPWCNT Register (Offset = 324h) [Reset = 00000000h]

STPWCNT is shown in Table 23-37.

Return to the Summary Table.

Current Value of sample clock count This register is reset when STPEN = 0.

Table 23-37. STPWCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CURRVAL	R	0h	Current value of the Sample Clock counter 0h = Smallest value FFFFh = Highest possible value

23.13.34 STPXCNT Register (Offset = 328h) [Reset = 00000000h]

STPXCNT is shown in Table 23-38.

Return to the Summary Table.

Current Value of XCNT This register is reset when STPEN = 0.

Table 23-38. STPXCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CURRVAL	R	0h	Current value of the REFCLK counter, latched when reading [STMPWCNT]. 0h = Smallest value FFFFh = Highest possible value

23.13.35 STPSTAT Register (Offset = 32Ch) [Reset = 00000000h]

STPSTAT is shown in Table 23-39.

Return to the Summary Table.

Samplestamp Generator Status Register

Table 23-39. STPSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	INRDY	R	0h	Low until the input pins are ready to be started by the samplestamp generator. When started (that is [STMPINTRIG] equals the WCLK counter) the bit goes back low. 0h = Clear 1h = Set
0	RESERVED	R	0h	Reserved

23.13.36 CLKCFG Register (Offset = 1000h) [Reset = 00000000h]

CLKCFG is shown in Table 23-40.

Return to the Summary Table.

Clock configuration register Note: Disable the CLKCFG.MEM_CLK_EN and CLKCFG.ADFS_EN to change [CLK_CFG.MEM_CLK_SEL] or [ADFS_CTRL1]/[ADFS_CTRL2] After changing [CLK_CFG.MEM_CLK_SEL] or [ADFS_CTRL1]/[ADFS_CTRL2], enable CLKCFG.ADFS_EN followed by CLKCFG.MEM_CLK_EN

Table 23-40. CLKCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	ADFSEN	R/W	0h	ADFS Enable bit 0h = Disable ADFS 1h = Enable ADFS
6-4	CLKSEL	R/W	0h	Clock Select 0h = No Clock 1h = SOC Clock(80MHz) 2h = SOC PLL Clock(un-swallowed 80MHz) 3h = HFXT
3-1	RESERVED	R	0h	Reserved
0	CLKEN	R/W	0h	Clock enable 0h = Disable Clock 1h = Enable Clock

23.13.37 ADFSCTL1 Register (Offset = 1004h) [Reset = 00000000h]

ADFSCTL1 is shown in Table 23-41.

Return to the Summary Table.

ADFS control register

Table 23-41. ADFSCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20-0	TREF	R/W	0h	Reference clock time period

23.13.38 ADFSCTL2 Register (Offset = 1008h) [Reset = 00000000h]

ADFSCTL2 is shown in Table 23-42.

Return to the Summary Table.

ADFS control register 2

Table 23-42. ADFSCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-20	DIV	R/W	0h	Value of divider to be used for ADFS
19-18	RESERVED	R	0h	Reserved
17	DLTASIGN	R/W	0h	Sign of delta value to be used. 0h = Positive Sign 1h = Negative sign
16-0	DELTA	R/W	0h	Difference in time periods of (reference clk/divisor) and required clock

Chapter 24

Analog to Digital Converter (ADC)

This chapter describes the functionality of the Analog to Digital Converter (ADC) module.

24.1 Overview

The purpose of the ADC is to measure analog signals and convert them to a digital representation with minimal CPU intervention providing for lower power and greater task integration.

The ADC supports fast 12-bit analog-to-digital conversions. The ADC implements a 12-bit Successive Approximation Register (SAR) core, sample/conversion mode control, and up to 6 independent conversion-and-control buffers. This means the ADC allows up to 6 independent analog-to-digital converter (ADC) samples to be converted and stored without any CPU intervention.

ADC features include:

- 12-bit resolution conversion (based on SAR-12 core)
- Up to 12 (4 internal, 8 external) individually configurable analog input channels
  - Internal conversion channels for temperature sensing and supply monitoring.
  - External conversion channels accessible by GPIOs
- Full scale ADC operating voltage range (configurable 1.8V or 3.3V)
- Configurable ADC reference source: internal or external reference voltage
  - Internal reference
    - Voltage 1.4V (by on-chip Internal Reference Buffer)
    - 1Msps sample rate
  - External reference
    - Voltage 1.8V (Shorted to VPP pin)
    - 2Msps sample rate
- Configurable ADC clock source: SOC CLK or HFXT
- Sample-and-hold with programmable sampling periods controlled by software or timers
- Different conversion modes: Single-channel, repeat-single-channel, sequence, repeat-sequence, and software requested ad-hoc single conversion modes
- Window comparator with provision to configure low and high threshold values for low-power monitoring of input signals from conversion-result registers
- Two sampling trigger sources: software trigger and event trigger
- Sixteen 12-bit conversion-result storage registers (MEMRES_0:15)
- Support for FIFO and non-FIFO modes for CPU and DMA
- Data compaction within FIFO for 32-bit reads
- Automatic and manual power down schemes
- Unsigned binary and two's complement data format
- Single and differential mode inputs
- 10-bit sample timer with two independent sample time compare registers
- Sample time compare value selection in each memory control register
- Different event sources with single event output

24.2 Block Diagram

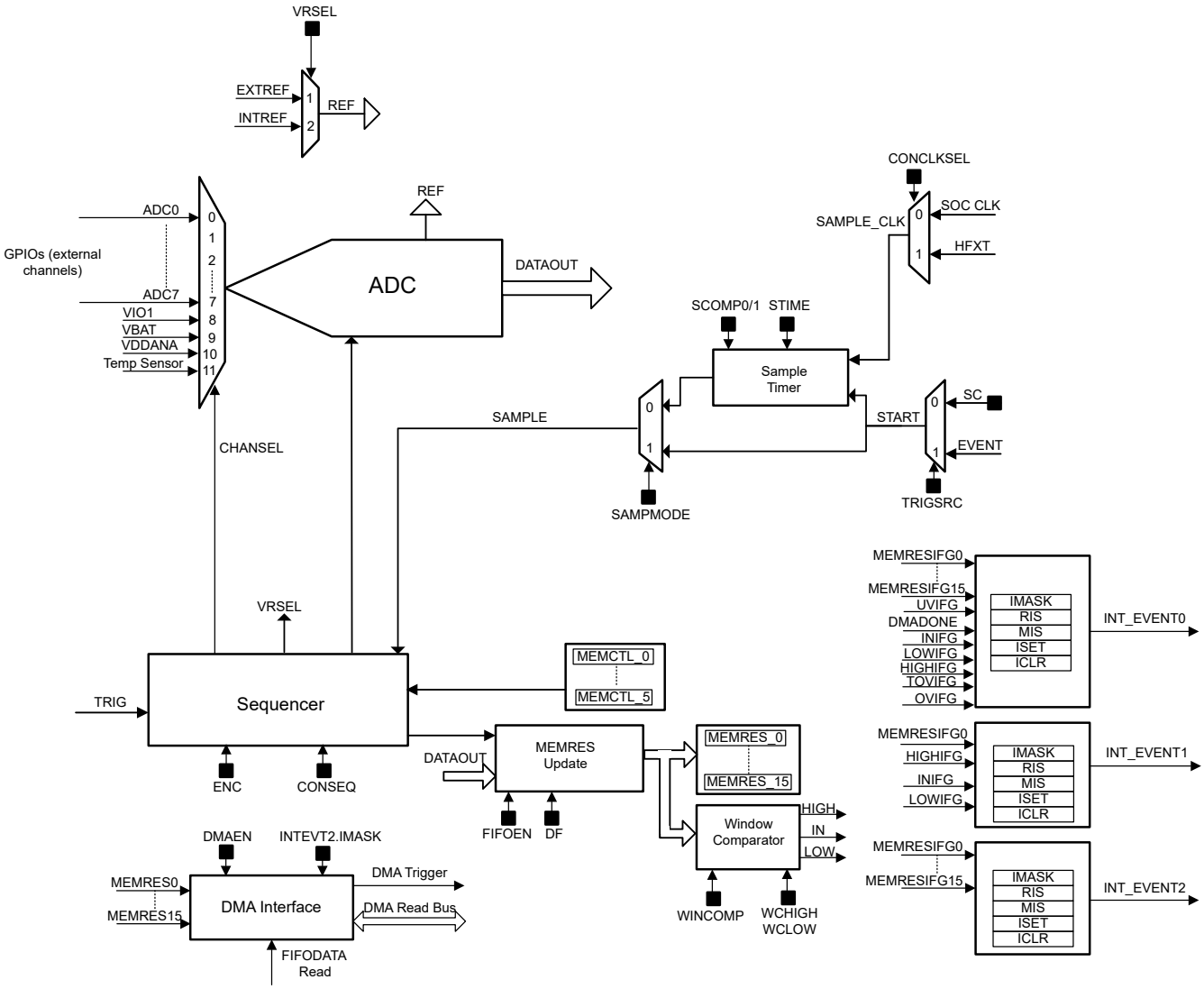

Figure 24-1. ADC Block Diagram

24.3 Functional Description

The ADC is configured with user software. The following sections describe the setup and operation of the ADC.

24.3.1 ADC Core

The ADC core converts an analog input to a digital representation. The core uses two voltage levels (V_{R+} and V_{R-}) to define the upper and lower limits of the conversion. The digital output (N_{ADC}) is full scale when the input signal is equal to or higher than V_{R+}, and is zero when the input signal is equal to or lower than V_{R-}. The input channel and the positive reference voltage level (V_{R+}) are defined in the conversion-control memory.

Equation 16 shows the conversion formula for the ADC result, NADC, for n-bit resolution mode

$$N_{ADC} = \left(2^n - 1\right) \times \frac{(V_{in} + 0.5LSB) - V_{R-}}{V_{R+} - V_{R-}} \qquad Where\ LSB = \frac{V_{R+} - V_{R-}}{2^n} \tag{16}$$

Given that V_{R-} is 0 V in this ADC, the equation for N_{ADC} becomes:

$$N_{ADC} = \left(2^n - 1\right) \times \frac{(V_{in} + 0.5LSB)}{V_{R+}} \qquad Where\ LSB = \frac{V_{R+}}{2^n} \tag{17}$$

Equation 18 describes the input voltage at which the ADC output saturates:

$$V_{in} = V_{R+} - 1.5LSB \tag{18}$$

Note

The ADC is not functional in SLEEP or SHUTDOWN modes.

24.3.2 Voltage Reference Options

The ADC voltage reference (V_{R+}) can be configured through the VRSEL bits in the MEMCTL register. Different reference sources can be selected for conversion on different channels. There are two options available for supplying a reference voltage to the ADC:

1. External reference (EXTREF) supplied to the ADC through the VPP pin.
2. Internal reference voltage of 1.4V (INTREF)

When supplying an external reference to the ADC, the VPP pin is connected to the reference source with the appropriate decoupling circuitry.

24.3.3 Internal Channels

The ADC module supports four internal channels (ADC channel 8-11) for preset measurements of temperature sensing and supply monitoring. These channels are set as:

Table 24-1. ADC Internal Channels

ADC Channel	Connected Module	Description
8	VIO1	I/O Voltage ring VIO1. The external ADC channels (which are accessible through GPIOs) are complacent with VIO1.
9	VBAT	Digital supply voltage. Sourced from external supply pin VMAIN.
10	VDDANA	Analog supply voltage. Sourced from external supply pin VDDANA1/2.
11	Temperature sensor	Internal temperature sensor

24.3.4 Resolution Modes

The ADC supports operation in 12-bit resolution mode. The conversion phase requires a total of 14 conversion clock cycles. The conversion window is based on the resolution mode and the frequency of ADCCLK. For more details, refer to Figure 24-2 and Figure 24-3.

24.3.5 ADC Clocking

The ADC peripheral clock (ADCCLK) is provided by PRCM and is used for the sampling clock (SAMPCLK). SOC CLK and HFXT are the clock sources available for ADCCLK, which can support up to 52 MHz. Refer to the device-specific data sheet for supported ADCCLK frequencies. Using SOC CLK, which is the bus clock for all peripherals, is very useful for deterministic start of sampling and simultaneous sampling. Using the HFXT as the clock source for ADCCLK is useful for when a very accurate, low-jitter, sampling period is needed. The ADC clock source can be selected by writing the CONVCTL[17:16] CONCLKSEL bit field.

24.3.6 Power Down Behavior

To save power, disable the ADC when not in use. The PWRDN bit in the CTL0 register selects the ADC power down policy between AUTO and MANUAL.

Configure PWRDN based on the max ADC sampling rate required and the operational needs in different power modes.

The reset value of PWRDN is ‘0’ which has the default behavior of automatic power down of the ADC peripheral at the end of a conversion and when the next sample signal is not required to be asserted immediately. When the PWRDN bit is set to ‘1’ the bit selects manual power down behavior. In this setting, the ADC is not powered down at the end of a conversion and remains enabled.

Refer to the device-specific data sheet for specifications on the ADC wakeup/enable time.

24.3.7 Sampling Trigger Sources and Sampling Modes

Sampling Trigger Sources

There are two sampling trigger sources available which can be selected through the TRIGSRC bit in the CTL1 register; one is a software trigger and the other is an event trigger.

When the software trigger is selected as the source, the application software can set the Start Conversion (SC) bit in the CTL1 register to initiate the sample phase. When the event trigger is selected as the source, a rising edge on the selected event from the event manager initiates the sample phase. An event is always edge triggered.

Sampling Modes

There are two sampling modes available, AUTO and MANUAL, which are selected through the SAMPMODE bit in the CTL1 register.

24.3.7.1 AUTO Sampling Mode

In AUTO mode, the sample signal is generated synchronous to the sampling clock (SAMPCLK) and can be programmed using an internal sampling timer to determine the duration of the sampling window. The sample timer is 10-bit wide and there are two sample time compare registers (SCOMPx) available to account for various source impedances to measure signals from. One of these two SCOMP registers can be selected using the STIME bit in the MEMCTL register.

Figure 24-2 shows the ADC sample and conversion timing diagram when the ADC is configured in AUTO sampling mode.

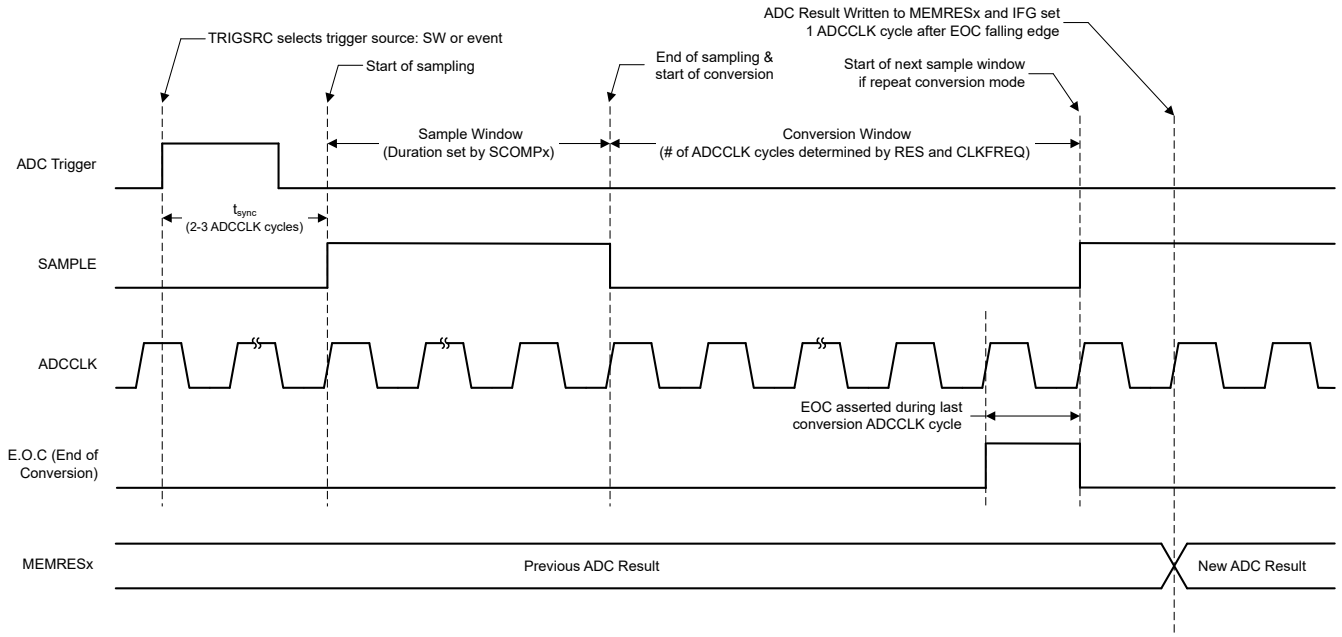

Figure 24-2. AUTO Sampling Mode - ADC Sample and Conversion Timing Diagram

Note

When the reset value of PWRDN is set as ‘0’, which has the default behavior of automatic power down, ADC wake-up time needs to be considered in each sample window. Refer to the device-specific data sheet for specifications on the ADC wake-up time. For example, if the maximum ADC wake-up time is 5 µs, then the duration set by SCOMPx is > (5 µS + Duration for sample window).

24.3.7.2 MANUAL Sampling Mode

In MANUAL mode, the sample signal is generated when the SC bit is set which can be asynchronous to the sampling clock. The duration of the sampling window is controlled by software by holding the SC bit high.

Because an event is always edge triggered, manual mode with event trigger is not supported for any of the conversion modes. Software trigger with manual sampling mode is supported only for single channel single conversion mode and is not supported for any of the other three conversion modes.

There is a 2-3 cycle synchronization latency from when the sample window ends to when the conversion window begins.

Figure 24-3 shows the ADC sample and conversion timing diagram when the ADC is configured in MANUAL sampling mode:

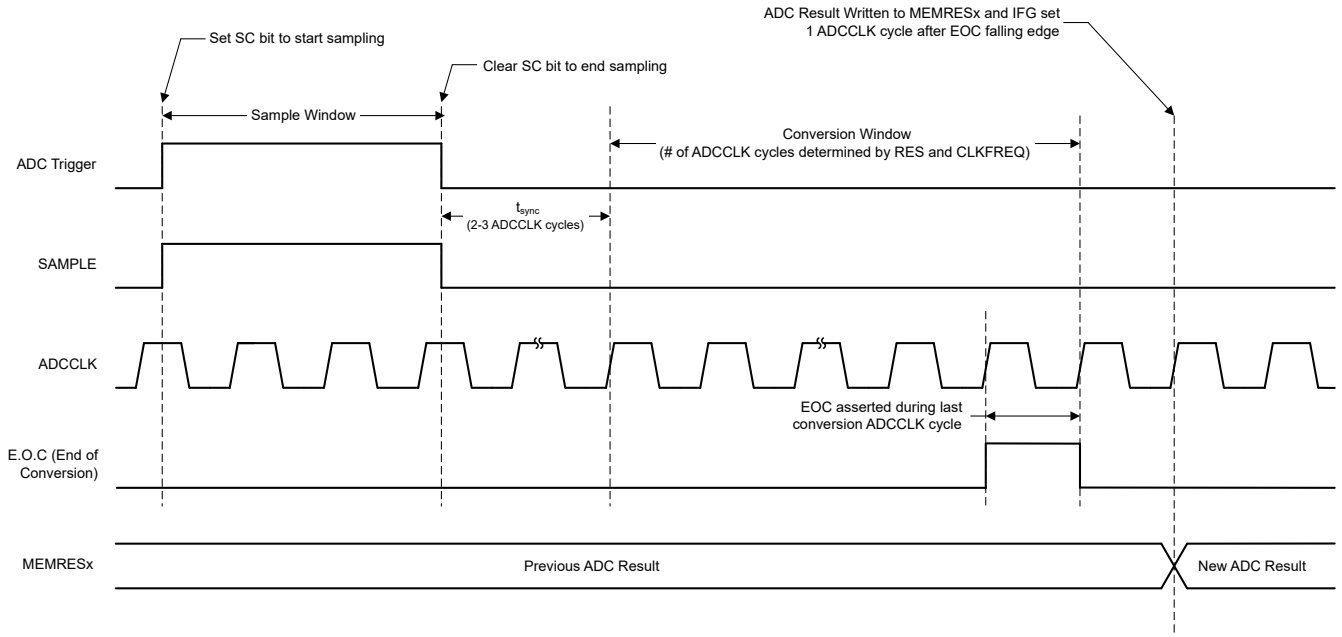

Figure 24-3. MANUAL Sampling Mode - ADC Sample and Conversion Timing Diagram

Note

When the reset value of PWRDN is set as '0' which has the default behavior of automatic power down, ADC wake-up time needs to be considered before sample window. Refer to the device-specific data sheet for specifications on the ADC wake-up time.

24.3.8 Sampling Period

The desired sampling period for ADC operation can be generated using the internal clock divider and/or the sample timer, which applies to AUTO sampling mode. The internal clock divider is configured using the SCLKDIV bits in the CTL0 register and has divide options of 1, 2, 4, 8, 16, 24, 32, and 48.

The duration of the sampling period can be programmed to one of two user-defined values set by the SCOMP0 and SCOMP1 sample timer registers. The value in SCOMPx configures the sampling period by defining the number of sample time clocks to set the sample window to. The default SCOMPx sample timer value translates to 1 cycle wide sample pulse which allows the sampling period to be solely based on the sample clock and SCLKDIV. In general, there are three parameters that can be used to control the sample period: SCOMPx, SCLKDIV, and the source of the sample clock.

When AUTO power down mode is selected using PWRDN=0, the module enable signal to the ADC peripheral is generated one sampling clock cycle after the sample signal is asserted. This should be considered by the user in the sample window calculation in addition to the ADC power time or settling time needs of other analog modules such as the Temperature Sensor, VREF, etc.

24.3.9 Conversion Modes

There are four conversion modes available in the ADC:

1. Single channel single conversion
   - The channel can be selected using MEMCTL
   - The selected channel is sampled and converted only once
2. Repeat single channel conversion
   - The channel can be selected using MEMCTL
   - The selected channel is repeatedly sampled and converted until ENC is cleared by software
3. Sequence of channels conversion

- Groups of channels can be formed using STARTADD, ENDADD, and MEMCTL registers
- Each of the channels in the group is sampled and converted only once
- The sequence completes even if ENC is cleared in the middle of the sequence

4. Repeat sequence of channels conversion
   - Groups of channels can be formed using STARTADD, ENDADD, and MEMCTL registers
   - Each of the channels is sampled based on trigger configuration
   - When ENC is cleared the operation stops at the end of the ongoing sequence

The following steps outline the recommended process for configuring the ADC for a desired conversion mode:

1. Use the CONSEQ bits in the CTL1 register to select the desired ADC conversion mode
2. Use the STARTADD bits in the CTL2 register to select which MEMCTLx is used for single conversion or as first MEMCTL for a sequence mode
3. If using a sequence mode, use the ENDADD bits in the CTL2 register to select which MEMCTLx is used for the last conversion of the sequence
4. Assign an ADC input channel to the appropriate MEMCTLx register using the CHANSEL bits
   - For sequence modes, ADC input channel must be assigned for each MEMCTLx that is part of the configured sequence
5. Select EVENT or SOFTWARE trigger using the TRIGSRC bit in the CTL1 register
6. Select AUTO or MANUAL sampling mode using the SAMPMODE bit in the CTL1 register
   - If using AUTO mode, program the desired sample timer value in the SCOMPx register and use the STIME bits in the MEMCTLx register to select the appropriate sample timer source (SCOMP0 or SCOMP1)
7. If using repeat single channel or sequence conversion modes, program the TRIG bit in each MEMCTLx register to indicate if a trigger is needed to step to the next MEMCTL in the sequence
8. Set the ENC bit in the CTL1 register to enable ADC conversions
9. Table 24-2 depicts the next step of ADC configuration and usage based on the selected trigger and sampling modes

Table 24-2. Trigger and Sample Mode ADC Usage Matrix

	Software Trigger	Event Trigger
AUTO Sampling Mode	• Set SC bit to start the sample phase (duration determined by sample timer) • Conversion starts once sample phase is over • In single channel single conversion, ENC is cleared when conversion is over • SC bit is automatically cleared once the trigger is captured For repeat and sequence modes, if TRIG is set in MEMCTL, the SC bit needs to be set for the next conversion to proceed.	• EVENT trigger starts the sample phase (duration determined by sample timer) • Conversion starts once sample phase is over • In single channel single conversion, ENC is cleared when conversion is over For repeat and sequence modes, ADC waits for EVENT trigger or automatically starts the next conversion based on TRIG setting.
MANUAL Sampling Mode	• Set SC bit to start the sample phase (SC bit is not automatically reset) • Clear the SC bit to end the sample phase and start the conversion • In single channel single conversion, ENC bit is cleared when conversion is over Repeated/sequential conversion modes are NOT supported in this configuration.	ADC operation is NOT supported in this configuration

10. The ADC results are stored in the MEMRES register of the associated MEMCTL (for example, the MEMCTL0 result is stored in MEMRES0).

- For repeat conversion modes, the result in MEMRES is updated after every associated MEMCTL conversion

When in FIFO mode, the ADC results are stored as described in Section 24.3.13.2.2

11. For repeated conversion modes, clear the ENC bit to stop ADC operation.

Note

In case a hardware event is being used as the sample trigger source, software must ensure that the event trigger is disabled first before clearing the ENC bit to stop ADC operations.

24.3.10 ADC Data Format

The ADC supports two data formats – unsigned binary and 2's complement signed binary. Unsigned binary results are stored right-justified in the MEMRES register or FIFO. Signed binary results are stored left justified in the MEMRES register or FIFO.

Table 24-3. ADC Data Formats

Data Format	Resolution	Result Range (decimal)	Result Range
Unsigned	12-bit	0 to 4095	0000h to 0FFFh
Signed	12-bit	-2048 to 2047	8000h to 7FF0h

24.3.11 Status Register

The ADC status register, STA, contains two bits – ASCACT and BUSY

- BUSY equaling '1' indicates that the ADC is busy performing a sample or conversion operation
  - For **single channel single conversion**, BUSY signals that a trigger has been received and sample or conversion is ongoing. BUSY is cleared when the conversion completes
  - For **repeat single conversion**, BUSY signals that repeat single operation has begun and has not ended. BUSY is cleared when ENC is written '0' and the last conversion completes
  - For **sequence of channels conversion**, BUSY signals that the sequence of channels conversion has started. BUSY is cleared at the end of the sequence
  - For **repeat sequence of channels conversion**, BUSY signals the repeat sequence is ongoing. BUSY is cleared when ENC is written '0' and the last conversion in the sequence completes

Note

In case of an ADC start of conversion issued by software through the SC bit, software has to wait for at least 9 SOC CLK clock cycles if polling for the BUSY status bit in the program code. This is to account for internal clock synchronization latencies before the ADC status bit is updated.

24.3.12 ADC Events

The ADC peripheral contains three event publishers and one event subscriber.

Two event publishers (INT_EVENT0 & INT_EVENT1) can be used to publish ADC events to a subscriber through the Event Manager. The third event publisher (INT_EVENT2) can be used as an ADC to DMA trigger to send ADC events directly to the DMA.

The event subscriber can be used to subscribe to events which are published to the event manager through a generic event route channel.

The ADC events are summarized in Table 24-4

Table 24-4. ADC Events

Event	Type	Source	Destination	Configuration	Functionality
Generic publisher event	Publisher	ADC	Event Manager	INT_EVENT0 registers	Trigger generic event channel from ADC

Table 24-4. ADC Events (continued)

Event	Type	Source	Destination	Configuration	Functionality
Generic publisher event	Publisher	ADC	Event Manager	INT_EVENT1 registers	Trigger generic event channel from ADC
DMA trigger event	Publisher	ADC	DMA	INT_EVENT2 registers	Fixed trigger route from ADC to DMA
Generic subscriber event	Subscriber	Other peripherals	ADC	SOC_AON.SPEVTCTL	ADC subscription to generic event within Event Manager

24.3.12.1 Generic Event Publishers (INT_EVENT0 & INT_EVENT1)

The ADC peripheral provides many interrupt sources which can be configured to publish one of the two generic ADC events (INT_EVENT0 or INT_EVENT1) through Event Manager . The possible interrupt sources for INT_EVENT0 and INT_EVENT1 are listed in Table 24-5 and Table 24-6, respectively.

Table 24-5. ADC Generic Event 0 Publisher Conditions (INT_EVENT0)

RIS (Bit Index)	Name	Description
0	OVIFG	Conversion overflow interrupt flag is set when the ADC updates MEMRESx before the previous sample is read by the CPU or DMA
1	TOVIFG	Sequence conversion time overflow interrupt flag is set when the ADC receives a new sampling trigger while the previous sample+conversion is still in progress
2	HIGHIFG	High threshold compare interrupt flag is set when the MEMRESx result register is higher than the WCHIGH threshold of the window comparator
3	LOWIFG	Low threshold compare interrupt flag is set when the MEMRESx result register is lower than the WCLOW threshold of the window comparator
4	INIFG	In-range comparator interrupt flag is set when the MEMRESx result register is within the range of WCLOW and WCHIGH of the window comparator
5	DMADONE	DMA done interrupt flag is set when the DMA data transfer of programmed block size is completed
6	UVIFG	Conversion underflow interrupt flag, the UVIFG flag is set when the CPU or DMA reads the MEMRESx register before the next conversion result is available
8 to 23	MEMRESIFG[0 to 15]	Memory register interrupt flag is set when MEMRESx is loaded with a new conversion result

Table 24-6. ADC Generic Event 1 Publisher Conditions (INT_EVENT1)

RIS (Bit Index)	Name	Description
2	HIGHIFG	High threshold compare interrupt flag is set when the MEMRESx result register is higher than the WCHIGH threshold of the window comparator
3	LOWIFG	Low threshold compare interrupt flag is set when the MEMRESx result register is lower than the WCLOW threshold of the window comparator
4	INIFG	In-range comparator interrupt flag is set when the MEMRESx result register is within the range of WCLOW and WCHIGH of the window comparator
8	MEMRESIFG0	Memory register interrupt flag is set when MEMRES0 is loaded with a new conversion result

The generic event configuration is managed with the INT_EVENT0 and INT_EVENT1 registers. Interrupt (RIS) flags are cleared upon software writing to the respective ICLR register bits.

24.3.12.2 DMA Trigger Event Publisher (INT_EVENT2)

The ADC module provides many interrupt sources which can be configured to source the DMA trigger. In order of decreasing interrupt priority, the DMA trigger events from the ADC are given in Table 24-7. When the DMA channel is needed by the ADC, the DMA trigger is unmasked in the IMASK register of INT_EVENT2 and the DMA is configured as needed to support the ADC operation.

Table 24-7. ADC DMA Trigger Event Conditions (INT_EVENT2)

RIS Index	Name	Description
8 to 23	MEMRESIFG[0 to 15]	Memory register interrupt flag is set when MEMRESx is loaded with a new conversion result

The DMA trigger event configuration is managed with the INT_EVENT2 event management registers. The interrupt (RIS) flags are cleared based on ACK from DMA.

24.3.12.3 Generic Event Subscriber

The ADC peripheral supports receiving events routed through a generic channel from other peripherals via the SOC_AON.SPEVCTL register.

24.3.13 Advanced Features

The following sections describe the additional features and benefits provided with the ADC peripheral and how to leverage them in an application.

24.3.13.1 Window Comparator

There is one window comparator unit available in the ADC which can be used to check if the input signal is within predefined threshold values set by software. The ADC result that goes into MEMRES is what gets checked against the threshold values of the window comparator.

Based on the comparison the window comparator can generate 3 interrupt conditions:

1. LOWIFG– Conversion result is below the Low threshold (WCLOW)
2. HIGHIFG– Conversion result is above the High threshold (WCHIGH)
3. INIFG– Conversion result is in between or equal to the Low and High thresholds

The window comparator low and high threshold values are global for all channels and the window comparison feature can be enabled for each channel as needed using the WINCOMP bit in the MEMCTL register.

When the ADC result data format (CTL2.DF) or resolution (CTL2.RES) configuration is changed, the window comparator threshold values are not reset by hardware and are retained as is. The software application is expected to reconfigure the threshold values as appropriate after changing the data format and/or resolution configuration.

Note

Do not use comparator mode when using FIFO mode described in 1.3.13.2.2.

24.3.13.2 DMA & FIFO Operation

The ADC has a dedicated interface for communicating with the DMA. This interface is useful to offload work from the CPU by using the DMA to store ADC results to memory automatically.

The DMAEN bit in the CTL2 register is used to enable the DMA for ADC data transfer. The DMAEN bit is cleared by ADC hardware when the DMA “DONE" status signal is asserted. Software is expected to re-enable the DMA using DMAEN to arm the ADC to generate the next DMA trigger.

The ADC also incorporates an optional First-In-First-Out buffer to provide a way for ADC results to be stored for future use, such as transferring to memory by the DMA. Either the CPU or the DMA can be used to move data from the ADC regardless of whether the FIFO is enabled or disabled. The memory result flags in the RIS register of the third event publisher serve as the FIFO threshold and can be unmasked to generate the DMA trigger.

The following sections explain the details of using the ADC with DMA or CPU in various conversion modes and with the FIFO enabled or disabled.

24.3.13.2.1 DMA/CPU Operation in Non-FIFO Mode (FIFOEN=0)

- Single Conversion and Repeat Single Conversion
  - Configure STARTADD bits to select the desired MEMCTLx register

    - MEMCTLx **is correlated to** MEMRESx
    - MEMRESx **is correlated to** MEMRESIFGx
  - Configure MEMCTL CHANSEL bits to select the desired ADC channel
  - Conversion data is available in MEMRESx
  - MEMRESIFGx can be set to generate a CPU interrupt (INT_EVENT0/1) or the DMA trigger (INT_EVENT2)
  - The conversion overflow flag is set when the ADC updates MEMRESx before the previous sample is read by the CPU or DMA
  - The conversion underflow flag is set when the CPU or DMA reads the MEMRESx register before the next conversion result is available
- Sequence Conversion and Repeat Sequence Conversion
  - Configure STARTADD bits to select the first MEMCTL in the sequence
  - Configure ENDADD bits to select the last MEMCTL in the sequence
    - MEMCTLx **is correlated to** MEMRESIFGx
  - Configure each MEMCTLx CHANSEL bits to select the desired ADC channels
  - Conversion data is available in MEMRESx – MEMRESIFGx can be set to generate a CPU interrupt (INT_EVENT0/1) or the DMA trigger
  - The conversion overflow flag is set when the ADC updates MEMRESx before the previous sample is read by the CPU or DMA (INT_EVENT2)
  - The conversion underflow flag is set when the CPU or DMA reads the MEMRESx register before the next conversion result is available

Note

For DMA based operation, the MEMCTL start address should be smaller than the end address for single sequence conversion as DMA source does not roll back. Repeat sequence conversion mode does not support DMA based data transfer because the DMA does not support circular addressing mode.

24.3.13.2.2 DMA/CPU Operation in FIFO Mode (FIFOEN=1)

- Single Conversion and Repeat Single Conversion
  - Configure STARTADD bits to select the desired MEMCTLx register
    - MEMCTLx **is NOT correlated to** MEMRESx
    - MEMRESx **is correlated to** MEMRESIFGx
  - Configure MEMCTL CHANSEL bits to select the desired ADC channel
  - Conversion data is loaded sequentially into MEMRES0,1,2,….N (organized as a FIFO)
  - The CPU or DMA must read ADC samples from the dedicated FIFODATA register and not from MEMRES registers directly
    - Data in the FIFO is always compacted with two samples and provided as 32-bit data upon a FIFODATA read by CPU or DMA
  - MEMRESIFGx can be used as a threshold condition to generate a CPU interrupt or DMA trigger
    - For full use of the FIFO, the last MEMRESIFG can be used
  - The conversion overflow flag is set when the ADC updates MEMRESx before the previous sample is read by the CPU or DMA
  - The conversion underflow flag is set when the CPU or DMA reads the FIFODATA register before the conversion result is available in the MEMRESx registers

Note

Single conversion mode with FIFO enabled is not recommended for CPU or DMA based operation. This leads to underflow condition and unwanted 16-bit data has to be discarded by software.

Additionally, **when using FIFO mode, do not use comparator mode described in section 1.3.13.1.**

- Sequence Conversion and Repeat Sequence Conversion

- Configure STARTADD bits to select the first MEMCTL in the sequence
- Configure ENDADD bits to select the last MEMCTL in the sequence
  - MEMCTLx **is NOT correlated to** MEMRESx
  - MEMRESx **is correlated to** MEMRESIFGx
- Configure each MEMCTLx CHANSEL bits to select the desired ADC channels
- Conversion data is loaded sequentially into MEMRES0,1,2,….N (organized as a FIFO)
- The CPU or DMA must read ADC samples from the dedicated FIFODATA register and not from MEMRES registers directly
  - Data in the FIFO is always compacted with two samples and provided as 32-bit data upon a FIFODATA read by CPU or DMA
- MEMRESIFGx can be used as a threshold condition to generate a CPU interrupt or DMA trigger
  - For full use of the FIFO, the last MEMRESIFG can be used
- The conversion overflow flag is set when the ADC updates MEMRESx before the previous sample is read by the CPU or DMA

24.3.13.2.3 DMA/CPU Operation Summary Matrix

Table 24-8. DMA/CPU Operation Summary Matrix

Conversion Mode	FIFO Disabled (FIFOEN=0) Samples not compacted. Read from MEMRESx registers directly		FIFO Enabled (FIFOEN=1) Samples always compacted Read from FIFODAT register only	
	CPU Read/Write	DMA Read/Write	CPU Read/Write	DMA Read/Write
Single	Supported	Supported	Not recommended Underflow flag is set Ignore unwanted 16 bits	Not recommended Underflow flag is set Ignore unwanted 16 bits
Repeat Single	Supported	Supported	Supported MEMRESIFG=CPU interrupt FIFODATA read in 32 bits	Supported MEMRESIFG=DMA trigger FIFODATA read in 32 bits
Sequence	Supported	Supported	Supported MEMRESIFG=CPU interrupt FIFODATA read in 32 bits	Supported MEMRESIFG=DMA trigger FIFODATA read in 32 bits
Repeat Sequence	Supported	Not Supported	Supported MEMRESIFG=CPU interrupt FIFODATA read in 32 bits	Supported MEMRESIFG=DMA trigger FIFODATA read in 32 bits

24.3.13.3 Ad-hoc Single Conversion

A mechanism to allow ADC to perform ad-hoc single conversions (ASC) without affecting the scheduled conversions is provided. The ADC sequencer slots the ASC request at a time when it finds an idle window in the middle of scheduled conversions without affecting the timing integrity of the scheduled conversions.

This is requested via CTL3 register which has fields for specifying the ADC channel number, voltage reference option and sample period for conversion. Any write to this register is treated as ad-hoc single conversion request by the sequencer. There is a separate result register available to store the data for ad-hoc single conversion (ASCRES). This is a dedicated register for ad-hoc single conversion operation which is different than result registers/FIFO available to store results from conversion on sensor channels.

Once software writes into ASC configuration register for ad-hoc single conversion there is a status bit that indicates the ASC is active (ASCACT) and goes low once the ASC operation is completed.

When the ASC operation is completed, an interrupt flag ASC done (ASCDONE) is set that can be unmasked by software to read the ASC result in the interrupt service routine.

Software can write into ASC configuration register at any time in ad-hoc manner and that request is registered by the sequencer and serviced at a suitable time.

Figure 24-4 shows the ADC sequencer state-machine for ASC operation.

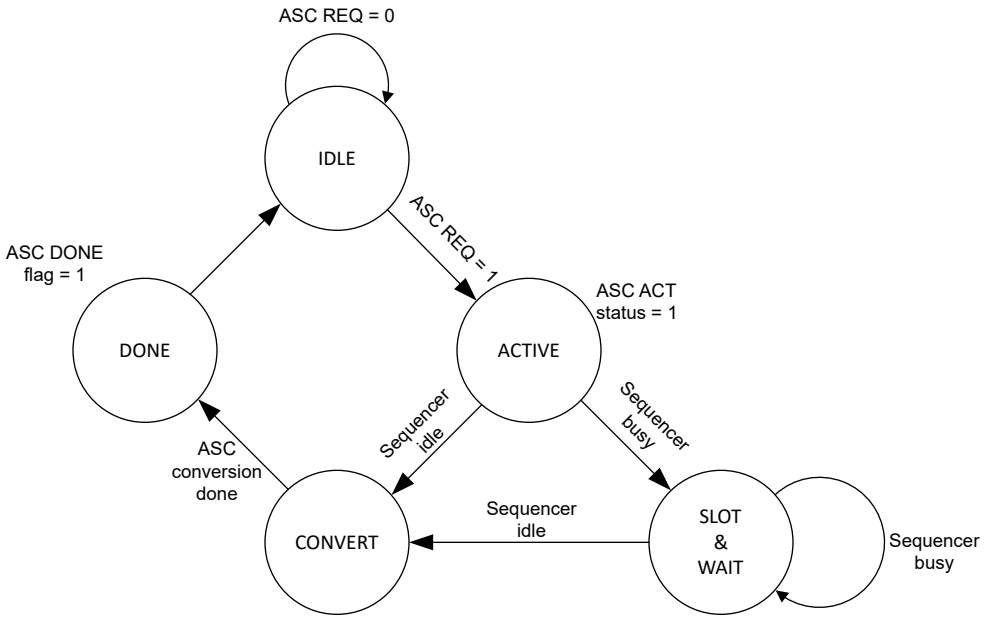

Figure 24-4. ADC Sequencer State-Machine for ASC Operation

Repeat Single Channel Mode and ASC Request

- When the sequencer operates in repeat single channel with sample trigger policy as auto-next, then the selected sensor channel is converted back to back continuously and the ASC request is pended by the sequencer and it is taken up and serviced only when the software stops repeat single channel conversion. When the sample trigger policy is trigger-next, then upon ASC request, the sequencer tries to schedule the ASC operation at the end of ongoing conversion (EOC - End of Conversion).
- It starts ASC operation and will complete it successfully if the scheduled trigger on sensor channel does not arrive in between.
- If the scheduled trigger is received in the middle of ASC operation, then ASC conversion is completed first and then the scheduled conversion is performed.
- If sequencer is not successful in completing ASC operation in the middle of scheduled conversions, then it will be serviced only when the software stops repeat single channel conversion.

Sequence of Channels mode and ASC Request

- In the case of sequence of channels operation with sample trigger policy as auto-next for all channels in the sequence, the ASC request will be slotted at the end of sequence and completed.
- If the sample trigger policy is trigger-next for one or more channels in the sequence, then sequencer tries to schedule the ASC operation at EOC of channel with trigger next policy set.
- If it can't complete ASC conversion successfully due to arrival of scheduled trigger then ASC operation is taken up and completed at the end after conversion of all channels in the sequence are completed.

Repeat Sequence of Channels Mode and ASC Request

- In the case of repeat sequence of channels operation with sample trigger policy as auto-next for all channels in the sequence, the ASC request will be slotted and completed when repeat sequence operation is stopped by software.
- If the sample trigger policy is trigger-next for one or more channels in the sequence, then sequencer tries to schedule the ASC operation at EOC of channel with trigger next policy set.

- If it can't complete ASC conversion successfully due to arrival of scheduled trigger then ASC operation is taken up and completed when the repeat sequence operation is stopped by software.

24.4 ADC Registers

Table 24-9 lists the memory-mapped registers for the ADC registers. All register offset addresses not listed in Table 24-9 should be considered as reserved locations and the register contents should not be modified.

Table 24-9. ADC Registers

Offset	Acronym	Register Name	Section
1020h	INTEVT0IDX	Interrupt Priority Index	Section 24.4.1
1028h	INTEVT0BM	Internal Event 0 Interrupt Mask	Section 24.4.2
1030h	INTEVT0RIS	Internal Event Raw Interrupt Status	Section 24.4.3
1038h	INTEVT0MIS	Masked Interrupt Status	Section 24.4.4
1040h	INTEVT0SET	Interrupt Set Register	Section 24.4.5
1048h	INTEVT0CLR	Interrupt Clear Register	Section 24.4.6
1050h	INTEVT1IDX	Interrupt Priority Index	Section 24.4.7
1058h	INTEVT1BM	Interrupt Mask Control	Section 24.4.8
1060h	INTEVT1RIS	Raw Interrupt Status	Section 24.4.9
1068h	INTEVT1MIS	Masked Interrupt Status	Section 24.4.10
1070h	INTEVT1SET	Interrupt Set Control	Section 24.4.11
1078h	INTEVT1CLR	Interrupt Clear Register	Section 24.4.12
1080h	INTEVT2IDX	Interrupt Priority Index	Section 24.4.13
1088h	INTEVT2BM	Event Interrupt Mask	Section 24.4.14
1090h	INTEVT2RIS	Raw Interrupt Status	Section 24.4.15
1098h	INTEVT2MIS	Masked Interrupt Status	Section 24.4.16
10A0h	INTEVT2SET	Interrupt Set Register	Section 24.4.17
10A8h	INTEVT2CLR	Interrupt Clear Register	Section 24.4.18
10E0h	EVTMOD	Event Handling Mode	Section 24.4.19
1100h	CTL0	Main Control	Section 24.4.20
1104h	CTL1	Control Register	Section 24.4.21
1108h	CTL2	Sequence Control Register	Section 24.4.22
110Ch	CTL3	Single Conversion Configuration	Section 24.4.23
1114h	SCOMP0	Sample Time Configuration	Section 24.4.24
1118h	SCOMP1	Sample Time Control	Section 24.4.25
111Ch	REFCFG	Reference Buffer Configuration	Section 24.4.26
1148h	WCLOW	Low Threshold Value	Section 24.4.27
1150h	WCHI	High Threshold Value	Section 24.4.28
1160h	FIFODATA	FIFO Data	Section 24.4.29
1170h	ASCRES	Analog Sequence Controller Result	Section 24.4.30
1180h	MEMCTL_0	Sequence memory 0 to memory 31 control registers.	Section 24.4.31
1184h	MEMCTL_1	Sequence memory 0 to memory 31 control registers.	Section 24.4.32
1188h	MEMCTL_2	Sequence memory 0 to memory 31 control registers.	Section 24.4.33
118Ch	MEMCTL_3	Sequence memory 0 to memory 31 control registers.	Section 24.4.34
1190h	MEMCTL_4	Sequence memory 0 to memory 31 control registers.	Section 24.4.35
1194h	MEMCTL_5	Sequence memory 0 to memory 31 control registers.	Section 24.4.36
1280h	MEMRES_0	Memory Results Register	Section 24.4.37
1284h	MEMRES_1	Memory Results Register	Section 24.4.38
1288h	MEMRES_2	Memory Results Register	Section 24.4.39
128Ch	MEMRES_3	Memory Results Register	Section 24.4.40
1290h	MEMRES_4	Memory Results Register	Section 24.4.41

Table 24-9. ADC Registers (continued)

Offset	Acronym	Register Name	Section
1294h	MEMRES_5	Memory Results Register	Section 24.4.42
1298h	MEMRES_6	Memory Results Register	Section 24.4.43
129Ch	MEMRES_7	Memory Results Register	Section 24.4.44
12A0h	MEMRES_8	Memory Results Register	Section 24.4.45
12A4h	MEMRES_9	Memory Results Register	Section 24.4.46
12A8h	MEMRES_10	Memory Results Register	Section 24.4.47
12ACh	MEMRES_11	Memory Results Register	Section 24.4.48
12B0h	MEMRES_12	Memory Results Register	Section 24.4.49
12B4h	MEMRES_13	Memory Results Register	Section 24.4.50
12B8h	MEMRES_14	Memory Results Register	Section 24.4.51
12BCh	MEMRES_15	Memory Results Register	Section 24.4.52
1340h	STA	Status Register	Section 24.4.53
1F14h	CONVCTL	Conversion Control	Section 24.4.54
1F18h	CTRL	Fuse Control	Section 24.4.55
1F1Ch	MODCTL	Mode Control	Section 24.4.56
1F20h	INTCHCTL	Internal Channel Control	Section 24.4.57
2000h	CLKCFG	Clock Enable	Section 24.4.58

Complex bit access types are encoded to fit into small table cells. Table 24-10 shows the codes that are used for access types in this section.

Table 24-10. ADC Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

24.4.1 INTEVT0IDX Register (Offset = 1020h) [Reset = 00000000h]

INTEVT0IDX is shown in Table 24-11.

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INTERNAL EVENT 0 IRQ IDX This register provides the highest priority enabled interrupt index. 0x0 means no event pending. Interrupt 1 is the highest priority, 2 next highest, 4, 8, ... 2^{31} is the least priority. That is, the least bit position that is set to 1 denotes the highest priority pending interrupt. The priority order is fixed. However, users can implement their own prioritization schemes using other registers that expose the full set of interrupts that have occurred. On each read, only one interrupt is indicated. On a read, the current interrupt (highest priority) is automatically cleared by the hardware and the corresponding interrupt flag in the RIS and MIS are cleared as well. After a read from the CPU (not from the debug interface), the register must be updated with the next highest priority interrupt, if none are pending, then it should display 0x0.

Table 24-11. INTEVT0IDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	
9-0	STAT	R	0h	Interrupt index status 00h = No bit is set means there is no pending interrupt request 01h = MEMRESx overflow interrupt 02h = Sequence Conversion time overflow interrupt 03h = High threshold compare interrupt 04h = Low threshold compare interrupt 05h = Primary Sequence In range comparator interrupt 6h = DMA done interrupt, generated on DMA transfer completion, 07h = MEMRESx underflow interrupt 9h = MEMRES0 data loaded interrupt Ah = MEMRES1 data loaded interrupt Bh = MEMRES2 data loaded interrupt Ch = MEMRES3 data loaded interrupt Dh = MEMRES4 data loaded interrupt Eh = MEMRES5 data loaded interrupt Fh = MEMRES6 data loaded interrupt 10h = MEMRES7 data loaded interrupt 11h = MEMRES8 data loaded interrupt 12h = MEMRES9 data loaded interrupt 13h = MEMRES10 data loaded interrupt 14h = MEMRES11 data loaded interrupt 15h = MEMRES12 data loaded interrupt 16h = MEMRES13 data loaded interrupt 17h = MEMRES14 data loaded interrupt 18h = MEMRES15 data loaded interrupt 19h = MEMRES16 data loaded interrupt 1Ah = MEMRES17 data loaded interrupt 1Bh = MEMRES18 data loaded interrupt 1Ch = MEMRES19 data loaded interrupt 1Dh = MEMRES20 data loaded interrupt 1Eh = MEMRES21 data loaded interrupt 1Fh = MEMRES22 data loaded interrupt 20h = MEMRES23 data loaded interrupt

24.4.2 INTEVT0BM Register (Offset = 1028h) [Reset = 00000000h]

INTEVT0BM is shown in Table 24-12.

Return to the Summary Table.

INTERNAL EVENT 0 IRQ MASK Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Table 24-12. INTEVT0BM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	0h	
23	MEMRESIFG15	R/W	0h	Raw interrupt status for MEMRES15. This bit is set to 1 when MEMRES15 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
22	MEMRESIFG14	R/W	0h	Raw interrupt status for MEMRES14. This bit is set to 1 when MEMRES14 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
21	MEMRESIFG13	R/W	0h	Raw interrupt status for MEMRES13. This bit is set to 1 when MEMRES13 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
20	MEMRESIFG12	R/W	0h	Raw interrupt status for MEMRES12. This bit is set to 1 when MEMRES12 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
19	MEMRESIFG11	R/W	0h	Raw interrupt status for MEMRES11. This bit is set to 1 when MEMRES11 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
18	MEMRESIFG10	R/W	0h	Raw interrupt status for MEMRES10. This bit is set to 1 when MEMRES10 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
17	MEMRESIFG9	R/W	0h	Raw interrupt status for MEMRES9. This bit is set to 1 when MEMRES9 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
16	MEMRESIFG8	R/W	0h	Raw interrupt status for MEMRES8. This bit is set to 1 when MEMRES8 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
15	MEMRESIFG7	R/W	0h	Raw interrupt status for MEMRES7. This bit is set to 1 when MEMRES7 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
14	MEMRESIFG6	R/W	0h	Raw interrupt status for MEMRES6. This bit is set to 1 when MEMRES6 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.

Table 24-12. INTEVT0BM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	MEMRESIFG5	R/W	0h	Raw interrupt status for MEMRES5. This bit is set to 1 when MEMRES5 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
12	MEMRESIFG4	R/W	0h	Raw interrupt status for MEMRES4. This bit is set to 1 when MEMRES4 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
11	MEMRESIFG3	R/W	0h	Raw interrupt status for MEMRES3. This bit is set to 1 when MEMRES3 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
10	MEMRESIFG2	R/W	0h	Raw interrupt status for MEMRES2. This bit is set to 1 when MEMRES2 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
9	MEMRESIFG1	R/W	0h	Raw interrupt status for MEMRES1. This bit is set to 1 when MEMRES1 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
8	MEMRESIFG0	R/W	0h	Raw interrupt status for MEMRES0. This bit is set to 1 when MEMRES0 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
7	RESERVED	R/W	0h	
6	UVIFG	R/W	0h	Raw interrupt flag for MEMRESx underflow. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
5	DMADONE	R/W	0h	Raw interrupt flag for DMADONE. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
4	INIFG	R/W	0h	Mask INIFG in MIS_EX register. 0h = Interrupt is not pending. 1h = Interrupt is pending.
3	LOFG	R/W	0h	LOW FG Raw interrupt flag for the MEMRESx result register being below than the WCLOWx threshold of the window comparator. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
2	HIFG	R/W	0h	Raw interrupt flag for the MEMRESx result register being higher than the WCHIGHx threshold of the window comparator. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
1	TOVIFG	R/W	0h	Raw interrupt flag for sequence conversion timeout overflow. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.

Table 24-12. INTEVT0BM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	OVIFG	R/W	0h	Raw interrupt flag for MEMRESx overflow. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.

24.4.3 INTEVT0RIS Register (Offset = 1030h) [Reset = 00000000h]

INTEVT0RIS is shown in Table 24-13.

Return to the Summary Table.

INTERNAL EVENT 0 RAW IRQ STATUS Raw interrupt status. Reflects all pending interrupts, regardless of masking. The INT_EVENT0_RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Table 24-13. INTEVT0RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	
23	MEMRESIFG15	R	0h	Raw interrupt status for MEMRES15. This bit is set to 1 when MEMRES15 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
22	MEMRESIFG14	R	0h	Raw interrupt status for MEMRES14. This bit is set to 1 when MEMRES14 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
21	MEMRESIFG13	R	0h	Raw interrupt status for MEMRES13. This bit is set to 1 when MEMRES13 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
20	MEMRESIFG12	R	0h	Raw interrupt status for MEMRES12. This bit is set to 1 when MEMRES12 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
19	MEMRESIFG11	R	0h	Raw interrupt status for MEMRES11. This bit is set to 1 when MEMRES11 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
18	MEMRESIFG10	R	0h	Raw interrupt status for MEMRES10. This bit is set to 1 when MEMRES10 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
17	MEMRESIFG9	R	0h	Raw interrupt status for MEMRES9. This bit is set to 1 when MEMRES9 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
16	MEMRESIFG8	R	0h	Raw interrupt status for MEMRES8. This bit is set to 1 when MEMRES8 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
15	MEMRESIFG7	R	0h	Raw interrupt status for MEMRES7. This bit is set to 1 when MEMRES7 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
14	MEMRESIFG6	R	0h	Raw interrupt status for MEMRES6. This bit is set to 1 when MEMRES6 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.

Table 24-13. INTEVT0RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	MEMRESIFG5	R	0h	Raw interrupt status for MEMRES5. This bit is set to 1 when MEMRES5 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
12	MEMRESIFG4	R	0h	Raw interrupt status for MEMRES4. This bit is set to 1 when MEMRES4 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
11	MEMRESIFG3	R	0h	Raw interrupt status for MEMRES3. This bit is set to 1 when MEMRES3 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
10	MEMRESIFG2	R	0h	Raw interrupt status for MEMRES2. This bit is set to 1 when MEMRES2 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
9	MEMRESIFG1	R	0h	Raw interrupt status for MEMRES1. This bit is set to 1 when MEMRES1 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
8	MEMRESIFG0	R	0h	Raw interrupt status for MEMRES0. This bit is set to 1 when MEMRES0 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
7	RESERVED	R	0h	
6	UVIFG	R	0h	Raw interrupt flag for MEMRESx underflow. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
5	DMADONE	R	0h	Raw interrupt flag for DMADONE. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
4	INIFG	R	0h	Mask INIFG in MIS_EX register. 0h = Interrupt is not pending. 1h = Interrupt is pending.
3	LOFG	R	0h	LOW FG Raw interrupt flag for the MEMRESx result register being below than the WCLOWx threshold of the window comparator. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
2	HIFG	R	0h	HIGH FG Raw interrupt flag for the MEMRESx result register being higher than the WCHIGHx threshold of the window comparator. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
1	TOVIFG	R	0h	Raw interrupt flag for sequence conversion timeout overflow. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.

Table 24-13. INTEVT0RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	OVIFG	R	0h	Raw interrupt flag for MEMRESx overflow. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.

24.4.4 INTEVT0MIS Register (Offset = 1038h) [Reset = 00000000h]

INTEVT0MIS is shown in Table 24-14.

Return to the Summary Table.

INTERNAL EVENT 0 MASKED IRQ STATUS Masked interrupt status. This is an AND of the IMASK and RIS registers.

Table 24-14. INTEVT0MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	
23	MEMRESIFG15	R	0h	Raw interrupt status for MEMRES15. This bit is set to 1 when MEMRES15 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
22	MEMRESIFG14	R	0h	Raw interrupt status for MEMRES14. This bit is set to 1 when MEMRES14 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
21	MEMRESIFG13	R	0h	Raw interrupt status for MEMRES13. This bit is set to 1 when MEMRES13 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
20	MEMRESIFG12	R	0h	Raw interrupt status for MEMRES12. This bit is set to 1 when MEMRES12 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
19	MEMRESIFG11	R	0h	Raw interrupt status for MEMRES11. This bit is set to 1 when MEMRES11 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
18	MEMRESIFG10	R	0h	Raw interrupt status for MEMRES10. This bit is set to 1 when MEMRES10 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
17	MEMRESIFG9	R	0h	Raw interrupt status for MEMRES9. This bit is set to 1 when MEMRES9 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
16	MEMRESIFG8	R	0h	Raw interrupt status for MEMRES8. This bit is set to 1 when MEMRES8 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
15	MEMRESIFG7	R	0h	Raw interrupt status for MEMRES7. This bit is set to 1 when MEMRES7 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
14	MEMRESIFG6	R	0h	Raw interrupt status for MEMRES6. This bit is set to 1 when MEMRES6 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.

Table 24-14. INTEVT0MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	MEMRESIFG5	R	0h	Raw interrupt status for MEMRES5. This bit is set to 1 when MEMRES5 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
12	MEMRESIFG4	R	0h	Raw interrupt status for MEMRES4. This bit is set to 1 when MEMRES4 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
11	MEMRESIFG3	R	0h	Raw interrupt status for MEMRES3. This bit is set to 1 when MEMRES3 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
10	MEMRESIFG2	R	0h	Raw interrupt status for MEMRES2. This bit is set to 1 when MEMRES2 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
9	MEMRESIFG1	R	0h	Raw interrupt status for MEMRES1. This bit is set to 1 when MEMRES1 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
8	MEMRESIFG0	R	0h	Raw interrupt status for MEMRES0. This bit is set to 1 when MEMRES0 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 11 0h = No new data ready. 1h = A new data is ready to be read.
7	RESERVED	R	0h	
6	UVIFG	R	0h	Raw interrupt flag for MEMRESx underflow. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
5	DMADONE	R	0h	Raw interrupt flag for DMADONE. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
4	INIFG	R	0h	Mask INIFG in MIS_EX register. 0h = Interrupt is not pending. 1h = Interrupt is pending.
3	LOFG	R	0h	LOW FG Raw interrupt flag for the MEMRESx result register being below than the WCLOWx threshold of the window comparator. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
2	HIFG	R	0h	HIGH FG Raw interrupt flag for the MEMRESx result register being higher than the WCHIGHx threshold of the window comparator. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
1	TOVIFG	R	0h	Raw interrupt flag for sequence conversion timeout overflow. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.

Table 24-14. INTEVT0MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	OVIFG	R	0h	Raw interrupt flag for MEMRESx overflow. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.

24.4.5 INTEVT0SET Register (Offset = 1040h) [Reset = 00000000h]

INTEVT0SET is shown in Table 24-15.

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INTERNAL EVENT 0 IRQ SET Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in INT_EVENT0_ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Table 24-15. INTEVT0SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	0h	
23	MEMRESIFG15	W	0h	Raw interrupt status for MEMRES15. This bit is set to 1 when MEMRES15 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
22	MEMRESIFG14	W	0h	Raw interrupt status for MEMRES14. This bit is set to 1 when MEMRES14 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
21	MEMRESIFG13	W	0h	Raw interrupt status for MEMRES13. This bit is set to 1 when MEMRES13 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
20	MEMRESIFG12	W	0h	Raw interrupt status for MEMRES12. This bit is set to 1 when MEMRES12 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
19	MEMRESIFG11	W	0h	Raw interrupt status for MEMRES11. This bit is set to 1 when MEMRES11 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
18	MEMRESIFG10	W	0h	Raw interrupt status for MEMRES10. This bit is set to 1 when MEMRES10 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
17	MEMRESIFG9	W	0h	Raw interrupt status for MEMRES9. This bit is set to 1 when MEMRES9 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
16	MEMRESIFG8	W	0h	Raw interrupt status for MEMRES8. This bit is set to 1 when MEMRES8 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
15	MEMRESIFG7	W	0h	Raw interrupt status for MEMRES7. This bit is set to 1 when MEMRES7 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
14	MEMRESIFG6	W	0h	Raw interrupt status for MEMRES6. This bit is set to 1 when MEMRES6 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.

Table 24-15. INTEVT0SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	MEMRESIFG5	W	0h	Raw interrupt status for MEMRES5. This bit is set to 1 when MEMRES5 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
12	MEMRESIFG4	W	0h	Raw interrupt status for MEMRES4. This bit is set to 1 when MEMRES4 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
11	MEMRESIFG3	W	0h	Raw interrupt status for MEMRES3. This bit is set to 1 when MEMRES3 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
10	MEMRESIFG2	W	0h	Raw interrupt status for MEMRES2. This bit is set to 1 when MEMRES2 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
9	MEMRESIFG1	W	0h	Raw interrupt status for MEMRES1. This bit is set to 1 when MEMRES1 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
8	MEMRESIFG0	W	0h	Raw interrupt status for MEMRES0. This bit is set to 1 when MEMRES0 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
7	RESERVED	R/W	0h	
6	UVIFG	W	0h	Raw interrupt flag for MEMRESx underflow. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
5	DMADONE	W	0h	Raw interrupt flag for DMADONE. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
4	INIFG	W	0h	Mask INIFG in MIS_EX register. 0h = Interrupt is not pending. 1h = Interrupt is pending.
3	LOFG	W	0h	LOW FG Raw interrupt flag for the MEMRESx result register being below than the WCLOWx threshold of the window comparator. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
2	HIFG	W	0h	HIGH FG Raw interrupt flag for the MEMRESx result register being higher than the WCHIGHx threshold of the window comparator. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
1	TOVIFG	W	0h	Raw interrupt flag for sequence conversion timeout overflow. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.

Table 24-15. INTEVT0SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	OVIFG	W	0h	Raw interrupt flag for MEMRESx overflow. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.

24.4.6 INTEVT0CLR Register (Offset = 1048h) [Reset = 00000000h]

INTEVT0CLR is shown in Table 24-16.

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INTERNAL EVENT 0 IRQ CLEAR Interrupt clear. Write a 1 to clear corresponding Interrupt.

Table 24-16. INTEVT0CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	0h	
23	MEMRESIFG15	W	0h	Raw interrupt status for MEMRES15. This bit is set to 1 when MEMRES15 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
22	MEMRESIFG14	W	0h	Raw interrupt status for MEMRES14. This bit is set to 1 when MEMRES14 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
21	MEMRESIFG13	W	0h	Raw interrupt status for MEMRES13. This bit is set to 1 when MEMRES13 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
20	MEMRESIFG12	W	0h	Raw interrupt status for MEMRES12. This bit is set to 1 when MEMRES12 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
19	MEMRESIFG11	W	0h	Raw interrupt status for MEMRES11. This bit is set to 1 when MEMRES11 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
18	MEMRESIFG10	W	0h	Raw interrupt status for MEMRES10. This bit is set to 1 when MEMRES10 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
17	MEMRESIFG9	W	0h	Raw interrupt status for MEMRES9. This bit is set to 1 when MEMRES9 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
16	MEMRESIFG8	W	0h	Raw interrupt status for MEMRES8. This bit is set to 1 when MEMRES8 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
15	MEMRESIFG7	W	0h	Raw interrupt status for MEMRES7. This bit is set to 1 when MEMRES7 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
14	MEMRESIFG6	W	0h	Raw interrupt status for MEMRES6. This bit is set to 1 when MEMRES6 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.

Table 24-16. INTEVT0CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	MEMRESIFG5	W	0h	Raw interrupt status for MEMRES5. This bit is set to 1 when MEMRES5 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
12	MEMRESIFG4	W	0h	Raw interrupt status for MEMRES4. This bit is set to 1 when MEMRES4 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
11	MEMRESIFG3	W	0h	Raw interrupt status for MEMRES3. This bit is set to 1 when MEMRES3 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
10	MEMRESIFG2	W	0h	Raw interrupt status for MEMRES2. This bit is set to 1 when MEMRES2 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
9	MEMRESIFG1	W	0h	Raw interrupt status for MEMRES1. This bit is set to 1 when MEMRES1 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
8	MEMRESIFG0	W	0h	Raw interrupt status for MEMRES0. This bit is set to 1 when MEMRES0 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
7	RESERVED	R/W	0h	
6	UVIFG	W	0h	Raw interrupt flag for MEMRESx underflow. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
5	DMADONE	W	0h	Raw interrupt flag for DMADONE. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
4	INIFG	W	0h	Mask INIFG in MIS_EX register. 0h = Interrupt is not pending. 1h = Interrupt is pending.
3	LOFG	W	0h	LOW FG Raw interrupt flag for the MEMRESx result register being below than the WCLOWx threshold of the window comparator. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
2	HIFG	W	0h	HIGH FG Raw interrupt flag for the MEMRESx result register being higher than the WCHIGHx threshold of the window comparator. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
1	TOVIFG	W	0h	Raw interrupt flag for sequence conversion timeout overflow. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.

Table 24-16. INTEVT0CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	OVIFG	W	0h	Raw interrupt flag for MEMRESx overflow. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.

24.4.7 INTEVT1IDX Register (Offset = 1050h) [Reset = 00000000h]

INTEVT1IDX is shown in Table 24-17.

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INTERNAL EVENT 1 IRQ IDX This register provides the highest priority enabled interrupt index. 0x0 means no event pending. Interrupt 1 is the highest priority, 2 next highest, 4, 8, ... 2^{31} is the least priority. That is, the least bit position that is set to 1 denotes the highest priority pending interrupt. The priority order is fixed. However, users can implement their own prioritization schemes using other registers that expose the full set of interrupts that have occurred. On each read, only one interrupt is indicated. On a read, the current interrupt (highest priority) is automatically cleared by the hardware and the corresponding interrupt flag in the RIS and MIS are cleared as well. After a read from the CPU (not from the debug interface), the register must be updated with the next highest priority interrupt, if none are pending, then it should display 0x0.

Table 24-17. INTEVT1IDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	
9-0	STAT	R	0h	Interrupt index status 00h = No bit is set means there is no pending interrupt request 03h = High threshold compare interrupt 04h = Low threshold compare interrupt 05h = Primary Sequence In range comparator interrupt 9h = MEMRES0 data loaded interrupt

24.4.8 INTEVT1BM Register (Offset = 1058h) [Reset = 00000000h]

INTEVT1BM is shown in Table 24-18.

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INTERNAL EVENT 1 IRQ MASK Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Table 24-18. INTEVT1BM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	0h	
8	MEMRESIFG0	R/W	0h	Raw interrupt status for MEMRES0. This bit is set to 1 when MEMRES0 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
7-5	RESERVED	R/W	0h	
4	INIFG	R/W	0h	Mask INIFG in MIS_EX register. 0h = Interrupt is not pending. 1h = Interrupt is pending.
3	LOFG	R/W	0h	LOW FG Raw interrupt flag for the MEMRESx result register being below than the WCLOWx threshold of the window comparator. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
2	HIFG	R/W	0h	HIGH FG Raw interrupt flag for the MEMRESx result register being higher than the WCHIGHx threshold of the window comparator. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
1-0	RESERVED	R/W	0h	

24.4.9 INTEVT1RIS Register (Offset = 1060h) [Reset = 00000000h]

INTEVT1RIS is shown in Table 24-19.

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INTERNAL EVENT 1 RAW IRQ STATUS Raw interrupt status. Reflects all pending interrupts, regardless of masking. The INT_EVENT1_RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Table 24-19. INTEVT1RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8	MEMRESIFG0	R	0h	Raw interrupt status for MEMRES0. This bit is set to 1 when MEMRES0 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
7-5	RESERVED	R	0h	
4	INIFG	R	0h	Mask INIFG in MIS_EX register. 0h = Interrupt is not pending. 1h = Interrupt is pending.
3	LOFG	R	0h	LOW FG Raw interrupt flag for the MEMRESx result register being below than the WCLOWx threshold of the window comparator. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
2	HIFG	R	0h	HIGH FG Raw interrupt flag for the MEMRESx result register being higher than the WCHIGHx threshold of the window comparator. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
1-0	RESERVED	R	0h	

24.4.10 INTEVT1MIS Register (Offset = 1068h) [Reset = 00000000h]

INTEVT1MIS is shown in Table 24-20.

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INTERNAL EVENT 1 MASKED IRQ STATUS Masked interrupt status. This is an AND of the IMASK and RIS registers.

Table 24-20. INTEVT1MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8	MEMRESIFG0	R	0h	Raw interrupt status for MEMRES0. This bit is set to 1 when MEMRES0 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
7-5	RESERVED	R	0h	
4	INIFG	R	0h	Mask INIFG in MIS_EX register. 0h = Interrupt is not pending. 1h = Interrupt is pending.
3	LOFG	R	0h	LOW FG Raw interrupt flag for the MEMRESx result register being below than the WCLOWx threshold of the window comparator. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
2	HIFG	R	0h	HIGH FG Raw interrupt flag for the MEMRESx result register being higher than the WCHIGHx threshold of the window comparator. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
1-0	RESERVED	R	0h	

24.4.11 INTEVT1SET Register (Offset = 1070h) [Reset = 00000000h]

INTEVT1SET is shown in Table 24-21.

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INTERNAL EVENT 1 IRQ SET Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in INT_EVENT1_ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Table 24-21. INTEVT1SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	0h	
8	MEMRESIFG0	W	0h	Raw interrupt status for MEMRES0. This bit is set to 1 when MEMRES0 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
7-5	RESERVED	R/W	0h	
4	INIFG	W	0h	Mask INIFG in MIS_EX register. 0h = Interrupt is not pending. 1h = Interrupt is pending.
3	LOFG	W	0h	LOW FG Raw interrupt flag for the MEMRESx result register being below than the WCLOWx threshold of the window comparator. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
2	HIFG	W	0h	HIGH FG Raw interrupt flag for the MEMRESx result register being higher than the WCHIGHx threshold of the window comparator. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
1-0	RESERVED	R/W	0h	

24.4.12 INTEVT1CLR Register (Offset = 1078h) [Reset = 00000000h]

INTEVT1CLR is shown in Table 24-22.

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INTERNAL EVENT 1 IRQ CLEAR Interrupt clear. Write a 1 to clear corresponding Interrupt.

Table 24-22. INTEVT1CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	0h	
8	MEMRESIFG0	W	0h	Raw interrupt status for MEMRES0. This bit is set to 1 when MEMRES0 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
7-5	RESERVED	R/W	0h	
4	INIFG	W	0h	Mask INIFG in MIS_EX register. 0h = Interrupt is not pending. 1h = Interrupt is pending.
3	LOFG	W	0h	LOW FG Raw interrupt flag for the MEMRESx result register being below than the WCLOWx threshold of the window comparator. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
2	HIFG	W	0h	HIGH FG Raw interrupt flag for the MEMRESx result register being higher than the WCHIGHx threshold of the window comparator. This bit is reset to 0 by IIDX read or when corresponding bit in ICLR_EX is set to 1. 0h = Interrupt is not pending. 1h = Interrupt is pending.
1-0	RESERVED	R/W	0h	

24.4.13 INTEVT2IDX Register (Offset = 1080h) [Reset = 00000000h]

INTEVT2IDX is shown in Table 24-23.

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INTERNAL EVENT 2 IRQ IDX This register provides the highest priority enabled interrupt index. 0x0 means no event pending. Interrupt 1 is the highest priority, 2 next highest, 4, 8, ... 2^{31} is the least priority. That is, the least bit position that is set to 1 denotes the highest priority pending interrupt. The priority order is fixed. However, users can implement their own prioritization schemes using other registers that expose the full set of interrupts that have occurred. On each read, only one interrupt is indicated. On a read, the current interrupt (highest priority) is automatically cleared by the hardware and the corresponding interrupt flag in the RIS and MIS are cleared as well. After a read from the CPU (not from the debug interface), the register must be updated with the next highest priority interrupt, if none are pending, then it should display 0x0.

Table 24-23. INTEVT2IDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	
9-0	STAT	R	0h	Interrupt index status 00h = No bit is set means there is no pending interrupt request 9h = MEMRES0 data loaded interrupt Ah = MEMRES1 data loaded interrupt Bh = MEMRES2 data loaded interrupt Ch = MEMRES3 data loaded interrupt Dh = MEMRES4 data loaded interrupt Eh = MEMRES5 data loaded interrupt Fh = MEMRES6 data loaded interrupt 10h = MEMRES7 data loaded interrupt 11h = MEMRES8 data loaded interrupt 12h = MEMRES9 data loaded interrupt 13h = MEMRES10 data loaded interrupt 14h = MEMRES11 data loaded interrupt 15h = MEMRES12 data loaded interrupt 16h = MEMRES13 data loaded interrupt 17h = MEMRES14 data loaded interrupt 18h = MEMRES15 data loaded interrupt 19h = MEMRES16 data loaded interrupt 1Ah = MEMRES17 data loaded interrupt 1Bh = MEMRES18 data loaded interrupt 1Ch = MEMRES19 data loaded interrupt 1Dh = MEMRES20 data loaded interrupt 1Eh = MEMRES21 data loaded interrupt 1Fh = MEMRES22 data loaded interrupt 20h = MEMRES23 data loaded interrupt

24.4.14 INTEVT2BM Register (Offset = 1088h) [Reset = 00000000h]

INTEVT2BM is shown in Table 24-24.

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INTERNAL EVENT 2 IRQ MASK Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Table 24-24. INTEVT2BM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	0h	
23	MEMRESIFG15	R/W	0h	Raw interrupt status for MEMRES15. This bit is set to 1 when MEMRES15 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
22	MEMRESIFG14	R/W	0h	Raw interrupt status for MEMRES14. This bit is set to 1 when MEMRES14 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
21	MEMRESIFG13	R/W	0h	Raw interrupt status for MEMRES13. This bit is set to 1 when MEMRES13 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
20	MEMRESIFG12	R/W	0h	Raw interrupt status for MEMRES12. This bit is set to 1 when MEMRES12 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
19	MEMRESIFG11	R/W	0h	Raw interrupt status for MEMRES11. This bit is set to 1 when MEMRES11 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
18	MEMRESIFG10	R/W	0h	Raw interrupt status for MEMRES10. This bit is set to 1 when MEMRES10 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
17	MEMRESIFG9	R/W	0h	Raw interrupt status for MEMRES9. This bit is set to 1 when MEMRES9 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
16	MEMRESIFG8	R/W	0h	Raw interrupt status for MEMRES8. This bit is set to 1 when MEMRES8 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
15	MEMRESIFG7	R/W	0h	Raw interrupt status for MEMRES7. This bit is set to 1 when MEMRES7 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
14	MEMRESIFG6	R/W	0h	Raw interrupt status for MEMRES6. This bit is set to 1 when MEMRES6 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.

Table 24-24. INTEVT2BM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	MEMRESIFG5	R/W	0h	Raw interrupt status for MEMRES5. This bit is set to 1 when MEMRES5 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
12	MEMRESIFG4	R/W	0h	Raw interrupt status for MEMRES4. This bit is set to 1 when MEMRES4 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
11	MEMRESIFG3	R/W	0h	Raw interrupt status for MEMRES3. This bit is set to 1 when MEMRES3 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
10	MEMRESIFG2	R/W	0h	Raw interrupt status for MEMRES2. This bit is set to 1 when MEMRES2 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
9	MEMRESIFG1	R/W	0h	Raw interrupt status for MEMRES1. This bit is set to 1 when MEMRES1 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
8	MEMRESIFG0	R/W	0h	Raw interrupt status for MEMRES0. This bit is set to 1 when MEMRES0 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
7-0	RESERVED	R/W	0h	

24.4.15 INTEVT2RIS Register (Offset = 1090h) [Reset = 00000000h]

INTEVT2RIS is shown in Table 24-25.

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INTERNAL EVENT 2 RAW IRQ STATUS Raw interrupt status. Reflects all pending interrupts, regardless of masking. The INT_EVENT2_RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Table 24-25. INTEVT2RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	
23	MEMRESIFG15	R	0h	Raw interrupt status for MEMRES15. This bit is set to 1 when MEMRES15 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
22	MEMRESIFG14	R	0h	Raw interrupt status for MEMRES14. This bit is set to 1 when MEMRES14 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
21	MEMRESIFG13	R	0h	Raw interrupt status for MEMRES13. This bit is set to 1 when MEMRES13 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
20	MEMRESIFG12	R	0h	Raw interrupt status for MEMRES12. This bit is set to 1 when MEMRES12 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
19	MEMRESIFG11	R	0h	Raw interrupt status for MEMRES11. This bit is set to 1 when MEMRES11 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
18	MEMRESIFG10	R	0h	Raw interrupt status for MEMRES10. This bit is set to 1 when MEMRES10 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
17	MEMRESIFG9	R	0h	Raw interrupt status for MEMRES9. This bit is set to 1 when MEMRES9 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
16	MEMRESIFG8	R	0h	Raw interrupt status for MEMRES8. This bit is set to 1 when MEMRES8 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
15	MEMRESIFG7	R	0h	Raw interrupt status for MEMRES7. This bit is set to 1 when MEMRES7 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
14	MEMRESIFG6	R	0h	Raw interrupt status for MEMRES6. This bit is set to 1 when MEMRES6 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.

Table 24-25. INTEVT2RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	MEMRESIFG5	R	0h	Raw interrupt status for MEMRES5. This bit is set to 1 when MEMRES5 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
12	MEMRESIFG4	R	0h	Raw interrupt status for MEMRES4. This bit is set to 1 when MEMRES4 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
11	MEMRESIFG3	R	0h	Raw interrupt status for MEMRES3. This bit is set to 1 when MEMRES3 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
10	MEMRESIFG2	R	0h	Raw interrupt status for MEMRES2. This bit is set to 1 when MEMRES2 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
9	MEMRESIFG1	R	0h	Raw interrupt status for MEMRES1. This bit is set to 1 when MEMRES1 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
8	MEMRESIFG0	R	0h	Raw interrupt status for MEMRES0. This bit is set to 1 when MEMRES0 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
7-0	RESERVED	R	0h	

24.4.16 INTEVT2MIS Register (Offset = 1098h) [Reset = 00000000h]

INTEVT2MIS is shown in Table 24-26.

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INTERNAL EVENT 2 MASKED IRQ STATUS Extension of Masked interrupt status. This is an AND of the IMASK and RIS registers.

Table 24-26. INTEVT2MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	
23	MEMRESIFG15	R	0h	Raw interrupt status for MEMRES15. This bit is set to 1 when MEMRES15 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
22	MEMRESIFG14	R	0h	Raw interrupt status for MEMRES14. This bit is set to 1 when MEMRES14 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
21	MEMRESIFG13	R	0h	Raw interrupt status for MEMRES13. This bit is set to 1 when MEMRES13 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
20	MEMRESIFG12	R	0h	Raw interrupt status for MEMRES12. This bit is set to 1 when MEMRES12 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
19	MEMRESIFG11	R	0h	Raw interrupt status for MEMRES11. This bit is set to 1 when MEMRES11 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
18	MEMRESIFG10	R	0h	Raw interrupt status for MEMRES10. This bit is set to 1 when MEMRES10 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
17	MEMRESIFG9	R	0h	Raw interrupt status for MEMRES9. This bit is set to 1 when MEMRES9 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
16	MEMRESIFG8	R	0h	Raw interrupt status for MEMRES8. This bit is set to 1 when MEMRES8 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
15	MEMRESIFG7	R	0h	Raw interrupt status for MEMRES7. This bit is set to 1 when MEMRES7 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
14	MEMRESIFG6	R	0h	Raw interrupt status for MEMRES6. This bit is set to 1 when MEMRES6 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.

Table 24-26. INTEVT2MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	MEMRESIFG5	R	0h	Raw interrupt status for MEMRES5. This bit is set to 1 when MEMRES5 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
12	MEMRESIFG4	R	0h	Raw interrupt status for MEMRES4. This bit is set to 1 when MEMRES4 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
11	MEMRESIFG3	R	0h	Raw interrupt status for MEMRES3. This bit is set to 1 when MEMRES3 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
10	MEMRESIFG2	R	0h	Raw interrupt status for MEMRES2. This bit is set to 1 when MEMRES2 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
9	MEMRESIFG1	R	0h	Raw interrupt status for MEMRES1. This bit is set to 1 when MEMRES1 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
8	MEMRESIFG0	R	0h	Raw interrupt status for MEMRES0. This bit is set to 1 when MEMRES0 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
7-0	RESERVED	R	0h	

24.4.17 INTEVT2SET Register (Offset = 10A0h) [Reset = 00000000h]

INTEVT2SET is shown in Table 24-27.

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INTERNAL EVENT 2 IRQ SET Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in INT_EVENT2_ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Table 24-27. INTEVT2SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	0h	
23	MEMRESIFG15	W	0h	Raw interrupt status for MEMRES15. This bit is set to 1 when MEMRES15 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
22	MEMRESIFG14	W	0h	Raw interrupt status for MEMRES14. This bit is set to 1 when MEMRES14 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
21	MEMRESIFG13	W	0h	Raw interrupt status for MEMRES13. This bit is set to 1 when MEMRES13 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
20	MEMRESIFG12	W	0h	Raw interrupt status for MEMRES12. This bit is set to 1 when MEMRES12 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
19	MEMRESIFG11	W	0h	Raw interrupt status for MEMRES11. This bit is set to 1 when MEMRES11 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
18	MEMRESIFG10	W	0h	Raw interrupt status for MEMRES10. This bit is set to 1 when MEMRES10 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
17	MEMRESIFG9	W	0h	Raw interrupt status for MEMRES9. This bit is set to 1 when MEMRES9 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
16	MEMRESIFG8	W	0h	Raw interrupt status for MEMRES8. This bit is set to 1 when MEMRES8 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
15	MEMRESIFG7	W	0h	Raw interrupt status for MEMRES7. This bit is set to 1 when MEMRES7 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
14	MEMRESIFG6	W	0h	Raw interrupt status for MEMRES6. This bit is set to 1 when MEMRES6 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.

Table 24-27. INTEVT2SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	MEMRESIFG5	W	0h	Raw interrupt status for MEMRES5. This bit is set to 1 when MEMRES5 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
12	MEMRESIFG4	W	0h	Raw interrupt status for MEMRES4. This bit is set to 1 when MEMRES4 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
11	MEMRESIFG3	W	0h	Raw interrupt status for MEMRES3. This bit is set to 1 when MEMRES3 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
10	MEMRESIFG2	W	0h	Raw interrupt status for MEMRES2. This bit is set to 1 when MEMRES2 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
9	MEMRESIFG1	W	0h	Raw interrupt status for MEMRES1. This bit is set to 1 when MEMRES1 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
8	MEMRESIFG0	W	0h	Raw interrupt status for MEMRES0. This bit is set to 1 when MEMRES0 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
7-0	RESERVED	R/W	0h	

24.4.18 INTEVT2CLR Register (Offset = 10A8h) [Reset = 00000000h]

INTEVT2CLR is shown in Table 24-28.

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INTERNAL EVENT 2 IRQ CLEAR Interrupt clear. Write a 1 to clear corresponding Interrupt.

Table 24-28. INTEVT2CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	0h	
23	MEMRESIFG15	W	0h	Raw interrupt status for MEMRES15. This bit is set to 1 when MEMRES15 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
22	MEMRESIFG14	W	0h	Raw interrupt status for MEMRES14. This bit is set to 1 when MEMRES14 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
21	MEMRESIFG13	W	0h	Raw interrupt status for MEMRES13. This bit is set to 1 when MEMRES13 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
20	MEMRESIFG12	W	0h	Raw interrupt status for MEMRES12. This bit is set to 1 when MEMRES12 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
19	MEMRESIFG11	W	0h	Raw interrupt status for MEMRES11. This bit is set to 1 when MEMRES11 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
18	MEMRESIFG10	W	0h	Raw interrupt status for MEMRES10. This bit is set to 1 when MEMRES10 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
17	MEMRESIFG9	W	0h	Raw interrupt status for MEMRES9. This bit is set to 1 when MEMRES9 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
16	MEMRESIFG8	W	0h	Raw interrupt status for MEMRES8. This bit is set to 1 when MEMRES8 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
15	MEMRESIFG7	W	0h	Raw interrupt status for MEMRES7. This bit is set to 1 when MEMRES7 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
14	MEMRESIFG6	W	0h	Raw interrupt status for MEMRES6. This bit is set to 1 when MEMRES6 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.

Table 24-28. INTEVT2CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	MEMRESIFG5	W	0h	Raw interrupt status for MEMRES5. This bit is set to 1 when MEMRES5 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
12	MEMRESIFG4	W	0h	Raw interrupt status for MEMRES4. This bit is set to 1 when MEMRES4 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
11	MEMRESIFG3	W	0h	Raw interrupt status for MEMRES3. This bit is set to 1 when MEMRES3 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
10	MEMRESIFG2	W	0h	Raw interrupt status for MEMRES2. This bit is set to 1 when MEMRES2 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
9	MEMRESIFG1	W	0h	Raw interrupt status for MEMRES1. This bit is set to 1 when MEMRES1 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
8	MEMRESIFG0	W	0h	Raw interrupt status for MEMRES0. This bit is set to 1 when MEMRES0 is loaded with a new conversion result. To clear this bit, corresponding bit in ICLR should be set to 1 0h = No new data ready. 1h = A new data is ready to be read.
7-0	RESERVED	R/W	0h	

24.4.19 EVTMOD Register (Offset = 10E0h) [Reset = 00000000h]

EVTMOD is shown in Table 24-29.

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EVENT MODE Event mode register. It is used to select whether each line is disabled, in software mode (software clears the RIS) or in hardware mode (hardware clears the RIS)

Table 24-29. EVTMOD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	
3-2	EVT1CFG	R/W	2h	EVENT 1 CONFIG Event line mode select for event corresponding to none.INT_EVENT1 0h = The interrupt or event line is disabled. 1h = The interrupt or event line is in software mode. Software must clear the RIS. 2h = The interrupt or event line is in hardware mode. The hardware (another module) clears automatically the associated RIS flag.
1-0	INT0CFG	R/W	1h	INTERNAL 0 CONFIG Event line mode select for event corresponding to none.INT_EVENT0 0h = The interrupt or event line is disabled. 1h = The interrupt or event line is in software mode. Software must clear the RIS. 2h = The interrupt or event line is in hardware mode. The hardware (another module) clears automatically the associated RIS flag.

24.4.20 CTL0 Register (Offset = 1100h) [Reset = 00000000h]

CTL0 is shown in Table 24-30.

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ULP_ADCHP Control Register 0

Table 24-30. CTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	0h	
26-24	SCLKDIV	R/W	0h	NU - should keep as '0'. Selects divide ratio of of sample clock. 0h = Do not divide clock source 1h = Divide clock source by 2 2h = Divide clock source by 3 3h = Divide clock source by 4 4h = Divide clock source by 5 5h = Divide clock source by 6 6h = Divide clock source by 7 7h = Divide clock source by 8
23-17	RESERVED	R/W	0h	
16	PWRDN	R/W	0h	Auto or manual power down mode. 0h = ADC is powered down on completion of a conversion, if there isn't a pending trigger. 1h = ADC is kept powered up as long as ADCEN bit is set.
15-1	RESERVED	R/W	0h	
0	ENC	RH/W	0h	ULP_ADCHP Enable Conversions. 0h = ULP_ADCHP primary sequencer is off Transition from ON to OFF will abort the primary single or repeat sequence on a MEMCTLx boundary. (The current conversion will finish and result stored in corresponding MEMRESx) 1h = ULP_ADCHP primary sequencer is ON. Waiting for valid trigger (Software or Hardware)

24.4.21 CTL1 Register (Offset = 1104h) [Reset = 00000000h]

CTL1 is shown in Table 24-31.

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Primary Sequence Control Register

Table 24-31. CTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	
30-28	AVGD	R/W	0h	Hardware average denominator. The number to divide the accumulated value by (this is a shift). Note results register is maximum of 16-bits long so if not shifted appropriately result will be truncated. 0h (R/W) = 0 bit shift 1h (R/W) = 1 bit shift 2h (R/W) = 2 bit shift 3h (R/W) = 3 bit shift 4h (R/W) = 4 bit shift 5h (R/W) = 5 bit shift 6h (R/W) = 6 bit shift 7h (R/W) = 7 bit shift
27	RESERVED	R/W	0h	
26-24	AVGN	R/W	0h	Hardware averager numerator. Selects number of conversions to accumulate for current MEMCTLx and then is get divided by AVGD. Result will be stored in MEMRESx. 0h (R/W) = Disables averager. 1h (R/W) = Averages 2 conversions before storing in MEMRES register. 2h (R/W) = Averages 4 conversions before storing in MEMRES register. 3h (R/W) = Averages 8 conversions before storing in MEMRES register. 4h (R/W) = Averages 16 conversions before storing in MEMRES register. 5h (R/W) = Averages 32 conversions before storing in MEMRES register. 6h (R/W) = Averages 64 conversions before storing in MEMRES register. 7h (R/W) = Averages 128 conversions before storing in MEMRES register.
23-21	RESERVED	R/W	0h	
20	SAMPMODE	R/W	0h	ULP_ADCHP Primary Sequencer Sample Mode. This bit select the source of the sampling signal. 0h = The sample timer high phase is used as sample signal. 1h = The external or software trigger is used as sample signal.
19-18	RESERVED	R/W	0h	
17-16	CONSEQ	R/W	0h	ULP_ADCHP Primary Sequencer Conversion Sequence Mode Select. 0h = The MEMCTLx pointed by PSTARTADD will be converted once. 1h = The primary sequence pointed by PSTARTADD will be converted once. 2h = The MEMCTLx pointed by PSTARTADD will be converted in repeat mode. 3h = Primary sequence pointed by PSTARTADD will be converted in repeat mode.
15-9	RESERVED	R/W	0h	

Table 24-31. CTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SC	RH/W	0h	ULP_ADCHP Sequencer Start Of Conversion. If ULP_ADCHP is configured as FOLLOWER, this bit has no effect. 0h = When PSAMPMODE is set to MANUAL (1) mode, clearing this bit will end the sampling phase and the conversion phase will start. When PSAMPMODE is set to AUTO mode (0), writing 0 has no effect. This bit is automatically cleared at the end of the current conversion. 1h = When PSAMPMODE is set to MANUAL (1), setting this bit, will start the sampling phase. Sample phase will last as long as this bit is set. When PSAMPMODE is set to AUTO mode (0), setting this bit will trigger the timer based sample time.
7-1	RESERVED	R/W	0h	
0	TRIGSRC	R/W	0h	ULP_ADCHP Primary Sequence Trigger Source. 0h = Primary sequence or single conversion is triggered by software. 1h = Primary sequence or single conversion is triggered by hardware event_0. (See device specific data-sheet for source for availability of this trigger)

24.4.22 CTL2 Register (Offset = 1108h) [Reset = 00000000h]

CTL2 is shown in Table 24-32.

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Primary Sequence Control Register

Table 24-32. CTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	0h	
28-24	ENDADD	R/W	0h	ULP_ADCHP Primary Sequence End Address. These bits select which MEMCTLx is the last MEMCTL for primary sequence mode. The value of PSTARTADD is 0x00 to 0x1F, corresponding to MEMRES0 to MEMRES31. 00h = MEMCTL0 is selected as end address of primary sequence. 01h = MEMCTL1 is selected as end address of primary sequence. 02h = MEMCTL2 is selected as end address of primary sequence. 03h = MEMCTL3 is selected as end address of primary sequence. 04h = MEMCTL4 is selected as end address of primary sequence. 05h = MEMCTL5 is selected as end address of primary sequence. 06h = MEMCTL6 is selected as end address of primary sequence. 07h = MEMCTL7 is selected as end address of primary sequence. 08h = MEMCTL8 is selected as end address of primary sequence. 09h = MEMCTL9 is selected as end address of primary sequence. 0Ah = MEMCTL10 is selected as end address of primary sequence. 0Bh = MEMCTL11 is selected as end address of primary sequence. 0Ch = MEMCTL12 is selected as end address of primary sequence. 0Dh = MEMCTL13 is selected as end address of primary sequence. 0Eh = MEMCTL14 is selected as end address of primary sequence. 0Fh = MEMCTL15 is selected as end address of primary sequence. 10h = MEMCTL16 is selected as end address of primary sequence. 11h = MEMCTL17 is selected as end address of primary sequence. 12h = MEMCTL18 is selected as end address of primary sequence. 13h = MEMCTL19 is selected as end address of primary sequence. 14h = MEMCTL20 is selected as end address of primary sequence. 15h = MEMCTL21 is selected as end address of primary sequence. 16h = MEMCTL22 is selected as end address of primary sequence. 17h = MEMCTL23 is selected as end address of primary sequence. 18h = MEMCTL24 is selected as end address of primary sequence. 19h = MEMCTL25 is selected as end address of primary sequence. 1Ah = MEMCTL26 is selected as end address of primary sequence. 1Bh = MEMCTL27 is selected as end address of primary sequence. 1Ch = MEMCTL28 is selected as end address of primary sequence. 1Dh = MEMCTL29 is selected as end address of primary sequence. 1Eh = MEMCTL30 is selected as end address of primary sequence. 1Fh = MEMCTL31 is selected as end address of primary sequence.
23-21	RESERVED	R/W	0h	

Table 24-32. CTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	STARTADD	R/W	0h	ULP_ADCHP Primary Sequence Start Address. These bits select which MEMCTLx is used for single conversion or as first MEMCTL for primary sequence mode. The value of PSTARTADD is 0x00 to 0x1F, corresponding to MEMRES0 to MEMRES31. 00h = MEMCTL0 is selected as start address of a primary sequence or as a single conversion. 01h = MEMCTL1 is selected as start address of a primary sequence or as a single conversion. 02h = MEMCTL2 is selected as start address of a primary sequence or as a single conversion. 03h = MEMCTL3 is selected as start address of a primary sequence or as a single conversion. 04h = MEMCTL4 is selected as start address of a primary sequence or as a single conversion. 05h = MEMCTL5 is selected as start address of a primary sequence or as a single conversion. 06h = MEMCTL6 is selected as start address of a primary sequence or as a single conversion. 07h = MEMCTL7 is selected as start address of a primary sequence or as a single conversion. 08h = MEMCTL8 is selected as start address of a primary sequence or as a single conversion. 09h = MEMCTL9 is selected as start address of a primary sequence or as a single conversion. 0Ah = MEMCTL10 is selected as start address of a primary sequence or as a single conversion. 0Bh = MEMCTL11 is selected as start address of a primary sequence or as a single conversion. 0Ch = MEMCTL12 is selected as start address of a primary sequence or as a single conversion. 0Dh = MEMCTL13 is selected as start address of a primary sequence or as a single conversion. 0Eh = MEMCTL14 is selected as start address of a primary sequence or as a single conversion. 0Fh = MEMCTL15 is selected as start address of a primary sequence or as a single conversion. 10h = MEMCTL16 is selected as start address of a primary sequence or as a single conversion. 11h = MEMCTL17 is selected as start address of a primary sequence or as a single conversion. 12h = MEMCTL18 is selected as start address of a primary sequence or as a single conversion. 13h = MEMCTL19 is selected as start address of a primary sequence or as a single conversion. 14h = MEMCTL20 is selected as start address of a primary sequence or as a single conversion. 15h = MEMCTL21 is selected as start address of a primary sequence or as a single conversion. 16h = MEMCTL22 is selected as start address of a primary sequence or as a single conversion. 17h = MEMCTL23 is selected as start address of a primary sequence or as a single conversion. 18h = MEMCTL24 is selected as start address of a primary sequence or as a single conversion. 19h = MEMCTL25 is selected as start address of a primary sequence or as a single conversion. 1Ah = MEMCTL26 is selected as start address of a primary sequence or as a single conversion. 1Bh = MEMCTL27 is selected as start address of a primary sequence or as a single conversion. 1Ch = MEMCTL28 is selected as start address of a primary sequence or as a single conversion. 1Dh = MEMCTL29 is selected as start address of a primary sequence or as a single conversion.

Table 24-32. CTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				1Eh = MEMCTL30 is selected as start address of a primary sequence or as a single conversion. 1Fh = MEMCTL31 is selected as start address of a primary sequence or as a single conversion.
15-11	RESERVED	R/W	0h	
10	FIFOEN	R/W	0h	Enables configuring of MEMRES register in FIFO mode. 0h = Disabled FIFO mode of operation, 1h = Enables FIFO mode of operation.
9	RESERVED	R/W	0h	
8	DMAEN	RH/W	0h	Enable DMA for data transfer. 0h (R/W) = DMA triggers are not enabled. 1h (R/W) = Enable DMA.
7-3	RESERVED	R/W	0h	
2-1	RES	R/W	0h	ULP_ADCHP resolution. This bits define the conversion result resolution. Note : A value of 3 defaults to 12 bit resolution. 0h = 16-bits resolution
0	DF	R/W	0h	ULP_ADCHP data read-back format. Data is always stored in binary unsigned format. 0h = Digital result reads as Binary Unsigned. 1h = Digital result reads Signed Binary. (2s complement), left aligned.

24.4.23 CTL3 Register (Offset = 110Ch) [Reset = 00000000h]

CTL3 is shown in Table 24-33.

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Control Register 3. This register is used to configure ADC for ad-hoc single conversion.

Table 24-33. CTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15	ASCMODE	R/W	0h	Single vs Differential
14	ASCFSR	R/W	0h	Full scale range of ADC limited to 1.8V or 3.3V *Exact range may be limited below the above mentioned voltages based on the design constraints
13-12	ASCVRSEL	R/W	0h	Selects the voltage reference for ASC operation. VEREFM must be connected to on-board ground when external reference option is selected. Note: Writing value 0x3 defaults to INTREF. 1h = EXTREF pin reference. 2h = Internal reference.
11-9	RESERVED	R/W	0h	
8	ASCSTIME	R/W	0h	ASC sample time compare value select. This is used to select between SCOMP0 and SCOMP1 registers for ASC operation. 0h = Select SCOMP0 1h = Select SCOMP1
7-5	RESERVED	R/W	0h	
4-0	ASCCHSEL	R/W	0h	ASC channel select 00h = Selects channel 0 01h = Selects channel 1 02h = Selects channel 2 03h = Selects channel 3 04h = Selects channel 4 05h = Selects channel 5 06h = Selects channel 6 07h = Selects channel 7 08h = Selects channel 8 09h = Selects channel 9 0Ah = Selects channel 10 0Bh = Selects channel 11 0Ch = Selects channel 12 0Dh = Selects channel 13 0Eh = Selects channel 14 0Fh = Selects channel 15 10h = Selects channel 16 11h = Selects channel 17 12h = Selects channel 18 13h = Selects channel 19 14h = Selects channel 20 15h = Selects channel 21 16h = Selects channel 22 17h = Selects channel 23 18h = Selects channel 24 19h = Selects channel 25 1Ah = Selects channel 26 1Bh = Selects channel 27 1Ch = Selects channel 28 1Dh = Selects channel 29 1Eh = Selects channel 30 1Fh = Selects channel 31

24.4.24 SCOMP0 Register (Offset = 1114h) [Reset = 00000000h]

SCOMP0 is shown in Table 24-34.

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ULP_ADCHP sample time register x Specifies the sample time, in number of ADCCLK cycles, when PSSM = 0 (AUTO) or SSSM = 0 (AUTO). CTL0.ENC must be set to 0 to write to this register.

Table 24-34. SCOMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	0h	
13-0	SMP	R/W	0h	SAMPLE This bit-field specify the number of sample time clocks (SCOMPx +1) for a conversion when SAMPLE_TIME in MEMCTLx is set to SCOMPx.

24.4.25 SCOMP1 Register (Offset = 1118h) [Reset = 00000000h]

SCOMP1 is shown in Table 24-35.

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ULP_ADCHP sample time register x Specifies the sample time, in number of ADCCLK cycles, when PSSM = 0 (AUTO) or SSSM = 0 (AUTO). CTL0.ENC must be set to 0 to write to this register.

Table 24-35. SCOMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	0h	
13-0	SMP	R/W	0h	SAMPLE This bitfield specify the number of sample time clocks (SCOMPx +1) for a conversion when SAMPLE_TIME in MEMCTLx is set to SCOMPx.

24.4.26 REFCFG Register (Offset = 111Ch) [Reset = 00000000h]

REFCFG is shown in Table 24-36.

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REFBUF configuration register

Table 24-36. REFCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	0h	
7-6	SPAR	R/W	0h	SPARE
5	PWRDN	R/W	0h	POWER DOWN Similar to ADC PWRDN control to save power in duty cycled mode of operation. 0 - AUTO, 1 - MANUAL In case of ADC, Sample time MMR needs to take into account time required to power on ADC. Since REF BUF may take time in us, recommendation is to use REFOKf th output oe buffer instead to start ADC conversion
4-3	IBPROG	R/W	0h	Configures REFBUF IBIAS current output value 0h = 1uA 1h = 0.5uA 2h = 2uA 3h = 0.67uA
2	IBEN	R/W	0h	REFBUF IBIAS enable 0h = Disable 1h = Enable
1	REFVSEL	R/W	0h	Configures REFBUF output voltage
0	REFEN	R/W	0h	REFBUF enable 0h = Disable 1h = Enable

24.4.27 WCLOW Register (Offset = 1148h) [Reset = 00000000h]

WCLOW is shown in Table 24-37.

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ULP_ADCHP Window Comparator Low Threshold 0 Register. The data format that is used to write and read WCLOW0 depends on the value of the DATAFORMAT bit in the CTL1 register. If DATAFORMAT = 0, the data is binary unsigned and right aligned. If DATAFORMAT = 1, the data is 2s complement and left aligned. Refer to the WCLOW0 bit-field description for details. CTL0.ENC must be set to 0 to write to this register. Design Note: To minimize cycles transforming data, the data written to WCLOW0 should be transformed into DATAFORMAT = 0 to match the MEMRESx register so a direct comparison can be done. Thus, there are extra cycles to write to this register but no penalty when a comparison is done.

Table 24-37. WCLOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15-0	DATA	R/W	0h	Low threshold register 0. If DATAFORMAT = 0, unsigned binary format has to be used: The value based on the resolution has to be right aligned with the MSB on the left. For 14-bits and 12-bits resolution, unused bit have to be 0s Reset value is 0x0000. If DATAFORMAT = 1, 2s-complement format has to be used. The value based on the resolution has to be left aligned with the LSB on the right. For 14-bits and 12-bits resolution, unused bit have to be 0s Reset value is 0x8000.

24.4.28 WCHI Register (Offset = 1150h) [Reset = 00000000h]

WCHI is shown in Table 24-38.

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WC HIGH ULP_ADCHP Window Comparator High Threshold 0 Register. The data format that is used to write and read WCHIGH0 depends on the value of the DATAFORMAT bit in the CTL1 register. If DATAFORMAT = 0, the data is binary unsigned and right aligned. If DATAFORMAT = 1, the data is 2s complement and left aligned. Refer to the WCHIGH0 bit-field description for details. CTL0.ENC must be set to 0 to write to this register. Design Note: To minimize cycles transforming data, the data written to WCHIGH0 should be transformed in DATAFORMAT = 0 to match the MEMRESx register so a direct comparison can be done. Thus, there are extra cycles to write to this register but no penalty when a comparison is done.

Table 24-38. WCHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15-0	DATA	R/W	0h	ULP_ADCHP Low threshold register 0. If DATAFORMAT = 0, unsigned binary format has to be used: The threshold value has to be right aligned, with the MSB on the left. Reset value are: 0xFFFF (16-bit), 0x3FFF (14-bit) or 0x0FFF (12-bit) If DATAFORMAT = 1, 2s-complement format has to be used. The value based on the resolution has to be left aligned with the LSB on the right. For 14-bits and 12-bits resolution, unused bit have to be 0s Reset value are: 0x7FFF (16-bit), 0x7FFC (14-bit) or 0x7FF0 (12-bit)

24.4.29 FIFODATA Register (Offset = 1160h) [Reset = 00000000h]

FIFODATA is shown in Table 24-39.

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Virtual data register used to do a read from FIFO.

Table 24-39. FIFODATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R	0h	Read from data field returns the data from the top of FIFO.

24.4.30 ASCRES Register (Offset = 1170h) [Reset = 00000000h]

ASCRES is shown in Table 24-40.

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ASC result register.

Table 24-40. ASCRES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R	0h	Data

24.4.31 MEMCTL_0 Register (Offset = 1180h) [Reset = 00000100h]

MEMCTL_0 is shown in Table 24-41.

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ULP_ADCHP Conversion Memory Control Register x (x=0 to 31) CTL0.ENC must be set to 0 to write to this register.

Table 24-41. MEMCTL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	
30	MOD	R/W	0h	MODE Single vs Differential
29	FSR	R/W	0h	Full scale range of ADC limited to 1.8V or 3.3V '0' - 3.3V '1' - 1.8V * Exact range may be limited below the above mentioned voltages based on the design constraints
28	WINCOMP	R/W	0h	Window Comparator Enable. Select for the current conversion if the Window Comparator feature is used. 0h = Window Comparator is disabled. 1h = Window Comparator is enabled.
27-25	RESERVED	R/W	0h	
24	TRIG	R/W	0h	TRIG. Indicates if a trigger will be needed to step to the next MEMCTL in the sequence. 0h = Automatically step to next MEMCTL register. 1h = A valid trigger will step to next MEMCTL register.
23-17	RESERVED	R/W	0h	
16	AVGEN	R/W	0h	Enable averaging. 0h (R/W) = Averaging disabled. 1h = Averaging enabled.
15-13	RESERVED	R/W	0h	
12	STIME	R/W	0h	Selects the source of sample timer period. Can choose between SCOMP0 and SCOMP1. 0h = Select SCOMP0. 1h = Select SCOMP1.
11-10	RESERVED	R/W	0h	
9-8	VRSEL	R/W	1h	Selects the combination of V(Rp) and V(Rn) sources. It is recommended to connect VeREFn0 to on-board ground when VeREFn is selected for V(Rn). Note: A value of 3 defaults to INTREF and value of 0 defaults to EXTREF. 1h = EXTREF pin reference. 2h = INTREF reference.
7-5	RESERVED	R/W	0h	

Table 24-41. MEMCTL_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	CHANSEL	R/W	0h	ULP_ADCHP Input channel select. In single ended mode, any of the 32 channels can be selected. In differential mode, this field will select which EVEN channel to be connected to the vin+ input. The vin- is automatically set to the next ODD channel. (CHANSEL+1) 00h = If DIFIN= 0: Ain+ = A0. If DIFIN = 1: Ain+ = A0, Ain- = A1 01h = If DIFIN= 0: Ain+ = A1. If DIFIN = 1: Ain+ = A0, Ain- = A1 02h = If DIFIN = 0: Ain+ = A2. If DIFIN = 1: Ain+ = A2, Ain- = A3 03h = If DIFIN = 0: Ain+ = A3. If DIFIN = 1: Ain+ = A2, Ain- = A3 04h = If DIFIN = 0: Ain+ = A4. If DIFIN = 1: Ain+ = A4, Ain- = A5 05h = If DIFIN = 0: Ain+ = A5. If DIFIN = 1: Ain+ = A4, Ain- = A5 06h = If DIFIN = 0: Ain+ = A6. If DIFIN = 1: Ain+ = A6, Ain- = A7 07h = If DIFIN = 0: Ain+ = A7. If DIFIN = 1: Ain+ = A6, Ain- = A7 08h = If DIFIN = 0: Ain+ = A8. If DIFIN = 1: Ain+ = A8, Ain- = A9 09h = If DIFIN= 0: Ain+ = A9. If DIFIN = 1: Ain+ = A8, Ain- = A9 0Ah = If DIFIN= 0: Ain+ = A10. If DIFIN = 1: Ain+ = A10, Ain- = A11 0Bh = If DIFIN= 0: Ain+ = A11. If DIFIN = 1: Ain+ = A10, Ain- = A11 0Ch = If DIFIN= 0: Ain+ = A12. If DIFIN = 1: Ain+ = A12, Ain- = A13 0Dh = If DIFIN= 0: Ain+ = A13. If DIFIN = 1: Ain+ = A12, Ain- = A13 0Eh = If DIFIN= 0: Ain+ = A14. If DIFIN = 1: Ain+ = A14, Ain- = A15 0Fh = If DIFIN= 0: Ain+ = A15. If DIFIN = 1: Ain+ = A14, Ain- = A15 10h = If DIFIN= 0: Ain+ = A16. If DIFIN = 1: Ain+ = A16, Ain- = A17 11h = If DIFIN= 0: Ain+ = A17. If DIFIN = 1: Ain+ = A16, Ain- = A17 12h = If DIFIN= 0: Ain+ = A18. If DIFIN = 1: Ain+ = A18, Ain- = A19 13h = If DIFIN= 0: Ain+ = A19. If DIFIN = 1: Ain+ = A18, Ain- = A19 14h = If DIFIN= 0: Ain+ = A20. If DIFIN = 1: Ain+ = A20, Ain- = A21 15h = If DIFIN= 0: Ain+ = A21. If DIFIN = 1: Ain+ = A20, Ain- = A21 16h = If DIFIN= 0: Ain+ = A22. If DIFIN = 1: Ain+ = A22, Ain- = A23 17h = If DIFIN= 0: Ain+ = A23. If DIFIN = 1: Ain+ = A22, Ain- = A23 18h = If DIFIN= 0: Ain+ = A24. If DIFIN = 1: Ain+ = A24, Ain- = A25 19h = If DIFIN= 0: Ain+ = A25. If DIFIN = 1: Ain+ = A24, Ain- = A25 1Ah = If DIFIN= 0: Ain+ = A26. If DIFIN = 1: Ain+ = A26, Ain- = A27 1Bh = If DIFIN= 0: Ain+ = A27. If DIFIN = 1: Ain+ = A26, Ain- = A27 1Ch = If DIFIN= 0: Ain+ = A28. If DIFIN = 1: Ain+ = A28, Ain- = A29 1Dh = If DIFIN= 0: Ain+ = A29. If DIFIN = 1: Ain+ = A28, Ain- = A29 1Eh = If DIFIN= 0: Ain+ = A30. If DIFIN = 1: Ain+ = A30, Ain- = A31 1Fh = If DIFIN= 0: Ain+ = A31. If DIFIN = 1: Ain+ = A30, Ain- = A31

24.4.32 MEMCTL_1 Register (Offset = 1184h) [Reset = 00000100h]

MEMCTL_1 is shown in Table 24-42.

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ULP_ADCHP Conversion Memory Control Register x (x=0 to 31) CTL0.ENC must be set to 0 to write to this register.

Table 24-42. MEMCTL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	
30	MOD	R/W	0h	MODE Single vs Differential
29	FSR	R/W	0h	Full scale range of ADC limited to 1.8V or 3.3V '0' - 3.3V '1' - 1.8V * Exact range may be limited below the above mentioned voltages based on the design constraints
28	WINCOMP	R/W	0h	Window Comparator Enable. Select for the current conversion if the Window Comparator feature is used. 0h = Window Comparator is disabled. 1h = Window Comparator is enabled.
27-25	RESERVED	R/W	0h	
24	TRIG	R/W	0h	TRIG. Indicates if a trigger will be needed to step to the next MEMCTL in the sequence. 0h = Automatically step to next MEMCTL register. 1h = A valid trigger will step to next MEMCTL register.
23-17	RESERVED	R/W	0h	
16	AVGEN	R/W	0h	Enable averaging. 0h (R/W) = Averaging disabled. 1h = Averaging enabled.
15-13	RESERVED	R/W	0h	
12	STIME	R/W	0h	Selects the source of sample timer period. Can choose between SCOMP0 and SCOMP1. 0h = Select SCOMP0. 1h = Select SCOMP1.
11-10	RESERVED	R/W	0h	
9-8	VRSEL	R/W	1h	Selects the combination of V(Rp) and V(Rn) sources. It is recommended to connect VeREFn0 to on-board ground when VeREFn is selected for V(Rn). Note: A value of 3 defaults to INTREF and value of 0 defaults to EXTREF. 1h = EXTREF pin reference. 2h = INTREF reference.
7-5	RESERVED	R/W	0h	

Table 24-42. MEMCTL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	CHANSEL	R/W	0h	ULP_ADCHP Input channel select. In single ended mode, any of the 32 channels can be selected. In differential mode, this field will select which EVEN channel to be connected to the vin+ input. The vin- is automatically set to the next ODD channel. (CHANSEL+1) 00h = If DIFIN= 0: Ain+ = A0. If DIFIN = 1: Ain+ = A0, Ain- = A1 01h = If DIFIN= 0: Ain+ = A1. If DIFIN = 1: Ain+ = A0, Ain- = A1 02h = If DIFIN = 0: Ain+ = A2. If DIFIN = 1: Ain+ = A2, Ain- = A3 03h = If DIFIN = 0: Ain+ = A3. If DIFIN = 1: Ain+ = A2, Ain- = A3 04h = If DIFIN = 0: Ain+ = A4. If DIFIN = 1: Ain+ = A4, Ain- = A5 05h = If DIFIN = 0: Ain+ = A5. If DIFIN = 1: Ain+ = A4, Ain- = A5 06h = If DIFIN = 0: Ain+ = A6. If DIFIN = 1: Ain+ = A6, Ain- = A7 07h = If DIFIN = 0: Ain+ = A7. If DIFIN = 1: Ain+ = A6, Ain- = A7 08h = If DIFIN = 0: Ain+ = A8. If DIFIN = 1: Ain+ = A8, Ain- = A9 09h = If DIFIN= 0: Ain+ = A9. If DIFIN = 1: Ain+ = A8, Ain- = A9 0Ah = If DIFIN= 0: Ain+ = A10. If DIFIN = 1: Ain+ = A10, Ain- = A11 0Bh = If DIFIN= 0: Ain+ = A11. If DIFIN = 1: Ain+ = A10, Ain- = A11 0Ch = If DIFIN= 0: Ain+ = A12. If DIFIN = 1: Ain+ = A12, Ain- = A13 0Dh = If DIFIN= 0: Ain+ = A13. If DIFIN = 1: Ain+ = A12, Ain- = A13 0Eh = If DIFIN= 0: Ain+ = A14. If DIFIN = 1: Ain+ = A14, Ain- = A15 0Fh = If DIFIN= 0: Ain+ = A15. If DIFIN = 1: Ain+ = A14, Ain- = A15 10h = If DIFIN= 0: Ain+ = A16. If DIFIN = 1: Ain+ = A16, Ain- = A17 11h = If DIFIN= 0: Ain+ = A17. If DIFIN = 1: Ain+ = A16, Ain- = A17 12h = If DIFIN= 0: Ain+ = A18. If DIFIN = 1: Ain+ = A18, Ain- = A19 13h = If DIFIN= 0: Ain+ = A19. If DIFIN = 1: Ain+ = A18, Ain- = A19 14h = If DIFIN= 0: Ain+ = A20. If DIFIN = 1: Ain+ = A20, Ain- = A21 15h = If DIFIN= 0: Ain+ = A21. If DIFIN = 1: Ain+ = A20, Ain- = A21 16h = If DIFIN= 0: Ain+ = A22. If DIFIN = 1: Ain+ = A22, Ain- = A23 17h = If DIFIN= 0: Ain+ = A23. If DIFIN = 1: Ain+ = A22, Ain- = A23 18h = If DIFIN= 0: Ain+ = A24. If DIFIN = 1: Ain+ = A24, Ain- = A25 19h = If DIFIN= 0: Ain+ = A25. If DIFIN = 1: Ain+ = A24, Ain- = A25 1Ah = If DIFIN= 0: Ain+ = A26. If DIFIN = 1: Ain+ = A26, Ain- = A27 1Bh = If DIFIN= 0: Ain+ = A27. If DIFIN = 1: Ain+ = A26, Ain- = A27 1Ch = If DIFIN= 0: Ain+ = A28. If DIFIN = 1: Ain+ = A28, Ain- = A29 1Dh = If DIFIN= 0: Ain+ = A29. If DIFIN = 1: Ain+ = A28, Ain- = A29 1Eh = If DIFIN= 0: Ain+ = A30. If DIFIN = 1: Ain+ = A30, Ain- = A31 1Fh = If DIFIN= 0: Ain+ = A31. If DIFIN = 1: Ain+ = A30, Ain- = A31

24.4.33 MEMCTL_2 Register (Offset = 1188h) [Reset = 00000100h]

MEMCTL_2 is shown in Table 24-43.

Return to the Summary Table.

ULP_ADCHP Conversion Memory Control Register x (x=0 to 31) CTL0.ENC must be set to 0 to write to this register.

Table 24-43. MEMCTL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	
30	MOD	R/W	0h	MODE Single vs Differential
29	FSR	R/W	0h	Full scale range of ADC limited to 1.8V or 3.3V '0' - 3.3V '1' - 1.8V * Exact range may be limited below the above mentioned voltages based on the design constraints
28	WINCOMP	R/W	0h	Window Comparator Enable. Select for the current conversion if the Window Comparator feature is used. 0h = Window Comparator is disabled. 1h = Window Comparator is enabled.
27-25	RESERVED	R/W	0h	
24	TRIG	R/W	0h	TRIG. Indicates if a trigger will be needed to step to the next MEMCTL in the sequence. 0h = Automatically step to next MEMCTL register. 1h = A valid trigger will step to next MEMCTL register.
23-17	RESERVED	R/W	0h	
16	AVGEN	R/W	0h	Enable averaging. 0h (R/W) = Averaging disabled. 1h = Averaging enabled.
15-13	RESERVED	R/W	0h	
12	STIME	R/W	0h	Selects the source of sample timer period. Can choose between SCOMP0 and SCOMP1. 0h = Select SCOMP0. 1h = Select SCOMP1.
11-10	RESERVED	R/W	0h	
9-8	VRSEL	R/W	1h	Selects the combination of V(Rp) and V(Rn) sources. It is recommended to connect VeREFn0 to on-board ground when VeREFn is selected for V(Rn). Note: A value of 3 defaults to INTREF and value of 0 defaults to EXTREF. 1h = EXTREF pin reference. 2h = INTREF reference.
7-5	RESERVED	R/W	0h	

Table 24-43. MEMCTL_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	CHANSEL	R/W	0h	ULP_ADCHP Input channel select. In single ended mode, any of the 32 channels can be selected. In differential mode, this field will select which EVEN channel to be connected to the vin+ input. The vin- is automatically set to the next ODD channel. (CHANSEL+1) 00h = If DIFIN= 0: Ain+ = A0. If DIFIN = 1: Ain+ = A0, Ain- = A1 01h = If DIFIN= 0: Ain+ = A1. If DIFIN = 1: Ain+ = A0, Ain- = A1 02h = If DIFIN = 0: Ain+ = A2. If DIFIN = 1: Ain+ = A2, Ain- = A3 03h = If DIFIN = 0: Ain+ = A3. If DIFIN = 1: Ain+ = A2, Ain- = A3 04h = If DIFIN = 0: Ain+ = A4. If DIFIN = 1: Ain+ = A4, Ain- = A5 05h = If DIFIN = 0: Ain+ = A5. If DIFIN = 1: Ain+ = A4, Ain- = A5 06h = If DIFIN = 0: Ain+ = A6. If DIFIN = 1: Ain+ = A6, Ain- = A7 07h = If DIFIN = 0: Ain+ = A7. If DIFIN = 1: Ain+ = A6, Ain- = A7 08h = If DIFIN = 0: Ain+ = A8. If DIFIN = 1: Ain+ = A8, Ain- = A9 09h = If DIFIN= 0: Ain+ = A9. If DIFIN = 1: Ain+ = A8, Ain- = A9 0Ah = If DIFIN= 0: Ain+ = A10. If DIFIN = 1: Ain+ = A10, Ain- = A11 0Bh = If DIFIN= 0: Ain+ = A11. If DIFIN = 1: Ain+ = A10, Ain- = A11 0Ch = If DIFIN= 0: Ain+ = A12. If DIFIN = 1: Ain+ = A12, Ain- = A13 0Dh = If DIFIN= 0: Ain+ = A13. If DIFIN = 1: Ain+ = A12, Ain- = A13 0Eh = If DIFIN= 0: Ain+ = A14. If DIFIN = 1: Ain+ = A14, Ain- = A15 0Fh = If DIFIN= 0: Ain+ = A15. If DIFIN = 1: Ain+ = A14, Ain- = A15 10h = If DIFIN= 0: Ain+ = A16. If DIFIN = 1: Ain+ = A16, Ain- = A17 11h = If DIFIN= 0: Ain+ = A17. If DIFIN = 1: Ain+ = A16, Ain- = A17 12h = If DIFIN= 0: Ain+ = A18. If DIFIN = 1: Ain+ = A18, Ain- = A19 13h = If DIFIN= 0: Ain+ = A19. If DIFIN = 1: Ain+ = A18, Ain- = A19 14h = If DIFIN= 0: Ain+ = A20. If DIFIN = 1: Ain+ = A20, Ain- = A21 15h = If DIFIN= 0: Ain+ = A21. If DIFIN = 1: Ain+ = A20, Ain- = A21 16h = If DIFIN= 0: Ain+ = A22. If DIFIN = 1: Ain+ = A22, Ain- = A23 17h = If DIFIN= 0: Ain+ = A23. If DIFIN = 1: Ain+ = A22, Ain- = A23 18h = If DIFIN= 0: Ain+ = A24. If DIFIN = 1: Ain+ = A24, Ain- = A25 19h = If DIFIN= 0: Ain+ = A25. If DIFIN = 1: Ain+ = A24, Ain- = A25 1Ah = If DIFIN= 0: Ain+ = A26. If DIFIN = 1: Ain+ = A26, Ain- = A27 1Bh = If DIFIN= 0: Ain+ = A27. If DIFIN = 1: Ain+ = A26, Ain- = A27 1Ch = If DIFIN= 0: Ain+ = A28. If DIFIN = 1: Ain+ = A28, Ain- = A29 1Dh = If DIFIN= 0: Ain+ = A29. If DIFIN = 1: Ain+ = A28, Ain- = A29 1Eh = If DIFIN= 0: Ain+ = A30. If DIFIN = 1: Ain+ = A30, Ain- = A31 1Fh = If DIFIN= 0: Ain+ = A31. If DIFIN = 1: Ain+ = A30, Ain- = A31

24.4.34 MEMCTL_3 Register (Offset = 118Ch) [Reset = 00000100h]

MEMCTL_3 is shown in Table 24-44.

Return to the Summary Table.

ULP_ADCHP Conversion Memory Control Register x (x=0 to 31) CTL0.ENC must be set to 0 to write to this register.

Table 24-44. MEMCTL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	
30	MOD	R/W	0h	MODE Single vs Differential
29	FSR	R/W	0h	Full scale range of ADC limited to 1.8V or 3.3V '0' - 3.3V '1' - 1.8V * Exact range may be limited below the above mentioned voltages based on the design constraints
28	WINCOMP	R/W	0h	Window Comparator Enable. Select for the current conversion if the Window Comparator feature is used. 0h = Window Comparator is disabled. 1h = Window Comparator is enabled.
27-25	RESERVED	R/W	0h	
24	TRIG	R/W	0h	TRIG. Indicates if a trigger will be needed to step to the next MEMCTL in the sequence. 0h = Automatically step to next MEMCTL register. 1h = A valid trigger will step to next MEMCTL register.
23-17	RESERVED	R/W	0h	
16	AVGEN	R/W	0h	Enable averaging. 0h (R/W) = Averaging disabled. 1h = Averaging enabled.
15-13	RESERVED	R/W	0h	
12	STIME	R/W	0h	Selects the source of sample timer period. Can choose between SCOMP0 and SCOMP1. 0h = Select SCOMP0. 1h = Select SCOMP1.
11-10	RESERVED	R/W	0h	
9-8	VRSEL	R/W	1h	Selects the combination of V(Rp) and V(Rn) sources. It is recommended to connect VeREFn0 to on-board ground when VeREFn is selected for V(Rn). Note: A value of 3 defaults to INTREF and value of 0 defaults to EXTREF. 1h = EXTREF pin reference. 2h = INTREF reference.
7-5	RESERVED	R/W	0h	

Table 24-44. MEMCTL_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	CHANSEL	R/W	0h	ULP_ADCHP Input channel select. In single ended mode, any of the 32 channels can be selected. In differential mode, this field will select which EVEN channel to be connected to the vin+ input. The vin- is automatically set to the next ODD channel. (CHANSEL+1) 00h = If DIFIN= 0: Ain+ = A0. If DIFIN = 1: Ain+ = A0, Ain- = A1 01h = If DIFIN= 0: Ain+ = A1. If DIFIN = 1: Ain+ = A0, Ain- = A1 02h = If DIFIN = 0: Ain+ = A2. If DIFIN = 1: Ain+ = A2, Ain- = A3 03h = If DIFIN = 0: Ain+ = A3. If DIFIN = 1: Ain+ = A2, Ain- = A3 04h = If DIFIN = 0: Ain+ = A4. If DIFIN = 1: Ain+ = A4, Ain- = A5 05h = If DIFIN = 0: Ain+ = A5. If DIFIN = 1: Ain+ = A4, Ain- = A5 06h = If DIFIN = 0: Ain+ = A6. If DIFIN = 1: Ain+ = A6, Ain- = A7 07h = If DIFIN = 0: Ain+ = A7. If DIFIN = 1: Ain+ = A6, Ain- = A7 08h = If DIFIN = 0: Ain+ = A8. If DIFIN = 1: Ain+ = A8, Ain- = A9 09h = If DIFIN= 0: Ain+ = A9. If DIFIN = 1: Ain+ = A8, Ain- = A9 0Ah = If DIFIN= 0: Ain+ = A10. If DIFIN = 1: Ain+ = A10, Ain- = A11 0Bh = If DIFIN= 0: Ain+ = A11. If DIFIN = 1: Ain+ = A10, Ain- = A11 0Ch = If DIFIN= 0: Ain+ = A12. If DIFIN = 1: Ain+ = A12, Ain- = A13 0Dh = If DIFIN= 0: Ain+ = A13. If DIFIN = 1: Ain+ = A12, Ain- = A13 0Eh = If DIFIN= 0: Ain+ = A14. If DIFIN = 1: Ain+ = A14, Ain- = A15 0Fh = If DIFIN= 0: Ain+ = A15. If DIFIN = 1: Ain+ = A14, Ain- = A15 10h = If DIFIN= 0: Ain+ = A16. If DIFIN = 1: Ain+ = A16, Ain- = A17 11h = If DIFIN= 0: Ain+ = A17. If DIFIN = 1: Ain+ = A16, Ain- = A17 12h = If DIFIN= 0: Ain+ = A18. If DIFIN = 1: Ain+ = A18, Ain- = A19 13h = If DIFIN= 0: Ain+ = A19. If DIFIN = 1: Ain+ = A18, Ain- = A19 14h = If DIFIN= 0: Ain+ = A20. If DIFIN = 1: Ain+ = A20, Ain- = A21 15h = If DIFIN= 0: Ain+ = A21. If DIFIN = 1: Ain+ = A20, Ain- = A21 16h = If DIFIN= 0: Ain+ = A22. If DIFIN = 1: Ain+ = A22, Ain- = A23 17h = If DIFIN= 0: Ain+ = A23. If DIFIN = 1: Ain+ = A22, Ain- = A23 18h = If DIFIN= 0: Ain+ = A24. If DIFIN = 1: Ain+ = A24, Ain- = A25 19h = If DIFIN= 0: Ain+ = A25. If DIFIN = 1: Ain+ = A24, Ain- = A25 1Ah = If DIFIN= 0: Ain+ = A26. If DIFIN = 1: Ain+ = A26, Ain- = A27 1Bh = If DIFIN= 0: Ain+ = A27. If DIFIN = 1: Ain+ = A26, Ain- = A27 1Ch = If DIFIN= 0: Ain+ = A28. If DIFIN = 1: Ain+ = A28, Ain- = A29 1Dh = If DIFIN= 0: Ain+ = A29. If DIFIN = 1: Ain+ = A28, Ain- = A29 1Eh = If DIFIN= 0: Ain+ = A30. If DIFIN = 1: Ain+ = A30, Ain- = A31 1Fh = If DIFIN= 0: Ain+ = A31. If DIFIN = 1: Ain+ = A30, Ain- = A31

24.4.35 MEMCTL_4 Register (Offset = 1190h) [Reset = 00000100h]

MEMCTL_4 is shown in Table 24-45.

Return to the Summary Table.

ULP_ADCHP Conversion Memory Control Register x (x=0 to 31) CTL0.ENC must be set to 0 to write to this register.

Table 24-45. MEMCTL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	
30	MOD	R/W	0h	MODE Single vs Differential
29	FSR	R/W	0h	Full scale range of ADC limited to 1.8V or 3.3V '0' - 3.3V '1' - 1.8V * Exact range may be limited below the above mentioned voltages based on the design constraints
28	WINCOMP	R/W	0h	Window Comparator Enable. Select for the current conversion if the Window Comparator feature is used. 0h = Window Comparator is disabled. 1h = Window Comparator is enabled.
27-25	RESERVED	R/W	0h	
24	TRIG	R/W	0h	TRIG. Indicates if a trigger will be needed to step to the next MEMCTL in the sequence. 0h = Automatically step to next MEMCTL register. 1h = A valid trigger will step to next MEMCTL register.
23-17	RESERVED	R/W	0h	
16	AVGEN	R/W	0h	Enable averaging. 0h (R/W) = Averaging disabled. 1h = Averaging enabled.
15-13	RESERVED	R/W	0h	
12	STIME	R/W	0h	Selects the source of sample timer period. Can choose between SCOMP0 and SCOMP1. 0h = Select SCOMP0. 1h = Select SCOMP1.
11-10	RESERVED	R/W	0h	
9-8	VRSEL	R/W	1h	Selects the combination of V(Rp) and V(Rn) sources. It is recommended to connect VeREFn0 to on-board ground when VeREFn is selected for V(Rn). Note: A value of 3 defaults to INTREF and value of 0 defaults to EXTREF. 1h = EXTREF pin reference. 2h = INTREF reference.
7-5	RESERVED	R/W	0h	

Table 24-45. MEMCTL_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	CHANSEL	R/W	0h	ULP_ADCHP Input channel select. In single ended mode, any of the 32 channels can be selected. In differential mode, this field will select which EVEN channel to be connected to the vin+ input. The vin- is automatically set to the next ODD channel. (CHANSEL+1) 00h = If DIFIN= 0: Ain+ = A0. If DIFIN = 1: Ain+ = A0, Ain- = A1 01h = If DIFIN= 0: Ain+ = A1. If DIFIN = 1: Ain+ = A0, Ain- = A1 02h = If DIFIN = 0: Ain+ = A2. If DIFIN = 1: Ain+ = A2, Ain- = A3 03h = If DIFIN = 0: Ain+ = A3. If DIFIN = 1: Ain+ = A2, Ain- = A3 04h = If DIFIN = 0: Ain+ = A4. If DIFIN = 1: Ain+ = A4, Ain- = A5 05h = If DIFIN = 0: Ain+ = A5. If DIFIN = 1: Ain+ = A4, Ain- = A5 06h = If DIFIN = 0: Ain+ = A6. If DIFIN = 1: Ain+ = A6, Ain- = A7 07h = If DIFIN = 0: Ain+ = A7. If DIFIN = 1: Ain+ = A6, Ain- = A7 08h = If DIFIN = 0: Ain+ = A8. If DIFIN = 1: Ain+ = A8, Ain- = A9 09h = If DIFIN= 0: Ain+ = A9. If DIFIN = 1: Ain+ = A8, Ain- = A9 0Ah = If DIFIN= 0: Ain+ = A10. If DIFIN = 1: Ain+ = A10, Ain- = A11 0Bh = If DIFIN= 0: Ain+ = A11. If DIFIN = 1: Ain+ = A10, Ain- = A11 0Ch = If DIFIN= 0: Ain+ = A12. If DIFIN = 1: Ain+ = A12, Ain- = A13 0Dh = If DIFIN= 0: Ain+ = A13. If DIFIN = 1: Ain+ = A12, Ain- = A13 0Eh = If DIFIN= 0: Ain+ = A14. If DIFIN = 1: Ain+ = A14, Ain- = A15 0Fh = If DIFIN= 0: Ain+ = A15. If DIFIN = 1: Ain+ = A14, Ain- = A15 10h = If DIFIN= 0: Ain+ = A16. If DIFIN = 1: Ain+ = A16, Ain- = A17 11h = If DIFIN= 0: Ain+ = A17. If DIFIN = 1: Ain+ = A16, Ain- = A17 12h = If DIFIN= 0: Ain+ = A18. If DIFIN = 1: Ain+ = A18, Ain- = A19 13h = If DIFIN= 0: Ain+ = A19. If DIFIN = 1: Ain+ = A18, Ain- = A19 14h = If DIFIN= 0: Ain+ = A20. If DIFIN = 1: Ain+ = A20, Ain- = A21 15h = If DIFIN= 0: Ain+ = A21. If DIFIN = 1: Ain+ = A20, Ain- = A21 16h = If DIFIN= 0: Ain+ = A22. If DIFIN = 1: Ain+ = A22, Ain- = A23 17h = If DIFIN= 0: Ain+ = A23. If DIFIN = 1: Ain+ = A22, Ain- = A23 18h = If DIFIN= 0: Ain+ = A24. If DIFIN = 1: Ain+ = A24, Ain- = A25 19h = If DIFIN= 0: Ain+ = A25. If DIFIN = 1: Ain+ = A24, Ain- = A25 1Ah = If DIFIN= 0: Ain+ = A26. If DIFIN = 1: Ain+ = A26, Ain- = A27 1Bh = If DIFIN= 0: Ain+ = A27. If DIFIN = 1: Ain+ = A26, Ain- = A27 1Ch = If DIFIN= 0: Ain+ = A28. If DIFIN = 1: Ain+ = A28, Ain- = A29 1Dh = If DIFIN= 0: Ain+ = A29. If DIFIN = 1: Ain+ = A28, Ain- = A29 1Eh = If DIFIN= 0: Ain+ = A30. If DIFIN = 1: Ain+ = A30, Ain- = A31 1Fh = If DIFIN= 0: Ain+ = A31. If DIFIN = 1: Ain+ = A30, Ain- = A31

24.4.36 MEMCTL_5 Register (Offset = 1194h) [Reset = 00000100h]

MEMCTL_5 is shown in Table 24-46.

Return to the Summary Table.

ULP_ADCHP Conversion Memory Control Register x (x=0 to 31) CTL0.ENC must be set to 0 to write to this register.

Table 24-46. MEMCTL_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	
30	MOD	R/W	0h	MODE Single vs Differential
29	FSR	R/W	0h	Full scale range of ADC limited to 1.8V or 3.3V '0' - 3.3V '1' - 1.8V * Exact range may be limited below the above mentioned voltages based on the design constraints
28	WINCOMP	R/W	0h	Window Comparator Enable. Select for the current conversion if the Window Comparator feature is used. 0h = Window Comparator is disabled. 1h = Window Comparator is enabled.
27-25	RESERVED	R/W	0h	
24	TRIG	R/W	0h	TRIG. Indicates if a trigger will be needed to step to the next MEMCTL in the sequence. 0h = Automatically step to next MEMCTL register. 1h = A valid trigger will step to next MEMCTL register.
23-17	RESERVED	R/W	0h	
16	AVGEN	R/W	0h	Enable averaging. 0h (R/W) = Averaging disabled. 1h = Averaging enabled.
15-13	RESERVED	R/W	0h	
12	STIME	R/W	0h	Selects the source of sample timer period. Can choose between SCOMP0 and SCOMP1. 0h = Select SCOMP0. 1h = Select SCOMP1.
11-10	RESERVED	R/W	0h	
9-8	VRSEL	R/W	1h	Selects the combination of V(Rp) and V(Rn) sources. It is recommended to connect VeREFn0 to on-board ground when VeREFn is selected for V(Rn). Note: A value of 3 defaults to INTREF and value of 0 defaults to EXTREF. 1h = EXTREF pin reference. 2h = INTREF reference.
7-5	RESERVED	R/W	0h	

Table 24-46. MEMCTL_5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	CHANSEL	R/W	0h	ULP_ADCHP Input channel select. In single ended mode, any of the 32 channels can be selected. In differential mode, this field will select which EVEN channel to be connected to the vin+ input. The vin- is automatically set to the next ODD channel. (CHANSEL+1) 00h = If DIFIN= 0: Ain+ = A0. If DIFIN = 1: Ain+ = A0, Ain- = A1 01h = If DIFIN= 0: Ain+ = A1. If DIFIN = 1: Ain+ = A0, Ain- = A1 02h = If DIFIN = 0: Ain+ = A2. If DIFIN = 1: Ain+ = A2, Ain- = A3 03h = If DIFIN = 0: Ain+ = A3. If DIFIN = 1: Ain+ = A2, Ain- = A3 04h = If DIFIN = 0: Ain+ = A4. If DIFIN = 1: Ain+ = A4, Ain- = A5 05h = If DIFIN = 0: Ain+ = A5. If DIFIN = 1: Ain+ = A4, Ain- = A5 06h = If DIFIN = 0: Ain+ = A6. If DIFIN = 1: Ain+ = A6, Ain- = A7 07h = If DIFIN = 0: Ain+ = A7. If DIFIN = 1: Ain+ = A6, Ain- = A7 08h = If DIFIN = 0: Ain+ = A8. If DIFIN = 1: Ain+ = A8, Ain- = A9 09h = If DIFIN= 0: Ain+ = A9. If DIFIN = 1: Ain+ = A8, Ain- = A9 0Ah = If DIFIN= 0: Ain+ = A10. If DIFIN = 1: Ain+ = A10, Ain- = A11 0Bh = If DIFIN= 0: Ain+ = A11. If DIFIN = 1: Ain+ = A10, Ain- = A11 0Ch = If DIFIN= 0: Ain+ = A12. If DIFIN = 1: Ain+ = A12, Ain- = A13 0Dh = If DIFIN= 0: Ain+ = A13. If DIFIN = 1: Ain+ = A12, Ain- = A13 0Eh = If DIFIN= 0: Ain+ = A14. If DIFIN = 1: Ain+ = A14, Ain- = A15 0Fh = If DIFIN= 0: Ain+ = A15. If DIFIN = 1: Ain+ = A14, Ain- = A15 10h = If DIFIN= 0: Ain+ = A16. If DIFIN = 1: Ain+ = A16, Ain- = A17 11h = If DIFIN= 0: Ain+ = A17. If DIFIN = 1: Ain+ = A16, Ain- = A17 12h = If DIFIN= 0: Ain+ = A18. If DIFIN = 1: Ain+ = A18, Ain- = A19 13h = If DIFIN= 0: Ain+ = A19. If DIFIN = 1: Ain+ = A18, Ain- = A19 14h = If DIFIN= 0: Ain+ = A20. If DIFIN = 1: Ain+ = A20, Ain- = A21 15h = If DIFIN= 0: Ain+ = A21. If DIFIN = 1: Ain+ = A20, Ain- = A21 16h = If DIFIN= 0: Ain+ = A22. If DIFIN = 1: Ain+ = A22, Ain- = A23 17h = If DIFIN= 0: Ain+ = A23. If DIFIN = 1: Ain+ = A22, Ain- = A23 18h = If DIFIN= 0: Ain+ = A24. If DIFIN = 1: Ain+ = A24, Ain- = A25 19h = If DIFIN= 0: Ain+ = A25. If DIFIN = 1: Ain+ = A24, Ain- = A25 1Ah = If DIFIN= 0: Ain+ = A26. If DIFIN = 1: Ain+ = A26, Ain- = A27 1Bh = If DIFIN= 0: Ain+ = A27. If DIFIN = 1: Ain+ = A26, Ain- = A27 1Ch = If DIFIN= 0: Ain+ = A28. If DIFIN = 1: Ain+ = A28, Ain- = A29 1Dh = If DIFIN= 0: Ain+ = A29. If DIFIN = 1: Ain+ = A28, Ain- = A29 1Eh = If DIFIN= 0: Ain+ = A30. If DIFIN = 1: Ain+ = A30, Ain- = A31 1Fh = If DIFIN= 0: Ain+ = A31. If DIFIN = 1: Ain+ = A30, Ain- = A31

24.4.37 MEMRES_0 Register (Offset = 1280h) [Reset = 00000000h]

MEMRES_0 is shown in Table 24-47.

Return to the Summary Table.

Memory Results Register

Table 24-47. MEMRES_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R	0h	MEMRESx result register. If DATAFORMAT = 0, unsigned binary: The conversion results are right aligned. In 14 and 12 bit mode, the unused MSB bits are forced to 0. If DATAFORMAT = 1, 2s-complement format: The conversion results are left aligned. In 14 and 12 bit mode, the unused LSB bits are forced to 0. The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back. Reading this register clears the corresponding bit in RIS.

24.4.38 MEMRES_1 Register (Offset = 1284h) [Reset = 00000000h]

MEMRES_1 is shown in Table 24-48.

Return to the Summary Table.

Memory Results Register

Table 24-48. MEMRES_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R	0h	MEMRESx result register. If DATAFORMAT = 0, unsigned binary: The conversion results are right aligned. In 14 and 12 bit mode, the unused MSB bits are forced to 0. If DATAFORMAT = 1, 2s-complement format: The conversion results are left aligned. In 14 and 12 bit mode, the unused LSB bits are forced to 0. The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back. Reading this register clears the corresponding bit in RIS.

24.4.39 MEMRES_2 Register (Offset = 1288h) [Reset = 00000000h]

MEMRES_2 is shown in Table 24-49.

Return to the Summary Table.

Memory Results Register

Table 24-49. MEMRES_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R	0h	MEMRESx result register. If DATAFORMAT = 0, unsigned binary: The conversion results are right aligned. In 14 and 12 bit mode, the unused MSB bits are forced to 0. If DATAFORMAT = 1, 2s-complement format: The conversion results are left aligned. In 14 and 12 bit mode, the unused LSB bits are forced to 0. The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back. Reading this register clears the corresponding bit in RIS.

24.4.40 MEMRES_3 Register (Offset = 128Ch) [Reset = 00000000h]

MEMRES_3 is shown in Table 24-50.

Return to the Summary Table.

Memory Results Register

Table 24-50. MEMRES_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R	0h	MEMRESx result register. If DATAFORMAT = 0, unsigned binary: The conversion results are right aligned. In 14 and 12 bit mode, the unused MSB bits are forced to 0. If DATAFORMAT = 1, 2s-complement format: The conversion results are left aligned. In 14 and 12 bit mode, the unused LSB bits are forced to 0. The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back. Reading this register clears the corresponding bit in RIS.

24.4.41 MEMRES_4 Register (Offset = 1290h) [Reset = 00000000h]

MEMRES_4 is shown in Table 24-51.

Return to the Summary Table.

Memory Results Register

Table 24-51. MEMRES_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R	0h	MEMRESx result register. If DATAFORMAT = 0, unsigned binary: The conversion results are right aligned. In 14 and 12 bit mode, the unused MSB bits are forced to 0. If DATAFORMAT = 1, 2s-complement format: The conversion results are left aligned. In 14 and 12 bit mode, the unused LSB bits are forced to 0. The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back. Reading this register clears the corresponding bit in RIS.

24.4.42 MEMRES_5 Register (Offset = 1294h) [Reset = 00000000h]

MEMRES_5 is shown in Table 24-52.

Return to the Summary Table.

Memory Results Register

Table 24-52. MEMRES_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R	0h	MEMRESx result register. If DATAFORMAT = 0, unsigned binary: The conversion results are right aligned. In 14 and 12 bit mode, the unused MSB bits are forced to 0. If DATAFORMAT = 1, 2s-complement format: The conversion results are left aligned. In 14 and 12 bit mode, the unused LSB bits are forced to 0. The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back. Reading this register clears the corresponding bit in RIS.

24.4.43 MEMRES_6 Register (Offset = 1298h) [Reset = 00000000h]

MEMRES_6 is shown in Table 24-53.

Return to the Summary Table.

Memory Results Register

Table 24-53. MEMRES_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R	0h	MEMRESx result register. If DATAFORMAT = 0, unsigned binary: The conversion results are right aligned. In 14 and 12 bit mode, the unused MSB bits are forced to 0. If DATAFORMAT = 1, 2s-complement format: The conversion results are left aligned. In 14 and 12 bit mode, the unused LSB bits are forced to 0. The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back. Reading this register clears the corresponding bit in RIS.

24.4.44 MEMRES_7 Register (Offset = 129Ch) [Reset = 00000000h]

MEMRES_7 is shown in Table 24-54.

Return to the Summary Table.

Memory Results Register

Table 24-54. MEMRES_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R	0h	MEMRESx result register. If DATAFORMAT = 0, unsigned binary: The conversion results are right aligned. In 14 and 12 bit mode, the unused MSB bits are forced to 0. If DATAFORMAT = 1, 2s-complement format: The conversion results are left aligned. In 14 and 12 bit mode, the unused LSB bits are forced to 0. The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back. Reading this register clears the corresponding bit in RIS.

24.4.45 MEMRES_8 Register (Offset = 12A0h) [Reset = 00000000h]

MEMRES_8 is shown in Table 24-55.

Return to the Summary Table.

Memory Results Register

Table 24-55. MEMRES_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R	0h	MEMRESx result register. If DATAFORMAT = 0, unsigned binary: The conversion results are right aligned. In 14 and 12 bit mode, the unused MSB bits are forced to 0. If DATAFORMAT = 1, 2s-complement format: The conversion results are left aligned. In 14 and 12 bit mode, the unused LSB bits are forced to 0. The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back. Reading this register clears the corresponding bit in RIS.

24.4.46 MEMRES_9 Register (Offset = 12A4h) [Reset = 00000000h]

MEMRES_9 is shown in Table 24-56.

Return to the Summary Table.

Memory Results Register

Table 24-56. MEMRES_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R	0h	MEMRESx result register. If DATAFORMAT = 0, unsigned binary: The conversion results are right aligned. In 14 and 12 bit mode, the unused MSB bits are forced to 0. If DATAFORMAT = 1, 2s-complement format: The conversion results are left aligned. In 14 and 12 bit mode, the unused LSB bits are forced to 0. The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back. Reading this register clears the corresponding bit in RIS.

24.4.47 MEMRES_10 Register (Offset = 12A8h) [Reset = 00000000h]

MEMRES_10 is shown in Table 24-57.

Return to the Summary Table.

Memory Results Register

Table 24-57. MEMRES_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R	0h	MEMRESx result register. If DATAFORMAT = 0, unsigned binary: The conversion results are right aligned. In 14 and 12 bit mode, the unused MSB bits are forced to 0. If DATAFORMAT = 1, 2s-complement format: The conversion results are left aligned. In 14 and 12 bit mode, the unused LSB bits are forced to 0. The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back. Reading this register clears the corresponding bit in RIS.

24.4.48 MEMRES_11 Register (Offset = 12ACh) [Reset = 00000000h]

MEMRES_11 is shown in Table 24-58.

Return to the Summary Table.

Memory Results Register

Table 24-58. MEMRES_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R	0h	MEMRESx result register. If DATAFORMAT = 0, unsigned binary: The conversion results are right aligned. In 14 and 12 bit mode, the unused MSB bits are forced to 0. If DATAFORMAT = 1, 2s-complement format: The conversion results are left aligned. In 14 and 12 bit mode, the unused LSB bits are forced to 0. The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back. Reading this register clears the corresponding bit in RIS.

24.4.49 MEMRES_12 Register (Offset = 12B0h) [Reset = 00000000h]

MEMRES_12 is shown in Table 24-59.

Return to the Summary Table.

Memory Results Register

Table 24-59. MEMRES_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R	0h	MEMRESx result register. If DATAFORMAT = 0, unsigned binary: The conversion results are right aligned. In 14 and 12 bit mode, the unused MSB bits are forced to 0. If DATAFORMAT = 1, 2s-complement format: The conversion results are left aligned. In 14 and 12 bit mode, the unused LSB bits are forced to 0. The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back. Reading this register clears the corresponding bit in RIS.

24.4.50 MEMRES_13 Register (Offset = 12B4h) [Reset = 00000000h]

MEMRES_13 is shown in Table 24-60.

Return to the Summary Table.

Memory Results Register

Table 24-60. MEMRES_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R	0h	MEMRESx result register. If DATAFORMAT = 0, unsigned binary: The conversion results are right aligned. In 14 and 12 bit mode, the unused MSB bits are forced to 0. If DATAFORMAT = 1, 2s-complement format: The conversion results are left aligned. In 14 and 12 bit mode, the unused LSB bits are forced to 0. The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back. Reading this register clears the corresponding bit in RIS.

24.4.51 MEMRES_14 Register (Offset = 12B8h) [Reset = 00000000h]

MEMRES_14 is shown in Table 24-61.

Return to the Summary Table.

Memory Results Register

Table 24-61. MEMRES_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R	0h	MEMRESx result register. If DATAFORMAT = 0, unsigned binary: The conversion results are right aligned. In 14 and 12 bit mode, the unused MSB bits are forced to 0. If DATAFORMAT = 1, 2s-complement format: The conversion results are left aligned. In 14 and 12 bit mode, the unused LSB bits are forced to 0. The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back. Reading this register clears the corresponding bit in RIS.

24.4.52 MEMRES_15 Register (Offset = 12BCh) [Reset = 00000000h]

MEMRES_15 is shown in Table 24-62.

Return to the Summary Table.

Memory Results Register

Table 24-62. MEMRES_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R	0h	MEMRESx result register. If DATAFORMAT = 0, unsigned binary: The conversion results are right aligned. In 14 and 12 bit mode, the unused MSB bits are forced to 0. If DATAFORMAT = 1, 2s-complement format: The conversion results are left aligned. In 14 and 12 bit mode, the unused LSB bits are forced to 0. The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back. Reading this register clears the corresponding bit in RIS.

24.4.53 STA Register (Offset = 1340h) [Reset = 00000000h]

STA is shown in Table 24-63.

Return to the Summary Table.

STATUS ULP_ADCHP Status Register 0

Table 24-63. STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	
2	ASCACT	R	0h	ASC active 0h = Idle or done 1h = ASC active
1	REFBUFRDY	R	0h	Indicates reference buffer is powered up. 0h = REFBUF not ready. 1h = REFBUF is ready.
0	BUSY	R	0h	ULP_ADCHP busy. This bit indicates that an active sample or conversion operation is in progress. 0h = No sampling or conversion in progress. 1h = A sample or conversion is in progress.

24.4.54 CONVCTL Register (Offset = 1F14h) [Reset = 00000000h]

CONVCTL is shown in Table 24-64.

Return to the Summary Table.

Conversion Control

Table 24-64. CONVCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	0h	
18	CONVCLKEN	R/W	0h	CONV CLK ICG EN should be enabled after selecting CONV CLK
17-16	CONCLKSEL	R/W	0h	CONVERSION CLOCK SELECTOR ADC functional clock selection 0x0 - (Reset/Default) CLK_GATE 0x1 - SOC_CLK 0x2 - HFXT 0x3 - SOC_PLL_CLK_DIV note: not glitch free, therefore ICG should be enabled after selecting the right clk
15	OV	R/W	0h	OVERRIDE 1 : Override, 0 : Use LUT values LUT is mentioned since the proposal was to pick up values automatically based on Internal vs External reference
14-9	RESERVED	R/W	0h	
8-5	HOLD	R/W	0h	000 : 1 Clock delay, ..., 111 : 8 Clock delay bit[3] - don't care and not used
4-3	PREAMP	R/W	0h	00 : 1 Clock delay, ..., 11 : 4 Clock delay
2-0	DAC	R/W	0h	000 : 1 Clock delay, ..., 111 : 8 Clock delay

24.4.55 CTRL Register (Offset = 1F18h) [Reset = 00000000h]

CTRL is shown in Table 24-65.

Return to the Summary Table.

Table 24-65. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	0h	
16-9	FSBIT1	R/W	20h	FUSE BITS 1 values for fuse OV
8-0	FSBIT0	R/W	0h	FUSE BITS 0 values for fuse OV

24.4.56 MODCTL Register (Offset = 1F1Ch) [Reset = 00000000h]

MODCTL is shown in Table 24-66.

Return to the Summary Table.

MODE CONTROL

Table 24-66. MODCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1	SCASEL	R/W	0h	SCALE SELECT 0 --> Normal output 1 --> scale 0-4223 in 0-4095 (efectively supporting 0-3.3V in 12 bit space)
0	VREFRAN	R/W	0h	VOLTAGE REFERENCE RANGE 0 --> 0 - 4095 in 0 - 3.2V 1 --> 0 - 4095 in 0.1 to 3.3V Only in Single Ended mode

24.4.57 INTCHCTL Register (Offset = 1F20h) [Reset = 00000000h]

INTCHCTL is shown in Table 24-67.

Return to the Summary Table.

INTERNAL CHANNEL CONTROL

Table 24-67. INTCHCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1	RLOV	R/W	0h	RLADDER OVERRIDE Override Enable/Disable control for R-ladder inside RFCIO. This provides divided voltage to ADC by limiting the max. voltage. Default : 0 use value driven by ADC FSM
0	RLVAL	R/W	0h	RLADDER VALUE 0 --> 0 - 4095 in 0 - 3.2V 1 --> 0 - 4095 in 0.1 to 3.3V Only in Single Ended mode

24.4.58 CLKCFG Register (Offset = 2000h) [Reset = 00000000h]

CLKCFG is shown in Table 24-68.

Return to the Summary Table.

ADC CLK CONFIG

Table 24-68. CLKCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	EN	R/W	0h	ENABLE enables system clk to work with ADC '1' - enable adc clk '0' - disable adc clk

Chapter 25

Controller Area Network (CAN)

This chapter describes the Controller Area Network (CAN) module.

25.1 Introduction

This device uses the CAN IP known as DCAN. The DCAN module is implemented for primarily automotive applications. The module has 4KB of message RAM and supports CAN operation up to 1Mbps and 8 bytes of payload. The message RAM has ECC implementation. Two event publishers and two dedicated DMA trigger interfaces are implemented.

25.2 Functions

CAN module on CC35xx supports the following functional requirements:

- Designed based on Bosch MCAN IP
- Conform with CAN Protocol 2.0 A, B and ISO 11898-1:2015
- Supports AUTOSAR and SAE J1939
- Supports Bosch CAN 2.0 A/B protocol with up to 8 message bytes
- Supports up to 1Mbps communication rate in CAN2.0 mode
- Supports up to 32 dedicated transmit buffers
- Supports configurable transmit FIFO for up to 32 elements
- Supports configurable transmit queue for up to 32 elements
- Supports configurable transmit event FIFO for up to 32 elements
- Supports up to 64 dedicated receive buffers
- Supports two configurable receive FIFOs for up to 64 elements each
- Supports up to 128 filter elements
- 4KB embedded SRAM for message buffering
- Supports SECDED ECC (single error correction double error detection) mechanism on message SRAM
- Supports internal and external loop back mode for self-test
- Supports time stamp counters
- Supports clock stop and wakeup feature
- Possiblity to access message RAM and DCAN registers from debugger when DCAN operation is suspended due to CPU halt
- Responds within 50ms to a wakeup CAN message
- Supports all necessary interrupt conditions as implemented in DCAN core IP
- Implementation of 2 DMA triggers for system DMA based data transfer with DCAN
- Have two clock domains - bus interface clock domain (HCLK) and CAN functional clock (CCLK) for bit timing
- The bus interface clock (HCLK) have be same or higher frequency than CAN functional clock (CCLK)
- Have internal clock prescaler to generate lower functional clock frequencies for operation at lower bit rates
- Maintain clock continuity while transitioning between data rates
- CAN interface clock is 80MHz and provided by PRCM module when DCAN is enabled
- CAN functional clock is 80MHz and provided by PRCM module
- Ability to operate alongside RF radio in regards to hardware implementation as well as software handling

25.3 DCAN Subsystem

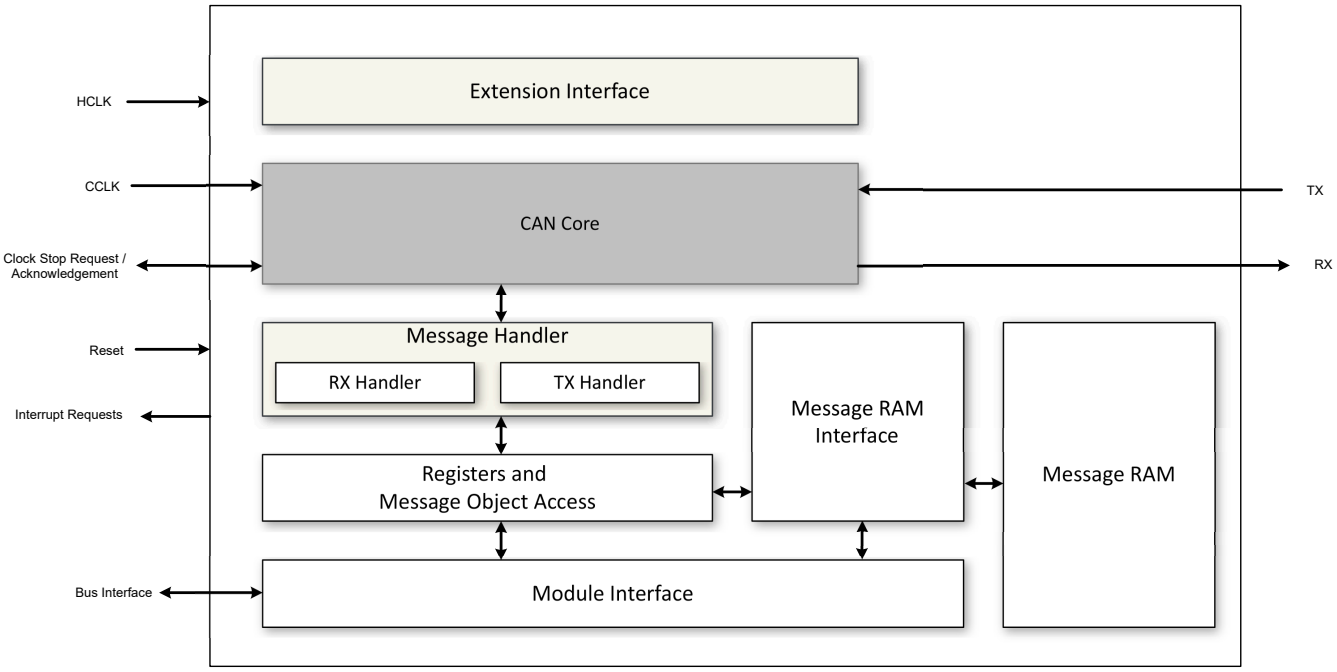


Figure 25-1. DCAN Block Diagram

25.4 DCAN Functional Description

25.4.1 Operating Modes

25.4.1.1 Software Initialization

Software initialization is started by setting bit CCCR.INIT, either by software or by a hardware reset, when an uncorrected bit error is detected in the Message RAM, or by going Bus_Off. While CCCR.INIT is set, message transfer from and to the CAN bus is stopped, the status of the CAN bus output d_can_tx is recessive (HIGH). The counters of the Error Management Logic EML are unchanged. Setting CCCR.INIT does not change any configuration register. Resetting CCCR.INIT finishes the software initialization. Afterwards the Bit Stream Processor BSP synchronizes itself to the data transfer on the CAN bus by waiting for the occurrence of a sequence of 11 consecutive recessive bits (≡ Bus_Idle) before it can take part in bus activities and start the message transfer.

Access to the DCAN configuration registers is only enabled when both bits CCCR.INIT and CCCR.CCE are set (protected write).

CCCR.CCE can only be set/reset while CCCR.INIT = ‘1’. CCCR.CCE is automatically reset when CCCR.INIT is reset.

The following registers are reset when CCCR.CCE is set:

- HPMS - High Priority Message Status
- RXF0S - Rx FIFO 0 Status
- RXF1S - Rx FIFO 1 Status
- TXFQS - Tx FIFO/Queue Status
- TXBRP - Tx Buffer Request Pending
- TXBTO - Tx Buffer Transmission Occurred
- TXBCF - Tx Buffer Cancellation Finished
- TXEFS - Tx Event FIFO Status

The Timeout Counter value TOCV.TOC is preset to the value configured by TOCC.TOP when CCCR.CCE is set.

In addition the state machines of the Tx Handler and Rx Handler are held in idle state while CCCR.CCE = ‘1’.

The following registers are only writeable while CCCR.CCE = ‘0’:

- TXBAR - Tx Buffer Add Request
- TXBCR - Tx Buffer Cancellation Request

CCCR.TEST and CCCR.MON can only be set by the Host while CCCR.INIT = ‘1’ and CCCR.CCE = ‘1’. Both bits may be reset at any time. CCCR.DAR can only be set/reset while CCCR.INIT = ‘1’ and CCCR.CCE = ‘1’.

Note

In case the Message RAM is equipped with parity or ECC functionality, it is recommended to initialize the Message RAM after hardware reset by writing e.g. 0x00000000 to each Message RAM word to create valid parity/ECC checksums. This avoids that reading from uninitialized Message RAM sections will activate interrupt IR.BEU (Bit Error Uncorrected).

25.4.1.2 Normal Operation

Once the DCAN is initialized and CCCR.INIT is reset to zero, the DCAN synchronizes itself to the CAN bus and is ready for communication.

After passing the acceptance filtering, received messages including Message ID and DLC are stored into a dedicated Rx Buffer or into Rx FIFO 0 or Rx FIFO 1.

For messages to be transmitted dedicated Tx Buffers and/or a Tx FIFO or a Tx Queue can be initialized or updated. Automated transmission on reception of remote frames is not implemented.

25.4.1.3 Restricted Operation Mode

In Restricted Operation Mode, the node is able to receive data and remote frames and acknowledge valid frames, but it does not send data frames, remote frames, active error frames, or overload frames. In case of an error condition or overload condition, it does not send dominant bits, instead it waits for the occurrence of bus idle condition to resynchronize itself to the CAN communication. The error counters (ECR.REC, ECR.TEC) are frozen while Error Logging (ECR.CEL) is active. The Host can set the DCAN into Restricted Operation mode by setting bit CCCR.ASM. The bit can only be set by the Host when both CCCR.CCE and CCCR.INIT are set to ‘1’. The bit can be reset by the Host at any time.

Restricted Operation Mode is automatically entered when the Tx Handler was not able to read data from the Message RAM in time. To leave Restricted Operation Mode, the Host CPU has to reset CCCR.ASM.

The Restricted Operation Mode can be used in applications that adapt themselves to different CAN bit rates. In this case the application tests different bit rates and leaves the Restricted Operation Mode after it has received a valid frame.

If the DCAN is connected to a Clock Calibration, CCCR.ASM is controlled by input d_can_cok. In case d_can_cok switches to ‘0’, bit CCCR.ASM is set. When d_can_cok switches back to ‘1’, bit CCCR.ASM returns to the previously written value.When there is no Clock Calibration on CAN unit connected input d_can_cok is hardwired to ‘1’.

Note

The Restricted Operation Mode must not be combined with the Loop Back Mode (internal or external).

25.4.1.4 Bus Monitoring Mode

The DCAN is set in Bus Monitoring Mode by programming CCCR.MON to one. In Bus Monitoring Mode (see ISO 11898-1:2015, 10.14 Bus monitoring), the DCAN is able to receive valid data frames and valid remote frames, but cannot start a transmission. In this mode, it sends only recessive bits on the CAN bus. If the DCAN is required to send a dominant bit (ACK bit, overload flag, active error flag), the bit is rerouted internally so that

the DCAN monitors this dominant bit, although the CAN bus may remain in recessive state. In Bus Monitoring Mode register TXBRP is held in reset state.

The Bus Monitoring Mode can be used to analyze the traffic on a CAN bus without affecting it by the transmission of dominant bits. Figure 25-2 shows the connection of signals d_can_tx and d_can_rx to the DCAN in Bus Monitoring Mode.

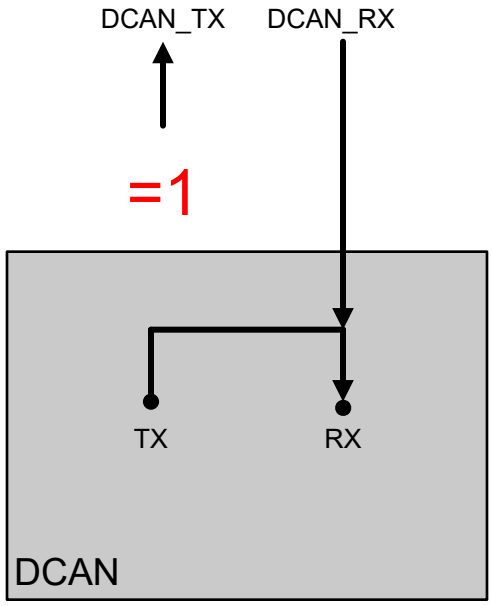


Figure 25-2. Pin Control in Bus Monitoring Mode

25.4.1.5 Disabled Automatic Retransmission

According to the CAN Specification (see ISO 11898-1:2015, 8.3.4 Recovery Management), the DCAN provides means for automatic retransmission of frames that have lost arbitration or that have been disturbed by errors during transmission. By default automatic retransmission is enabled. To support time-triggered communication as described in ISO 11898-1:2015, chapter 9.2, the automatic retransmission may be disabled via CCCR.DAR.

25.4.1.5.1 Frame Transmission in DAR Mode

In DAR mode all transmissions are automatically cancelled after they started on the CAN bus. A Tx Buffer's Tx Request Pending bit TXBRP.TRPx is reset after successful transmission, when a transmission has not yet been started at the point of cancellation, has been aborted due to lost arbitration, or when an error occurred during frame transmission.

- Successful transmission:
  - Corresponding Tx Buffer Transmission Occurred bit TXBTO.TOx set
  - Corresponding Tx Buffer Cancellation Finished bit TXBCF.CFx not set
- Successful transmission in spite of cancellation:
  - Corresponding Tx Buffer Transmission Occurred bit TXBTO.TOx set
  - Corresponding Tx Buffer Cancellation Finished bit TXBCF.CFx set
- Arbitration lost or frame transmission disturbed:
  - Corresponding Tx Buffer Transmission Occurred bit TXBTO.TOx not set
  - Corresponding Tx Buffer Cancellation Finished bit TXBCF.CFx set

In case of a successful frame transmission, and if storage of Tx events is enabled, a Tx Event FIFO element is written with Event Type ET = "10" (transmission in spite of cancellation).

25.4.1.6 Power Down (Sleep Mode)

The DCAN can be set into power down mode controlled by input signal m_can_clkstop_req or via CC Control Register CCCR.CSR. As long as the clock stop request signal d_can_clkstop_req is active, bit CCCR.CSR is read as one.

When all pending transmission requests have completed, the DCAN waits until bus idle state is detected. Then the DCAN sets then CCCR.INIT to one to prevent any further CAN transfers. Now the DCAN acknowledges that it is ready for power down by setting output signal d_can_clkstop_ack to one and CCCR.CSA to one. In this state, before the clocks are switched off, further register accesses can be made. A write access to CCCR.INIT will have no effect. Now the module clock inputs d_can_hclk and d_can_cclk may be switched off.

To leave power down mode, the application has to turn on the module clocks before resetting signal d_can_clkstop_req resp. CC Control Register flag CCCR.CSR. The DCAN will acknowledge this by resetting output signal d_can_clkstop_ack and resetting CCCR.CSA. Afterwards, the application can restart CAN communication by resetting bit CCCR.INIT.

25.4.1.6.1 DCAN clock stop and wake operations

Clock stop in functional mode with wakeup request disabled (WUREQEN =0)

- When CLKCTL.STOPREQ bit is set the clock stop request is asserted at DCAN core input.
- DCAN module completes any ongoing communication and asserts clock stop ack signal at its output.
- The clock stop logic in the DCANSS can use the clock stop ack signal to gate off both HCLK and CCLK to DCAN. DCAN core sets CCCR.INIT bit to 1 while asserting clock stop ack signal.
- Clock stop ack signal when high sets CLKSTA.STPACKSTA bit to 1.
- In this state, DCAN module is fully clock gated and will not be able to receive any data from RXD pin when SSCTL.WUREQEN bit is 0.
- Software has to clear CLKCTL.STOPREQ bit when needed which will de-assert clock stop request upon which both HCLK and CCLK are ungated to DCAN core.
- Then DCAN core de-asserts clock stop ack signal which is used to clear CLKSTA.STPACKSTA bit.
- Software can clear CCCR.INIT to 0 when necessary and put the DCAN module back in operation.

Clock stop in functional mode with wakeup request enabled (WUREQEN = 1, AUTOWU = 0)

- When CLKCTL.STOPREQ is set by software with SSCTL.WUREQEN = 1 and SSCTL.AUTOWU = 0 then the clock stop request is asserted.
- DCAN sets CCCR.INIT = 1 once it becomes idle and then provides clock stop ack signal for gating the HCLK and CCLK.
- Clock stop ack signal when high sets CLKSTA.STPACKSTA bit to 1.
- Now when there is any 1 to 0 transition detected on RXD pin (which is filtered if glitch filter is enabled) while clocks are gated, DCAN asserts clock stop wake request to DCANSS.
- This signal when high clears CLKCTL.STOPREQ bit and sets CLKSTA.STPREQHWOV bit. The purpose is to let software know that stop request was cleared due to hardware override mechanism.
- When clock stop request is de-asserted, HCLK and CCLK are ungated to DCANSS. CLKSTA.STPACKSTA bit is cleared once clock stop ack signal is de-asserted from DCANSS.
- CLKSTA.STPREQHWOV bit will be cleared by hardware when software sets CLKCTL.STOPREQ bit next time for module low power state.
- Clock stop wake request can be used to trigger an interrupt when CLKCTL.WUINTEN bit is set.
- Software can clear CCCR.INIT to 0 and put the DCAN module back in operation.

Clock stop in functional mode with auto wakeup feature enabled (WUREQEN = 1, AUTOWU = 1)

- DCAN operation in the case of clock stop and auto wake up with SSCTL.WUREQEN = 1 and SSCTL.AUTOWU = 1 configuration is similar to SSCTL.WUREQEN = 1 and SSCTL.AUTOWU = 0 except that CCCR.INIT bit will be cleared automatically by the read-modify-write logic in DCANSS.

- When the clocks are ungated due to clock stop wake request upon RXD pin activity, DCAN de-asserts the clock stop ack signal and the hardware mechanism in DCANSS clears CCCR.INIT bit when the clock stop ack signal goes low.
- The CAN bus is a 2-wire differential bus using non-return-to-zero (NRZ) encoding and has two states:
  - Recessive state (logical 1)
  - Dominant state (logical 0)

  In idle state the CAN bus is in Recessive state. The RXD pin activity is considered when this bus goes to dominant state.
- DCAN module is re-enabled automatically by hardware in this scenario and there is no need for software to clear the CCCR.INIT bit.

The wakeup scenarios discussed here are related to device active or idle modes only and not related to standby mode. In active or idle modes the HCLK and CCLK are available at the input of DCAN and gated off inside the module during sleep. When the wakeup condition is received, these clocks are ungated to resume module operation.

In the case of standby scenario, we need to take an interrupt from an IOC/GPIO based on Rx falling edge to wake up the SoC from standby and then reenable clock source like AFOSC and then reconfigure the DCAN registers before the module is put back in operation. This guideline is same as how any other serial communication module is handled for standby exit scenario.

Note

There is no retention of DCAN registers so all register configuration data is lost upon standby entry. DCAN registers have to be reinitialized after wake from standby before the module is put back in operation.

25.4.1.6.2 DCAN debug suspend operation

- The DCAN module implements debug suspend feature. The module operation will suspend when the CPU is halted for debug with SSCTL.DBGSF = 0.
- When CPU halt signal is asserted to DCAN and if SSCTL.DBGSF bit is set to 0, the clock stop request is asserted to DCANSS.
- DCAN completes pending operations and sets CCCR.INIT = 1 once the CAN bus becomes idle and subsequently asserts clock stop ack signal.
- This clock stop ack status is captured in the CCCR.CSA bit but it is not captured in the CLKSTA.STPACKSTA bit within the DCANSS.
- The clock stop ack status in the DCANSS status register is masked based on the clock stop request bit in the CLKCTL register.
- Both HCLK and CCLK continue to run and they are not gated under this condition. This allows debugger accesses to message RAM and CAN registers when the module is stopped.
- When the CPU comes out of debug halt, the clock stop request is de-asserted to DCAN core. CAN core de-asserts clock stop ack signal once the clock stop request is de-asserted.
- At this stage, if SSCTL.AUTOWU = 1 then the read-modify-write mechanism in the DCANSS will automatically make CCCR.INIT = 0 and re-enables DCAN operation.
- If SSCTL.AUTOWU = 0 when clock stop ack signal is de-asserted due to CPU coming out of debug halt, then DCAN operation should be re-enabled by software by clearing the CCCR.INIT bit.
- If there is any activity on RXD pin while DCAN is stopped due to CPU debug halt and if the SSCTL.WUREQEN = 1 then clock stop wake signal will be asserted by DCAN core.
- But this will not take any effect on clock stop request as that is controlled based on debug halt. Clock stop request is de-asserted only when CPU comes out of debug halt.
- Clock stop wake interrupt will not be generated even if CLKCTL.WUINTEN = 1 in this scenario as clock stop wake output from Bosch CAN controller is masked based on the clock stop request bit in the CLKCTL register.

- When CPU halt signal is asserted to DCAN and if SSCTL.DBGSF bit is set to 1, the clock stop request is not asserted and DCAN continues to remain in operational state. The reset value of SSCTL.DBGSF bit is 1 which keeps DCAN operational when CPU halt is asserted.
- During suspend mode the auto-clear feature is disabled. The following register fields have an auto-clear feature:
  - ECR.CEL
  - PSR.LEC
  - PSR.DLEC
  - PSR.RESI
  - PSR.PXE

25.4.1.7 Test Modes

To enable write access to register TEST, bit CCCR.TEST has to be set to one. This allows the configuration of the test modes and test functions.

Four output functions are available for the CAN transmit pin DCAN_TX by programming TEST.TX. Additionally to its default function – the serial data output – it can drive the CAN Sample Point signal to monitor the DCAN's bit timing and it can drive constant dominant or recessive values. The actual value at pin DCAN_RX can be read from TEST.RX. Both functions can be used to check the CAN bus' physical layer.

Due to the synchronization mechanism between CAN clock and Host clock domain, there may be a delay of several Host clock periods between writing to TEST.TX until the new configuration is visible at output pin DCAN_TX. This applies also when reading input pin DCAN_RX via TEST.RX.

Note

Test modes should be used for production tests or self test only. The software control for pin DCAN_TX interferes with all CAN protocol functions. It is not recommended to use test modes for application.

25.4.1.7.1 External Loop Back Mode

The DCAN can be set in External Loop Back Mode by programming TEST.LBCK to one. In Loop Back Mode, the DCAN treats its own transmitted messages as received messages and stores them (if they pass acceptance filtering) into an Rx Buffer or an Rx FIFO. shows the connection of signals m_can_tx and m_can_rx to the DCAN in External Loop Back Mode.

This mode is provided for hardware self-test. To be independent from external stimulation, the DCAN ignores acknowledge errors (recessive bit sampled in the acknowledge slot of a data/remote frame) in Loop Back Mode. In this mode the DCAN performs an internal feedback from its Tx output to its Rx input. The actual value of the DCAN_RX input pin is disregarded by the DCAN. The transmitted messages can be monitored at the DCAN_TX pin.

25.4.1.7.2 Internal Loop Back Mode

Internal Loop Back Mode is entered by programming bits TEST.LBCK and CCCR.MON to one. This mode can be used for a "Hot Selftest", meaning the DCAN can be tested without affecting a running CAN system connected to the pins DCAN_TX and DCAN_RX. In this mode pin DCAN_RX is disconnected from the DCAN and pin DCAN_TX is held recessive. Figure 25-3 shows the connection of DCAN_TX and DCAN_RX to the DCAN in case of Internal Loop Back Mode.

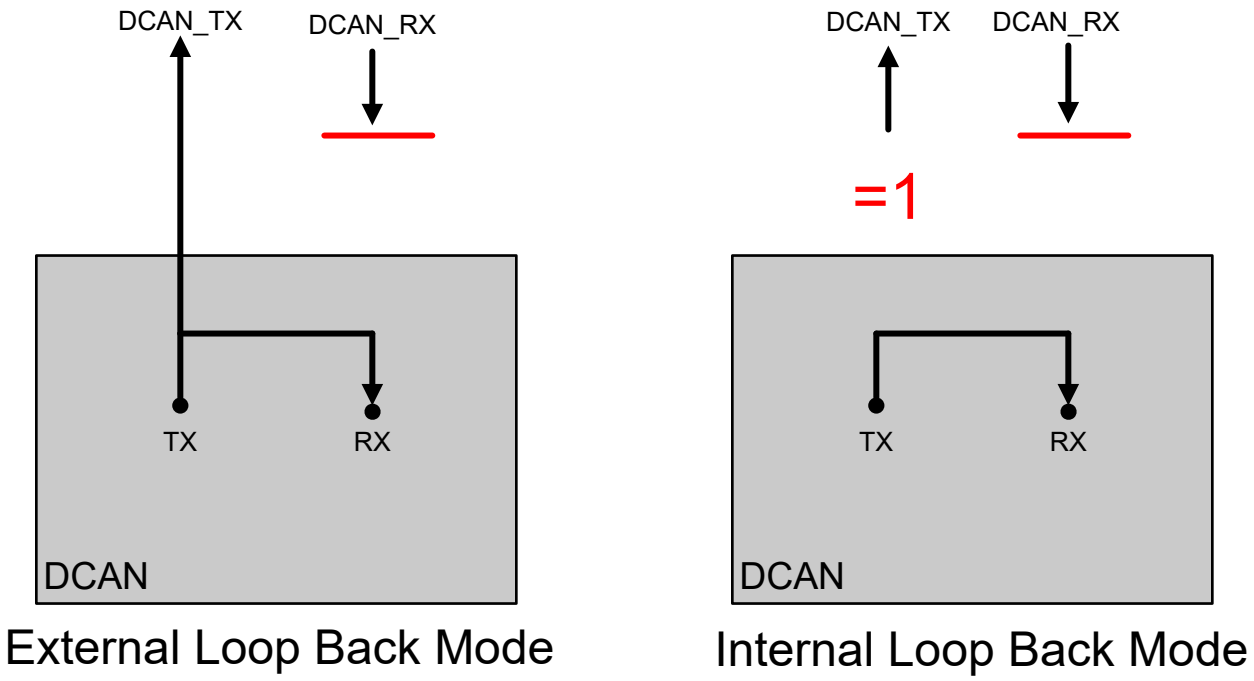


Figure 25-3. Pin Control in Loop Back Modes

25.4.2 Timestamp Generation

The DCAN module has integrated a 16-bit wrap-around counter for timestamp generation. The timestamp counter prescaler TSCC.TCP field can be configured to clock the counter in multiples of CAN bit times (1-16). The counter is readable by way of the TSCV.TSC field. A write access to the TSCV register resets the counter to zero. When the timestamp counter wraps around the interrupt IR.TSW flag is set. On start of a frame reception/ transmission the counter value is captured and stored into the timestamp section of an Rx Buffer/Rx FIFO (RXTS[15:0]) or Tx Event FIFO (TXTS[15:0]) element.

The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx). When TSCC.TSS = “01”, the Timestamp Counter is incremented in multiples of CAN bit times [1…16] depending on the configuration of TSCC.TCP. A wraparound sets interrupt flag IR.TSW.

Write access resets the counter to zero. When TSCC.TSS = “10”, TSC reflects the external Timestamp Counter value. A write access has no impact.

The TSW bit shows the the wraparound for the timer(internal/external) selected for time stamping the Rx/Tx message while EXT_TS_CNTR_OVFL is exclusively for external timestamp counter only.

25.4.2.1 Block Diagram

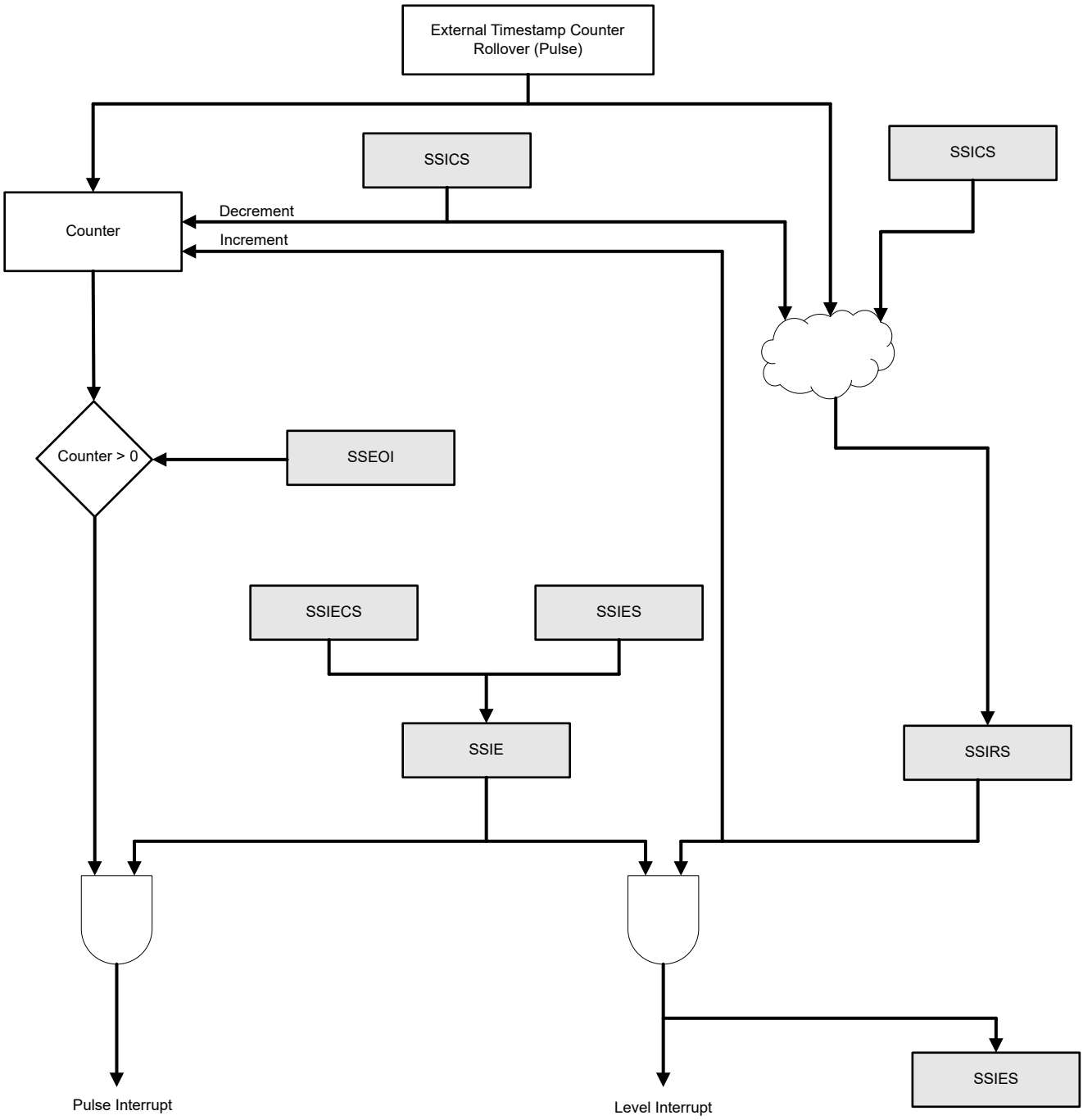


Figure 25-4. External Timestamp Counter Interrupt

25.4.3 Timeout Counter

To signal timeout conditions for Rx FIFO 0, Rx FIFO 1, and the Tx Event FIFO the DCAN supplies a 16-bit Timeout Counter. It operates as down-counter and uses the same prescaler controlled by TSCC.TCP as the Timestamp Counter. The Timeout Counter is configured via register TOCC. The actual counter value can be read from TOCV.TOC. The Timeout Counter can only be started while CCCR.INIT = '0'. It is stopped when CCCR.INIT = '1', e.g. when the DCAN enters Bus_Off state.

The operation mode is selected by TOCC.TOS. When operating in Continuous Mode, the counter starts when CCCR.INIT is reset. A write to TOCV presets the counter to the value configured by TOCC.TOP and continues down-counting.

When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by TOCC.TOP. Down-counting is started when the first FIFO element is stored. Writing to TOCV has no effect.

When the counter reaches zero, interrupt flag IR.TOO is set. In Continuous Mode, the counter is immediately restarted at TOCC.TOP.

Note

The clock signal for the Timeout Counter is derived from the CAN Core's sample point signal. Therefore the point in time where the Timeout Counter is decremented may vary due to the synchronization / re-synchronization mechanism of the CAN Core.

25.4.4 Rx Handling

The Rx Handler controls the acceptance filtering, the transfer of received messages to the Rx Buffers or to one of the two Rx FIFOs, as well as the Rx FIFO's Put and Get Indices.

25.4.4.1 Acceptance Filtering

The DCAN offers the possibility to configure two sets of acceptance filters, one for standard identifiers and one for extended identifiers. These filters can be assigned to an Rx Buffer or to Rx FIFO 0,1. For acceptance filtering each list of filters is executed from element #0 until the first matching element. Acceptance filtering stops at the first matching element. The following filter elements are not evaluated for this message.

The main features are:

- Each filter element can be configured as
  - range filter (from - to)
  - filter for one or two dedicated IDs
  - classic bit mask filter
- Each filter element is configurable for acceptance or rejection filtering
- Each filter element can be enabled / disabled individually
- Filters are checked sequentially, execution stops with the first matching filter element

Related configuration registers are:

- Global Filter Configuration GFC
- Standard ID Filter Configuration SIDFC
- Extended ID Filter Configuration XIDFC
- Extended ID AND Mask XIDAM

Depending on the configuration of the filter element (SFEC/EFEC) a match triggers one of the following actions:

- Store received frame in FIFO 0 or FIFO 1
- Store received frame in Rx Buffer
- Store received frame in Rx Buffer and generate pulse at filter event pin
- Reject received frame
- Set High Priority Message interrupt flag IR.HPM
- Set High Priority Message interrupt flag IR.HPM and store received frame in FIFO 0 or FIFO 1

Acceptance filtering is started after the complete identifier has been received. After acceptance filtering has completed, and if a matching Rx Buffer or Rx FIFO has been found, the Message Handler starts writing the received message data in portions of 32 bit to the matching Rx Buffer or Rx FIFO. If the CAN protocol controller has detected an error condition (e.g. CRC error), this message is discarded with the following impact on the affected Rx Buffer or Rx FIFO:

- Rx Buffer
  - New Data flag of matching Rx Buffer is not set, but Rx Buffer (partly) overwritten with received data. For error type see PSR.LEC respectively PSR.DLEC.
- Rx FIFO
  - Put index of matching Rx FIFO is not updated, but related Rx FIFO element (partly) overwritten with received data. For error type see PSR.LEC respectively PSR.DLEC.

Note

When an accepted message is written to one of the two Rx FIFOs, or into an Rx Buffer, the unmodified received identifier is stored independent of the filter(s) used. The result of the acceptance filter process is strongly depending on the sequence of configured filter elements

25.4.4.1.1 Range Filter

The filter matches for all received frames with Message IDs in the range defined by SF1ID/SF2ID resp. EF1ID/EF2ID.

There are two possibilities when range filtering is used together with extended frames:

- EFT = “00”: The Message ID of received frames is ANDed with the Extended ID AND Mask (XIDAM) before the range filter is applied
- EFT = “11”: The Extended ID AND Mask (XIDAM) is not used for range filtering

25.4.4.1.2 Filter for specific IDs

Afilter element can be configured to filter for one or two specific Message IDs. To filter for one specific Message ID, the filter element has to be configured with SF1ID = SF2ID resp. EF1ID = EF2ID.

25.4.4.1.3 Classic Bit Mask Filter

Classic bit mask filtering is intended to filter groups of Message IDs by masking single bits of a received Message ID.With classic bit mask filtering SF1ID/EF1ID is used as Message ID filter, while SF2ID/EF2ID is used as filter mask.

A zero bit at the filter mask will mask out the corresponding bit position of the configured ID filter, e.g. the value of the received Message ID at that bit position is not relevant for acceptance filtering. Only those bits of the received Message ID where the corresponding mask bits are one are relevant for acceptance filtering.

In case all mask bits are one, a match occurs only when the received Message ID and the Message ID filter are identical. If all mask bits are zero, all Message IDs match.

25.4.4.1.4 Standard Message ID Filtering

Figure 25-5 below shows the flow for standard Message ID (11-bit Identifier) filtering. The Standard Message ID Filter element is described in Section 25.4.7.5.

Controlled by the Global Filter Configuration GFC and the Standard ID Filter Configuration SIDFC Message ID, Remote Transmission Request bit (RTR), and the Identifier Extension bit (IDE) of received frames are compared against the list of configured filter elements.

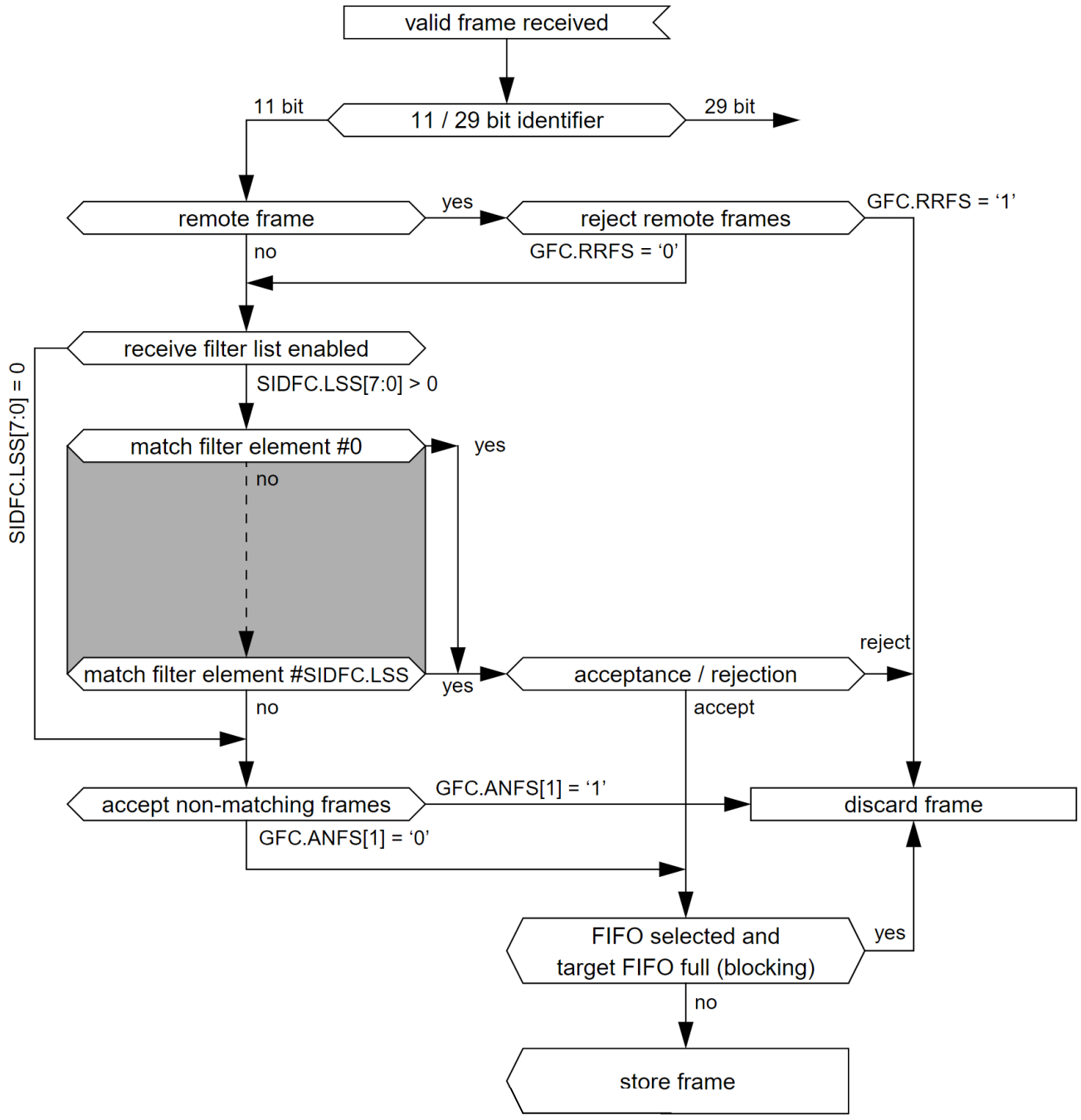


Figure 25-5. Standard Message ID Filter Path

25.4.4.1.5 Extended Message ID Filtering

Figure 25-6 below shows the flow for extended Message ID (29-bit Identifier) filtering. The Extended Message ID Filter element is described in Section 25.4.7.6.

Controlled by the Global Filter Configuration GFC and the Extended ID Filter Configuration XIDFC Message ID, Remote Transmission Request bit (RTR), and the Identifier Extension bit (IDE) of received frames are compared against the list of configured filter elements.

The Extended ID AND Mask XIDAM is ANDed with the received identifier before the filter list is executed.

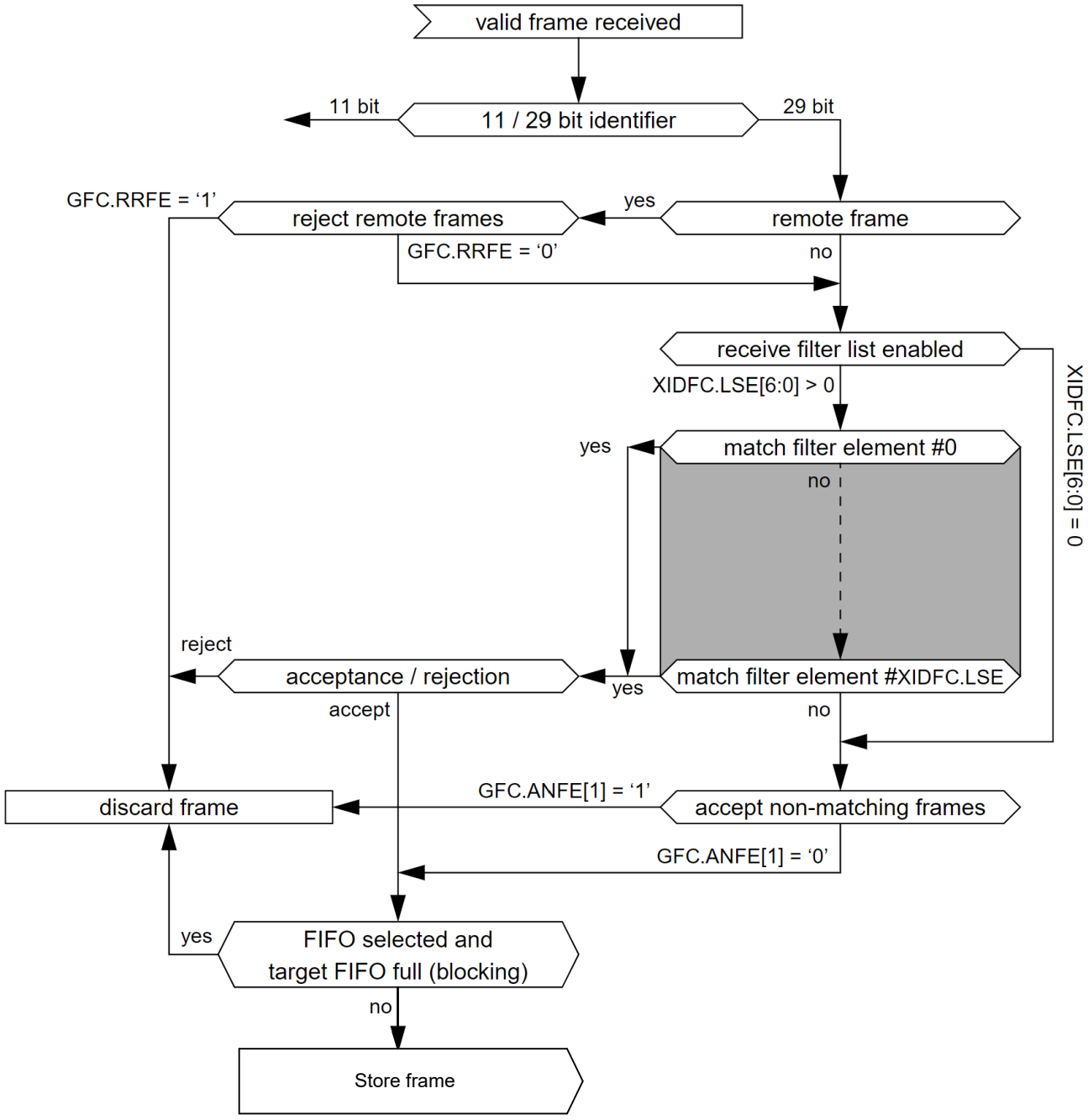


Figure 25-6. Extended Message ID Filter Path

25.4.4.2 Rx FIFOs

Rx FIFO 0 and Rx FIFO 1 can be configured to hold up to 64 elements each. Configuration of the two Rx FIFOs is done via registers RXF0C and RXF1C.

Received messages that passed acceptance filtering are transferred to the Rx FIFO as configured by the matching filter element. For a description of the filter mechanisms available for Rx FIFO 0 and Rx FIFO 1 see Section 25.4.4.1. The Rx FIFO element is described in Section 25.4.7.2.

To avoid an Rx FIFO overflow, the Rx FIFO watermark can be used. When the Rx FIFO fill level reaches the Rx FIFO watermark configured by RXFnC.FnWM, interrupt flag IR.RFnW is set. When the Rx FIFO Put Index reaches the Rx FIFO Get Index an Rx FIFO Full condition is signalled by RXFnS.FnF. In addition interrupt flag IR.RFnF is set.

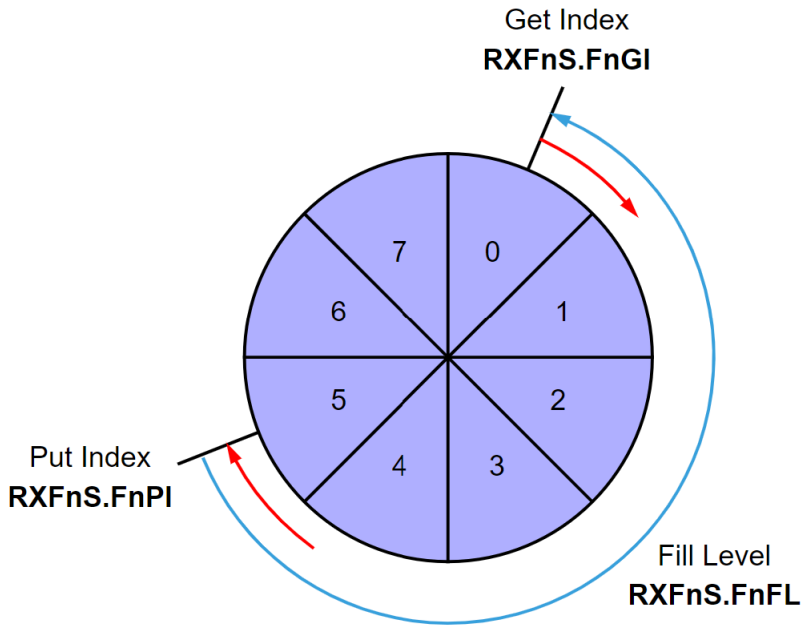


Figure 25-7. Rx FIFO Status

When reading from an Rx FIFO, Rx FIFO Get Index RXFnS.FnGI FIFO • Element Size has to be added to the corresponding Rx FIFO start address RXFnC.FnSA.

Table 25-1. Rx Buffer / FIFO Element Size

RXESC.RBDS[2:0] RXESC.FnDS[2:0]	Data Field [bytes]	FIFO Element Size [RAM words]
000	8	4
001	12	5
010	16	6
011	20	7
100	24	8
101	32	10
110	48	14
111	64	18

25.4.4.2.1 Rx FIFO Blocking Mode

The Rx FIFO blocking mode is configured by RXFnC.FnOM = ‘0’. This is the default operation mode for the Rx FIFOs.

When an Rx FIFO full condition is reached (RXFnS.FnPI = RXFnS.FnGI), no further messages are written to the corresponding Rx FIFO until at least one message has been read out and the Rx FIFO Get Index has been incremented. An Rx FIFO full condition is signalled by RXFnS.FnF = ‘1’. In addition interrupt flag IR.RFnF is set.

In case a message is received while the corresponding Rx FIFO is full, this message is discarded and the message lost condition is signalled by RXFnS.RFnL = ‘1’. In addition interrupt flag IR.RFnL is set.

25.4.4.2.2 Rx FIFO Overwrite Mode

The Rx FIFO overwrite mode is configured by RXFnC.FnOM = ‘1’.

When an Rx FIFO full condition (RXFnS.FnPI = RXFnS.FnGI) is signalled by RXFnS.FnF = ‘1’, the next message accepted for the FIFO will overwrite the oldest FIFO message. Put and get index are both incremented by one.

When an Rx FIFO is operated in overwrite mode and an Rx FIFO full condition is signalled, reading of the Rx FIFO elements should start at least at get index + 1. The reason for that is, that it might happen, that a received message is written to the Message RAM (put index) while the CPU is reading from the Message RAM (get index). In this case inconsistent data may be read from the respective Rx FIFO element. Adding an offset to the get index when reading from the Rx FIFO avoids this problem. The offset depends on how fast the CPU accesses the Rx FIFO. Figure 9 shows an offset of two with respect to the get index when reading the Rx FIFO. In this case the two messages stored in element 1 and 2 are lost.

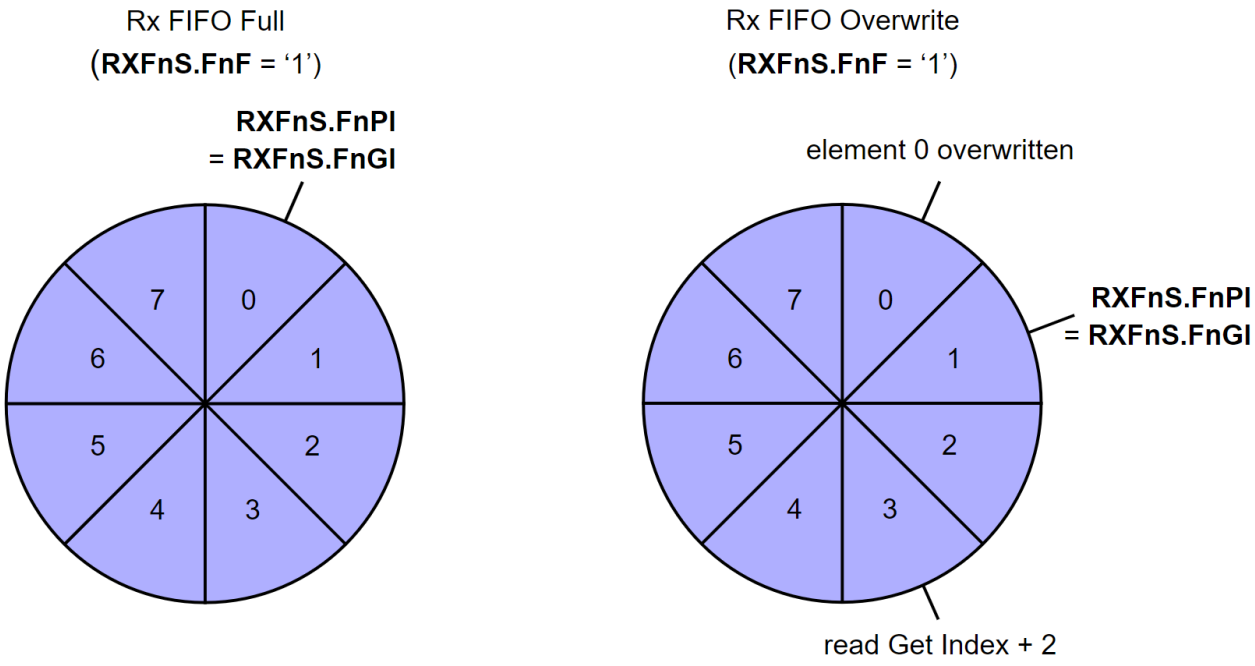


Figure 25-8. Rx FIFO Overflow Handling

After reading from the Rx FIFO, the number of the last element read has to be written to the Rx FIFO Acknowledge Index RXFnA.FnA. This increments the get index to that element number. In case the put index has not been incremented to this Rx FIFO element, the Rx FIFO full condition is reset (RXFnS.FnF = ‘0’).

25.4.4.3 Dedicated Rx Buffers

The DCAN supports up to 64 dedicated Rx Buffers. The start address of the dedicated Rx Buffer section is configured via RXBC.RBSA.

For each Rx Buffer a Standard or Extended Message ID Filter Element with SFEC / EFEC = “111” and SFID2 / EFID2[10:9] = “00” has to be configured (see Section 25.4.7.5 and Section 25.4.7.6).

After a received message has been accepted by a filter element, the message is stored into the Rx Buffer in the Message RAM referenced by the filter element. The format is the same as for an Rx FIFO element. In addition the flag IR.DRX (Message stored in Dedicated Rx Buffer) in the interrupt register is set.

Table 25-2. Example Filter Configuration for Rx Buffers

Filter Element	SFID1[10:0] EFID1[28:0]	SFID2[10:9] EFID2[10:9]	SFID2[5:0] EFID2[5:0]
0	ID message 1	00	00 0000
1	ID message 2	00	00 0001
2	ID message 3	00	00 0010

After the last word of a matching received message has been written to the Message RAM, the respective New Data flag in register NDAT1,2 is set. As long as the New Data flag is set, the respective Rx Buffer is locked against updates from received matching frames. The New Data flags have to be reset by the Host by writing a '1' to the respective bit position.

While an Rx Buffer's New Data flag is set, a Message ID Filter Element referencing this specific Rx Buffer will not match, causing the acceptance filtering to continue. Following Message ID Filter Elements may cause the received message to be stored into another Rx Buffer, or into an Rx FIFO, or the message may be rejected, depending on filter configuration.

25.4.4.3.1 Rx Buffer Handling

- Reset interrupt flag IR.DRX
- Read New Data registers
- Read messages from Message RAM
- Reset New Data flags of processed messages

25.4.4.4 Debug on CAN Support

Debug messages are stored into Rx Buffers. For debug handling three consecutive Rx buffers (e.g. #61, #62, #63) have to be used for storage of debug messages A, B, and C. The format is the same as for an Rx Buffer or an Rx FIFO element (see M_CAN User's Manual section 2.4.2).

Advantage: Fixed start address for the DMA transfers (relative to RXBC.RBSA), no additional configuration required.

For filtering of debug messages Standard / Extended Filter Elements with SFEC / EFEC = "111" have to be set up. Messages matching these filter elements are stored into the Rx Buffers addressed by SFID2 / EFID2[5:0].

After message C has been stored, the DMA request output m_can_dma_req is activated and the three messages can be read from the Message RAM under DMA control. The RAM words holding the debug messages will not be changed by the DCAN while m_can_dma_req is activated. The behaviour is similar to that of an Rx Buffers with its New Data flag set.

After the DMA has completed the DMA unit sets m_can_dma_ack. This resets m_can_dma_req. Now the DCAN is prepared to receive the next set of debug messages.

25.4.4.4.1 Filtering for Debug Messages

Filtering for debug messages is done by configuring one Standard / Extended Message ID Filter Element for each of the three debug messages. To enable a filter element to filter for debug messages SFEC / EFEC has to be programmed to "111". In this case fields SFID1 / SFID2 and EFID1 / EFID2 have a different meaning (see Section 25.4.7.5 and Section 25.4.7.6). While SFID2 / EFID2[10:9] controls the debug message handling state machine, SFID2 / EFID2[5:0] controls the location for storage of a received debug message.

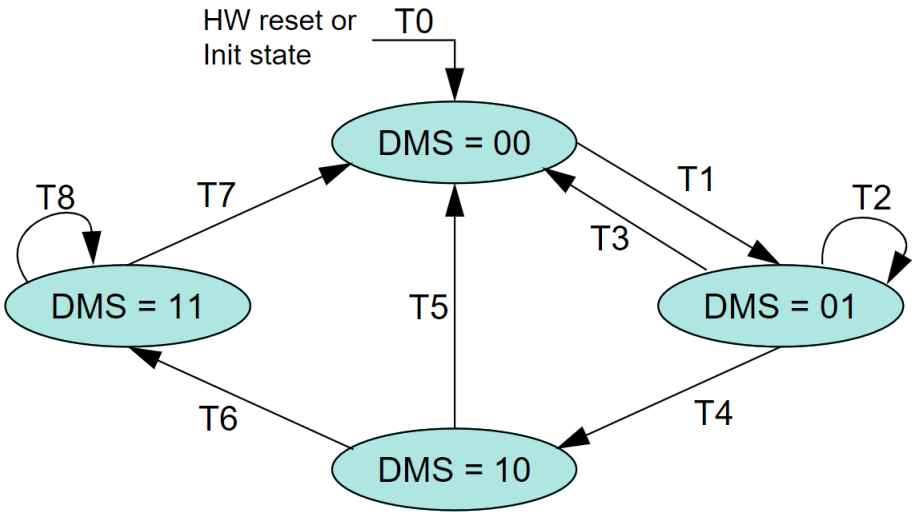
When a debug message is stored, neither the respective New Data flag nor IR.DRX are set. The reception of debug messages can be monitored via RXF1S.DMS.

Table 25-3. Example Filter Configuration for Debug Messages

Filter Element	SFID1[10:0] EFID1[28:0]	SFID2[10:9] EFID2[10:9]	SFID2[5:0] EFID2[5:0]
0	ID debug message A	01	11 1101
1	ID debug message B	10	11 1110
2	ID debug message C	11	11 1111

25.4.4.4.2 Debug Message Handling

The debug message handling state machine assures that debug messages are stored to three consecutive Rx Buffers in correct order. In case of missing messages the process is restarted. The DMArequest is activated only when all three debug messages A, B, C have been received in correct order.



T0: reset m_can_dma_req output, enable reception of debug messages A, B, and C

T1: reception of debug message A

T2: reception of debug message A

T3: reception of debug message C

T4: reception of debug message B

T5: reception of debug messages A, B

T6: reception of debug message C

T7: DMA transfer completed

T8: reception of debug message A,B,C (message rejected)

Figure 25-9. Debug Message Handling State Machine

25.4.5 Tx Handling

The Tx Handler handles transmission requests for the dedicated Tx Buffers, the Tx FIFO, and the Tx Queue. It controls the transfer of transmit messages to the CAN Core, the Put and Get Indices, and the Tx Event FIFO. Up to 32 Tx Buffers can be set up for message transmission. The Tx Buffer element is described in Section 25.4.7.3.

Note

AUTOSAR requires at least three Tx Queue Buffers and support of transmit cancellation.

The Tx Handler starts a Tx scan to check for the highest priority pending Tx request (Tx Buffer with lowest Message ID) when the Tx Buffer Request Pending register TXBRP is updated, or when a transmission has been started.

25.4.5.1 Transmit Pause

The transmit pause feature is intended for use in CAN systems where the CAN message identifiers are (permanently) specified to specific values and cannot easily be changed. These message identifiers may have a higher CAN arbitration priority than other defined messages, while in a specific application their relative arbitration priority should be inverse. This may lead to a case where one ECU sends a burst of CAN messages that cause another ECU's CAN messages to be delayed because that other messages have a lower CAN arbitration priority.

If e.g. CAN ECU-1 has the transmit pause feature enabled and is requested by its application software to transmit four messages, it will, after the first successful message transmission, wait for two CAN bit times of bus idle before it is allowed to start the next requested message. If there are other ECUs with pending messages, those messages are started in the idle time, they would not need to arbitrate with the next message of ECU-1. After having received a message, ECU-1 is allowed to start its next transmission as soon as the received message releases the CAN bus.

The transmit pause feature is controlled by bit CCCR.TXP. If the bit is set, the DCAN will, each time it has successfully transmitted a message, pause for two CAN bit times before starting the next transmission. This enables other CAN nodes in the network to transmit messages even if their messages have lower prior identifiers. Default is transmit pause disabled (CCCR.TXP = '0').

This feature looses up burst transmissions coming from a single node and it protects against "babbling idiot" scenarios where the application program erroneously requests too many transmissions.

25.4.5.2 Dedicated Tx Buffers

Dedicated Tx Buffers are intended for message transmission under complete control of the Host CPU. Each Dedicated Tx Buffer is configured with a specific Message ID. In case that multiple Tx Buffers are configured with the same Message ID, the Tx Buffer with the lowest buffer number is transmitted first.

If the data section has been updated, a transmission is requested by an Add Request via TXBAR.ARn. The requested messages arbitrate internally with messages from an optional Tx FIFO or Tx Queue and externally with messages on the CAN bus, and are sent out according to their Message ID.

A Dedicated Tx Buffer allocates Element Size 32-bit words in the Message RAM (see Table 25-4). Therefore the start address of a dedicated Tx Buffer in the Message RAM is calculated by adding transmit buffer index (0…31) • Element Size to the Tx Buffer Start Address TXBC.TBSA.

Table 25-4. Tx Buffer / FIFO / Queue Element Size

TXESC.TBDS[2:0]	Data Field [bytes]	Element Size [RAM words]
000	8	4
001	12	5
010	16	6
011	20	7
100	24	8
101	32	10
110	48	14
111	64	18

25.4.5.3 Tx FIFO

Tx FIFO operation is configured by programming TXBC.TFQM to '0'. Messages stored in the Tx FIFO are transmitted starting with the message referenced by the Get Index TXFQS.TFGI. After each transmission the Get Index is incremented cyclically until the Tx FIFO is empty. The Tx FIFO enables transmission of messages with the same Message ID from different Tx Buffers in the order these messages have been written to the Tx FIFO. The DCAN calculates the Tx FIFO Free Level TXFQS.TFFL as difference between Get and Put Index. It indicates the number of available (free) Tx FIFO elements.

New transmit messages have to be written to the Tx FIFO starting with the Tx Buffer referenced by the Put Index TXFQS.TFQPI. An Add Request increments the Put Index to the next free Tx FIFO element. When the Put Index reaches the Get Index, Tx FIFO Full (TXFQS.TFQF = ‘1’) is signalled. In this case no further messages should be written to the Tx FIFO until the next message has been transmitted and the Get Index has been incremented.

When a single message is added to the Tx FIFO, the transmission is requested by writing a ‘1’ to the TXBAR bit related to the Tx Buffer referenced by the Tx FIFO’s Put Index.

When multiple (n) messages are added to the Tx FIFO, they are written to n consecutive Tx Buffers starting with the Put Index. The transmissions are then requested via TXBAR. The Put Index is then cyclically incremented by n. The number of requested Tx buffers should not exceed the number of free Tx Buffers as indicated by the Tx FIFO Free Level.

When a transmission request for the Tx Buffer referenced by the Get Index is cancelled, the Get Index is incremented to the next Tx Buffer with pending transmission request and the Tx FIFO Free Level is recalculated. When transmission cancellation is applied to any other Tx Buffer, the Get Index and the FIFO Free Level remain unchanged.

ATx FIFO element allocates Element Size 32-bit words in the Message RAM (see Table 25-4). Therefore the start address of the next available (free) Tx FIFO Buffer is calculated by adding Tx FIFO/Queue Put Index TXFQS.TFQPI (0…31) • Element Size to the Tx Buffer Start Address TXBC.TBSA.

25.4.5.4 Tx Queue

Tx Queue operation is configured by programming TXBC.TFQM to ‘1’. Messages stored in the Tx Queue are transmitted starting with the message with the lowest Message ID (highest priority). In case that multiple Queue Buffers are configured with the same Message ID, the Queue Buffer with the lowest buffer number is transmitted first.

New messages have to be written to the Tx Buffer referenced by the Put Index TXFQS.TFQPI. A n Add Request cyclically increments the Put Index to the next free Tx Buffer. In case that the Tx Queue is full (TXFQS.TFQF = ’1’), the Put Index is not valid and no further message should be written to the Tx Queue until at least one of the requested messages has been sent out or a pending transmission request has been cancelled.

The application may use register TXBRP instead of the Put Index and may place messages to any Tx Buffer without pending transmission request.

ATx Queue Buffer allocates Element Size 32-bit words in the Message RAM (see Table 25-4). Therefore the start address of the next available (free) Tx Queue Buffer is calculated by adding Tx FIFO/Queue Put Index TXFQS.TFQPI (0…31) • Element Size to the Tx Buffer Start Address TXBC.TBSA.

25.4.5.5 Mixed Dedicated Tx Buffers / Tx FIFO

In this case the Tx Buffers section in the Message RAM is subdivided into a set of Dedicated Tx Buffers and a Tx FIFO. The number of Dedicated Tx Buffers is configured by TXBC.NDTB. The number of Tx Buffers assigned to the Tx FIFO is configured by TXBC.TFQS. In case TXBC.TFQS is programmed to zero, only Dedicated Tx Buffers are used.

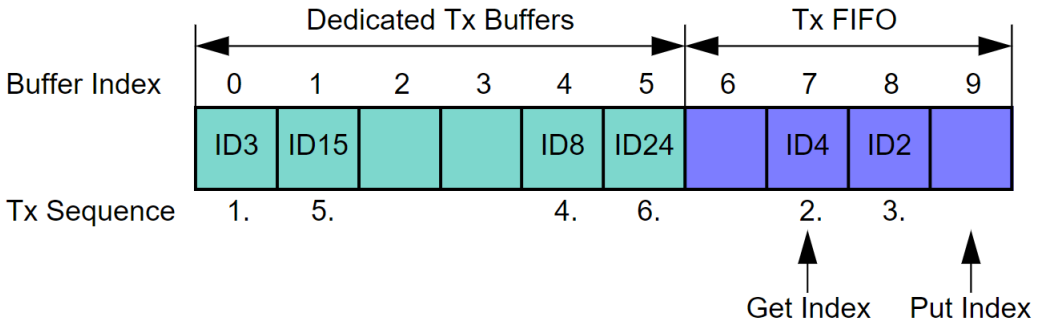


Figure 25-10. Example of Mixed Configuration Dedicated Tx Buffers / Tx FIFO

Tx prioritization:

- Scan Dedicated Tx Buffers and oldest pending Tx FIFO Buffer (referenced by TXFS.TFGI)
- Buffer with lowest Message ID gets highest priority and is transmitted next

25.4.5.6 Mixed Dedicated Tx Buffers / Tx Queue

In this case the Tx Buffers section in the Message RAM is subdivided into a set of Dedicated Tx Buffers and a Tx Queue. The number of Dedicated Tx Buffers is configured by TXBC.NDTB. The number of Tx Queue Buffers is configured by TXBC.TFQS. In case TXBC.TFQS is programmed to zero, only Dedicated Tx Buffers are used.

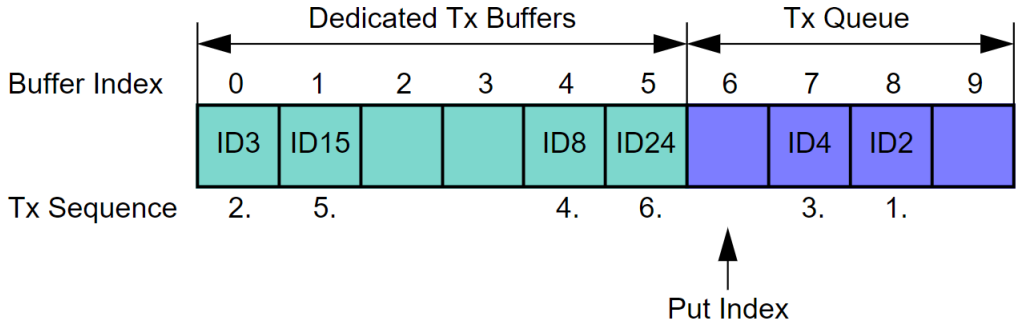


Figure 25-11. Example of mixed Configuration Dedicated Tx Buffers / Tx Queue

Tx prioritization:

- Scan all Tx Buffers with activated transmission request
- Tx Buffer with lowest Message ID gets highest priority and is transmitted next

25.4.5.7 Transmit Cancellation

The DCAN supports transmit cancellation. This feature is especially intended for gateway applications and AUTOSAR based applications. To cancel a requested transmission from a dedicated Tx Buffer or a Tx Queue Buffer the Host has to write a '1' to the corresponding bit position (=number of Tx Buffer) of register TXBCR. Transmit cancellation is not intended for Tx FIFO operation.

Successful cancellation is signalled by setting the corresponding bit of register TXBCF to '1'.

In case a transmit cancellation is requested while a transmission from a Tx Buffer is already ongoing, the corresponding TXBRP bit remains set as long as the transmission is in progress. If the transmission was successful, the corresponding TXBTO and TXBCF bits are set. If the transmission was not successful, it is not repeated and only the corresponding TXBCF bit is set.

Note

In case a pending transmission is cancelled immediately before this transmission could have been started, there follows a short time window where no transmission is started even if another message is also pending in this node. This may enable another node to transmit a message which may have a lower priority than the second message in this node.

25.4.5.8 Tx Event Handling

To support Tx event handling the DCAN has implemented a Tx Event FIFO. After the DCAN has transmitted a message on the CAN bus, Message ID and timestamp are stored in a Tx Event FIFO element. To link a Tx event to a Tx Event FIFO element, the Message Marker from the transmitted Tx Buffer is copied into the Tx Event FIFO element.

The Tx Event FIFO can be configured to a maximum of 32 elements. The Tx Event FIFO element is described in Section 25.4.7.4.

The purpose of the Tx Event FIFO is to decouple handling transmit status information from transmit message handling i.e. a Tx Buffer holds only the message to be transmitted, while the transmit status is stored separately in the Tx Event FIFO. This has the advantage, especially when operating a dynamically managed transmit queue, that a Tx Buffer can be used for a new message immediately after successful transmission. There is no need to save transmit status information from a Tx Buffer before overwriting that Tx Buffer.

When a Tx Event FIFO full condition is signalled by IR.TEFF, no further elements are written to the Tx Event FIFO until at least one element has been read out and the Tx Event FIFO Get Index has been incremented. In case a Tx event occurs while the Tx Event FIFO is full, this event is discarded and interrupt flag IR.TEFL is set.

To avoid a Tx Event FIFO overflow, the Tx Event FIFO watermark can be used. When the Tx Event FIFO fill level reaches the Tx Event FIFO watermark configured by TXEFC.EFWM, interrupt flag IR.TEFW is set.

When reading from the Tx Event FIFO, two times the Tx Event FIFO Get Index TXEFS.EFGI has to be added to the Tx Event FIFO start address TXEFC

25.4.6 FIFO Acknowledge Handling

The Get Indices of Rx FIFO 0, Rx FIFO 1, and the Tx Event FIFO are controlled by writing to the corresponding FIFO Acknowledge Index (see RXF0A, RXF1A, and TXEFA registers). Writing to the FIFO Acknowledge Index will set the FIFO Get Index to the FIFO Acknowledge Index plus one and thereby updates the FIFO Fill Level. There are two use cases:

- When only a single element has been read from the FIFO (the one being pointed to by the Get Index), this Get Index value is written to the FIFO Acknowledge Index.
- When a sequence of elements has been read from the FIFO, it is sufficient to write the FIFO Acknowledge Index only once at the end of that read sequence (value: Index of the last element read), to update the FIFO's Get Index.

Due to the fact that the CPU has free access to the DCAN's Message RAM, special care has to be taken when reading FIFO elements in an arbitrary order (Get Index not considered). This might be useful when reading a High Priority Message from one of the two Rx FIFOs. In this case the FIFO's Acknowledge Index should not be written because this would set the Get Index to a wrong position and also alters the FIFO's Fill Level. In this case some of the older FIFO elements would be lost.

Note

The application has to ensure that a valid value is written to the FIFO Acknowledge Index. The DCAN does not check for erroneous values.

25.4.7 DCAN Message RAM

For storage of Rx/Tx messages and for storage of the filter configuration a single- or dual-ported Message RAM has to be connected to the DCAN module.For storage of Rx/Tx messages and for storage of the filter configuration a single- or dual-ported Message RAM has to be connected to the DCAN module.

Note

In case the Message RAM is equipped with parity or ECC functionality, it is recommended to initialize the Message RAM after hardware reset by writing e.g. 0x00000000 to each Message RAM word to create valid parity/ECC checksums. This avoids that reading from uninitialized Message RAM sections will activate interrupt IR.BEC (Bit Error Corrected) or IR.BEU (Bit Error Uncorrected).

25.4.7.1 Message RAM Configuration

The Message RAM has a width of 32 bits. In case parity checking or ECC is used a respective number of bits has to be added to each word. The DCAN module can be configured to allocate up to 4352 words in the Message RAM. It is not necessary to configure each of the sections listed in Figure below, nor is there any restriction with respect to the sequence of the sections.

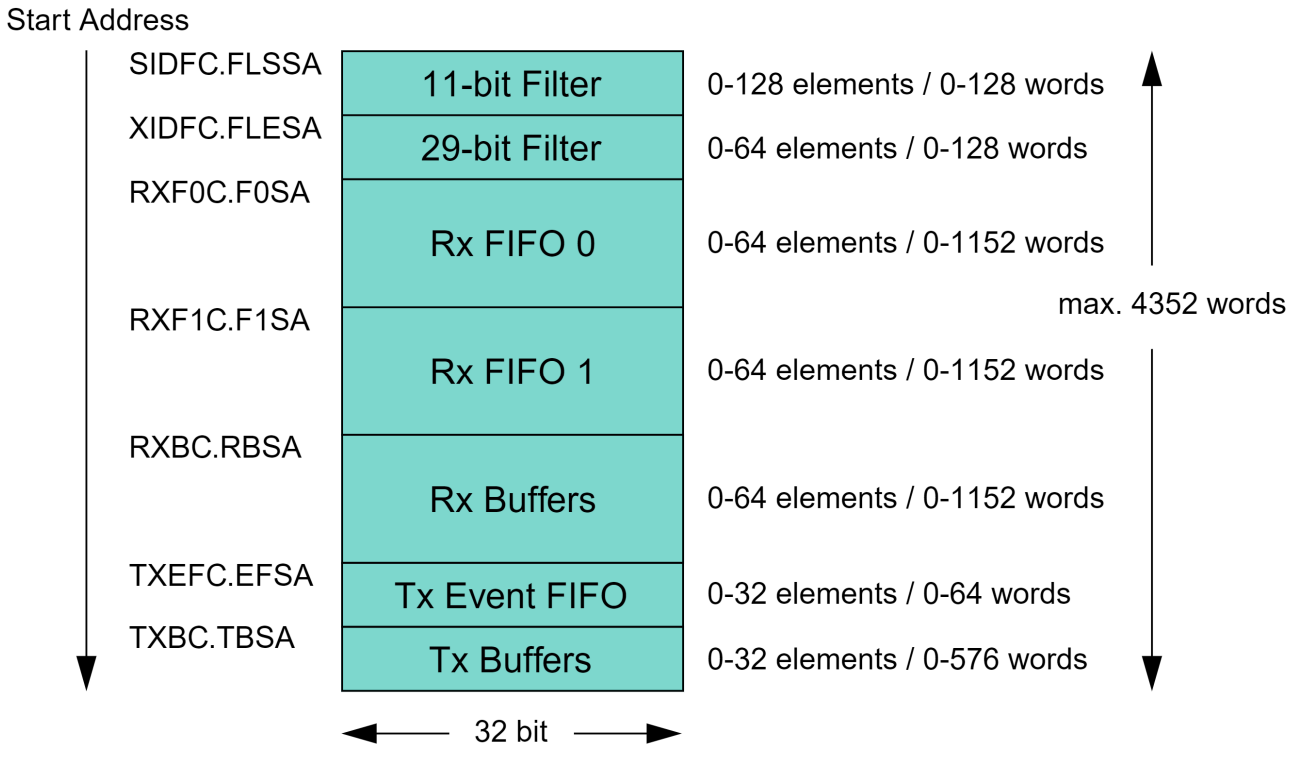


Figure 25-12. DCAN Message RAM Configuration

When the DCAN addresses the Message RAM it addresses 32-bit words, not single bytes. The configurable start addresses are 32-bit word addresses i.e. only bits 15 to 2 are evaluated, the two least significant bits are ignored.

Note

The DCAN does not check for erroneous configuration of the Message RAM. Especially the configuration of the start addresses of the different sections and the number of elements of each section has to be done carefully to avoid falsification or loss of data.

25.4.7.2 Rx Buffer and FIFO Element

Up to 64 Rx Buffers and two Rx FIFOs can be configured in the Message RAM. Each Rx FIFO section can be configured to store up to 64 received messages. The structure of a Rx Buffer / FIFO element is shown in Table 25-5 below.

Table 25-5. Rx Buffer and FIFO Element

RX Buffer/FIFO	Bit	Name	Description
R0	31	ESI	Error State Indicator 0= Transmitting node is error active 0= Transmitting node is error active
	30	XTD	Extended Identifier Signals to the Host whether the received frame has a standard or extended identifier. 0= 11-bit standard identifier 1= 29-bit extended identifier
	29	RTR	Remote Transmission Request Signals to the Host whether the received frame is a data frame or a remote frame. 0= Received frame is a data frame 1= Received frame is a remote frame
	28:0	ID[28:0]	Identifier Standard or extended identifier depending on bit XTD. Astandard identifier is stored into ID[28:18].
R1	31	ANMF	Accepted Non-matching Frame Acceptance of non-matching frames may be enabled via GFC.ANFS and GFC.ANFE. 0= Received frame matching filter index FIDX 1= Received frame did not match any Rx filter element
	30:24	FIDX[6:0]	Filter Index 0-127=Index of matching Rx acceptance filter element (invalid if ANMF = ‘1’). Range is 0 to SIDFC.LSS - 1 resp. XIDFC.LSE - 1.
	18:16	DLC[2:0]	Data Length Code 0-8= CAN received frame has 0-8 data bytes
	15:0	RXTS[15:0]	Rx Timestamp Timestamp Counter value captured on start of frame reception. Resolution depending on configuration of the Timestamp Counter Prescaler TSCC.TCP.
R2	31:24	DB3[7:0]	Data Byte 3
	23:16	DB2[7:0]	Data Byte 2
	15:8	DB1[7:0]	Data Byte 1
	7:0	DB0[7:0]	Data Byte 0
R3	31:24	DB7[7:0]	Data Byte 7
	23:16	DB6[7:0]	Data Byte 6
	15:8	DB5[7:0]	Data Byte 5
	7:0	DB4[7:0]	Data Byte 4

Note

Depending on the configuration of the element size (RXESC), between two and sixteen 32-bit words (Rn = 3 ..17) are used for storage of a CAN message's data field.

25.4.7.3 Tx Buffer Element

The Tx Buffers section can be configured to hold dedicated Tx Buffers as well as a Tx FIFO / Tx Queue. In case that the Tx Buffers section is shared by dedicated Tx buffers and a Tx FIFO / Tx Queue, the dedicated Tx Buffers start at the beginning of the Tx Buffers section followed by the buffers assigned to the Tx FIFO or Tx Queue. The Tx Handler distinguishes between dedicated Tx Buffers and Tx FIFO / Tx Queue by evaluating the Tx Buffer configuration TXBC.TFQS and TXBC.NDTB.

Table 25-6. Tx Buffer Element

Tx Buffer	Bit	Name	Description
T0	30	XTD	Extended Identifier 0= 11-bit standard identifier 1= 29-bit extended identifier
	29	RTR	Remote Transmission Request 0= Transmit data frame 1= Transmit remote frame Note: WhenRTR = 1, the DCAN transmits a remote frame according to ISO 11898-1:2015
	28:0	ID[28:0]	Identifier Standard or extended identifier depending on bit XTD. A standard identifier has to be written to ID[28:18].
T1	31:24	MM[7:0]	Message Marker Written by CPU during Tx Buffer configuration. Copied into Tx Event FIFO element for identification of Tx message status.
	23	EFC	Event FIFO Control 0= Don't store Tx events 1= Store Tx events
	18:16	DLC[2:0]	Data Length Code 0-8= CAN transmit frame has 0-8 data bytes
T2	31:24	DB3[7:0]	Data Byte 3
	23:16	DB2[7:0]	Data Byte 2
	15:8	DB1[7:0]	Data Byte 1
	7:0	DB0[7:0]	Data Byte 0
T3	31:24	DB7[7:0]	Data Byte 7
	23:16	DB6[7:0]	Data Byte 6
	15:8	DB5[7:0]	Data Byte 5
	7:0	DB4[7:0]	Data Byte 4

Note

Depending on the configuration of the element size (TXESC), between two and sixteen 32-bit words (Tn = 3 ..17) are used for storage of a CAN message's data field.

25.4.7.4 Tx Event FIFO Element

Each element stores information about transmitted messages. By reading the Tx Event FIFO the Host CPU gets this information in the order the messages were transmitted. Status information about the Tx Event FIFO can be obtained from register TXEFS.

Table 25-7. Tx Event FIFO Element

Tx Event	Bit	Name	Description
E0	31	ESI	Error State Indicator 0= Transmitting node is error active 1= Transmitting node is error passive
	30	XTD	Extended Identifier 0= 11-bit standard identifier 1= 29-bit extended identifier
	29	RTR	Remote Transmission Request 0= Data frame transmitted 1= Remote frame transmitted
	28:0	ID[28:0]	Identifier Standard or extended identifier depending on bit XTD. A standard identifier has to be written to ID[28:18].
E1	31:24	MM[7:0]	Message Marker Copied from Tx Buffer into Tx Event FIFO element for identification of Tx message status.
	23:22	ET[1:0]	Event Type 00= Reserved 01= Tx event 10= Transmission in spite of cancellation (always set for transmissions in DAR mode) 11= Reserved
	19:16	DLC[3:0]	Data Length Code 0-8= frame with 0-8 data bytes transmitted
	15:0	TXTS[15:0]	Tx Timestamp Timestamp Counter value captured on start of frame transmission. Resolution depending on configuration of the Timestamp Counter Prescaler TSCC.TCP.

25.4.7.5 Standard Message ID Filter Element

Up to 128 filter elements can be configured for 11-bit standard IDs. When accessing a Standard Message ID Filter element, its address is the Filter List Standard Start Address SIDFC.FLSSA plus the index of the filter element (0…127).

Table 25-8. Standard Message ID Filter Element

Standard Message	Bit	Name	Description
S0	31:30	SFT[1:0]	Standard Filter Type 00= Range filter from SFID1 to SFID2 (SFID2 ≥ SFID1) 01= Dual ID filter for SFID1 or SFID2 10= Classic filter: SFID1 = filter, SFID2 = mask 11= Filter element disabled Note: With SFT = “11” the filter element is disabled and the acceptance filtering continues (same behaviour as with SFEC = “000”)
	29:27	SFEC[2:0]	Standard Filter Element Configuration All enabled filter elements are used for acceptance filtering of standard frames. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If SFEC = “100”, “101”, or “110” a match sets interrupt flag IR.HPM and, if enabled, an interrupt is generated. In this case register HPMS is updated with the status of the priority match. 000= Disable filter element 001= Store in Rx FIFO 0 if filter matches 010= Store in Rx FIFO 1 if filter matches 011= Reject ID if filter matches 100= Set priority if filter matches 101= Set priority and store in FIFO 0 if filter matches 110= Set priority and store in FIFO 1 if filter matches 111= Store into Rx Buffer or as debug message, configuration of SFT[1:0] ignored
	26:16	SFID1[10:0]	Standard Filter ID 1 First ID of standard ID filter element. When filtering for Rx Buffers or for debug messages this field defines the ID of a standard message to be stored. The received identifiers must match exactly, no masking mechanism is used
	10:0	SFID2[10:0]	Standard Filter ID 2 This bit field has a different meaning depending on the configuration of SFEC: 1) SFEC = “001”...”110” Second ID of standard ID filter element 2) SFEC = “111” Filter for Rx Buffers or for debug messages SFID2[10:9] decides whether the received message is stored into an Rx Buffer or treated as message A, B, or C of the debug message sequence. 00= Store message into an Rx Buffer 01= Debug Message A 10= Debug Message B 11= Debug Message C SFID2[8:6] is used to control the filter event pins m_can_fe[2:0] at the Extension Interface. Aone at the respective bit position enables generation of a pulse at the related filter event pin with the duration of one m_can_hclk period in case the filter matches. SFID2[5:0] defines the offset to the Rx Buffer Start Address RXBC.RBSA for storage of a matching message.

25.4.7.6 Extended Message ID Filter Element

Up to 64 filter elements can be configured for 29-bit extended IDs. When accessing an Extended Message ID Filter element, its address is the Filter List Extended Start Address XIDFC.FLESA plus two times the index of the filter element (0…63).

Table 25-9. Extended Message ID Filter Element

Standard Message	Bit	Name	Description
F0	31:29	EFEC[2:0]	Extended Filter Element Configuration All enabled filter elements are used for acceptance filtering of extended frames. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If EFEC = “100”, “101”, or “110” a match sets interrupt flag IR.HPM and, if enabled, an interrupt is generated. In this case register HPMS is updated with the status of the priority match. 000= Disable filter element 001= Store in Rx FIFO 0 if filter matches 010= Store in Rx FIFO 1 if filter matches 011= Reject ID if filter matches 100= Set priority if filter matches 101= Set priority and store in FIFO 0 if filter matches 110= Set priority and store in FIFO 1 if filter matches 111= Store into Rx Buffer or as debug message, configuration of EFT[1:0] ignored
	28:0	EFID1[28:0]	Extended Filter ID 1 First ID of extended ID filter element. When filtering for Rx Buffers or for debug messages this field defines the ID of an extended message to be stored. The received identifiers must match exactly, only XIDAM masking mechanism (see Section 25.4.4.1.5, Extended Message ID Filtering) is used.

Table 25-9. Extended Message ID Filter Element (continued)

Standard Message	Bit	Name	Description
F1	31:30	EFT[1:0]	Extended Filter Type 00= Range filter from EFID1 to EFID2 (EFID2 ≥ EFID1) 01= Dual ID filter for EFID1 or EFID2 10= Classic filter: EFID1 = filter, EFID2 = mask 11= Range filter from EFID1 to EFID2 (EFID2 ≥ EFID1), XIDAM mask not applied
	28:0	EFID2[28:0]	Extended Filter ID 2 This bit field has a different meaning depending on the configuration of EFEC: 1) EFEC = “001”...”110” Second ID of extended ID filter element 2) EFEC = “111” Filter for Rx Buffers or for debug messages EFID2[10:9] decides whether the received message is stored into an Rx Buffer or treated as message A, B, or C of the debug message sequence. 00= Store message into an Rx Buffer 01= Debug Message A 10= Debug Message B 11= Debug Message C EFID2[8:6] is used to control the filter event pins m_can_fe[2:0] at the Extension Interface. A one at the respective bit position enables generation of a pulse at the related filter event pin with the duration of one m_can_hclk period in case the filter matches. EFID2[5:0] defines the offset to the Rx Buffer Start Address RXBC.RBSA for storage of a matching message.

25.4.8 Interrupt Requests

The DCAN module provides interrupt and DMA requests. They are configured via the Event Manager. The Suspend Mode is requesting or forcing (based on SSCTL[3] DBGSF bit) the DCAN module to go into initialization mode (see CCCR[0] INIT bit) in which new interrupts and DMA requests will not be issued, that is to prevents the interrupt and DMA requests from propagating to the Event Manager.

The DCAN module has two interrupt lines. There are 30 internal interrupt sources. Each source can be configured to drive one of the two interrupt lines. The interrupts are 'level high' interrupts.

The DCAN core provides two interrupt requests (for Line 0 and Line 1). For more information, see the following registers:

- Interrupt Register (IR)
- Interrupt Enable (IE)
- Interrupt Line Select (ILS)
- Interrupt Line Enable (ILE)

To clear IRQ_INT0, IRQ_INT1 and TS_WAKE interrupts, write to the EOI bit field for the corresponding interrupt number that is described in the EOI register.

The DCAN module is capable of issuing ECC interrupts. After clearing the ECC interrupt source, the application software must also write 1 to EOI register.

The DCAN module supports External Timestamp Counter. When the External Timestamp Counter rolls over it produces an interrupt (see Section 25.4.2).

For more information, see the following registers:

- Interrupt Clear Shadow Register (ICS)
- Interrupt Raw Status Register (IRS)

- Interrupt Enable Clear Shadow Register (IECS)
- Interrupt Enable Register (IE)
- Interrupt Enable Status Register (IES)
- End Of Interrupt Register (EOI)
- External Timestamp Prescaler Register (EXTTSPS)
- External Timestamp Unserviced Interrupts Counter Register (EXTTSUSI)

25.5 DCAN Wrapper

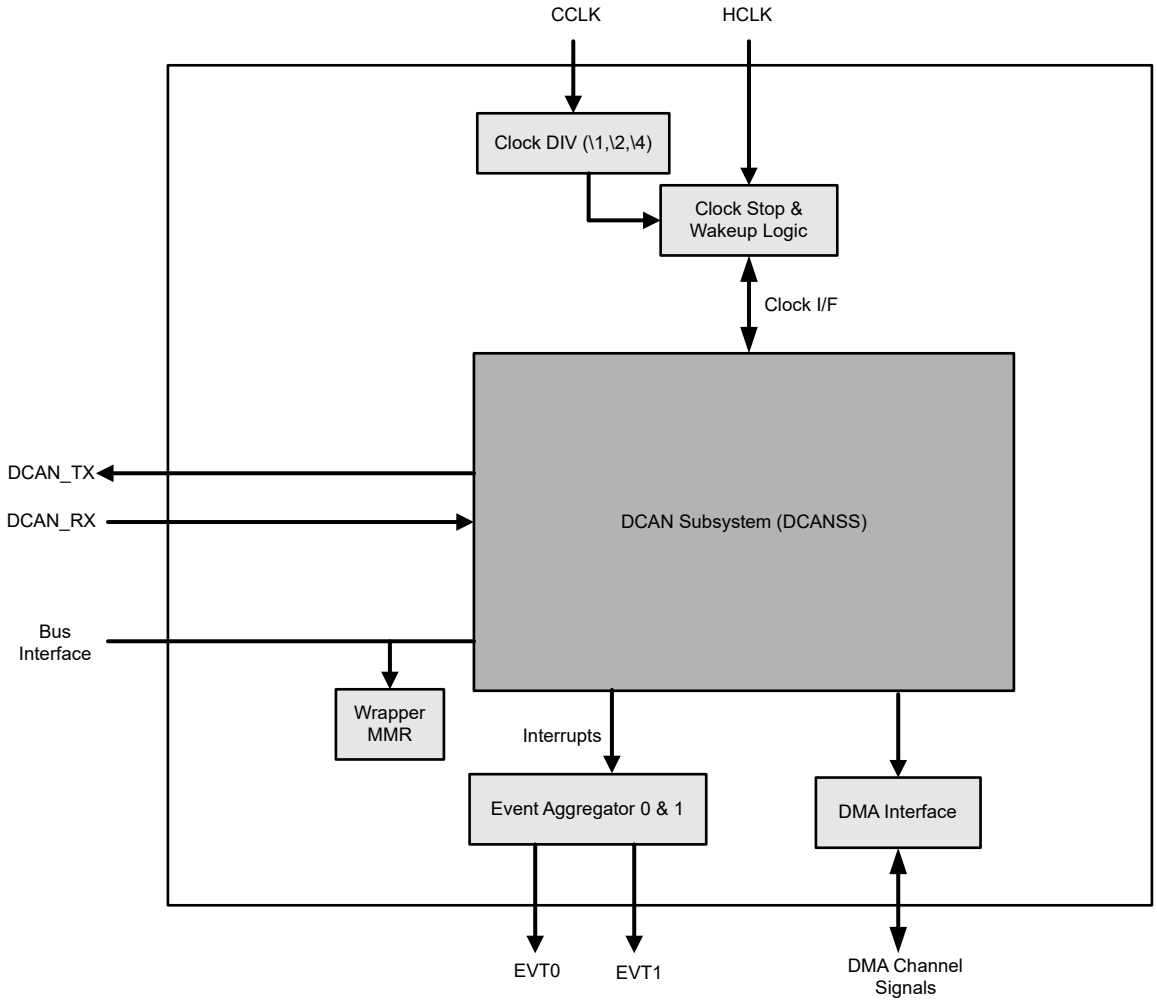


Figure 25-13. DCAN Wrapper

25.6 DCAN Clock Enable

- When the CLKCFG.MEM_CLK_EN is disabled, HCLK is gated to MMRs and RAM and CCLK is gated to DCAN core.
- When the CLKCFG.MEM_CLK_EN is enabled, HCLK is ungated to MMRs and RAM and CCLK is also ungated to DCAN core.

25.7 DCAN Registers

Table 25-10 lists the memory-mapped registers for the DCAN registers. All register offset addresses not listed in Table 25-10 should be considered as reserved locations and the register contents should not be modified.

Table 25-10. DCAN Registers

Offset	Acronym	Register Name	Section
0h	CREL	Core Release	Section 25.7.1
4h	ENDN	Endianness Identifier	Section 25.7.2
Ch	DBTP	Data Bit Timing	Section 25.7.3
10h	TEST	Test Control	Section 25.7.4
14h	RWD	RAM Watchdog Counter	Section 25.7.5
18h	CCCR	Configuration Control Register	Section 25.7.6
1Ch	NBTP	Nominal Bit Timing	Section 25.7.7
20h	TSCC	Timestamp Counter Configuration	Section 25.7.8
24h	TSCV	Timestamp Counter	Section 25.7.9
28h	TOCC	Timeout Counter Configuration	Section 25.7.10
2Ch	TOCV	DCAN Timeout Counter Value	Section 25.7.11
40h	ECR	Error Counter	Section 25.7.12
44h	PSR	Protocol Status	Section 25.7.13
48h	TDCR	DCAN Transmitter Delay Compensation Register	Section 25.7.14
50h	IR	DCAN Interrupt Register	Section 25.7.15
54h	IE	DCAN Interrupt Enable	Section 25.7.16
58h	ILS	Interrupt Line Selection	Section 25.7.17
5Ch	ILE	Interrupt Line Enable	Section 25.7.18
80h	GFC	Global Filter Configuration	Section 25.7.19
84h	SIDFC	Standard Filter Configuration	Section 25.7.20
88h	XIDFC	Extended Filter Configuration	Section 25.7.21
90h	XIDAM	DCAN Extended ID and Mask	Section 25.7.22
94h	HPMS	Priority Message Status	Section 25.7.23
98h	NDAT1	New Data Register	Section 25.7.24
9Ch	NDAT2	DCAN New Data 2	Section 25.7.25
A0h	RXF0C	Receive FIFO Configuration	Section 25.7.26
A4h	RXF0S	Receive FIFO Status	Section 25.7.27
A8h	RXF0A	Receive FIFO Acknowledge	Section 25.7.28
ACh	RXBC	Receive Buffer Configuration	Section 25.7.29
B0h	RXF1C	Receive Buffer Configuration	Section 25.7.30
B4h	RXF1S	Receive FIFO Status	Section 25.7.31
B8h	RXF1A	Receive FIFO Acknowledge	Section 25.7.32
BCh	RXESC	Receive Element Size	Section 25.7.33
C0h	TXBC	Transmit Buffer Configuration	Section 25.7.34
C4h	TXFQS	Transmit Queue Status	Section 25.7.35
C8h	TXESC	Transmit Element Size	Section 25.7.36
CCh	TXBRPAP	Transmit Request Status	Section 25.7.37
D0h	TXBAR	DCAN Tx Buffer Add Request	Section 25.7.38
D4h	TXBCR	DCAN Tx Buffer Cancellation Request	Section 25.7.39
D8h	TXBTO	Transmission Status	Section 25.7.40
DCh	TXBCF	Transmission Cancellation Status	Section 25.7.41

Table 25-10. DCAN Registers (continued)

Offset	Acronym	Register Name	Section
E0h	TXTIE	DCAN Tx Buffer Transmission Interrupt Enable	Section 25.7.42
E4h	TXBCIE	Transmission Cancellation Interrupt	Section 25.7.43
F0h	TXEFC	Transmit Event Configuration	Section 25.7.44
F4h	TXEFS	DCAN Tx Event FIFO Status	Section 25.7.45
F8h	TXEFA	Transmit Event Acknowledgement	Section 25.7.46
200h	SSPID	Subsystem Revision	Section 25.7.47
204h	SSCTL	Subsystem Control	Section 25.7.48
208h	SSSTA	Subsystem Status	Section 25.7.49
20Ch	SSICS	DCAN Subsystem Interrupt Clear Shadow Register	Section 25.7.50
210h	SSIRS	Interrupt Raw Status	Section 25.7.51
214h	SSIECS	Interrupt Disable Register	Section 25.7.52
218h	SSIE	DCAN Subsystem Interrupt Enable Register	Section 25.7.53
21Ch	SSIES	Masked Interrupt Status	Section 25.7.54
220h	SSEOI	Interrupt Completion	Section 25.7.55
224h	EXTTSPS	Timestamp Prescaler	Section 25.7.56
228h	EXTTSUSI	Timestamp Interrupt Counter	Section 25.7.57
400h	ERRREV	Revision Identifier	Section 25.7.58
408h	ERRVEC	Error Controller Selection	Section 25.7.59
40Ch	ERRSTA	Error Status	Section 25.7.60
410h	ERRWRAPREV	Wrapper Revision	Section 25.7.61
414h	ERRCTL	DCAN ECC Control	Section 25.7.62
418h	ERRCTL1	DCAN ECC Error Control 1 Register	Section 25.7.63
41Ch	ERRCTL2	Error Control Configuration	Section 25.7.64
420h	ERRSTA1	DCAN ECC Error Status 1 Register	Section 25.7.65
424h	ERRSTA2	Error Status	Section 25.7.66
428h	ERRSTA3	DCAN ECC Error Status 3 Register	Section 25.7.67
43Ch	SECEOI	Error Correction Acknowledgment	Section 25.7.68
440h	SECSTA	Error Correction Status	Section 25.7.69
480h	SECENSET	Error Correction Enable	Section 25.7.70
4C0h	SECENCLR	Error Correction Enable	Section 25.7.71
53Ch	DEDEOI	DCAN Double Error Detected End of Interrupt Register	Section 25.7.72
540h	DEDSTA	DCAN Double Error Detected Interrupt Status Register	Section 25.7.73
580h	DEDENSET	Error Interrupt Enable	Section 25.7.74
5C0h	DEDENCLR	Error Detection Clear	Section 25.7.75
600h	AGGRENSET	DCAN error Aggregator Enable Set Register	Section 25.7.76
604h	AGGRENCLR	DCAN error Aggregator Enable Clear Register	Section 25.7.77
608h	AGGRSTASET	DCAN error Aggregator Status Set Register	Section 25.7.78
60Ch	AGGRSTACLR	DCAN error Aggregator Status Clear Register	Section 25.7.79
800h	DESC	Module Identification	Section 25.7.80
844h	IMASK0	Interrupt Mask	Section 25.7.81
848h	RIS0	Interrupt Status Flags	Section 25.7.82
84Ch	MIS0	Masked Interrupt Status	Section 25.7.83
850h	ISET0	Interrupt Set Control	Section 25.7.84
854h	ICLR0	Interrupt Clear	Section 25.7.85
868h	IMASK1	Interrupt Mask Control	Section 25.7.86

Table 25-10. DCAN Registers (continued)

Offset	Acronym	Register Name	Section
86Ch	RIS1	Raw Interrupt Status	Section 25.7.87
870h	MIS1	Masked Interrupt Status	Section 25.7.88
874h	ISET1	Interrupt Set Register	Section 25.7.89
878h	ICLR1	Interrupt Clear	Section 25.7.90
904h	CLKDIV	Clock Divider	Section 25.7.91
908h	CLKCTL	Clock Control	Section 25.7.92
90Ch	CLKSTA	Clock Status	Section 25.7.93
924h	DMA0CTL	DMA Control	Section 25.7.94
92Ch	DMA1CTL	DMA Control Register	Section 25.7.95
938h	TTOFE0	Receive Buffer Address	Section 25.7.96
948h	TTOFE1	Receive Buffer Base	Section 25.7.97
950h	TTONDAT1	NDAT1 Value Register	Section 25.7.98
2000h	CLKCFG	Audio clock selection and DCAN IP enable register.	Section 25.7.99

Complex bit access types are encoded to fit into small table cells. Table 25-11 shows the codes that are used for access types in this section.

Table 25-11. DCAN Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
RC	R C	Read to Clear
RS	R S	Read to Set
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
W1S	W 1S	Write 1 to set
W1SQ	W 1S Q	Write 1 to set Qualified. A condition must be met for this operation to occur.
WD	W D	Write Decrement. Decrements the specified bit field by the amount written.
WI	W I	Write Increment. Increments the specified bit field by the amount written.
WQ	W Q	Write Qualified. A condition must be met for this operation to occur.
Reset or Default Value		
-n		Value after reset or the default value

25.7.1 CREL Register (Offset = 0h) [Reset = 32380608h]

CREL is shown in Table 25-12.

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DCAN Core Release Register

Table 25-12. CREL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	REL	R	3h	Core Release. One digit, BCD-coded.
27-24	STEP	R	2h	Step of Core Release. One digit, BCD-coded.
23-20	SUBSTEP	R	3h	Sub-Step of Core Release. One digit, BCD-coded.
19-16	YEAR	R	8h	Time Stamp Year. One digit, BCD-coded.
15-8	MON	R	6h	Time Stamp Month. Two digits, BCD-coded.
7-0	DAY	R	8h	Time Stamp Day. Two digits, BCD-coded.

25.7.2 ENDN Register (Offset = 4h) [Reset = 87654321h]

ENDN is shown in Table 25-13.

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DCAN Endian Register

Table 25-13. ENDN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ETV	R	87654321h	Endianess Test Value. Reading the constant value maintained in this register allows software to determine the endianess of the host CPU.

25.7.3 DBTP Register (Offset = Ch) [Reset = 00000A33h]

DBTP is shown in Table 25-14.

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This register is only writable if bits CCCR.CCE and CCCR.INIT are set. The CAN bit time may be programmed in the range of 4 to 49 time quanta. The CAN time quantum may be programmed in the range of 1 to 32 m_can_cclk periods. tq = (DBRP + 1) mtq. DTSEG1 is the sum of Prop_Seg and Phase_Seg1. DTSEG2 is Phase_Seg2. Therefore the length of the bit time is (programmed values) (DTSEG1 + DTSEG2 + 3) tq or (functional values) (Sync_Seg + Prop_Seg + Phase_Seg1 + Phase_Seg2) tq. The Information Processing Time (IPT) is zero, meaning the data for the next bit is available at the first clock edge after the sample point.

Table 25-14. DBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23	TDC	R/WQ	0h	Transmitter Delay Compensation 0 Transmitter Delay Compensation disabled 1 Transmitter Delay Compensation enabled +I107
22-21	RESERVED	R	0h	Reserved
20-16	DBRP	R/WQ	0h	Data Bit Rate Prescaler. The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-13	RESERVED	R	0h	Reserved
12-8	DTSEG1	R/WQ	Ah	Data Time Segment Before Sample Point. Valid values are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
7-4	DTSEG2	R/WQ	3h	Data Time Segment After Sample Point. Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
3-0	DSJW	R/WQ	3h	Data Resynchronization Jump Width. Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

25.7.4 TEST Register (Offset = 10h) [Reset = 000000X0h]

TEST is shown in Table 25-15.

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Write access to the Test Register has to be enabled by setting bit CCCR.TEST to '1'. All Test Register functions are set to their reset values when bit CCCR.TEST is reset. Loop Back Mode and software control of the internal CAN TX pin are hardware test modes. Programming of TX ? "00" may disturb the message transfer on the CAN bus.

Table 25-15. TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	RX	R	Xh	Receive Pin. Monitors the actual value of the CAN receive pin. 0 The CAN bus is dominant (CAN RX pin = '0') 1 The CAN bus is recessive (CAN RX pin = '1')
6-5	TX	R/WQ	0h	Control of Transmit Pin 00 CAN TX pin controlled by the CAN Core, updated at the end of the CAN bit time 01 Sample Point can be monitored at CAN TX pin 10 Dominant ('0') level at CAN TX pin 11 Recessive ('1') at CAN TX pin Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
4	LBCK	R/WQ	0h	Loop Back Mode 0 Reset value, Loop Back Mode is disabled 1 Loop Back Mode is enabled Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
3-0	RESERVED	R	0h	Reserved

25.7.5 RWD Register (Offset = 14h) [Reset = 00000000h]

RWD is shown in Table 25-16.

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DCAN RAM Watchdog

Table 25-16. RWD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	WDV	R	0h	Watchdog Value. Actual Message RAM Watchdog Counter Value. The RAM Watchdog monitors the READY output of the Message RAM. A Message RAM access via the DCAN's Generic Commander Interface starts the Message RAM Watchdog Counter with the value configured by the WDC field. The counter is reloaded with WDC when the Message RAM signals successful completion by activating its READY output. In case there is no response from the Message RAM until the counter has counted down to zero, the counter stops and interrupt flag DCAN_IR.WDI is set. The RAM Watchdog Counter is clocked by the host (system) clock.
7-0	WDC	R/WQ	0h	Watchdog Configuration. Start value of the Message RAM Watchdog Counter. With the reset value of "00" the counter is disabled. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

25.7.6 CCCR Register (Offset = 18h) [Reset = 00000001h]

CCCR is shown in Table 25-17.

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DCAN CC Control Register

Table 25-17. CCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	NISO	R/WQ	0h	Non ISO Operation. If this bit is set, the DCAN uses the CAN FD frame format as specified by the Bosch CAN FD Specification V1.0. 0 CAN FD frame format according to ISO 11898-1:2015 1 CAN FD frame format according to Bosch CAN FD Specification V1.0
14	TXP	R/WQ	0h	Transmit Pause. If this bit is set, the DCAN pauses for two CAN bit times before starting the next transmission after itself has successfully transmitted a frame. 0 Transmit pause disabled 1 Transmit pause enabled Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
13	EFBI	R/WQ	0h	Edge Filtering during Bus Integration 0 Edge filtering disabled 1 Two consecutive dominant tq required to detect an edge for hard synchronization Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
12	PXHD	R/WQ	0h	Protocol Exception Handling Disable 0 Protocol exception handling enabled 1 Protocol exception handling disabled Note: When protocol exception handling is disabled, the DCAN will transmit an error frame when it detects a protocol exception condition. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
11-10	RESERVED	R	0h	Reserved
9	BRSE	R/WQ	0h	Bit Rate Switch Enable 0 Bit rate switching for transmissions disabled 1 Bit rate switching for transmissions enabled Note: When CAN FD operation is disabled FDOE = '0', BRSE is not evaluated. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
8	FDOE	R/WQ	0h	Flexible Datarate Operation Enable 0 FD operation disabled 1 FD operation enabled Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
7	TEST	R/W1SQ	0h	Test Mode Enable 0 Normal operation, register TEST holds reset values 1 Test Mode, write access to register TEST enabled Qualified Write 1 to Set is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
6	DAR	R/WQ	0h	Disable Automatic Retransmission 0 Automatic retransmission of messages not transmitted successfully enabled 1 Automatic retransmission disabled Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
5	MON	R/W1SQ	0h	Bus Monitoring Mode. Bit MON can only be set by SW when both CCE and INIT are set to '1'. The bit can be reset by SW at any time. 0 Bus Monitoring Mode is disabled 1 Bus Monitoring Mode is enabled Qualified Write 1 to Set is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
4	CSR	R/W	0h	Clock Stop Request 0 No clock stop is requested 1 Clock stop requested. When clock stop is requested, first INIT and then CSA will be set after all pending transfer requests have been completed and the CAN bus reached idle.
3	CSA	R	0h	Clock Stop Acknowledge 0 No clock stop acknowledged 1 DCAN may be set in power down by stopping the Host and CAN clocks
2	ASM	R/W1SQ	0h	Restricted Operation Mode. Bit ASM can only be set by SW when both CCE and INIT are set to '1'. The bit can be reset by SW at any time. 0 Normal CAN operation 1 Restricted Operation Mode active Qualified Write 1 to Set is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

Table 25-17. CCCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CCE	R/WQ	0h	Configuration Change Enable 0 The CPU has no write access to the protected configuration registers 1 The CPU has write access to the protected configuration registers (while CCCR.INIT = '1') Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
0	INIT	R/W	1h	Initialization 0 Normal Operation 1 Initialization is started Note: Due to the synchronization mechanism between the two clock domains, there may be a delay until the value written to INIT can be read back. Therefore the programmer has to assure that the previous value written to INIT has been accepted by reading INIT before setting INIT to a new value.

25.7.7 NBTP Register (Offset = 1Ch) [Reset = 06000A03h]

NBTP is shown in Table 25-18.

Return to the Summary Table.

This register is only writable if bits CCCR.CCE and CCCR.INIT are set. The CAN bit time may be programmed in the range of 4 to 385 time quanta. The CAN time quantum may be programmed in the range of 1 to 512 m_can_cclk periods. tq = (NBRP + 1) mtq. NTSEG1 is the sum of Prop_Seg and Phase_Seg1. NTSEG2 is Phase_Seg2. Therefore the length of the bit time is (programmed values) (NTSEG1 + NTSEG2 + 3) tq or (functional values) (Sync_Seg + Prop_Seg + Phase_Seg1 + Phase_Seg2) tq. The Information Processing Time (IPT) is zero, meaning the data for the next bit is available at the first clock edge after the sample point. Note: With a CAN clock of 8 MHz, the reset value of 0x06000A03 configures the DCAN for a bit rate of 500 kBit/s.

Table 25-18. NBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	NSJW	R/WQ	3h	Nominal (Re)Synchronization Jump Width. Valid values are 0 to 127. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
24-16	NBRP	R/WQ	0h	Nominal Bit Rate Prescaler. The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 511. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-8	NTSEG1	R/WQ	Ah	Nominal Time Segment Before Sample Point. Valid values are 1 to 255. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
7	RESERVED	R	0h	Reserved
6-0	NTSEG2	R/WQ	3h	Nominal Time Segment After Sample Point. Valid values are 1 to 127. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

25.7.8 TSCC Register (Offset = 20h) [Reset = 00000000h]

TSCC is shown in Table 25-19.

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DCAN Timestamp Counter Configuration

Table 25-19. TSCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	TCP	R/WQ	0h	Timestamp Counter Prescaler. Configures the timestamp and timeout counters time unit in multiples of CAN bit times. Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Note: With CAN FD an external counter is required for timestamp generation (TSS = "10"). Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-2	RESERVED	R	0h	Reserved
1-0	TSS	R/WQ	0h	Timestamp Select 00 Timestamp counter value always 0x0000 01 Timestamp counter value incremented according to TCP 10 External timestamp counter value used 11 Same as "00" Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

25.7.9 TSCV Register (Offset = 24h) [Reset = 00000000h]

TSCV is shown in Table 25-20.

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DCAN Timestamp Counter Value

Table 25-20. TSCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	TSC	R/W	0h	Timestamp Counter. The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx). When TSCC.TSS = "01", the Timestamp Counter is incremented in multiples of CAN bit times, (1...16), depending on the configuration of TSCC.TCP. A wrap around sets interrupt flag IR.TSW. Write access resets the counter to zero. When TSCC.TSS = "10", TSC reflects the External Timestamp Counter value, and a write access has no impact. Note: A "wrap around" is a change of the Timestamp Counter value from non-zero to zero not caused by write access to DCAN_TSCV.

25.7.10 TOCC Register (Offset = 28h) [Reset = FFFF0000h]

TOCC is shown in Table 25-21.

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DCAN Timeout Counter Configuration

Table 25-21. TOCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TOP	R/WQ	FFFFh	Timeout Period. Start value of the Timeout Counter (down-counter). Configures the Timeout Period. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-3	RESERVED	R	0h	Reserved
2-1	TOS	R/WQ	0h	Timeout Select. When operating in Continuous mode, a write to TOCV presets the counter to the value configured by TOCC.TOP and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by TOCC.TOP. Down-counting is started when the first FIFO element is stored. 00 Continuous operation 01 Timeout controlled by Tx Event FIFO 10 Timeout controlled by Rx FIFO 0 11 Timeout controlled by Rx FIFO 1 Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
0	ETOC	R/WQ	0h	Enable Timeout Counter 0 Timeout Counter disabled 1 Timeout Counter enabled Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

25.7.11 TOCV Register (Offset = 2Ch) [Reset = 0000FFFFh]

TOCV is shown in Table 25-22.

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DCAN Timeout Counter Value

Table 25-22. TOCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	TOC	R/W	FFFFh	Timeout Counter. The Timeout Counter is decremented in multiples of CAN bit times, (1...16), depending on the configuration of TSCC.TCP. When decremented to zero, interrupt flag IR.TOO is set and the Timeout Counter is stopped. Start and reset/restart conditions are configured via TOCC.TOS.

25.7.12 ECR Register (Offset = 40h) [Reset = 00000000h]

ECR is shown in Table 25-23.

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DCAN Error Counter Register

Table 25-23. ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	CEL	RC	0h	CAN Error Logging. The counter is incremented each time when a CAN protocol error causes the Transmit Error Counter or the Receive Error Counter to be incremented. It is reset by read access to CEL. The counter stops at 0xFF; the next increment of TEC or REC sets interrupt flag IR.ELO. Note: When CCCR.ASM is set, the CAN protocol controller does not increment TEC and REC when a CAN protocol error is detected, but CEL is still incremented.
15	RP	R	0h	Receive Error Passive 0 The Receive Error Counter is below the error passive level of 128 1 The Receive Error Counter has reached the error passive level of 128
14-8	REC	R	0h	Receive Error Counter. Actual state of the Receive Error Counter, values between 0 and 127. Note: When CCCR.ASM is set, the CAN protocol controller does not increment TEC and REC when a CAN protocol error is detected, but CEL is still incremented.
7-0	TEC	R	0h	Transmit Error Counter. Actual state of the Transmit Error Counter, values between 0 and 255. Note: When CCCR.ASM is set, the CAN protocol controller does not increment TEC and REC when a CAN protocol error is detected, but CEL is still incremented.

25.7.13 PSR Register (Offset = 44h) [Reset = 00000707h]

PSR is shown in Table 25-24.

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DCAN Protocol Status Register

Table 25-24. PSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Reserved
22-16	TDCV	R	0h	Transmitter Delay Compensation Value. Position of the secondary sample point, defined by the sum of the measured delay from the internal CAN TX signal to the internal CAN RX signal and TDCR.TDCO. The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point. Valid values are 0 to 127 mtq.
15	RESERVED	R	0h	Reserved
14	PXE	RC	0h	Protocol Exception Event 0 No protocol exception event occurred since last read access 1 Protocol exception event occurred
13	RFDF	RC	0h	Received a CAN FD Message. This bit is set independent of acceptance filtering. 0 Since this bit was reset by the CPU, no CAN FD message has been received 1 Message in CAN FD format with FDF flag set has been received
12	RBRS	RC	0h	BRS Flag of Last Received CAN FD Message. This bit is set together with RFDF, independent of acceptance filtering. 0 Last received CAN FD message did not have its BRS flag set 1 Last received CAN FD message had its BRS flag set
11	RESI	RC	0h	ESI Flag of Last Received CAN FD Message. This bit is set together with RFDF, independent of acceptance filtering. 0 Last received CAN FD message did not have its ESI flag set 1 Last received CAN FD message had its ESI flag set
10-8	DLEC	RS	7h	Data Phase Last Error Code. Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set. Coding is the same as for LEC. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been transferred (reception or transmission) without error.
7	BO	R	0h	Bus_Off Status 0 The M_CAN is not Bus_Off 1 The M_CAN is in Bus_Off state
6	EW	R	0h	Warning Status 0 Both error counters are below the Error_Warning limit of 96 1 At least one of error counter has reached the Error_Warning limit of 96
5	EP	R	0h	Error Passive 0 The M_CAN is in the Error_Active state. It normally takes part in bus communication and sends an active error flag when an error has been detected 1 The M_CAN is in the Error_Passive state
4-3	ACT	R	0h	Node Activity. Monitors the module's CAN communication state. 00 Synchronizing - node is synchronizing on CAN communication 01 Idle - node is neither receiver nor transmitter 10 Receiver - node is operating as receiver 11 Transmitter - node is operating as transmitter Note: ACT is set to "00" by a Protocol Exception Event.

Table 25-24. PSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	LEC	RS	7h	Last Error Code. The LEC indicates the type of the last error to occur on the CAN bus. This field will be cleared to '0' when a message has been transferred (reception or transmission) without error. 0 No Error: No error occurred since LEC has been reset by successful reception or transmission. 1 Stuff Error: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed. 2 Form Error: A fixed format part of a received frame has the wrong format. 3 AckError: The message transmitted by the DCAN was not acknowledged by another node. 4 Bit1Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value '1'), but the monitored bus value was dominant. 5 Bit0Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value '0'), but the monitored bus value was recessive. During Bus_Off recovery this status is set each time a sequence of 11 recessive bits has been monitored. This enables the CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed). 6 CRCError: The CRC check sum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data. 7 NoChange: Any read access to the Protocol Status Register re-initializes the LEC to '7'. When the LEC shows the value '7', no CAN bus event was detected since the last CPU read access to the Protocol Status Register. Note: When a frame in CAN FD format has reached the data phase with BRS flag set, the next CAN event (error or valid frame) will be shown in DLEC instead of LEC. An error in a fixed stuff bit of a CAN FD CRC sequence will be shown as a Form Error, not Stuff Error. Note: The Bus_Off recovery sequence (see ISO 11898-1:2015) cannot be shortened by setting or resetting CCCR.INIT. If the device goes Bus_Off, it will set CCCR.INIT of its own accord, stopping all bus activities. Once CCCR.INIT has been cleared by the CPU, the device will then wait for 129 occurrences of Bus Idle (129 * 11 consecutive recessive bits) before resuming normal operation. At the end of the Bus_Off recovery sequence, the Error Management Counters will be reset. During the waiting time after the resetting of CCCR.INIT, each time a sequence of 11 recessive bits has been monitored, a Bit0Error code is written to PSR.LEC, enabling the CPU to readily check up whether the CAN bus is stuck at dominant or continuously disturbed and to monitor the Bus_Off recovery sequence. ECR.REC is used to count these sequences.

25.7.14 TDCR Register (Offset = 48h) [Reset = 00000000h]

TDCR is shown in Table 25-25.

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DCAN Transmitter Delay Compensation Register

Table 25-25. TDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14-8	TDCO	R/WQ	0h	Transmitter Delay Compensation Offset. Offset value defining the distance between the measured delay from the internal CAN TX signal to the internal CAN RX signal and the secondary sample point. Valid values are 0 to 127 mtq. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
7	RESERVED	R	0h	Reserved
6-0	TDCF	R/WQ	0h	Transmitter Delay Compensation Filter Window Length. Defines the minimum value for the SSP position, dominant edges on the internal CAN RX signal that would result in an earlier SSP position are ignored for transmitter delay measurement. The feature is enabled when TDCF is configured to a value greater than TDCO. Valid values are 0 to 127 mtq. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

25.7.15 IR Register (Offset = 50h) [Reset = 80000000h]

IR is shown in Table 25-26.

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The flags are set when one of the listed conditions is detected (edge-sensitive). The flags remain set until the Host clears them. Aflag is cleared by writing a '1' to the corresponding bit position. Writing a '0' has no effect. Ahard reset will clear the register. The configuration of IE controls whether an interrupt is generated. The configuration of ILS controls on which interrupt line an interrupt is signalled.

Table 25-26. IR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	ARA	R/W1C	0h	Access to Reserved Address 0 No access to reserved address occurred 1 Access to reserved address occurred
28	PED	R/W1C	0h	Protocol Error in Data Phase (Data Bit Time is used) 0 No protocol error in data phase 1 Protocol error in data phase detected (PSR.DLEC ? 0,7)
27	PEA	R/W1C	0h	Protocol Error in Arbitration Phase (Nominal Bit Time is used) 0 No protocol error in arbitration phase 1 Protocol error in arbitration phase detected (PSR.LEC ? 0,7)
26	WDI	R/W1C	0h	Watchdog Interrupt 0 No Message RAM Watchdog event occurred 1 Message RAM Watchdog event due to missing READY
25	BO	R/W1C	0h	Bus_Off Status 0 Bus_Off status unchanged 1 Bus_Off status changed
24	EW	R/W1C	0h	Warning Status 0 Error_Warning status unchanged 1 Error_Warning status changed
23	EP	R/W1C	0h	Error Passive 0 Error_Passive status unchanged 1 Error_Passive status changed
22	ELO	R/W1C	0h	Error Logging Overflow 0 CAN Error Logging Counter did not overflow 1 Overflow of CAN Error Logging Counter occurred
21	BEU	R/W1C	0h	Bit Error Uncorrected. Message RAM bit error detected, uncorrected. This bit is set when a double bit error is detected by the ECC aggregator attached to the Message RAM. An uncorrected Message RAM bit error sets CCCR.INIT to '1'. This is done to avoid transmission of corrupted data. 0 No bit error detected when reading from Message RAM 1 Bit error detected, uncorrected (e.g. parity logic)
20	RESERVED	R	0h	Reserved
19	DRX	R/W1C	0h	Message Stored to Dedicated Rx Buffer. The flag is set whenever a received message has been stored into a dedicated Rx Buffer. 0 No Rx Buffer updated 1 At least one received message stored into an Rx Buffer
18	TOO	R/W1C	0h	Timeout Occurred 0 No timeout 1 Timeout reached
17	MRAF	R/W1C	0h	Message RAM Access Failure. The flag is set, when the Rx Handler: - has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message. - was not able to write a message to the Message RAM. In this case message storage is aborted. In both cases the FIFO put index is not updated resp. the New Data flag for a dedicated Rx Buffer is not set, a partly stored message is overwritten when the next message is stored to this location. The flag is also set when the Tx Handler was not able to read a message from the Message RAM in time. In this case message transmission is aborted. In case of a Tx Handler access failure the DCAN is switched into Restricted Operation Mode. To leave Restricted Operation Mode, the Host CPU has to reset CCCR.ASM. 0 No Message RAM access failure occurred 1 Message RAM access failure occurred

Table 25-26. IR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	TSW	R/W1C	0h	Timestamp Wraparound 0 No timestamp counter wrap-around 1 Timestamp counter wrapped around
15	TEFL	R/W1C	0h	Tx Event FIFO Element Lost 0 No Tx Event FIFO element lost 1 Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero
14	TEFF	R/W1C	0h	Tx Event FIFO Full 0 Tx Event FIFO not full 1 Tx Event FIFO full
13	TEFW	R/W1C	0h	Tx Event FIFO Watermark Reached 0 Tx Event FIFO fill level below watermark 1 Tx Event FIFO fill level reached watermark
12	TEFN	R/W1C	0h	Tx Event FIFO New Entry 0 Tx Event FIFO unchanged 1 Tx Handler wrote Tx Event FIFO element
11	TFE	R/W1C	0h	Tx FIFO Empty 0 Tx FIFO non-empty 1 Tx FIFO empty
10	TCF	R/W1C	0h	Transmission Cancellation Finished 0 No transmission cancellation finished 1 Transmission cancellation finished
9	TC	R/W1C	0h	Transmission Completed 0 No transmission completed 1 Transmission completed
8	HPM	R/W1C	0h	High Priority Message 0 No high priority message received 1 High priority message received
7	RF1L	R/W1C	0h	Rx FIFO 1 Message Lost 0 No Rx FIFO 1 message lost 1 Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero
6	RF1F	R/W1C	0h	Rx FIFO 1 Full 0 Rx FIFO 1 not full 1 Rx FIFO 1 full
5	RF1W	R/W1C	0h	Rx FIFO 1 Watermark Reached 0 Rx FIFO 1 fill level below watermark 1 Rx FIFO 1 fill level reached watermark
4	RF1N	R/W1C	0h	Rx FIFO 1 New Message 0 No new message written to Rx FIFO 1 1 New message written to Rx FIFO 1
3	RF0L	R/W1C	0h	Rx FIFO 0 Message Lost 0 No Rx FIFO 0 message lost 1 Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero
2	RF0F	R/W1C	0h	Rx FIFO 0 Full 0 Rx FIFO 0 not full 1 Rx FIFO 0 full
1	RF0W	R/W1C	0h	Rx FIFO 0 Watermark Reached 0 Rx FIFO 0 fill level below watermark 1 Rx FIFO 0 fill level reached watermark
0	RF0N	R/W1C	0h	Rx FIFO 0 New Message 0 No new message written to Rx FIFO 0 1 New message written to Rx FIFO 0

25.7.16 IE Register (Offset = 54h) [Reset = 00000000h]

IE is shown in Table 25-27.

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DCAN Interrupt Enable

Table 25-27. IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	ARAE	R/W	0h	Access to Reserved Address Enable
28	PEDE	R/W	0h	Protocol Error in Data Phase Enable
27	PEAE	R/W	0h	Protocol Error in Arbitration Phase Enable
26	WDIE	R/W	0h	Watchdog Interrupt Enable
25	BOE	R/W	0h	Bus_Off Status Enable
24	EWE	R/W	0h	Warning Status Enable
23	EPE	R/W	0h	Error Passive Enable
22	ELOE	R/W	0h	Error Logging Overflow Enable
21	BEUE	R/W	0h	Bit Error Uncorrected Enable
20	RESERVED	R/W	0h	
19	DRXE	R/W	0h	Message Stored to Dedicated Rx Buffer Enable
18	TOOE	R/W	0h	Timeout Occurred Enable
17	MRAFE	R/W	0h	Message RAM Access Failure Enable
16	TSWE	R/W	0h	Timestamp Wraparound Enable
15	TEFLE	R/W	0h	Tx Event FIFO Element Lost Enable
14	TEFFE	R/W	0h	Tx Event FIFO Full Enable
13	TEFWE	R/W	0h	Tx Event FIFO Watermark Reached Enable
12	TEFNE	R/W	0h	Tx Event FIFO New Entry Enable
11	TFEE	R/W	0h	Tx FIFO Empty Enable
10	TCFE	R/W	0h	Transmission Cancellation Finished Enable
9	TCE	R/W	0h	Transmission Completed Enable
8	HPME	R/W	0h	High Priority Message Enable
7	RF1LE	R/W	0h	Rx FIFO 1 Message Lost Enable
6	RF1FE	R/W	0h	Rx FIFO 1 Full Enable
5	RF1WE	R/W	0h	Rx FIFO 1 Watermark Reached Enable
4	RF1NE	R/W	0h	Rx FIFO 1 New Message Enable
3	RF0LE	R/W	0h	Rx FIFO 0 Message Lost Enable
2	RF0FE	R/W	0h	Rx FIFO 0 Full Enable
1	RF0WE	R/W	0h	Rx FIFO 0 Watermark Reached Enable
0	RF0NE	R/W	0h	Rx FIFO 0 New Message Enable

25.7.17 ILS Register (Offset = 58h) [Reset = 00000000h]

ILS is shown in Table 25-28.

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The Interrupt Line Select register assigns an interrupt generated by a specific interrupt flag from the Interrupt Register to one of the two module interrupt lines. For interrupt generation the respective interrupt line has to be enabled via ILE.EINT0 and ILE.EINT1.

Table 25-28. ILS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	ARAL	R/W	0h	Access to Reserved Address Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
28	PEDL	R/W	0h	Protocol Error in Data Phase Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
27	PEAL	R/W	0h	Protocol Error in Arbitration Phase Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
26	WDIL	R/W	0h	Watchdog Interrupt Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
25	BOL	R/W	0h	Bus_Off Status Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
24	EWL	R/W	0h	Warning Status Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
23	EPL	R/W	0h	Error Passive Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
22	ELOL	R/W	0h	Error Logging Overflow Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
21	BEUL	R/W	0h	Bit Error Uncorrected Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
20	BECL	R/W	0h	Bit Error Corrected Line A separate interrupt line reserved for corrected bit errors is provided via the DCAN_ERROR_REGS. It advised for the user to use these registers and leave the DCAN_IE.BECE bit cleared to '0' (disabled), thereby relegating this bit to not applicable.
19	DRXL	R/W	0h	Message Stored to Dedicated Rx Buffer Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
18	TOOL	R/W	0h	Timeout Occurred Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
17	MRAFL	R/W	0h	Message RAM Access Failure Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
16	TSWL	R/W	0h	Timestamp Wraparound Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
15	TEFLL	R/W	0h	Tx Event FIFO Element Lost Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
14	TEFFL	R/W	0h	Tx Event FIFO Full Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
13	TEFWL	R/W	0h	Tx Event FIFO Watermark Reached Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
12	TEFNL	R/W	0h	Tx Event FIFO New Entry Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
11	TFEL	R/W	0h	Tx FIFO Empty Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1

Table 25-28. ILS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	TCFL	R/W	0h	Transmission Cancellation Finished Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
9	TCL	R/W	0h	Transmission Completed Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
8	HPML	R/W	0h	High Priority Message Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
7	RF1LL	R/W	0h	Rx FIFO 1 Message Lost Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
6	RF1FL	R/W	0h	Rx FIFO 1 Full Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
5	RF1WL	R/W	0h	Rx FIFO 1 Watermark Reached Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
4	RF1NL	R/W	0h	Rx FIFO 1 New Message Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
3	RF0LL	R/W	0h	Rx FIFO 0 Message Lost Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
2	RF0FL	R/W	0h	Rx FIFO 0 Full Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
1	RF0WL	R/W	0h	Rx FIFO 0 Watermark Reached Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
0	RF0NL	R/W	0h	Rx FIFO 0 New Message Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1

25.7.18 ILE Register (Offset = 5Ch) [Reset = 00000000h]

ILE is shown in Table 25-29.

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DCAN Interrupt Line Enable

Table 25-29. ILE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	EINT1	R/W	0h	Enable Interrupt Line 1 0 Interrupt Line 1 is disabled 1 Interrupt Line 1 is enabled
0	EINT0	R/W	0h	Enable Interrupt Line 0 0 Interrupt Line 0 is disabled 1 Interrupt Line 0 is enabled

25.7.19 GFC Register (Offset = 80h) [Reset = 00000000h]

GFC is shown in Table 25-30.

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DCAN Global Filter Configuration

Table 25-30. GFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-4	ANFS	R/WQ	0h	Accept Non-matching Frames Standard. Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated. 00 Accept in Rx FIFO 0 01 Accept in Rx FIFO 1 10 Reject 11 Reject Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
3-2	ANFE	R/WQ	0h	Accept Non-matching Frames Extended. Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated. 00 Accept in Rx FIFO 0 01 Accept in Rx FIFO 1 10 Reject 11 Reject Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
1	RRFS	R/WQ	0h	Reject Remote Frames Standard 0 Filter remote frames with 11-bit standard IDs 1 Reject all remote frames with 11-bit standard IDs Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
0	RRFE	R/WQ	0h	Reject Remote Frames Extended 0 Filter remote frames with 29-bit extended IDs 1 Reject all remote frames with 29-bit extended IDs Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

25.7.20 SIDFC Register (Offset = 84h) [Reset = 00000000h]

SIDFC is shown in Table 25-31.

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DCAN Standard ID Filter Configuration

Table 25-31. SIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	LSS	R/WQ	0h	List Size Standard 0 No standard Message ID filter 1-128 Number of standard Message ID filter elements >128 Values greater than 128 are interpreted as 128
15-2	FLSSA	R/WQ	0h	Filter List Standard Start Address. Start address of standard Message ID filter list (32-bit word address).
1-0	RESERVED	R	0h	Reserved

25.7.21 XIDFC Register (Offset = 88h) [Reset = 00000000h]

XIDFC is shown in Table 25-32.

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DCAN Extended ID Filter Configuration

Table 25-32. XIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Reserved
22-16	LSE	R/WQ	0h	List Size Extended 0 No extended Message ID filter 1-64 Number of extended Message ID filter elements >64 Values greater than 64 are interpreted as 64 Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-2	FLESA	R/WQ	0h	Filter List Extended Start Address. Start address of extended Message ID filter list (32-bit word address). Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
1-0	RESERVED	R	0h	Reserved

25.7.22 XIDAM Register (Offset = 90h) [Reset = 1FFFFFFFh]

XIDAM is shown in Table 25-33.

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DCAN Extended ID and Mask

Table 25-33. XIDAM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28-0	EIDM	R/WQ	1FFFFFFFh	Extended ID Mask. For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

25.7.23 HPMS Register (Offset = 94h) [Reset = 00000000h]

HPMS is shown in Table 25-34.

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This register is updated every time a Message ID filter element configured to generate a priority event matches. This can be used to monitor the status of incoming high priority messages and to enable fast access to these messages.

Table 25-34. HPMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	FLST	R	0h	Filter List. Indicates the filter list of the matching filter element. 0 Standard Filter List 1 Extended Filter List
14-8	FIDX	R	0h	Filter Index. Index of matching filter element. Range is 0 to SIDFC.LSS - 1 resp. XIDFC.LSE - 1.
7-6	MSI	R	0h	Message Storage Indicator 00 No FIFO selected 01 FIFO message lost 10 Message stored in FIFO 0 11 Message stored in FIFO 1
5-0	BIDX	R	0h	Buffer Index. Index of Rx FIFO element to which the message was stored. Only valid when MSI(1) = '1'.

25.7.24 NDAT1 Register (Offset = 98h) [Reset = 00000000h]

NDAT1 is shown in Table 25-35.

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DCAN New Data 1

Table 25-35. NDAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ND31	R/W1C	0h	New Data RX Buffer 31 0 Rx Buffer not updated 1 Rx Buffer updated from new message
30	ND30	R/W1C	0h	New Data RX Buffer 30 0 Rx Buffer not updated 1 Rx Buffer updated from new message
29	ND29	R/W1C	0h	New Data RX Buffer 29 0 Rx Buffer not updated 1 Rx Buffer updated from new message
28	ND28	R/W1C	0h	New Data RX Buffer 28 0 Rx Buffer not updated 1 Rx Buffer updated from new message
27	ND27	R/W1C	0h	New Data RX Buffer 27 0 Rx Buffer not updated 1 Rx Buffer updated from new message
26	ND26	R/W1C	0h	New Data RX Buffer 26 0 Rx Buffer not updated 1 Rx Buffer updated from new message
25	ND25	R/W1C	0h	New Data RX Buffer 25 0 Rx Buffer not updated 1 Rx Buffer updated from new message
24	ND24	R/W1C	0h	New Data RX Buffer 24 0 Rx Buffer not updated 1 Rx Buffer updated from new message
23	ND23	R/W1C	0h	New Data RX Buffer 23 0 Rx Buffer not updated 1 Rx Buffer updated from new message
22	ND22	R/W1C	0h	New Data RX Buffer 22 0 Rx Buffer not updated 1 Rx Buffer updated from new message
21	ND21	R/W1C	0h	New Data RX Buffer 21 0 Rx Buffer not updated 1 Rx Buffer updated from new message
20	ND20	R/W1C	0h	New Data RX Buffer 20 0 Rx Buffer not updated 1 Rx Buffer updated from new message
19	ND19	R/W1C	0h	New Data RX Buffer 19 0 Rx Buffer not updated 1 Rx Buffer updated from new message
18	ND18	R/W1C	0h	New Data RX Buffer 18 0 Rx Buffer not updated 1 Rx Buffer updated from new message
17	ND17	R/W1C	0h	New Data RX Buffer 17 0 Rx Buffer not updated 1 Rx Buffer updated from new message
16	ND16	R/W1C	0h	New Data RX Buffer 16 0 Rx Buffer not updated 1 Rx Buffer updated from new message
15	ND15	R/W1C	0h	New Data RX Buffer 15 0 Rx Buffer not updated 1 Rx Buffer updated from new message
14	ND14	R/W1C	0h	New Data RX Buffer 14 0 Rx Buffer not updated 1 Rx Buffer updated from new message
13	ND13	R/W1C	0h	New Data RX Buffer 13 0 Rx Buffer not updated 1 Rx Buffer updated from new message
12	ND12	R/W1C	0h	New Data RX Buffer 12 0 Rx Buffer not updated 1 Rx Buffer updated from new message
11	ND11	R/W1C	0h	New Data RX Buffer 11 0 Rx Buffer not updated 1 Rx Buffer updated from new message
10	ND10	R/W1C	0h	New Data RX Buffer 10 0 Rx Buffer not updated 1 Rx Buffer updated from new message
9	ND9	R/W1C	0h	New Data RX Buffer 9 0 Rx Buffer not updated 1 Rx Buffer updated from new message

Table 25-35. NDAT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	ND8	R/W1C	0h	New Data RX Buffer 8 0 Rx Buffer not updated 1 Rx Buffer updated from new message
7	ND7	R/W1C	0h	New Data RX Buffer 7 0 Rx Buffer not updated 1 Rx Buffer updated from new message
6	ND6	R/W1C	0h	New Data RX Buffer 6 0 Rx Buffer not updated 1 Rx Buffer updated from new message
5	ND5	R/W1C	0h	New Data RX Buffer 5 0 Rx Buffer not updated 1 Rx Buffer updated from new message
4	ND4	R/W1C	0h	New Data RX Buffer 4 0 Rx Buffer not updated 1 Rx Buffer updated from new message
3	ND3	R/W1C	0h	New Data RX Buffer 3 0 Rx Buffer not updated 1 Rx Buffer updated from new message
2	ND2	R/W1C	0h	New Data RX Buffer 2 0 Rx Buffer not updated 1 Rx Buffer updated from new message
1	ND1	R/W1C	0h	New Data RX Buffer 1 0 Rx Buffer not updated 1 Rx Buffer updated from new message
0	ND0	R/W1C	0h	New Data RX Buffer 0 0 Rx Buffer not updated 1 Rx Buffer updated from new message

25.7.25 NDAT2 Register (Offset = 9Ch) [Reset = 00000000h]

NDAT2 is shown in Table 25-36.

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DCAN New Data 2

Table 25-36. NDAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ND63	R/W1C	0h	New Data RX Buffer 63 0 Rx Buffer not updated 1 Rx Buffer updated from new message
30	ND62	R/W1C	0h	New Data RX Buffer 62 0 Rx Buffer not updated 1 Rx Buffer updated from new message
29	ND61	R/W1C	0h	New Data RX Buffer 61 0 Rx Buffer not updated 1 Rx Buffer updated from new message
28	ND60	R/W1C	0h	New Data RX Buffer 60 0 Rx Buffer not updated 1 Rx Buffer updated from new message
27	ND59	R/W1C	0h	New Data RX Buffer 59 0 Rx Buffer not updated 1 Rx Buffer updated from new message
26	ND58	R/W1C	0h	New Data RX Buffer 58 0 Rx Buffer not updated 1 Rx Buffer updated from new message
25	ND57	R/W1C	0h	New Data RX Buffer 57 0 Rx Buffer not updated 1 Rx Buffer updated from new message
24	ND56	R/W1C	0h	New Data RX Buffer 56 0 Rx Buffer not updated 1 Rx Buffer updated from new message
23	ND55	R/W1C	0h	New Data RX Buffer 55 0 Rx Buffer not updated 1 Rx Buffer updated from new message
22	ND54	R/W1C	0h	New Data RX Buffer 54 0 Rx Buffer not updated 1 Rx Buffer updated from new message
21	ND53	R/W1C	0h	New Data RX Buffer 53 0 Rx Buffer not updated 1 Rx Buffer updated from new message
20	ND52	R/W1C	0h	New Data RX Buffer 52 0 Rx Buffer not updated 1 Rx Buffer updated from new message
19	ND51	R/W1C	0h	New Data RX Buffer 51 0 Rx Buffer not updated 1 Rx Buffer updated from new message
18	ND50	R/W1C	0h	New Data RX Buffer 50 0 Rx Buffer not updated 1 Rx Buffer updated from new message
17	ND49	R/W1C	0h	New Data RX Buffer 49 0 Rx Buffer not updated 1 Rx Buffer updated from new message
16	ND48	R/W1C	0h	New Data RX Buffer 48 0 Rx Buffer not updated 1 Rx Buffer updated from new message
15	ND47	R/W1C	0h	New Data RX Buffer 47 0 Rx Buffer not updated 1 Rx Buffer updated from new message
14	ND46	R/W1C	0h	New Data RX Buffer 46 0 Rx Buffer not updated 1 Rx Buffer updated from new message
13	ND45	R/W1C	0h	New Data RX Buffer 45 0 Rx Buffer not updated 1 Rx Buffer updated from new message
12	ND44	R/W1C	0h	New Data RX Buffer 44 0 Rx Buffer not updated 1 Rx Buffer updated from new message
11	ND43	R/W1C	0h	New Data RX Buffer 43 0 Rx Buffer not updated 1 Rx Buffer updated from new message
10	ND42	R/W1C	0h	New Data RX Buffer 42 0 Rx Buffer not updated 1 Rx Buffer updated from new message
9	ND41	R/W1C	0h	New Data RX Buffer 41 0 Rx Buffer not updated 1 Rx Buffer updated from new message

Table 25-36. NDAT2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	ND40	R/W1C	0h	New Data RX Buffer 40 0 Rx Buffer not updated 1 Rx Buffer updated from new message
7	ND39	R/W1C	0h	New Data RX Buffer 39 0 Rx Buffer not updated 1 Rx Buffer updated from new message
6	ND38	R/W1C	0h	New Data RX Buffer 38 0 Rx Buffer not updated 1 Rx Buffer updated from new message
5	ND37	R/W1C	0h	New Data RX Buffer 37 0 Rx Buffer not updated 1 Rx Buffer updated from new message
4	ND36	R/W1C	0h	New Data RX Buffer 36 0 Rx Buffer not updated 1 Rx Buffer updated from new message
3	ND35	R/W1C	0h	New Data RX Buffer 35 0 Rx Buffer not updated 1 Rx Buffer updated from new message
2	ND34	R/W1C	0h	New Data RX Buffer 34 0 Rx Buffer not updated 1 Rx Buffer updated from new message
1	ND33	R/W1C	0h	New Data RX Buffer 33 0 Rx Buffer not updated 1 Rx Buffer updated from new message
0	ND32	R/W1C	0h	New Data RX Buffer 32 0 Rx Buffer not updated 1 Rx Buffer updated from new message

25.7.26 RXF0C Register (Offset = A0h) [Reset = 00000000h]

RXF0C is shown in Table 25-37.

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DCAN Rx FIFO 0 Configuration

Table 25-37. RXF0C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F0OM	R/WQ	0h	FIFO 0 Operation Mode. FIFO 0 can be operated in blocking or in overwrite mode. 0 FIFO 0 blocking mode 1 FIFO 0 overwrite mode Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
30-24	F0WM	R/WQ	0h	Rx FIFO 0 Watermark 0 Watermark interrupt disabled 1-64 Level for Rx FIFO 0 watermark interrupt (IR.RF0W) >64 Watermark interrupt disabled Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
23	RESERVED	R	0h	Reserved
22-16	F0S	R/WQ	0h	Rx FIFO 0 Size. The Rx FIFO 0 elements are indexed from 0 to F0S-1. 0 No Rx FIFO 0 1-64 Number of Rx FIFO 0 elements >64 Values greater than 64 are interpreted as 64 Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-2	F0SA	R/WQ	0h	Rx FIFO 0 Start Address. Start address of Rx FIFO 0 in Message RAM (32-bit word address). Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
1-0	RESERVED	R	0h	Reserved

25.7.27 RXF0S Register (Offset = A4h) [Reset = 00000000h]

RXF0S is shown in Table 25-38.

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DCAN Rx FIFO 0 Status

Table 25-38. RXF0S Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	RF0L	R	0h	Rx FIFO 0 Message Lost. This bit is a copy of interrupt flag IR.RF0L. When IR.RF0L is reset, this bit is also reset. 0 No Rx FIFO 0 message lost 1 Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero Note: Overwriting the oldest message when RXF0C.F0OM = '1' will not set this flag.
24	F0F	R	0h	Rx FIFO 0 Full 0 Rx FIFO 0 not full 1 Rx FIFO 0 full
23-22	RESERVED	R	0h	Reserved
21-16	F0PI	R	0h	Rx FIFO 0 Put Index. Rx FIFO 0 write index pointer, range 0 to 63.
15-14	RESERVED	R	0h	Reserved
13-8	F0GI	R	0h	Rx FIFO 0 Get Index. Rx FIFO 0 read index pointer, range 0 to 63.
7	RESERVED	R	0h	Reserved
6-0	F0FL	R	0h	Rx FIFO 0 Fill Level. Number of elements stored in Rx FIFO 0, range 0 to 64.

25.7.28 RXF0A Register (Offset = A8h) [Reset = 00000000h]

RXF0A is shown in Table 25-39.

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DCAN Rx FIFO 0 Acknowledge

Table 25-39. RXF0A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	F0AI	R/W	0h	Rx FIFO 0 Acknowledge Index. After the Host has read a message or a sequence of messages from Rx FIFO 0 it has to write the buffer index of the last element read from Rx FIFO 0 to F0AI. This will set the Rx FIFO 0 Get Index RXF0S.F0GI to F0AI + 1 and update the FIFO 0 Fill Level RXF0S.F0FL.

25.7.29 RXBC Register (Offset = ACh) [Reset = 00000000h]

RXBC is shown in Table 25-40.

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DCAN Rx Buffer Configuration

Table 25-40. RXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-2	RBSA	R/WQ	0h	Rx Buffer Start Address. Configures the start address of the Rx Buffers section in the Message RAM (32-bit word address). +I466
1-0	RESERVED	R	0h	Reserved

25.7.30 RXF1C Register (Offset = B0h) [Reset = 00000000h]

RXF1C is shown in Table 25-41.

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DCAN Rx FIFO 1 Configuration

Table 25-41. RXF1C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F1OM	R/WQ	0h	FIFO 1 Operation Mode. FIFO 1 can be operated in blocking or in overwrite mode. 0 FIFO 1 blocking mode 1 FIFO 1 overwrite mode Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
30-24	F1WM	R/WQ	0h	Rx FIFO 1 Watermark 0 Watermark interrupt disabled 1-64 Level for Rx FIFO 1 watermark interrupt (IR.RF1W) >64 Watermark interrupt disabled Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
23	RESERVED	R	0h	Reserved
22-16	F1S	R/WQ	0h	Rx FIFO 1 Size. The Rx FIFO 1 elements are indexed from 0 to F1S - 1. 0 No Rx FIFO 1 1-64 Number of Rx FIFO 1 elements >64 Values greater than 64 are interpreted as 64 Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-2	F1SA	R/WQ	0h	Rx FIFO 1 Start Address Start address of Rx FIFO 1 in Message RAM (32-bit word address).
1-0	RESERVED	R	0h	Reserved

25.7.31 RXF1S Register (Offset = B4h) [Reset = 00000000h]

RXF1S is shown in Table 25-42.

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DCAN Rx FIFO 1 Status

Table 25-42. RXF1S Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	DMS	R	0h	Debug Message Status 00 Idle state, wait for reception of debug messages, DMA request is cleared 01 Debug message A received 10 Debug messages A, B received 11 Debug messages A, B, C received, DMA request is set
29-26	RESERVED	R	0h	Reserved
25	RF1L	R	0h	Rx FIFO 1 Message Lost. This bit is a copy of interrupt flag IR.RF1L. When IR.RF1L is reset, this bit is also reset. 0 No Rx FIFO 1 message lost 1 Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero Note: Overwriting the oldest message when RXF1C.F1OM = '1' will not set this flag.
24	F1F	R	0h	Rx FIFO 1 Full 0 Rx FIFO 1 not full 1 Rx FIFO 1 full
23-22	RESERVED	R	0h	Reserved
21-16	F1PI	R	0h	Rx FIFO 1 Put Index. Rx FIFO 1 write index pointer, range 0 to 63.
15-14	RESERVED	R	0h	Reserved
13-8	F1GI	R	0h	Rx FIFO 1 Get Index. Rx FIFO 1 read index pointer, range 0 to 63.
7	RESERVED	R	0h	Reserved
6-0	F1FL	R	0h	Rx FIFO 1 Fill Level. Number of elements stored in Rx FIFO 1, range 0 to 64.

25.7.32 RXF1A Register (Offset = B8h) [Reset = 00000000h]

RXF1A is shown in Table 25-43.

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DCAN Rx FIFO 1 Acknowledge

Table 25-43. RXF1A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	F1AI	R/W	0h	Rx FIFO 1 Acknowledge Index. After the Host has read a message or a sequence of messages from Rx FIFO 1 it has to write the buffer index of the last element read from Rx FIFO 1 to F1AI. This will set the Rx FIFO 1 Get Index RXF1S.F1GI to F1AI + 1 and update the FIFO 1 Fill Level RXF1S.F1FL.

25.7.33 RXESC Register (Offset = BCh) [Reset = 00000000h]

RXESC is shown in Table 25-44.

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Configures the number of data bytes belonging to an Rx Buffer / Rx FIFO element. Data field sizes >8 bytes are intended for CAN FD operation only.

Table 25-44. RXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-8	RBDS	R/WQ	0h	Rx Buffer Data Field Size 000 8 byte data field 001 12 byte data field 010 16 byte data field 011 20 byte data field 100 24 byte data field 101 32 byte data field 110 48 byte data field 111 64 byte data field Note: In case the data field size of an accepted CAN frame exceeds the data field size configured for the matching Rx Buffer or Rx FIFO, only the number of bytes as configured by RXESC are stored to the Rx Buffer resp. Rx FIFO element. The rest of the frame's data field is ignored. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
7	RESERVED	R	0h	Reserved
6-4	F1DS	R/WQ	0h	Rx FIFO 1 Data Field Size 000 8 byte data field 001 12 byte data field 010 16 byte data field 011 20 byte data field 100 24 byte data field 101 32 byte data field 110 48 byte data field 111 64 byte data field Note: In case the data field size of an accepted CAN frame exceeds the data field size configured for the matching Rx Buffer or Rx FIFO, only the number of bytes as configured by RXESC are stored to the Rx Buffer resp. Rx FIFO element. The rest of the frame's data field is ignored. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
3	RESERVED	R	0h	Reserved
2-0	F0DS	R/WQ	0h	Rx FIFO 0 Data Field Size 000 8 byte data field 001 12 byte data field 010 16 byte data field 011 20 byte data field 100 24 byte data field 101 32 byte data field 110 48 byte data field 111 64 byte data field Note: In case the data field size of an accepted CAN frame exceeds the data field size configured for the matching Rx Buffer or Rx FIFO, only the number of bytes as configured by RXESC are stored to the Rx Buffer resp. Rx FIFO element. The rest of the frame's data field is ignored. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

25.7.34 TXBC Register (Offset = C0h) [Reset = 00000000h]

TXBC is shown in Table 25-45.

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DCAN Tx Buffer Configuration

Table 25-45. TXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	TFQM	R/WQ	0h	Tx FIFO/Queue Mode 0 Tx FIFO operation 1 Tx Queue operation Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
29-24	TFQS	R/WQ	0h	Transmit FIFO/Queue Size 0 No Tx FIFO/Queue 1-32 Number of Tx Buffers used for Tx FIFO/Queue >32 Values greater than 32 are interpreted as 32 Note: Be aware that the sum of TFQS and NDTB may be not greater than 32. There is no check for erroneous configurations. The Tx Buffers section in the Message RAM starts with the dedicated Tx Buffers. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
23-22	RESERVED	R	0h	Reserved
21-16	NDTB	R/WQ	0h	Number of Dedicated Transmit Buffers 0 No Dedicated Tx Buffers 1-32 Number of Dedicated Tx Buffers >32 Values greater than 32 are interpreted as 32 Note: Be aware that the sum of TFQS and NDTB may be not greater than 32. There is no check for erroneous configurations. The Tx Buffers section in the Message RAM starts with the dedicated Tx Buffers. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-2	TBSA	R/WQ	0h	Tx Buffers Start Address. Start address of Tx Buffers section in Message RAM (32-bit word address). Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
1-0	RESERVED	R	0h	Reserved

25.7.35 TXFQS Register (Offset = C4h) [Reset = 00000000h]

TXFQS is shown in Table 25-46.

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The Tx FIFO/Queue status is related to the pending Tx requests listed in register TXBRP. Therefore the effect of Add/Cancellation requests may be delayed due to a running Tx scan (TXBRP not yet updated).

Table 25-46. TXFQS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0h	Reserved
21	TFQF	R	0h	Tx FIFO/Queue Full 0 Tx FIFO/Queue not full 1 Tx FIFO/Queue full
20-16	TFQP	R	0h	Tx FIFO/Queue Put Index. Tx FIFO/Queue write index pointer, range 0 to 31. Note: In case of mixed configurations where dedicated Tx Buffers are combined with a Tx FIFO or a Tx Queue, the Put and Get Indices indicate the number of the Tx Buffer starting with the first dedicated Tx Buffers. Example: For a configuration of 12 dedicated Tx Buffers and a Tx FIFO of 20 Buffers a Put Index of 15 points to the fourth buffer of the Tx FIFO.
15-13	RESERVED	R	0h	Reserved
12-8	TFGI	R	0h	Tx FIFO Get Index. Tx FIFO read index pointer, range 0 to 31. Read as zero when Tx Queue operation is configured (TXBC.TFQM = '1'). Note: In case of mixed configurations where dedicated Tx Buffers are combined with a Tx FIFO or a Tx Queue, the Put and Get Indices indicate the number of the Tx Buffer starting with the first dedicated Tx Buffers. Example: For a configuration of 12 dedicated Tx Buffers and a Tx FIFO of 20 Buffers a Put Index of 15 points to the fourth buffer of the Tx FIFO.
7-6	RESERVED	R	0h	Reserved
5-0	TFFL	R	0h	Tx FIFO Free Level. Number of consecutive free Tx FIFO elements starting from TFGI, range 0 to 32. Read as zero when Tx Queue operation is configured (TXBC.TFQM = '1').

25.7.36 TXESC Register (Offset = C8h) [Reset = 00000000h]

TXESC is shown in Table 25-47.

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Configures the number of data bytes belonging to a Tx Buffer element. Data field sizes > 8 bytes are intended for CAN FD operation only.

Table 25-47. TXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	TBDS	R/WQ	0h	Tx Buffer Data Field Size 000 8 byte data field 001 12 byte data field 010 16 byte data field 011 20 byte data field 100 24 byte data field 101 32 byte data field 110 48 byte data field 111 64 byte data field Note: In case the data length code DLC of a Tx Buffer element is configured to a value higher than the Tx Buffer data field size TXESC.TBDS, the bytes not defined by the Tx Buffer are transmitted as "0xCC" (padding bytes). Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

25.7.37 TXBRPAP Register (Offset = CCh) [Reset = 00000000h]

TXBRPAP is shown in Table 25-48.

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DCAN Tx Buffer Request Pending

Table 25-48. TXBRPAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRP31	R	0h	Transmission Request Pending 31. See description for bit 0.
30	TRP30	R	0h	Transmission Request Pending 30. See description for bit 0.
29	TRP29	R	0h	Transmission Request Pending 29. See description for bit 0.
28	TRP28	R	0h	Transmission Request Pending 28. See description for bit 0.
27	TRP27	R	0h	Transmission Request Pending 27. See description for bit 0.
26	TRP26	R	0h	Transmission Request Pending 26. See description for bit 0.
25	TRP25	R	0h	Transmission Request Pending 25. See description for bit 0.
24	TRP24	R	0h	Transmission Request Pending 24. See description for bit 0.
23	TRP23	R	0h	Transmission Request Pending 23. See description for bit 0.
22	TRP22	R	0h	Transmission Request Pending 22. See description for bit 0.
21	TRP21	R	0h	Transmission Request Pending 21. See description for bit 0.
20	TRP20	R	0h	Transmission Request Pending 20. See description for bit 0.
19	TRP19	R	0h	Transmission Request Pending 19. See description for bit 0.
18	TRP18	R	0h	Transmission Request Pending 18. See description for bit 0.
17	TRP17	R	0h	Transmission Request Pending 17. See description for bit 0.
16	TRP16	R	0h	Transmission Request Pending 16. See description for bit 0.
15	TRP15	R	0h	Transmission Request Pending 15. See description for bit 0.
14	TRP14	R	0h	Transmission Request Pending 14. See description for bit 0.
13	TRP13	R	0h	Transmission Request Pending 13. See description for bit 0.
12	TRP12	R	0h	Transmission Request Pending 12. See description for bit 0.
11	TRP11	R	0h	Transmission Request Pending 11. See description for bit 0.
10	TRP10	R	0h	Transmission Request Pending 10. See description for bit 0.
9	TRP9	R	0h	Transmission Request Pending 9. See description for bit 0.
8	TRP8	R	0h	Transmission Request Pending 8. See description for bit 0.
7	TRP7	R	0h	Transmission Request Pending 7. See description for bit 0.
6	TRP6	R	0h	Transmission Request Pending 6. See description for bit 0.
5	TRP5	R	0h	Transmission Request Pending 5. See description for bit 0.
4	TRP4	R	0h	Transmission Request Pending 4. See description for bit 0.
3	TRP3	R	0h	Transmission Request Pending 3. See description for bit 0.
2	TRP2	R	0h	Transmission Request Pending 2. See description for bit 0.
1	TRP1	R	0h	Transmission Request Pending 1. See description for bit 0.

Table 25-48. TXBRPAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TRP0	R	0h	Transmission Request Pending 0. Each Tx Buffer has its own Transmission Request Pending bit. The bits are set via register TXBAR. The bits are reset after a requested transmission has completed or has been cancelled via register TXBCR. TXBRP bits are set only for those Tx Buffers configured via TXBC. After a TXBRP bit has been set, a Tx scan is started to check for the pending Tx request with the highest priority (Tx Buffer with lowest Message ID). A cancellation request resets the corresponding transmission request pending bit of register TXBRP. In case a transmission has already been started when a cancellation is requested, this is done at the end of the transmission, regardless whether the transmission was successful or not. The cancellation request bits are reset directly after the corresponding TXBRP bit has been reset. After a cancellation has been requested, a finished cancellation is signalled via TXBCF - after successful transmission together with the corresponding TXBTO bit - when the transmission has not yet been started at the point of cancellation - when the transmission has been aborted due to lost arbitration - when an error occurred during frame transmission In DAR mode all transmissions are automatically cancelled if they are not successful. The corresponding TXBCF bit is set for all unsuccessful transmissions. 0 No transmission request pending 1 Transmission request pending Note: TXBRP bits which are set while a Tx scan is in progress are not considered during this particular Tx scan. In case a cancellation is requested for such a Tx Buffer, this Add Request is cancelled immediately, the corresponding TXBRP bit is reset.

25.7.38 TXBAR Register (Offset = D0h) [Reset = 00000000h]

TXBAR is shown in Table 25-49.

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DCAN Tx Buffer Add Request

Table 25-49. TXBAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AR31	R/WQ	0h	Add Request 31. See description for bit 0.
30	AR30	R/WQ	0h	Add Request 30. See description for bit 0.
29	AR29	R/WQ	0h	Add Request 29. See description for bit 0.
28	AR28	R/WQ	0h	Add Request 28. See description for bit 0.
27	AR27	R/WQ	0h	Add Request 27. See description for bit 0.
26	AR26	R/WQ	0h	Add Request 26. See description for bit 0.
25	AR25	R/WQ	0h	Add Request 25. See description for bit 0.
24	AR24	R/WQ	0h	Add Request 24. See description for bit 0.
23	AR23	R/WQ	0h	Add Request 23. See description for bit 0.
22	AR22	R/WQ	0h	Add Request 22. See description for bit 0.
21	AR21	R/WQ	0h	Add Request 21. See description for bit 0.
20	AR20	R/WQ	0h	Add Request 20. See description for bit 0.
19	AR19	R/WQ	0h	Add Request 19. See description for bit 0.
18	AR18	R/WQ	0h	Add Request 18. See description for bit 0.
17	AR17	R/WQ	0h	Add Request 17. See description for bit 0.
16	AR16	R/WQ	0h	Add Request 16. See description for bit 0.
15	AR15	R/WQ	0h	Add Request 15. See description for bit 0.
14	AR14	R/WQ	0h	Add Request 14. See description for bit 0.
13	AR13	R/WQ	0h	Add Request 13. See description for bit 0.
12	AR12	R/WQ	0h	Add Request 12. See description for bit 0.
11	AR11	R/WQ	0h	Add Request 11. See description for bit 0.
10	AR10	R/WQ	0h	Add Request 10. See description for bit 0.
9	AR9	R/WQ	0h	Add Request 9. See description for bit 0.
8	AR8	R/WQ	0h	Add Request 8. See description for bit 0.
7	AR7	R/WQ	0h	Add Request 7. See description for bit 0.
6	AR6	R/WQ	0h	Add Request 6. See description for bit 0.
5	AR5	R/WQ	0h	Add Request 5. See description for bit 0.
4	AR4	R/WQ	0h	Add Request 4. See description for bit 0.
3	AR3	R/WQ	0h	Add Request 3. See description for bit 0.
2	AR2	R/WQ	0h	Add Request 2. See description for bit 0.
1	AR1	R/WQ	0h	Add Request 1. See description for bit 0.
0	AR0	R/WQ	0h	Add Request 0. Each Tx Buffer has its own Add Request bit. Writing a '1' will set the corresponding Add Request bit; writing a '0' has no impact. This enables the Host to set transmission requests for multiple Tx Buffers with one write to TXBAR. TXBAR bits are set only for those Tx Buffers configured via TXBC. When no Tx scan is running, the bits are reset immediately, else the bits remain set until the Tx scan process has completed. 0 No transmission request added 1 Transmission requested added Note: If an add request is applied for a Tx Buffer with pending transmission request (corresponding TXBRP bit already set), this add request is ignored. Qualified Write is possible only with CCCR.CCE='0'

25.7.39 TXBCR Register (Offset = D4h) [Reset = 00000000h]

TXBCR is shown in Table 25-50.

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DCAN Tx Buffer Cancellation Request

Table 25-50. TXBCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CR31	R/WQ	0h	Cancellation Request 31. See description for bit 0.
30	CR30	R/WQ	0h	Cancellation Request 30. See description for bit 0.
29	CR29	R/WQ	0h	Cancellation Request 29. See description for bit 0.
28	CR28	R/WQ	0h	Cancellation Request 28. See description for bit 0.
27	CR27	R/WQ	0h	Cancellation Request 27. See description for bit 0.
26	CR26	R/WQ	0h	Cancellation Request 26. See description for bit 0.
25	CR25	R/WQ	0h	Cancellation Request 25. See description for bit 0.
24	CR24	R/WQ	0h	Cancellation Request 24. See description for bit 0.
23	CR23	R/WQ	0h	Cancellation Request 23. See description for bit 0.
22	CR22	R/WQ	0h	Cancellation Request 22. See description for bit 0.
21	CR21	R/WQ	0h	Cancellation Request 21. See description for bit 0.
20	CR20	R/WQ	0h	Cancellation Request 20. See description for bit 0.
19	CR19	R/WQ	0h	Cancellation Request 19. See description for bit 0.
18	CR18	R/WQ	0h	Cancellation Request 18. See description for bit 0.
17	CR17	R/WQ	0h	Cancellation Request 17. See description for bit 0.
16	CR16	R/WQ	0h	Cancellation Request 16. See description for bit 0.
15	CR15	R/WQ	0h	Cancellation Request 15. See description for bit 0.
14	CR14	R/WQ	0h	Cancellation Request 14. See description for bit 0.
13	CR13	R/WQ	0h	Cancellation Request 13. See description for bit 0.
12	CR12	R/WQ	0h	Cancellation Request 12. See description for bit 0.
11	CR11	R/WQ	0h	Cancellation Request 11. See description for bit 0.
10	CR10	R/WQ	0h	Cancellation Request 10. See description for bit 0.
9	CR9	R/WQ	0h	Cancellation Request 9. See description for bit 0.
8	CR8	R/WQ	0h	Cancellation Request 8. See description for bit 0.
7	CR7	R/WQ	0h	Cancellation Request 7. See description for bit 0.
6	CR6	R/WQ	0h	Cancellation Request 6. See description for bit 0.
5	CR5	R/WQ	0h	Cancellation Request 5. See description for bit 0.
4	CR4	R/WQ	0h	Cancellation Request 4. See description for bit 0.
3	CR3	R/WQ	0h	Cancellation Request 3. See description for bit 0.
2	CR2	R/WQ	0h	Cancellation Request 2. See description for bit 0.
1	CR1	R/WQ	0h	Cancellation Request 1. See description for bit 0.
0	CR0	R/WQ	0h	Cancellation Request 0. Each Tx Buffer has its own Cancellation Request bit. Writing a '1' will set the corresponding Cancellation Request bit; writing a '0' has no impact. This enables the Host to set cancellation requests for multiple Tx Buffers with one write to TXBCR. TXBCR bits are set only for those Tx Buffers configured via TXBC. The bits remain set until the corresponding bit of TXBRP is reset. 0 No cancellation pending 1 Cancellation pending Qualified Write is possible only with CCCR.CCE='0'

25.7.40 TXBTO Register (Offset = D8h) [Reset = 00000000h]

TXBTO is shown in Table 25-51.

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DCAN Tx Buffer Transmission Occurred

Table 25-51. TXBTO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TO31	R	0h	Transmission Occurred 31. See description for bit 0.
30	TO30	R	0h	Transmission Occurred 30. See description for bit 0.
29	TO29	R	0h	Transmission Occurred 29. See description for bit 0.
28	TO28	R	0h	Transmission Occurred 28. See description for bit 0.
27	TO27	R	0h	Transmission Occurred 27. See description for bit 0.
26	TO26	R	0h	Transmission Occurred 26. See description for bit 0.
25	TO25	R	0h	Transmission Occurred 25. See description for bit 0.
24	TO24	R	0h	Transmission Occurred 24. See description for bit 0.
23	TO23	R	0h	Transmission Occurred 23. See description for bit 0.
22	TO22	R	0h	Transmission Occurred 22. See description for bit 0.
21	TO21	R	0h	Transmission Occurred 21. See description for bit 0.
20	TO20	R	0h	Transmission Occurred 20. See description for bit 0.
19	TO19	R	0h	Transmission Occurred 19. See description for bit 0.
18	TO18	R	0h	Transmission Occurred 18. See description for bit 0.
17	TO17	R	0h	Transmission Occurred 17. See description for bit 0.
16	TO16	R	0h	Transmission Occurred 16. See description for bit 0.
15	TO15	R	0h	Transmission Occurred 15. See description for bit 0.
14	TO14	R	0h	Transmission Occurred 14. See description for bit 0.
13	TO13	R	0h	Transmission Occurred 13. See description for bit 0.
12	TO12	R	0h	Transmission Occurred 12. See description for bit 0.
11	TO11	R	0h	Transmission Occurred 11. See description for bit 0.
10	TO10	R	0h	Transmission Occurred 10. See description for bit 0.
9	TO9	R	0h	Transmission Occurred 9. See description for bit 0.
8	TO8	R	0h	Transmission Occurred 8. See description for bit 0.
7	TO7	R	0h	Transmission Occurred 7. See description for bit 0.
6	TO6	R	0h	Transmission Occurred 6. See description for bit 0.
5	TO5	R	0h	Transmission Occurred 5. See description for bit 0.
4	TO4	R	0h	Transmission Occurred 4. See description for bit 0.
3	TO3	R	0h	Transmission Occurred 3. See description for bit 0.
2	TO2	R	0h	Transmission Occurred 2. See description for bit 0.
1	TO1	R	0h	Transmission Occurred 1. See description for bit 0.
0	TO0	R	0h	Transmission Occurred 0. Each Tx Buffer has its own Transmission Occurred bit. The bits are set when the corresponding TXBRP bit is cleared after a successful transmission. The bits are reset when a new transmission is requested by writing a '1' to the corresponding bit of register TXBAR. 0 No transmission occurred 1 Transmission occurred

25.7.41 TXBCF Register (Offset = DCh) [Reset = 00000000h]

TXBCF is shown in Table 25-52.

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DCAN Tx Buffer Cancellation Finished

Table 25-52. TXBCF Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CF31	R	0h	Cancellation Finished 31. See description for bit 0.
30	CF30	R	0h	Cancellation Finished 30. See description for bit 0.
29	CF29	R	0h	Cancellation Finished 29. See description for bit 0.
28	CF28	R	0h	Cancellation Finished 28. See description for bit 0.
27	CF27	R	0h	Cancellation Finished 27. See description for bit 0.
26	CF26	R	0h	Cancellation Finished 26. See description for bit 0.
25	CF25	R	0h	Cancellation Finished 25. See description for bit 0.
24	CF24	R	0h	Cancellation Finished 24. See description for bit 0.
23	CF23	R	0h	Cancellation Finished 23. See description for bit 0.
22	CF22	R	0h	Cancellation Finished 22. See description for bit 0.
21	CF21	R	0h	Cancellation Finished 21. See description for bit 0.
20	CF20	R	0h	Cancellation Finished 20. See description for bit 0.
19	CF19	R	0h	Cancellation Finished 19. See description for bit 0.
18	CF18	R	0h	Cancellation Finished 18. See description for bit 0.
17	CF17	R	0h	Cancellation Finished 17. See description for bit 0.
16	CF16	R	0h	Cancellation Finished 16. See description for bit 0.
15	CF15	R	0h	Cancellation Finished 15. See description for bit 0.
14	CF14	R	0h	Cancellation Finished 14. See description for bit 0.
13	CF13	R	0h	Cancellation Finished 13. See description for bit 0.
12	CF12	R	0h	Cancellation Finished 12. See description for bit 0.
11	CF11	R	0h	Cancellation Finished 11. See description for bit 0.
10	CF10	R	0h	Cancellation Finished 10. See description for bit 0.
9	CF9	R	0h	Cancellation Finished 9. See description for bit 0.
8	CF8	R	0h	Cancellation Finished 8. See description for bit 0.
7	CF7	R	0h	Cancellation Finished 7. See description for bit 0.
6	CF6	R	0h	Cancellation Finished 6. See description for bit 0.
5	CF5	R	0h	Cancellation Finished 5. See description for bit 0.
4	CF4	R	0h	Cancellation Finished 4. See description for bit 0.
3	CF3	R	0h	Cancellation Finished 3. See description for bit 0.
2	CF2	R	0h	Cancellation Finished 2. See description for bit 0.
1	CF1	R	0h	Cancellation Finished 1. See description for bit 0.
0	CF0	R	0h	Cancellation Finished 0. Each Tx Buffer has its own Cancellation Finished bit. The bits are set when the corresponding TXBRP bit is cleared after a cancellation was requested via TXBCR. In case the corresponding TXBRP bit was not set at the point of cancellation, CF is set immediately. The bits are reset when a new transmission is requested by writing a '1' to the corresponding bit of register TXBAR. 0 No transmit buffer cancellation 1 Transmit buffer cancellation finished

25.7.42 TXTIE Register (Offset = E0h) [Reset = 00000000h]

TXTIE is shown in Table 25-53.

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DCAN Tx Buffer Transmission Interrupt Enable

Table 25-53. TXTIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TIE31	R/W	0h	Transmission Interrupt Enable 31. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
30	TIE30	R/W	0h	Transmission Interrupt Enable 30. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
29	TIE29	R/W	0h	Transmission Interrupt Enable 29. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
28	TIE28	R/W	0h	Transmission Interrupt Enable 28. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
27	TIE27	R/W	0h	Transmission Interrupt Enable 27. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
26	TIE26	R/W	0h	Transmission Interrupt Enable 26. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
25	TIE25	R/W	0h	Transmission Interrupt Enable 25. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
24	TIE24	R/W	0h	Transmission Interrupt Enable 24. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
23	TIE23	R/W	0h	Transmission Interrupt Enable 23. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
22	TIE22	R/W	0h	Transmission Interrupt Enable 22. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
21	TIE21	R/W	0h	Transmission Interrupt Enable 21. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
20	TIE20	R/W	0h	Transmission Interrupt Enable 20. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
19	TIE19	R/W	0h	Transmission Interrupt Enable 19. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
18	TIE18	R/W	0h	Transmission Interrupt Enable 18. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
17	TIE17	R/W	0h	Transmission Interrupt Enable 17. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
16	TIE16	R/W	0h	Transmission Interrupt Enable 16. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable

Table 25-53. TXTIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	TIE15	R/W	0h	Transmission Interrupt Enable 15. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
14	TIE14	R/W	0h	Transmission Interrupt Enable 14. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
13	TIE13	R/W	0h	Transmission Interrupt Enable 13. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
12	TIE12	R/W	0h	Transmission Interrupt Enable 12. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
11	TIE11	R/W	0h	Transmission Interrupt Enable 11. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
10	TIE10	R/W	0h	Transmission Interrupt Enable 10. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
9	TIE9	R/W	0h	Transmission Interrupt Enable 9. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
8	TIE8	R/W	0h	Transmission Interrupt Enable 8. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
7	TIE7	R/W	0h	Transmission Interrupt Enable 7. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
6	TIE6	R/W	0h	Transmission Interrupt Enable 6. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
5	TIE5	R/W	0h	Transmission Interrupt Enable 5. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
4	TIE4	R/W	0h	Transmission Interrupt Enable 4. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
3	TIE3	R/W	0h	Transmission Interrupt Enable 3. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
2	TIE2	R/W	0h	Transmission Interrupt Enable 2. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
1	TIE1	R/W	0h	Transmission Interrupt Enable 1. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
0	TIE0	R/W	0h	Transmission Interrupt Enable 0. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable

25.7.43 TXBCIE Register (Offset = E4h) [Reset = 00000000h]

TXBCIE is shown in Table 25-54.

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DCAN Tx Buffer Cancellation Finished Interrupt Enable

Table 25-54. TXBCIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CFIE31	R/W	0h	Cancellation Finished Interrupt Enable 31. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
30	CFIE30	R/W	0h	Cancellation Finished Interrupt Enable 30. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
29	CFIE29	R/W	0h	Cancellation Finished Interrupt Enable 29. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
28	CFIE28	R/W	0h	Cancellation Finished Interrupt Enable 28. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
27	CFIE27	R/W	0h	Cancellation Finished Interrupt Enable 27. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
26	CFIE26	R/W	0h	Cancellation Finished Interrupt Enable 26. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
25	CFIE25	R/W	0h	Cancellation Finished Interrupt Enable 25. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
24	CFIE24	R/W	0h	Cancellation Finished Interrupt Enable 24. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
23	CFIE23	R/W	0h	Cancellation Finished Interrupt Enable 23. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
22	CFIE22	R/W	0h	Cancellation Finished Interrupt Enable 22. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
21	CFIE21	R/W	0h	Cancellation Finished Interrupt Enable 21. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
20	CFIE20	R/W	0h	Cancellation Finished Interrupt Enable 20. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
19	CFIE19	R/W	0h	Cancellation Finished Interrupt Enable 19. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
18	CFIE18	R/W	0h	Cancellation Finished Interrupt Enable 18. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
17	CFIE17	R/W	0h	Cancellation Finished Interrupt Enable 17. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
16	CFIE16	R/W	0h	Cancellation Finished Interrupt Enable 16. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled

Table 25-54. TXBCIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	CFIE15	R/W	0h	Cancellation Finished Interrupt Enable 15. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
14	CFIE14	R/W	0h	Cancellation Finished Interrupt Enable 14. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
13	CFIE13	R/W	0h	Cancellation Finished Interrupt Enable 13. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
12	CFIE12	R/W	0h	Cancellation Finished Interrupt Enable 12. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
11	CFIE11	R/W	0h	Cancellation Finished Interrupt Enable 11. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
10	CFIE10	R/W	0h	Cancellation Finished Interrupt Enable 10. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
9	CFIE9	R/W	0h	Cancellation Finished Interrupt Enable 9. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
8	CFIE8	R/W	0h	Cancellation Finished Interrupt Enable 8. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
7	CFIE7	R/W	0h	Cancellation Finished Interrupt Enable 7. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
6	CFIE6	R/W	0h	Cancellation Finished Interrupt Enable 6. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
5	CFIE5	R/W	0h	Cancellation Finished Interrupt Enable 5. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
4	CFIE4	R/W	0h	Cancellation Finished Interrupt Enable 4. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
3	CFIE3	R/W	0h	Cancellation Finished Interrupt Enable 3. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
2	CFIE2	R/W	0h	Cancellation Finished Interrupt Enable 2. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
1	CFIE1	R/W	0h	Cancellation Finished Interrupt Enable 1. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
0	CFIE0	R/W	0h	Cancellation Finished Interrupt Enable 0. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled

25.7.44 TXEFC Register (Offset = F0h) [Reset = 00000000h]

TXEFC is shown in Table 25-55.

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DCAN Tx Event FIFO Configuration

Table 25-55. TXEFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-24	EFWM	R/WQ	0h	Event FIFO Watermark 0 Watermark interrupt disabled 1-32 Level for Tx Event FIFO watermark interrupt (IR.TEFW) >32 Watermark interrupt disabled
23-22	RESERVED	R	0h	Reserved
21-16	EFS	R/WQ	0h	Event FIFO Size. The Tx Event FIFO elements are indexed from 0 to EFS - 1. 0 Tx Event FIFO disabled 1-32 Number of Tx Event FIFO elements >32 Values greater than 32 are interpreted as 32
15-2	EFSA	R/WQ	0h	Event FIFO Start Address. Start address of Tx Event FIFO in Message RAM (32-bit word address).
1-0	RESERVED	R	0h	Reserved

25.7.45 TXEFS Register (Offset = F4h) [Reset = 00000000h]

TXEFS is shown in Table 25-56.

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DCAN Tx Event FIFO Status

Table 25-56. TXEFS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	TEFL	R	0h	Tx Event FIFO Element Lost. This bit is a copy of interrupt flag IR.TEFL. When IR.TEFL is reset, this bit is also reset. 0 No Tx Event FIFO element lost 1 Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero.
24	EFF	R	0h	Event FIFO Full 0 Tx Event FIFO not full 1 Tx Event FIFO full
23-21	RESERVED	R	0h	Reserved
20-16	EFPI	R	0h	Event FIFO Put Index.Tx Event FIFO write index pointer, range 0 to 31.
15-13	RESERVED	R	0h	Reserved
12-8	EFGI	R	0h	Event FIFO Get Index. Tx Event FIFO read index pointer, range 0 to 31.
7-6	RESERVED	R	0h	Reserved
5-0	EFFL	R	0h	Event FIFO Fill Level. Number of elements stored in Tx Event FIFO, range 0 to 32.

25.7.46 TXEFA Register (Offset = F8h) [Reset = 00000000h]

TXEFA is shown in Table 25-57.

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DCAN Tx Event FIFO Acknowledge

Table 25-57. TXEFA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	EFAI	R/W	0h	Event FIFO Acknowledge Index. After the Host has read an element or a sequence of elements from the Tx Event FIFO it has to write the index of the last element read from Tx Event FIFO to EFAI. This will set the Tx Event FIFO Get Index TXEFS.EFGI to EFAI + 1 and update the Event FIFO Fill Level TXEFS.EFFL.

25.7.47 SSPID Register (Offset = 200h) [Reset = 68E04901h]

SSPID is shown in Table 25-58.

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DCAN Subsystem Revision Register

Table 25-58. SSPID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID Register Scheme
29-28	BU	R	2h	Business Unit: 0x2 = Processors
27-16	MODULEID	R	8E0h	Module Identification Number
15-11	RTL	R	9h	RTL revision. Will vary depending on release
10-8	MAJOR	R	1h	Major Revision of the DCAN Subsystem
7-6	CUSTOM	R	0h	Custom Value
5-0	MINOR	R	1h	Minor Revision of the DCAN Subsystem

25.7.48 SSCTL Register (Offset = 204h) [Reset = 00000008h]

SSCTL is shown in Table 25-59.

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DCAN Subsystem Control Register

Table 25-59. SSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	EXTTSCNTEN	R/W	0h	External Timestamp Counter Enable. 0 External timestamp counter disabled 1 External timestamp counter enabled
5	AUTOWU	R/W	0h	Automatic Wakeup Enable. Enables the DCANSS to automatically clear the DCAN CCCR.INIT bit, fully waking the DCAN up, on an enabled wakeup request. 0 Disable the automatic write to CCCR.INIT 1 Enable the automatic write to CCCR.INIT
4	WUREQEN	R/W	0h	Wakeup Request Enable. Enables the DCANSS to wakeup on CAN RXD activity. 0 Disable wakeup request 1 Enables wakeup request
3	DBGSF	R/W	1h	Debug Suspend Free Bit. Enables debug suspend. 0 Disable debug suspend 1 Enable debug suspend
2-0	RESERVED	R	0h	Reserved

25.7.49 SSSTA Register (Offset = 208h) [Reset = 0000000Xh]

SSSTA is shown in Table 25-60.

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DCAN Subsystem Status Register

Table 25-60. SSSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	ENFDOE	R	Xh	Flexible Datarate Operation Enable. Determines whether CAN FD operation may be enabled via the DCAN core CCCR.FDOE bit (bit 8) or if only standard CAN operation is possible with this instance of the DCAN. 0 DCAN is only capable of standard CAN communication 1 DCAN may be configured to perform CAN FD communication
1	MEMINITSTA	R	0h	Memory Initialization Done. 0 Message RAM initialization is in progress 1 Message RAM is initialized for use
0	RESET	R	0h	Soft Reset Status. 0 Not in reset 1 Reset is in progress

25.7.50 SSICS Register (Offset = 20Ch) [Reset = 00000000h]

SSICS is shown in Table 25-61.

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DCAN Subsystem Interrupt Clear Shadow Register

Table 25-61. SSICS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TSCNTOVFL	R-0/W1C	0h	External Timestamp Counter Overflow Interrupt Status Clear. Reads always return a 0. 0 Write of '0' has no effect 1 Write of '1' clears the DCANSS IRS.EXT_TS_CNTR_OVFL bit

25.7.51 SSIRS Register (Offset = 210h) [Reset = 00000000h]

SSIRS is shown in Table 25-62.

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DCAN Subsystem Interrupt Raw Status Register

Table 25-62. SSIRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TSCNTOVFL	R/W1S	0h	External Timestamp Counter Overflow Interrupt Status. This bit is set by HW or by a SW write of '1'. To clear, use the ICS.EXT_TS_CNTR_OVFL bit. 0 External timestamp counter has not overflowed 1 External timestamp counter has overflowed When this bit is set to '1' by HW or SW, the EXT_TS_UNSERVICED_INTR_CNTR.EXT_TS_INTR_CNTR bit field will increment by 1.

25.7.52 SSIECS Register (Offset = 214h) [Reset = 00000000h]

SSIECS is shown in Table 25-63.

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DCAN Subsystem Interrupt Enable Clear Shadow Register

Table 25-63. SSIECS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TSCNTOVFL	R-0/W1C	0h	External Timestamp Counter Overflow Interrupt Enable Clear. Reads always return a 0. 0 Write of '0' has no effect 1 Write of '1' clears the DCANSS_IES.EXT_TS_CNTR_OVFL bit

25.7.53 SSIE Register (Offset = 218h) [Reset = 00000000h]

SSIE is shown in Table 25-64.

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DCAN Subsystem Interrupt Enable Register

Table 25-64. SSIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TSCNTOVFL	R/W1S	0h	External Timestamp Counter Overflow Interrupt Enable. A write of '0' has no effect. A write of '1' sets the IES.EXT_TS_CNTR_OVFL bit.

25.7.54 SSIES Register (Offset = 21Ch) [Reset = 00000000h]

SSIES is shown in Table 25-65.

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DCAN Subsystem Masked Interrupt Status. It is the logical AND of IRS and IE for the respective bits.

Table 25-65. SSIES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TSCNTOVFL	R	0h	External Timestamp Counter Overflow masked interrupt status. 0 External timestamp counter overflow interrupt is cleared 1 External timestamp counter overflow interrupt is set

25.7.55 SSEOI Register (Offset = 220h) [Reset = 00000000h]

SSEOI is shown in Table 25-66.

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DCAN Subsystem End of Interrupt

Table 25-66. SSEOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	EOI	R-0/W1S	0h	End of Interrupt. A write to this register will clear the associated interrupt. If the unserviced interrupt counter is > 1, another interrupt is generated. 0x00 External TS Interrupt is cleared 0x01 DCAN(0) interrupt is cleared 0x02 DCAN(1) interrupt is cleared Other writes are ignored.

25.7.56 EXTTSPS Register (Offset = 224h) [Reset = 00000000h]

EXTTSPS is shown in Table 25-67.

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DCAN Subsystem External Timestamp Prescaler 0

Table 25-67. EXTTSPS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	PRESCALER	R/W	0h	External Timestamp Prescaler Reload Value. The external timestamp count rate is the host (system) clock rate divided by this value, except in the case of 0. A zero value in this bit field will act identically to a value of 0x000001.

25.7.57 EXTTSUSI Register (Offset = 228h) [Reset = 00000000h]

EXTTSUSI is shown in Table 25-68.

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DCAN Subsystem External Timestamp Unserviced Interrupts Counter

Table 25-68. EXTTSUSI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	INTRCNT	R	0h	External Timestamp Counter Unserviced Rollover Interrupts. If this value is > 1, an EOI write of '1' to bit 0 will issue another interrupt. The status of this bit field is affected by the DCANSS_IRS.EXT_TS_CNTR_OVFL bit field.

25.7.58 ERRREV Register (Offset = 400h) [Reset = 66A0EA00h]

ERRREV is shown in Table 25-69.

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DCAN error Aggregator Revision Register

Table 25-69. ERRREV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID Register Scheme
29-28	BU	R	2h	Business Unit: 0x2 = Processors
27-16	MODULEID	R	6A0h	Module Identification Number
15-11	REVRTL	R	1Dh	RTL revision. Will vary depending on release
10-8	REVMAJ	R	2h	Major Revision of the Error Aggregator
7-6	REVCUSTOM	R	0h	Custom Revision of the Error Aggregator
5-0	REVMIN	R	0h	Minor Revision of the Error Aggregator

25.7.59 ERRVEC Register (Offset = 408h) [Reset = 00000000h]

ERRVEC is shown in Table 25-70.

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Each error detection and correction (EDC) controller has a bank of error registers (offsets 0x10 - 0x3B) associated with it. These registers are accessed via an internal serial bus (SVBUS). To access them through the ECC aggregator the controller ID desired must be written to the ECC_VECTOR field, together with the RD_SVBUS trigger and RD_SVBUS_ADDRESS bit field. This initiates the serial read which consummates by setting the RD_SVBUS_DONE bit. At this point the addressed register may be read by a normal CPU read of the appropriate offset address.

Table 25-70. ERRVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	SVBUSDONE	R	0h	Read Completion Flag
23-16	RDSVBUSA	R/W	0h	Read Address Offset
15	RDSVBUS	R-0/W1S	0h	Read Trigger
14-11	RESERVED	R	0h	Reserved
10-0	ECCVEC	R/W	0h	ECC RAM ID. Each error detection and correction (EDC) controller has a bank of error registers (offsets 0x10 - 0x3B) associated with it. These registers are accessed via an internal serial bus (SVBUS). To access them through the ECC aggregator the controller ID desired must be written to the ECC_VECTOR field, together with the RD_SVBUS trigger and RD_SVBUS_ADDRESS bit field. This initiates the serial read which consummates by setting the RD_SVBUS_DONE bit. At this point the addressed register may be read by a normal CPU read of the appropriate offset address. 0x000 Message RAM ECC controller is selected Others Reserved (do not use) Subsequent writes through the SVBUS (offsets 0x10 - 0x3B) have a delayed completion. To avoid conflicts, perform a read back of a register within this range after writing.

25.7.60 ERRSTA Register (Offset = 40Ch) [Reset = 00000002h]

ERRSTA is shown in Table 25-71.

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DCAN error Misc Status

Table 25-71. ERRSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	NUMRAMS	R	2h	Number of RAMs. Number of ECC RAMs serviced by the aggregator.

25.7.61 ERRWRAPREV Register (Offset = 410h) [Reset = 66A46A02h]

ERRWRAPREV is shown in Table 25-72.

Return to the Summary Table.

This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the DCANECC Vector Register.

Table 25-72. ERRWRAPREV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID Register Scheme
29-28	BU	R	2h	Business Unit: 0x2 = Processors
27-16	MODULEID	R	6A4h	Module Identification Number
15-11	REVRTL	R	Dh	RTL revision. Will vary depending on release
10-8	REVMAJ	R	2h	Major Revision of the Error Aggregator
7-6	REVCUSTOM	R	0h	Custom Revision of the Error Aggregator
5-0	REVMIN	R	2h	Minor Revision of the Error Aggregator

25.7.62 ERRCTL Register (Offset = 414h) [Reset = 00000187h]

ERRCTL is shown in Table 25-73.

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This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the DCANECC Vector Register.

Table 25-73. ERRCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CHECKSVBTO	R/W	1h	Enables Serial VBUS timeout mechanism
7	CHECKPAR	R/W	1h	Enables parity checking on internal data
6	ERRONCE	R/W	0h	If this bit is set, the FORCE_SEC/FORCE_DED will inject an error to the specified row only once. The FORCE_SEC bit will be cleared once a writeback happens. If writeback is not enabled, this error will be cleared the cycle following the read when the data is corrected. For double-bit errors, the FORCE_DED bit will be cleared the cycle following the double-bit error. Any subsequent reads will not force an error.
5	FRCNROW	R/W	0h	Enable single/double-bit error on the next RAM read, regardless of the MCANERR_ERR_CTRL1.ECC_ROW setting. For write through mode, this applies to writes as well as reads.
4	FRCDED	R/W	0h	Force double-bit error. Cleared the cycle following the error if ERROR_ONCE is asserted. For write through mode, this applies to writes as well as reads. MCANERR_ERR_CTRL1 and MCANERR_ERR_CTRL2 should be configured prior to setting this bit.
3	FRCSEC	R/W	0h	Force single-bit error. Cleared on a writeback or the cycle following the error if ERROR_ONCE is asserted. For write through mode, this applies to writes as well as reads. MCANERR_ERR_CTRL1 and MCANERR_ERR_CTRL2 should be configured prior to setting this bit.
2	ENRMW	R/W	1h	Enable read-modify-write on partial word writes
1	ECCCHECK	R/W	1h	Enable ECC Check. ECC is completely bypassed if both ECC_ENABLE and ECC_CHECK are '0'.
0	ECCEN	R/W	1h	Enable ECC Generation

25.7.63 ERRCTL1 Register (Offset = 418h) [Reset = 00000000h]

ERRCTL1 is shown in Table 25-74.

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This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the DCANECC Vector Register.

Table 25-74. ERRCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ECCROW	R/W	0h	Row address where FORCE_SEC or FORCE_DED needs to be applied. This is ignored if FORCE_N_ROW is set.

25.7.64 ERRCTL2 Register (Offset = 41Ch) [Reset = 00000000h]

ERRCTL2 is shown in Table 25-75.

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This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the DCANECC Vector Register.

Table 25-75. ERRCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ECCB2	R/W	0h	Second column/data bit that needs to be flipped when FORCE_DED is set
15-0	ECCB1	R/W	0h	Column/Data bit that needs to be flipped when FORCE_SEC or FORCE_DED is set

25.7.65 ERRSTA1 Register (Offset = 420h) [Reset = 00000000h]

ERRSTA1 is shown in Table 25-76.

Return to the Summary Table.

This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the DCANECC Vector Register.

Table 25-76. ERRSTA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ECCB1	R	0h	ECC Error Bit Position. Indicates the bit position in the RAM data that is in error on an SEC error. Only valid on an SEC error. 0 Bit 0 is in error 1 Bit 1 is in error 2 Bit 2 is in error 3 Bit 3 is in error ... 31 Bit 31 is in error >32 Invalid
15	CLRCTLERR	R/W1S	0h	Writing a '1' clears the CTRL_REG_ERROR bit
14-13	CLRPARERR	R/WD	0h	Clear Parity Error. A write of a non-zero value to this bit field decrements the PARITY_ERROR bit field by the value provided.
12	CLRECCOT	R/W1C	0h	Writing a '1' clears the ECC_OTHER bit.
11-10	CLRECCDED	R/WD	0h	Clear ECC_DED. A write of a non-zero value to this bit field decrements the ECC_DED bit field by the value provided.
9-8	CLRECCSEC	R/WD	0h	Clear ECC_SEC. A write of a non-zero value to this bit field decrements the ECC_SEC bit field by the value provided.
7	CTLERR	R/W1S	0h	Control Register Error. A bit field in the control register is in an ambiguous state. This means that the redundancy registers have detected a state where not all values are the same and has defaulted to the reset state. S/W needs to re-write these registers to a known state. A write of 1 will set this interrupt flag.
6-5	PARERR	R/WI	0h	Parity Error Status. A 2-bit saturating counter of the number of parity errors that have occurred since last cleared. 0 No parity error detected 1 One parity error was detected 2 Two parity errors were detected 3 Three parity errors were detected A write of a non-zero value to this bit field increments it by the value provided.
4	ECCOTHER	R/W1S	0h	SEC While Writeback Error Status 0 No SEC error while writeback pending 1 Indicates that successive single-bit errors have occurred while a writeback is still pending
3-2	ECCDED	R/WI	0h	Double Bit Error Detected Status. A 2-bit saturating counter of the number of DED errors that have occurred since last cleared. 0 No double-bit error detected 1 One double-bit error was detected 2 Two double-bit errors were detected 3 Three double-bit errors were detected A write of a non-zero value to this bit field increments it by the value provided.
1-0	ECCSEC	R/WI	0h	Single Bit Error Corrected Status. A 2-bit saturating counter of the number of SEC errors that have occurred since last cleared. 0 No single-bit error detected 1 One single-bit error was detected and corrected 2 Two single-bit errors were detected and corrected 3 Three single-bit errors were detected and corrected A write of a non-zero value to this bit field increments it by the value provided.

25.7.66 ERRSTA2 Register (Offset = 424h) [Reset = 00000000h]

ERRSTA2 is shown in Table 25-77.

Return to the Summary Table.

This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the DCANECC Vector Register.

Table 25-77. ERRSTA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ECCROW	R	0h	Indicates the row address where the single or double-bit error occurred. This value is address offset/4.

25.7.67 ERRSTA3 Register (Offset = 428h) [Reset = 00000000h]

ERRSTA3 is shown in Table 25-78.

Return to the Summary Table.

This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the DCANECC Vector Register.

Table 25-78. ERRSTA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9	CLRSVBTO	R-0/W1C	0h	Write 1 to clear the Serial VBUS Timeout Flag
8-2	RESERVED	R	0h	Reserved
1	SVBUSTO	R-0/W1S	0h	Serial VBUS Timeout Flag. Write 1 to set.
0	WBPEND	R	0h	Delayed Write Back Pending Status 0 No write back pending 1 An ECC data correction write back is pending

25.7.68 SECEOI Register (Offset = 43Ch) [Reset = 00000000h]

SECEOI is shown in Table 25-79.

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DCAN Single Error Corrected End of Interrupt Register

Table 25-79. SECEOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOIWR	R-0/W1S	0h	Write to this register indicates that software has acknowledged the pending interrupt and the next interrupt can be sent to the host. Note that a write to the MCANERR_ERR_STAT1.CLR_ECC_SEC goes through the SVBUS and has a delayed completion. To avoid an additional interrupt, read the MCANERR_ERR_STAT1 register back prior to writing to this bit field.

25.7.69 SECSTA Register (Offset = 440h) [Reset = 00000000h]

SECSTA is shown in Table 25-80.

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DCANSingle Error Corrected Interrupt Status Register

Table 25-80. SECSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	MGSPEND	R-0/W1S	0h	Message RAM SEC Interrupt Pending 0 No SEC interrupt is pending 1 SEC interrupt is pending

25.7.70 SECENSET Register (Offset = 480h) [Reset = 00000000h]

SECENSET is shown in Table 25-81.

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DCANSingle Error Corrected Interrupt Enable Set Register

Table 25-81. SECENSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	MSGENSET	R/W1S	0h	Message RAM SEC Interrupt Pending Enable Set. Writing a 1 to this bit enables the Message RAM SEC error interrupts. Writing a 0 has no effect. Reads return the corresponding enable bit's current value.

25.7.71 SECENCLR Register (Offset = 4C0h) [Reset = 00000000h]

SECENCLR is shown in Table 25-82.

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DCANSingle Error Corrected Interrupt Enable Clear Register

Table 25-82. SECENCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	MSGENCLR	R/W1C	0h	Message RAM SEC Interrupt Pending Enable Clear. Writing a 1 to this bit disables the Message RAM SEC error interrupts. Writing a 0 has no effect. Reads return the corresponding enable bit's current value.

25.7.72 DEDEOI Register (Offset = 53Ch) [Reset = 00000000h]

DEDEOI is shown in Table 25-83.

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DCANDouble Error Detected End of Interrupt Register

Table 25-83. DEDEOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOIWR	R-0/W1S	0h	Write to this register indicates that software has acknowledged the pending interrupt and the next interrupt can be sent to the host. Note that a write to the MCANERR_ERR_STAT1.CLR_ECC_DED goes through the SVBUS and has a delayed completion. To avoid an additional interrupt, read the MCANERR_ERR_STAT1 register back prior to writing to this bit field.

25.7.73 DEDSTA Register (Offset = 540h) [Reset = 00000000h]

DEDSTA is shown in Table 25-84.

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DCANDouble Error Detected Interrupt Status Register

Table 25-84. DEDSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TXREQPEND	R-0/W1S	0h	TX Empty DMA Request Parity Interrupt Pending 0 No parity error interrupt is pending 1 A parity error interrupt is pending
0	MSGPEND	R-0/W1S	0h	Message RAM DED Interrupt Pending 0 No DED interrupt is pending 1 DED interrupt is pending

25.7.74 DEDENSET Register (Offset = 580h) [Reset = 00000000h]

DEDENSET is shown in Table 25-85.

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DCANDouble Error Detected Interrupt Enable Set Register

Table 25-85. DEDENSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TXREQENSET	R/W1S	0h	TX Empty DMA Request Parity Interrupt Pending Enable Set. Writing a 1 to this bit enables the TX empty DMA request parity error interrupts. Writing a 0 has no effect. Reads return the corresponding enable bit's current value.
0	MSGENSET	R/W1S	0h	Message RAM DED Interrupt Pending Enable Set. Writing a 1 to this bit enables the Message RAM DED error interrupts. Writing a 0 has no effect. Reads return the corresponding enable bit's current value.

25.7.75 DEDENCLR Register (Offset = 5C0h) [Reset = 00000000h]

DEDENCLR is shown in Table 25-86.

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DCANDouble Error Detected Interrupt Enable Clear Register

Table 25-86. DEDENCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TXREQENCLR	R/W1C	0h	TX Empty DMA Request Parity Interrupt Pending Enable Clear. Writing a 1 to this bit disables the TX empty DMA request parity error interrupts. Writing a 0 has no effect. Reads return the corresponding enable bit's current value.
0	MSGENCLR	R/W1C	0h	Message RAM DED Interrupt Pending Enable Clear. Writing a 1 to this bit disables the Message RAM DED error interrupts. Writing a 0 has no effect. Reads return the corresponding enable bit's current value.

25.7.76 AGGRENSET Register (Offset = 600h) [Reset = 00000000h]

AGGRENSET is shown in Table 25-87.

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DCAN error Aggregator Enable Set Register

Table 25-87. AGGRENSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1S	0h	Write 1 to enable timeout errors. Reads return the corresponding enable bit's current value.
0	PARITY	R/W1S	0h	Write 1 to enable parity errors. Reads return the corresponding enable bit's current value.

25.7.77 AGGRENCLR Register (Offset = 604h) [Reset = 00000000h]

AGGRENCLR is shown in Table 25-88.

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DCAN error Aggregator Enable Clear Register

Table 25-88. AGGRENCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1C	0h	Write 1 to disable timeout errors. Reads return the corresponding enable bit's current value.
0	PARITY	R/W1C	0h	Write 1 to disable parity errors. Reads return the corresponding enable bit's current value.

25.7.78 AGGRSTASET Register (Offset = 608h) [Reset = 00000000h]

AGGRSTASET is shown in Table 25-89.

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DCAN error Aggregator Status Set Register

Table 25-89. AGGRSTASET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/WI	0h	Aggregator Serial VBUS Timeout Error Status 2-bit saturating counter of the number of SVBUS timeout errors that have occurred since last cleared. 0 No timeout errors have occurred 1 One timeout error has occurred 2 Two timeout errors have occurred 3 Three timeout errors have occurred A write of a non-zero value to this bit field increments it by the value provided.
1-0	PARITY	R/WI	0h	Aggregator Parity Error Status 2-bit saturating counter of the number of parity errors that have occurred since last cleared. 0 No parity errors have occurred 1 One parity error has occurred 2 Two parity errors have occurred 3 Three parity errors have occurred A write of a non-zero value to this bit field increments it by the value provided.

25.7.79 AGGRSTACLR Register (Offset = 60Ch) [Reset = 00000000h]

AGGRSTACLR is shown in Table 25-90.

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DCAN error Aggregator Status Clear Register

Table 25-90. AGGRSTACLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/WD	0h	Aggregator Serial VBUS Timeout Error Status 2-bit saturating counter of the number of SVBUS timeout errors that have occurred since last cleared. 0 No timeout errors have occurred 1 One timeout error has occurred 2 Two timeout errors have occurred 3 Three timeout errors have occurred A write of a non-zero value to this bit field decrements it by the value provided.
1-0	PARITY	R/WD	0h	Aggregator Parity Error Status 2-bit saturating counter of the number of parity errors that have occurred since last cleared. 0 No parity errors have occurred 1 One parity error has occurred 2 Two parity errors have occurred 3 Three parity errors have occurred A write of a non-zero value to this bit field decrements it by the value provided.

25.7.80 DESC Register (Offset = 800h) [Reset = 00000000h]

DESC is shown in Table 25-91.

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This register identifies the peripheral and its exact version.

Table 25-91. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODULEID	R	940h	Module identification contains a unique peripheral identification number. The assignments are maintained in a central database for all of the platform modules to ensure uniqueness. 0h = Smallest value FFFFh = Highest possible value
15-12	FEATUREVER	R	0h	Feature Set for the module *instance* 0h = DCANmodule with CAN-FD mode enabled <<Internal Note: This is an in-IP paper spin variant. How does this map to the SYS_MCAN_ENABLE_FD choice value?>> 1h = DCANmodule with CAN-FD mode disabled <<Internal Note: This is an in-IP paper spin variant. How does this map to the SYS_MCAN_ENABLE_FD choice value?>>
11-8	RESERVED	R	0h	Reserved
7-4	MAJREV	R	0h	Major rev of the IP 0h = Smallest value Fh = Highest possible value
3-0	MINREV	R	0h	Minor rev of the IP 0h = Smallest value Fh = Highest possible value

25.7.81 IMASK0 Register (Offset = 844h) [Reset = 00000000h]

IMASK0 is shown in Table 25-92.

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Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Table 25-92. IMASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DMADONE1	R/W	0h	Mask Channel1 Event. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
6	DMADONE0	R/W	0h	Mask Channel1 Event. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
5	FE2	R/W	0h	Mask Channel1 Event. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
4	TSORWAKE	R/W	0h	Mask Channel1 Event. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
3	DED	R/W	0h	Mask Channel1 Event. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
2	SEC	R/W	0h	Mask Channel1 Event. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
1	INTL1	R/W	0h	Mask Channel1 Event. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
0	INTL0	R/W	0h	Mask channel0 Event 0h = Clear Interrupt Mask 1h = Set Interrupt Mask

25.7.82 RIS0 Register (Offset = 848h) [Reset = 00000000h]

RIS0 is shown in Table 25-93.

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Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS0 register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Table 25-93. RIS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DMADONE1	R	0h	Raw interrupt status for EVENT0. This bit is set to 1 when an event is received on EVENT0 channel. when the corresponding bit in ICLR is set to 1, this bit will be cleared. This bit is also cleared when a new compare value is written in CH0CMP register 0h = Interrupt did not occur 1h = Interrupt occured
6	DMADONE0	R	0h	Raw interrupt status for EVENT0. This bit is set to 1 when an event is received on EVENT0 channel. when the corresponding bit in ICLR is set to 1, this bit will be cleared. This bit is also cleared when a new compare value is written in CH0CMP register 0h = Interrupt did not occur 1h = Interrupt occured
5	FE2	R	0h	Raw interrupt status for EVENT0. This bit is set to 1 when an event is received on EVENT0 channel. when the corresponding bit in ICLR is set to 1, this bit will be cleared. This bit is also cleared when a new compare value is written in CH0CMP register 0h = Interrupt did not occur 1h = Interrupt occured
4	TSORWAKE	R	0h	Raw interrupt status for EVENT0. This bit is set to 1 when an event is received on EVENT0 channel. when the corresponding bit in ICLR is set to 1, this bit will be cleared. This bit is also cleared when a new compare value is written in CH0CMP register 0h = Interrupt did not occur 1h = Interrupt occured
3	DED	R	0h	Raw interrupt status for EVENT0. This bit is set to 1 when an event is received on EVENT0 channel. when the corresponding bit in ICLR is set to 1, this bit will be cleared. This bit is also cleared when a new compare value is written in CH0CMP register 0h = Interrupt did not occur 1h = Interrupt occured
2	SEC	R	0h	Raw interrupt status for EVENT0. This bit is set to 1 when an event is received on EVENT0 channel. when the corresponding bit in ICLR is set to 1, this bit will be cleared. This bit is also cleared when a new compare value is written in CH0CMP register 0h = Interrupt did not occur 1h = Interrupt occured
1	INTL1	R	0h	Raw interrupt status for EVENT1. This bit is set to 1 when an event is received on EVENT1 channel. when the corresponding bit in ICLR is set to 1, this bit will be cleared. This bit is also cleared when the captured time value is read from the CH1CAPT register. 0h = Interrupt did not occur 1h = Interrupt occured
0	INTL0	R	0h	Raw interrupt status for EVENT0. This bit is set to 1 when an event is received on EVENT0 channel. when the corresponding bit in ICLR is set to 1, this bit will be cleared. This bit is also cleared when a new compare value is written in CH0CMP register 0h = Interrupt did not occur 1h = Interrupt occured

25.7.83 MIS0 Register (Offset = 84Ch) [Reset = 00000000h]

MIS0 is shown in Table 25-94.

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Masked interrupt status. This is an AND of the IMASK and RIS registers.

Table 25-94. MIS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DMADONE1	R	0h	Mask interrupt status for EVENT0 0h = Interrupt did not occur 1h = Interrupt occured
6	DMADONE0	R	0h	Mask interrupt status for EVENT0 0h = Interrupt did not occur 1h = Interrupt occured
5	FE2	R	0h	Mask interrupt status for EVENT0 0h = Interrupt did not occur 1h = Interrupt occured
4	TSORWAKE	R	0h	Mask interrupt status for EVENT0 0h = Interrupt did not occur 1h = Interrupt occured
3	DED	R	0h	Mask interrupt status for EVENT0 0h = Interrupt did not occur 1h = Interrupt occured
2	SEC	R	0h	Mask interrupt status for EVENT0 0h = Interrupt did not occur 1h = Interrupt occured
1	INTL1	R	0h	Mask interrupt status for EVENT1 0h = Interrupt did not occur 1h = Interrupt occured
0	INTL0	R	0h	Mask interrupt status for EVENT0 0h = Interrupt did not occur 1h = Interrupt occured

25.7.84 ISET0 Register (Offset = 850h) [Reset = 00000000h]

ISET0 is shown in Table 25-95.

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Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET0 will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Table 25-95. ISET0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DMADONE1	W	0h	Sets EVENT0 in RIS 0h = Writing 0 has no effect 1h = Sets interrupt
6	DMADONE0	W	0h	Sets EVENT0 in RIS 0h = Writing 0 has no effect 1h = Sets interrupt
5	FE2	W	0h	Sets EVENT0 in RIS 0h = Writing 0 has no effect 1h = Sets interrupt
4	TSORWAKE	W	0h	Sets EVENT0 in RIS 0h = Writing 0 has no effect 1h = Sets interrupt
3	DED	W	0h	Sets EVENT0 in RIS 0h = Writing 0 has no effect 1h = Sets interrupt
2	SEC	W	0h	Sets EVENT0 in RIS 0h = Writing 0 has no effect 1h = Sets interrupt
1	INTL1	W	0h	Sets EVENT1 in RIS 0h = Writing 0 has no effect 1h = Sets interrupt
0	INTL0	W	0h	Sets EVENT0 in RIS 0h = Writing 0 has no effect 1h = Sets interrupt

25.7.85 ICLR0 Register (Offset = 854h) [Reset = 00000000h]

ICLR0 is shown in Table 25-96.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Table 25-96. ICLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DMADONE1	W	0h	Clears EVENT0 in RIS 0h = Writing 0 has no effect 1h = Clears the Event
6	DMADONE0	W	0h	Clears EVENT0 in RIS 0h = Writing 0 has no effect 1h = Clears the Event
5	FE2	W	0h	Clears EVENT0 in RIS 0h = Writing 0 has no effect 1h = Clears the Event
4	TSORWAKE	W	0h	Clears EVENT0 in RIS 0h = Writing 0 has no effect 1h = Clears the Event
3	DED	W	0h	Clears EVENT0 in RIS 0h = Writing 0 has no effect 1h = Clears the Event
2	SEC	W	0h	Clears EVENT0 in RIS 0h = Writing 0 has no effect 1h = Clears the Event
1	INTL1	W	0h	Clears EVENT1 in RIS 0h = Writing 0 has no effect 1h = Clears the Event
0	INTL0	W	0h	Clears EVENT0 in RIS 0h = Writing 0 has no effect 1h = Clears the Event

25.7.86 IMASK1 Register (Offset = 868h) [Reset = 00000000h]

IMASK1 is shown in Table 25-97.

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Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Table 25-97. IMASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DMADONE1	R/W	0h	Mask Channel1 Event. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
6	DMADONE0	R/W	0h	Mask Channel1 Event. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
5	FE2	R/W	0h	Mask Channel1 Event. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
4	TSORWAKE	R/W	0h	Mask Channel1 Event. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
3	DED	R/W	0h	Mask Channel1 Event. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
2	SEC	R/W	0h	Mask Channel1 Event. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
1	INTL1	R/W	0h	Mask Channel1 Event. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
0	INTL0	R/W	0h	Mask channel0 Event 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask

25.7.87 RIS1 Register (Offset = 86Ch) [Reset = 00000000h]

RIS1 is shown in Table 25-98.

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Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS0 register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Table 25-98. RIS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DMADONE1	R	0h	Raw interrupt status for EVENT0. This bit is set to 1 when an event is received on EVENT0 channel. when the corresponding bit in ICLR is set to 1, this bit will be cleared. This bit is also cleared when a new compare value is written in CH0CMP register 0h = Interrupt did not occur 1h = Interrupt occured
6	DMADONE0	R	0h	Raw interrupt status for EVENT0. This bit is set to 1 when an event is received on EVENT0 channel. when the corresponding bit in ICLR is set to 1, this bit will be cleared. This bit is also cleared when a new compare value is written in CH0CMP register 0h = Interrupt did not occur 1h = Interrupt occured
5	FE2	R	0h	Raw interrupt status for EVENT0. This bit is set to 1 when an event is received on EVENT0 channel. when the corresponding bit in ICLR is set to 1, this bit will be cleared. This bit is also cleared when a new compare value is written in CH0CMP register 0h = Interrupt did not occur 1h = Interrupt occured
4	TSORWAKE	R	0h	Raw interrupt status for EVENT0. This bit is set to 1 when an event is received on EVENT0 channel. when the corresponding bit in ICLR is set to 1, this bit will be cleared. This bit is also cleared when a new compare value is written in CH0CMP register 0h = Interrupt did not occur 1h = Interrupt occured
3	DED	R	0h	Raw interrupt status for EVENT0. This bit is set to 1 when an event is received on EVENT0 channel. when the corresponding bit in ICLR is set to 1, this bit will be cleared. This bit is also cleared when a new compare value is written in CH0CMP register 0h = Interrupt did not occur 1h = Interrupt occured
2	SEC	R	0h	Raw interrupt status for EVENT0. This bit is set to 1 when an event is received on EVENT0 channel. when the corresponding bit in ICLR is set to 1, this bit will be cleared. This bit is also cleared when a new compare value is written in CH0CMP register 0h = Interrupt did not occur 1h = Interrupt occured
1	INTL1	R	0h	Raw interrupt status for EVENT1. This bit is set to 1 when an event is received on EVENT1 channel. when the corresponding bit in ICLR is set to 1, this bit will be cleared. This bit is also cleared when the captured time value is read from the CH1CAPT register. 0h = Interrupt did not occur 1h = Interrupt occured
0	INTL0	R	0h	Raw interrupt status for EVENT0. This bit is set to 1 when an event is received on EVENT0 channel. when the corresponding bit in ICLR is set to 1, this bit will be cleared. This bit is also cleared when a new compare value is written in CH0CMP register 0h = Interrupt did not occur 1h = Interrupt occured

25.7.88 MIS1 Register (Offset = 870h) [Reset = 00000000h]

MIS1 is shown in Table 25-99.

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Masked interrupt status. This is an AND of the IMASK and RIS registers.

Table 25-99. MIS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DMADONE1	R	0h	Mask interrupt status for EVENT0 0h = Interrupt did not occur 1h = Interrupt occured
6	DMADONE0	R	0h	Mask interrupt status for EVENT0 0h = Interrupt did not occur 1h = Interrupt occured
5	FE2	R	0h	Mask interrupt status for EVENT0 0h = Interrupt did not occur 1h = Interrupt occured
4	TSORWAKE	R	0h	Mask interrupt status for EVENT0 0h = Interrupt did not occur 1h = Interrupt occured
3	DED	R	0h	Mask interrupt status for EVENT0 0h = Interrupt did not occur 1h = Interrupt occured
2	SEC	R	0h	Mask interrupt status for EVENT0 0h = Interrupt did not occur 1h = Interrupt occured
1	INTL1	R	0h	Mask interrupt status for EVENT1 0h = Interrupt did not occur 1h = Interrupt occured
0	INTL0	R	0h	Mask interrupt status for EVENT0 0h = Interrupt did not occur 1h = Interrupt occured

25.7.89 ISET1 Register (Offset = 874h) [Reset = 00000000h]

ISET1 is shown in Table 25-100.

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Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET0 will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Table 25-100. ISET1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DMADONE1	W	0h	Sets EVENT0 in RIS 0h = Writing 0 has no effect 1h = Sets interrupt
6	DMADONE0	W	0h	Sets EVENT0 in RIS 0h = Writing 0 has no effect 1h = Sets interrupt
5	FE2	W	0h	Sets EVENT0 in RIS 0h = Writing 0 has no effect 1h = Sets interrupt
4	TSORWAKE	W	0h	Sets EVENT0 in RIS 0h = Writing 0 has no effect 1h = Sets interrupt
3	DED	W	0h	Sets EVENT0 in RIS 0h = Writing 0 has no effect 1h = Sets interrupt
2	SEC	W	0h	Sets EVENT0 in RIS 0h = Writing 0 has no effect 1h = Sets interrupt
1	INTL1	W	0h	Sets EVENT1 in RIS 0h = Writing 0 has no effect 1h = Sets interrupt
0	INTL0	W	0h	Sets EVENT0 in RIS 0h = Writing 0 has no effect 1h = Sets interrupt

25.7.90 ICLR1 Register (Offset = 878h) [Reset = 00000000h]

ICLR1 is shown in Table 25-101.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Table 25-101. ICLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DMADONE1	W	0h	Clears EVENT0 in RIS 0h = Writing 0 has no effect 1h = Clears the Event
6	DMADONE0	W	0h	Clears EVENT0 in RIS 0h = Writing 0 has no effect 1h = Clears the Event
5	FE2	W	0h	Clears EVENT0 in RIS 0h = Writing 0 has no effect 1h = Clears the Event
4	TSORWAKE	W	0h	Clears EVENT0 in RIS 0h = Writing 0 has no effect 1h = Clears the Event
3	DED	W	0h	Clears EVENT0 in RIS 0h = Writing 0 has no effect 1h = Clears the Event
2	SEC	W	0h	Clears EVENT0 in RIS 0h = Writing 0 has no effect 1h = Clears the Event
1	INTL1	W	0h	Clears EVENT1 in RIS 0h = Writing 0 has no effect 1h = Clears the Event
0	INTL0	W	0h	Clears EVENT0 in RIS 0h = Writing 0 has no effect 1h = Clears the Event

25.7.91 CLKDIV Register (Offset = 904h) [Reset = 00000000h]

CLKDIV is shown in Table 25-102.

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Needs to go to the Management aperture once available

Table 25-102. CLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	RATIO	R/W	0h	Clock divide ratio specification. Enables configuring clock divide settings for the DCANfunctional clock input to the MCAN-SS. 0h (R/W) = Divides input clock by 1 1h (R/W) = Divides input clock by 2 2h (R/W) = Divides input clock by 4

25.7.92 CLKCTL Register (Offset = 908h) [Reset = 00000000h]

CLKCTL is shown in Table 25-103.

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DCANSS clock stop control MMR. <Internal note> Bus clock for the Dragon wrapper MMRs (including this MMR) is not gated by this register.

Table 25-103. CLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	WUGLTFLTEN	R/W	0h	Setting this bit enables the glitch filter on DCAN RXD input, which wakes up the DCANcontroller to exit clock gating. 0h = Disable glitch filter enable on RXD input when DCANis in clock stop mode (waiting for event on RXD input for clock stop wakeup). 1h = Enable glitch filter enable on RXD input when DCANis in clock stop mode (waiting for event on RXD input for clock stop wakeup).
7-5	RESERVED	R	0h	Reserved
4	WUINTEN	R/W	0h	This bit controls enabling or disabling the DCANIP clock stop wakeup interrupt (when CTRL.WAKEUPREQEN wakeup request is enabled to wakeup DCANIP upon CAN RXD activity) 0h = Disable DCANIP clock stop wakeup interrupt 1h = Enable DCANIP clock stop wakeup interrupt
3-1	RESERVED	R	0h	Reserved
0	STOPREQ	R/W	0h	This bit is used to enable/disable DCANclock (both host clock and functional clock) gating request. Note: This bit can be reset by HW by Clock-Stop Wake-up via CAN RX Activity. See spec for more details. 0h = Disable MCAN-SS clock stop request 1h = Enable MCAN-SS clock stop request

25.7.93 CLKSTA Register (Offset = 90Ch) [Reset = 00000000h]

CLKSTA is shown in Table 25-104.

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DCANSS clock stop status register to indicate status of clock stop mechanism

Table 25-104. CLKSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	STPREQHWOV	R	0h	DCANSS clock stop HW override status bit. This bit indicates when the CLKCTL.STOPREQ bit has been cleared by HW when a clock-stop wake-up event via CAN RX activity is triggered. 0h = CLKCTL.STOPREQ bit has not been cleared by HW. 1h = CLKCTL.STOPREQ bit has been cleared by HW.
3-1	RESERVED	R	0h	Reserved
0	STPACKSTA	R	0h	Clock stop acknowledge status from DCANIP 0h = No clock stop acknowledged. 1h = MCAN-SS may be clock gated by stopping both the CAN host and functional clocks.

25.7.94 DMA0CTL Register (Offset = 924h) [Reset = 00000000h]

DMA0CTL is shown in Table 25-105.

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DCANSS fixed DMA0 control and configuration register

Table 25-105. DMA0CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	BUFTTOOFST	R/W	0h	Indicates the Rx-buffer (index x) to be mapped to FE_0 (FE001) and automatically maps and Rx buffer (index x+1) to FE_1 (FE010) Valid range: Rxbuffer (0) to Rxbuffer (30) 0h = Minimum index value: 0 1Eh = Maximum index value: 30 Note: RX_FE_TTO_SEL Rx buffer index selection for FE01 cannot be 31, as Rxbuffer (index +1) maps to 32, which requires updating NDAT1 and NDAT2 value, which is not supported.
26-25	RESERVED	R	0h	Reserved
24	FEOTOSEL	R/W	0h	RX_FE_OTO_SEL is used to select the DCAN RX buffer filter event signal mapped to trigger fixed DCANSS DMA channel trigger 0h = Filter Event 0 1h = Filter Event 1
23-22	RESERVED	R	0h	Reserved
21-16	BRPMTONUM	R/W	2h	Number of TX buffer request pending (BRP) signals for multi-to-one DMA trigger mapping sequence, starting from the buffer offset number selected by TX_BRP_MTO_OFFST bits 2h = Min number for TX BRP multi-to-one DMA trigger mapping sequence is 2 20h = Max number for TX BRP multi-to-one DMA trigger mapping sequence is 32
15	RESERVED	R	0h	Reserved

Table 25-105. DMA0CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-10	BRPMTOOFST	R/W	0h	TX_BRP_MTO_OFFST selects the Tx buffer offset number for the multi-to-one round robin DMA trigger mode. 0h = TX Buffer Request Pending 0 1h = TX Buffer Request Pending 1 2h = TX Buffer Request Pending 2 3h = TX Buffer Request Pending 3 4h = TX Buffer Request Pending 4 5h = TX Buffer Request Pending 5 6h = TX Buffer Request Pending 6 7h = TX Buffer Request Pending 7 8h = TX Buffer Request Pending 8 9h = TX Buffer Request Pending 9 Ah = TX Buffer Request Pending 10 Bh = TX Buffer Request Pending 11 Ch = TX Buffer Request Pending 12 Dh = TX Buffer Request Pending 13 Eh = TX Buffer Request Pending 14 Fh = TX Buffer Request Pending 15 10h = TX Buffer Request Pending 16 11h = TX Buffer Request Pending 17 12h = TX Buffer Request Pending 18 13h = TX Buffer Request Pending 19 14h = TX Buffer Request Pending 20 15h = TX Buffer Request Pending 21 16h = TX Buffer Request Pending 22 17h = TX Buffer Request Pending 23 18h = TX Buffer Request Pending 24 19h = TX Buffer Request Pending 25 1Ah = TX Buffer Request Pending 26 1Bh = TX Buffer Request Pending 27 1Ch = TX Buffer Request Pending 28 1Dh = TX Buffer Request Pending 29 1Eh = TX Buffer Request Pending 30 1Fh = TX Buffer Request Pending 31
9	RESERVED	R	0h	Reserved

Table 25-105. DMA0CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-4	BRPOTOSEL	R/W	0h	TX_BRP_OTO_SEL is used to select the DCAN TX buffer request pending (BRP) signal mapped to trigger fixed DCANSS DMA channel trigger 0h = TX Buffer Request Pending 0 1h = TX Buffer Request Pending 1 2h = TX Buffer Request Pending 2 3h = TX Buffer Request Pending 3 4h = TX Buffer Request Pending 4 5h = TX Buffer Request Pending 5 6h = TX Buffer Request Pending 6 7h = TX Buffer Request Pending 7 8h = TX Buffer Request Pending 8 9h = TX Buffer Request Pending 9 Ah = TX Buffer Request Pending 10 Bh = TX Buffer Request Pending 11 Ch = TX Buffer Request Pending 12 Dh = TX Buffer Request Pending 13 Eh = TX Buffer Request Pending 14 Fh = TX Buffer Request Pending 15 10h = TX Buffer Request Pending 16 11h = TX Buffer Request Pending 17 12h = TX Buffer Request Pending 18 13h = TX Buffer Request Pending 19 14h = TX Buffer Request Pending 20 15h = TX Buffer Request Pending 21 16h = TX Buffer Request Pending 22 17h = TX Buffer Request Pending 23 18h = TX Buffer Request Pending 24 19h = TX Buffer Request Pending 25 1Ah = TX Buffer Request Pending 26 1Bh = TX Buffer Request Pending 27 1Ch = TX Buffer Request Pending 28 1Dh = TX Buffer Request Pending 29 1Eh = TX Buffer Request Pending 30 1Fh = TX Buffer Request Pending 31
3-2	TRIGSEL	R/W	0h	DMA trigger select bits used to select between DCAN TX one-to-one mapping, DCAN TX multi-to-one round robin mapping and DCAN Rx one-to-one mapping options 0h = DCAN TX Buffer one-to-one Tx BRP (buffer request pending) trigger to DMA channel select 1h = DCAN TX Buffer multi-to-one round robin, Tx BRP (buffer request pending) triggers to DMA channel select 2h = DCAN RX Buffer one-to-one Tx BRP (buffer request pending) trigger to DMA channel select 3h = Rx buffer two-to-one DMA trigger
1	RESERVED	R	0h	Reserved
0	TRIGEN	R/W	0h	DMA_TRIG_EN is used to enable/disable DCAN RX, TX triggers to DCANSS fixed DMA channel. <Note to design> check if this bit is needed depending on if similar functionality is enabled in the EXT_DMA aperture. 0h = DCANSS fixed DMA channel trigger is disabled. 1h = DCANSS fixed DMA channel trigger is enabled.

25.7.95 DMA1CTL Register (Offset = 92Ch) [Reset = 00000000h]

DMA1CTL is shown in Table 25-106.

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DCANSS fixed DMA1 control and configuration register

Table 25-106. DMA1CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	BUFTTOOFST	R/W	0h	Indicates the Rx-buffer (index x) to be mapped to FE_0 (FE001) and automatically maps and Rx buffer (index x+1) to FE_1 (FE010) Valid range: Rxbuffer (0) to Rxbuffer (30) 0h = Minimum index value: 0 1Eh = Maximum index value: 30 Note: RX_FE_TTO_SEL Rx buffer index selection for FE01 cannot be 31, as Rxbuffer (index +1) maps to 32, which requires updating NDAT1 and NDAT2 value, which is not supported.
26-25	RESERVED	R	0h	Reserved
24	FEOTOSEL	R/W	0h	RX_FE_OTO_SEL is used to select the DCAN RX buffer filter event signal mapped to trigger fixed DCANSS DMA channel trigger 0h = Filter Event 0 1h = Filter Event 1
23-22	RESERVED	R	0h	Reserved
21-16	BRPMTONUM	R/W	2h	Number of TX buffer request pending (BRP) signals for multi-to-one DMA trigger mapping sequence, starting from the buffer offset number selected by TX_BRP_MTO_OFFST bits 2h = Min number for TX BRP multi-to-one DMA trigger mapping sequence is 2 20h = Max number for TX BRP multi-to-one DMA trigger mapping sequence is 32
15	RESERVED	R	0h	Reserved

Table 25-106. DMA1CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-10	BRPMTOOFST	R/W	0h	TX_BRP_MTO_OFFST selects the Tx buffer offset number for the multi-to-one round robin DMA trigger mode. 0h = TX Buffer Request Pending 0 1h = TX Buffer Request Pending 1 2h = TX Buffer Request Pending 2 3h = TX Buffer Request Pending 3 4h = TX Buffer Request Pending 4 5h = TX Buffer Request Pending 5 6h = TX Buffer Request Pending 6 7h = TX Buffer Request Pending 7 8h = TX Buffer Request Pending 8 9h = TX Buffer Request Pending 9 Ah = TX Buffer Request Pending 10 Bh = TX Buffer Request Pending 11 Ch = TX Buffer Request Pending 12 Dh = TX Buffer Request Pending 13 Eh = TX Buffer Request Pending 14 Fh = TX Buffer Request Pending 15 10h = TX Buffer Request Pending 16 11h = TX Buffer Request Pending 17 12h = TX Buffer Request Pending 18 13h = TX Buffer Request Pending 19 14h = TX Buffer Request Pending 20 15h = TX Buffer Request Pending 21 16h = TX Buffer Request Pending 22 17h = TX Buffer Request Pending 23 18h = TX Buffer Request Pending 24 19h = TX Buffer Request Pending 25 1Ah = TX Buffer Request Pending 26 1Bh = TX Buffer Request Pending 27 1Ch = TX Buffer Request Pending 28 1Dh = TX Buffer Request Pending 29 1Eh = TX Buffer Request Pending 30 1Fh = TX Buffer Request Pending 31
9	RESERVED	R	0h	Reserved

Table 25-106. DMA1CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-4	BRPOTOSEL	R/W	0h	TX_BRP_OTO_SEL is used to select the DCAN TX buffer request pending (BRP) signal mapped to trigger fixed DCANSS DMA channel trigger 0h = TX Buffer Request Pending 0 1h = TX Buffer Request Pending 1 2h = TX Buffer Request Pending 2 3h = TX Buffer Request Pending 3 4h = TX Buffer Request Pending 4 5h = TX Buffer Request Pending 5 6h = TX Buffer Request Pending 6 7h = TX Buffer Request Pending 7 8h = TX Buffer Request Pending 8 9h = TX Buffer Request Pending 9 Ah = TX Buffer Request Pending 10 Bh = TX Buffer Request Pending 11 Ch = TX Buffer Request Pending 12 Dh = TX Buffer Request Pending 13 Eh = TX Buffer Request Pending 14 Fh = TX Buffer Request Pending 15 10h = TX Buffer Request Pending 16 11h = TX Buffer Request Pending 17 12h = TX Buffer Request Pending 18 13h = TX Buffer Request Pending 19 14h = TX Buffer Request Pending 20 15h = TX Buffer Request Pending 21 16h = TX Buffer Request Pending 22 17h = TX Buffer Request Pending 23 18h = TX Buffer Request Pending 24 19h = TX Buffer Request Pending 25 1Ah = TX Buffer Request Pending 26 1Bh = TX Buffer Request Pending 27 1Ch = TX Buffer Request Pending 28 1Dh = TX Buffer Request Pending 29 1Eh = TX Buffer Request Pending 30 1Fh = TX Buffer Request Pending 31
3-2	TRIGSEL	R/W	0h	DMA trigger select bits used to select between DCAN TX one-to-one mapping, DCAN TX multi-to-one round robin mapping and DCAN Rx one-to-one mapping options 0h = DCAN TX Buffer one-to-one Tx BRP (buffer request pending) trigger to DMA channel select 1h = DCAN TX Buffer multi-to-one round robin Tx BRP (buffer request pending) triggers to DMA channel select 2h = DCAN RX Buffer one-to-one Tx BRP (buffer request pending) trigger to DMA channel select 3h = Rx buffer two-to-one DMA trigger
1	RESERVED	R	0h	Reserved
0	TRIGEN	R/W	0h	DMA_TRIG_EN is used to enable/disable DCAN RX, TX triggers to DCANSS fixed DMA channel. <Note to design> check if this bit is needed depending on if similar functionality is enabled in the EXT_DMA aperture. 0h = DCANSS fixed DMA channel trigger is disabled. 1h = DCANSS fixed DMA channel trigger is enabled.

25.7.96 TTOFE0 Register (Offset = 938h) [Reset = 00000000h]

TTOFE0 is shown in Table 25-107.

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Rx buffer (index x) base address. <Internal: Absolute address within DCAN IP: 0x7938> Applicable to Rx buffer DMA two-to-one mode mapped to FE001 trigger: >> LS bits 0:1 in this MMR are reserved and read as '0' as the DCAN SRAM is 4 byte data addressable. >> Index x is selected using DMAn_CTL.RX_FE_TTO_SEL bits.

Table 25-107. TTOFE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14-2	BASEADDR	R/W	0h	FE0 Rx Buf x Base address (14:2). Address should be computed based on the 14-bit RBSA (Rx buffer start address) + offset (depending on Rx buffer element index value and data length code (DLC) for all the buffer elements before the Rx buffer element (x)) 0h = Min address offset within DCANSS SRAM: 0x0 1FFFh = Max address offset within DCANSS SRAM: 0x1fff
1-0	RESERVED	R	0h	Reserved

25.7.97 TTOFE1 Register (Offset = 948h) [Reset = 00000000h]

TTOFE1 is shown in Table 25-108.

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Rx buffer (index x+1) base address <Internal: Absolute address within DCAN IP: 0x7948> Applicable to Rx buffer DMA two-to-one mode mapped to FE010 trigger: >> LS bits 0:1 in this MMR are reserved and read as '0' as the DCAN SRAM is 4 byte data addressable. >> Index x is selected using DMAn_CTL.RX_FE_TTO_SEL bits.

Table 25-108. TTOFE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14-2	BASEADDR	R/W	0h	FE010 Rx Buf x Base adddress (14:2). Address should be compited based on the 14-bit RBSA (Rx buffer start address) + offset (depending on Rx buffer element index value and data length code (DLC) for all the buffer elements before the Rx buffer element (x+1)) 0h = Min address offset within DCANSS SRAM: 0x0 1FFFh = Max address offset within DCANSS SRAM: 0x1fff
1-0	RESERVED	R	0h	Reserved

25.7.98 TTONDAT1 Register (Offset = 950h) [Reset = 00000000h]

TTONDAT1 is shown in Table 25-109.

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Rx Buffer two-to-one DMA mode, hardware NDAT1 value register. The address of this register is programmed as the DMA source address register for moving NDAT1 value during DMA operation. This register is automatically updated on the fly depending on FE001/FE010 (Rxbuf(x)/Rxbuf(x+1)) ongoing transfer.

Table 25-109. TTONDAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NDAT1VAL	R	0h	NDAT1 value to be programmed onto MCAN.NDAT1 MMR. Automatically updated by HW. 0h = Min value = 0x0 (not bits set) 80000000h = max value = (bit 31 set) = 0x80000000

25.7.99 CLKCFG Register (Offset = 2000h) [Reset = 00000000h]

CLKCFG is shown in Table 25-110.

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Clock Configuration MMR for **DCAN**

Table 25-110. CLKCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6-5	CLKSEL	R/W	0h	DCAN clock selection 0h = No clock is selected 1h = 80Mhz host clock is selected. 2h = HFXT is selected as source 3h = Un-swallowed clock 80Mhz is selected.
4	RAMEN	R/W	0h	Ram Enable Paper spin option.
3-1	RESERVED	R	0h	Reserved
0	CLKEN	R/W	0h	0: **DCAN** clock disabled 1: **DCAN** clock enabled

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

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Last updated 10/2025